SYMPOSIUM G

Advanced Gate Dielectric Stacks on High-Mobility Semiconductors

March 28 - 31, 2005

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TUTORIAL

High-Permittivity Dielectrics and High-Mobility Semiconductors for Advanced Field Effect Transistors
Monday March 28, 2005
1:30 PM - 5:00 PM
Room 2007 (Moscone West)

This tutorial will provide an overview of recent trends and guiding principles motivating the combination of high-permittivity dielectrics and high-mobility semiconducting channel materials in nanoscale metal-oxide semiconducter (MOS) field-effect devices. The first portion of the tutorial, which will be presented by Dr. McIntyre, will review deposition of alternative gate dielectrics by CVD, ALD, and physical vapor-deposition methods. The effects of dielectric microstructure, interface structure and the phonon properties of high-k materials in controlling key MOS electrical characteristics, such as carrier mobility, will described. Compatibility of high-k dielectrics with various gate metals and novel semiconductor substrates, and prospects for "ultrahigh" dielectric materials ($k > 50$) will also be addressed. The second half of the tutorial will be presented by Dr. Uchida. Channel engineering to enhance mobility will be discussed in terms of strain effects and new materials introduction. The strain effects on carrier mobility in silicon MOSFETs will be reviewed in terms of strain directions and surface orientations. The process techniques used to induce strains will be also described. The possibilities and issues associated with introduction of new channel materials such as germanium will be also discussed.

Instructors:
Paul C. McIntyre, Stanford University
Ken Uchida, Toshiba Corporation/Stanford University

SESSION G1: Gate Dielectrics on Ge-I
Chairs: A. Dimoulas and D-L Kwong
Tuesday Morning, March 29, 2005
Room 2007 (Moscone West)

8:30 AM *G1.1
High Mobility Channel Engineering. Eugene A. Fitzgerald, Dept. of Materials Science and Engineering, MIT, Cambridge, Massachusetts.

As processing-centric methods to achieving higher-performance (lower power-delay product) in CMOS reach limits, new materials have been increasing explored as a potential solution. One of the most researched areas has been employing new materials in the channel region of the MOSFET. Using substrate engineering, we have created a plethora of channels based on Si substrates: strained Si, dual-channel strained Si-strained SiGe, tri-channel strained Si/SiGe/Si, and symmetric strained Si-strained Ge. These channels can exist on any substrate; we have demonstrated fabrication of some of these channels on OI, for example, as well as these channels directly on Si. The objective of all channel materials in our studies is to create a platform capable of high electron and high hole mobility in one material, thus optimizing for maximum performance increase in CMOS and lowest cost by embedding the performance advantage in the substrate material. We review mobility vs. field data for these channels, and connect band structure empirically to mobility improvements. To further electron mobility beyond strained Si enhancements, we will also present data verifying that III-V materials can be deposited of high quality on Si, and that engineered substrates can be made to support such III-V channel devices.

9:00 AM *G1.2
Interface Reaction of High-k Films with Germanium Substrate. Akira Toriumi, Koji Kita, Masahiro Toyama and Kentaro Kyuno; The University of Tokyo, Tokyo, Japan.

Ge CMOS with high-k films is very attractive from the viewpoint of post-Si devices with low-power and high-performance. The most important issue to focus is how to achieve a good interface quality at high-k film/Ge. In principle, it is not necessary to worry about gate dielectric films in high-k Ge FETs, since high-k films can be used instead of a very fragile GeOx film grown on Ge substrates. The interface layer at high-k film/Ge, however, is associated with GeOx growth as same as high-k/Si interface. In fact, GeOx on Ge is worse than SiOx grown on Si substrate in the high temperature process. SiN or GeN buffer layer has been actually examined for blocking the catalytic oxidation process through high-k films, but problems accompanying nitrided interface layer are the same as those in the gate stack formation of Si-CMOS. This paper describes a different approach to good high-k films/Ge interface, where a scavenging property of high-k films for GeOx is utilized. We prepared HfO2/Ge and Y2O3/Ge MIS capacitors by sputtering HfO2 or Y2O3, respectively. The results show that high-k films efficiently react with GeOx, and that a poor quality interface layer is reduced. Furthermore, we found that the reaction process reduces the top HfO2 thickness, which results in the further improvement of EOT in high-k film on Ge. Another interesting feature of high-k/Ge interface is an effect of Ge surface orientation on interface properties between (100) Ge and (111) Ge substrates. There is a long history that (100) Si substrate has been employed for the real application in Si microelectronics. In the case of Ge device application, a careful investigation is absolutely required for appropriate surface orientation of Ge. We have looked into the oxidation rate, surface roughening effects, and MIS capacitor characteristics with HfO2 dielectric film on both (111) and (100) Ge substrates. The paper reports a distinct difference of the surface chemistry and discusses an advantage of (111) Ge surface in terms of the better interface as well as of the higher performance Ge device with lower effective mass.

9:30 AM G1.3
Growth of Hafnium Oxide on Passivated Germanium(100). Sandrine Rivillon and Yves J. Chabal; Laboratory for Surface Modification, Rutgers University, Piscataway, New Jersey.

Germanium is a promising semiconductor substrate for high speed electronics due to its high mobility. The control of its surface chemistry is critical because, in contrast to silicon, it is difficult to passivate or chemically functionalize its surface. It is therefore important to establish reliable wet chemical cleaning and passivating methods, particularly for the growth of high-k dielectrics. Controlling the chemical nature of the surface is essential to achieve an abrupt interface between Ge and the high-k dielectrics, and to minimize the formation of interfacial oxide. We have investigated different methods for cleaning and passivating germanium substrates and studied the resulting surfaces using infrared absorption spectroscopy. In particular, we show that the degree of hydrogen termination and the surface morphology after HF-etching depend critically on the initial cleaning sequence. A monolayer H-termination can be achieved on Ge(100) using HF-etching after a cleaning process involving deionized water and hydrogen peroxide. This monolayer is composed of both Ge-H at 1990 cm^{-1} and Ge-H_2 at 2008 cm^{-1} similarly to H-terminated silicon (100) except for the absence of trihydride. However the same wet chemical sequence can also lead to the formation of more porous surfaces if the initial oxide is not a native oxide, but a wet chemically grown oxide. Using a transmission geometry, we have examined with FTIR the nature of the various oxides. The native oxide is characterized by a TO and LO modes at 830 and 920 cm^{-1}. This amorphous oxide is removed effectively in deionized water due to its solubility in water (up to 5.2g/l). In contrast, oxide formed by H_2O_2 is characterized by modes at 860 and 960 cm^{-1} and water can not remove this particular oxide. Finally, we can clearly observed that the initial oxide is thicker than the oxide creating by exposing a H-terminated Ge(100) wafer to room air as well as the nature may be different. In summary, we are using FTIR to study both the nature and stability of oxides and the HF-etched surfaces obtained under wet chemical process. We observe the formation of GeO_2 oxide while GeO is not present. The absence of oxide for H-terminated Ge(100) indicates that HF completely removes the oxide formed by H_2O_2. Finally, HfO_2 has been grown on clean GeO_2 and H-terminated Ge(100) and studied. The results will be compared to results obtained on Si(100).

9:45 AM G1.4
Direct Nitridation of Ge Substrates by Nitrogen Radical Source for Application to Ge MIS Structures. Tatsuro Maeda[1], Tetsuji Yasuda[1], Masayasu Nishizawa[1], Noriyuki Miyata[1], Yukinori Morita[1] and Shinichi Takagi[1,2]; [1]MIRAI, ASRC-AIST, Tsukuba, Ibaraki, Japan; [2]The University of Tokyo, Tokyo, Japan.

A Ge channel MISFET has been regarded as one of promising devices for future high-speed CMOS technology, because it offers high carrier mobilities needed for larger drive current. However, the formation of gate dielectrics is a challenging issue because of the lack in a good passivation layer of a Ge surface. Direct nitridation of Ge can be one of plausible techniques to form gate dielectrics with a clean and stable interface inside Ge substrates. Recently, we have successfully demonstrated the direct nitridation of Ge substrates using DC nitrogen plasma. However, the Ge surface was exposed to the discharge region and suffered the plasma damage. In this work, nitrogen radicals generated by remote RF plasma source was used for direct nitridation of Ge surfaces instead of DC plasma and the electrical characteristics of the fabricated Ge-MIS structures with germanium nitride layers were studied. Starting substrates were commercially available (100) oriented, n-type and p-type Ge wafers with resistivity 1.5-4.5ohm-cm. Thermal annealing for Ge surface cleaning was carried out in a UHV reaction chamber. The nitridation

was performed with nitrogen radicals generated by remote RF plasma source. Form the nitrogen plasma emission spectra, the atomic nitrogen radicals existed mainly but a small amount of other excited species were also generated. A part of confined radicals was diffused from the plasma source to the UHV process chamber through the aperture which induces the pressure difference between the two chambers. From in-situ AES analyses, we confirmed the clean Ge surface by thermal annealing in the UHV chamber and followed by direct formation of pure germanium nitride layer without including any oxygen and carbon. XPS analyses revealed that the chemical composition of the nitrided surface is estimated to be nearly Ge3N4. The thickness of Ge3N4 films can be controlled by changing the growth temperature and nitridation time. The maximum thickness of Ge3N4 films, evaluated by the spectroscopic ellipsometry, increased up to 5 nm, when grown at 500°C for 30min. Ge-MIS structures with germanium nitride were fabricated by depositing Au films to evaluate electrical characteristics. The high-frequency Cg-Vg curves with germanium nitride films after appropriate post thermal treatments indicated the formation of accumulation and inversion regions for both n- and p- type substrates. No significant hysteresis and kinks were observed in the bidirectional Cg-Vg curves, suggesting low surface states and trap states with small VFB shifts. Therefore, this direct germanium nitridation technique has a possibility to use as a gate dielectric layer for Ge-MISFETs as well as a passivation layer.

SESSION G2: Gate Dielectrics on Ge II
Chairs: S. Takagi and A. Toriumi
Tuesday Morning, March 29, 2005
Room 2007 (Moscone West)

10:30 AM *G2.1
Interface Engineering for High-k/Ge CMOS Devices. W. Bai[1], N. Lu[1], A. Ritenour[1], M. L. Lee[2], E. A. Fitzgerald[2], D. A. Antoniadis[1] and Dim-Lee Kwong[3]; [1]Microsystems Technology Laboratory, MIT, Cambridge, Massachusetts; [2]Department of Materials Science and Engineering, MIT, Cambridge, Massachusetts; [3]University of Texas at Austin, Dept of Electrical and Computer Engineering, Austin, Texas.

High-K dielectric materials are being developed for pure Ge channel CMOS devices in order to achieve low EOT and tunneling gate leakage. These materials pose unique challenges due to the complex nature of their interface with Ge, and its thermal stability and electrical properties. In this talk, the processing challenges for the fabrication of high quality, ultra-thin high-K gate stack on bulk Ge as well as epitaxial Ge-on-Si and GOI substrates will be presented. The requirement for effective pre-gate clean and robust high-K/Ge interface engineering for achieving thin EOT and improved MOS device properties will be discussed, including comparison with results obtained from high-K/Si CMOS devices.

11:00 AM G2.2
Effects of the Oxygen Precursors on the Electrical and Structural Properties of HfO_2 films grown by ALD on Ge. Sabina Spiga, Giovanna Scarel, Claudia Wiemer, Grazia Tallarida, Sandro Ferrari and Marco Fanciulli; Laboratorio Nazionale MDM-INFM, Agrate Brianza, Italy.

The growth of high dielectric constant materials (high-k) on germanium substrates has recently received a growing interest for the fabrication of future ultra-scaled devices. Different deposition techniques and substrate surface preparation before growth are currently investigated in order to improve the electrical properties of Ge-based gate dielectric stack. In this work, we grew thin (3-10 nm) HfO_2 films on (001) Ge substrates at 375 °C by atomic layer deposition (ALD). Films were grown on HF-dip Ge starting surfaces using $HfCl_4$ as hafnium source and either H_2O or O_3 as oxygen sources. The metal alkoxide complex $Hf(O^tBu)_2(mmp)_2$, which acts both as oxygen and metal source, was also used in combination with $HfCl_4$. The structural, compositional and electrical properties are strongly influenced by the choice of the precursor combination. Films grown with H_2O exhibit a local epitaxial growth, a high density of interface states and a large amount of contaminants such as chlorine and carbon. Capacitance-voltage (CV) curves show a significant frequency dispersion both in accumulation and inversion. A large hysteresis ($>$ 400 mV) is detected sweeping the gate voltage from inversion to accumulation and back. HfO_2 films grown using the precursor schemes $HfCl_4$ + $Hf(O^tBu)_2(mmp)_2$ and $HfCl_4$+O_3 are good quality insulating films with low leakage. Moreover, with respect to HfO_2 films grown with H_2O, they are smoother and more amorphous without any evidence of epitaxial growth on Ge. A very thin layer ($<$ 1 nm) is present at the HfO_2/Ge interface in films grown with the $Hf(O^tBu)_2(mmp)_2$ precursors, while a thicker interfacial layer (1.5-2 nm) is revealed in films grown with O_3. On the other hand, the HfO_2 ALD growth on Ge with O_3 is effective in reducing the impurity content (as detected by ToF-SIMS) and the interface defect density. CV curves of films grown with O_3 show a very small frequency dispersion of the accumulation capacitance (20 Hz-500 kHz) and no frequency dispersion in the inversion capacitance between 10 kHz and 500 kHz. Our results clearly indicate that precursor schemes alternative to the widely used H_2O + $HfCl_4$ are promising to obtain good quality high-k films on Ge by ALD.

11:15 AM G2.3
HfO_2 High-κ Gate Dielectrics on High Mobility Semiconductors by Atomic-Oxygen-Beam-Assisted Deposition. Athanasios Dimoulas[1], Georgia Mavrou[1], George Vellianitis[1], Evangelos Evangelou[1], Nikos Boukos[1], Michel Houssa[2], Matty Caymax[2] and Yukiko Furukawa[3]; [1]Institute of Materials Science, NCSR DEMOKRITOS, Athens, Greece; [2]IMEC, Leuven, Belgium; [3]Philips Research Leuven, Leuven, Belgium.

Germanium and GaAs MOSFETs with high-κ gate dielectric stacks present a good alternative for future high performance logic devices due to the high carrier mobility in these materials. In this work, using molecular beam deposition methodology, the native oxide on Ge is removed in-situ under UHV by thermal desorption at $\sim$ 360^{0}C. Subsequently, the Ge (100) surface is treated by combined atomic oxygen and nitrogen beams from an rf plasma source to improve the electrical quality of the interfaces. The native oxide on GaAs (100) is reduced at 400^{0}C in-situ by atomic hydrogen until a (2x4) reconstruction pattern is obtained in RHEED. After surface preparation, HfO_2 is deposited by evaporating Hf in the presence of atomic oxygen beam in a range of temperatures between 60 and 400^{0}C. HfO_2 grown directly on GaAs (100) substrates at 400^{0}C is polycrystalline, in the monoclinic phase, showing a strong preferential orientation with the (002) planes parallel to GaAs (100) as verified by XRD. XPS measurements show no evidence of oxidation of GaAs at the interface. HfO_2 films form sharp interfaces with Ge as verified by HRTEM. P-and n-type MIS devices in inversion show strong frequency dispersion and low-frequency behavior of the high-frequency (i.e 1 kHz) C-V curves which are not observed in device quality Si MIS. The origin of this effect is not well-understood at the present time. Here, we provide evidence that this behavior is more pronounced in Ge because of the high intrinsic carrier concentration n_i. By analyzing C-V and G-V data at various temperatures we show that the minority carrier response time t_R varies as $t_R \sim 1/n_i$ around room temperature [1]. Since n_i in Ge is at least 3 orders of magnitude higher compared to Si, the t_R in Ge is expected to be much shorter implying that the minority carriers are fast enough to respond at frequencies as high as 1 kHz (or higher) leading to the observed low frequency behavior in the inversion capacitance. From the accumulation capacitance at low frequency (20 Hz) the EOT was obtained and plotted as a function of the physical oxide thickness from which the interfacial thickness was estimated to be only 3 Å and the HfO_2 dielectric permittivity κ around 25. This is close to the expected bulk value and appreciably higher than the values reported for the HfO_2/Si system which typically range between 15 and 20. It is also found that HfO_2 behaves as an excellent insulator on Ge exhibiting low leakage currents. Record values were obtained in 3 nm-thick HfO_2 films which show EOT $\sim$ 7.5 Å and gate current $J_g \sim 4.5\times10^{-4}$ A/cm^2 at 1V in accumulation. [1] E.H. Nicolian and J.R. Brews, in "MOS Physics and Technology", John Wiley $ Sons, New York 1982, p. 139

11:30 AM G2.4
Atomic Layer Deposition (ALD) of High-k Dielectric Films and Metal Nitride Gate Stacks for Ge MOS Devices. Kyoungha Kim[2,1], Jin-seong Park[1], Philippe de Rouffignac[1] and Roy G. Gordon[1]; [1]Chemistry and Chemical Biology, Harvard University, Cambridge, Massachusetts; [2]Division of Engineering and Applied Sciences, Harvard University, Cambridge, Massachusetts.

Atomic layer deposition (ALD) was used to deposit a high-k dielectric layer on a Ge substrate for MOS applications. A thin Ge oxynitride layer ($\sim$1 nm) was formed using low power NH3 plasma treatment and the thickness of the oxynitride layer was controlled by the treatment time. Pr1.1Al0.9O3 and La1.1Al0.9O3 thin films were then deposited using Pr (La) tris(N,N'-diisopropylacetamidinate), trimethylaluminum and water by ALD at 290 oC. Pt electrodes were sputtered on the dielectric layer using a shadow mask to make MOS capacitors, and C-V and I-V curves were measured. Although the growth rate ($\sim$1.1 angstrom/cycle) was the same on both HF last Ge substrates and nitrided substrates, only devices with Ge oxynitride interfacial layers showed high electrical permittivity ($\sim$ 14). A thin film ($\sim$10 nm) showed low leakage current ($<$ 1x10-7 A/cm2 at 1 MV/cm, E.O.T. $\sim$ 2.9 nm), zero flat band voltage shift, and 70 mV hysteresis after post metal annealing at 350 oC. Metal (Hf, Zr, W, or Ti) nitride films were also deposited on high-k dielectric films by ALD and patterned to make metal gate stacks. The electrical properties of the MOS devices with high-k dielectric layers and metal nitride gate electrodes will be reported.

11:45 AM G2.5
Germanium Oxynitride Gate Dielectrics Prepared by Rapid Thermal Processing. Ali Khakifirooz, Andrew Ritenour, Minjoo L. Lee and Dimitri A. Antoniadis; Microsystems Technology Laboratories, Massachusetts Institute of Technology, Cambridge, Massachusetts.

Germanium oxynitride gate dielectrics are grown on 6" (100) n-type germanium wafers as well as relaxed p-type Ge layers epitaxially grown on silicon. A special "RCA-equivalent" cleaning process has been developed to minimize Ge loss during the cleaning step and to give reasonably smooth surface (Ra $\sim$ 0.2 nm). Oxidation is performed in an RTP chamber at 550°C for 30 s and in oxygen, followed by the nitridation at 600°C for 60-120 s in ammonia. From spectroscopic ellipsometry the thickness of the oxynitride layer is determined to be 50 Å with ±5 Å uniformity across the wafer and from wafer to wafer. Upon nitridation the refraction index of the film measured at 600 nm is increased from 1.5 to 1.7, indicating the formation of the oxynitride. From CV measurements the effective electrical oxide thickness is about 30 Å, corresponding to a dielectric constant of about 6.5. This is even higher than the values reported for oxynitride films grown in a furnace and with a similar process [1]. MOS capacitors made by depositing Al gates on as grown oxynitride dielectrics show a kink in the CV characteristics measured at lower frequencies. A forming gas annealing step at 400°C effectively removes this kink and reduces the surface states density. The midgap D_{it} is extracted from the conductance method to be roughly 8×10^{11}. PMOS transistors were fabricated with a TiN metal gate and show a peak effective mobility of 260 cm^2/V.s. This corresponds to 30% enhancement over p-channel Si MOSFETs. [1] S. C. Martin, L. M. Hitt, and J. J. Rosenberg, "Germanium p-channel MOSFET's with high channel mobility, transconductance, and k-value," IEEE Trans. Electron Devices, 36(11), p. 2629, 1989.

SESSION G3: Gate Dielectrics on III-V Compound Semiconductors

Chairs: R. Kwo and M. Orlowski
Tuesday Afternoon, March 29, 2005
Room 2007 (Moscone West)

1:30 PM *G3.1
High Mobility III-V Heterostructure MOSFET Technology with High-κ Gate Dielectric Stack. Matthias Passlack, Ravi Droopad, Jonathan Abrokwah and Karthik Rajagopalan; Microwave and Mixed-Signal Technologies Laboratory, Freescale Semiconductor, Inc., Tempe, Arizona.

New materials, manufacturing processes, characterization techniques, and device concepts have been developed for high mobility III-V heterostructure MOSFET applications. A broad spectrum of oxides including Ga_2O_3, SiO_x, MgO, Al_xO_y, Ti_xO_y, Ta_xO_y, Mo_xO_y, Zr_xO_y, Gd_2O_3, In_2O_3, and $LaAlO_3$ was investigated; only Ga_2O_3 was found to have the unique property of unpinning the Fermi level on GaAs. High-κ ($\kappa\cong$ 20) $Gd_xGa_{0.4-x}O_{0.6}/Ga_2O_3$ gate dielectric stacks have been manufactured on GaAs based heterostructures using molecular beams of Ga_2O, Gd, and oxygen whereas the Ga_2O and Gd beams are supplied by high temperature effusion cells. In addition to unpinning the Fermi level, the thin ($\cong$1 nm) interfacial Ga_2O_3 template provides the transition from crystalline semiconductor to amorphous oxide. Besides scanning tunneling spectroscopy, current-voltage, capacitance-voltage, and Hall measurements, a new photoluminescence intensity technique has been used for electrical characterization. Typical midgap interface state density and leakage current of high-κ MOS capacitors after post-deposition annealing are 2×10^{11} cm^{-2} eV^{-1} and 2×10^{-8} A/cm^2 at 1 MV/cm, respectively. Charge carrier injection from GaAs or an InGaAs device channel into the gate oxide has been significantly reduced by the use of AlGaAs pre-barriers. Hall mobilities of up to 5,700 cm^2/Vs have been measured in high-κ MOSFET heterostructures with InGaAs channels. A new device concept termed the "Flatband MOSFET" has been developed to take better advantage of the high electron mobility property in III-V semiconductors. Flatband MOSFETs do not require ion implantation for source and drain regions (and extensions) and provide maximum drain current (I_{max} or I_{on}) under flatband conditions at the source side of the gate electrode. Potential benefits comprise higher device performance, more device and circuit flexibility, and the ability to scale III-V devices using general two-dimensional MOSFET scaling rules well known from silicon MOSFETs. Future applications may include RF and mixed circuits for mobile, wireless, and radar products as well as heterointegration concepts in the longer term.

2:00 PM G3.2
Depletion Mode n-Channel InGaAs/GaAs MOSFET using $Ga_2O_3(Gd_2O_3)$ as a Gate Dielectric. Kou-Liang Jaw[1], Yiwen Chen[1], Pejun Tsai[1], Hung-Pin Yang[2], Pen Chang[1], J. Raynien Kwo[3], Jim Y. Chi[2] and Minghwei Hong[1]; [1]Department of Material Science Engineering, National Tsing-Hua University, Hsinchu, Taiwan; [2]Opto-Electronics & Systems Labs, Industrial Technology Research Institute, Hsinchu, Taiwan; [3]Department of Physics, National Tsing Hua University, Hsinchu, Taiwan.

GaAs-based electronic devices have advantages over Si-based devices for high-speed and high-power applications, due to an electron mobility in GaAs that is five times greater than that in Si (the electron mobility in InGaAs is even higher), the availability of semi-insulating GaAs substrates, and a higher breakdown field. The growth of $Ga_2O_3(Gd_2O_3)$ dielectric film on GaAs surface was found to give a low interfacial density of states (D_{it}), which is a key to realize credible III-V MOSFET's[1]. The related inversion-channel GaAs[2] and InGaAs/InP[3] MOSFET's as well as the highly performed depletion mode GaAs power MOSFET's[4] with hysteresis-free drain currents were demonstrated. In this paper, we report the first achievement of strong accumulation drain currents at a gate bias (V_g) larger than 3 V in a D-mode GaAs MOSFET. The D-mode n-channel GaAs MOSFET with $Ga_2O_3(Gd_2O_3)$ as the gate oxide and a 1.6 μm gate length shows a maximum output transconductance of 110 mS/mm and a drain current of 330 mA/mm. The results are comparable to the best data reported on D-mode GaAs MOSFET. Moreover, by inserting an $In_{0.15}Ga_{0.85}As$ channel layer between n-channel GaAs and the gate oxide, the transconductance has been further increased to 170 mS/mm, which is higher than a recently reported excellent InGaAs/GaAs MOSFET with an ALD grown Al_2O_3 as a gate dielectric[5]. The above two samples were grown in a mutli-chamber UHV/MBE system[1], with the structures given here: (i) an n-channel GaAs 1000Å in thickness and with a 4×10^{17} cm^{-3} doping; and (ii) an n-channel GaAs 800 Å in thickness, with a 4×10^{17} cm^{-3} doping and a second layer of $In_{0.15}Ga_{0.85}As$ 80 Å (which is immediately adjacent to the gate dielectric) in thickness and with a 4×10^{17} cm^{-3} doping. Both were grown on buffer layers of undoped GaAs 1000Å in thickness, which were epitaxially grown on semi-insulating GaAs substrates. $Ga_2O_3(Gd_2O_3)$ was in-situ deposited in a separate oxide chamber. The devices were made with planar processing steps. An oxygen implantation, instead of the mesa etching, was utilized for the device isolation. No noticeable drain current hysteresis and drift was observed in devices of both of these samples. The oxide breakdown field strength is about +6MV/cm for the positive sweep and at least -7MV/cm for the negative sweep. [1] M. Hong, et al, J. Vac. Sci. Technol. B14, 2297, 1996. [2] F. Ren, et al, IEEE Int'l Electron Devices Meeting (IEDM) Technical Digest, p.943, 1996, and also in Solid State Electronics, 41 (11), 1751, 1997. [3] F. Ren, et al, IEEE Electron Device Letters, V. 19, No. 8, 309, 1998. [4] Y. C. Wang, et al, Electronics Letters, V. 35, No. 8, 667, 1999. [5] P. D. Ye, et al, Appl. Phys. Lett. 84, 434, 2004.

2:15 PM G3.3
Growth and Characterization of High-K Epitaxial Rutile Films on GaN and AlGaN/GaN HFET. Venu Vaithyanathan[1], P. J. Hansen[2], Y. Wu[2], T. Mates[2], S. Heikman[3], R. A. York[3], U. K. Mishra[3], J. S. Speck[2], A. R. Fisher[1] and D. G. Schlom[1]; [1]Department of Materials Science and Engineering, Pennsylvania State University, University Park, Pennsylvania; [2]Materials Department, University of California, Santa Barbara, California; [3]Electrical and Computer Engineering Department, University of California, Santa Barbara, California.

TiO_2 in rutile form is the candidate high-K gate oxide investigated in this work because of the thermodynamic preditction that TiO_2 will be stable in contact with GaN. Epitaxial rutile phase titanium dioxide (TiO_2) films were grown on (0001) oriented GaN and (0001) $Al_{0.33}Ga_{0.67}N$/GaN heterostructure field effect transistor (HFET) structures by reactive molecular beam epitaxy. The phase-pure rutile films were grown at a substrate temperature of $\sim$500 ^oC in an oxygen/ozone ($\sim$15% ozone) background pressure of 2-3 $\times$ 10^{-6} Torr. *Ex − situ* x-ray diffraction revealed that the rutile films are epitaxial with rocking curve FWHMs as narrow as 0.7^o. The films are a-axis oriented out-of-plane, with the following epitaxial orientation relationship: (100) TiO_2 —— (0001) GaN(AlGaN) and [001] TiO_2 —— <11-20> GaN(AlGaN). Multipositioning was observed with three rotational twin variants in-plane (rotated from each other by 120°) and a FWHM in ϕ of $\sim$6°. Transmission electron microscopy of 50 nm thick TiO_2 films on GaN and AlGaN/GaN showed sharp interfaces with no intermixing or reaction between the oxide and semiconductor, as predicted by thermodynamics. Metal-oxide HFETs with 50 nm thick TiO_2 dielectric layers under the gate were processed and compared to HFETs without the TiO_2 dielectric layer. The dielectric constant of the TiO_2 film was $\sim$70, as compared to the bulk value of $\sim$90. The gate leakage current of the HFETs with TiO_2 was $\sim$4 $\times$ 10^{-6} mA/mm at 50 V, approximately four orders of magnitude lower than that of the HFETs with no dielectric.

2:30 PM G3.4
HfO_2 Highκ Dielectrics for GaAs Compound Semiconductor Passivation. Pen Chang[1], Wei-Jin Lee[1], Yi-Lin Huang[1], Yi-Jun Lee[1], Zhi-Kai Yang[1], Minghwei Hong[1] and J. Raynien Kwo[2]; [1]Materials Science and Engineering, Department of Materials Science and Engineering, National Tsing Hua University, Hsin Chu, Taiwan; [2]Physics, Department of Physics, National Tsing Hua University, Hsin Chu, Taiwan.

The compound semiconductor offers key advantages of high electron mobility and semi-insulating substrate, thus is anticipated to outperform Si in MIS applications. High-frequency wireless communications, high-speed computations, and microwave high power applications could be realized by devices based on MOS type related structures. The attainment of electrically and thermodynamically stable insulators for surface passivation that exhibit a low density of state (D_{it}) and low leakage current is one important challenge of compound semiconductor device processing. Remarkably, our earlier work of in-situ deposition of $Ga_2O_3(Gd_2O_3)$ for GaAs passivation has produced low D_{it} and low electrical leakage MOS diode, and was later employed as a gate dielectric to demonstrate successfully depletion-mode and enhancement-mode GaAs MOSFETs. We also discovered that using pure Gd_2O_3 (κ=14) epitaxially growing on GaAs (100) substrate showed an excellent insulting barrier for passivation. [1-3] In this work, we have extended the studies to another new high κ material HfO_2 growing on GaAs (100) substrate by the MBE method. HfO_2 films are recently used to replace SiO_2 on Si industry for 45 nm CMOS as alternative gate dielectrics. HfO_2 films were grown at various temperature in a multi-chamber MBE system in conjunction with structural and electrical characterizations including AFM, x-ray reflectivity, and HRTEM. Low electrical leakage current films of amorphous HfO_2 on GaAs(100) were attained by room temperature deposition using e-beam evaporation from the ceramic oxide sources. A very abrupt interface about one atomic layer thickness was observed by HRTEM. The leakage current density J_E of 69 Å HfO_2 film at 1 MV/cm is 10^{-5} A/cm^2, with a κ value deduced from the capacitance data at 100KHz of $\sim$14.9. Comparing to the electrical data of amorphous HfO_2 films of similar thickness on Si, the leakage current density of amorphous HfO_2 on GaAs at 1 MV/cm is about one order of magnitude higher, and the dielectric constant κ of both cases are quite comparable. Epitaxial growth of (100) cubic HfO_2 on GaAs (100) was also achieved by depositions at elevated temperature over 210øC but with rougher surface morphology. The structural order is being determined by x-ray diffraction. Extensive XPS analysis is now in progress to examine the interfacial structure. [1] M. Passlack et al, IEEE Transaction of Electron Devices, **44** (2), 214, (1997). [2] M. Hong et al, J. Crystal Growth, **175/176**, 422, (1997). [3] M. Hong et al, Science, **283**, 1897, (1999).

2:45 PM G3.5
Ferroelectric Gates for GaN and GaAs Heterostructures and Rewritable Nanofeatures Induced by Polarization Domains. Igor Stolichnov, Lisa Malin and Nava Setter; Ceramics Laboratory, Swiss Federal Institute of Technology (EPFL), Lausanne, Switzerland.

The idea of incorporation of a ferroelectric gate into a semiconductor device with high-mobility channel has been proposed about 10 years ago for memory applications, but its implementation encountered serious technological problems. In the present work we combine the concept of ferroelectric transistor with advanced technique of direct domain writing. The considered sandwich structure comprises a III-V semiconductor heterostructure with 2D electron gas and a ferroelectric layer on top of it. The ferroelectric film grown on such heterostructure can be poled in controllable way by scanning probe microscope inducing depletion or accumulation effects in the 2D gas depending on the polarity orientation. The artificially created domain arrangements can be projected onto the 2D gas provoking local depletion underneath the poled area. The idea was implemented using the GaN/AlGaN heterostructure with 2D electron gas, and a thin Pb(Zr,Ti)O3 film that played a role of ferroelectric gate. In this work we demonstrate the possibility of ferroelectric gate patterning by making rewritable domain arrangements and its impact on the charge carriers concentration and mobility in the 2D gas. GaAs-based heterostructures represent another group of materials, which look very interesting for such devices because of high 2D gas quality. However, integration of the ferroelectric layer into the GaAs structure with 2D gas close to the surface is a complicated issue. In this work we show the first results on GaAs-based systems with patterned ferroelectric gates. These results suggest that ferroelectric gates may be potentially interesting for a number of experiments and applications as a flexible and nondestructive way of making rewritable nanofeatures on low-dimensional semiconductor structures.

SESSION G4: Gate Dielectrics on Si

Chairs: A. Dimoulas and S. Guha
Tuesday Afternoon, March 29, 2005
Room 2007 (Moscone West)

3:30 PM *G4.1
Molecular Beam Epitaxy for Advanced Gate Stack Materials and Processes. Jean-Pierre Locquet[1], C. Marchiori[1], M. Sousa[1], H. Siegwart[1], D. Caimi[1], J. Fompeyrine[1], L. Pantisano[2], M. Claes[2], T. Conard[2], M. Demand[2], W. Deweerd[2], S. DeGendt[2], M. Heyns[2], M. Houssa[2], M. Aoulaiche[2], G. Lujan[2], L. Ragnarsson[2], E. Rohr[2], T. Schram[2], J. Hooker[3], Z. Rittersma[3], Y. Furukawa[3], J. W. Seo[4] and A. Dimoulas[5]; [1]IBM, Rueschlikon, Switzerland; [2]IMEC, Leuven, Belgium; [3]Philips Research Leuven, Leuven, Belgium; [4]EPFL, Lausanne, Switzerland; [5]NCSR, Athens, Greece.

The material requirements for future CMOS generations - as given by the ITRS roadmap - are very challenging. This includes a high K dielectric without a low K interfacial layer, a high mobility channel and the appropriate metal gate. With the help of two EU projects INVEST and ET4US, we are building up a molecular beam epitaxy (MBE) infrastructure to grow this material set on large area wafers that can be further processed into small scale devices. In the INVEST project, we have developed an MBE system for the growth of oxides on semiconductors. The system made by Riber follows the overall design of a production tool and is equipped with an RF atomic oxygen source, effusion cells, e-beam evaporators and a differential pumping stage. The oxide growth process starts with desorbing the initial surface oxide on the Si wafers in ultra-high vacuum and high temperature to create a clean reconstructed 2x1 surface. Using the atomic oxygen it is possible to oxidize the surface in a well controlled manner at low temperature and to grow very thin and dense SiOx layers, followed by the growth of 2-6 nm amorphous high K dielectrics. The process parameters permit to tune the interface layer from a SiOx rich to a silicide rich interface with a significant impact on the capacitance and the leakage. Initial focus is on developing an optimized growth recipe for high quality amorphous HfO2 and LaHfO3.5 films. This recipe was subsequently used to make wafers for a transistor batch that gave us the first N short channel MBE MOSFET's (100 nm) using an etched gate process flow. Some highlights of the first batch for 3nm HfO2 MOSFET are a high mobility (> 270 cm2/Vs) with a corresponding low leakage current of 2 mA/cm2). While there were some process issues for LaHfO3.5 , the 3 nm MOSFET showed very low leakage currents below 10-6 A/cm2. Interestingly all the LaHFO3.5 MOSFETs showed very low threshold voltage instabilities. In the ET4US project that has just started, the focus is on the semiconductor channel with the addition of a Si/Ge and a III/V cluster tool - provided by DCA - to the MBE infrastructure. Since most of the advanced gate stacks will be made on silicon on insulator structures (SOI), the first challenge is to grown a graded epitaxial oxide template buffer on Si that will lattice match with Ge / GaAs. So far, we have explored two materials systems, namely the (Sr, Ba)TiO3 system with Sr to Ba grading and the Sr(Ti, Hf)O3 system with a Ti to Hf grading. The second challenge is to grow a high quality semiconductor layer (Ge / GaAs) on the oxide and finally the third challenge is to produce and amorphous or epitaxial high K dielectric on the high mobility channel. Initial results will be presented.

4:00 PM G4.2
Interface Control in MBE Grown High K Dielectrics. Chiara Marchiori[1], M. Sousa[1], A. Guiller[1], J. W. Seo[2], H. Siegwart[1], D. Caimi[1], D. J. Webb[1], C. Rossel[1], R. Germann[1], J. Fompeyrine[1] and J.-P. Locquet[1]; [1]Science&Technology, IBM Research Laboratory Zurich, Rueschlikon, Switzerland; [2]IMPC, EPFL, Lausanne, Switzerland.

The materials of the high K stack for future CMOS generations, requires a very low equivalent oxide thicknesses (EOT) in a low leakage dielectric film while maintaining a maximal high mobility in the inversion channel. Today, these three objectives have not been fulfilled simultaneously. The first objective can only be reached if the transition from the clean silicon surface to the high K dielectric phase is kept under very tight control. Any interfacial SiOx monolayer will increase the EOT by more than 20% for such low EOT values. Here we use an 8 inch molecular beam epitaxy system (MBE) equipped with an RF atomic oxygen source to first create an ultrathin in-situ interfacial SiOx layer, followed by the growth of 2-8 nm amorphous HfO2 and LaHfOx films. In this paper we focus on XPS to provide a quick feedback on the interface chemistry (amount of SiOx) as well as the bulk properties (composition, oxidation state). This is also compared with information extrapolated from other analytical techniques such as ellipsometry, x-ray reflectivity and especially from electrical I-V and C-V measurements. After desorbing the initial surface oxide on the Si wafers in ultra-high vacuum and high temperature, the clean reconstructed 2x1 surface is the starting point of the growth. Using the atomic oxygen it is possible to oxidize the

surface in a well controlled manner at low temperature and to grow very thin and dense SiOx layers. The thickness and composition of this interfacial layer (IL) oxide were determined using XPS with the help of a calibration curve derived from standard SiO2 samples, with the method of the peak area ratio. Two types of IL were observed depending on the oxygen budget during growth, namely SiOx rich versus silicide rich. At low O pressure, Hf silicide phases were detected and their presence increased with temperature. The oxygen stoichiometry was estimated from the ratios between the O1s bulk peak and the Hf4f peak at a binding energy of 17eV. Electrically, these samples were characterized by a very high capacitance and high leakage. The introduction of La (Hf:La flux ratio 1:1) suppressed the silicide formation under the same conditions. The pyrochlore LaHfOx structure being more O transparent, induced the formation of an oxidized IL and significantly decreases the leakage. In contrast, at higher oxygen pressure or on an in-situ grown ultrathin SiOx layer, a siliciate interfacial layer is observed which reduced the capacitance of the structure. To confirm the scalability of the approach, we then performed a systematic pre-oxidation of the clean Si surface prior to the growth of the high K layer. Finally, from these results an optimal growth recipe was derived and then used to make long and short channel HfOx and LaHfOx MOSFET with high channel mobilities.

4:15 PM G4.3
Epitaxial Growth of Sc_2O_3 and La-based Perovskites on Silicon by Molecular Beam Epitaxy. Lisa Friedman Edge[1], Venu Vaithyanathan[1], Darrell G. Schlom[1], Dmitri O. Klenov[2] and Susanne Stemmer[2]; [1]Materials Science and Engineering, Pennsylvania State University, University Park, Pennsylvania; [2]Materials Department, University of California, Santa Barbara, California.

The continued scaling of SiO_2 in metal-oxide-semiconductor field-effect transistors (MOSFETs) is approaching its fundamental limit and in the next few years will have to be replaced with an alternative gate dielectric if Moore's law is to continue. The higher K and low density of dangling bonds that an epitaxial dielectric could offer are attractive for future generations of MOSFETs. In this work, we investigate the growth of epitaxial $LaScO_3$ and Sc_2O_3 thin films on silicon. A major challenge in the growth of alternative gate dielectrics on silicon is the formation of excessive SiO_2 at the interface between silicon and the high-K gate dielectric. One technique to prevent the formation of SiO_2 is to grow in a low temperature / kinetically-limited oxidation regime. We have investigated the oxidation kinetics of La and Sc from their elemental state to fully oxidized La_2O_3 and Sc_2O_3 in the presence of oxygen using an in situ quartz crystal microbalance (QCM). Using these parameters, we have grown epitaxial Sc_2O_3 by molecular beam epitaxy (MBE) directly on silicon. High-resolution TEM revealed a sharp Sc_2O_3 / Si interface with no discernable interfacial layer between the Sc_2O_3 thin film and silicon. Sc_2O_3 thin films grew epitaxially with a cube-on-cube orientation relationship on (111) silicon. Because of the considerable lattice mismatch (9.8 %), there was a high density of misfit dislocations at the interface between Sc_2O_3 and (111) silicon. The epitaxial $LaScO_3$ thin films were grown on (100) silicon using buffer layers of alkaline earth oxides. The epitaxial orientation relationship between the orthorhombic $LaScO_3$ and the underlying Si was (101) $LaScO_3$ // (100) Si and [010] $LaScO_3$ // [110] Si. The films were structurally characterized by RHEED during growth and four-circle XRD and high-resolution plan-view and cross-section TEM, including Z-contrast TEM after growth.

4:30 PM G4.4
The Nucleation of ALD HfO2 Films Studied by Grazing Incidence Small Angle X-ray Scattering with Synchrotron Radiation. Martin L. Green[1], Xuefa Li[2], Jin Wang[2], Andrew J. Allen[1], Jan Ilavsky[2], Anneliese Delabie[3] and Riikka Puurunen[3]; [1]Materials Science and Engineering Laboratory, NIST, Gaithersburg, Maryland; [2]Argonne National Labs, Argonne, Illinois; [3]IMEC, Leuven, Belgium.

Major efforts have been underway to identify replacements for SiO_2 or Si-O-N gate dielectrics for Si microelectronics, and several candidate materials, notably HfO_2, have been identified. Atomic layer deposition (ALD) is the leading deposition technology for these alternate gate dielectric films, but very little is known about the microstructural evolution of such films. For the gate dielectric application, the film must be continuous (coalesced and pore-free) at the minimum thickness; this will give the film maximum capacitance and therefore minimum capacitive equivalent thickness (CET). Thus, the film growth mode must be understood and carefully controlled. Using grazing incidence small angle x-ray scattering (GISAXS) we have obtained, for the first time, growth information such as nuclei island size and alignment. Such information can be used to characterize film coalescence as a function of starting substrate preparation, and allows one to establish ideal growth conditions for these critical ultrathin layers. Nuclei size is of nanometer dimensions, and therefore the synchrotron flux is needed to provide a sufficient scattering signal, to study the earliest stages of film growth and coalescence. Our sample library consists of ALD HfO_2 films with coverages in the range $0.1-10$ monolayers (equivalent), grown on either H-terminated Si or chemically oxidized Si. Using a reflectometry geometry, for example, we can observe oscillations that are indicative of regions of the film that are parallel to the substrate. This behavior is more persistent for films grown on chemical oxide than those grown on H-terminated Si. This behavior, as well as diffuse and small angle scattering observations, will be discussed at the meeting.

4:45 PM G4.5
Physical Characterization of $Hf_xTi_yO_z$ Thin Films Deposited on Si by Pulsed Injection MOCVD. Sandrine Lhostis[1], Bernard Pelissier[2], Karen Dabertrand[1], Vincent Cosnier[1], Jean-Pierre Gonchond[1], Marc Juhel[1], Kostas Giannakopoulos[3] and Guy Rolland[4]; [1]STMicroelectronics, Crolles, France; [2]LTM, Grenoble, France; [3]Electron Microscopy Laboratory, National Center for Research Demokritos, Agia Paraskevi (Athens), Greece; [4]CEA, Grenoble, France.

HfO_2 based thin films are the predicted candidates for the replacement of the gate oxide in future CMOS devices. However hafnium silicate, hafnium aluminate or even pure hafnium oxide gate will present some limits in terms of scalability for sub-1 nm EOT. We present here a study on $Hf_xTi_yO_z$ thin films. The dielectric constant of crystalline TiO_2 being around 60, higher dielectric constants than the k values of 20-25 obtained for pure HfO2 are already reported for the mixture $Hf_xTi_yO_z$[1]. The aim of this work is to get a first overview of the different crystalline phases that could be formed in the films during the deposition of hafnium titanates by pulsed injection MOCVD (AVD^{TM}) in an Aixtron tool. The regulation of the Ti/Hf ratio is obtained by varying the relative frequency of two injectors delivering separately the $Hf(O^tBu)_2(mmp)_2$ and $Ti(O^iPr)_2(mmp)_2$ precursors. 2 to 30 nm thin films have been deposited at 550°C on RCA cleaned (100) Si wafers. A higher Ti concentration on top of the films has been revealed by SIMS analysis. XRF, XPS and EELS measurements have been performed to evaluate the global Ti/Hf composition in the layers. TEM observations show that the interface between native SiO_x layer and Si is sharp indicating no diffusion of titanium down to the Si substrate. According to thermodynamic considerations, $HfTiO_4$ should be formed for a Ti/Hf ratio exceeding 0.1 [2]. This phase has not been put into evidence in this work according to grazing incidence XRD. The global crystallization state of the $Hf_xTi_yO_z$ films studied by XRD, XPS and ATR-FTIR is shifting from monoclinic HfO_2, amorphous $Hf_xTi_yO_z$ phase, anatase TiO_2 up to rutile TiO_2, when increasing the Ti/Hf ratio from pure HfO_2 to pure TiO_2 films. It is shown to be due to the particularity of the used deposition technology. We report also on the related dielectric constants extracted trough capacitance measurements as a function of the Ti/Hf ratio. The k-value of the deposited layers is found to be stable around 25-30 for a large set of Ti/Hf composition, then to increase up to 60 when the layers are highly Ti rich. However the density of interfacial charges is increasing with the TiO_2 concentration. Selection of the $Hf_xTi_yO_z$ materials leads to a compromise between high k value and low interface charge density. [1] Chen, F. Microelectronic engineering 72 (2004) 263-266 [2] Ruh, R. J.Am.Ceram.Soc. 59 (11-12) (1976) 495-499

SESSION G5: Poster Session: 1
Chairs: M. Fanciulli and P. McIntyre
Tuesday Evening, March 29, 2005
8:00 PM
Salons 8-15 (Marriott)

G5.1
High Quality Heteroepitaxial-GE Layers on SI by Multi-Step Hydrogen Annealing and Re-Growth. Ammar Munir Nayfeh[1], Chi On Chui[1], Takao Yonehara[2] and Krishna Saraswat[1]; [1]Department of Electrical Engineering, Stanford University, Stanford, California; [2]Leading-Edge Technology Development Headquarters, Canon Inc., Atsugi Kanagawa, Japan.

It is pivotal to develop new methods for heteroepitaxial Germanium (Ge) technology as Ge has been emerging as a viable candidate to augment Si for CMOS and optoelectronic applications. Ge growth on Si is hampered by the large lattice mismatch (4 percent), which results in growth that is dominated by islanding and misfit dislocations, rendering the layer not useful in device application. Misfit dislocations form at the substrate/film interface and typically terminate at the film surface as threading dislocations, thus degrading device performance. We report a novel technique to achieve high quality heteroepitaxial Ge layers on Si. The technique involves CVD growth of Ge on Si, followed by in-situ hydrogen annealing with subsequent growth and anneal steps and hence the name Multiple Hydrogen Annealing for Heteroepitaxy (MHAH). Following the first Ge growth and hydrogen anneal, the Ge surface roughness from

islanding is reduced by 90 percent. An additional CVD Ge layer is grown on the low roughness Ge layer followed by the final hydrogen annealing. From Cross Sectional Transmission Electron Microscopy (TEM), misfit dislocations are confined to the Si/Ge interface or bend parallel to this interface, rather than threading to the surface as expected in this 4 percent lattice mismatched heteroepitaxial system. XRD confirmed the epi-Ge layer is single crystal and fully relaxed. AFM indicated the final layer surface roughness is reduced to device quality, making this technique useful for fabrication of Ge based MOS devices, GOI substrates, or for the eventual integration of GaAs/Ge/Si for optoelectronics. The results are discussed in terms of reduction in the Ge diffusion barrier during hydrogen anneal, thermal stress, silicon diffusion, lattice matching, and re-crystallization.

G5.2

High Temperature Annealed $Ga_2O_3(Gd_2O_3)$/GaAs Heterostructures. Yilin Huang[1], Pen Chang[1], Zhi-Kai Yang[1], Yi-Jun Lee[2], Hsin-Yi Lee[3], Heng-Jui Liu[3], J. Raynien Kwo[2], Joseph Petra Mannaerts[1] and Minghwei Hong[1]; [1]Department of Materials Science and Engineering, National Tsing Hua University, Hsinchu, Taiwan; [2]Department of Physics, National Tsing Hua University, Hsinchu, Taiwan; [3]National Synchrotron Radiation Research Center, Hsinchu, Taiwan.

A low interfacial density of states (D_{it}) between gate dielectrics and GaAs is key for fabricating GaAs-based MOSFET's, which were realized in the growth of $Ga_2O_3(Gd_2O_3)$ dielectric films on GaAs surface[1-3]. In particular, the inversion channel devices require a high temperature annealing, which is used to activate ion implantation in the source and drain regions for ohmic contacts. A smooth gate dielectric/GaAs interface upon the high temperature annealing is necessary for ensuring the low D_{it} and maintaining high carrier mobility in the channel of the MOSFET. Previously, the rough surfaces and $Ga_2O_3(Gd_2O_3)$/GaAs interfaces during high temperature annealing were caused mainly by the hydro-oxide formation, which occurs during air exposure of the dielectric films[4]. The hydro-oxide formation has caused the oxide deterioration and more harmfully the interaction between the film and the substrate. In this work, the thermodynamic stability of $Ga_2O_3(Gd_2O_3)$, not the hydro-oxides, with GaAs has been studied by annealing the samples to high temperatures in UHV. The samples were all prepared in a multi-chamber MBE system[1]. After the oxide growth, one sample was directly heated to 780°C in the UHV system without exposing to air. Two other samples were removed from UHV and exposed to air for months, and then put back to UHV for annealing. We have demonstrated that the hydro-oxides have been greatly reduced with proper annealing in UHV. Moreover, studies using structural and morphological probing tools of x-ray reflectivity (XRR), atomic force microscopy (AFM), and cross-sectional transmission electron microscopy (TEM) have revealed that the interface between $Ga_2O_3(Gd_2O_3)$ and GaAs for all the samples remains intact with the high temperature annealing and the interfacial roughness is less than 0.2 nm, a value close to that of SiO_2-Si interface. I-V (current-voltage) and C-V (capacitance-voltage) measurements showed excellent electrical properties of the annealed $Ga_2O_3(Gd_2O_3)$/GaAs, having low D_{it}, low leakage currents (10^{-8} to 10^{-9} A/cm^2), and high dielectric constant of 15. The excellent results presented are critical for developing a high-performance inversion channel GaAs-based MOSFET. [1]M. Hong, et al, J. Vac. Sci. Technol. B, 14, 2297, 1996. [2] F. Ren, et al, IEEE Int'l Electron Devices Meeting (IEDM) Technical Digest, p.943, 1996, and also in Solid State Electronics, 41 (11), 1751, 1997. [3] Y. C. Wang, et al, Mat. Res. Soc. Symp. Proc. Vol. 573, p. 219, (1999). [4] M. Hong, et al, Appl. Phys. Lett. 76 (3), p. 312, 2000

G5.3

Jahn-Teller Term Splittings in Transition Metal and Rare Earth Elemental and Complex Oxides: A Sensitive Test for Nano-Crystallites below the Level of Detection by X-ray Diffraction. Lisa Edge[1], Charles Fulton[2], Gerald Lucovsky[2], Darrell Schlom[1], Jon-Paul Maria[2], Jan Luning[3] and Robert Nemanich[2]; [1]Penn State University, State College, Pennsylvania; [2]NC State Univ, Raleigh, North Carolina; [3]Stanford Synchrotron Radiation Laboratory, Menlo Park, California.

High-resolution x-ray absorption spectra (XAS) for transition metal (TM) elemental, and complex oxides reveal Jahn-Teller (J-T) term-split d-state features associated with local bonding distortions. In this paper, these term splittings are shown to provide a sensitive test for nano-scale crystallites that are below the level of detection by conventional x-ray diffraction (XRD). Complex oxides have been grown by reactive evaporation in UHV MBE chambers using effusion cell sources for LaScO3 and LaAlO3, and e-beam evaporation sources for HfxTi1-xO2 and ZrxTi1-xO2 with x = 0.33, 0.50 and 0.67. X-ray absorption spectra were obtained at the Stanford Synchrotron Research Laboratory (SSRL) in the spectral range from 300 to 1250 eV. J-T term-split states, ~ 0.5 to 1.5 eV, were found for the Sc L2,3 and O K1 edges in LaScO3, and La M2,3 and O K1 edges in LaAlO3. In contrast, M2,3 spectra for La in LaScO3 displayed a single d-state feature indicating a symmetric 12-fold coordination for La. Sc L2,3 J-T term splittings were obtained in as-deposited films (~25 C), and films annealed in inert ambients at 700 C and 1000 C. The threshold annealing temperature for detection of crystallites by XRD was 800 C. The Sc L2,3 edge J-T d-state term splittings, and single La M2,3 d-state feature are indicative of a crystalline structure. Spectral line-widths of L2,3 features decrease by more than 2x as the annealing temperature is increased from 700 to 1000 C. The line-width of the 5d-feature in the La M2,3 edge doesn't change with annealing, and is > 5x greater than the L2,3 features due to a short core hole life-time. Complete removal of d-state degeneracies at the six-fold Sc site is consistent with an orthorhombic distortion of the perovskite crystal structure. Term splittings of the La M2,3 and O K1 edges in as-deposited LaAlO3 films indicate a complete removal of the La 5d-state degeneracy, leading to a rhombohedral distortion of the perovskite crystal structure. Term splittings in the Ti L2,3 T2g p-states are the same in TiO2 and all Hf(Zr) complex titanate oxides. In contrast, term splittings for L2,3 Eg s-states are more sensitive to second neighbor transition metal bonding, displaying dependence on alloy composition indicative of nano-crystalline order. Complementary term splittings of the O K1 edge spectra, and shifts in valence band spectral features in ultra-violet photoemission spectroscopy are also consistent with nano-crystalline order in both as-deposited and annealed films at all compositions studied, even though crystalline phases are not reported at these compositions in equilibrium phase diagrams.

G5.4

Interfacial Study of High κ Dielectrics TiN/HfO_2/Si Gate Stack for Nano CMOS. Wei-Chin Lee[1], Chi-Hsin Chu[1], Yi-Jun Lee[1], KouLiang Jaw[1], Kuen-Yu Lee[1], C. H. Pan[2], Ya-Ling Hsu[3], Pen Chang[1], Yilin Huang[1], T. Gustafsson[4], E. Garfunkel[4], Minghwei Hong[1] and J. Raynien Kwo[3]; [1]Department of Materials Science and Engineering, National Tsing Hua University, Hsinchu, Taiwan; [2]Department of Materials Electronic and Engineering, National Tsing Hua University, Hsinchu, Taiwan; [3]Department of Physics, National Tsing Hua University, Hsinchu, Taiwan; [4]Department of Physics, Rutgers University, Piscataway, New Jersey.

The latest International Technology Roadmap for Semiconductors (ITRS) shows that the thickness of the SiO_2 gate oxide is now approaching the quantum tunneling limit ~1.0-1.5nm, and calls for identifying highκ dielectrics to replace SiO_2 in gate related applications by the year 2007 for 45 nm CMOS. However, the progress toward attaining high performance high κCMOSFET has been hampered due to the lack of good thermodynamic stability of the Si/high κdielectrics interface. Traditional film growth method such as sputtering and the manufactured preferred tool of atomic layer deposition inevitably led to formation of sub nm thick interfacial layer due to chemical reactions, thus severely limiting the outlook of reducing the equivalent oxide thickness (EOT) below 1.0 nm. We have overcome such problem by employing the MBE method to grow high κ dielectric HfO_2 films on clean Si (100) surface. The HfO_2 films were deposited from an e-beam evaporator using HfO_2 ceramic pellets as the source, thus producing bounded HfO_2 molecules arriving at the Si surface, and preventing direct exposure of the Si surface to oxygen. The oxygen partial pressure during growth is kept at about 10^{-8} torr, hence the oxidation of the Si surface can be effectively avoided. Based on extensive characterizations including RHEED, ellipsometry, x-ray reflectivity, TEM, XPS, and MEIS, we have demonstrated for the first time an atomically abrupt interface between amorphous HfO_2 film and Si free of SiO_2 or silicate formation, and the interface remains stable even after vacuum anneal up to 530°C. This abrupt high κ dielectric /Si interface achieves a significant saving of EOT to be under 1.0 nm, and implies a good possibility for interfacial engineering on the atomic scale in order to achieve a low interfacial state density D_{it} comparable to the Si/SiO_2 case. Typical 4.9 nm thick amorphous HfO_2 films showed low leakage current density ~0.4A /cm^2 at 1V, a dielectric constant κ of 20.7, and an EOT of 0.9 nm. After annealing up to 530°C, leakage current density showed substantial reduction with the removal of frequency dispersion. But when vacuum annealed at 630°C, leakage current density increases sharply. It may result from the recrystallization of the amorphous film, and causes current leakages along domain boundaries. Furthermore, self-aligned high ??MOSFET devices have been successfully fabricated using a LOCOS isolation process with a typical gate length of 2 μm. Among many candidates, TiN is widely applied as a metal gate electrode due to its high thermal stability and process compatibility. TiN films were formed by reactive sputtering from a pure Ti target through thermal nitridation in N_2 ambient. In addition, furnace anneals and rapid thermal anneals at various temperature have been carried out to test the thermal stability of TiN/HfO_2/Si gate stack, and to further improve the electrical performance.

G5.5

Thermochemistry of Fluorite and Pyrochlore Phases in HfO_2-La_2O_3(Gd_2O_3) Systems. Sergey V. Ushakov[1], Alexandra Navrotsky[1], Jean A. Tangeman[2], Katheryn B. Helean[3] and Alex Demkov[4]; [1]Thermochemistry Facility and NEAT ORU, University of California at Davis, Davis, California; [2]Containerless Research, Inc., Evanston, Illinois; [3]Sandia National Laboratory, Albuquerque, New Mexico; [4]Freescale Semiconductor, Austin, Texas.

The crystallization temperature of amorphous $Hf_2La_2O_7$ is higher than 900 °C, which is one of the properties that makes it a candidate for an advanced gate dielectric [1]. Both disordered fluorite-type and ordered pyrochlore-type phases in the HfO_2-La_2O_3 system can be obtained on crystallization of an amorphous precursor. $Hf_2La_2O_7$ can be grown epitaxially on silicon [2]. Thus, the relationship between fluorite and pyrochlore phases in the HfO_2 -La_2O_3 system and the effects of nonstoichiometry on their stability and properties are of interest. We applied containerless processing using aerodynamic levitation coupled with laser heating to prepare samples of $Hf_xLa_yO_7$ and $Hf_2Gd_2O_7$ by melt quenching. All prepared samples were crystalline. As-prepared $Hf_2Gd_2O_7$ was mostly fluorite-type, which ordered into pyrochlore on annealing at 1450 °C. As-prepared $Hf_xLa_yO_7$ was mostly pyrochlore-type with a cell parameter which increased from 10.74 to 10.87 Å with La content. Enthalpies of formation of $Hf_2La_2O_7$ and $Hf_2Gd_2O_7$ pyrochlores from binary oxides were measured as -104 ±5 kJ/mol and -54 ±5 kJ/mol using high temperature oxide melt drop solution calorimetry and found to be close to their zirconate analogues. The effect of non-stoichiometry on fluorite-pyrochlore phase stability will be discussed. [1] S.V. Ushakov, C.E. Brown, A. Navrotsky, J. Mater. Res. 19(3) 1 (2004) [2] G. Apostolopoulos, G. Vellianitis, A. Dimoulas, J.C. Hooker, T. Conard, Appl. Phys. Lett. 84(2) 260 (2004)

G5.6

Size Dependent Hall Mobility in a High Germanium Content Si0.1Ge0.9 Alloy Layer for MODFET Structure Grown by MBE. Joo-Young Lee, H.J. Kim, Dongho Cha, Filipp Baron and Kang L. Wang; Electrical Engineering, Device Research Laboratory, UCLA, Los Angeles, California.

The size dependence of Hall mobility has been investigated with van der Pauw patterns in a high germanium content Si1-XGeX (x=90%) alloy layer grown by MBE (Molecular Beam Epitaxy). Raman Spectroscopy (Ranishaw 1000 u-Raman system, Ar ion laser 514.5 nm) and AFM (Atomic Force Spectroscopy) are also employed to evaluate the residual strain and surface morphology of the epi layers, respectively. The results show an exponential increase of electron mobility at 77K as the size decreases below 1x10$\hat{4}$ um$\hat{2}$. Meanwhile, room temperature mobility increases linearly as the size decreases from 1x10$\hat{6}$ um$\hat{2}$ to 25 um$\hat{2}$. This trend suggests that the mobility of the SiGe layers is mainly limited by crystal imperfections and interface roughness, which are generated during the epitaxial growth and partial strain relaxation. The 96% of relaxation and 8.4~9.5nm of rms roughness are observed in Raman spectra and AFM images. It is thus suggested that nanoepi can be used to reduce dislocations and improve morphology for the higher mobility epi grown layers. We conclude that higher mobility can be achieved with epi layers in nanometer scale for the next generation electronic and photonic devices. Furthermore nano-epitaxial growth can be used for the integration of different lattice mismatched materials and Si.

G5.7

Crystalline and Amorphous LaAlO3 Grown on Si(001) by MBE. Sebastien Gaillard[1,2], Mario Kazzi[1], Michel Gendry[1], Laetitia Rapenne[3], Bernard Chenevier[3] and Guy Hollinger[1]; [1]Ecole Centrale de Lyon - LEOM-UMR CNRS 5512, Ecully, France; [2]ST Microelectronics, Crolles, France; [3]LMGP - ENSPG/INPG - UMR CNRS 5628, St Martin d' Heres, France.

Downscaling of CMOS devices requires for an equivalent oxide thickness (EOT) of the gate dielectric less than 1 nm as well as a low gate leakage current. LaAlO3 (LAO) perovskite oxide is a potential high-k dielectric candidate for the replacement of SiO2 in the sub-50 nm CMOS technology on Silicon. Among many possible deposition methods, Molecular Beam Epitaxy (MBE) has shown to be an adequate technique for preparing high-k dielectrics because it can produce high quality crystalline films with atomically sharp interfaces. The aim of this work is to investigate the potentiality of MBE tools (including evaporation cells and e-guns) to prepare high quality LAO films and interfaces on Silicon. In a first step, the homoepitaxial growth of LAO was demonstrated for growth temperatures higher than 500 C. LAO layers are amorphous below 500 C. Then, amorphous and crystalline LAO films were grown on p-type Si(001) substrates. We show that the compromise between the growth temperature Tg, the deposition rate, and the oxygen partial pressure controls the properties of LAO films. LAO layers directly grown on Si(001) appear made of multi single crystal domains in the 650-750 C growth temperature range, as observed by RHEED, TEM and AFM. In order to improve the quality of the LAO crystalline layers, various La-Si and Al-Si epitaxial atomic layers as intermediate buffers between LAO and Si(001) have also been investigated and optimized. Finally, several factors which influence the quality of the high-k oxides, such as the thermodynamical stability of the oxide-silicon interface, the growth of interfacial SiO2 and the layer's microstructure, were studied, using a large range of in-situ and ex-situ characterization techniques, such as XPS, AFM, TEM, RBS, and ellipsometry.

G5.8

New Tailored Precursors for the MOCVD of Group IVB Metal Oxides: High-k Application. Reji Thomas[1], Peter Ehrhart[1], Raghunandan Bhakta[2], Urmila Patil[2], Anjana Devi[2] and Rainer Waser[1]; [1]IFF-Institut for Festkorperforschung and CNI-Center for Nanoelectronic Systems for Information Technology, Forschungszentrum, Juelich, Germany; [2]Anorganische Chemie II, Ruhr-Universitat Bochum, Bochum, Germany.

Imminent replacement of SiO_2 gate oxide in the MOSFET is predicted by the ITRS roadmap with a high-k (k>3.9) material in near future to cope up with continuing scaling of integrated circuits. Among many probable candidates, group IVB metal oxides, like ZrO_2 and HfO_2 are considered for gate oxide applications and hence deposition of these materials with a industry friendly, high throughput, MOCVD reactor and fine tuned new precursors are of technological importance. Precursor development was performed on the line of chemical and thermal stability without increasing the vaporization temperature, to have deposition at lower temperature without much carbon content in the grown films. Present work introduces a new type of precursor, which is similarly applicable for all Group-IVB metals: beta ketoesters were combined with alkoxides of Ti, Zr and Hf resulting in mononuclear $Ti(O^iPr)_2$ $(tbaoac)_2$[1], $Zr(O^iPr)_2$ $(tbaoac)_2$[2], $Hf(O^iPr)_2$ $(tbaoac)_2$ [3] precursors. The properties of these precursors are compared to commercial precursors for the examples: $Ti(O^iPr)_2$ $(thd)_2$ and $Hf(OBu^t)_2$ $(dmae)_2$. Depositions were performed in a multi-wafer AIXTRON 2600G3 reactor using liquid injection of 0.05molar precursor solutions. Highest efficiency obtained with the new Ti- precursor was par with the standard thd precursor, but remarkably at a lower temperature, thus the prospect of low temperature deposition is bright. Compared to the new Ti-precursor Zr and Hf showed a reduction in the efficiency, but still showed a reasonable deposition at lower temperature and peaked in the same temperature range, thus allowing the mixed oxide deposition among themselves. X-ray reflectance and AFM showed good smoothness with a surface roughness $~0.3nm. Density of the film was lower in the case of as-deposited films, but improved greatly after post-deposition annealing. Electrical properties of ultra-thin films on Si(100) was studied in terms of Capacitance–Voltage and Current-Voltage characteristics. Interface charge density (D_{it}), Flat band voltage (V_{fb}) , Equivalent oxide thickness (EOT) were deduced from the high frequency C-V characteristics. Finally, leakage current density of these three films were shown as a function of EOT and compared with the corresponding SiO_2 films. References 1.R.Bhakta, R.Thomas, F.Hipler, H.Bettinger, J.Muller, P.Ehrhart and A. Devi, J. Mat. Chem, 14, 3231 - 3238(2004). 2.R. Thomas, S.Regnery, P.Ehrhart, R.Waser, U.Patil, R.Bhakta and A.Devi: Ferroelectrics (accepted, 2004). 3.A.Baunemann, R. Thomas, R.Becker, M.Winter, R.A. Fischer, P.Ehrhart, R.Waser, and A.Devi, Chem Comm, 1601-1602 (2004).

G5.9

Analysis of Leakage Current in Sputter-deposited HfSiON Films with High Hf and N Concentrations. Masahiro Koike, Tsunehiro Ino, Yuichiro Mitani and Akira Nishiyama; Advanced LSI Tech. Lab., Corporate R&D Center, Toshiba, Kawasaki, Japan.

HfSiON is a promising gate insulator for application in next-generation LSIs. We have previously reported that films with high Hf and high N contents (Hf/(Hf+Si) ratio~80%, [N]>~20at.%) exhibited high dielectric constant (~25) for a silicate, high thermal stability (>1000°C), and high immunity to boron penetration in ultra-thin films (EOT~0.6nm) [1]. Besides, it has been revealed from RBS, XPS, and REELS measurements that this material consists of Hf-N bonds forming insulating Hf_3N_4 or its alloy with HfO_2; however, the effect of Hf-N bonds on the leakage currents in the films has yet to be clarified. In this study, we investigated the leakage current in HfSiON containing high Hf and high N concentrations using Metal-Insulator-Metal (MIM) capacitors with thick films (~100nm). The use of the thick dielectric films allows us to avoid the influence of an interfacial layer (IL) between HfSiON film and Si substrate on the leakage currents, and to simplify the determination of the electric field. The films were deposited on n^+Si(100) or HfSi(~5nm)/n^+Si(100) substrates by the co-sputtering of Hf and Si in $O_2/N_2/Ar$ ambient. The Hf/(Hf+Si) ratio was set to 80%, and the [N] were 0, 10, 20, and 35at.%. Various metals with different work functions (Al, TiN, Mo, and Au) were deposited on the film as the

gate electrodes. These different metals enable us to examine the effect of the different work functions on the leakage current. We measured the IV characteristics at various temperatures (20-473K) and in a wide range of voltage (-100~100V). Due to the increase of [N] from 10 to 20at.%, the abrupt increase of the leakage current was observed, coinciding with the Hf-N formation inside the film [1]. In the films with Hf-N bonds, Poole-Frenkel (P-F) plots of the IV characteristics at high temperatures clearly showed the P-F effect saturation [2]. The trap level obtained from these plots was ~0.9eV, and remained unchanged with further increase in [N]. Since leakage currents are extremely sensitive to work functions of electrodes for the quantum mechanical tunneling, they should be different by several orders of magnitude if this is the case; however, the IV characteristics for the different electrode metals were almost the same, even at low temperatures. For this reason, we conclude that the major conduction mechanism of the sputter-deposited HfSiON films with high Hf and high N concentrations is bulk limited current: P-F conduction at high temperatures and trap assisted tunneling at low temperatures. [1] M. Koike *etal.*, IEDM Tech. Dig. 107 (2003). [2] W. R. Harrell and J. Frey, Thin Solid Films, **352**, 195 (1999).

G5.10

Paramagnetic Centers in Hafnium Oxide Films on Silicon.
Jason T. Ryan[1], Jason P. Campbell[1], Thomas G. Pribicko[1], Patrick M. Lenahan[1], John F. Conley[2] and Wilman Tsai[3]; [1]Engineering Science, Pennsylvania State University, University Park, Pennsylvania; [2]Sharp Labs, Camas, Washington; [3]Intel, Santa Clara, California.

We have investigated paramagnetic defects in hafnium oxide films prepared under a fairly wide variety of processing parameters; most films were deposited with atomic layer deposition. Deposition took place on both hydrogen terminated silicon and on silicon substrates upon which a thin chemical oxide had previously been grown. In all samples, we observe Si/dielectric interface defects similar to the Si/SiO_2 interface P_b centers. However, we note differences between the g tensors of defects observed in hydrogen terminated silicon substrate samples and those observed on the thin chemical oxide/silicon substrate samples. In hydrogen terminated substrate samples we consistently observe shifts in the g perpendicular component of the g tensor toward higher values than those found in Si/SiO_2 structures. This is not necessarily the case in hafnium oxides films deposited upon very thin SiO_2 films on silicon. We also observe several paramagnetic centers in the dielectrics themselves. As previously reported,[1] we have observed a likely O_2^- center. In addition, in some samples we observe a narrow ESR spectra with zero crossing g values very close to that of the free-electron g = 2.001 to 2.003. The density of these paramagnetic defects are strongly processing dependent. We speculate that these centers are within the dielectric but very near the silicon substrate, and likely involve an unpaired electron on a silicon atom in the oxide. [1] A. Y. Kang, P. M. Lenahan, and J. F. Conley, Jr., Appl. Phys. Lett. **83**, 3407 (2003). Work at Penn State was supported by the Semiconductor Research Corporation through Intel Corporation Funding.

G5.11

First Principles Based Kinetic Monte Carlo Modeling of the HfO2 Film Roughness in an ALD Process.
Inna Iskandarova[1], Elena Rykova[1], Andrey Knizhnik[1], Stanislav Umanskii[1], Alexander Bagatur'yants[1], Boris Potapkin[1] and Mattew Stoker[2]; [1]KINTECH Ltd, Moscow, Russian Federation; [2]Freescale Semiconductor, Tempe, Arizona.

The roughness of a hafnia film deposited by atomic layer deposition (ALD) is studied as a function of the deposition conditions using a kinetic lattice Monte Carlo (KLMC) model and quantum-chemical calculations of elementary surface reactions. The reduced chemical mechanism of HfO2 film growth for the KLMC model was obtained from the detailed kinetic mechanism of hafnia ALD proposed previously [1]. The kinetic parameters of the diffusion processes on the hafnia surface that can affect the film roughness were determined on the basis of first-principles calculations. It is shown that proton hopping along oxygen rows on the hafnia surface is characterized by a small diffusion barrier of about 15 kcal/mol. Therefore, 2D diffusion on the hydroxylated HfO2 surface is fast. The adsorbed HfCl4 precursors are extremely mobile on the oxide surface, due to the small diffusion barrier (about 8 kcal/mol), while chemisorbed HfClx metal groups are virtually immobile at low temperatures, because the diffusion barrier is large (> 35 kcal/mol). Based on these results the KLMC model of HfO2 film growth was extended to describe the film roughness at low temperatures T < 400C. This model shows that the HfO2 film roughness weakly depends on temperature for T < 300C and increases as about L̂0.4 with film thickness L. A comparison of the film roughness for ALD and PVD deposition techniques is also discussed. [1] M. Deminsky, A. Knizhnik, I. Belov, et al,, Surf. Sci. 549 (2004) 67

G5.12

Abstract Withdrawn

G5.13

Al_2O_3 Dielectric Thin Films Fabricated by Single and Double Temperature Atomic Layer Deposition.
Salvador Duenas[1], Helena Castan[1], Hector Garcia[1], Juan Barbolla[1], Kaupo Kukli[2] and Jann Aarik[3]; [1]Electronica, Universidad De Valladolid, Valladolid, Valladolid, Spain; [2]Institute of Experimental Physics and Technology, Tartu, Estonia; [3]Institute of Physics, Tartu, Estonia.

This work present a comparative electrical characterization of metal-insulator-semiconductor (MIS) structures fabricated single and double temperature atomic layer deposition atomic layer deposited (ALD) Al_2O_3 dielectric thin films on silicon substrates. The interface states as well as defects inside the insulator bulk were measured by using capacitance-voltage (C-V), deep level transient spectroscopy (DLTS) and conductance-transient (G-t) techniques. The Al_2O_3 films were deposited using AlCl3 and H2O as the precursors. Single temperature ALD samples were grown by varying growth temperatures between 300 and 800 C, whereas thickness ranged between 2.5 and 6.2 nm. Some Al_2O_3 films (Tabel 1) were deposited, however, on a buffer layer that was grown in the same process by using 15 ALD cycles at 300 C. Afterwards, a second layer was grown at higher temperatures ranging from 400 to 800 C. A description of the fabricated samples is included in Table I. The thickness values of the films deposited for electrical measurements ranged from 2.5 to 8 nm. Potential advantages of using two growing temperatures consist on the fact that the very first ALD cycles define the dielectric-semiconductor interface quality. An upper layer is grown at higher ALD temperature in order to improve the bulk dielectric properties. These films were too thin for reliable composition analysis. However EPMA measurements performed for thicker films grown under similar conditions demonstrated that the concentration of residual chlorine was 2-3 atomic % in the Al2O3 films grown at 270-365 C and below 1 atomic % in the films grown at 470 C and higher temperatures. The experimental results show that the sample T991 (15 cycles at 300 C-120 cycles at 500 C) shows the best properties: near zero flat band voltage shift and hysteresis in C-V curves and the lowest interface state ($1x10^{11}$ $cm^{-2}eV^{-1}$) and DIGS (1.4 $x10^{11}$ $cm^{-2}eV^{-1}$). In contrast, samples T965 and T966 shows the poorest results in terms of interface states ($2x10^{11}$ $cm^{-2}eV^{-1}$) and DIGS ($3x10^{11}$ $cm^{-2}eV^{-1}$). In these samples, the only layer or the upper one, respectively, were grown at the highest temperature (800 C). That suggests to us that using very high temperatures yield defective dielectric films. Moreover, sample T965 shows the maximum flat band voltage shift (1 V). More detailed experimental results and discussion will be presented during the conference.

G5.14

Design and Material Characterization of a Complimentary Fowler-Nordheim Tunneling Transistor.
Lit Ho Chong, Kanad Mallik and C. H. De Groot; School of Electronics and Computer Science, University of Southampton, Southampton, United Kingdom.

The downscaling of MOSFETs is facing its fundamental limit due to quantum mechanical and short channel effects. One of the approach to the problem is to replace the MOSFET with a new type of device. We propose a new field effect transistor, the vertical metal insulator semiconductor tunnel transistor (VMISTT) which is a modified version of the metal oxide tunneling transistor (MOTT). The principle of operating of the device is based on the Fowler Nordheim Tunneling of carriers through an insulating layer, with the probability of the tunneling being modulated by the gate electrode. The main advantages of MOTT are scalability to nanoscale, high speed, simple fabrication process and elimination of short channel effects. VMISTT is different from MOTT in two important aspects. First, the metallic source in MOTT is replaced by doped silicon. By choosing a suitable tunnel insulator and metal drain, it is possible to make both n-type and p-type devices and hence complimentary devices. Secondly, the vertical structure will allow better control on material growth and device processing. The tunnel insulator can be grown by conventional process such as evaporation followed by thermal oxidation. This will help to reduce the leakage current and hence enhance the performance of the device. Subsequent processing can continue along the same lines as the vertical MOSFET's with the gate oxide replaced by a high-k dielectric. We have grown TiO_2 layers as the tunnel insulator by oxidizing 7 and 10 nm thick Ti metal films vacuum-evaporated on silicon substrates. MOS capacitors were fabricated to characterize and optimize the tunnel insulator. TiO_2 is a suitable candidate for tunnel insulator as its band off-set is approximately equal for electrons from the conduction band and holes in the valence band. The quality of the oxide films show variation, depending on the oxidation temperatures in the range of 450-550C. From current-voltage and capacitance-voltage techniques, the leakage current through the oxide is shown to decrease as the oxidation temperature increases. The dielectric constants of the oxides are in the range of 20 to 40.

Fowler-Nordheim tunneling is observed clearly at room temperature at bias voltage of 2V and above and a barrier height of 0.4eV is extracted. Leakage currents present are due to Schottky barrier emission at room temperature, and hopping at liquid nitrogen temperature. Also, the variation in Fowler-Nordheim tunneling with metal work function will be shown experimentally and simulations of the operation of the new device will be discussed.

G5.15
ALD Grown ZrO2/TiO2 Nanolaminate Layers for High-k Gate Dielectric Applications. TaeKwan Oh, Daekyun Jeong and Jiyoung Kim; Kookmin University, Seoul, South Korea.

SiO2 as a dielectric of gate structure for CMOS has been facing the scaling limitation due to direct tunneling current and reliability problems. There are several candidate dielectrics as alternative gate dielectrics such as HfO2, ZrO2, TiO2, ZrSiO4, etc. Even though TiO2 has much higher dielectric constant than SiO2 and ZrO2, it has low band gap about 3-4 eV and poor thermal stability, which results in TiSi metal compound. On the other hand, ZrO2 shows better thermal stability and higher band-offset which results in smaller leakage current. In order to improve thermal stability and electrical properties for gate dielectric applications, we investigate characteristics of nano-laminate structured ZrO2 and TiO2 thin films grown by atomic layer deposition (ALD) using a metal-organic precursors, zirconium t-butoxide and titanium-isopropoxide. At the same time, we used oxidizer with water (H2O). The multilayer films have higher capacitance and lower leakage current than ZrO2 single layer. When post-deposition annealing was performed at 500 °C, multilayer thin films increase the capacitance and reduce the leakage current. These results may come from through formation and crystallization of ZrTiO4 layer which results from alloying of ZrO2 and TiO2 layers. The electrical characteristics of the nanolaminate structure capacitors will be discussed based on C-V and I-V behaviors. At the same time, the materials characteristics will be also discussed based on cross-sectional TEM and AES (Auger-Electron Spectroscopy) results.

G5.16
Valence and Conduction Carrier Effective Masses and Optical Properties of Three Phases of Zirconia. Luisa M. R. Scolfaro[1], A. T. Lino[1], J. C. Garcia[1], V. N. Freire[2], G. A. Farias[2] and E. F. da Silva[3]; [1]Materials Science, Physics Institute, University of Sao Paulo, Sao Paulo, Brazil; [2]Physics Department, Federal University of Ceara, Fortaleza, Brazil; [3]Physics Department, Federal University of Pernambuco, Recife, Brazil.

Zirconia (ZrO2) is one of the most important high-dielectric constant materials for silicon dioxide replacement due to the shrinkage of the gate oxide thickness to less than 10 nm. Recently, it was shown the possibility of the existence of the monoclinic, tetragonal, and cubic phases in ZrO2 films deposited on fused silica due to annealing at different temperatures. The crystalline structure of the gate oxide after annealing processes is a key issue for the device operation. Some results based on first principle calculations of the structural and optical properties of ZrO2 were already published, but without either taking into account relativistic effects or explicitly presenting values for the ZrO2 carrier effective masses, which are fundamental to the modeling of tunneling currents through floating gate dielectric memory devices with ZrO2 as the tunneling oxide, for example. In this work, we present state of the art full-relativistic calculations of optical properties derived from electronic structure, e.g. dielectric function, refractive index, reflectance, as well as the carrier effective masses of ZrO2 in the monoclinic, tetragonal and cubic phases. We obtain the conduction- and valence-band effective masses in the most important symmetry directions, which are shown to be highly anisotropic. Relativistic effects are demonstrated to be important for a correct evaluation of the effective masses values and the detailed structure of the frequency dependent dielectric function. Our results compare well with the experimental findings.

G5.17
Interface Oxides in Ozone-Based ALD Grown High-k Dielectric Layers on Si. Wesley R. Nieveen[1], Yoshi Senzaki[2] and Hood Chatham[2]; [1]Evans Analytical Group, Sunnyvale, California; [2]Aviza Technology, Scotts Valley, California.

There has been great interest and considerable effort in understanding the formation and growth of interfacial oxide layers between the Si substrate and deposited high-k dielectric layers. Under certain conditions a SiO_2-like layer is formed under an HfO_2 layer, while in other circumstances and conditions, almost no interfacial layer is formed with deposition of HfSiON. Intermediate cases of layers of apparent Si-rich silicates have been suggested as interface layers in the deposition of Hf silicates. In any event, there is a need to know what kind of interface layer (if any) has formed, how thick is it, what is its nominal composition, and under what conditions of substrate pretreatment, deposition conditions, post-deposition treatments, etc. cause a specific type of interface layer to form. Knowledge of these interface layer properties is fundamental to device performance where the total gate dielectric constant is a function of whether the interface layer is a lower k, SiO_2 type material or a higher k, Si-rich high-k silicate. In this work, we report on the formation and analysis of interface layers from the deposition and treatment of ALD deposited hafnium oxide and hafnium silicate films on Si. ALD films have been grown on HF-last treated Si substrates using liquid metal-organic precursors and ozone. HfO_2 was deposited using TEMAHf and hafnium silicate was deposited using a novel precursor co-injection of TEMAHf/Si mixed vapor in an ALD mode (ref: J. Vac. Sci. Technol. A. vol.22, p.1175, 2004). It is known that H_2O-based HfO_2 ALD processes from an inorganic $HfCl_4$ precursor suffers from discontinuous 'island' growth on a hydrophobic surface at the nucleation stage. In the ozone based ALD using the metal amide precursor in the present study, no such discontinuity was observed by cross section TEM analysis for $12\AA$ HfO_2 grown on HF-last Si substrates while approximately $10\AA$ of interface layer was grown. This feature helps to scale high-k dielectric layers to meet sub-65nm node requirements for advanced gate stacks. Characterization and analysis of the films and the interface layer have been examined using XPS, TEM, RBS, and ellipsometry. Differentiating between a Si-rich silicate interface layer and the HfO_2 or silicate dielectric layer compared to the more straightforward SiO_2 -HfO_2 case is examined.

G5.18
Gd_2O_3Gate Dielectric Grown on n-type GaN by Pulse Electron Beam Deposition. Christian Mion and John Muth; ECE, North Carolina State University, Raleigh, North Carolina.

We report on a novel growth technique for the deposition of Gd_2O_3 (5.3 eV) on n-GaN (3.4 eV) at relatively low temperatures. Gd_2O_3 thin films approximately 100 nm thick were grown on n-GaN by pulse electron deposition (PED). XRD on films grown at 650 °C revealed that the monoclinic phase (-201) coexists with the cubic phase (111). By lowering the growth temperature to 450 °C, XRD shows that Gd_2O_3//GaN is highly oriented cubic (111). The effect of the temperature on the epitaxial relationship between the film and the underlying GaN layer is addressed. 5x5 um AFM scans demonstrate an excellent rms surface roughness of 1.7nm whereas the rms surface roughness of the underlying GaN layer is measured to be 1.5nm. In addition, similar results are obtained for the growth of Gd_2O_3 on $Al_{30}Ga_{70}N$. At low biases the films were insulating, but an exponential increase of leakage current was observed that was attributed to the relatively small band offset between the Gd_2O_3 and the wide band gap semiconductor. CV measurements for the cubic phase films grown at 450 °C showed low hysteresis. The very low surface roughness and conformal nature of the deposition with the preliminary electrical results indicate that pulsed electron beam deposition is a viable means to explore the formation of novel gate dielectrics on wide band gap semiconductors.

G5.19
Thermal Desorption of Bulk Trapped Hydrogen in HfO2/Si Structures. Vaishali Ukirde, ChangDuk Lim and Mohamed El Bouanani; University of North Texas, Denton, Texas.

Hydrogen plays major role in semiconductor technology, due to its pervasiveness in a variety of processes such as deposition and post annealing of electronic structures. Therefore, it has become increasingly important to better understand the properties and behavior like trapping and release of hydrogen in semiconductor in order to improve electronic performance of the structures. Hydrogen is known to have most ambivalent (both beneficial and harmful effects) behavior in MOS devices. Trap transformations under annealing treatments in hydrogen ambient is known to be highly efficient in improving the device characteristics by passivating defects at the SiO2/Si interface. Comparable behavior is observed in the high-? dielectrics based Metal-Oxide-Semiconductor (MOS) structures. Despite wealth of electrical knowledge there is little direct information about the actual location and concentration of hydrogen and effects under hydrogen annealing in high-? dielectrics based MOS devices. The effect of processing ambient and annealing time on the hydrogen trapping and release will be reported. Elastic Recoil Detection Analysis was used to characterize the evolution of hydrogen in the bulk of oxygen pre-processed HfO2/Si structures during annealing in Forming Gas. Thermal desorption study of hydrogen from HfO2/Si structures in vacuum will be presented. Acknowledgements: This work is supported by the Texas Advanced Technology Program (*) Corresponding Author: M. El Bouanani, Phone: (940) 369-8109, E-mail: bouanani@unt.edu

G5.20
Electrical Properties of HfO_2/SiO_x, HfO_2/SiO_2 and HfO_2/SiON Stacks on Si as an Alternate High-k Gate Oxide Material. Reji Thomas[1], Eduard Rije[2], Peter Ehrhart[1], Siegfried Mantl[2] and Rainer Waser[1]; [1]IFF-Institut for Festkorperforschung and

CNI-Center for Nanoelectronic Systems for Information Technology, Forschungszentrum, Juelich, Germany; [2]ISG-Institut for Schichten und Grezflachen and CNI-Center for Nanoelectronic Systems for Information Technology, Forchungszentrum, Juelich, Germany.

The implementation of high-k materials into CMOS process flow presents a lot of challenges for future ULSI. HfO_2 has high potential for this kind of applications due to its large energy-band gap, high-dielectric constant and compatibility with conventional CMOS processes because of the thermal stability with under-laying Si substrate and overlaying poly-silicon gate electrode. In the present report ultra-thin HfO_2 thin films were prepared on three types of p-type Si(100); i) native oxide, ii) with thermally grown SiON and iii) IMEC cleaned Si with stable SiO_2 by pulsed metal organic chemical vapor deposition (MOCVD). The MOCVD system consist of an AIXTRON 2600G3 planetary reactor and a liquid-delivery TRIJET vaporizer. The precursor used was hafnium tert-butoxide dimethyl-amino-ethoxide $[Hf(OBu^t)_2(dmae)_2$, dmae= $OCH_2CH_2NMe_2]$ dissolved in octane to make a 0.05 molar solution. Deposition characteristics are discussed in terms of growth rate, film density, crystal structure and surface morphology as a function of temperature. In addition, influences of different precursors and different solvents on the film properties are considered. Electrical properties of the films in terms of the capacitance-voltage and current-voltage were extensively studied for metal-insulator-semiconductor configurations. Annealing of the as-deposited films and annealing after the deposition of the top-electrode were systematically analyzed for two different electrode deposition methods: sputtering and thermal evaporation. Pre-annealing (before metallization) was found necessary for the films deposited below 500°C, and post-annealing (after electrode deposition) was found necessary for all films for better C-V and I-V behavior. Additionally top-electrode patterning, shadow mask, lift-off and ion-beam etching, were also found to affect the electrical properties. Top electrode material influence on the electrical properties will be discussed for three different electrode materials, namely platinum, TaN and TaSiN. C-V and I-V characteristics of selected samples will be evaluated by measuring the interface density, equivalent oxide thickness (EOT), flatband voltage and current density. Finally, a comparison will be made between SiO_2 gate oxide and the present HfO_2 gate oxide in terms of the EOT and leakage current density.

G5.21
Electrical Characterization of Al_2O_3/HfO_2 Gate Oxide about the Various Thickness of Al_2O_3 Deposited by Atomic Layer Deposition. Lee Sangtae[1], Kim Inhoe[1], Park Myungjin[1], Bae Choelhwyi[2] and Jeon Hyeongtag[1]; [1]Division of Materials Science & Engineering, Hanyang University, Seoul, South Korea; [2]System LSI division, Samsung Electronics, Seoul, South Korea.

One of the major issues of metal-oxide-semiconductor field effect transistors is the gate dielectric application of high dielectric constant (high-k) materials with an equivalent oxide thickness (EOT) of SiO_2 below 2nm in order to suppress the gate leakage current within an allowable level. Among the various high-k dielectric materials, Al_2O_3 and HfO_2 are mainly studied with the alternative materials of the SiO_2. Al_2O_3 exhibits a large band gap (~8.8 eV), high field strength, excellent thermal stability, and large band offsets with silicon substrate. And another material is HfO_2 because of its high dielectric constant (25~30), high density (9.68 g/cm^3), and large band gap (~5.68 eV). However, HfO_2 has problems such as the formation of undesired interfacial layer and crystallization at temperatures less than 500 °C. Interfacial layer is composed with the silicate mainly and it causes lowering of capacitance. According to earlier reports, Al_2O_3 reduced a leakage current and prevented a diffusion of hydrogen and oxygen to silicon substrate because it has an amorphous structure. For this reason, we deposited Al_2O_3 prior to the HfO_2 deposition. In this study, we deposited HfO_2 on the top of various thicknesses of Al_2O_3 by atomic layer deposition method and formed the Pt electrode. We investigated the effect of Al_2O_3 thickness on Al_2O_3/HfO_2 gate dielectric structure by X-ray photoelectron spectroscope, high-resolution transmission electron microscope, and Auger electron spectroscope, and we analyzed the electrical properties of Al_2O_3/HfO_2 films depending on the various thickness of Al_2O_3. The electrical properties including EOT, flatband voltage shift, dielectric constant, interface trap density and leakage current were calculated by capacitance-voltage, and current-voltage measurements.

G5.22
Formation of Epitaxial Cobalt Germanide Co5Ge7 on Ge (100) Surface by Reactive Deposition and Solid Phase Epitaxy in in-situ Ultra-High-Vacuum TEM. Haiping Sun[1], Yan Bin Chen[1], Dong Zhi Chi[2], R Nath[2], Yong Lim Foo[2] and Xiaoqing Pan[1]; [1]University of Michigan, Ann Arbor, Michigan; [2]Institute of Materials Research and Engineering, Singapore, Singapore.

To meet the sub-45nm technology requirements, germanium (Ge) is recently considered as one of the new materials to replace Si substrate to fabricate advanced high speed CMOS, because of its high carrier mobility and excellent compatibility with high-k dielectrics. Consequently, metal germanides will reasonably be considered as electrode contact materials in the future Ge-based devices as well. Similar to the contact applications in Si-based microelectronics, epitaxial metal germanides with low electronic resistivity and high thermal stability are preferred. Growth conditions are important factors that determine the phase formation, morphology and crystal quality of the epitaxial film. In this work, two approaches were used to study the reaction of Co with Ge (001) surface in a JEOL-2010 TEM that is modified for in-situ deposition of materials in ultra high vacuum. One is solid state epitaxy i.e. deposit Co on Ge surface at room temperature and then anneal it at higher temperature; the other is reactive deposition, i.e. deposit Co on Ge at elevated temperature to ensure immediate alloy phase formation during the deposition. The nucleation and growth of the cobalt germanide phase during the deposition/reaction processes in the both experiments were recorded in real time. The formation of Co5Ge7 phase is identified by electron diffraction analysis in both experiments but reaction mechanisms as well as the morphology formed are significantly different.

G5.23
III-V Compound Epitaxial Films on Monolithic and Porous GaAs Substrates with YSZ Sublayer. Alexander Buzynin[1], Vjatcheslav Osiko[1], Yuri Voron'ko[1], Albert Luk'yanov[2], Yuri Buzynin[3], Boris Volodin[3], Yuri Drozdov[3] and Alexey Parafin[3]; [1]A.M. Prokhorov General Physics Institute, Russian Academy of Sciences, Moscow, Russian Federation; [2]Department of Physics, Moscow State University, Moscow, Russian Federation; [3]Institute for Physics of Microstructure, Russian Academy of Sciences, Nizhniy Novgorod, Russian Federation.

Basic difficulty for fabrication of perfect heteroepitaxial III-N layers is absence of the suitable substrate. GaAs is a perspective substrate due to high quality, big sizes, low cost, and an opportunity to lead (carry out) integration of III-N devices with conventional GaAs optoelectronics. However, usually III-N layers received on GaAs substrates contain high density of structural defects and concede on parameters to the layers on sapphire or SiC substrates. To overcoming, these difficulties usually apply various buffer layers. Nevertheless, problem of search and development of new buffer layers still costs very sharply. Epitaxial GaN and GaAsN layers on GaAs with new single YSZ buffer layer and two-layer buffer (YSZ on porous GaAs) were grown in the system TMG-NH3-H2 at the temperature 1050°C by both capillary epitaxy [1] and conventional two-step MOCVD technique. The two-layer buffer consisted of porous GaAs (100) layer (10-15 micron thick), received by the electrochemical etching technique [2], and the top layer YSZ (100nm thick). Laser, electronic beam and RF magnetron sputtering techniques prepared epitaxial YSZ layers on monolithic and porous GaAs substrates. Both optically transparent and mirror smooth YSZ layers with good adhesion of film to substrate were received. YSZ films prepared by RF magnetron sputtering had the greatest structural perfection. By using porous substrate, we managed to improve the structure and morphology of YSZ layers. We found that the first, "compliant" porous layer reduced thermo-elastic stress in the second heteroepitaxial buffer layer and improved its structure perfection and morphology. Another porous buffer benefit is higher electric uniformity of III-V layers received on such substrates, due to impurity gettering by porous layer. The second buffer, chemically proof, in the environment of cultivation prevents its interaction with the basic substrate and provides thin crystal-chemical conformity with the working heteroepitaxial layer. Good damping of YSZ by gallium and indium allows fabrication on this substrate continuous and very thin layer of these materials. Stability of this layer at the epitaxy temperature provides high YSZ adaptability for capillary epitaxy Ga-V and In-V compounds layers with high quality. Porous buffer layer on GaAs substrate improves adhesion and structural perfection of III-V layers. Two-layer buffer (YSZ on porous GaAs) is a way to improvement of III-N layers quality. [1] A.N.Buzynin, V.V.Osiko, E.E.Lomonova et al. Wide-Bandgap semiconductors for High Power, High Frequensy and High Temperature. (MRS Simp.Proc.1998). Vol.512.Pittsburg, PA. P.205-210. [2] Yu.N.Buzynin, S.A Gusev, V.M.Daniltsev, et al. Technical Physics Letters V.26, No.4, pp. 298-301, 2000. The work was supported by the Russian Foundation for Basic Research (grant N 03-02-17337) and by the Office of Naval Research (Grant N 00014-01-1-0828).

G5.24
Influence of Post Treatment on the Electrical/Dielectric Properties of Nanoscale Al_2O_3 Thin Film Deposited by Atomic Layer Deposition. B. S. So[1], S. M. Kim[1], J. H. Hwang[1], Y. H. Kim[1], W. T. Cho[2] and K. S. Ahn[2]; [1]Dept. of Materials Sci. & Eng., Hongik University, Seoul, South Korea; [2]KRICT, Daejeon, South Korea.

The technological success of integrated complementary metal oxide semiconductors (CMOS) can be attributed to the extraordinary properties of the robust $Si-SiO_2$ system. Higher charge mobility and smaller transistor dimensions require an alternative material in gate dielectrics, whose candidates are HfO2, ZrO_2, Y_2O_3, Al_2O_3, etc. The so-called high-k dielectric materials have been investigated in order to replace the conventional SiO_2 for sub-micron CMOS technology generation. Al_2O_3 is one of the alternative materials because of the thermal stability, large band-offset (>2eV), similar band gap (~8.8eV) to SiO_2. The atomic layer deposition has been evaluated to be a breakthrough against the practical limitation of SiO_2-based materials, due to superior thickness uniformity, thermal budget, and excellent step coverage in stringent requirements in advanced CMOS device structure. Nanoscale (5 to 60 nm) Al_2O_3 thin films were prepared through atomic layer deposition. The electrical/dielectric characteristics should be optimized in terms of leakage currents, flat band voltage, dielectric constants, breakdown voltages, etc. The optimization is attempted using rapid thermal annealing with and without magnetic field. The electrical/dielectric features are characterized using current-voltage characteristics, capacitance-voltage measurement, impedance measurement, bias temperature stress etc, as a function of defect concentrations. The ramifications of field-enhanced rapid thermal annealing are discussed towards the next-generation CMOS integration.

G5.25
On the Crystallization of High k Unary Metal Oxide Thin Films on Silicon. Yong Gao and Kenneth A. Jackson; Materials Science and Engineering, The University of Arizona, Tucson, Arizona.

ZrO2 and HfO2 films are potential candidates for the replacement of silicon dioxide for next generation gate dielectrics. However, crystallization of these oxides at relatively low temperatures is a problem due to current leakage at the grain boundaries. In this work, we have successfully stabilized amorphous ZrO2 and HfO2 films to much higher temperatures than their bulk crystallization temperatures. By sandwiching ultra thin (< 5nm) ZrO2 or HfO2 films between two silica layers, a crystallization temperature which was typically a few hundred degrees higher than that of bare films was achieved. Ultra thin HfO2 films remained amorphous after annealed at 900øC for 15 seconds. This capping technique did not increase the crystallization temperature of relatively thick films. Possible mechanisms for this phenomenon are discussed.

G5.26
Effects of the Incorporation of Nitrogen in HfO_2 and HfO_xN_y Films Deposited by Remote Plasma Enhanced Atomic Layer Deposition Method. Jinwoo Kim, Seokhoon Kim, Jihoon Choi, Hyunseok Kang and Hyeongtag Jeon; Division of Materials Science and Engineering, Hanyang University, Seoul, South Korea.

As complementary metal oxide semiconductor (CMOS) devices reaches the design rule below 0.1?m, the current gate dielectric, SiO_2 must be scaled down below 20Å. This projected scaling of SiO_2 creates leakage and reliability issues. Thus, the adoption of high dielectric constant materials have recently been highlighted as possible replacements for SiO_2 gate dielectrics in CMOS devices. Among high dielectric constant materials, HfO_2 is considered as one of choices due to its high dielectric constant (25~30), high density (9.68 g/cm^3), wide bandgap (5.68 eV) and relatively large band offset. The Gibbs free energy of formation for HfO_2 is negative (-1088 kJ/mol), and HfO_2 is reported to be stable when in contact with Si. Although these thermodynamics data predict the stability of the HfO_2 /Si interface, the formation of interfacial layers appears to be an issue. The high oxygen diffusion rate through HfO_2, which results in the formation of interfacial layers, and a low crystallization temperatures (<500°C) remain concerns. Therefore, nitridation treatment is required to maintain amorphous structure with high dielectric constant after thermal process. The incorporation of nitrogen in HfO_2 has been suggested to reduce the tunneling current boron diffusion and to increase crystallization temperature. Incorporation of nitrogen in the oxide layer can be achieved by high temperature thermal treatments in N_2O, NO, and NH_3 atmospheres. In this study, we accomplished a nitridation process using a remote nitrogen plasma to achieve a high amount of nitrogen incorporation at low temperature and to minimize plasma damage. HfO_2 and HfON films deposited by remote plasma enhanced atomic layer deposition (RPEALD) method. We used tetrakis-dimethyl-amino-hafnium(TDEAH) as a Hf precursor, oxygen plasma as a reactant gas and nitrogen plasma as nitridation process, respectively. The nitrided and oxynitrided HfO_2 films were investigated by high resolution transmission electron microscope (HRTEM), auger electron spectroscopy(AES), x-ray photoemission spectroscopy(XPS) and x-ray Diffraction(XRD). The electrical properties including EOT, hysteresis, leakage current and capacitance were evaluated by using capacitance-voltage(C-V) and current density-voltage(J-V) measurements.

SESSION G6: Metal Gates and FUSI Gates-I
Chairs: M. Copel and M. Heyns
Wednesday Morning, March 30, 2005
Room 2007 (Moscone West)

8:30 AM *G6.1
Abstract Withdrawn

9:00 AM G6.2
In-situ Characterization of Growth, Thermal Stability and Electronic Structure of Poly-Si and FUSI Gate Electrodes on HfO2 High-k Gate Dielectrics. Yuri Lebedinskii[1], Andrei Zenkevich[1], Michael Gribelyuk[2] and Evgeni Gusev[3]; [1]Moscow Engineering Physics Institute, Moscow, Russian Federation; [2]IBM Microelectronics Division, Hopewell Junction, New York; [3]IBM T.J. Watson Research Center, Yorktown Heights, New York.

There is an enormous interest and significant research activities in developing novel high-k dielectric materials and metal gate electrodes to replace traditional ultrathin (sub-2 nm) SiO2 gate oxides in advanced MOSFET devices. In this paper, we report on formation and thermal stability of poly-Si and fully silicided (FUSI) gate materials on HfO2. Special focus is given to the gate electrode/ high-k interface, its structural and electronic properties, as well as reaction(s) upon annealing. For this study, we developed a method based on the deposition of an ultrathin (1-5 nm) continuous and very uniform layer of Si, metal (Ni) or/and a dopant (Sb, As, B, Al and Ge) marker layer on high-k by pulsed laser deposition (PLD) with the well-controlled rate of as slow as 0.01 monolayer/pulse and in-situ characterization by complementary techniques of XPS (film composition , chemical bonding and electronic structure) and LEIS (surface composition of the outmost layer). Ex-situ HRTEM was performed to evaluate stack structure. For the poly-Si/HfO2 system, we observed a layer-by-layer growth of ultrathin Si layers at room temperature, while at T>600 C an island-like growth of Si dominated. We also found silicidation reaction at higher temperatures, that can be inhibited by barrier layers. This reaction may be important to help to understand device behavior (especially PFETs) after high temperature anneals. In the FUSI part of the presentation, we will address silicidation reaction between thin Ni overlayer on thin Si/HfO2/Si(100) and the effect of the dopants on FUSI formation and, more importantly, work function modulation.

9:15 AM G6.3
Bilayer Metal Structure for Tunable Workfunction Gate Electrodes. Ching-Haung Lu[1], Gloria Wong[1], Mike Deal[1,2], Yoshio Nishi[1,2], Bruce Clemens[1], Paul McIntyre[1], Steven Hung[3], Seongjun Park[1], Prashant Majhi[5] and Wilman Tsai[4]; [1]Materials Science and Enginnering, Stanford University, Stanford, California; [2]Electrical Engineering, Stanford University, Stanford, California; [3]Applied Materials, Santa Clara, California; [4]Intel Corporation, Santa Clara, California; [5]International Sematech, Houston, Texas.

As CMOS technology continues to scale, metal gate electrodes are being introduced to minimize gate electrode depletion found in doped polysilicon, overcome the incompatibility of high-k gate dielectrics with poly silicon, and reduce mobility degradation. For optimizing the performance of different devices, future metal gate electrodes require a workfunction that can be tuned to a particular value. A tunable workfunction engineering approach using bilayer metal structures was reported by S. Hung et al.(SISC,2003) They tuned the workfunction of Al/Ni/SiO2 and Ni/Al/SiO2 gate stacks by varying the Ni or Al thickness over a 10nm range from that of one metal workfunction to the other. This behavior was initially explained by a simple carrier redistribution model. However, simulations of this model and photocurrent results of surfaces suggest that the workfunction should change more abruptly than what Hung reported. In this work we extended this tunable gate approach using several other metal pairs in addition to Al/Ni, and also when utilizing high-k gate dielectrics. The structures studied include Al/Ni/SiO2, Ti/Pt/SiO2, Ti/W/SiO2, Ti/Pt/HfO2, Pt/Ti/HfO2, and Ti/W/HfO2. Both evaporated and sputtered metals were used, with thickness from 2 to 20nm for the bottom metal. From CV measurements, VFB versus dielectric thickness was determined to extract the workfunction for a range of metal thickness. In all these metal gate stack systems, the same gradual workfunction transition was observed in which it takes around 10nm to fully change the workfunction from that of one metal to the other. Up to a 1 eV range in workfunction were obtained by varying the bottom metal thickness. As-deposited and annealed films (200~400C for up to 5 hours) were characterized by CV, TEM, EELS, EDX, SIMS, and XPS. CV measurements show that the workfunction behavior changes from a near-abrupt transition to the gradual transition behavior during an initial anneal. During subsequent annealing, the behavior does not change any further and the

structures exhibit good thermal stability in regards to workfunction on both SiO2 and high-k dielectrics. The compositional analysis indicates some diffusion occurs during annealing, but we have not to date observed any evidence of pile-up of the top metal at the interface of the lower metal/gate dielectric. We investigated several possible mechanisms for the gradual workfunction transition behavior, including carrier redistribution, non-uniform thin film deposition, metal/metal reaction, and metal diffusion. While direct evidence of a diffusion mechanism for this behavior is not clearly seen in our initial compositional analyses, the electrical behavior before and after anneal points to a diffusion/reaction mechanism that saturates after the initial anneal, rather than to a carrier redistribution mechanism. We will report on all these results involving tunable workfunction bilayer metal gates on SiO2 and high-k dielectrics.

9:30 AM G6.4
Work Function Controllability of Al-Ni Alloy Metal Gates Evaluated by Scanning Maxwell-Stress Microscopy.
Takashi Matsukawa, Chiaki Yasumuro, Hiromi Yamauchi, Meishoku Masahara, Kenichi Ishii, Kazuhiko Endo, Eiichi Suzuki and Seigo Kanemaru; Nanoelectronics Research Institute, National Institute of Advanced Science and Technology (AIST), Tsukuba, Ibaraki, Japan.

Work function (ϕ_m) control of metal gates is essential to obtain optimum threshold voltage (V_{th}) especially in FD-SOI or double-gate MOSFETs [1]. One possible candidate for a gate metal enabling work function adjustment is a binary alloy composed of metals with different work functions [2,3]. In this study, we investigated the applicability of the alloys combining Al, with low ϕ_m (4.28 eV), and Ni, with high ϕ_m (5.15 eV). Two different processes, interdiffusion of Ni/Al stack and direct sputtering of Al-Ni alloy target, were used to form Al-Ni alloy films. The CV curves of Al-Ni alloy MOS capacitors fabricated by both the processes exhibited work functions approximately between those of Al and Ni. The CV curve for the interdiffusion process, however, exhibited a significant decrease in CV slope in comparison with those of Al and Ni. In addition to the conventional CV measurement, we microscopically characterized the work function uniformity through scanning Maxwell-stress microscopy (SMM), which is capable of measuring the contact potential distribution between a sample and a probe [4]. The SMM image for the Al-Ni alloy formed by direct sputtering exhibited an uniform work function distribution, in a manner comparable to that for pure Ni film. On the other hand, the SMM image for the interdiffused Al-Ni alloy exhibited a remarkably non-uniform distribution of the work function. The non-uniform work function correlated with the degradation of CV characteristics for the interdiffused Al-Ni alloy. Thus, we conclude that direct sputtering is preferable for the Al-Ni alloy formation to suppress work function non-uniformity. The composition of the direct-sputtered Al-Ni alloy films was varied by using three different targets: $Al_{75}Ni_{25}$, $Al_{50}Ni_{50}$ and $Al_{25}Ni_{75}$. The CV and SMM measurements revealed that the work functions of the alloys were successfully controlled by the alloy composition. Except for the Al-rich alloy made from the $Al_{75}Ni_{25}$ target, the Al-Ni alloys exhibited sufficient thermal stability against annealing up to 700°C in terms of gate leak currents of the MOS capacitors. This work was partially supported by the Industrial Technology Research Grant Program (2002) of NEDO, Japan. [1] L. Chang *etal.*, IEDM (2000) 719. [2] H.Zhong *etal.*, IEDM (2001) 467. [3] I. Polishchuk *etal.*, IEEE EDL 23 (2002) 200. [4] T.Matsukawa *etal.*, J. Vac. Sci. Technol., B19 (2001) 1911

9:45 AM G6.5
Fabrication and Electrical Characteristics of HfN_x Metal Gate Electrode by MOCVD. Wen Wu Wang[1], Toshihide Nabatame[2] and Yukihiro Shimogaki[1]; [1]Dept. of Materials Engineering, The Univ. of Tokyo, Tokyo, Japan; [2]MIRAI-ASET, Tsukuba, Japan.

Continued scaling down of CMOS devices now requires metal gate electrode. HfN may be one of the most suitable candidates as gate electrode because of various advantages, such as work function of 4.65eV for midgap electrode material and simple device integration of $HfN/HfO_2/Si$ MOS gate stack by single CVD/ALD apparatus just changing reactants. In this work, hafnium nitride HfN_x was prepared by MOCVD using $Hf[N(C_2H_5)_2]_4$ (TDEAHf) precursor and its work function was evaluated from $HfN_x/SiO_2/Si$ stack. The film composition and electrical properties were evaluated by XPS, I-V and C-V measurements. It was found that HfN_x films with low levels of C (<0.1 at.%) and O impurities (<2 at.%) were formed by employing TDEAHf precursor and NH_3 reaction gas, however the film resistivity was very high about $4.8\times10^{10}\mu\Omega$-cm. This was due to the formation of N-rich Hf_3N_4 phase with high resistivity. Therefore, in order to decrease the sheet resistance of HfN_x films, NH_3-free thermal growth was employed. As a result, metallic HfN_x films were synthesized. The composition and electrical properties of HfN_x films were strongly dependent on the deposition temperature, especially beyond 500°C, the resistivity was decreased to the level of $1\times10^4\mu\Omega$-cm. For I-V and C-V measurement, in order to achieve much low total sheet resistance for the final metal gate, Au(100nm)/Ti(50nm) layers were deposited sequentially on the $HfN_x/SiO_2/Si$ stack by electron assisted vacuum evaporation technique. After gate patterning using Cl_2-based dry etching, the work function of HfN_x in $Au/Ti/HfN_x/SiO_2/Si$ MOS stack was extracted from the C-V measurements of the MOS stack with different SiO_2 thickness ranging from 4nm to 10nm. The work function of MOCVD-HfN_x was estimated to be about 4.74eV. In addition, C-V characteristics revealed that the EOT values of $HfN_x/SiO_2/Si$ MOS stack decreased for the final gate stack, e.g., $Au/Ti/SiO_2/Si$ stack showed EOT of 11nm, the EOT value became 9.7nm. By means of XPS depth profile and composition analysis, this was confirmed to be due to the formation of Hf silicate interlayer during film deposition. The thickness of interlayer was estimated to be 3nm assuming the dielectric constant of interlayer to be 16. I-V characteristics indicate that the leakage current density was almost the same with $Au/Ti/SiO_2/Si$ stack sample. One point should be noteworthy that a relative large slope value was extracted from the plot of flatband voltage (V_{fb}) versus equivalent oxide thickness (EOT) for the as-deposited samples. This suggests the existence of charge trapping, which may be mainly from the integration process of gate stack, especially the Cl_2-based dry etching process. The effect of post RTA treatment on reducing charge trapping will be discussed in detail. In addition, the growth sequence and RTA dependences of metal work function, EOT and leakage current are also studied.

SESSION G7: Transistor Processing and Characterization-I
Chairs: R. Chau and E. Gusev
Wednesday Morning, March 30, 2005
Room 2007 (Moscone West)

10:30 AM *G7.1
Integration of Advanced Gate Dielectrics on Germanium and Strained Germanium Channel MOSFETs. Huiling Shang[1], Evgeni Gusev[1], Michael Gribelyuk[2], Paul Jamison[2], Jack Chu[1], John Ott[1], Kathryn Guarini[1] and Meikei Ieong[1]; [1]IBM T.J. Watson Research Center, Yorktown Heights, New York; [2]IBM MD division, Hopewell Junction, New York.

Pure Ge channel MOSFETs have been considered as one promising option for future high performance CMOS technology because of the high electron and hole mobilities in Ge. A compressively strained Ge (s-Ge) channel is expected to further enhance hole mobility due to the very small effective hole mass ($0.1m_0$). Indeed, dramatic hole mobility enhancement of 4-25X has been demonstrated in s-Ge MOSFETs – the highest mobility enhancement for hole carriers among all available options. However, achieving a high quality thin gate dielectric for Ge and s-Ge channel MOSFETs has proven to be challenging. We will show the effects of Ge surface preparation before the high-K film deposition and the gate electrode material on the final Ge/high-K MOS characteristics. On s-Ge channel MOSFETs, we demonstrated the thinnest ever SiO_2 (2.5nm) by low temperature remote plasma oxidation of the thin Si cap while maintaining the strain in the s-Ge layer. We have also demonstrated that combining a Ge channel with HfO_2/poly can achieve appropriate PFET Vth. Finally, we will describe two CMOS-compatible integration scheme for s-Ge channel PMOSFETs, including the conventional STI isolation and scaled thin gate dielectrics for high performance CMOS technology.

11:00 AM *G7.2
Germanium Deep-Submicron pFET and nFET Devices with Etched TaN Metal Gate and High-K Dielectric, Fabricated on Germanium-on-Insulator Substrates. Marc A. Meuris[1], Brice De Jaeger[1], Jan Van Steenbergen[1], Fabrice Letertre, Geofrroy Raskin, Thierry Billon and Marc Heyns[1]; [1]IMEC, Leuven, Belgium; [2]Soitec, Bernin, France; [3]Umicore, Olen, Belgium; [4]LETI, Grenoble, France.

Since a few years, the interest of Ge FET devices has been increasing. The higher mobility of the germanium material could be one of the solutions for the problem of further CMOS scaling. In this paper, the results of pFET and nFET germanium devices with gate lengths down to 0.15 micron will be shown. The issues of the germanium will be discussed: the interface state passivation of the Ge/High-K interface, the diode leakage and the necessity of high quality germanium-on-insulator substrates.

11:30 AM G7.3
A Reason for Poor Ge n-MOSFET Performance: Source/Drain Junction Dose-Dependent Activation.
Chi On Chui[1,2], Leonard Kulig[1], Jean Moran[1], Wilman Tsai[1] and Krishna C. Saraswat[2]; [1]Intel Corporation, Santa Clara, California; [2]Electrical Engineering, Stanford University, Stanford, California.

Ge-channel has previously been suggested to supplement Si in decanano-scale MOSFET owing to its higher complementary carrier

mobilities. This inspiration has been technologically enabled by passivating the unstable Ge surface with high-k dielectrics, which also concurrently guarantees the gate stack scalability by employing metal gate electrodes. Nonetheless, the limited thermal stability of these advanced gate stacks imposes additional complexity in optimizing the source and drain junction formation process. Since p-dopants in Ge could be activated below 400 degree Celsius with minimum redistribution, mobility enhanced Ge p-MOSFET demonstrations with metal gate and high-k dielectric have not been an issue. On the contrary, the relatively higher thermal budget required to n-dope Ge causes significant diffusion and challenges the gate stack integrity. Before a better Ge n-MOSFET performance could be discerned, an uncompromised source and drain junction formation process with minimized parasitic impedance should be established. In this work, the activation of common n-dopants in Ge and the associated dependencies are investigated. Phosphorus and arsenic were first ion-implanted into p-Ge at a range of dose, and these samples are subsequently annealed with a spectrum of thermal budgets. On these n-Ge junctions, secondary mass ion spectroscopy (SIMS) and spreading resistance probe (SRP) were employed to monitor the chemical and electrically active dopant concentration respectively. By cross-comparing these SIMS and SRP profiles, several dependencies on the activation anneal are observed. For instance, higher thermal budget anneals on a given implanted dose often lowers the maximum concentrations, which could be attributed to either an excessive diffusion or a solid-solubility limitation (SSL). In order to suppress both the first and second order diffusion effects, activations were analyzed at lower thermal budgets to map out their dose-dependency. Chemical profiles reveal an increase in maximum concentration with implanted dose, yet the accompanying electrical data indicate a rather constant active level. This resultant decrease in the fraction of activated dopant hints that any excess input dose beyond the point of SSL would not improve the junction sheet resistance, but simply worsen the crystal damage due to the surplus implants. Among others, this important finding may provide an explanation for many unsatisfactory Ge n-MOSFET experimentations, whose source and drain junctions were either over-dosed or under-activated.

11:45 AM G7.4

High-Mobility GaAs and GaN MOSFETs using Atomic Layer Deposition Al_2O_3 Gate Dielectrics. Glen Wilk[1] and Peide Ye[2]; [1]ASM America, Phoenix, Arizona; [2]Purdue University, West Lafayette, Indiana.

Achieving excellent electrical properties of high-k films on GaAs or GaN substrates has been very difficult to realize, due to the nature GaAs interface, and the lack of a high-quality, stable native oxide. Previous attempts at depositing high-k oxides by CVD have led to high interface state density, large I-V hysteresis, and poor support of positive biases. MBE techniques have shown promising results for films such as Gd_2O_3, but this process requires ultrahigh vacuum, and extreme control of surface conditions, and therefore has several challenges for manufacturability. We have demonstrated excellent electrical properties on both GaAs and GaN MOSFETs using a robust, highly manufacturable Atomic Layer Deposition Al_2O_3 process for the gate dielectric. These MOSFET devices exhibit extremely low gate leakage currents on GaAs of ~1 pA/μm2 over a 10 V gate bias range, which is many orders of magnitude lower than for MESFETs under similar bias. For these same GaAs devices, channel mobilities of ~550 cm^2/Vs have been achieved at E_{eff} = 1E5 V/cm, with an f_T and f_{max} of 14 and 25 GHz, respectively, and negligible drain current drift and I-V hysteresis on these devices. GaN devices using ALD Al_2O_3 gate dielectrics have measured breakdown of ~145 V for a 2μm gate-drain spacing, with a drive current > 350 mA/mm for V_{GS} = +6V. Electron mobilities of ~1200 cm^2/Vs at E_{eff} = 1E5 V/cm have been achieved on AlGaN/GaN channels. A description of the mechanism by which this ALD Al_2O_3 process forms a high-quality interface on these channels will be given.

SESSION G8: Physical & Electrical Characterization-I
Chairs: P. McIntyre and K. Saraswat
Wednesday Afternoon, March 30, 2005
Room 2007 (Moscone West)

1:30 PM *G8.1

Negative Bias Temperature Instabilities in High-k Based MOSFETs. Michel J. C. Houssa[1], Marc Aoulaiche[1], Stefan De Gendt[1], Guido Groeseneken[1], Marc Heyns[1] and Andre Stesmans[2]; [1]IMEC, Leuven, Belgium; [2]Department of Physics, University of Leuven, Leuven, Belgium.

Negative bias temperature instabilities (NBTI) are considered as major reliability issues in metal-oxide-semiconductor field effect transistors (MOSFETs), affecting the threshold voltage, drive current and mobility of the devices. NBTI in HfO2, HfON and HfSiON-based MOSFETs are investigated, with an emphasis on the impact of Hf and N content on device degradation. It is shown that an optimal Hf content of about 50 at.% results in reduced NBTI, which is attributed to the competition between increasing density of defect precursors and slower diffusion of hydrogen species with increasing amount of Hf. On the other hand, increasing the concentration of nitrogen in the high-k stack results, like in SiON-based devices, in enhanced NBTI. The experimental results are modeled considering the generation of interface defects, within the reaction-dispersive proton transport model, as well as the creation of bulk traps in the high-k layer. The partial recovery of device degradation, when the electrical stress is interrupted or the gate voltage is switched, is next studied. The recovery implies both partial interface states annealing, possibly via atomic hydrogen or proton re-passivation, as well as bulk defect reduction, resulting from hole (thermally and field assisted) de-trapping in the high-k gate stack.

2:00 PM G8.2

Electron Spin Resonance Observation of Si/Dielectric Interface Traps in Fully Processed Metal Gate Hafnium Oxide Field Effect Transistors. Thomas G. Pribicko[1], Jason P. Campbell[1], Patrick M. Lenahan[1] and Wilman Tsai[2]; [1]Engineering Science, Pennsylvania State University, University Park, Pennsylvania; [2]Intel Corporation, Santa Clara, California.

The alternative high-k gate dielectric, hafnium oxide, is arguably the leading candidate for SiO_2 replacement in future MOS transistors. Using a very sensitive electron spin resonance (ESR) technique, spin dependent recombination (SDR), we have investigated dominating (100) Si/HfO_2 interface defects on fully processed metal/gate transistors. Transistor SDR spectra display a g-value of 2.0051 +/- 0.0003 when the magnetic field is perpendicular to the (100) Si surface. Although sample rotation in the magnetic field alters the average g-value, we are as yet unable to clearly resolve the SDR pattern into the several anticipated lines. The observed defects appear to be similar to, but probably not identical to a P_{b0} center, an unpaired electron strongly localized on a single silicon atom back bonded to three other silicon atoms at the Si/SiO_2 interface. The observed spectra may be a superposition of P_{b1}- and P_{b0}-like centers. We find that the densities of these defects may be altered greatly by gate dielectric stressing. After in-situ gate voltage stressing at modest gate voltages, we observed that the SDR amplitude of the (100) Si/HfO_2 interface P_b-like defect increases with the application of an increasing gate voltage. A hysteretic behavior in the SDR response was observed when modest negative and positive voltages were applied to the gate. This hysteretic result suggests that the application of modest gate voltages changes the chemical/physical nature of the observed defect, but does not eliminate electronic activity or paramagnetism. Work at Penn State was supported by the Semiconductor Research Corporation through Intel Corporation Funding.

2:15 PM G8.3

Interface and Defect States at Ultrathin SiO2-HfO2-SiO2-Si Junctions. Mykola Bataiev[1], Sergey P. Tumakha[1], Yuri M. Strzhemechny[1], Stephen H. Goss[1], Leonard J. Brillson[1], Chris L. Hinkle[2] and Gerry Lucovsky[2]; [1]Electrical & Computer Engineering, Physics, and Center for Materials Research, The Ohio State University, Columbus, Ohio; [2]Physics, North Carolina State University, Raleigh, North Carolina.

We have used low energy electron-excited nanoscale luminescence spectroscopy (LEEN), a low energy form of cathodoluminescence spectroscopy, to probe the interface states at ultrathin layers of SiO2 and HfO2 deposited by a remote plasma process on remote plasma-processed Si-SiO2 substrates. HfO2 is a leading alternative dielectric material for reducing direct tunneling in metal oxide semiconductor (MOS) devices. This is due to its increased dielectric constant K compared to SiO2 and a significant reduction in tunneling current with respect to SiO2 with the same equivalent oxide thickness. Critical to use of such structures is the reduction of interface defect densities that could introduce fixed charge that degrades threshold voltages and reduces field effect control. Currently, the only measurements of such states involve indirect transport and capacitance methods and show interface state densities of 1012 cm-2, far from state-of-the-art. Here we provide direct measurements of optical transitions involving deep localized energy states inside these ultrathin dielectrics and at their internal interfaces. We employed incident electron beam energies of 0.5 - 3.5 keV to probe 5 nm SiO2/15 nm HfO2/5 nm SiO2/Si dielectric stacks in ultrahigh vacuum (UHV) with corresponding probe depths ranging from the outer SiO2 layer to the Si substrate. These results revealed the presence of defect luminescence bands at 2.75 eV and 1.90 eV within the SiO2 and at their interfaces with HfO2. LEEN spectra also exhibited two non-SiO2-related spectral peaks at 3.5 eV and 4.2 eV associated with the HfO2 thin film and its interfaces with SiO2. These assignments are confirmed by measurements on thick HfO2. For the as-grown

stack, the 2.75 eV feature is maximum at the outer SiO2/HfO2 interface and decreases by 2x at the inner HfO2/SiO2 interface, whereas the 3.5 eV HfO2 midgap transition reaches a maximum at depths inside the HfO2 film. The 1.9 eV defect feature appears relatively constant throughout the entire stack. A 900°C anneal exhibits a strain-induced self-organization that induces interfacial bonding changes resulting in order-of-magnitude fixed charge reduction. Annealed stacks exhibit strong localization of 2.75 eV, 3.5 eV, and 4.2 eV LEEN defect emission to the outer SiO2/HfO2 interface, a 3-4x increase in I(3.5 eV)/I(2.75 eV), and a 35x in I(4.2 eV)/I(2.75 eV), consistent with changes in HfO2 and HfO2 interface bonding. Secondary ion mass spectrometry (SIMS) reveals minimal interdiffusion but H accumulation at the inner HfO2/SiO2 interface that annealing removes. These results were compared with those of analogous SiO2/Al2O3/SiO2/Si dielectric stacks with essentially the same dimensions. As expected, these exhibit qualitatively different high-K dielectric features. The capability to assess local state intensities and spatial distributions enables in-situ process optimization for defect reduction.

2:30 PM G8.4
Band Edge States Derived from Jahn-Teller Term Splittings in High-k Dielectrics: Bias-Dependent, Intrinsic Bulk Traps in High-k Gate Stacks for Advanced Si Devices. Gerald Lucovsky[1], Charles Fulton[1], Lisa Edge[2], Robert Nemanich[1], Darrell Schlom[2] and Jan Luning[3]; [1]NC State Univ, Raleigh, North Carolina; [2]Penn State University, State College, Pennsylvania; [3]Stanford Synchrotron Research Laboratory, Menlo Park, California.

This paper reports for the first time high-resolution x-ray absorption spectra (XAS) for transition metal (TM) elemental, and TM/rare earth (RE) complex oxides that demonstrate term-split d-state features associated with Jahn-Teller local bonding distortions. Electron states at the conduction band edge of SiO2 are derived primarily from Si 3s* states mixed with O 2p* states and are free-electron-like, whereas band edge states in high-k dielectrics are derived from TM/RE d*-states mixed with O 2p* states and are considerably more localized [1]. In this paper, Jahn-Teller (J-T) term splittings of localized d*-states by XAS are correlated with published results for photoconductivity (PC) "band-tails" [2], and bias dependent trapping [3,4]. High-resolution XAS L2,3 spectra for Ti in TiO2, and in TiO2-HfO2 and ZrO2 complex oxide are presented. L2,3 transitions in TiO2 terminate in empty 3d states with 3- and 2-fold degeneracies of the respective 3d5/2 and 3d3/2 states completely removed. These term-splittings are attributed to J-T distortions of 6-fold coordinated bonding of Ti to 3-fold coordinated O. 3d5/2-state term splittings in p-bonded valence bands are quantitatively the same in rutile TiO2, and Hf(Zr)O2-TiO2 oxides. However, there are differences in the 3d3/2 state s-bond term splittings between i) TiO2, and the ii) Hf(Zr)O2-TiO2 oxides that derive from Ti d-states interacting with different 2nd neighbor Ti, Zr or Hf, d-states through s-bonding interactions. O K1 edges in TiO2, and Hf(Zr)O2-TiO2 display 5 d*-features that are also present at the conduction band edge. Term splittings have not observed for 4d and 5d states in M2,3 and N2,3 spectra of ZrO2 and HfO2; however, 5 4d* and 5d*-state features are present in the O K1 edges of both ZrO2 and HfO2. J-T term split states will also be reported for Sc L2,3 in LaScO3, and La M2,3 spectra in LaAlO3. In contrast, the M2,3 spectra for La in LaScO3 as-deposited and annealed films show a single d-state feature consist with a spherically-symmetric, or ordered 12-fold coordination for La. The respective O K1 edges for LaScO3 and LaAlO3 also display J-T term splittings. Band-tail photoconductivity, correlated with 5d*-states in O K1 spectra, has been reported in TiO2, ZrO2, HfO2, and complex oxides including LaAlO3 and LaScO3 [2]. Bias temperature instabilities HFO2 devices reported in Ref. 3 are consistent with bias dependent Frenkel-Poole transport thru Hf 5d band edge, term split states [4]. NEC has recently engineered around bias dependent transport/trapping by restricting biases to less than about 1.1 eV in stacked SiO2-Hf silicate devices. [1] G Lucovsky et al. JVST B 22, 2132 (2004), [2] VVAfanase'v et al, Chap 3.3, High-k Dielectrics, M Housa (ed), and APL in process. [3] JC Lee and K Oishi in Chap. 5.3, in Ref. 2, [4] Z Yu et al., APL 80, 1975 (2002).

2:45 PM G8.5
Energy-band Alignments and Interface Stability at ZrO_2/Si, SiGe and Ge Interfaces. S. J. Wang[1], J. W. Chai[1], J. S. Pan[1], Y. L. Foo[1] and A. C. H. Huan[1,2]; [1]Institute of Materials Research & Engineering, Singapore, Singapore; [2]Department of Physics, National University of Singapore, Singapore, Singapore.

High-k gate dielectrics have been expected to replace conventional SiO_2 gate oxide to continue the scaling of silicon-based semiconductor device. However, because of phonon scattering in moderate electrical field, field effect transistors (FETs) with high-k gate dielectrics show that their carrier mobility is less than those of FETs with a SiO_2 gate oxide, and is well below the universal mobility curve. This will hamper the objective of device scaling using high-k gate dielectrics if an FET with a high-k material actually has a lower mobility than the equivalent SiO2 device. Because of higher low-field intrinsic carrier mobility than that of silicon, Ge and its alloy are attractive for high-frequency applications. The integration of high-k gate dielectrics with high performance substrate or channel materials of Ge and its alloy not only allow the continued scaling of semiconductor devices, but also have the higher mobility to improve device speed. In this presentation, we present the energy-band alignment and interface stability studies for ZrO_2/Si, $Si_{0.75}Ge_{0.25}$/Si and Ge systems. The energy-band alignments have been studied using x-ray photoemission. The valence-band offsets of ZrO_2/Si, $ZrO_2/Si_{0.75}Ge_{0.25}$ and ZrO_2/Ge interfaces are determined to be 2.95, 3.13 and 3.36 eV, respectively, while the conduction-band offsets are found to be the same value of 1.76±0.03 eV for three interfaces. The upward shift of valence-band top accounts for the difference in the energy-band alignment at three interfaces. The interface thermal stability has been studied using in-situ x-ray photoemission, in-situ transmission electron microscope and high-resolution transmission electron microscope. The phase transition of high-k and interface reaction upon high-temperature annealing has been identified.

SESSION G9: Modeling and Simulation
Chair: P. McIntyre
Wednesday Afternoon, March 30, 2005
Room 2007 (Moscone West)

3:30 PM *G9.1
Electron Mobility in High-κ MOSFETs: Remote Phonon Scattering and its Temperature and Material Dependence. Massimo V. Fischetti[1,2], Deborah A. Neumayer[1], Eduard A. Cartier[1], Zhibin Ren[3], Evgeni P. Gusev[1] and Michael P. Chudzik[3]; [1]IBM SRDC, Research Division, T. J. Watson Research, Yorktown Heights, New York; [2]Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, Massachusetts; [3]IBM Microelectronics Division, Hopewell Junction, New York.

The high dielectric constant of insulators currently investigated as alternatives to SiO_2 in metal-oxide-semiconductor structures – due mostly to their large ionic polarizability – is accompanied by the presence of soft optical phonons. The long-range dipole field associated with the interface excitations resulting from these bulk modes and from their coupling with surface plasmons, while small in the case of SiO_2, for most high-κ materials causes a reduction of the effective electron mobility in the inversion layer of the Si substrate. We study the dispersion of the interfacial coupled phonon-plasmon modes, their electron-scattering strength, and their effect on the electron mobility for Si-gate structures employing films of SiO_2, Al_2O_3, AlN, ZrO_2, HfO_2, and $ZrSiO_4$ for 'SiO2-equivalent' thicknesses ranging from 5 nm to 0.5 nm. We show that the effective electron mobility is severely depressed in systems employing the insulators with the highest κ (namely, ZrO_2 and HfO_2), while nitrides and oxy-silicates still yield satisfactory mobilities, especially for films thin enough to benefit from dielectric screening from the electrons in the polycrystalline Si gate. We also show that the electron mobility increases with the increasing thickness of the interfacial oxide layer often present – intentionally or not – in these gate stacks and discuss the beneficial (screening) effects of metal gates. Finally, we present experimental data and calculations regarding the temperature and material (HfO_2 vs. $HfSi_xO_y$ dependence of the electron mobility, providing additional support to the theory.

4:00 PM G9.2
Surface States and Rectification at a Metal High-k Dielectric Contact. Alex Demkov, Freescale Semiconductor, Inc., Austin, Texas.

The properties of metal-to-insulator junctions are often discussed in terms of the Fermi level pinning by the interface states. An alternative point of view is based on the picture of polarized chemical bonds at the metal-to-insulator interface. We consider theoretically the case of molybdenum on the (111) surface of the tetragonal polymorph of hafnia, and trace the formation of the Schottky barrier from the Newens-Anderson chemisorption limit to a one nm thick layer of the (110) oriented metal. The role of the surface band of hafnia in the pinning of the Fermi level is discussed, including the analysis of relative roles of the evanescent and chemical interface states. We critically compare the predictions of the metal induced gaps states (MIGS) model with the results of direct density functional calculations.

4:15 PM G9.3
Defect Energy Levels in HfO2 and ZrO2. Ka Xiong, Barbara Falabretti and John Robertson; Engineering, Cambridge University, Cambridge, United Kingdom.

High dielectric constant (K) oxides such as HfO2 are needed to replace SiO2 as the gate oxide in future CMOS devices. However, these oxides

possess a much higher bulk density of charge traps than SiO2. Little is known about these traps and their energy levels. Lenahan et al [1] have observed ESR spectra of 3 centres, the O vacancy, the Hf3+ ion and the peroxyl or superoxyl radical, a specific type of O interstitial. Takeuchi [2] recently used spectroscopic ellipsometry to deduce that the O vacancy level lay about 1.2 eV below the HfO2 conduction band (CB). Injection measurements of HfO2 on Si of Kerber [3] are consistent with partly filled levels above the Si CB. Foster et al [4] calculated the energy levels of the vacancy and O interstitial in ZrO2 and in HfO2 using the local density approximation (LDA) with scissors corrections for the under-estimate of the band gap. They found the O vacancy gives a state below the Si VB top, when aligned to the HfO2 bands, and the O interstitial gives various states across the lower part of the HfO2 gap. We have calculated the energy levels of the O vacancy and the various O interstitial charge states, by finding their energy levels directly as excited states. Correct band gaps were found by using methods beyond LDA, called screened exchange (sX) and weighted density approximation (WDA). We find the neutral O vacancy gives a filled level lying near the Si CB, higher than Foster [4], and closer to Takeuchi [2] and Kerber [3]. When partially filled, as in V+, the level lies higher. Thus, the O vacancy is the principle electron trap. For the interstitial, overall, we find states well away from the Si gap and closer to the HfO2 band edges, so they are less likely to act as traps. The neutral O interstitial forms an O-O bond. It creates filled states about 0.5 eV above the HfO2 VB edge, plus an empty state just below the HfO2 CB. The positive O interstitial, equivalent to the superoxyl radical seen by Lenahan [2], gives a half filled state about 1 eV above the HfO2 VB edge and an empty state in the HfO2 conduction band. The negative O interstitial breaks the O-O bond, and this has a half-filled state just above the HfO2 VB edge, and no other states in the gap or CB. 1. A Y Kang, P M Lenahan, J F Conley, App Phys Lett 83 3407 (2003); + unpublished 2. H Takeuchi, D Ha, T J King, J Vac Sci Technol A 22 1337 (2004) 3. A Kerber, E Cartier, IEEE ED Lett 24 87 (2003) 4. A S Foster, et al, Phys Rev B 64 224108 (2001); ibid 65 174117 (2002)

4:30 PM G9.4

Chemical Mechanisms for Atomic Layer Deposition of Hafnium Nitrides and Nitrogen Incorporation into HfO2 ALD Films Using Ammonia and Alkylamide as Precursors. Ye Xu[1] and Charles B. Musgrave[2,1]; [1]Materials Science and Engineering, Stanford University, Stanford, California; [2]Chemical Engineering, Stanford University, Stanford, California.

We use DFT to investigate an atomistic mechanism for the ALD of hafnium nitride films grown using $Hf[N(CH_3)_2]_4$ and NH_3. We find a ligand-exchange mechanism similar to those thought to occur in the ALD of HfO_2 using the same Hf source and H_2O. Both half-reactions involve intermediates that are more stable than the products. Although the $Hf[N(CH_3)_2]_4$ half-reaction at NH* sites has a barrier similar to that of reaction with OH* sites, the barrier for the NH_3 half-reaction on the $Hf[N(CH_3)_2]_x$* terminated surfaceis significantly larger than for reaction between H_2O and $Hf[N(CH_3)_2]_x$*. Thus, the NH_3 half-reaction is significantly slower than reaction with H_2O and thus the NH_3 half-cycle will be prone to oxygen incorporation into Hf-nitride from residual H_2O. Therefore water must be purged from the chamber when depositing Hf nitrides or incorporating N into HfO_2 using this chemistry. These results indicate that NH_3 and $Hf[N(CH_3)_2]_4$ can be used to either incorporate N into HfO_2 ALD films or grow Hafnium nitride.

4:45 PM G9.5

Dielectric Properties of Rare-Earth High-k Oxides. Pietro Delugas, Vincenzo Fiorentini and Alessio Filippetti; INFM-SLACS and Dept. of Physics, University of Cagliari, Monserrato, Italy.

Rare-earth oxides have recently come into focus as candidates for the replacement of silica as a gate dielectric in transistor and as a barrier oxide in FLASH memories. We are currently investigated by density-functional and self-interaction-correction methods several oxides involving para-rare-earths such as lanthanum and lutetium. We started with sesquioxides (X_2O_3), which exhibit competing cubic (bixbyite) and hexagonal structures: the dielectric and IR and Raman spectral properties of bixbyite Lu_2O_3 have been calculated and succesfully compared with experiment [1]; the results suggested that the cubic phase is generally poorer in terms of dielectric screening than the hex phase, the static dielectric constant values for Lu_2O_3 being 12 and 18 respectively. This was confirmed by an extension of our work to La_2O_3 [2], whose dielectric constant is higher (about 24) on account of both the softer IR modes of the hex phase, and the higher dynamic polarizability. We then considered [3] the properties of crystalline $LaAlO_3$, a distorted cubic perovskite with a 1% mismatch to Si (001), which has a dielectric constant of 20-25; theory confirms a static value of 22 to 27 depending on the treatment of the effective dynamical charges. We are currently investigating amorphous $LaAlO_3$, to ascertain the reasons (if any) that cause it to have a static constant comparable to the crystalline phase, and $LuMnO_3$, a magnetic compound exhibiting dielecric anomalies, currently under experimental investigation at a partner laboratory. [1] E. Bonera, G. Scarel, M. Fanciulli, P. Delugas, and V. Fiorentini, to be published [2] P. Delugas and V. Fiorentini, to be published [2] P. Delugas, V. Fiorentini, and A. Filippetti, to be published

SESSION G10: Poster Session: II

Chairs: A. Dimoulas and J.-P Locquet
Wednesday Evening, March 30, 2005
8:00 PM
Salons 8-15 (Marriott)

G10.1

Impact of Oxygen on the Work Functions of Metal Gates on High-k Oxides. Andrey Knizhnik[1], Andrey Safonov[1], Inna Iskandarova[1], Alexander Bagatur'yants[1], Boris Potapkin[1] and Leonardo Fonseca[2]; [1]KINTECH Ltd, Moscow, Russian Federation; [2]Freescale Semiconductores Brasil Ltda, Jaguariuna, Brazil.

The impact of oxygen on the work functions of promising metal gates (Mo, WC) for new MOSFET devices is investigated using first-principles calculations. The effect of oxygenation is compared for metal surfaces and for interfaces with typical high-k oxides (monoclinic zirconia and hafnia). It is shown that oxygen adsorption on the metal gate surfaces (Mo(110) and WC(0001)) strongly increases the vacuum metal work function, a similar trend is observed for the Mo(110) (WC(0001)) work function on zirconia (hafnia) upon the oxygenation of the Mo/m-ZrO2 (WC/m-HfO2) interface, though to a lesser extent. As expected, the effective metal work function decreases upon the reduction of the metal/oxide interface and increases upon its oxidation. However, interface overoxidation with the formation of a thin MOx layer between the metal gate and the oxide can causes the work function to decrease with respect to the unoxidized interface as shown for the Mo/m-ZrO2 interface with a MoOx intermediate layer. The physical origin of this effect is explained by the partial cancellation of interface dipoles. These results are compared with the calculated work functions of the conducting metal oxide MoO2 (WO2) surfaces.

G10.2

Area-Selective Atomic Layer Deposition for *in − situ* Gate Stack. Rong Chen[1,2], David W. Porter[2], Hyoungsub Kim[3,4], Paul C. McIntyre[3], Hemanth Jagannathan[4], Yoshi Nishi[4] and Stacey F. Bent[2]; [1]Dept. of Chemistry, Stanford University, Stanford, California; [2]Dept. of Chemical Engineering, Stanford University, Stanford, California; [3]Dept. of Materials Science and Engineering, Stanford University, Stanford, California; [4]Dept. of Electrical Engineering, Stanford University, Stanford, California.

Atomic layer deposition (ALD) is a technique that can be used to deposit a variety of materials. While ALD inherently provides nano-scale control of materials in the vertical direction, we are investigating an area-selective ALD technique that enables micro- and nano-scale definition of the lateral structure. Our research emphasizes controlling the substrate surface chemistry in order to impart spatial selectivity to ALD. Using a variety of analytical techniques, we will demonstrate that functionalizing the surface with self-assembled monolayers (SAMs) can block the ALD chemistry in the growth of HfO_2 and ZrO_2, which are both important high-κ materials for potential gate dielectrics. At the same time, SAMs are effective monolayer resists towards ALD growth of Pt thin films that could serve as a future gate metal. Specifically, we have investigated the surface chemistry required to block ALD under the more extreme conditions used to deposit these metal oxide dielectrics and gate metal at temperature above 300°C. The efficiency of blocking depends strongly on the quality of the SAMs and on the chain length of the attached layer. The potential of the area selective process for defining lateral structure has been examined using different patterning methods, including selective functionalization of patterned SiO_2/Si as well as soft lithography. Using a combination of image analysis by SEM and elemental analysis by scanning Auger microscopy, we show that the high-κgate dielectric and gate metals can be deposited with spatial selectivity. Other types of SAMs have also been investigated as monolayer resists against the HfO_2 ALD process on Si and Ge substrates. These monolayer films also exhibit good deactivation and selectivity. The ability to achieve area-selective ALD for both gate dielectrics and gate metals enables the potential fabrication of an *in − situ* gate stack, providing for an additive patterning scheme that has several advantages over the subtractive patterning used in current CMOS process flow.

G10.3

TEM Characterization of Epitaxial HfO2 Thin Films Grown on Ge by MBE. Jin Won Seo[1], C. Dieker[1], A. Dimoulas[2], Jean-Pierre Locquet[3], J. Fompeyrine[3], H. Siegwart[3], C. Wiemer[4], G.

Tallarida[4], S. Ferrari[4] and M. Fanciulli[4]; [1]EPFL, Lausanne, Switzerland; [2]NCSR Demokritos, Athens; [3]IBM, Rueschlikon, Switzerland; [4]MDM-INFM, Agrate Brianza Milano, Italy.

High mobility materials such as Ge are emerging as potential silicon replacement in CMOS. Unfortunately, for advanced gate stack on Ge the native oxide GeO has a low thermal stability. Therefore, the challenge is to find a set of suitable high K dielectric compounds that can be used as gate dielectrics while maintaining a high mobility in the channel. The main question to be answered is the chemical and structural interface stability during the growth, and their influence on the high-k dielectric layer grown above. In this contribution, we report on structural and chemical properties of HfO2 films deposited on Ge substrates by molecular beam epitaxy. We carried out the growth studies along two directions: on conventional single-crystalline (001)Ge substrates and on electron transparent single-crystalline Ge nanowires. Using the latter, the growth characteristics can directly be assessed without the time-consuming and dedicated sample preparation for transmission electron microscopy. Ge nanowires were produced in a MBE system by vapor-liquid-solid reaction of Au catalyst deposited on (111)Si substrates. To be precise 1.0 nm Au is deposited on Si substrate at 300 C and subsequently annealed at 600 C in order to form metal clusters, whereby their diameter determines the resulting diameter of the nanowires. By the subsequent deposition of Ge, the Au catalytic particles initiate the growth of the nanowires. Ge nanowires were obtained with (111) orientation with average diameter of 50 nm. HfO2 films were deposited at 350 C on the Ge nanowires. On conventional Ge substrates, HfO2 thin films were grown with and without GeOxNy interfacial layer in the temperature range up to 360C. By means of transmission electron microscopy, the interface and the crystallinity of HfO2 films are analyzed: HfO2 grows polycrystalline but with a crystalline interface on Ge. The interface characteristics are compared for different substrate materials. Energy dispersive x-ray scanning profiles show that Ge diffusion occurs into the oxide film when deposited on GeOxNy whereas for pristine Ge interface no significant Ge diffusion was observed. This result was confirmed by time of flight secondary ion mass spectrometry depth profiles.

G10.4
Improved Workfunction Tunability and EOT Control with Clustered ALD TaN/PVD Ta for Multilayer Metal Gate.
Steven C. H. Hung[1], Khaled Ahmed[1], Chris Olsen[1], Rongjung Wong[2], Fred Wu[2], Nety Krishna[2], Gary Miner[1], Ching Huang Lu[3], Michael Deal[3] and Yoshio Nishi[3]; [1]ADC/Front End, Applied Materials, Sunnyvale, California; [2]CPI, Applied Materials, Sunnyvale, California; [3]Electrical Engineering, Stanford University, Stanford, California.

Metallic gate electrodes have been considered as the primary solution for resolving the polysilicon gate depletion effect for the sub 65nm node technology. However the workfunction requirement has limited the amount of material candidates for such application. Multilayer metal gates have been previously demonstrated as possible solution for providing the adequate workfunction tuning for CMOS circuitry. The purpose of this paper is to investigate the applicability of multilayer metal gate by focusing on the process integration issues. The key questions that will be addressed in this paper include: - Can multilayer metal gates be implemented with previously integrated back end of line metallic materials and deposition technologies? - Do the deposition processes between metallic layers need to be clustered to reduce oxygen contamination in order to achieve the desired workfunction adjustment? Would the clustering result in any other device benefit, such as EOT control? NMOS capacitors were fabricated to test the effect of clustering on electrical behavior. The gate stack consists of rapid thermal oxidation (RTO) silicon dioxide (SiO2) as the gate dielectric; atomic layer deposition (ALD) TaN as the bottom contacting metal layer and physical vapor deposition (PVD) Ta as the capping layer. The thickness of the SiO2 layer was fixed at 50A, and the thickness of ALD TaN was varied from 20, 40, 60, 80, 120 and 200A for the purpose of workfunction tuning. The deposition of the PVD Ta layer was either clustered or non-clustered with the deposition of the ALD TaN layer. In the case of the non-clustering process, a four-hour air-break was introduced. The film stacks were fabricated into MOS capacitor, and the devices were annealed in forming gas ambient (FGA) before capacitance-voltage (CV) measurement. The values of equivalent oxide thickness (EOT) and the flat band voltage (Vfb) were extracted during additional analysis. The CV measurements revealed that the clustered gate stack resulted in approximately 200mV of Vfb adjustment, whereas the non-clustered case resulted in half of Vfb adjustment ($\sim$ 100mV). It was also found that the EOT of the non-clustered case to be approximately 4A thicker than that of clustered case. The increase in the EOT suggested of a larger dielectric thickness in the non-clustered case, a direct result of oxidation on the ALD TaN film during the four-hour air break process. X-ray photoemission spectroscopy (XPS) was later used to confirm the extent of oxidation in the ALD TaN film after air exposure. This experiment has demonstrated the effectiveness of using a clustering process between ALD TaN / PVD Ta deposition in improving the workfunction tuning and providing EOT control for the multilayer metal gate stack.

G10.5
Nitrided Hafnium Silicates for Gate Dielectrics.
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Nitrided hafnium silicate (HfSiON) gate dielectric films deposited by atomic layer chemical vapor deposition (ALCVDTM) show excellent capacitor and transistor characteristics with both poly-Si and metal gates, which are directly correlated with local physical and chemical properties. A wide range of compositions are demonstrated, with Si/(Hf+Si) percentages from 0 to 75% and uniformly distributed N levels up to 30 at. %. XPS is used to distinguish the local bonding arrangements of N to Hf, Si and O. The distribution and depth profile of these N bonds is directly attributable to the observed electrical and physical properties of these films as measured by TOF-SIMS, TEM, EELS, nuclear reaction analysis and angle-resolved XPS. Using poly-silicon gate electrodes with chemical or thermal oxide underlayers, EOT values down to 1.3nm with substantial leakage reduction vs. SiO2 have been achieved using stacks with ultrathin HfSiON. Hysteresis and midgap interface density (Dit) are less than 10mV and 5E10 cm-2eV-1, respectively. Transistors (gate length of 110nm) with these ALD HfSiON films display excellent VT stability and channel electron mobility > 90% of SiO2 at high Eeff. Detailed analysis on silicate compositions, the distribution of nitrogen in the interface layers, and corresponding impact on device performance will be presented.

G10.6
The Perfect Interface: Ge/SiO2. Gerd Duscher[1,2], Sergei Lopatin[3], Tao Liang[4] and Wolfgang Windl[4]; [1]Materials Science & Engineering, North Carolina State University, Raleigh, North Carolina; [2]Condensed Matter Science Division, Oak Ridge National Laboratory, Raleigh, Tennessee; [3]NCEM, Lawrence Berkeley National Laboratory, Berkeley, California; [4]Materials Science & Engineering, The Ohio State University, Columbus, Ohio.

We propose that a thin layer of Ge on a Si substrate with SiO2 as dielectric can serve as an alternative to high-k materials in CMOS technology. The Ge-SiO2 interface was studied with a combination of atomic resolution Z-contrast imaging, electron energy-loss spectroscopy (EELS) and ab initio density functional theory. The atomic resolution experimental and theoretical results agree extremely well and show that this interface is chemically abrupt. The exact structure consists of Ge thin film, one atomic layer of SiGe and one layer of Si 2+. The first silicon atom in the oxide is already fully oxidized. The thermally grown Si-SiO2 interface, however, has a 0.3 nm wide transitional (suboxide) region. The bandgap of the oxide does not follow the chemical gradient at the Si-SiO2 interface, but opens up slower than the chemical composition. We verified this result by comparing the conduction band derived from EELS and from calculations. Both agree excellently for all the investigated interfaces. By using the chemical abrupt (perfect) Ge-SiO2 interface, we gain 0.3 nm of effective oxide thickness. Therefore, this structure will result in faster devices because the interface allows a smaller SiO2 thickness, while Ge has intrinsically a higher mobility. The interface, however, is effectively still a Si-SiO2 interface, and we expect the same level of interface defects. Because the chemically abrupt Ge-SiO2 interface is thermally stable, this structure is fully compatible with standard CMOS technology.

G10.7
The Study on Growth Kinetics of Hf-Silicate Films on Si (100) Grown by Atomic Layer Deposition using in-situ Medium Energy Ion Scattering. Kwun Bum Chung[1,2], Mann-Ho Cho[2], Dae Won Moon[2] and Chung Nam Whang[1]; [1]Institute of Physics and Applied Physics, Yonsei University, Seoul, South Korea; [2]Nano Surface Group, Korea Research Institute of Standards and Science, Daejeon, South Korea.

The growth kinetics and initial growth characteristics of Hf-silicates grown on Si(100) by atomic layer deposition (ALD) was investigated by in-situ medium energy ion scattering (MEIS). SiO2 incorporated Hf-Si-O was grown by alternant ALD process for HfO2 and SiO2 using HfCl4 and TDMAS, respectively. The interaction between HfO2 and SiO2 films was examined in relation to the each layer thickness, substrate temperatures. The SiO2 growth on HfO2 was critically depended on the HfO2 thickness. Moreover, the thickness of HfO2 layer and SiO2 layer affected the interfacial reactions and stoichiometry, which indicate that the HfO2 layer acts as a catalyst to stimulate Hf-silicate growth. The amount of SiO2 incorporated HfO2

was decisively affected by the catalytic effects. The initial growth stage definitely varied according to buffer layer on Si substrates. The physical analysis of the films with XPS, XAS, TEM also supported the formation mechanism of Hf-silicate. Based on the interfacial interactions between HfO2 layer and SiO2 layer, we suggested the model for growth kinetics of Hf-silicates at the initial growth stage in relation to the formation energy, interfacial reaction, and catalytic action. Our study on the growth model for Hf-silicate will be a great help to understand the interfacial reactions in the ALD growth and to control the reactions for application of the Hf based high-k dielectrics.

G10.8
Work Function Engineering of Fully Silicided NiSi Metal Gate Through Pt Addition. Rinus Tek Po Lee, Siao Li Liew, Weide Wang, Hai Biao Yao, Emily Kwee Choo Chua, Shue Yin Chow, Doreen Mei Ying Lai and Dongzhi Chi; Institute of Materials Research and Engineering, Singapore, Singapore.

In this work, NiSi and $Ni_{1-x}Pt_xSi$ (x=5%-33%) mono-silicides were investigated as metal gate electrode materials for complementary-metal-oxide-semiconductor (CMOS) technologies. Our results showed that NiSi gates formed by the reaction of pure Ni on undoped poly-Si are thermally stable on SiO_2 gate oxide up to 950 ^oC. From the capacitance - voltage measurement of MOS structures, it has been found that the NiSi gate has a work function of $\sim$ 4.59 eV. The work function of the NiSi gate was found to increase monotonically with increasing Pt content when Pt was added to the NiSi gate. With a proper composition of $Ni_{1-x}Pt_xSi$, the work function of the gate electrode can be tuned from $\sim$ 4.59 eV (for pure NiSi) up to $\sim$ 5.21 eV (for $Ni_{1-0.33}Pt_{0.33}Si$). The integrity of the fully silicided gate stacks (i.e. NiSi and $Ni_{1-0.33}Pt_{0.33}Si$ gates on the SiO_2 gate oxide) after high temperature processing was also studied, which showed no evidence of degradation at both metal/oxide and oxide/Si interfaces and/or in the gate oxide. The tunable work function and good thermal stability of $Ni_{1-x}Pt_xSi$ makes it a viable option in the selection of metal gate materials for p-MOSFETs in dual metal gate CMOS devices.

G10.9
The Impact of Interface Structure on Schottky-Barrier Height for Metal-Gate/High-k Interfaces. Ach Huan[1,2], Y. F. Dong[2], Q. Li[2], Y. P. Feng[2] and S. J. Wang[1]; [1]Institute of Materials Research & Engineering, Singapore, Singapore; [2]Department of Physics, National University of Singapore, Singapore, Singapore.

With the alternative high-k gate dielectrics are expected to replace current gate oxide for the continued scaling of metal-oxide-semiconductor field-effect transistors (MOSFET), there is an immense interest in replacing conventional poly-Si gate with metal gates because of the serious problems related to poly-Si gate depletion and high gate resistance. In order to achieve low and symmetrical threshold voltages, the optimal work functions for metal gate material should be such that its Fermi level (FL) coincides with the conduction (or valence) band edge for n-MOSFET (or p-MOSFET) devices. However, the possible atomic bonds of metal-metal or metal-oxygen at metal gate/oxide gate dielectric interface are quit different from conventional silicon-oxygen bond at poly-Si-SiO_2 interface. How these bonds affect the band alignment at the metal/high-k oxide interface is important issue for the implementation of this gate stack. In this presentation, we present the impact of interface atomic structure on the schottky-barrier heights (SBH) for Ni/ZrO_2 (HfO_2) interfaces by photoemission study and first-principle calculation. The schottky-barrier heights for the Ni and ZrO_2 (HfO_2) interfaces have been determined by means of x-ray photoemission spectroscopy. Depending on the interface treatment, the variation of SBH was found as large as 0.8 eV. First-principles calculations for model interfaces provide a microscopic explanation of such variation. The results show that the SBH at metal/high-k can be engineered through the interface structure-control.

G10.10
Investigation of Magnetic Properties of R.F. Sputtered Hafnium Oxide Layers. Heinrich Grueger[1], Christian Kunath[1], Eberhard Kurth[1], M. Venkatesan[2], L. S. Dorneles[2] and Michael Coey[2]; [1]Sensors Division, Fraunhofer IPMS, Dresden, Germany; [2]Physics Department, Trinity College, Dublin, Ireland.

Recently ferromagnetic behaviour has been observed in thin films of hafnium oxide [1]. There is evidence that the phenomenon is defect-related, and confined to a thin layer at the interface with the substrate. An very interesting question is the correlation of magnetic properties of the hafnium oxide layer and properties such as crystallinity or impurity content. Hafnium oxide layers with thickness ranging between 50 and 150 nm have been deposited by r.f. sputtering of a high-purity hafnium oxide target in argon and/or oxygen gas mixtures. (100) Si wafers with 150 mm diameter etched in HF or thermally oxidized served as substrates. The layers have been characterized by AFM, SEM, XRD, and selected samples were investigated in detail by TEM. Thin layers of the as-deposited material were highly disorderd, and they were subject to a rapid thermal anneal at a rate of up to 50 K s^{-1} in order to produce a fine-grained polycrystalline texture with grain size below 50 nm. With increasing thickness, the crystallization starts during deposition. After annealing at 950°C all layers are crystalline with a (-1 1 1) texture. For magnetic analysis, 5 x 5 mm pieces were cut from the wafers, and measured in a 5 T Quantum Design SQUID magnetometer. The magnetization of four typical films are given in the table 1, where the magnetic moment of the sample is expressed in Am^2, or Bohr magnetons per square nanometer. The moment is expressed per unit area of substrate because detailed investigations as a function of film thickness failed to show any proportionality. The magnetic properties appear to be correlated with the defect structure of the films, which depends on heat transport during deposition. The M samples are better oriented and better crystallised than the R samples. Magnetism is more likely to be observed on oxidised than on unoxidised silicon. Results of the quantitative analysis of an extended series of films will be shown and a comparison of results on hafnium dioxide and tantalum pentoxide will be presented. [1] M. Venkatesan, C. B. Fitzgerald and J. M. D. Coey, Nature 430 630 (2004)

G10.11
Dielectric Properties of High-Pressure Reactive Sputtered and Atomic Layer Deposited Titanium Oxide Thin Films on Silicon. Salvador Duenas[1], Helena Castan[1], Hector Garcia[1], Juan Barbolla[1], Enrique San Andres[2], Ignacio Martil[2], German Gonzalez-Diaz[2], Kaupo Kukli[3] and Jaan Aarik[4]; [1]Electronica, Universidad De Valladolid, Valladolid, Valladolid, Spain; [2]Fisica Aplicada III, Universidad Complutense, Madrid, Spain; [3]Institute of Experimental Physics and Technology, University of Tartu, Tartu, Estonia; [4]Institute of Physics, University of Tartu, Tartu, Estonia.

Titanium dioxide has been one of the most extensively studied oxides because of its remarkable optical and electrical properties. The high dielectric constant of TiO_2 make it a good alternative as gate dielectric for deep-submicron MOSFETs due to the acceptance of titanium in most modern CMOS fabrication facilities. Studies of thin films of TiO_2 typically report dielectric constants that range from 40 to 86. The present work deals with the interface quality of Al/TiO_2/Si metal-insulator-semiconductor (MIS) structures, with TiO_2 being fabricated by using two different methods: high-pressure reactive sputtering (HPRS) and atomic layer deposition (ALD). These methods have been chosen because they induce low values of interface state densities and disordered-induced gap states on the dielectric. ALD thin films were grown on n-type silicon substrates in an ALD flow-type low-pressure (250 Pa) reactor. TiO_2 films were deposited from 3 different precursor systems employing titanium tetrachloride ($TiCl_4$) and titanium ethoxide ($Ti(OC_2H_5)_4$) as the metal precursors and water (H_2O) and hydrogen peroxide (H_2O_2) vapors as the oxygen precursors. The thickness values of the films deposited for electrical measurements ranged from 2.5 to 20 nm. Thermal annealing was used to improve dielectric properties of those films. The annealing has been carried out at 750 °C in purified oxygen under atmospheric pressure for 10 min. HPRS TiO_2/SiO_2 dielectric thin films stacks were grown on n-type silicon substrates. First, a 7 nm SiO_2 film was grown by ECR-CVD. After, 77.5 nm TiO_2 films were grown in a HPRS system at a pressure of 1 mbar during 3 hours , the growing temperature was kept at 200°C and the RF power was 600 W. Finnaly, the samples were annealed in oxygen atmosphere at temperatures ranging from 600 to 900°C. We used C-V, DLTS and Conductance Transient Techniques in order to obtain the electrical characteristics of these films. In particular, we will present a detailed comparison of relevant properties of these films, such as flat-band voltage, interface-state densities and disordered-induced gap state (DIGS) profiles. Unannealed films deposited by HPRS show a great positive flat-band voltage shift which means negative trapped charge in the insulator. Also, C-V curves have a considerable stretch-out as well as hysteresis. However, annealed films both atomic layer deposited and high-pressure sputtered show flat band voltage values very near to 0 V, and their C-V shape are much less distorted, thus indicating better interface quality. Unannealed HPRS films and annealed ALD films have Dit densities of about 4 - 6 x 10^{12} $cm^{-2}eV^{-1}$. However, for annealed HPRS films we obtain Dit values of 1 x 10^{12} $cm^{-2}eV^{-1}$. A more detailed discussion as well as conductance-transient measurement results will be provided at the conference.

G10.12
Gate Technologies for Gallium Nitride in High-Frequency MOSFETs. Mark Johnson[1], Doug Barlage[2] and Dave Braddock[3]; [1]Materials Science and Engineering, NC State University, Raleigh, North Carolina; [2]Electrical and Computer Engineering, NC State University, Raleigh, North Carolina; [3]OSEMI Inc, Rochester, Minnesota.

Insulating gate materials for III-V compound semiconductors have

long been studied for use in potential high-frequency devices. III-V compound semiconductors are attractive for high frequency applications due to the combination of higher bandgap energy, high electron mobility and high breakdown field relative to traditional silicon based devices. Of particular note is the favorable ballistic transport and negative differential resistance under high-fields (nanoscale dimensions), thereby providing physical phenomena for frequencies approaching the terahertz range. However, oxide layers and other insulating gate materials have been generally unsuccessful for III-V compound semiconductor metal oxide semiconductor field effect transistors (MOSFETs) as fermi-level is pinned due to a high density of mid-gap interface states. In recent years, significant advances have been achieved through the epitaxial deposition of complex oxides such as a gallium-oxide / gadolinium-oxide multiple layer gate stack which exhibit low-interface state densities suitable for MOSFET fabrication. Using an epitaxially deposited gate structure, we have fabricated initial MOSFET structures on Gallium Nitride (GaN) which operate in an enhancement mode with electron charge accumulation of $n_s = 4 \times 10^{13}$ cm^{-2}. These proof-of-concept results provide evidence for the prospects of achieving viable MOSFET devices with GaN as a compound semiconductor. GaN is a potential channel material for ITRS devices in the 8-12 year time horizon, particularly as channel dimensions are reduced to nanoscale dimensions. GaN has a bandgap energy of 3.4eV and saturated electron velocity of $v_s = 2.5\text{-}3 \times 10^7$ m/s, as well as a high electron and hole mobilities in bulk material. The high bandgap energy of GaN is advantageous for high-density and sub-10nm gate length devices as it minimizes off-state current and can provides a substantial barrier to unwanted tunneling currents. Additionally, GaN has shown promise as a material for high-density / reduced dimensional structures with nanowires successfully synthesized by vapor-liquid-solid (VLS) and metal-organic chemical vapor deposition (MOCVD). As a result, the combination of excellent transport properties, a viable gate process, proven ohmic contacts and novel nanoscale fabrication processes motivate the investigation of GaN as a possible device material for international technology roadmap for semiconductor (ITRS) applications. In this paper, we review electron transport properties for competing short gate-length nanowire devices to provide a benchmark for comparing potential material solutions such as GaN, Silicon, Se-Ge and carbon nanotubes. The combined structure and properties of GaN MOSFETs offer a compelling option for high-speed applications.

G10.13

Reliability Characteristics of HfO_2 Gate Dielectrics Prepared by Atomic Layer Deposition Using $HfCl_4$ and TEMAH.

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In order to reduce the leakage current of gate oxide with effective oxide thickness of less than 1.5nm, SiO_2 should be replaced with a high-k material such as HfO_2, ZrO_2, Al_2O_3, which allows the use of physically thicker film. The atomic layer deposition (ALD) method is the process of choice due to its excellent capability of thickness control, its ability to obtain good uniformity and low deposition temperature. HfO_2 films were deposited in a traveling wave type ALD reactor using $HfCl_4$ and TEMAH ($Hf[NC_2H_6]_4$) as Hf-precursor and H_2O as oxidant, at a wafer temperature of 300°C on B-doped p-type Si(100) wafers after the native oxide removal by RCA cleaning. MOS capacitors with 100nm-thick Pt electrode were fabricated using a conventional photolithography process. After MOS capacitor fabrication, PMA (post metallization annealing) was performed at 400°C for 30min in forming gas (4% N_2). In this research, the electrical properties of HfO_2 film fabricated by using $HfCl_4$ and TEMAH were measured and compared with the physical/chemical properties of films. Both samples show a negative flatband voltage shift during electrical stress, indicating a net positive charge generation in the HfO_2 film. This positive charge trap could be explained by hydrogen-release at the interface between HfO_2 and Si-substrate. We confirmed that the TEMAH-HfO_2 sample shows significantly less interface trap generation than $HfCl_4$-HfO_2 under the same electrical stress. The effects of Hf-precursor on the ALD HfO_2 films will be discussed in the viewpoint of film composition, chemical structure, and impurity distribution. The comparison of the evaluation resulted from the several analytical techniques such as AES, SIMS, XPS, and TEM-EELS will be addressed in detail. The reliability properties of $HfCl_4$-HfO_2 and TEMAH-HfO_2 under the same electrical stress will be discussed specially with concerning physical/chemical characteristics of HfO_2 film.

G10.14

Effect of High Pressure Post-Metallization Annealing on Electrical and Reliability Characteristics of MOSFET with High-k Gate Dielectric.

Man Chang, M.Shahriar Rahman, Hokyung Park and Hyunsang Hwang; GIST, Gwangju, South Korea.

Hafnium based high-k gate dielectrics were intensively studied for past few years to replace the silicon dioxide in future CMOSFET technologies. Mobility degradation is one of the most difficult problems of the high-k gate dielectric applications. The degraded channel mobility of nMOSFET is responsible for high interface trap density in upper half of the band-gap. In high-k gate dielectrics, high temperature (above 500°C) forming gas (H2/Ar=4%/96%) annealing seems to more efficiently passivates the high-k/Si interface traps. However, high temperature annealing process is incompatible after metallization process. To completely passivate interface states of high-k gate dielectric at relatively low temperature, we have developed a new high-pressure (up to 100atm), pure(100%) hydrogen annealing system. Compared with control (1atm) forming gas (H2/Ar=4%/96%) annealed sample, high pressure(5-20atm), pure H2 annealing of nMOSFET at 400°C shows 10-15% improvements of saturation drain current(Id,sat) and maximum transconductance (gm,max). Using charge pumping method and pulsed I-V hysteresis, significant reduction of interface trap densities and fast trapping sites for high-pressure H2 annealed samples were confirmed. Compare with hydrogen annealing, D2 annealed samples exhibits longer hot carrier lifetime which can be explained by heavy mass effect. By optimizing process parameter, we are able to improve both device performance and reliability characteristics.

G10.15

Work Function of Layered Refractory Metal Electrodes in Metal Oxide Semiconductor Structures.

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Scaling the gate length and oxide thickness of the metal oxide semiconductor field effect transistor (MOSFET) offers great potential to improve device performance and circuit density. However, shrinking the device size reveals fundamental limitations to increased performance using polycrystalline silicon as the gate electrode. Polycrystalline silicon offers process compatibility, self-aligned processing, and a tunable interface work function. However, its susceptibility to depletion and boron penetration are driving the need to investigate alternative gate materials. The use of metals for the gate electrode eliminates these problems, and may also show better compatibility with high-k gate dielectrics with respect to threshold voltage control. However, the work function of metals is not easily tuned, and several methods are being investigated in order to achieve the desired work function values for n and pMOS devices. Bilayer metal structures offer the possibility to tune the interface work function by varying the thickness of the inner metal layer (the layer closest to the oxide). Interestingly, in several systems the work function shows a gradual transition as a function of inner layer thickness, requiring approximately 10 nm before the inner layer dominates the work function. This gradual transition is contrary to theoretical and experimental results, which show that the work function at a surface is sensitive to layers on the order of monolayers. Recent work has shown that interdiffusion between the metals is likely responsible for this gradual transition. Hence the issue of using non-intermixed bilayer electrodes to control interface work function remains open. In this work the work function behavior of W/Nb bilayers, where interdiffusion during processing conditions is expected to be minimal, was investigated. W/Nb bilayers were deposited using DC magnetron sputter deposition, and then patterned into MOS-capacitors. The layer thickness and structure was investigated using x-ray reflectivity. The work function was calculated by plotting the flat band voltage extracted from capacitor CV measurements as a function of dielectric thickness. In contrast to interdiffusing systems, a relatively sharp transition in work function behavior is observed, with the work function being dominated by very thin W inner layers. This shows that the work function can be controlled by atomic scale layers.

G10.16

Ge Nanocrystal Metal-Oxide-Semiconductor Memory with LaAlO3 Tunneling Oxide.

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In this work, a new kind of nonvolatile memory structure using Ge nanocrystals embedded in high-k LaAlO3 (LAO) gate dielectric films has been fabricated and characterized. The Ge nanocrystals and LAO films were grown by laser molecular-beam epitaxy technique, which provided precise control of the size and density of the Ge nanocrystals, and also the thickness of the control and tunneling oxide films. High-resolution transmission electron microscopy study revealed that the diameter of sphere-like Ge nanocrystals was around 6 nm, and the corresponding calculated density of the nanocrystals was about 2E12/cm2. Using capacitance-voltage measurements, we have demonstrated the write and erase process in this novel memory structure. Large flat-band voltage shift of 1.0 V was obtained for the structure of LAO(8 nm)/Ge/LAO(2nm)/Si in the voltage sweep of

5V→-5V→5V. Good charge retention characteristics was also observed by the capacitance-time measurements. These results show that the this memory structure utilizing the Ge nanocrystals with LAO tunneling oxide has a high potential for further scaling of floating gate memory devices.

G10.17

Precise Characterization of Silicon on Insulator (SGOI), SiGe on SOI and Strained Silicon on SiGe on Insulator (SSOI) Stacks with UV-Visible and Infra Red Spectroscopic Ellipsometry. Adrien Darragon, Jean Louis Stehle and Christophe Defranoux; SOPRA, Bois-colombes, France.

Further improvements in CMOS circuit performance such as switching speed and power reduction will rely on the use of silicon on insulator (SOI) substrates with decreased functional thicknesses. According to the International Technology Roadmap for Semiconductors ITRS), the silicon and buried SiO2 (BOX) layer thicknesses for a fully depleted device should the ranges of 10 to 16nm and 24 to 40nm by 2005, respectively. A key issue for fully depleted CMOS transistors is the control of such ultra-thin layers thickness and their uniformity with other parameters such as surface and interface roughness. This is a challenge to metrology, especially to conventional reflectometry technique because the layers thickness must determined with angstrom precision for both silicon cap and SiO2 box layer. Spectroscopic ellipsometry (SE) is an optical and non-destructive technique for determining thin film thickness and material optical properties. Because ellipsometry measures change in the polarization state for both the amplitude ratio of the p to s polarizations, and in phase retardation, it provides a precise way to characterize such ultra thin SOI stacks (10 to 20nm) . Comprehensive characterization results for a number of thin and ultra thin SOI stacks with different thickness ranges will be presented together with measurement repeatability results relevant to the film thickness process tolerances. In addition, characterization results for advanced device applications such as SiGe on SOI (SGOI) and strained silicon-on- SiGe-on-insulator (SSOI) will be shown, demonstrating the use and capability of spectroscopic ellipsometry for precise determination of layer thickness, material composition, interfacial layers, etc. Metrology of other advanced Substrates such as the characterization of very thin Silicon Epi layers, SIC, Silicon on Sapphire (SOS) will also be presented. Principles and advantages of the technique will also be discussed in the presentation.

G10.18

Phase Transformation of HfO2 Thin Films Grown by Liquid Pulsed MOCVD. Karen Dabertrand[1], Andy Zauner[2], Christopher Hobbs[3], Sandrine Lhostis[1], Guy Rolland[4], Olivier Renault[4], Frederic Laugier[4], Philippe Holliger[4], Helmut Metzger[5], Cristian Mocuta[5], Simone Pokrant[2], Denise Muyard[4], Konstantinos Giannakopoulos[6] and Vincent Cosnier[1]; [1]STMicroelectronics, Crolles Cedex, France; [2]Philips, Crolles Cedex, France; [3]Freescale, Crolles Cedex, France; [4]DRT/D2NT, CEA-LETI, Grenoble Cedex, France; [5]ESRF, Grenoble Cedex, France; [6]Electron Microscopy Laboratory, Athens, Greece.

"High-k" dielectrics materials for microelectronics are more and more focused on the Hf-based family. Previous works have shown that the dielectric constant of HfO2 is strongly dependent on its crystal structure. This paper investigates the crystalline structure of HfO2 layers as a function of process parameters (temperature, thickness) and after post-annealing treatments. HfO2 layers were deposited by pulsed-MOCVD (or AVD) Tricent in an Aixtron tool, using Hf-alkoxyl liquid precursor. Using liquid injectors enable to control the precursor amount and thus, a tight control of the thickness in a large process window. Deposition is performed under O2 flow to fully dissociate the precursor molecules and to reduce the carbon content into the layer. Films were grown with different thicknesses (3-12 nm) and at different temperature (400-600C). Deposited films were assessed via their structural and electrical properties. Synchrotron and CuK radiation were used to study grazing-incidence small angle X-ray scattering (GISAXS), grazing-incidence X-ray diffraction (GID), and X-ray reflectivity (XRR) of the films. Transmission Electron Microscopy (TEM) has been also performed to get complementary information. All GISAXS and GID analyses were performed at the European Synchrotron Radiation Facilities (ESRF) on 5 nm HfO2 layers. HfO2 layers deposited at high temperature (550C) are polycrystalline, with a monoclinic or a mixture of orthorhombic and monoclinic phases. The layers did not behave any texture and the grain size is roughly that of the film thickness, as deduced from Scherrer equation. This was confirmed by cross-sectional TEM analysis. Furthermore, XRR indicates sharp interface SiO2/HfO2 and XPS profiles show no silicate formation at the interface. Post annealing, performed at 600C under N2, do not modify the crystal phase, as the film is thermodynamically stable; but annealing contributes to further crystallization of the layer, with oxygen diffusion near the interface. If HfO2 is crystalline at high temperature, it is amorphous-like at lower temperature. Moreover, post RTP anneals up to 600C, used to cure defects (e.g. interfacial states) did not result in crystallization of the amorphous-like layers. TEM analysis, however, reveals the presence of small grains which are embedded in an amorphous matrix. Preliminary works with Hg probe measurement confirm the high-k value dependence according to the micro-crystalline stru

G10.19

Abstract Withdrawn

G10.20

Probing Local Atomic Environments in High-k Gate Stacks on the Nanometre Scale. Maureen MacKenzie[2], Frances T. Docherty[2], Alan J. Craven[2] and David W. McComb[1]; [1]Materials, Imperial College London, London, United Kingdom; [2]Physics and Astronomy, University of Glasgow, Glasgow, United Kingdom.

Replacing Si(ON) by a high k dielectric is still one of the grand challenges of the International Technology Roadmap for Semiconductors. The physical and chemical changes that occur in the as-deposited structures due to the thermal budget required during processing of the gate stack are of particular concern. Only by gaining a clear understanding of these changes and their driving forces can the development of high-k gate stacks be placed on a firm footing. Analytical electron microscopy, in particular electron energy loss spectroscopy (EELS), allows the local atomic environments in the layers and interfaces in gate stacks to be probed with nanometre scale spatial resolution. In this contribution we will discuss how EELS can be used to provide unique insights into the structure-property-processing inter-relationships in these chemically complex multilayer structures.

G10.21

Optimization and Integration of a Long Pulse Laser Thermal Process for Ultra-Shallow Junction Formation of CMOS Device. Julien Venturini[1], Miguel Hernandez[1], Cyrille Laviron[2], Hassan Akhouayri[3] and Jacques Boulmer[4]; [1]SOPRA, Bois-Colombes, France; [2]CEA-G/LETI, Grenoble, France; [3]Institut Fresnel, Marseille, France; [4]IEF, Orsay, France.

We present results on ultra-shallow junction formation for the sub 65 nm CMOS node by means of a Long Pulse Laser Thermal Process (LP-LTP). This method achieve to form abrupt and ultra-shallow junctions with low resistivities, but the different irradiated structures like transistor gates need to be preserved. To assess the integration of the laser process in the fabrication of a CMOS device, we studied two laser process windows enlargement : first, the influence of optical coatings deposited before the laser irradiation in order to protect the structures and second the proper use of the explosive crystallization of pre-amorphized implanted layer during laser irrdiation. Different materials and coating thicknesses have been evaluated on blanket implanted wafers under a long pulse Excimer laser (200ns-15 J) irradiation. The junctions have been characterized by 4-point probe, in-situ reflectivity, UV photometry and transmission electronic microscopy (TEM) pictures. Irradiations have also been performed on coated CMOS structures with 35 nm junctions to assess the integration of the process on a real structure. A selective etching scanning electronic microscope (SEM) view shows that a proper optical coating coupled to the explosive crystallization induced by the long laser pulse optimizes the coupling of the deposited laser energy and improves the integration of the laser activation process of future CMOS junctions.

G10.22

Effect of Process Parameters on the Structral and Electrical Properties of Barium Strontium Titanate Thin Films Grown by LS-MOCVD. Young Kuk Lee, Taek-Mo Chung, Chang Gyoun Kim and Yunsoo Kim; Thin Film Materials Laboratory, Korea Research Institute of Chemical Technology, Taejon, South Korea.

High dielectric materials with a perovskite-structure have attracted much attention in memory devices such as DRAMs or FeRAMs. However, low volatility of the Ba, Sr, or Zr precursors with only THMD ligands has limitations in obtaining high quality thin films due to the low volatility. To improve the volatility of these precursors, many attempts have been made such as adding various ligands to satisfy the coordinative saturation. We report the synthesis of new precursors $Ba(thd)_2(tmeea)$ and $Sr(thd)_2(tmeea)$, where tmeea = tris[2-(2-methoxyethoxy)ethyl]amine, and LS-MOCVD of barium strontium titanate (BST) thin films using these precursors. Due to increased basicity of amines compared with ethers, it is expected that the nitrogen-donor ligand will make a strong bond to a metal than an analogous oxygen-donor ligand, consequently improving the volatility and thermal behavior of these precursors. BST thin films were grown on $Pt(111)/SiO_2/Si(100)$ substrates by LS-MOCVD using a cocktail source consisting of the conventional Ti precursor $Ti(thd)_2(O^iPr)_2$ and these new Ba and Sr precursors. As-grown films were characterized by XPS, SEM, XRD, XRF, and C-V and I-V

measurements. BSTO films grown in the temperature ranges of 400-450 °C were almost stoichiometric with very smooth surface morphology. The maximum dielectric constant was measured up to 460. Dependence of the composition, microstructure and the electrical properties of the BST films on the growth temperature, annealing temperature, anneaing atmosphere and working pressure also will be presented.

G10.23
Study of Dielectric Titanium Dioxide Thin Film Deposited by Plasma-Enhanced Atomic Layer Deposition.
Guoxia Liu[1,2], Fukai Shan[2], Won-Jae Lee[1,2], G. H. Lee[1,2], I. S. Kim[1,2] and B. C. Shin[1,2]; [1]Department of Information Engineering, DongEui University, Busan, South Korea; [2]Electronic Ceramics Center, DongEui University, Busan, South Korea.

Titanium dioxide thin films were deposited by plasma-enhanced atomic layer deposition (PE-ALD) technique with alternating supply of reactant source, Ti[N(CH3)2]4, and oxygen palsma at different temperatures. X-ray diffraction (XRD) was used to investigate the structural properties. It is found that, the thin film deposited at the temperatures lower than 200 centigrade is amorphous; the thin film deposited at temperature higher than 300 centigrade has (101), (200), and (211) orientations which belong to anatase phase. The thin films deposited at low temperatures were annealed at 500, 700, and 900 centigrade in rapid thermal annealing (RTA) system for 1 minute. The amorphous thin films showed anatase phase after annealing in RTA system. Atomic force microscope was used to investigate the surface morphologies of thin films. The as-deposited thin films showed very smooth surface, the roughness is as small as 0.3 nm. The surface of the thin films became rougher with increasing annealing temperature. The transmittance spectra were used to calculate the band gap energies of the thin films. The band gap energies of the thin films were around 3.2 eV. The electrical properties of Pt/dielectric/Si structured films were investigated. The leakage current density was as small as 10-7 A/cm2 up about 1000 kV/cm.

G10.24
Amorphous ABO3 on Si.
Fude Liu[1], Lisa F. Edge[2], Darrell G. Schlom[2] and Gerd Duscher[1,3]; [1]Department of Materials Science and Engineering, North Carolina State University, Raleigh, North Carolina; [2]Department of Materials Science and Engineering, Penn State University, University Park, Pennsylvania; [3]Condensed Matter Division, Oak Ridge National Lab, Oak, Ridge, Tennessee.

Aggressive down scaling of CMOS devices requires the introduction of an alternative insulator to replace SiO2. Generally, there are two groups of possible high-K oxides of technological importance, binary metal oxides and perovskite-type materials. Perovskite-type metal oxides (ABO3) have many unique properties [1]. For CMOS technology, the extremely high dielectric constant of this material class makes them an obvious candidate. A good interface for this application requires either that the perovskite is amorphous, or that it is crystalline with a low density of dangling bonds between it and the underlying silicon. Amorphous perovskites are one solution, as they are expected to be able to adjust their local bonding and reduce the silicon dangling bonds at the interface. However, these ionic materials must be kept amorphous even after post-deposition high-temperature processing in order to maintain a sharp interface and avoid possible additional leakage along grain boundaries. A crystalline oxide on silicon involves more effort, but it avoids the steric hindrance and bond-coordination problems inherent in amorphous oxides [2]. In this study, we concentrate on the former case. Z-contrast imaging, EELS and HRTEM have been applied to study the interfaces of the SrTiO3/Si and LaScO3/Si systems. Especially, the formation of interface layers with different deposition conditions is analyzed. Acknowledgement This work has been funded by the National Science Foundation under contract number DMR 0244724 and the U.S. Department of Energy under contract number DE-AC05-00OR22725. References: [1] Yu et al., Mat. Res. Soc. Symp. Proc. (2003) 747. [2] R. A. McKee,et al., Science, 293 (2001) 468

G10.25
Perowskite Based Alloyed Thin Films with High k as Alternative Gate Oxides for Microelectronic Applications.
Juergen Schubert, Tassilo Heeg and Martin Wagner; ISG 1-IT, Forschungszentrum Juelich GmbH, Juelich, Germany.

The search for a replacement of SiO_2 as gate oxide in microelectronics didn't succeed until now. The materials with high bandgap and high k (HfO_2, $LaAlO_3$ and several silicates) have material specific disadvantages. We have prepared thin films of a new alloy based on perowskite materials using pulsed laser deposition. Epitaxial films were grown on $SrRuO_3$//$SrTiO_3$(100) as well as amorphous films on silicon substrates. The epitaxial films are investigated to measure the physical properties of the crystalline material. We will present the crystallographic characterization of the thin films using RBS/Channeling and XRD-studies. Electrical measurements (CV, leakage current) show for example high $k>35$ for the epitaxial and amorphous films. A diffusion between the new material and silicon is not observed.

G10.26
Characterization of Zr Incorporating Gd2O3 Film.
S. A. Park[1], Y. K. Kim[1], J. H. Baeck[1], I. S. Jeong[1], M. K. Noh[1], K. Jeong[1] and M.-H. Cho[2]; [1]Department of Physics, Yonsei University, Seoul, South Korea; [2]Korea Research Institute of Standards and Science, Daejeon, South Korea.

Gd2O3 films incorporated with ZrO2 were deposited on various substrates with e-beam evaporation by reactive thermal evaporation. X-ray diffraction and RBS data showed that Gd2O3 films incorporated with ZrO2 are superior epitaxial quality to pure Gd2O3 films. The improved crystallinity is caused by suppression of interfacial reaction between rare earth metal Gd and Si substrate. X-ray photoelectron spectroscopy showed that silicide layer between Si and Gd formed in as-grown film and the silicate formation process was prevail over the films after annealing treatment. The reaction at interfacial region influenced thermal stability of the films such as morphology and crystallinity which are confirmed by AFM and X-ray reflectivity data. As the annealing temperature goes up to higher, Ge segregation is observed in the film. In this work, we found that interface reaction in the film was closely related to the substrate and post annealing.

SESSION G11: Gate Dielectrics on Engineered Substrates
Chairs: E. Fitzgerald and M. Orlowski
Thursday Morning, March 31, 2005
Room 2007 (Moscone West)

8:30 AM *G11.1
High Current Drivability MOSFET Fabricated on Si(110) Surface.
Akinobu Teramoto and Tadahiro Ohmi; New Industry Creation Hatchery Center, Tohoku University, Sendai, Japan.

This paper demonstrated the CMOS characteristics on Si(110) surface by using surface flattening process and radical oxidation. By forming a MOS device on Si(110) surface, the high-speed and low flicker noise p-MOSFET can be realized. Furthermore, the current drivability of p-MOS and n-MOS has balanced in the CMOS (balanced CMOS) on Si(110) surface can be also realized. These are very useful to the analog/digital mixed signal circuits. In Current CMOS, the current drivability of p-MOSFET is about 1/3 of that of n-MOSFET. Then, the occupied area of p-MOSFET is 3 times larger than that of n-MOSFET, and each current drivability of p-MOSFET and n-MOSFET is unbalanced. It is well kwon that the hole mobility in the p-MOSFET on Si(110) is much larger than that on Si(100) which is used to current LSI. However, it is also well kwon that a high quality gate oxide cannot be formed except on Si(100) surface. We have reported that the radical oxidation using microwave-excited very low electron temperature plasma can form the high quality oxide which has low fixed charge density and low interface trap density on every silicon surface; as a result, every silicon surface can be employed for LSI fabrication. The current drivability of p-MOSFET on Si(110) surface can be 3 times larger than that on Si(100) surface by using the radical gate oxide formation. However, the electron mobility on SI(110) surface is 0.6 times less than that on Si(100) surface. It is considered that the surface micro-roughness on Si(110) surface is very large compared with Si(100) surface, and the electron mobility in the channel on Si(110) surface is more sensitive against interface micro-roughness than that on Si(100) surface. We employ the 5-step room temperature clean which consist all acid solution; as a result, the silicon surface is not etched by cleaning solutions and the surface micro-roughness on Si(110) can be reduced. The electron mobility in n-MOSFET on Si(110) surface can be improved and flicker noise in MOSFETs can be reduced by using the surface flattening by the isotropic oxidation, such as high temperature wet oxidation, and the 5-step room temperature clean which does not generate the surface micro-roughness. The balanced CMOS that is constructed by same current drivability n-MOSFET and p-MOSFET can consist on Si(110) surface. By using the balanced CMOS, the NOR circuit is same area and same oscillation frequency as the NAND circuit, although the are of NOR circuit is larger than that on NAND circuit on Si(100) surface. In the CMOS switch which is usually used in analog circuits, the offset of output voltage becomes small since parasitic capacitance balances between n- and p-MOSFETs by using the balanced CMOS.

9:00 AM *G11.2
Advanced High-Mobility Semiconductor-On-Insulator Materials.
Bruno Ghyselen, Ian Cayrefourcq, Fabrice Letertre, Takeshi Akatsu, George Celler and Carlos Mazure; SOITEC, Bernin,

France.

SOI is today the substrate of choice for several applications, including high performance, low voltage, and low power consumption ICs. Although the adoption of SOI enables extending silicon based IC capabilities, the ITRS roadmap poses additional technological challenges. New technological solutions are being explored in order to boost circuit performance for the next logic and mixed signal generations. Increasing the charge carrier mobility has been identified as one necessary requirement to meet the future demands. Some solutions to increase mobility are based on local strain that can be induced in Si CMOS transistor channels by transistor manufacturing steps such as nitride spacer deposition or SiGe pockets formation: the so-called local strain or process-induced strain approach. This approach has an advantage that it seems to depend only on the precise tuning of some basic deposition or etch steps at the transistor level. However, this method is clearly dimension (scalability), transistor technology and design dependent. The strain that needs to be initially applied and the way it transfers to the point of use (CMOS channel) depend on many aspects of device, circuit architecture, and processing. In this paper, we will review several alternative solutions to increase mobilities at the substrate level. Such solutions, which may be combined with process-induced strain, have as the main advantage that they transfer the high mobility building and engineering concerns to the starting material level, adding value to the starting substrates and simplifying the tasks of device designers and process engineers. Among the different substrate level approaches to increased mobilities in SOI architectures, we will focus on three main families: (1) moving to strained Si and/or SiGe layers On Insulator, (2) moving to monocrystalline Ge-On-Insulator substrates and (3) re-visiting crystalline orientation effects on mobilities through specific combinations of crystalline orientations of semiconductor layers on Insulator. The attractiveness at the device level of those material based solutions is largely fixed and may be measured by their compatibility with CMOS integration processes, standard MOSFET architectures, and circuit layouts. In each case, we will give an overview of the development status at the substrate level. Different material manufacturing techniques will be considered, and the potential of wafer bonding and layer transfer techniques (such as Smart Cut TM) will be highlighted. Results of in-depth physical characterization of these substrates will be shown in order to demonstrate the present quality of the advanced High-mobility Semiconductor-On-Insulator materials of interest. Those results, in addition to the remaining technical challenges to be met at the substrate level, will serve to show for which of the ITRS technological roadmap nodes those families of innovative substrates will bring appropriate enabling solutions.

9:30 AM G11.3
Surface Orientation Dependence of Inversion Carrier Mobilities in HfAlOx CMOS Fabricated on (100), (110) and (111) Si Substrates. Hiroyuki Ota[1], Kenji Okada[2], Hideki Satake[2] and Akira Toriumi[1,3]; [1]MIRAI-ASRC, AIST, Tsukuba, Ibaraki, Japan; [2]MIRAI-ASET, Tsukuba, Ibaraki, Japan; [3]The Univ. of Tokyo, Bunkyo-ku, Tokyo, Japan.

The inversion layer mobility degradation is one of critical issues in high-k MOSFETs, and the degradation mechanism should be urgently clarified. This paper discusses the inversion layer carrier mobilities of high-k MOSFETs on various surface-orientated Si, which is expected to offer invaluable information on the carrier scattering mechanism. Since the scattering rate ${\tau_c}^{-1}$ is proportional to the density of state mass m_d in a two dimensional electron system, we introduce a new parameter of effective mass independent scattering rate η^{-1} as $\eta^{-1}={m_d}^{-1}{\tau_c}^{-1}$, where ${\tau_c}^{-1} = (e/m_c)mu$, e, m_c, and mu are the electronic charge, the conductivity mass and the inversion carrier mobility, respectively. By using η^{-1}, we can compare the mobility values on different surface orientations from the viewpoint of the effective mass independent scattering rate. Both n- and p-channel MOSFETs with n^+ poly-Si gate electrodes were fabricated on (100), (110) and (111) Si substrates. The channel direction was along <110> for all of the devices. 4 nm-thick $HfAlO_x$ (Hf: 60 at.%) films were deposited on thermally oxidized interfacial SiO_2 layers (1.6 nm) by the LL-D&A process [1]. MOSFETs with conventional SiO_2 were also fabricated. It was found that the mobility of $HfAlO_x$ p-MOSFETs on (110) is 2.3 times larger than the universal hole mobility on (100), thus p-MOSFET on (110) seems to be promising for advanced CMOS. However, it was certainly degraded when compared with (110) SiO_2 p-MOSFET and more detailed analysis is needed. Concerning the scattering mechanisms in the inversion layer, the η^{-1} of hole for (111) was similar to that for (110), and larger than that for (100). This is understandable by the enhanced interface state scattering, because the interface state densities of the $HfAlO_x$ gate stack on (110) and (111) were twice as large as that of (100). On the other hand, η^{-1} of electron is in order of (100), (110), and (111). This fact cannot be simply explained by the difference of the interface state density. We consider that the spatial distribution of the wave function in the inversion layer on the three orientation substrates may explain the experimental results. In summary, the following conclusion was obtained from the surface orientation dependence of the effective mass independent scattering rate η^{-1}: in the case of hole, the scattering is the interface sensitive, while in the case of electron it is determined not only by the interface but also by the wave function characteristics. These results suggest a guideline for improving the inversion layer mobility. This work was supported by NEDO. [1] T. Nabatame *etal.*, VLSI Symp. Tech. Dig., p 25 (2003).

9:45 AM G11.4
Interdiffusion Studies Under Oxidative Conditions in Si-Ge Heterostructures. Nevran Ozguven and Paul C. McIntyre; Materials Science and Engineering, Stanford University, Stanford, California.

In this study, we explore two different conditions of interdiffusion in SiGe heterostructures. First, we present the results of interdiffusion measurements on single crystal $Si_{1-x}Ge_x/Si_{1-y}Ge_y$ superlattices grown by low-pressure chemical vapor deposition (LPCVD) onto Si (001) substrates. The effects of Si surface oxidation, a well-established method for injection of interstitial defects into silicon, on Si-Ge interdiffusion is studied. An epitaxial Si cap, which is partially consumed during dry O_2 post-anneals, is grown on these superlattices for the oxidation experiments. The interdiffusion kinetics is measured via high resolution superlattice x-ray diffraction (XRD), which involves monitoring the decay of x-ray (000) or (004) superlattice satellites as a function of annealing time. The effect of oxidation on the interdiffusivity of Si and Ge is studied over the temperature range 770°C to 870°C and we show the effect of Ge concentration on the interdiffusion kinetics. We also explore the effects of direct oxidation of a LPCVD-grown $Si_{1-x}Ge_x$ layer prepared on a SOI (100) substrate. In this case, thermal oxidation is carried out at temperatures below the melting point of $Si_{1-x}Ge_x$. This is a possible means of preparing high mobility Ge-rich semiconductor channels on insulator for future high performance transistors. During oxidation the Ge atoms are rejected from the SiO_2 layers, and their out-diffusion is suppressed by the top and buried oxides. As a result, the thickness of the SiGe layer decreases and the Ge concentration in the SiGe layer increases. Transmission electron microscopy (TEM) is used to measure the thickness and to observe the crystal quality of the resulting Ge-rich layer. The Ge fraction in the SiGe layer as a function of process conditions is determined using XRD and Rutherford backscattering.

SESSION G12: Physical & Electrical Characterization-II
Chairs: M. Houssa and S. Takagi
Thursday Morning, March 31, 2005
Room 2007 (Moscone West)

10:30 AM *G12.1
High Dielectric Constant Oxide Stacks on Germanium for CMOS: Materials Challenges. Supratik Guha[1], James Chen[2], Sanjay Banerjee[2], Edward Preisler[5], Nestor Bojarczuk[1], Michael Gribelyuk[3], Alex Zaslavsky[4], B. R. Perkins[4] and D. Kazazis[4]; [1]IBM T. J. Watson Research Center, Yorktown Heights, New York; [2]Electrical Engineering, University of Texas at Austin, Austin, Texas; [3]IBM Microelectronics Division, East Fishkill, New York; [4]Electrical Engineering, Brown University, Providence, Rhode Island; [5]Jazz Semiconductor, Newport Beach, California.

There is much activity today towards replacing the Si/SiO2 interface with a Si/high-k oxide stack in silicon MOSFETs. This work has in turn stimulated discussion for replacing the silicon itself with germanium for a Ge/high-k interface as a basis for a future CMOS technology. The development of insulating high-k dielectrics on germanium is at a preliminary stage compared to silicon. However, several clear differences have emerged, related generally to the lower temperature stability of germanium and the relative instability of germanium oxide compared to silicon oxide. We will describe the effects of these differences in developing processes for optimizing the electrical quality of Ge-HfO2 and Ge-Al2O3 interfaces. We show that it is relatively easy(compared to Si) to grow dielectric stacks that have very low electrical thickness on Ge. At the same time we demonstrate, through mobility measurements on Ge-HfO2 MOSFETs, that the reduction in electrical thickness comes at the cost of reduced carrier mobility for samples that were similar in all other aspects. This is observed in both p and n FETs and the reason for this is not clear. It however questions the perceived benefits of adopting a Ge based CMOS approach. A Ge CMOS technology also needs to be based upon a germanium-on-insulator (GOI) platform. We will describe our efforts at growing ultrathin epitaxial germanium on crystalline insulator structures. We demonstrate simple back gated MOSFETs made from such structures and show that it is possible to obtain fully depleted effects in such devices.

11:00 AM *G12.2
Atomic Layer Deposition of High-k Dielectrics on Ge and GaAs. Marco Fanciulli, Laboratorio Nazionale MDM, Istituto Nazionale per la Fisica della Materia, Agrate Brianza, Italy.

The scaling down of modern nano-electronic devices, based on a MOS structure, has motivated an intense activity on high-k dielectrics. Although a large number of materials have been investigated, suitable candidates have not been identified yet. A possible intrinsic problem could be also related to the reduction of the effective electron mobility in the inversion layer of the Si substrate due to remote phonon scattering. High-mobility substrates such as Ge, despite the lower junction breakdown voltage and difficulties in the etching steps, and GaAs are now reconsidered for MOSFET applications due to the availability of a variety of insulating materials. The application of the atomic layer deposition (ALD) process on Ge and III-V compound semiconductors opens new opportunities for semiconductor devices. The growth, by ALD, and characterization of high-k dielectrics (HfO2 and Rare Earth Oxides) on Ge and GaAs will be discussed with particular emphasis on the semiconductor/oxide interface structure and physical and chemical properties, such as composition, defects, and band offsets.

11:30 AM G12.3
Soft X-ray Photoemission Studies of HfO2 on Ge (001). Kang-ill Seo[1], Shiyu Sun[2,3], Dong-Ick Lee[1,3], Piero Pianetta[3], Krishna C. Saraswat[4] and Paul C. McIntyre[1]; [1]Materials Sci.ence and Engineering, Stanford University, Stanford, California; [2]Physics, Stanford University, Stanford, California; [3]Stanford Synchrotron Radiation Laboratory, Stanford University, Stanford, California; [4]Electrical Engineering, Stanford University, Stanford, California.

Recently, high-k dielectrics on Ge channels have been studied widely for MOSFET applications to take advantage of the high intrinsic electron mobility (2x) and hole mobility (4x) of Ge, compared to that of Si, and to avoid using poor quality germanium oxide as a gate dielectric by adapting high-k films developed for Si CMOS technology. As a high-k gate insulator on Ge, GeOxNy, ZrO2, HfO2 and Al2O3 have recently been studied. Although many promising results have been reported, such as low gate leakage current density and enhanced hole mobility, little attention has focused on the chemical nature of the interfacial layer between high-k and Ge and the associated energy band alignment at the interface. In this presentation, we report the chemical bonding structure and valence band alignment at the HfO2/Ge (001) interface by systematically probing various core level spectra as well as valence band spectra using synchrotron x-rays at beam line 8-1 of the Stanford Synchrotron Radiation Laboratory. We investigated chemical bonding changes as a function of depth through the dielectric stack by taking a series of XPS spectrum as we etched through the HfO2 film using diluted HF-solution. The photon energy was tuned to achieve high surface sensitivity. First, we used atomic force microscopy to confirm that 2% HF-solution etching does not deteriorate the HfO2 film by increasing surface roughness or generating pin holes. By analyzing Ge 3d core levels precisely, we found that a very thin GeOx layer of ~0.3nm thickness with highly non-stoichiometric chemical nature exists at the HfO2/Ge interface. The valence band spectra near the Fermi level for each etched film structure were carefully fitted, and as a result, the valence band offset between Ge and GeOx was determined to be Ev(Ge) - Ev(GeOx) = ~2.2 eV, and between Ge and HfO2, Ev(Ge) - Ev(HfO2) = ~2.7 eV. The implications of this highly non-stoichiometric GeOx interfacial layer and the observed energy band alignment for electrical properties such as C-V and I-V characteristics will be discussed.

11:45 AM G12.4
Characterization of MBE Grown HfO_2 films on Ge(001). Claudia Wiemer[1], Grazia Tallarida[1], Sandro Ferrari[1], Marco Fanciulli[1], Sascha Kremmer[2], Christian Teichert[2], Jin Won Seo[4], Christel Dieker[4] and Athanasios Dimoulas[3]; [1]MDM-INFM, Agrate Brianza, Mi, Italy; [2]Institute of Physics, University of Leoben, Leoben, Austria; [3]MBE Laboratory, NCSR, Paraskevi Attikis, Greece; [4]Institute of Physics of Complex Matters, EPFL, Lausanne, Switzerland.

The structural and chemical properties of HfO_2 deposited on germanium strongly influence the electrical behaviour of metal-oxide-germanium capacitors and therefore the integration of high-κ dielectrics on high mobility substrates. Due to the poor electrical quality and thermal stability of germanium oxide, growing HfO_2 on Ge and assuring a high quality interface is of primary interest. The morphology, as well as the stoichiometry and thickness of the interlayer deposited, or developed during the growth, and its influence on the HfO_2 film must be addressed. In this work we investigate the structural and chemical properties of HfO_2 films deposited on Ge by molecular beam epitaxy at different temperatures (60-360 °C). The films were grown on Ge (001) either on a 2×1 reconstructed surface, or on a GeO_xN_y layer. Very smooth and dense HfO_2 films are obtained on all the investigated surfaces. The crystallisation of HfO_2 is influenced by the deposition temperature and by the nature of the starting Ge surface. Time of flight secondary ion mass spectrometry depth profiles show Ge diffusion into the HfO_2 deposited on GeO_xN_y. This result is confirmed by energy dispersive x-ray spectroscopy profiles of cross section high-resolution transmission electron microscopy images. Spatially resolved current maps, obtained by conducting-AFM at fixed bias voltage, show that the presence of 'weak' spots, where a high current between the probe and sample is detected, is related to the nature of the interfacial layer, as well as to the crystallinity of the HfO_2 film.

SESSION G13: Metal Gates and FUSI Gates-II
Chairs: E. Gusev and H. Shang
Thursday Afternoon, March 31, 2005
Room 2007 (Moscone West)

1:30 PM *G13.1
Gate Work Function and Fermi Level Pinning on HfO2 Dielectrics. John Robertson and Ka Xiong; Engineering, Cambridge University, Cambridge, United Kingdom.

High dielectric constant or high K oxides are needed to replace silicon dioxide as the gate oxide in future CMOS devices. The favoured oxide is HfO2. High K gate oxides have a narrower band gap than SiO2 and therefore their band alignment pinning factor S is less than 1, the Schottky limit. There has been considerable debate about the implications of this for the choice of work functions for metal gates [1], and the related question of Fermi level pinning at poly-Si gate electrodes on HfO2 [2]. First we note that photoemission [3] and internal photoemission data [4] confirm a value S~0.5 for HfO2, for S in dimensionless units. This is the same as expected theoretically by the MIGS model [5]. Second, Yeo et al [1] then argued that for dual metal gates on HfO2, this requires the NMOS and PMOS metal work functions would need to be separated by Eg/S or ~2 eV, which is practically impossible (Eg is the band gap of Si). This leads to the belief that metal gates cannot easily be implemented with HfO2 gate oxides and low threshold voltages, despite the fact that some firms have actually done it [6]. We argue here that this model not true. Dual metal gates does not correspond to a change in work function applied to a single system, but to two separate systems of gates on n-Si and p-Si substrates. The work function difference needed is then nearer Eg. Thirdly, we model the apparent pinning of the work function at HfO2:poly-Si gate stacks [2], and show that partial pinning by Hf-Si bonds is consistent with the experimental observation. We have constructed various atomic models of an abrupt HfO2:Si interface [7] for mainly O-termination and partial Hf-Si bonding. Unlike the HfO2:channel interface which can contain a thin SiO2 interfacial layer and is likely to be O-rich, the HfO2:poly-Si interface is likely to be abrupt and contain some Hf-Si bonds because it is formed in a O-poor ambient. 1. Y C Yeo, T J King, C Hu, J App Phys 92 7266 (2002) + IEEE ED Letts (2001) 2. C Hobbs et al, Tech digest VLSI (2003); C C Hobbs et al, IEEE Trans ED 51 971 (2004); ibid 51 978 (2004) 3. S Sayan,.., J Robertson, E Garfunkel, Proc ECS (2004-01) p255 4. V V Afanaseev, M Houssa, A Stesmans, M M Heyns, J App Phys 91 3079 (2002) 5. J Robertson, J Vac Sci Technol B 18 1785 (2000) 6. P Chau et al, IEEE ED Letts 25 408 (2004) 7. P W Peacock, J Robertson, Phys Rev Letts 92 057601 (2004)

2:00 PM G13.2
Gate Metal/HfO_2 Interactions in MOSFET Stacks: Dissolved Oxygen and Other Pitfalls. Matthew Copel, E. J. Preisler, R. Pezzi, N. A. Bojarczuk, M. C. Reuter, E. Gusev, S. Guha and F. R. McFeely; IBM, Yorktown Hts, New York.

Recent interest in metal-gated high-k MOSFET stacks has led us to investigate reactions between "inert" metals and HfO_2. pFET candidates such as W and Re are valued for their lack of reactivity. Yet under certain conditions, reactions can take place. Dissolved oxygen in the gate metal is a particular problem, since it can react with the silicon substrate to increase buffer layer thickness during high temperature processing. In extreme cases, there is an increase in Tinv of up to 20$\AA$ due to the formation of interfacial oxides between the HfO2 and the silicon. Both structural probes (medium energy ion scattering) and electrical measurements point to the importance of oxygen solubility in metals, which is high in many candidate gate stack electrodes. We find the strict control of dissolved oxygen is critical to maintaining low EOT in thermal processing of metal-gated HfO_2 FETs. Reduction of gate dielectrics is another possible difficulty, potentially altering device thresholds and ultimately causing unacceptable leakage characteristics.

2:15 PM G13.3
Fermi-Level Pinning of Fully Silicide Gate Electrode on Hf-Silicate Gate Insulator. Kazuaki Nakajima, Seiji Inumiya, Akio

Kaneko, Soichi Yamazaki, Kazuhiro Eguchi and Yoshitaka Tsunashima; Toshiba Corporation, Semiconductor Company, Yokohama, Japan.

Metal gate electrode without gate depletion and B penetration is required to realize high performance CMOSFETs for hp 45nm generation and beyond. Fully silicide gate processing is attractive technology for realizing metal gate transistors, since it is compatible with conventional Si processing. However, it is reported that work function of fully silicide gate electrode on high-k dielectric differs from that of fully silicide gate electrode on SiO2. Therefore, in order to clarify the root causes of this phenomenon, we studied the workfunction of various kinds of fully silicide gates on HfSiON gate insulator. In this report, we discuss about a thermal stability of fully silicide gate and a controllable range of workfunction on both SiO2 and HfSiON gate insulator. In this study, we formed MOS capacitors to measure workfunctions of various fully silicide gates. At first, a SiO2 gate insulator is thermally grown on Si substrates. Oxide thickness is varied from 5nm to 10nm. A HfSiON film with thickness of 4.5nm is deposited on the SiO2. A 100nm thick Poly-Si film is deposited on the HfSiON/SiO2 stacked gate insulator. Poly-Si gate is formed by dry etching. On the Poly-Si gate, various metal films, such as Ni, Co, Pt, and Er, are deposited. Silicide formation is carried out by annealing at the range of temperature from 250°C to 450°C for 1hours in a N2 ambient. After the silicide formation, unreacted metal is removed. Finally, forming gas annealing is carried out at 450°C for 1hour. We obtained work functions of metal silicide gates from flat band voltage as a function of dielectric film thickness by C-V We examined thermal stability of fully silicide gate on both SiO2 and HfSiON gate insulator. In Ni2Si gate, a fully silicide is completely formed at 350°C. At annealing temperature of silicide formation above 400°C, leakage current of MOS capacitor with HfSiON gate insulator degraded. On the other hand, no degradation is observed on MOS capacitor with SiO2 gate insulator at annealing temperature of 450C. The degradation of electrical property is due to diffusion of Ni atoms into the HfSiON gate insulator. Work function of Ni2Si gate electrode on SiO2 and on HfSiON gate insulator are 4.66eV and 4.73eV, In PtSi gate, no degradation is observed on MOS capacitor with HfSiON gate insulator at annealing temperature of 450°C. In order to examine the interface between PtSi and gate insulator, we observed the cross section by TEM. No apparent interaction of PtSi/HfSiON is observed. However, work function of PtSi gate electrode on HfSiON The work function of metal silicide on the SiO2 was successfully controlled from 3.9eV to 4.8eV by using ErSi1.7 and PtSi gate electrode. The controllable range of workfunction of these fully silicide gate is 0.9eV. On the other hand, the controllable range of work function was found to be so narrow as 0.34eV on the HfSiON gate insulator, even though rare earth metal silicide and noble metal silicide are used.

2:30 PM G13.4
Intermixing in NiSi/HfO2/SiOx/Si Gate Stacks.
Michael Gribelyuk[3,1], Cyril Cabral[2,1], Nestor Bojarczuk[2,1], Supratik Guha[2,1], Evgeni Gusev[2,1] and Vijay Narayanan[2,1]; [1]Semiconductor Research and Development Center, IBM, Hopewell Junction, New York; [2]Research Division, T. J. Watson Research Center, IBM, Yorktwon, New York; [3]Systems and Technology Group, IBM, Hopewell Junction, New York.

Implementation of fully silicided metal gates (FUSI) together with high-k gate dielectrics provides a promising path toward further scaling of semiconductor CMOS devices. A combination of High resolution TEM (HRTEM) and a 0.5nm small probe electron energy loss spectroscopy (EELS) has been applied to study interfacial reactions between metal gate, NiSi, and high-k gate dielectric, HfO2. NiSi was found to be polycrystalline with the grain size varying from 5nm to 10nm. Some 2nm large Si regions were found between the NiSi grains. On the other hand, some NiSix grains at NiSi/MOCVD HfO2 interface were matched by lattice images to a Ni-rich m-Ni3Si phase, thus confirming a non-uniform distribution of Ni both in bulk and at the interface and incomplete silicidation. EELS analysis has shown presence of Ni in HfO2 gate dielectric (but not in underlying Si oxide film!). The same conclusion was drawn from analysis of lattice spacings of some crystalline grains of Hf oxide in HRTEM images: they could not be matched to any of reported Hf oxide phases whereby the best match was found for the Ni21Hf8 alloy. A monolayer of Si3N4 grown by MBE between Hf oxide and NiSi to prevent intermixing was found ineffective: HRTEM and EELS data showed similar results as in the stack without Si nitride.

2:45 PM G13.5
Combinatorial Study of Metal Gate Compatibility on HfO_2.
Martin L. Green[1], Kao-Shuo Chang[2], Toyohiro Chikyow[4], Ahmed Parhat[4], John Suehle[1], Eric Vogel[1], Prashant Majhi[3] and Ichiro Takeuchi[2]; [1]NIST, Gaithersburg, Maryland; [2]University of Maryland, College Park, Maryland; [3]Sematech, Austin, Texas; [4]NIMS, Tsukuba, Japan.

The Si microelectronics community is currently faced with major materials challenges to further scaling. The SiO_2/polycrystalline Si gate stack that has served the industry for 35 years must now be entirely replaced with one having a higher capacitance and lower power dissipation. At a minimum, the interfaces of the HfO_2/metal gate electrode advanced gate stack must be thermally stable with respect to interfacial reactions, and the changes in electrical properties that would ensue. In this talk, we will describe research aimed at understanding the thermal as well as electrical stability of metal gate electrode layers on HfO2, a likely high-k gate dielectric. Combinatorial methodologies, ideally suited for this problem since a wide variety of metal electrode layers will be examined, will be utilized to determine the ideal composition and structure of the metal gate electrode. An ideal metal gate stack is one in which the work function is properly matched to HfO_2, and the interface between the HfO_2 and the electrode is stable under typical processing conditions. We will determine the band structure at the HfO_2/metal gate electrode interface through the extraction of appropriate parameters from I-V and C-V capacitor measurements, and internal photoemission and Kelvin probe measurements. Typical of the metal gate alloy systems that will be investigated are binary and ternary combinatorial "libraries" containing Ru, Ta, W, Pt, Al, and Si. We will also present data for polycrystalline Si gates on HfO_2, for comparison.

SESSION G14: Transistor Processing and Characterization-II
Chairs: M. Heyns and M. Meuris
Thursday Afternoon, March 31, 2005
Room 2007 (Moscone West)

3:30 PM *G14.1
Ge Based High Performance Nanoscale MOSFETs.
Krishna C. Saraswat[1], Chi On Chui[1], Tejas Krishnamohan[1], Ammar Nayfeh[1] and Paul McIntyre[2]; [1]Department of Electrical Engineering, Stanford University, Stanford, California; [2]Department of Materials Science and Engineering, Stanford University, Stanford, California.

It is believed that the difficulty in scaling the conventional Si MOSFET makes it prudent to search for alternative device structures, new material and fabrication technology solutions that are generally compatible with current and forecasted installed Si manufacturing. The saturation of Si MOSFET drain current upon dimension shrinkage limits the prospect of future scaling. It has been recently pointed out that a fundamental scaling limit for MOSFETs is the source injection velocity into the channel limiting the drain current. The lower effective mass (and lower valley degeneracy) of Ge could alleviate the problem by providing a higher source injection velocity, which translates into higher drive current and smaller gate delay. Heteroepitaxial growth of Ge on Si, surface passivation for gate dielectric and field isolation and n-type dopant incorporation are classic problems that obstruct CMOS device realization in Ge. In this paper we present a review of the recent activity in this area. Using a novel multi-step growth and hydrogen anneal process we have grown heteroepitaxial-germanium layers directly on silicon, with defects confined near the Si/Ge interface, thus not threading to the surface as expected in this 4.2% lattice mismatched system. The results achieved are defect-free fully-relaxed smooth single crystal Ge layers on Si without any graded buffer SiGe layer. High mobility MOSFETs have been demonstrated in bulk Ge and in nanowires with high-k gate dielectrics and metal gates. In order to enhance performance and continue scaling MOSFETs to the sub-20nm regime, novel, high-mobility materials like strained-Si and Ge (or Si_xGe_{1-x}) are actively being researched for incorporation into the channel. We demonstrate novel heterostructures with high mobility center channel, double gate N and PFETs that incorporate novel transport principles, which fully exploit the advantage of high mobility.

4:00 PM G14.2
MOSFET with La_2HfO_7 and HfO_2 High-k Dielectrics Integrated in a Conventional Flow. Luigi Pantisano[1], Thierry Conard[1], Martine Claes[1], M. Demand[1], Wim Deweerd[1], Stefan Degendt[1], Marc Heyns[1], Michel Houssa[1], Marc Aoulaiche[1], Guilherme Lujan[1], Lara-Ake. Ragnarsson[1], Erika Rohr[1], Tom Schram[1], J. C. Hooker[2], Z. M. Rittersma[2], Jean Fompereyne[3], Jean Pierre Locquet[3] and A. Dimoulas[4]; [1]SPDT / Hirel, IMEC, Leuven, Belgium; [2]Philips Research Leuven, Leuven, Belgium; [3]IBM Research, Ruschlikon, Switzerland; [4]NCSR "Demokritos", Athens, Greece.

N-channel MOSFET were fabricated in a conventional etched gate flow using either 15A SiON or bare silicon (HF-last) as starting surface. LaHfO or HfO2 were deposited in an 8in Riber MBE tool. LaHfO or HfO2 were considered with a physical thickness in the 3-6nm range. TaN was used as gate material. Since LaHfO was found to be hydrophilic and soluble in acid solutions, no polymer removal step was done after gate etching. The gate was spacer-encapsulated

for protection during the silicidation. The process thermal budgets have the dopant activation (1000C spike for HfO2 or 900C 10s for LaHO) and forming gas annealing. The EOT extracted from large area capacitors was ranging from 15A up to 22A. The extracted k-value for the LaHfO is in the order of 14 and 24 for HfO2. The Vfb vs. EOT plot indicates that little fixed charge is present in these stacks. Functional MOSFET were obtained down to L=100nm. However poor short channel behavior / performances were found due to the high resistivity of the non-optimised TiSi2 junctions (in the order of 1KOhm) and process flow (especially for the LaHfO). In the following only the long channel performance will be discussed. The performance of these MOSFET was benchmarked measuring the gate current JG @ VT+1V and the peak Gm. The former measures the leakage in a dielectric at operating conditions (i.e., fixed overdrive). The latter is a quantity proportional to the mobility and the EOT. For MBE HfO2 similar / better performances were found compared to other deposition techniques, especially for thin oxides. Consistent with this picture, the channel electron mobility was also rather high (in the order of 300 cm2/Vs for an EOT of 16A and an interfacial layer of 12A±2A). For LaHfO the leakage reduction was dramatic at operating conditions (JG~10-7 A/cm2 @ VT+1V). To further analyze the electrical properties of these materials, the transient VT-instability was measured. It is well known that high-k dielectrics may have a large density of pristine traps that may be charged / discharged during the Id-Vg measurement [Kerber et al., IEEE IRPS 2003]. The Id-Vg hysteresis measured in the μs time range can help to quantify / benchmark the number of electrically active traps in these materials. Within the instrument resolution (~10mV) even at high bias (VG=2V) negligible VT-instability was found in all LaHfO stacks suggesting that very little pristine traps are present in these layers. Conversely, at the same time and bias range the HfO2 was exhibiting a large VT-instability (~150mV), similar to what found in other experiments [Kerber et al., IEEE IRPS 2003]. **Conclusions:** For the first time 100nm MOSFET fully processed on an 8in tool were demonstrated with an etched gate approach for MBE-deposited HfO2 and LaHfO. Good mobility was found for HfO2 MOSFET. Similar mobilities and very low leakage was observed in LaHfO samples. Negligible VT-instability found in n-channel MOSFET with LaHfO.

4:15 PM G14.3
Strained Silicon MOSFETs with Hafnium Dioxide Gate Dielectrics and Metal Gate Electrodes. Yanxia Lin, Veena Misra and Mehmet Ozturk; Dept. of Electrical and Computer Engineering, North Carolina State University, Raleigh, North Carolina.

A thin Si layer grown on relaxed $Si_{1-x}Ge_x$ is under biaxial tensile strain and it can provide mobility enhancement for both electrons and holes. Incorporation of high-K dielectrics on strained silicon is necessary to fulfill the continuous scaling requirements with the additional benefit of low gate leakage current. Also, the degradation in carrier mobility due to high-K/polysilicon gate stack can be partially compensated by using strained Si. To eliminate gate depletion problems and Fermi level pinning associated with polysilicon electrodes, metal gates are also necessary. In this paper, strained-Si MOS capacitors and MOSFETs were fabricated with SiO_2 and HfO_2 as gate dielectrics and Ru-Ta alloy and TaN as metal gate electrodes. Strained Si layers were grown on relaxed SiGe virtual substrates by ultrahigh vacuum rapid thermal chemical vapor deposition (UHV/RTCVD). HfO_2 was deposited by physical vapor deposition (PVD) of thin Hf layers followed by either oxidation at 600 ^oC in N_2 for 30 seconds or ultraviolet ozone oxidation. Different metal gate electrodes, both elemental metal and binary metal alloys, were deposited by PVD. Devices on bulk Si with same gate stacks were fabricated as controls. The effect of metal gate electrodes on the channel strain will be discussed by presenting a comparison of electrical characteristics between strained Si MOSFETs with SiO_2 as gate dielectrics and either polysilicon or metal gate electrodes. Also, the interfacial layer formation of strained Si/high-K system and the impact of Ge on strained Si channels will be investigated by a comparison of strained Si/SiO_2 and strained Si/high-K MOSFETs with polysilicon gate electrodes. Finally, the electrical properties of strained Si/high-K/metal gate electrode MOSFETs will be presented to understand the effects of metal gate electrodes on high-K dielectrics and the corresponding effects on mobility degradation.

4:30 PM G14.4
Physical Properties of Thin Nitrided Hf Silicates and their Impact on the Performance of Advanced Transistors having a TaN Metal Gate Electrode. Florence Cubaynes[1], Cees van der Marel[2], Marco Hopstaken[2], Sven van Elshocht[3], Jean-Luc Everaert[3] and Marc Schaekers[3]; [1]Philips Research, Leuven, Belgium; [2]Philips Research, Eindhoven, Netherlands; [3]IMEC, Leuven, Belgium.

Hafnium-based dielectric in combination with a metal gate electrode are seen as the best option to further scale Metal Oxide Semiconductor (MOS) devices while keeping low power consumption. HfO2 gate dielectrics have the advantage of having a higher dielectric constant (K) than nitrided silicon oxides yielding lower gate leakage current for a given equivalent oxide thickness (EOT). However, HfO2 films feature disadvantages such as low crystallization temperature and channel mobility degradation when integrated in MOS devices. Si and N atoms have been incorporated in HfO2 films to mainly improve their thermal stability. This work investigates the impact of each individual processing step to form a high quality HfSiON film. The physical properties of these films were investigated using XPS and ToF-SIMS techniques. The impact of the physical properties of these HfSiON films on the electrical behavior of MOS devices having a TaN metal gate has also been studied. The Hf silicates were deposited by MOCVD using two recipes yielding two Hf concentrations: Hf/Hf+Si = 15 % (Si-rich) and 35 % (Hf-rich). We observed that Hf atoms are directly bonded to O and only indirectly to N or Si atoms (next nearest neighbor). After nitridation, a shift of the N1s and Si2p peaks towards lower binding energies showed that N is mainly bonded to Si in the HfSiON matrix. This result is in good agreement with the larger amount of N measured in the Si-rich HfSiON films. Two nitridation techniques were investigated: an anneal in NH3 and a plasma nitridation. Much higher N concentrations were measured for the plasma nitrided HfSiON: N/O=50 % and 10 % for plasma nitrided and NH3 annealed films, respectively. The N profiles were also very different: a homogeneous distribution of N in the film was observed for the plasma nitrided films while N was observed at the interface with Si for the NH3 annealed films. It was found that an anneal prior to nitridation densified the silicate making the film more resistive to N incorporation. Finally, the performance of transistors with similar gate dielectrics has been investigated. Although lower leakage current was measured at a given EOT for devices having a Hf-rich HfSiON (higher K), the channel mobility of these devices was degraded resulting in poor device performance. The interface quality of the films was improved by performing an anneal prior to nitridation yielding higher channel mobility. However, these films exhibited a significant EOT increase for the same physical thickness (lower K) limiting their scalability. While EOTs decreased as a function of increasing N concentration, it was found that the N profile had a strong impact on the threshold voltage stability: larger hysteresis was measured on transistors with a NH3 annealed dielectric. In summary, we conclude that best device performance was achieved with transistors having a Si-rich plasma nitrided HfSiON gate dielectric.

4:45 PM G14.5
Molybdenum-Gate MOSFET Threshold Voltage Modification Based on Two-Dimensional Nitrogen Distribution Control in Gate Electrode. Takuji Hosoi, Masaki Hino, Kousuke Sano, Norihiro Ooishi and Kentaro Shibahara; Research Center for Nanodevices and Systems, Hiroshima University, Higashi-Hiroshima, Japan.

Metal gate technology is expected to resolve the problem of poly-Si gate depletion. Since single gate material with dual-workfunction is required for the existing CMOS integration process, workfunction tuning technique for several metals has been extensively investigated. Although nitrogen ion implantation into Mo demonstrated the sufficient workfunction shift [1], it also causes damage to gate oxide and interface [2]. Nitrogen solid-phase diffusion (N-SPD) from TiN deposited on Mo is a promising candidate for an alternative method because of less damage and large flat band voltage (V_{FB}) shift of about -0.5 V [3,4]. However, the shift was not reflected to threshold voltage (V_{th}) for MOSFETs fabricated with this technique. We have found out an origin of this discrepancy and have investigated how to modify V_{th} of MOSFETs. Nitrogen pileup at Mo/SiO_2 interface, which is considered to be an origin of the workfunction shift [4], has been confirmed by secondary ion mass spectroscopy (SIMS) and electron energy loss spectroscopy (EELS). Mo gate MOSFETs fabricated using N-SPD, in which TiN/Mo/SiO_2 (30 nm/50 nm/5 nm) stack was formed prior to N-SPD (800 °C, 1 min), showed only a slight V_{th} shift due to nitrogen redistribution during subsequent S/D (source and drain) activation annealing (900 °C, 1 min) [4]. In that fabrication process, TiN was removed just after N-SPD, and Mo gate was exposed to an atmosphere during the annealing. The fabrication process has been modified to control the nitrogen redistribution as follows. (a) Mo gate was covered by CVD SiO_2 film to prevent nitrogen out diffusion (oxide-cover). (b) TiN/Mo stack was covered by CVD SiO_2 and N-SPD was accompanied by S/D activation anneal (TiN-cap). In the case of oxide-cover process, V_{th} shift is still very small (<0.1 V). This is because that nitrogen was divided between four Mo/SiO_2 interfaces, bottom, sides, and top, and nitrogen concentration at each interface reduced. On the other hand, V_{th} shift of about -0.5 V was obtained in the TiN-cap process. However, when the gate length is scaled down to less than 2 μm, V_{th} shift decreases toward about -0.3 V. This can be also explained by reducing the nitrogen pileup at bottom interface of Mo gate with increasing the aspect ratio of Mo (gate thickness / gate length). The MOSFET characteristics exhibit no damage to gate leakage current and slight reduction in electron mobility. Furthermore, the gate oxide reliability is comparable to poly-Si/SiO_2/Si MOSFET. These results indicate that the N-SPD to Mo gate is a potential technique for CMOS

fabrication. This work was partly supported by STARC. [1] P. Ranade et al., Mat. Res. Soc. Proc. **611** (2001) C.3.2.1. [2] T. Amada et al., Mat. Res. Soc. Proc. **716** (2002) 299. [3] R.J.P. Lander et al., Mat. Res. Soc. Proc. **716** (2002) 253. [4] M. Hino et al., Ext. Abst. on Solid State Devices and Materials (2004) 494.