TUESDAY

ORAL PRESENTATIONS

* Invited Paper

Reliability and Ruggedness I

Session Chairs: Alberto Castellazzi and Peter Losee
Tuesday Morning, September 19, 2017
Thurgood Marshall Ballroom, North Salon
8:30 am – 10:00 am

8:30 AM TU.D1.1
Reliability of SiC Power Devices against Terrestrial Neutron Single-Event Burnout
Daniel J. Lichtenwalner[1], Akin Akturk[2], James McGarrity[2], Jim Richmond[1], Thomas Barbieri[3], Brett Hull[1], Dave Grider[1], Scott Allen[1] and Palmour W. John[1]; [1]Wolfspeed, A Cree Company, United States; [2]CoolCAD Electronics LLC, United States; [3]Wolfspeed, A Cree Company, United States.

8:45 AM TU.D1.2
Switching Reliability of SiC-MOSFETs Containing Expanded Stacking Faults
Ryusei Fujita, Kazuki Tani, Kumiko Konishi and Akio Shima; Hitachi, Japan.

9:00 AM *TU.D1.3
Reliability Challenges for SiC Power Devices in Systems and the Impact on Reliability Testing
Nando Kaminski; University of Bremen, Germany.

9:30 AM *TU.D1.4
Extreme Environment SiC Integrated Circuits
Carl-Mikael Zetterling; Royal Institute of Technology (KTH), Sweden.

10:00 AM BREAK

Manufacturing Innovations

Session Chairs: Anant Agarwal and Kimimori Hamada
Tuesday Morning, September 19, 2017
Thurgood Marshall Ballroom, North Salon
10:30 am – 12:00 pm

10:30 AM TU.C1.1
Investigation of Forward Voltage Degradation Due to Process-Induced Defects in 4H-SiC MOSFET
Kumiko Konishi, Ryusei Fujita, Yuki Mori and Akio Shima; Hitachi, Japan.

10:45 AM TU.C1.2
TLS-Dicing(TM) for SiC – Latest Assessment Results
Dirk Lewke[2, 1], Mercedes Maria Barreto[1], Karl O. Dohnke[3], Hans-Ulrich Zuehlke[2], Martin Schellenberger[1] and Christian Belgardt[2]; [1]Fraunhofer Institute for Integrated Systems and Device Technology IISB, Germany; [2]3D-Micromac AG, Germany; [3]Infineon Technologies AG, Germany.

11:00 AM TU.C1.3
In-Coming and In-Line Defectivity Control Solutions for Silicon Carbide Manufacturing
Daniel Arias[1], Mario Coppola[2], Nicolò Piluso[2], Simona Lorenti[2], Marcello Coco[2], Giovanni Franco[2], Antonella Di Salvo[2], Somanchi Anoop[1] and Paolo Parisi[1]; [1]KLA-Tencor, France; [2]STMicroelectronics, Italy.

11:15 AM TU.C1.4
Characterization of pn-Diode Fabricated from Surface Damage-Free 4H-SiC Wafer Using Si-Vapor Etching Process Satoshi Torimi[1], Norihito Yabuki[1], Takuya Sakaguchi[1], Masato Shinohara[1], Youji Teramoto[1], Satoru Nogami[1], Makoto Kitabatake[1] and Junji Senzaki[2]; [1]Toyo Tanso Co., Ltd., Japan; [2]National Institute of Advanced Industrial Science and Technology, Japan.

11:30 AM *TU.C1.5
History, Status and Prospects of Packaging Technology for SiC MOSFETS
David Levett; Infineon Technologies, Germany.

Focused Topics in SiC Epitaxy

Session Chairs: Al Burk and Hidekazu Tsuchida
Tuesday Morning, September 19, 2017
Thurgood Marshall Ballroom, West Salon
8:30 am – 10:00 am

8:30 AM *TU.A1.1
Status and Trends in Epitaxy and Defects
Hiroshi Osawa; Showa Denko K.K., Japan.

9:00 AM TU.A1.2
CVD Filling of Narrow Deep 4H-SiC Trenches in a Quasi-Selective Epitaxial Growth Mode
Shiyang Ji[1], Ryoji Kosugi[1], Kazutoshi Kojima[1], Kazuhiro Mochizuki[1], Yasuyuki Kawada[1, 2], Kohei Adachi[1], Yoshiyuki Yonezawa[1], Sadafumi Yoshida[1] and Hajime Okumura[1]; [1]National Institute of Advanced Industrial Science and Technology, Japan; [2]Fuji Electric Co., Ltd, Japan.

9:15 AM TU.A1.3
99.9% BPD Free 4H-SiC Epitaxial Layer with Precisely Controlled Doping upon 3 x 150 mm Hot-Wall CVD
Keiji Wada, Takemi Terao, Hironori Itoh, Takaya Miyase, Tsutomu Hori, Hideyuki Doi, Masaki Furumai and Tatsuya Tanabe; Sumitomo Electric Industries, Ltd., Japan.

9:30 AM TU.A1.4
Triangular Defects Reduction of 4H-SiC Epitaxial Growth in a Planetary Reactor
Weili Lu, Jia Li, Yulong Fang, Jiayun Yin and Zhihong Feng; Hebei Semiconductor Research Institute, China.

9:45 AM TU.A1.5
Wide-Range Control of Carrier Lifetimes in 4H-SiC Epilayer by V Doping
Koichi Murata[1], Takeshi Tawara[2, 3], Anli Yang[1], Tetsuya Miyazawa[1] and Hidekazu Tsuchida[1]; [1] Central Research Institute of Electric Power Industry, Japan; [2]National Institute of Advanced Industrial Science and Technology, Japan; [3]Fuji Electric Co., Ltd., Japan.

10:00 AM BREAK

Defects in MOS Devices

Session Chairs: Sarit Dhar and Tsunenobu Kimoto
Tuesday Morning, September 19, 2017
Thurgood Marshall Ballroom, West Salon
10:30 am – 12:00 pm

10:30 AM *TU.B1.1
Performance and Reliability Impacts of Extended Epitaxial Defects on 4H-SiC Power Devices
Edward R. Van Brunt, Al Burk, Daniel J. Lichtenwalner, Robert Leonard, Shadi Sabri, Donald A. Gajewski, A. Mackenzie, Brett Hull, Scott Allen and Palmour W. John; Wolfspeed, A Cree Company, United States.

11:00 AM TU.B1.2
Characterization of Traps at SiO_2/ SiC (000-1) near the Conduction Band Edge by Using Hall Effect Measurements
Tetsuo Hatakeyama[1], Yuji Kiuchi[1], Mitsuru Sometani[1], Dai Okamoto[2], Shinsuke Harada[1], Hiroshi Yano[2], Yoshiyuki Yonezawa[1] and Hajime Okumura[1]; [1]AIST, Japan; [2]University of Tsukuba, Japan.

11:15 AM TU.B1.3
A Method for Analyzing Traps at the SiO2/4H-SiC Interface Directly from Transfer Characteristics of 4H-SiC n-MOSFETs
Martin Hauck, Heiko Weber and Michael Krieger; Friedrich-Alexander-Universität Erlangen-Nürnberg (FAU), Germany.

11:30 AM TU.B1.4
Determination of Performance-Relevant Trapped Charge in 4H Silicon Carbide MOSFETs
Fabian Rasinger[1, 2], Gregor Pobegen[1], Thomas Aichinger[3], Heiko Weber[2] and Michael Krieger[2]; [1]KAI Kompetenzzentrum Automobil- u. Industrieelektronik GmbH, Austria; [2]FAU Erlangen, Germany; [3]Infineon Technologies Austria, Austria.

11:45 AM TU.B1.5
Oxide Traps Probed by Transient Capacitance Measurements on Lateral SiO_2/4H-SiC MOSFETs
Patrick Fiorenza[1], Ferdinando Iucolano[2], Mario Saggio[2] and Fabrizio Roccaforte[1]; [1]CNR-IMM, Italy; [2]STMicroelectronics, Italy.

Low Voltage SiC MOSFETs I

Session Chair: Takashi Nakamura
Tuesday Afternoon, September 19, 2017
Thurgood Marshall Ballroom, North Salon
1:30 pm – 3:00 pm

1:30 PM TU.D2.1
650 V, 7 mΩ 4H-SiC DMOSFETs for Dual-Side Sintered Power Modules
Qingchun J. Zhang[1], Matthew McCain[1], Brett Hull[1], Jeff Casady[1], Scott Allen[1], Palmour W. John[1], Monty Hayes[2], Aditya Neelakantan[2] and John Fruth[2]; [1]Wolfspeed, A Cree Company, United States; [2]Delphi LLC, United States.

1:45 PM TU.D2.2
1.2 kV 4H-SiC Split-Gate MOSFET—Analysis and Experimental Results
Kijeong Han[1], Bantval J. Baliga[1] and Woongje Sung[2]; [1]North Carolina State University, United States; [2]State University of New York Polytechnic Institute, United States.

2:00 PM TU.D2.3
Switching Characterization of 1.2 kV 4H-SiC Power MOSFETs and Si IGBTs at Cryogenic and High Temperatures
Jinwei Qi, Kai Tian, Zhangsong Mao, Jindou Liu, Song Yang, Wenjie Song, Shenhui Ma and Anping Zhang; Xi'an Jiaotong University, China.

2:15 PM TU.D2.4
Practical Design of 4H-SiC Superjunction Devices in the Presence of Charge Imbalance
Md Monzurul Alam[1], Dallas T. Morisette[1] and James A. Cooper[1, 2]; [1]Purdue University, United States; [2]Sonrisa Research, Inc., United States.

2:30 PM *TU.D2.5
SiC MOSFET Device Parameter Spread and Ruggedness of Parallel Multichip Structures
Alberto Castellazzi[1], Asad Fayyaz[1] and Rainer Kraus[2]; [1]University of Nottingham, United Kingdom; [2]University of Bundeswehr, Germany.

3:00 PM BREAK

High Voltage SiC MOSFETs

Session Chairs: Brett Hull and Ljubisa Stevanovic
Tuesday Afternoon, September 19, 2017
Thurgood Marshall Ballroom, North Salon
3:30 pm – 4:45 pm

3:30 PM TU.D2.6
3 kV, 13.5 mΩcm² 4H-SiC Reverse Blocking MOSFET with a Non-Punch-Through Drift Layer
Seigo Mori[1], Masatoshi Aketa[1], Takui Sakaguchi[1], Hirokazu Asahara[1], Takashi Nakamura[1] and Tsunenobu Kimoto[2]; [1]ROHM Co., Ltd., Japan; [2]Kyoto University, Japan.

3:45 PM TU.D2.7
Development of a High Performance 3,300V Silicon Carbide MOSFET
Leonid Fursin, Xing Huang, Xueqing Li, Ke Zhu, William Simon and Anup Bhalla; United Silicon Carbide, Inc., United States.

4:00 PM TU.D2.8
Impact of Embedding Schottky Barrier Diodes into 3.3 kV and 6.5 kV SiC MOSFETs
Koutarou Kawahara, Shiro Hino, Koji Sadamatsu, Yukiyasu Nakao, Toshiaki Iwamatsu, Shuhei Nakata, Shingo Tomohisa and Satoshi Yamakawa; Mitsubishi Electric, Japan.

4:15 PM TU.D2.9
3300V SiC Planar DMOSFETs Fabricated on 150mm Substrates
Blake Powell, Sauvik Chowdhury, Chris Hundley and Kevin Matocha; Monolith Semiconductor Inc., United States.

4:30 PM TU.D2.10
4600 V SiC DMOSFETs with $R_{on,sp}$ = 17.5 mΩ-cm²
Siddarth Sundaresan, Stoyan Jeliazkov and Ranbir Singh; GeneSiC Semiconductor, United States.

Fundamental Characterization

Session Chairs: Robert Devaty and Masashi Kato
Tuesday Afternoon, September 19, 2017
Thurgood Marshall Ballroom, West Salon
1:30 pm – 3:00 pm

1:30 PM *TU.B2.1
High Resolution Optical Spectroscopy of Free Exciton and Electronic Band Structure near the Fundamental Gap in 4H SiC
Walter M. Klahold, Wolfgang J. Choyke and Robert P. Devaty; University of Pittsburgh, United States.

2:00 PM TU.B2.2
Reliable Measurement of Silicon Carbide Thermal Conductivity
Björn Lundqvist, Robin Karhu, Ivan G. Ivanov, Jawad Ul Hassan and Olof Kordina; Linköping University, Sweden.

2:15 PM TU.B2.3
Diffusion of the Carbon Vacancy in A-Cut and C-Cut N-Type 4H-SiC
Marianne E. Bathen[1], Hussein Ayedh[1], Lasse Vines[1], Ildiko Farkas[2], Erik Janzén[2] and Bengt Svensson[1]; [1]University of Oslo, Norway; [2]Linköping University, Sweden.

2:30 PM TU.B2.4
Kinetics Modeling of the Carbon Vacancy Thermal Equilibration in 4H-SiC
Hussein Ayedh[1], Roberta Nipoti[2], Anders Hallén[3] and Bengt Svensson[1]; [1]University of Oslo, Norway; [2]Consiglio Nazionale delle Ricerche, Italy; [3]Royal Institute of Technology KTH, Sweden.

2:45 PM TU.B2.5
Processing Induced Surface Paramagnetic Defects in 4H-SiC
Nguyen T. Son, Robin Karhu, Pontus Stenberg, Valdas Jokubavicius, Olof Kordina and Jawad Ul Hassan; Linkoping University, Sweden.

3:00 PM BREAK

MOS Interface Defects

Session Chairs: Ulrike Grossner and Nadeemullah Mahadik
Tuesday Afternoon, September 19, 2017
Thurgood Marshall Ballroom, West Salon
3:30 pm – 4:45 pm

3:30 PM TU.B3.1
Evidence of Carbon-Related Defects at the SiC MOS Interface and Mechanism of Defect Passivation by Nitridation and Phosphorus Treatment—Chemical Analyses Combined with DFT Calculations
Takuma Kobayashi[1], Yu-ichiro Matsushita[2], Takafumi Okuda[1], Atsushi Oshiyama[2] and Tsunenobu Kimoto[1]; [1]Kyoto University, Japan; [2]The University of Tokyo, Japan.

3:45 PM TU.B3.2
Atomistic Insight into Carbon Defects at Thermally Grown SiC/SiO_2 Interfaces—Theory and Experiment
Dipanwita Dutta[1], Alla Sologubenko[2], Deb De[3], Shantanu Roy[3], Stefan Goedecker[3], Massimo Camarda[1], Joerg Lehmann[4], Giovanni Alfieri[4], Holger Bartolf[4], Adolf Schöner[5] and Thomas Jung[1, 3]; [1]Paul Scherrer Institute, Switzerland; [2]ETHZ, Switzerland; [3]Uni Basel, Switzerland; [4]ABB, Switzerland; [5]Ascatron, Sweden.

4:00 PM TU.B3.3
Exploring the Buried SiO_2/SiC Interface by Soft X-Ray ARPES
Judith Woerle[1, 2], Vladimir N. Strokov[1], Hans Sigg[1], Jens Gobrecht[1], Ulrike Grossner[2] and Massimo Camarda[1]; [1]Paul Scherrer Institut, Switzerland; [2]ETH Zürich, Switzerland.

4:15 PM TU.B3.4
DC Bias Dependence of Local Deep Level Transient Spectroscopy Signal and Quantitative Two-Dimensional Imaging of SiO_2/SiC Interface Trap Density
Norimichi Chinone[1], Ryoji Kosugi[2], Yasunori Tanaka[2], Shinsuke Harada[2], Hajime Okumura[2] and Yasuo Cho[1]; [1]Tohoku University, Japan; [2]National Institute of Advanced Industrial Science and Technology, Japan.

4:30 PM TU.B3.5
Investigation of Trap Behavior in SiC MOSCAPs with High Temperature High Frequency Method
Zhaoyang Peng[1], Shengkai Wang[1], Yun Bai[1], Yidan Tang[1], Ximing Chen[2], Chengzhan Li[3], Kean Liu[3] and Xinyu Liu[1]; [1]Institute of Microelectronics of Chinese Academy of Sciences, China; [2]University of Electronic Science and Technology of China, China; [3]Zhuzhou CRRC Times Electric Co., Ltd, China.

Tutorial

SiC Power Electronic Applications

Session Chair: Victor Veliadis
Tuesday Afternoon, September 19, 2017
Thurgood Marshall Ballroom, North Salon
5:45 pm – 6:45 pm

5:45 PM
15 kV IGBT Converters and High Voltage Circuit Topologies
Subhashish Bhattacharya, North Carolina State University

6:15 PM
Heavy-Duty Vehicle Inverter
Brij Singh, John Deere Electronic Solutions

WEDNESDAY

ORAL PRESENTATIONS

* Invited Paper

Applications and Package Integration

Session Chairs: Anup Bhalla and Peter Friedrichs
Wednesday Morning, September 20, 2017
Thurgood Marshall Ballroom, North Salon
8:30 am – 10:30 am

8:30 AM *WE.D1.1
SiC MOSFETs for Multi-MW PV Inverters—Opportunities and Challenges
Ljubisa Stevanovic; GE Global Research, United States.

9:00 AM WE.D1.2
30-kW All-SiC Inverter with 3D-Printed Air Cooled Heatsinks for Plug-in and Full Electric Vehicle Applications
Madhu Chinthavali; Oak Ridge National Laboratory, United States.

9:15 AM WE.D1.3
Module and System Considerations to Maximize Performance Advantages of SiC Power Devices
Ty R. McNutt[1], Kraig Olejniczak[2], Stephen Minden[2], Daniel Martin[2], Jonathan Hayes[2], Ajith Wijenayake[2] and David Simco[2]; [1]Wolfspeed, A Cree Company, United States; [2]Wolfspeed, A Cree Company, United States.

9:30 AM WE.D1.4
Impact of a Kelvin Source Connection on Discrete High Power SiC-MOSFETs
Christian Bödeker[1], Edgar Ayerbe[2] and Nando Kaminski[1]; [1]University of Bremen, Germany; [2]Wolfspeed, A Cree Company, United States.

9:45 AM WE.D1.5
The Development of High Thermal Conductivity SiC Power Modules through the Implementation of Advanced Cooling Techniques Coupled with High Heat Transfer Materials
Brandon Passmore, Brice McPherson and Alex Lostetter; Wolfspeed, A Cree Company, United States.

10:00 AM WE.D1.6
Benefits of High Voltage SiC Applications in Medium Voltage Power Distribution Grids
Shiqi Ji[1], Xiaojie Shi[2], Zheyu Zhang[1], Wenchao Cao[1] and Fred Wang[1]; [1]University of Tennessee Knoxville, United States; [2]EPRI, United States.

10:15 AM WE.D1.7
30 kV Pulse Diode Stack Based on 4H-SiC
Vladimir A. Ilyin[2], Alexey V. Afanasyev[2], Yuri S. Demin[2], Boris V. Ivanov[2], Alexey F. Kardo-Sysoev[3], Victor V. Luchinin[2], Sergey A. Reshanov[1], Adolf Schöner[1], K. A. Sergushichev[2] and A. A. Smirnov[2]; [1]Ascatron AB, Sweden; [2]St. Petersburg Electrotechnical University "LETI", Russian Federation; [3]Ioffe Physical Technical Institute of the Russian Academy of Science, Russian Federation.