SYMPOSIUM N

Novel Materials and Processes for Advanced CMOS

December 2 – 4, 2002

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SESSION N1: HIGH-k CHARACTERIZATION - I
Chairs: Jon-Paul Maria and Susanne Stemmer
Monday Morning, December 2, 2002
Room 202 (Hynes)

8:30 AM *N1.1
HIGH-PERMITTIVITY GATE DIELECTRICS: A MATERIALS EMPHASIS. Angus I. Kingon and Jon-Paul Maria, Department of Materials Science and Engineering, North Carolina State University, Raleigh, NC.

This tutorial will cover the recent rapid developments in the field of alternative, high permittivity gate dielectrics for Si logic and memory devices. The tutorial will first sketch the needs and requirements in terms of Si scaling and the Semiconductor Industry Association Roadmap, and provide a brief history of developments over the past 5 years. Thereafter, the tutorial will describe the issues of materials selection, and continue to describe the most promising current materials including the rare earth oxides, and their alloys with silicon dioxide. The materials issues will be emphasized, including interactions between Si and the dielectrics, thermodynamic stability under a variety of processing conditions, and the impact on properties (both MOS capacitor and transistor). The tutorial will conclude with a description of the major remaining issues for the gate stack, and some comments regarding the outlook. The tutorial will establish links to papers to be presented in the symposium.

10:00 AM *N1.2
PROBING THE ATOMIC-SCALE PROPERTIES AND INTERFACIAL LAYERS IN HIGH-K GATE DIELECTRICS USING SCANNING TRANSMISSION ELECTRON MICROSCOPY. David A. Muller, Bell Labs, Lucent Technologies, Murray Hill, NJ; Glen D. Wilk, Agere Systems, Murray Hill, NJ; Shriram Ramanathan, Stanford University, CA.

The mere presence of an interface between a high-k dielectric and the silicon channel results in (at the very least) a monolayer of material whose environment is neither like that of silicon nor that of the high-k dielectric. In many cases, it takes more than a single monolayer for the bulk properties to be recovered. This has two consequences: first, if reaction layers form at both the channel and gate electrode interfaces then a considerable fraction of the dielectric film is comprised of the interfacial phases. Second, the interfacial region may well have different electronic properties and chemical reactivities to that of the bulk material. Consequently, consideration of bulk thermodynamics is a necessary, but not sufficient condition in predicting the formation of interfacial layers. For instance, we have detected thin (<0.5 nm) layers of SiO_2 at Al_2O_3 /Si, and Zr-silicate/Si,interfaces, neither of which would have been predicted from bulk thermodynamics. Atomic-resolution scanning transmission electron microscopy, which has the sensitivity and resolution to detect a single impurity atom buried in a crystal[1], can also provide spectroscopic information on buried interfaces with 0.3 nm or better spatial resolutionl[2]. These direct measurements of local electronic structure allow us to correlate or even identify the origins of macroscopically measurable defect properties such as fixed charge. 1. P.M. Voyles, D.A. Muller, J.L. Grazul, P.H. Citrin, and H.-J. Gossmann, *Nature*, **416** 826 (2002). 2. D.A. Muller, T. Sorsch, S. Moccio, F.H. Baumann and G. Timp, *Nature*, **399**, 758-761 (1999).

10:30 AM N1.3
CHARGE TRAPPING STUDIES ON HIGH-k GATE STACKS GROWN BY ROOM TEMPERATURE ULTRAVIOLET-OZONE OXIDATION. Shriram Ramanathan, David Chi, Stanford Univ., Dept. of Materials Science and Engineering, Stanford, CA; Supratik Guha, Evgeni Gusev, IBM Watson Research Center, Yorktown Heights, NY; Paul C. McIntyre, Stanford Univ., Dept. of Materials Science and Engineering, Stanford, CA.

High-dielectric-constant oxides are presently being investigated for application as alternate gate dielectrics in future CMOS devices. Several metal oxides such as ZrO2 and HfO2 have been considered to be potential candidates owing to their high dielectric constant, large bandgap and predicted thermodynamic stability on silicon. Developing processing science and detailed electrical characterization methods are extremely important in order to integrate these new materials into conventional CMOS process flows. In particular, charge trapping in high-k gate stacks has been identified as one of the major fundamental issues for high-k integration. In addition, there is also an effort to develop metal gates to replace polysilicon as gate electrodes. So far, there have been few reports on the effect of top electrode deposition on the long-term electrical behavior of the gate stacks. This paper deals in particular with the charge trapping characteristics of ZrO2 and HfO2 gate stacks grown by the method of room temperature ultraviolet ozone oxidation. Thin films of zirconia and hafnia of varying thicknesses were grown on ultra-thin SiO2 underlayers. Three different conditions were chosen for the platinum top electrodes: in-situ sputtering, ex-situ sputtering and ex-situ electron beam evaporation. Capacitors with 1 nm equivalent electrical oxide thickness, negligible frequency dispersion and CV hysteresis were fabricated with ZrO2/SiO2 gate stacks. The leakage current was nearly four orders of magnitude lower than that of SiO2 films with similar thickness. It was found that capacitors fabricated by ex-situ methods showed a larger electrical thickness presumably due to interfacial layer growth. Detailed charge trapping studies were performed on both zirconia and hafnia dielectrics. Capacitors fabricated with in-situ Pt electrodes displayed little charge trapping while ex-situ samples showed a significant flatband voltage shift with bias stress. Results on the effects of top electrode deposition on the CV curves, leakage current characteristics and charge trapping will be presented in detail.

10:45 AM N1.4
THERMAL ANALYSES OF BULK AMORPHOUS OXIDES AND SILICATES OF ZIRCONIUM AND HAFNIUM. S.V. Ushakov, A. Navrotsky, Thermochemistry Facility, Dept of Chemical Engineering and Materials Science, Univ of California at Davis, Davis, CA; A. Demkov, B.-Y. Nguyen, C. Wang, Materials Theory and Simulations Physical Sciences Research Labs, Motorola, Inc., Tempe, AZ.

Oxides and silicates of zirconium and hafnium are of interest as alternative gate dielectrics for advanced CMOS. It is beneficial to have them amorphous to prevent effects associated with grain boundaries, but their thermal stability is of concern. While properties of amorphous zirconium and hafnium oxides and silicates prepared in bulk may differ from those in thin films, some energetic and structural trends are common and may be revealed from study of bulk materials. The crystallization of bulk amorphous ZrO_2, HfO_2 and HfO_2/ZrO_2-SiO_2 is studied here as part of ongoing research on thermochemistry of alternative gate dielectrics. Pure and Y-doped bulk amorphous Zr and Hf hydrous oxides were synthesized by precipitation from corresponding oxychlorides with ammonia or hydrazine. Surface areas were estimated by nitrogen adsorption and samples were characterized by thermogravimetry coupled with evolved gas analyses (TGA-EGA), differential scanning calorimetry (DSC) and high-temperature X-ray diffraction (HT XRD). Samples of amorphous zirconia with surface area 10 - 216 m^2/g crystallized to the metastable tetragonal phase at 423 $\pm$4°C with change in enthalpy of -21 $\pm$2 kJ/mol. Amorphous hafnium oxide samples were prepared with surface area from less than 10 to 160 m^2/g. HfO_2 crystallized directly in the monoclinic structure. Crystallization temperatures of HfO_2 were found to increase from 472 $\pm$10 to 539 $\pm$8°C with increasing surface area while crystallization enthalpy was in the range -31$\pm$3 kJ/mol for all samples. Doping with up to 8 mol % of Y_2 O_3 did not result in significant changes of crystallization temperatures of hafnium and zirconium oxides with low surface area. Crystallization of ZrO_2 was retarded up to ~890°C in ZrO_2 -SiO_2 (1:1) gel prepared by precipitation from tetraethoxysilane and zirconium oxychlorides. The crystallization enthalpies from DSC measurements are compared with enthalpies changes related to stable modifications measured by high-temperature oxide melt solution calorimetry. Applications of thermal analyses and solution calorimetry techniques for dielectric films characterization are discussed.

11:00 AM N1.5
THERMAL STABILITY OF HIGH-K LAYERS. Chao Zhao, Olivier Richard, Sven Van Elshocht, Hugo Bender, Matty Caymax, Wilfried Vandervorst, Stefan De Gendt, Marc Heyns, IMEC, Leuven, BELGIUM; Vincent Cosnier, ST Microelectronics, c/o IMEC; Jerry Chen, Texas Instrumnets Inc., c/o IMEC; Gert Roebben, Omer Van Der Biest, KU Leuven, MTM, Leuven, BELGIUM; Jan Maes, ASM International NV, c/o IMEC; Edward Young, Philips, c/o IMEC.

Morphology stability during thermal processes in conventional CMOS processing is a basic requirement for high-k dielectrics. This presentation summarizes our experimental observations on the thermostability of amorphous phases in various high-k layers (Al2O3, ZrO2, HfO2, Zr-aluminate and Hf-aluminate) as well as the phase transformation behavior of crystalline ZrO2 and HfO2, as functions of surface preparation, deposition conditions and technique, material composition and post deposition thermal treatment. It is found that pure ZrO2 and HfO2 show relatively low crystallization onset temperatures. The crystalline ZrO2 or HfO2 phases are tetragonal or monoclinic, depending on the layer thickness. The phase transformation of meta-stable tetragonal phases into stable monoclinic phase has been observed widely in pure HfO2, but has never been found in ZrO2 layers thinner than 7nm. Crystallization behavior of Al2O3 depends on the surface preparation of the substrate. ALCVD grown Al2O3 layers on an oxide-based surface remain amorphous after 1100°C spike annealing, while those on HF-last surface show a crystallization onset temperature around 800°C. It is demonstrated that alloying Al2O3 into ZrO2 and HfO2 can improve their resistance to crystallization under thermal exposure. In certain composition ranges, Zr-aluminates and Hf-aluminates have crystallization onset

temperatures higher than 900°C. Hf-aluminates show better thermal stability than Zr-aluminates. A defect model relative to the phase transformation is discussed, based on the above observation.

11:15 AM N1.6
INVESTIGATION OF DEFECTS AT THE HIGH-k OXIDE/(100)Si INTERFACE BY MAGNETIC RESONANCE TECHNIQUES.
S. Baldovino, G. Scarel and M. Fanciulli, Laboratorio MDM-INFM, Agrate Brianza, ITALY; T. Graf and M.S. Brandt, Walter Schottky Institut, München, GERMANY.

Electrically active defects at the interface between silicon and SiO_2 or high-k oxides, considerably affect the properties of MOS-based microelectronic devices. Among the experimental methods for defect detection and investigation Electron Paramagnetic Resonance (EPR) is one of the most sensitive and powerful ones. However, because of the low density of interface defects, there is a need for a more sensitive EPR technique to characterize a single interface. Enhanced sensitivity can be achieved measuring changes of a spin dependent physical property such as photoconductivity under magnetic resonance conditions. Paramagnetic defects at the interface between (100)Si and Al_2O_3 grown with atomic layer chemical vapour deposition or via sputtering have been investigated by electrically detected magnetic resonance (EDMR). In all the investigated samples the P_{b0} and P_{b1} paramagnetic centers appear as the prominent defects. A significant contribution of the isotropic signal of the silicon dangling bonds is observed. Signal intensities and line-widths observed at different interfaces will be presented and discussed.

11:30 AM N1.7
THERMAL TRANSFORMATION OF ZrO_2, HfO_2, AND Al_2O_3, BINARY OXIDE FILMS. Deborah Neumayer and Eduard Cartier, IBM Watson Research Center, Yorktown Heights, NY.

The thermal stability, and microstructure of zirconium aluminum oxide (ZAO) and hafnium aluminum oxide (HAO) mixed oxides were evaluated. The films were prepared by chemical solution deposition (CSD) using a solution prepared from zirconium, or hafnium butoxyethoxide, and aluminum butoxyethoxide dissolved in butoxyethanol. The films were spun onto SiO_xN_y coated Si wafers and furnace annealed at temperatures from 500-1200°C in oxygen for 30 minutes. The microstructure and electrical properties of ZAO and HAO films were examined as a function of Zr/Al and Hf/Al ratio and annealing temperature. Crystallization/ phase separation of ZrO_2 and HfO_2 in ZAO and HAO films was observed to be concentration and annealing temperature dependent. At low (<25%) ZrO_2 or HfO_2 concentrations at anneal temperatures less than 900°C, an amorphous γ-alumina like material was observed in the ZAO and HAO films. Phase partitioning of the ZAO and HAO films was observed at higher ZrO_2 or HfO_2 concentrations and at higher anneal temperatures. Addition of Al_2O_3 to ZrO_2 or HfO_2 was found to increase the crystallization temperature of tetraganol ZrO_2, enable the formation of the tetragonal HfO_2 phase and increase the annealing temperature at which transformation of the tetragonal to monoclinic phase of ZrO_2 or HfO_2 is observed. Transformation from the tetragonal to the monoclinic phase was observed to occur more readily at lower temperatures in HAO films than ZAO films. Evidence of enhanced oxygen conduction at elevated temperatures was observed for 90% Hf 10% Al mixed oxide films.

11:45 AM N1.8
SCREENING THE HIGH-K LAYER QUALITY BY MEANS OF OPEN CIRCUIT POTENTIAL ANALYSIS AND WET CHEMICAL ETCHING. Martine Claes, Thomas Witters, Genevieve Loriaux, Stefan De Gendt and Marc Heyns, IMEC, Heverlee, BELGIUM.

For sub-100 nm CMOS technologies, SiO_2 will need to be replaced by deposited high-k dielectric stacks. Because the electrical properties of high permittivity gate dielectric layers depend much on their chemical composition, crystallinity and high-k film/Si interface quality, a thorough physical characterization of these layers and/of the interlayer is necessary. Open Circuit Potential (OCP) analysis already has proven its capabilities for in-situ characterization of wet silicon surface cleaning/etching processes and SiO_2 oxide growth kinetics [1-2]. In this paper, the technique is evaluated as a fast-screening method to investigate the quality of high-k dielectric layers. OCP monitors their etch behavior qualitatively with etch time. The applicability is illustrated by demonstrating differences in etch behavior as function of surface pretreatment, high-k deposition process and temperature as well as post deposition anneals. The use of additional techniques, e.g. X-ray Photoelectron Spectroscopy (XPS), aid in understanding etch kinetics and/or morphology of the deposited high-k stacks. It is seen that the high-k layer quality is dependent on the surface pretreatment applied prior to high-k deposition. SiO_x interfaces are preferred. Though, depositing HfO_2 on SiO_X interfaces sometimes result in interface reactivity with formation of silicates. Furthermore, increased temperature high-k deposition and post deposition annealing (PDA) lead to high-k layer densification (i.e. better layer quality); both observations will be demonstrated from OCP measurements. Additionally, OCP can also be used as a first indication of defective high-k layer and allow evaluation of qualitative improvement by various post deposition treatments. [1] H.F. Okorn-Schmidt et al., Proc. ALTECH 95, B.O. Kolbesen, C. Claeys and P. Stallhofer (Edt), Electrochem. Soc., Proc. vol 95-30 (1995) 316-327. [2] H.F. Okorn-Schmidt et al., Solid State Phenomena Vols. 76-77 (2001) 161-164.

SESSION N2: HIGH-k CHARACTERIZATION - II AND ATOMIC LASER DEPOSITION - I

Chairs: Stefan De Gendt and Mark Gardner
Monday Afternoon, December 2, 2002
Room 202 (Hynes)

1:30 PM *N2.1
Si-COMPATIBLE ALTERNATIVE GATE DIELECTRICS WITH HIGH-k AND HIGH-OPTICAL BANDGAP. D.G. Schlom, J.H. Haeni, J. Lettieri, L.F. Edge, and V. Vaithyanathan, Pennsylvania State University, Department of Materials Science and Engineering, University Park, PA; Y. Yang and S. Stemmer, Materials Department, UCSB, Santa Barbara, CA; H. Li, Y. Wei, and K. Eisenbeiser, Physical Science Research Laboratory, Motorola Labs, Tempe, AZ; S.-G. Lim and T.N. Jackson, Pennsylvania State University, Department of Electrical Engineering, University Park, PA; J.L. Freeouf, Oregon Graduate Institute, ECE Department, Portland, OR; G. Lucovsky, Department of Physics, North Carolina State University, Raleigh, NC; R. Uecker and P. Reiche, Institute of Crystal Growth, Berlin, GERMANY.

This talk will give an overview of our work to identify a viable gate dielectric alternative with higher dielectric constant (K) than SiO2 for silicon MOSFETs. As a first step in the identification of such an alternative gate dielectric, we used tabulated thermodynamic data to comprehensively assess the thermodynamic stability of binary oxides and nitrides in contact with silicon at temperatures from 300 to 1600 K. We then extended this thermodynamic approach to multicomponent oxides comprised of candidate binary oxides. Unfortunately, limited experimental data for the K and bandgap of many of these compounds exist, making selection of the most suitable candidate for thin film growth impossible. Using the floating zone and Czochralski crystal growth methods we have grown single crystals of many of these compounds and measured their K and optical bandgaps. The result is 13 silicon-compatible gate dielectric materials with $K > 20$, of which at least six have an optical bandgap > 5 eV. Even though the identified materials are likely stable in direct contact with silicon, a significant challenge is to actually deposit these materials on silicon. A common problem during such deposition is that excess oxidant present during deposition oxidizes the silicon forming unwanted SiO2 at the interface. We have investigated the kinetics of oxidation of many of the constituents of the silicon-compatible alternative gate dielectrics that we have identified in an effort to identify deposition conditions in which the desired material can be deposited in a fully-oxidized state while avoiding the oxidation of the underlying silicon. A promising growth regime is a low temperature / excess oxidant regime. In this regime the oxidation of silicon by the oxidant is limited by kinetics. However, kinetic barriers to the oxidation of the constituents of the silicon-compatible alternative gate dielectrics that we have identified can also occur, as we have shown through in situ oxidation studies of various constituent elements. Silicon-compatibility, high K, and high optical bandgap are just three of the many requirements that a successful alternative gate dielectric for use in silicon MOSFETs must possess. Other factors including low Dit, low permeability to oxygen, low leakage, favorable band alignment with silicon, the capability for being integrated into a complementary metal-oxide-silicon (CMOS) process, reliability, etc., must also be considered. The candidate materials identified form a starting point for these additional considerations.

2:00 PM *N2.2
PHYSICAL CHARACTERISATION OF HIGH-K GATE STACKS.
W. Vandervorst, H. Bender, T. Conard, O. Richard, C. Zhao, B. Brijs, M. Caymax, S. De Gendt, Imec, BELGIUM; V. Cosnier, J. Chen, J. Kluth, E. Cartier, M. Green, International Sematech c/o IMEC.

When considering the formation of gate stacks with sub?nm EOT satisfying the leakage requirements as well, it becomes very rapidly clear that a judicious choice of the high k material (k>15) and a very tight control of the interfacial thickness is required suggesting that the for 0.5 nm EOT the ideal stack would be close to interfacial oxide free. Formation of these layers is pursued with various deposition techniques ALCVD, MOCVD. In particular ALCVD was promoted as a very attractive method in view of its saturating surface reactions and surface conformality. However this picture of ALD-growth is

highly idealized and in reality (in particular on HF-etched surfaces) serious limitations arise preventing the formation of a fully closed film for the thickness range required for EOT=1-0.5 nm. On the other hand the chemical reactivity of the MOCVD growth seems enhance the interfacial oxyde formation. Studies on the growth behavior of ALD-films have been based on large suite of techniques (LEIS, XPS, RBS, XRF, TOFSIMS, FT-IR). In particular TOFSIMS has proven to be extremely efficient to probe the morphology of the thin films and to test the closure of the film (or the presence of holes). In addition to forming a fully closed film, it is essential that the interfacial layer is controlled (minimized) as good as possible. The presence of an interfacial (SiOx) layer depends on several factors, e.g. the silicon surface preparation prior to the high?k deposition, the high?k deposition process and the post?deposition air exposure or thermal anneal. Understanding the mechanism of formation and the control of the interfacial oxide are therefore key-issues for the successful implementation of high?k dielectrics in future devices. Finally a crucial point is the investigation of films with respect to composition, crystallization behavior, stability upon anneal and poly-deposition as these are all aspects which will influence the final applicability of the high k stacks. Again extensive physical characterization has provided detailed insight ion phase separation, crystallization and thermal stability of the various high k materials.

2:30 PM N2.3
EFFECT OF Al-CONTENT AND POST DEPOSITION ANNEALING ON THE ELECTRICAL PROPERTIES OF ULTRA-THIN $HfAl_xO_y$ LAYERS DEPOSITED BY ATOMIC LAYER DEPOSITION. R.J. Carter, M. Caymax, A. Delabie, C. Zhao, S. DeGendt, M. Heyns, IMEC vzw, Leuven, BELGIUM; W. Tsai, E. Young, International Sematech, Austin, TX; J.W. Maes, ASM International, Bilthoven, NETHERLANDS.

The aggressive scaling of MOS devices is quickly reaching the fundamental limits of SiO_2 as the gate insulator. The replacement of SiO_2 with a high dielectric constant (high-k) material allows for an increase in the physical thickness of the gate insulator, while maintaining a low equivalent oxide thickness (EOT) and low direct tunneling current. The first use of high-k materials will likely be for low power applications with the first target EOT being 1.5 nm with a poly-Si gate electrode. Atomic layer deposition (ALD) is a well-controlled surface saturating process using gas-solid interactions to deposit thin films. The flexibility of ALD to deposit mixed oxides provides options to fabricate scalable Poly-Si/high-k gate stacks. In this paper we investigate the effect of Al-content and post deposition annealing on the properties of $HfAl_xO_y$ layers in terms of the dielectric constant, the oxide fixed charge and the scalability of the gate stack. It is observed that the benefit of using a Hf-aluminate is compromised if the film has an Al-content greater than 60-wt%. This is observed in terms of a dielectric constant close to that of pure Al_2O_3 ($\sim$9) and a large amount of negative fixed charge in the film ($\sim 10^{12}$ cm^{-2}). Post deposition annealing (PDA) proves important to reduce oxide fixed charge. Using oxygen post deposition anneals we have been able to reduce flatband voltage shifts as well as CV hysteresis. In terms of scaling, the benefit of using a high-k material is compromised if a SiO_2 layer is also present in the gate stack. Therefore, it is necessary to perform an O_2 PDA at moderate temperatures or in low O_2 partial pressures in order to control the thickness of the interfacial oxide layer so that EOT's below 1.5 nm can be achieved.

2:45 PM N2.4
ATOMIC-SCALE MECHANISMS OF ULTRA-THIN DIELECTRIC GROWTH. Martin Frank, Agere Systems, Murray Hill, NJ, and Rutgers Univ, Piscataway, NJ; Yves J. Chabal, Glen D. Wilk, Agere Systems, Murray Hill, NJ.

Continued gate dielectric scaling requires an ever higher degree of control over the deposition process of alternative dielectric materials. Atomic layer deposition (ALD) is ideally suited to meet this challenge: It is based on self-saturating surface reactions of precursor molecules, and thus intrinsically enables monolayer-by-monolayer growth of a wide range of materials. In an attempt to obtain sharp Si/dielectric interfaces, growth of novel gate oxides has been performed directly on H-terminated Si surfaces. However, incomplete coverage of the surface and formation of interfacial SiO_2 have been observed. An understanding of the underlying reaction mechanisms may help find processing conditions which lead to improved films. We have therefore performed a model in-situ infrared absorption study of Al_2O_3 growth on both HF-etched and oxidized Si using sequential trimethylaluminum (TMA, $Al(CH_3)_3$) and water exposures at 300°C. We have thus observed all relevant surface species after each processing step: CH_3, OH, Si-H, and oxides. We find that H-terminated Si(100) and Si(111) surfaces are neither oxidized nor hydroxylated by water at 300°C, in contrast to what has frequently been postulated. Instead, extended TMA exposure leads to the formation of both $Si\text{-}Al(CH_3)_x$ and $Si\text{-}(CH_3)_x$, with varying kinetics and morphology dependence. Once Al is chemisorbed, water exposure induces three reactions with different kinetics: replacement of Al-bonded CH_3 by OH; transfer of CH_3 from Al to Si; and the catalytic oxidation of Si. Si-C bonds remain unaffected by water, and may therefore be responsible for C contamination. During subsequent TMA-water cycles, more interfacial SiO_2 forms, while Al_2O_3 grows according to the well-known self-terminated mechanism. On all substrates, our Al_2O_3 films are equivalent to what is deposited in commercial ALD reactors. The understanding of the initial growth of Al_2O_3 makes it possible to suggest methods to achieve sharper Si/dielectric interfaces.

3:30 PM N2.5
MATERIALS AND ELECTRICAL PROPERTIES OF ZrO_2, HfO_2 AND NANO-LAMINATE GATE DIELECTRICS GROWN BY ALD. Hyoungsub Kim, Paul C. McIntyre, Stanford Univ, Dept of Materials Science & Engineering, Stanford, CA; Krishna Saraswat, Stanford Univ, Dept of Electrical Engineering, Stanford, CA.

Metal oxide-based high-k dielectric materials, including ZrO_2 and HfO_2, offer the opportunity to continue dimensional scaling of MOSFET devices, while retaining sufficient physical thickness of the dielectric to avoid direct tunneling conduction across the gate stack. Although there are many possible deposition techniques for high-k dielectrics, ALD (Atomic Layer Deposition) is very promising because extremely precise thickness control and near-perfect conformality can be achieved owing to its surface adsorption-controlled deposition mechanism. In this experiment, we used a cold wall ALD system with $ZrCl_4/H_2O$ and $HfCl_4/H_2O$ precursors for individual and nano-laminate processes. The deposition was carried out at 250 - 300°C on a thermally-grown thin SiO_2 underlayer. The C-V and I-V characteristics were evaluated using Pt gate capacitors fabricated through a shadow mask process, and film microstructures were investigated HR-TEM imaging and electron diffraction. In this presentation, we will compare the electrical and microstructural properties of ALD-grown ZrO_2 and HfO_2 as a function of deposited thickness and substrate temperature. In addition, data on the isothermal crystallization kinetics of ALD HfO_2 and the effects of crystallization on the conduction mechanism and dielectric properties will be discussed. Electrical data and microstructural results obtained from ZrO_2/HfO_2 nano-laminate structures having different layer sequences will also be presented.

3:45 PM N2.6
A MATHEMATICAL DESCRIPTION OF ATOMIC LAYER DEPOSITION (ALD), AND ITS APPLICATION TO THE NUCLEATION AND GROWTH OF HfO_2 GATE DIELECTRIC LAYERS. M.A. Alam, M.L. Green and M.-Y. Ho, Agere Systems, Murray Hill, NJ; W. Vandervorst, B. Brijs and T. Conard, IMEC, Leuven, Belgium; P.I. Räisänen, ASM America Inc., Phoenix, AZ.

Deposition of high-k gate dielectric layers such as HfO_2 is critical to the continued scaling of CMOS devices. Atomic layer deposition (ALD) is a leading candidate for the deposition of such films. We have developed a body of nucleation and growth data for HfO_2 that reproducibly exhibits either linear or linear-exponential kinetics, depending upon the surface treatment of the Si substrate onto which the film is deposited. Specifically, depending upon the Si-OH (silanol) content of the surface, one can observe linear growth (high OH content), or linear-exponential growth (low OH content). We have been able to describe the ALD process with a phenomenological mathematical model, and fit the data with a high degree of confidence. Our model assumes that either Si-OH or Hf-OH groups are the nuclei for ALD growth. The model is based on classical chemical kinetic theory, from which two differential equations arise. One describes the deposition rate of HfO_2, and the other describes the creation of new Si-OH sites as the film grows. The rate constant that describes linear HfO_2 growth is reasonably consistent with a steric hindrance model that limits the growth rate to 1/7 of a monolayer per cycle. The rate constant describing the creation of new Si-OH sites is related to the area of the substrate not covered by HfO_2, and thus can be related to TOFSIMS measurements that describe the relative degree of two (planar) or three (island) dimensional growth. Linear growth kinetics gives rise to the most planar films.

4:00 PM N2.7
ELECTRICAL CHARACTERISTICS OF Ir/ATOMIC LAYER DEPOSITED ZrO_2/Si FIELD EFFECT TRANSISTORS. Hyun Sang Sim, Sun Il Shim, Yong Tae Kim, Semiconductor Materials Laboratory, Korea Institute of Science and Technology, Seoul, KOREA; Jae-Hyoung Koo, Hyeongtag Jeon, Division of Materials Science and Engineering, Hanyang Univ, Seoul, KOREA; Chang Woo Lee, Department of Nano Electronic Physics, Kookmin Univ, Seoul, KOREA; Taeck-Hong Lee, Department of Chemical Engineering, Hoseo Univ, Chunan, KOREA.

MISFETs were fabricated with Iridium gate electrode and high-k

ZrO_2 gate dielectric. The ZrO_2 was prepared by the atomic layer chemical vapor deposition (ALCVD) process using terakis(dietylamio)zirconium source (TDEAZ) and O_2 at 250 °C, and annealed at 800 °C for 10 sec in N_2 ambient by RTA method. Electrical performance of fabricated MISFET shows that the equivalent oxide thickness (EOT) is 1.39 nm and the gate leakage current is 2.7×10^{-9} A/cm^2 at 0.6 Voltage. The steady-state high-low frequency C-V measurement indicates that interface trap density is about 2.0×10^{12} cm^2/eV. The effective mobility of MISFET is about 226 cm^2/V-s at V_{GS} =1.5 Voltage. We have also studied mean time failure mechanism and effects of charge injection on the interface with bias stress.

4:15 PM N2.8
ATOMIC LAYER DEPOSITION OF HIGH-k GATE DIELECTRICS USING METAL ORGANIC PRECURSOR AND CYCLIC PLASMA EXPOSURE. Kazuhiko Endo and Toru Tatsumi, NEC Corporation, Silicon Systems Research Laboratories, Kanagawa, JAPAN.

We have developed a new ALD method for HfO_2 and Hf silicates ($HfSi_XO_Y$) by using MO precursor and cyclic plasma exposure. The MO precursor was tetratertiarybutoxyhafnium Hf(t-OC_4H_9) $_4$. Because MO precursors have much C content and are sensitive to H_2O, we used oxygen plasma instead of using H_2O to suppress C incorporation and background reaction during ALD of HfO_2. To deposit $HfSi_XO_Y$ on the other hand, we focused on a spontaneous formation of interfacial silicate during sputter-deposition of HfO_2 and used cyclic MO and Ar plasma exposure to mimic mixing of Hf into SiO_2 followed by the oxygen plasma exposure. The plasmas were generated by an ECR source and were exposed to the sample alternately with MO precursor. Si wafers with 1 nm SiO_2 were used as substrates. By a cyclic exposure of MO and oxygen plasma, we successfully achieved an ALD of HfO_2. Gains of the thickness per 1 cycle was 0.05 nm and was consistent with previously reported value. The carbon content in the films was suppressed due to reactive oxygen plasma exposure. The leakage current was around two orders lower than that of H_2O oxidized film and was 10^{-5} A/cm^2 with an equivalent oxide thickness of 2.0 nm. By a cyclic exposure of MO and Ar plasma on the othe hand, $HfSi_XO_Y$ was successfully deposited. The concentration of Hf was increased as cycle number progressed and the thickness of $HfSi_XO_Y$ remained constant. We found that silicate layer has an in-depth profile of Hf atoms and Hf-rich layer was sandwiched with Si-rich top and bottom layers. We think that this gradual Hf composition is promising because interfacial properties of SiO_2 are preserved and combined with high-k Hf silicate. The leakage current of the film was 10^{-2} A/cm^2 with an equivalent oxide thickness of 1.2 nm.

4:30 PM N2.9
Al_2O_3/Si_3N_4 STACKED INSULATOR FOR ADVANCED MOS DEVICES. Yoshihisa Fujisaki, Kunie Iseki, and Hiroshi Ishiwara, Tokyo Institute of Technology, Frontier Collaborative Research Center, Yokohama, JAPAN.

High-k materials now under development face serious problems in controlling the interface between films and Si substrates. The major issue related the interface is how to suppress the emergence of SiO_2 throughout the device fabrication process. We have developed hydrogen-free and damage-free Si_3N_4 made by direct nitridation of silicon substrates using atomic nitrogen radicals[1]. Since this Si_3N_4 (radical-Si_3N_4) is highly resistive against the oxidation ambience, it can be used as a buffer layer to control the interface of Si and high-k oxide materials. We demonstrated the potential of the radical-Si_3N_4 with the Al_2O_3/radical-Si_3N_4 stack. Atomic layer deposition (ALD) technique was employed to deposit Al_2O_3 thin films using $Al(CH_3)_3$ and H_2O precursors. The physical thickness of the Al_2O_3 and Si_3N_4 films were 1 ∼ 2nm and 1nm, respectively. After depositing Al_2O_3 films, we performed the post oxidation at 950°C for 5min in 10%-O_2/90%-N_2 ambience to eliminate defects both in the film and at the interface. Due to the XPS analysis and TEM observations, the interface between radical-Si_3N_4 and Si is not oxidized even after the post oxidation process at temperatures higher than 950°C. The interface state density was found to be kept less than 10^{11} $cm^{-2}eV^{-1}$. It was also found that the flat band shift is negligible. The permittivity estimated from the thicker Al_2O_3 films is 9.7, which is as good as the reported value for bulk Al_2O_3. The current density less than 10^{-4} A/cm^2 is realized under the 1V bias application using films with the capacitance density of $35 fF/\mu m^2$. These excellent properties were derived from the high endurance of radical-Si_3N_4 against the oxidation treatment. Therefore, radical-Si_3N_4 can be used as a buffer layer for other high-k materials to control the interface. [1] Y. Fujisaki and H. Ishiwara, Jpn. J. Appl. Phys. 39, L1075 (2000).

4:45 PM N2.10
SUPPRESSION OF FIXED CHARGES AND BORON PENETRATION IN Al_2O_3 BY PLASMA NITRIDATION. K. Manabe[a], K. Endo[a], S. Kamiyama[a], T. Iwamoto[a], T. Ogura[a], M.-Y. Ho[b], P. Raisanen[c], G.D. Wilk[d], M.L. Green[d], and T. Tatsumi[a]; [a]NEC Corporation, Silicon Systems Research Laboratories, Kanagawa, JAPAN; [b]National University of Singapore, Crescent, SINGAPORE; [c]ASM America, AZ; [d]Agere Systems, NJ.

Al_2O_3 is considered one of the most promising candidates for high-k gate dielectrics. However, negative fixed charges and boron penetration in Al_2O_3 are serious problems in CMOS applications. It is reported that incorporating nitrogen into Al_2O_3 is effective for overcoming these problems [1, 2]. But reactive sputtering leads to too much nitrogen incorporation [1], which is suspected to increase the leakage current. Therefore, in this work, we demonstrate precise control of nitrogen content through use of plasma nitridation. We have found that a small amount of nitrogen incorporation can suppress fixed charges and boron penetration without increasing EOT and leakage current. Al_2O_3 (2-3 nm) films were deposited on pre-oxided Si wafers by atomic layer-CVD (ALCVD). Plasma nitridation of Al_2O_3/SiO_2/Si-substrates was carried out by using an ECR plasma source under various conditions (substrate temperature: 300-700°C, nitrogen pressure: 0.3-0.9 Pa). We found that a small amount of nitrogen incorporation (7.4%) can suppress negative fixed charges in Al_2O_3 (ΔV_{FB} = 0 V) without increasing EOT and leakage current. Our XPS analysis also showed that nitrogen was not incorporated into the Si substrate but only within the Al_2O_3 film. In addition, boron penetration and thermal stability against dopant activation annealing at 1000°C were investigated for B-doped poly-Si/AlON/SiO_2/Si-capacitors. The results showed that boron penetration can be suppressed, despite a low nitrogen content of 3.4%. TEM observation revealed that the amorphous structure of AlON remained after the high temperature annealing. These results indicate that plasma nitridation is a promising method for improving the electrical properties of Al_2O_3 gate dielectric. [1] L. Manchanda et al., Extended Abstracts of International Workshop on Gate Insulator, p. 56 (2001). [2] H.-J. Cho et al., Extended Abstracts of Int. Conf. SSDM, p. 504 (2001).

SESSION N3: GATE METAL MATERIALS AND INTEGRATION

Chair: Richard Carter
Tuesday Morning, December 3, 2002
Room 202 (Hynes)

8:30 AM *N3.1
METAL ALLOYS FOR GATE ELECTRODE APPLICATIONS. Veena Misra, North Carolina State University, Department of Electrical and Computer Engineering, Raleigh, NC.

Metal gate electrodes will be required to eliminate gate depletion problems associated with conventional polysilicon gates. For bulk CMOS devices, metals must have work functions that are near the conduction and valence band edges of Silicon. On the other hand, for non-bulk CMOS devices, the work function requirements are predicted to be ∼ 0.3 eV above and below the mid-gap level. It is difficult and costly to develop and sustain multiple gate electrode processes for different technologies. If a metal gate technology system work function tuning capability then it would be ideal for all devices on the ITRS roadmap Recently, binary metal alloys have been investigated and were found to have good work function tuning properties and good thermal stability up to 1000°C. This work will focus on the selection process of metal alloys based on the desired work function range, existence of wide range of stable phases and thermal stability. Both the material and electrical properties of metal alloys such as Ru-Ta, Ru-Hf and Ru-Y for gate electrode applications will be discussed. Work function dependence on alloy content will also be presented. The thermal stability will be evaluated in terms of the equivalent oxide thickness and flat band voltage change upon high temperature annealing. The impact of multiple phases on the electrical properties will also be discussed. Finally, schemes to simplify the metal gate integration will also be presented.

9:00 AM N3.2
MEASURING THE WORK FUNCTIONS OF VARIOUS PVD TANTALUM NITRIDE FILMS WITH A NOVEL SCHOTTKY DIODE CV TECHNIQUE FOR METAL GATE CMOS APPLICATIONS. James Pan, Christy Woo, Jinsong Yin, Ercan Adem, Paul Besser, Ming-Ren Lin, Advanced Micro Devices, Sunnyvale, CA.

The metal gate process becomes a promising candidate for sub-65nm CMOS, due to the elimination of polysilicon depletion effects, and the possibility of adjusting the CMOS threshold voltage without more threshold implants. Our goal is to process TaN films with tunable work functions, in order to meet the demand of sub-65nm metal gate CMOS. PVD TaN films are deposited with various processing conditions. Auger analysis shows that by changing the nitrogen flow rate and the plasma power, the nitrogen content in the TaN films can

be adjusted. In order to accurately determine the work function of these TaN materials, we have developed a Schottky Diode CV technique (or Metal-Silicon CV, or MS-CV). This approach not only improves the accuracy of the metal work function measurement, compared with the traditional MOS-CV technique (which is affected by the thickness and quality of the oxide), but also simplifies the fabrication. With the MS-CVs, we have successfully measured the work functions of Ni and Co and compared the data with published references. The work function of PVD TaN actually decreases with higher nitrogen content, according to the Auger data and the MS-CV measurement, ranging from 3.42 4.20 Volts. The MS-CV technique is shown to be independent to the size of the capacitors, and is little affected by the measurement frequency. By changing the frequency from 100KHz to 1MHz, the error in the work function is less than 50mV.

9:15 AM N3.3
CHARACTERIZATION OF RUTHENIUM AND RUTHENIUM OXIDE THIN FILMS DEPOSITED BY CHEMICAL VAPOR DEPOSITION FOR CMOS GATE ELECTRODE APPLICATIONS.
Filippos Papadatos, University at Albany Institute for Materials, School of Nanoscience and Nanoengineering, Albany, NY; Spyridon Skordas, University at Albany Institute for Materials, School of Nanoscience and Nanoengineering, Albany, NY; Steven Consiglio, University at Albany Institute for Materials, School of Nanoscience and Nanoengineering, Albany, NY; Eric Eisenbraun, University at Albany Institute for Materials, School of Nanoscience and Nanoengineering, Albany, NY; Alain E. Kaloyeros, University at Albany Institute for Materials, School of Nanoscience and Nanoengineering, Albany, NY.

In this work, a metal-organic precursor was used to deposit ruthenium (Ru) and ruthenium oxide (RuO_2) films on SiO_2 substrates using hot wall metal organic chemical vapor deposition (MOCVD) in a 200 mm wafer deposition cluster tool. Oxygen and hydrogen were employed as reactant gases for the depositions. The process temperature ranged from 360°C to 480°C and a broad range of processing parameters were investigated with respect to their effects on subsequent film properties. Key material properties of the films were characterized, including purity, stoichiometry, resistivity, thermal and chemical stability, nanostructure, and electrical properties. The techniques used throughout this study were cross-sectional scanning electron microscopy (CS-SEM), four-point resistance probe, x-ray photoelectron spectroscopy (XPS), Rutherford backscattering spectrometry (RBS), x-ray diffraction (XRD), transmission electron microscopy (TEM), and energy dispersive x-ray spectrometer (EDS). Capacitance and voltage measurements (CV) were also carried out. The produced films exhibited columnar structure (hexagonal for the ruthenium films and tetragonal for the oxide films) and low resistivity for both the metal and the oxide phase ($<80\ \mu\Omega\cdot$cm). In order to assess thermal stability, the films were subsequently annealed in forming gas and oxygen ambients for 60 min at 650°C. Results of PMOS gate electrode performance testing of CVD RuO_2 films will also be discussed.

9:30 AM N3.4
IRIDIUM AND IRIDIUM OXIDE FILMS FOR DUAL METAL GATE CMOS.
Dwi Wicaksana, Chris R. Hoffman, Jon-Paul Maria and Angus I. Kingon, North Carolina State Univ, Dept of Materials Science and Engineering, Raleigh, NC.

Iridium and iridium oxide were investigated for CMOS metal gate application. Both films were prepared on thermal oxide of various thicknesses; Ir films by dc magnetron sputtering and IrO_2 films by reactive magnetron sputtering and oxidation of Ir films. The films were annealed in both oxidizing and reducing atmosphere up to 1000 °C. From x-ray diffraction study, the oxidation of Ir showed a transition to IrO_2 at 800 °C. The diffraction peaks became weaker and disappeared after annealing at higher temperatures, indicating the loss of iridium from the substrate due to sublimation of the metal in the form of IrO_x. The work functions were derived from capacitance-voltage characteristics of the MOS capacitors. The work functions were 5.24 eV for Ir and 4.25 eV for IrO_2, showing these materials are appropriate for PMOS and NMOS application, respectively. IrO_2 can also be formed by annealing of Ir, but it needs a long-time high-temperature oxidation that may degrade the dielectric. A short-time oxidation is not enough to form IrO_2 with the right work function for NMOS.

10:15 AM *N3.5
SELECTION OF CMOS GATE METAL MATERIALS USING SYNCHROTRON RADIATION PHYSICAL CHARACTERIZATION TECHNIQUES.
C. Cabral Jr., C. Lavoie, J. Jordan-Sweet, J.M.E. Harper, and A.S. Ozcan†; IBM T.J. Watson Research Center, Yorktown Heights, NY; †Boston University, Department of Physics, Boston, MA.

We present an evaluation of the thermal stability for various elemental metals and binary/ternary conducting compounds on gate dielectrics using synchrotron x-ray diffraction techniques. Twenty different metallic materials with work functions ranging from 3.9 to 5.7 eV covering nFET, mid gap and pFET contacts were studied. The films were characterized during rapid thermal annealing in a forming gas ambient at a temperature ramp rate of 3°C/s up to 1000°C. Three techniques, in situ x-ray diffraction, resistance and optical scattering analysis were used simultaneously as well as ex situ x-ray reflectivity analysis. It was found that many of the materials, especially those with nFET work functions found in columns 4 and 5 of the periodic table, undergo reactions with the SiO_2 and Al_2O_3 gate dielectrics while others were unstable because of melting (Al) or agglomeration (Co, Ni and Pd). Two binary compounds, W_2N and RuO_2, underwent dissociation in the hydrogen containing forming gas annealing ambient. Materials stable up to 1000°C include W, Re, Rh, Ir, Pt, TaN and TaSiN making them possible gate metal choices for complementary metal oxide semiconductor integration involving high temperature processing.

10:45 AM N3.6
HIGHLY CONFORMAL THIN FILMS OF TUNGSTEN NITRIDE PREPARED BY ALD FROM A NOVEL PRECURSOR.
Jill Becker, Seigi Suh, Roy G. Gordon, Harvard University, Department of Chemistry and Chemical Biology, Cambridge, MA.

Highly uniform, smooth and conformal coatings of tungsten nitride were synthesized by atomic layer deposition (ALD) from vapors of a novel precursor, bis(*tert*-butylimido)bis(dimethylamido)tungsten, $(t\text{-BuN})_2(Me_2N)_2W$, and ammonia at low substrate temperatures (250-350 °C). This tungsten precursor is a low-viscosity, non-corrosive liquid with sufficient volatility at room temperature to be a vapor source for ALD. These vapors were alternately pulsed into a heated reactor, yielding up to 0.1 nm of tungsten nitride film for every cycle, with no initial delay or induction period. The films were uniform in thickness along the 20 cm length of the deposition zone, as determined by scanning electron microscopy. Successful depositions were carried out on all substrates tested, including silicon, glass, quartz, glassy carbon, stainless steel, aluminum, gold and copper. The films are shiny, silver colored and electrically conducting. All of the films showed good adhesion to the substrates, were acid resistant and did not oxidize over time. The stoichiometry of the WN films was determined to be 1:1 by Rutherford back-scattering spectrometry and X-ray diffraction. The films were mainly amorphous as deposited, with some nano-crystallites (< 3 nm in size) embedded in the film as shown by X-ray diffraction and high-resolution transmission electron microscopy. 100% step coverage was obtained inside holes with aspect ratios greater than 40:1. Annealing for 30 minutes at temperatures above 725°C converted the WN to pure, polycrystalline tungsten metal. WN films as thin as 5 nm proved to be good barriers to diffusion of copper for temperatures up to 600°C. ALD of copper onto the surface of the WN produced strongly adherent copper films that could be used as "seed" layers for CVD or electro-deposition of thicker copper coatings.

11:00 AM N3.7
X-RAY ABSORPTION STUDIES OF HIGH-PERFORMANCE LOW-K DIELECTRIC MATERIALS.
Takashi Yoda, Hideshi Miyajima, Keiji Fujita, Miyoko Shimada, Renpei Nakata, Toshiba Corporation, Tokyo, JAPAN; Hideki Hashimoto, Toray Research Center Inc., Shiga, JAPAN.

The integration of the multilevel interconnection by damascene Cu with low-k dielectrics is the key technology for SOC (System On Chip) devices. Cu with low-k dielectrics process is widely used for 0.13um and beyond devices. Requirements include high mechanical strength of low-k material to avoid the crack of the film by Cu CMP processes and packaging processes. The EB (Electron Beam) cured process is the most promising candidate to improve the mechanical strength of the MSQ (Methylsilsesquioxane) type low-k dielectrics (LKD film; JSR Corporation) without increasing the k value. The structural study of the films is necessary to understand the root cause of the strength change of the EB cured low-k film. XAFS (X-ray Absorption Fine Structure) is a nondestructive characterization technique, consisting of XANES (X-ray Absorption Near Edge Structure) spectrum and EXAFS (Extended X-ray Absorption Fine Structure) spectrum, which reveals local structure and local symmetry around the atom that absorbs x-rays and emits fluorescence. In this study, we have conducted the XAFS measurement of the MSQ type low-k dielectrics (LKD film) to clarify the structure change with and without the EB cure. Furthermore, three types of other MSQ films, the ladder structure, the random structure and the CVD film, have been investigated as references. We have determined Si-O-Si bond angle and Si-O (Si-C) bond length by fitting the Fourier transformed EXAFS spectra. The first measurements began with comparisons between the ladder structure and the random structure films. The Si K-edge XANES spectra of the ladder structure and the random

structure films exhibit quite different features. While Si-O (Si-C) bond lengths of measured samples are almost the same, the ladder structure and the random structure have Si-O-Si bond angle of 133° and 146°, respectively. The second measurements were focused on comparisons of LKD films with and without EB cure. Si-O-Si bond angle of LKD film is among that of the ladder and the random structure, and the XANES spectrum of LKD film displays two broad features, corresponding to the mixture of both structures. In contrast, Si-O-Si angles of the EB cured LKD film and the CVD film resemble each other, and the XANES features of the EB cured LKD film and the CVD film are almost identical with that of the random structure. We have confirmed that the EB cure process for LKD film makes the drastic structure change from the mixture of ladder and random structure to the random network structure. Further investigations such as theoretical calculation are in progress.

11:15 AM N3.8
ALTERNATIVE WAVELENGTH-INVARIANT RESIST COMPOSED OF BIMETALLIC LAYERS. Y. Tu, M. Karimi, N. Morawej, K.L. Kavanagh, and G.H. Chapman, Dept. of Physics and School of Engineering Science, Simon Fraser University, Burnaby, BC, CANADA.

Although organic photoresists dominate the field, it has recently been demonstrated that Bi/In bilayers can act as a sensitive wavelength invariant thermal resist for microlithography and the fabrication of direct-write photomasks. Bilayer films ranging in thickness from 20 to 200 nm, exposed to lasers of different wavelengths (CW Argon laser 514 nm and pulsed Nd:YAG laser 533 nm, 266 nm) show a change in optical transmission of approximately 4 orders of magnitude (optical density 4 to 0.3). Furnace anneals are less effective, but also result in films with a greater optical transparency. The optimal film compositions occur near the eutectic points in this system, (22 or 53 at% Bi). Experiments and optical modeling indicate that this system is wavelength invariant with similar sensitivity expected at extreme UV and X-ray wavelengths. The exposed patterns can be developed in dilute HCl-H2O2 solutions, which preferentially etches the unexposed areas (>60:1). The exposed resist is highly conductive (0.5 mOhm-cm), and stable at room temperature. In this paper, we report on an investigation of the composition, morphology, and nanostructure of the resist before and after annealing, to confirm the expected binary phase formation and to rule out oxidation. AFM and TEM investigations show that starting films, Bi/In (12 nm/12 nm) physical vapour deposited at room temperature onto Si or SiO surfaces, are polycrystalline, and continuous, but rough with a large grained, island morphology (150 nm average diameter). Furnace anneals above the eutectic temperature (150-250C, 3 hours) result in the formation of the expected tetragonal phase BiIn. The island morphology is maintained but there is evidence of melting and recrystallization. No phases attributable to oxidation were found. RBS and Auger depth profile analysis to confirm these conclusions are underway. The optical properties expected for the semi-metal BiIn will be discussed.

11:30 AM N3.9
A SELECTIVE ETCHING PROCESS FOR CHEMICALLY INERT HIGH-K METAL OXIDES. Katherine L. Saenger, Harald Okorn-Schmidt, and Christopher P. D'Emic, IBM Research, Yorktown Heights, NY.

High-k metal oxides such as HfO_2 and Al_2O_3 are being investigated as gate dielectrics for advanced CMOS devices due to the expected limitations of SiO2 at equivalent oxide thicknesses (EOT) less than 1 nm. However, integration of these metal oxide films into devices requires the existence of selective and controllable patterning processes. Conventional wet etches typically have no effect on these films, which are extremely chemically inert once they have been annealed, and reactive ion etching (RIE) processes, while effective, typically lack the required selectivity. In this paper we describe a new etch process in which exposed regions of HfO_2 films are treated to make them etchable in aqueous HF-based solutions. Etch times (as indicated by time to "dewet") were examined as a function of HfO_2 thickness, the treatment parameters, post-treatment anneals, and wet etch chemistry. Additional data provided by electrochemical open circuit potential (OCP) measurements will also be discussed.

11:45 AM N3.10
LASER-INDUCED LATERAL-EPITAXY IN FULLY DEPLETED SILICON-ON-INSULATOR JUNCTIONS. Kevin K. Dezfulian[a], J.P. Krusius[b], M.O. Thompson[c], and Somit Talwar[d]; [a]School of Applied and Engineering Physics, Cornell University, Ithaca, NY; [b]School of Electrical and Computer Engineering, Cornell University, Ithaca, NY; [c]Department of Materials Science and Engineering, Cornell University, Ithaca, NY; [d]Ultratech Stepper, San Jose, CA.

Junction formation in a fully-depleted silicon-on-insulator (FD-SOI) CMOS technology is being pursued using a locally selective laser thermal process (LTP). Such structures, designed for the 50 nm SIA technology node, involve a silicon layer only as thick as the junction depth (20–50 nm). With these dimensions, amorphization and laser melting—while selective laterally—by necessity consumes the entire film thickness, leaving no underlying crystal reference. However, under appropriate conditions, unmelted silicon beneath the MOS gate stack can serve as a template for crystallization. The LTP method offers meta-stable dopant activation, box-like dopant profiles, and negligible dopant diffusion beyond the amorphized regions. The selective melting of large-area 25–30 nm SOI films with a 35 ns 308 nm XeCl laser pulse was characterized *in situ* using transient conduction and optical reflectance techniques. These measurements identified a window of laser fluence for the selective melting of amorphous but not crystalline silicon. Subsequently, a set of samples were masked for implant amorphization with a pattern of 1 μm polysilicon-on-oxide "gate" lines spaced 1 μm apart, and annealed with a single laser pulse within the aforementioned fluence window. Cross-sectional STEM on such a sample after LTP at 300 mJ/cm^2 indicated lateral silicon epitaxy up to 150 nm beyond the channel edge. The first 30 nm of epitaxy was nearly defect free, followed by an increasing density of twins and ultimately terminating in an amorphous quench. The observed microstructure can be understood as a lateral equivalent of laser-induced amorphization of bulk Si. The observation after LTP of amorphous silicon beyond the epitaxial region indicates that complete recrystallization of the original implant-amorphized region could be accomplished using either repeated laser annealing or solid-phase diffusion.

SESSION N4: CONTACTS AND ULTRA-SHALLOW JUNCTION FORMATION
Chair: Vidya S. Kaushik
Tuesday Afternoon, December 3, 2002
Room 202 (Hynes)

1:30 PM N4.1
THE EFFECT OF SiGe BARRIERS ON THE THERMAL STABILITY OF HIGHLY B-DOPED Si SURFACE LAYERS. Phillip E. Thompson, Naval Research Laboratory, Washington, DC; Joe Bennett, International SEMATECH, Austin, TX; Robert Crosby, Mark E. Twigg, Naval Research Laboratory, Washington, DC.

Ultra-shallow junction layers in Si are required for deep submicron CMOS and quantum devices. We have investigated the use of low-temperature (320 °C) molecular-beam epitaxy (MBE) to form highly conductive, p$^+$, ultra-shallow layers in Si. In this work we have concentrated on 10 nm B-doped Si surface layers. The deposited B is fully electrically active. The junction depth, D_j, 17.5 nm, was defined by the location in the SIMS profile where the B concentration has dropped to 10^{18}/cm^3. The minimum resistivity of the doped Si layer, 2.38 x 10^{-4} ohm-cm, was attained with a B concentration of 10^{21}/cm^3. Although the as-grown B is electrically active, in a practical application the doped layers may be exposed to high temperature during post-growth device processing. The B-doped Si profiles were stable up to 700 °C for 10 min. However, after a 10 min furnace anneal at 800 °C, there was substantial redistribution of the B. To minimize the B diffusion, we investigated the use of 10 nm SiGe barrier layers. Each sample had the 10 nm B-doped Si layer on top of a 10 nm undoped SiGe barrier layer composed of either 20% Ge or 40% Ge. After the 800 °C/10 min anneal the D_j were 52.3 nm, 34.4 nm and 27.2 nm for no barrier, 20% Ge barrier, and 40% Ge barrier, respectively. Clearly there is less B redistribution with the SiGe barriers. The use of SiGe barriers may prove to be critical in the activation of B implants for the formation of ultra-shallow junctions.

1:45 PM N4.2
ENHANCED LOW TEMPERATURE B ACTIVATION IN Si VIA NON-AMORPHIZING HIGH-ENERGY ION IMPLANTATION. R. Kalyanaraman, Washington University, St. Louis, MO, Oak Ridge National Laboratory, Oak Ridge, TN and Agere Systems, Murray Hill, NJ; C.S. Rafferty, H.-J.L. Gossmann, Agere Systems, Murray Hill, NJ; V.C. Venezia, Phillips Research, Leuven, BELGIUM and Agere Systems, Murray Hill, NJ; L. Pelaz, University of Valladolid, Valladolid, SPAIN and Agere Systems, Murray Hill, NJ; T.E. Haynes, Oak Ridge National Laboratory, Oak Ridge, TN.

The ability to achieve efficient electrical activation of B in Si at low temperatures (T) has been an important goal in Si processing research. The main limitation to achieve efficient low T activation is related to the clustering phenomenon associated with B atoms, which is enhanced by the presence of interstitial atoms. The most successful approach to achieve low T activation has been via epitaxial regrowth of amorphized Si implanted with B, where B clustering is found to be reduced. However, this approach faces limitations when the amorphized Si has an interface with a non-Si region. This is a likely situation with devices fabricated on heterogeneous substrates, like Si-on-Insulator. Here, a thin active device layer of Si sits on an

insulator, like SiO_2. Consequently, epitaxial regrowth into a single crystal is not possible and hence alternate approaches must be discovered. Here, we demonstrate a new approach to achieve enhanced B activation at temperatures as low as 400°C. The approach relies on generating a large concentration of excess vacancy clusters prior to the B implant. These excess vacancies are generated by high-energy ion implantation in Si using 2-MeV Si in the dose range of $2x10^{15}$-$1x10^{16}$ atoms/cm^2. Amorphization is suppressed by holding the substrate at slightly elevated temperatures (~70°C). We show that the electrical activation of 40-keV, $2x10^{14}$ cm^{-2} B implants is enhanced by more than a factor of 2 in the temperature range from 400 to 800°C over the case without vacancies. We also discuss the vacancy concentration dependence of B-electrical activation. This approach will potentially allow low T activation of B doped Si on heterogeneous substrates.

2:00 PM N4.3
2D DOPANT PROFILING FOR ADVANCED PROCESS CONTROL. Xiang-Dong Wang, Qianghua Xie, Shifeng Lu, Motorola, DigitalDNA Laboratories, Mesa, AZ; Wei Liu, Motorola, Chandler, AZ; Linda Cross, Motorola, Austin, TX; J.J. Lee, Phil Tobin, Motorola, DigitalDNA Laboratories, Austin, TX.

Characterization of 2D dopant distribution is becoming increasingly demanding but also more difficult with the shrinking of CMOS device dimensions. Although a precisely quantitative 2D dopant profiling technique will ultimately solve all the manufacturing and development issues encountered, the advance of such a technique has not yet caught up with the pace of the progress in CMOS technologies. On the other hand, during the process development and product manufacturing, addressing 2D dopant distribution issues within limited timeframe are very critical. Here we report various characterization techniques that we used to address those issues. The main techniques we used are dopant selective etching (DSE) and scanning probe microscopy based techniques including scanning capacitance microscopy (SCM) and scanning spread resistance microscopy (SSRM). These techniques provided complimentary results and showed strengths in solving different issues. We have successfully delineated junction of CMOS devices with 0.13 um technology with source/drain extensions. Other applications, including diode leakage, well-well isolation, and buried layer delineation with the combination of these methods, will also be given. We will provide comparison of the results obtained with different techniques and discuss their advantages and disadvantages.

2:15 PM N4.4
HEAVY ARSENIC DOPING OF SILICON BY MOLECULAR BEAM EPITAXY: INCORPORATION AND TRANSPORT PROPERTIES. Xian Liu, Qiang Tang, James S. Harris, Stanford Univ, Solid State and Photonics Lab, Stanford, CA; Theodore I. Kamins, Hewlett-Packard Laboratories, Palo Alto, CA.

As MOSFETs scale to deep-submicron dimensions, there has been an increasing demand for silicon epitaxial layers with abrupt doping profiles. For nanoscale devices, arsenic is an attractive n-type dopant because of its high solubility and low diffusivity, but suffers from surface segregation during epitaxy, making high-concentration incorporation with abrupt profiles difficult. In this paper we report results of arsenic incorporation in Si molecular beam epitaxy (MBE) using a unique combination of solid (As, Si) and gas (disilane) sources to achieve these goals. Si epitaxy using disilane involves a series of surface reactions and requires substrate temperatures higher than approximately 600°C to produce a useful growth rate. At these temperatures, As segregates severely to the growing surface and terminates dangling bonds. As a result, epilayers with As concentrations in the 10^{18} cm^{-3} range suffers from significantly reduced growth rates and surface roughening, similar to those previously reported in As-doped epilayers using hydride precursors for both Si and As. Supplying Si from an elemental source, on the other hand, eliminates surface reaction steps and enables deposition at lower temperatures, where As segregation is kinetically suppressed. Under these conditions extremely high As concentrations were obtained with relatively small surface coverages. In this work, we demonstrated Si (100) epilayers with As concentrations up to 10^{21} cm^{-3} and doping transitions better than 3 and 2 nm/dec at the start and end of As-doped growth, respectively. In heavily doped as-grown epilayers, electron concentrations were found to saturate around 2 x 10^{20} cm^{-3}, with mobilities slightly lower than bulk values. Cross-section and plan-view TEM analysis did not show extended defects, such as the stacking faults, dislocation loops or precipitates often observed in heavily As-doped Si. Possible origins of this deactivation and effects of different annealing processes are discussed.

2:30 PM N4.5
MODELING THE INITIAL FAST INTERDIFFUSION REGIME IN Si/SiGe MULTILAYERS. Daniel B. Aubertine, Nevran Ozguven, Ann F. Marshall, Paul C. McIntyre, Stanford University, Dept of Materials Science and Engineering, Stanford, CA.

We present modeling results that explain the existence of an initial, fast interdiffusion regime at low Ge concentration Si/SiGe interfaces. During the early stages of annealing, Si/SiGe interfaces can exhibit more than an order of magnitude enhancement in interdiffusivity; limiting their thermal stability. We show that this enhancement can be accurately modeled by accounting for the concentration dependence of the activation enthalpy and exponential prefactor for Si/SiGe interdiffusion. We further demonstrate that by comparison, strain enhancement of Si/SiGe interdiffusion is a secondary effect. The model results are supported by direct measurements of Si/SiGe interdiffusivity and strain relaxation via synchrotron source x-ray diffraction from Si/SiGe superlattices. Both symmetric and asymmetric diffraction geometries were used to monitor strain relaxation while interdiffusion kinetics were determined from the attenuation of superlattice x-ray satellite peaks. Agreement is shown between modeling and experimental results for CVD-grown multilayers that received post deposition anneals between 795 and 895 degrees Celsius in an inert ambient.

3:15 PM N4.6
SiGe pMOSFETs FABRICATED ON LIMITED AREA SiGe VIRTUAL SUBSTRATES. A.M. Waite, U.N. Straube, N.S. Lloyd, S.G. Croucher, Y.T. Tang, B. Rong, A.G.R. Evans, University of Southampton, Dept. of Electronics and Computer Science, Southampton, UNITED KINGDOM; T.J. Grasby, T.E. Whall, E.H.C. Parker, University of Warwick, Dept. of Physics, Coventry, UNITED KINGDOM.

Silicon germanium pMOSFETs with channel lengths down to $0.4\mu m$ have been fabricated on novel limited area silicon germanium virtual substrates. The virtual substrates were grown by solid source MBE on $10\mu m$ x $10\mu m$ silicon pillars fabricated by dry etching trenches into the original silicon substrate. The pillars limit the area of the growth zone and this promotes the relaxation of the SiGe virtual substrate by allowing misfit dislocations to terminate at the edges of the growth zone. This reduces the amount of cross hatch on the surface of the wafer and increases wafer planarity. The devices were fabricated with a strained 5nm silicon germanium channel active layer with a germanium content of 70% grown on top of a relaxed SiGe virtual substrate. The substrate had a 250nm relaxed SiGe layer with a germanium content of 30% grown on top of a $1\mu m$ SiGe layer graded from 0% to 30%. A 2nm silicon cap separates the SiGe channel from the 5nm thick gate oxide. The polysilicon gate electrode was insitu doped with boron. Electrical measurements of $2\mu m$ devices show that the strained SiGe channel increases the effective low field hole mobility measured at Vdrain=-2.5V from $94.6cm^2/Vs$ to $156cm^2/Vs$ compared to conventional silicon counterparts. This is an increase of 65%. This increase in hole mobility increases the saturation drive current (Ion) measured at Vdrain=-2.5V and -2.5V gate overdrive from $199\mu A$ per micron width for $0.4\mu m$ silicon devices to $239\mu A$ per micron width for $0.4\mu m$ SiGe devices, an increase of 20%.

3:30 PM N4.7
SiGe-ON-INSULATOR (SGOI): FABRICATION OBSTACLES AND SOLUTIONS. Gianni Taraschi, Arthur J. Pitera, Lisa M. McGill, Zhiyuan Cheng, Minjoo L. Lee, Thomas A. Langdo, Eugene A. Fitzgerald, Dept of Materials Science and Engineering, Cambridge, MA.

High mobility strained Si will likely be incorporated into CMOS technology, hence it is worthwhile to seek a feasible fabrication method that combines both the benefits of strained Si and SOI. The generic substrate that can accomplish the above goal consists of high-quality, monocrystalline, relaxed SiGe-on-insulator (SGOI, and SSOI for strained Si on top of the SiGe). The most flexible approach requires the creation of wafer-scale, low defect density SGOI. To accomplish this, we have developed wafer bonding of insulating substrates to low defect density, relaxed SiGe virtual substrates, consisting of planarized, graded layers of SiGe on Si grown using UHVCVD. SiGe layer transfer onto the insulating substrate was accomplished using both grind/etch-back and Smart-cut. The most stringent requirement for SGOI substrates is uniform SiGe thickness across the entire wafer. In addition, for fully depleted MOS, the semiconductor layer on the buried oxide must also be ultra-thin ($T_{Si}+T_{SiGe}<30$nm). Because of these constraints, polishing after layer transfer is unacceptable due to non-uniform material removal across the wafer, and the lack of precise control on the final SiGe thickness. To solve these problems, we have incorporated a Si etch stop layer in the bonding structure. After layer transfer, a selective chemical etch is used to remove excess SiGe and controllably stop on the etch stop. Within the context of ultra-thin SGOI fabrication, we shall present recent improvements we have made to the etch stop, bonding process, and selective etch.

3:45 PM N4.8
Ni SILICIDE FORMATION ON POLYCRYSTALLINE SiGe AND SiGeC LAYERS. Erik Haralson, Kungl Tekniska Högskolan, Dept of

Microelectronics and Information Technology, SWEDEN; Tobias Jarmar, Uppsala University, Ångström Laboratory, SWEDEN; Johan Seger, Henry Radamson, Shi-Li Zhang, Mikael Östling, Kungl Tekniska Högskolan, Dept of Microelectronics and Information Technology, SWEDEN.

The reactions of Ni with polycrystalline $Si_{0.82}Ge_{0.18}$ and $Si_{0.816}Ge_{0.18}C_{0.004}$ films by vacuum annealing and rapid thermal processing were studied. Sheet resistance measurements and X-ray diffraction were used to determine the phase formation sequence as a function of temperature and to compare with the phase formation sequence of Ni with polycrystalline Si. The monosilicide phase is formed at higher temperatures for both the $Si_{0.82}Ge_{0.18}$ and $Si_{0.816}Ge_{0.18}C_{0.004}$ films compared to the Si reference. The agglomeration temperature of the $Si_{0.816}Ge_{0.18}C_{0.004}$ is shown to be higher compared to the $Si_{0.82}Ge_{0.18}$ sample. Finally, thin film lateral diffusion couples of Ni on polycrystalline $Si_{0.816}Ge_{0.18}C_{0.004}$ and $Si_{0.82}Ge_{0.18}$ films are studied by transmission electron microscopy (TEM) in conjuntion with energy dispersive spectrometry (EDS). The lateral growth rate as well as the phase formation sequence will be shown and compared with Ni on polycrystalline Si.

4:00 PM N4.9

FORMATION OF NICKEL MONO-GERMANOSILICIDE ON HEAVILY B-DOPED EPITAXIAL SiGe FOR ULTRA-SHALLOW SOURCE/DRAIN CONTACTS. Christian Isheden, Johan Seger, Henry Radamson, Shi-Li Zhang, Mikael Östling, Kungliga Tekniska Högskolan, Department of Microelectronics and Information Technology, Kista, SWEDEN.

Nickel monosilicide (NiSi) is one of the most promising candidates for low-resistivity contact formation in ultra-shallow source/drain junctions. In this study, the solid-state interaction between Ni and heavily B doped epitaxial $Si_{1-x}Ge_x$, intended for use in raised source/drain regions, has been investigated. Nickel was deposited on $Si_{1-x}Ge_x$ films with varying composition and subsequently heat-treated using rapid thermal processing over a range of temperatures. Sheet resistance measurements were used to monitor the interaction between Ni and $Si_{1-x}Ge_x$, resulting in Ni(Si,Ge). The results indicate that the Ni(Si,Ge) film is stable over a wide range of temperatures from 400 to 700 °C. Thus, there is a decent process window for simultaneous silicide formation on the poly-Si gate. Phase identification was carried out using X-ray diffraction (XRD). Epitaxial alignment is observed when Ni(Si,Ge) is formed on strained epitaxial $Si_{1-x}Ge_x$ substrates, which seems to improve the morphological and phase stability of the Ni(Si,Ge) film compared to silicide formed on poly-$Si_{1-x}Ge_x$. For the Ni/Si(100) reference, no such epitaxial alignment is observed. High-resolution XRD was used to determine the Ge fraction and thickness of the $Si_{1-x}Ge_x$ layers. Finally, results on the influence of Ge fraction on the properties of the film and electrical characterization of the metal-semiconductor contact between Ni(Si,Ge) and epitaxial $Si_{1-x}Ge_x$ will be presented.

4:15 PM N4.10

ELECTRON MICROSCOPY STUDY OF PHASE FORMATION IN Ti(Ta)-Ni/(001)Si AND Co-Ti/(001)Si IN NITROGEN ATMOSPHERE. A.L.Vassiliev, M. Aindow IMS, University of Connecticut, Storrs, CT; and A.G. Vasiliev, I.A. Horin, A.A. Orlikovsky, Institute of Physics and Technology, Russian Academy of Sciences, Moscow, RUSSIA, and Moscow State Institute of Radioengineering, Electronics and Automation (Technical University), Moscow, RUSSIA.

There have been considerable recent efforts to produce sequential layers for contact and barrier technologies by controlled solid state reactions of a multiple-component deposit. In this paper we describe a series of electron microscopy investigations on the microstructure produced by solid-phase reactions between (001) Si substrates and Ti-Co, Ti-Ni or Ta-Ni alloys deposited in a nitrogen ambient. For the Co-Ti alloys, it was found that deposition by rf-magnetron sputtering at 700 C led to the formation of a Ti-Si layer formed at the Si surface. Above a certain layer thickness, this acted as an effective barrier to the inward diffusion of Co, and led to the formation of cobalt silicides films with flat interface. When the barrier layer was not thick enough, the Co disilicide precipitates protruded to the Si substrate in a form of spikes. For the Ti-Ni and Ta-Ni alloys, deposition by e-beam coevaporation onto (001) Si substrate heated to 800 C also led to phase separation. In these systems, a thin upper layers of Ta silicide or Ta (Ti)-Ni silicide was formed, with a lower Ni silicide layer consisting of inverted epitaxially grown pyramids. These two layers were often separated by 1-2 nm amorphous layer. The way in which these distinctive microstructures develop will be discussed.

4:30 PM N4.11

NICKEL, PLATINUM AND ZIRCONIUM GERMANOSILICIDE CONTACTS TO HEAVILY PHOSPHOROUS DOPED SILICON-GERMANIUM ALLOYS FOR ADVANCED CMOS SOURCE/DRAIN JUNCTIONS. Hongxiang Mo, Jing Liu, and Mehmet C. Öztürk, NC State University, Department of Electrical and Computer Engineering, Raleigh, NC.

According to the International Technology Roadmap for Semiconductors, for technology nodes beyond 65 nm, source/drain contact resistance will dominate the MOSFET parasitic series resistance and require contact resistivity values within 2.4 6.4 x 10^{-8} ohm-cm^2. Selective $Si_{1-x}Ge_x$ source/drain technology is currently considered as a potential technique to form the ultra-shallow junctions of future CMOS technology nodes. One of the key advantages of the technology is the smaller bandgap of $Si_{1-x}Ge_x$, which provides a smaller contact barrier height, an essential requirement for low contact resistivity. We have previously reported low-resistivity Pt and Ni germanosilicide contacts to heavily boron doped $Si_{1-x}Ge_x$ alloys. In this work, we present formation of low resistivity germanosilicide contacts to phosphorous-doped $Si_{1-x}Ge_x$ alloys. Ni, Pt and Zr layers were deposited by RF-Sputtering and annealed in N_2 at temperatures ranging from 350 900°C for 30 seconds to form germanosilicides. Zr germanosilicide was found to be the most thermally stable of the three germanosilicides withstanding temperatures as high as 900°C. Ni and Pt germanosilicide stability was found to be less and limited to 750°C. Analysis of the samples by X-Ray Diffraction revealed that germanosilicides formed at low temperatures transformed into pure silicides as a result of Ge out-diffusion at higher formation temperatures. We have also considered stacked metal layers of Ni, Pt and Zr. A typical stack consisted of a main metal and an interlayer metal with a thickness around 20% of the main metal. The contact resistivity values for different stacked layers were measured using four-terminal Kelvin structures. Zr germanosilicide contacts yielded the highest contact resistivity values possibly due to phosphorus diffusion into the contact reducing the phosphorus concentration at the germanosilicide/ $Si_{1-x}Ge_x$ interface. In general, best results were obtained with the Ni/Pt stack resulting in contact resistivity values near 10^{-8} ohm-cm^2.

4:45 PM N4.12

KINETICS OF AGGLOMERATION AND $NiSi_2$ PHASE FORMATION FOR NiSi ON Si. Christophe Detavernier, Christian Lavoie, James M.E. Harper, IBM T.J. Watson Research Center, Yorktown Heights, NY.

We have determined the rates of agglomeration and $NiSi_2$ phase formation during heating of NiSi on Si, using simultaneous in situ measurements of resistance, light scattering and x-ray diffraction. NiSi is a desirable contact to Si because of its low resistivity, limited Si consumption and low formation temperature. However, the formation of the higher resistivity phase $NiSi_2$ must be avoided for device applications. Ni thin films 5 to 30 nm thick were deposited on substrates of poly-Si and silicon-on-insulator (SOI) as blanket layers and 0.13 μm wide lines, and were studied using heating rates from 1 to 27 °C/s. At low heating rates and for the thinnest films studied, NiSi agglomeration precedes $NiSi_2$ nucleation by as much as 350°C. The agglomeration temperature decreases with decreasing film thickness and linewidth. Once the film is agglomerated, the formation of $NiSi_2$ is delayed to higher temperature by its low nucleation site density and decreased contact area. At high heating rates, agglomeration occurs at higher temperature, but still precedes $NiSi_2$ formation. We conclude that agglomeration is the primary failure mechanism limiting the morphological stability of NiSi as a contact material to Si devices.

SESSION N5: POSTER SESSION
ATOMIC LAYER DEPOSITION - II / HIGH-k CHARACTERIZATION - III
Chair: Stefan De Gendt
Tuesday Evening, December 3, 2002
8:00 PM
Exhibition Hall D (Hynes)

N5.1

REACTION MECHANISM STUDIES ON ATOMIC LAYER DEPOSITION OF MICROELECTRONIC MATERIALS. Antti Rahtu, Raija Matero, Marika Juppo, Mikko Ritala, Univ of Helsinki, Dept of Chemistry, FINLAND.

Reaction mechanisms in the oxide and nitride atomic layer deposition (ALD) processes such as Al_2O_3, TiO_2, ZrO_2, $SrTiO_3$ and TiN were studied with quadrupole mass spectrometer (QMS) and quartz crystal microbalance (QCM). These materials have many potential applications such as insulating layers in DRAMs, gate oxides and diffusion barriers in MOSFETs. As an example different titanium alkoxides were studied as ALD precursors. The alkoxide group was found to have a strong effect to the ALD reaction mechanism and the stability of the precursor against thermal decomposition. In general, various important issues can be monitored with the in situ methods,

such as the effect of growth surface and the metal ratio of ternary films. This allows a sophisticated control of ALD processes. In addition to reaction mechanism studies, also recent improvements of the experimental set-up will be reported.

N5.2
EFFECT OF POST-METALLIZATION HYDROGEN ANNEALING ON C-V CHARACTERISTIC OF ZIRCONIA GROWN USING ATOMIC LAYER DEPOSITION. Arpan Chakraborty, V. Venkataraman, Indian Institute of Science, Department of Physics, Bangalore, INDIA; Anil U. Mane, S.A. Shivashankar, Indian Institute of Science, Materials Research Center, Bangalore, INDIA.

Most of the alternative gate dielectric materials examined to date appear to have a substantial amount of fixed charge, giving rise to large shifts in the flat-band voltage (V_{FB}). Shifts in the V_{FB} values are undesirable and this could present significant issues for CMOS applications. Moreover on voltage cycling the fixed charge gives rise to a hysterectic change in the V_{FB}. This affects a stable and reliable transistor operation. Annealing has some influence on the electrical characteristic of dielectrics. We have studied the effect of post-metallization annealing on the C-V curve of MOS capacitors with zirconia as the gate dielectric.
Thin films of ZrO_2 were deposited by ALD on p-Si(100). Aluminum was deposited as the gate metal. C-V measurements, on as-grown MOS capacitors, showed large hysteresis-width (~4-6V) as the gate-bias was swept from inversion to accumulation, and back to inversion. The samples were then annealed in hydrogen ambient for up to 30 minutes at different temperatures. Samples were annealed at successively higher temperatures in steps of 50°C and C-V measurements at 1MHz were done after annealing at each temperature. Hysteresis-width was calculated from the C-V curves. It was noted that the hysteresis-width decreased considerably as the annealing temperature was increased from room temperature to 200°C. But increasing the annealing temperature above 200°C resulted in increasing hysteresis-width. A minimum hysteresis-width of ~80mV was observed on annealing the sample at 200°C. The same experiment was carried out on samples grown using two different metalorganic complexes of Zr as precursors, and employing different deposition conditions, viz. different substrate temperature and different pulse duration of the reactants. Consistent results were obtained in every case. The lowest hysteresis-width was obtained at ~200°C in all the cases. Perhaps this method could be used to reduce the hysteresis-width in zirconia samples grown using different methods.

N5.3
PHYSICAL-CHEMICAL EVOLUTION UPON THERMAL TREATMENTS OF Al_2O_3, HfO_2 AND Al/Hf COMPOSITE MATERIALS DEPOSITED BY ALCVD. Barbara Crivelli, Mauro Alessandri, Stefano Alberici, Francesco Cazzaniga, Giuseppe Pavia, Giuseppe Queirolo, Federica Zanderigo, STMicroelectronics, Agrate Brianza, ITALY; David Dekadjevi, Laboratorio MDM-INFM, Agrate Brianza, ITALY; Jan Willem Maes, ASMB, Leuven, BELGIUM; Giampiero Ottaviani, University of Modena, Dept of Physic and Unita' INFM, Modena, ITALY; Sandro Santucci, University of L'Aquila, Dept of Physic and Unita' INFM, Coppito, ITALY.

In ULSI technology, high-k materials are considered feasible candidates for several applications in 100 nm CMOS generation and beyond. This paper presents a systematic investigation of thermal stability of high-k materials deposited by ALCVD in ASM Pulsar 2000 reactor. Physical-chemical evolution of Al_2O_3, HfO_2 and Al/Hf composite materials (aluminates and nanolaminate) was studied considering two types of thermal treatments: quenched vacuum anneals from 300°C to 900°C and furnace atmospheric processes in N_2 or O_2 at 850°C and 900°C. Material crystallization was studied by means of XRD and cross/planar TEM on vacuum annealed samples. Al_2O_3 was found still amorphous at 900°C. Not so for HfO_2 that crystallized in monoclinic phase at a temperature between 300-400°C. Crystallization temperature and possible phase separation of Al/Hf composite materials was found to be a function of Al_2O_3 content and film type. No variation in film and interfacial layer (IL) thickness were observed by both cross-sections TEM and XRR, while an increase in density was detected for pure materials from lower toward bulk values. Film thermal stability upon furnace treatments was found consistent with vacuum annealing results. In these samples, however, a chemical evolution was detected in addition to the above reported crystallization phenomena. TEM images evidenced a thicker interfacial layer, with no major differences upon temperature or annealing atmosphere. Non-contact electrical measurement showed that in correspondence with IL modification, but not directly correlated to that, increase in EOT and decrease in fixed charge were detected. Films composition was then studied by means of XRF, RBS, TOF-SIMS and XPS. Slightly increase in oxygen content, silicon diffusion from the substrate into high-k material and aluminum/hafnium redistribution were detected on all the annealed samples, but with differences depending on the class of material considered. All the achieved results demonstrate that depending on thermal treatment conditions, ALCVD high-k stability is not only related to possible phase-transition. A chemical evolution could also take place transforming "SiO_2/high-k" system into "doped-SiO_2/silicate" stack.

N5.4
STRUCTURAL PROPERTIES OF HIGH-K Y_2O_3 LAYERS PREPARED BY PULSED INJECTION PLASMA ENHANCED MOCVD. C. Vallée, C. Durand, M. Bonvalot, B. Pelissier, L. Vallier, O. Joubert LTM-CNRS, CEA-LETI, Grenoble, FRANCE.

Integration of high k materials in traditional industrial MOSFET devices is one of the major challenges to continued scaling of CMOS. Different methods are used to elaborate high k materials such as ALD (atomic layer deposition) and MOCVD (Metal Organic Chemical Vapor Deposition). In this study we have investigated an original method called pulsed injection Plasma Enhanced Metal Organic Chemical Vapor Deposition (PE-MOCVD). In this technique, $Y(thd)_3$ ($YO_6C_{33}H_{57}$) precursors (powder) are dissolved in cyclohexane and sequentially injected into an evaporator, which allows a perfect reproducibility of the amount of precursor delivered to the oxygen plasma chamber and then onto the substrate heated at 350°C. The Y_2O_3 high k material has been selected because it exhibits a medium k value as compared to SiO_2 and is thermodynamically compatible with silicon. The first challenge to achieve thin layers of Y_2O_3 with good electrical properties by PE-MOCVD is to completely remove carbon and hydrogen contaminations from the material, and to reduce material porosity. Some residual carbon (~6%) was found in Y_2O_3 layers obtained by ALD from $Y(thd)_3$ and O_3. In our new pulsed injection PE-MOCVD process, this can be achieved thanks to the assistance of an oxygen-rich plasma. For this purpose, we have investigated the effect of both pressure and RF power injected in the O_2 plasma on the precursor fragmentation and carbon removal by optical emission spectroscopy (OES). Plasma pressure also influences the process: at low pressure, plasma sheaths are nearly collision-free so high energy ions can bombard the surface while at the same time substrate heating is not optimum. Similarly, an opposite behavior (low bombardment energy and high substrate temperature) is obtained for a high pressure plasma. High bombardment may induce high interfacial state density (D_{it}) whereas a high substrate temperature may induce the formation of a silicate interface.

N5.5
STUDY OF THE INITIAL STEP OF HIGH K GROWTH BY ATOMIC LAYER DEPOSITION ON DIFFERENT STARTING SURFACE. J.-F. Damlencourt[a], F. Bedu[b], D. Blin[c], P. Holliger[a], O. Renault[a], F. Martin[a] and M.-N. Semeria[a]; [a]Leti (CEA-Grenoble), Grenoble, FRANCE; [b]STMicroelectronics, Crolles, FRANCE; [c]ASM-France, Montpellier, FRANCE.

High K dielectric materials such as HfO_2 and generic materials are now considered as serious candidates for gate dielectric applications due to their polysilicon gate compatibility. Preliminary encouraging results on these high K film must be confirmed through the use of manufacturing tools such as CVD, ALD. This paper focuses on the initial stage of the growth of high K materials on different surface preparations by Atomic Layer Deposition at 300°C and 350°C. On thin SiO_2 layers, no nucleation retardation was observed. However, the total dielectric constant measured on these layers was found to be lower than that of high K materials without SiO_2 layer. Therefore, the SiO_2 layers must be kept as thin as possible. Consequently, growth on HF dipped silicon surfaces was then investigated. We have pointed out the lack of nucleation groups (e.g. OH groups) on the H-terminated silicon surface induced some nucleation retardation. We have also evidenced, by STM and AFM, that the starting growth was three dimensional. The high K dots, thus formed, subsequently grow then coalesce into a 3D rough layer. Moreover, some interfacial oxide regrowth occurred during the subsequent deposition. An innovative chlorine chemical treatment on H-terminated silicon surface has been investigated. This treatment led to a surface with only one monolayer of OH groups. No nucleation retardation was observed anymore and very smooth layers were obtained. A 2D starting growth was observed by ATR. Moreover, a very thin parasitic bottom SiO_2 layer generated during deposition was pointed out by XPS. The composition and structure of these layers and their interface with Si were characterized by complementary physico-chemical techniques such as SIMS, XPS, AFM and ATR. Electrical characterizations of thin Al_2O_3 and HfO_2 layers deposited on Chlorine treated Silicon will be also presented.

N5.6
PHYSICAL AND ELECTRICAL PROPERTIES OF Al_2O_3-HfO_2 NANOLAMINATE FILMS PREPARED BY ATOMIC LAYER DEPOSITION FOR ADVANCED CMOS GATE DIELECTRIC APPLICATIONS. Takaaki Kawahara, Seiichi Fukuda, Takeshi Maeda, Atsushi Horiuchi, Akiyoshi Muto, Yoshitake Kato, Semiconductor

Leading Edge Technologies, Inc., Ibaraki, JAPAN.

The 2001 ITRS indicates that the technology node will reach to be 70nm in 2006, and that high-k materials are indispensable for the gate dielectric of CMOSFETs. The expected targets of equivalent oxide thickness (EOT) and allowable gate leakage current, especially for a low standby power CMOS, are 1.4-1.8nm and 2.7mA/cm^2, respectively. High-k materials such as Al_2O_3, HfO_2, and ZrO_2 have been studied as candidates for their moderately high dielectric constants and good thermal stability in contact with silicon. Moreover, they are required to have small grain sizes compared with a gate length, that is, to be amorphous even after the annealing for the activation of S/D regions. In this work, we investigated the physical and electrical properties of Al_2O_3, HfO_2, and their nanolaminate films deposited on 300mm Si wafers by Atomic Layer Deposition (ALD). The precursors are TMA/H_2O for Al_2O_3 and $HfCl_4$/H_2O for HfO_2, and one cycle, for example for Al_2O_3, consists of H_2O purge, TMA pulse, TMA purge, and H_2O pulse. These depositions were carried out at 300°C on 1nm-thick SiO_2 underlayer, and the atomic ratios Hf/(Hf+Al) of the nanolaminate films were controlled by changing the cycle numbers for Al_2O_3 and HfO_2, respectively. The physical properties of these films were measured by XRF, XRD, and TEM, and the electrical properties were measured by using aluminum gate electrodes, which were deposited through a shadow mask by RF sputtering.
The dependences of the EOT-values on the physical thicknesses of Al_2O_3 and HfO_2 films indicate that their dielectric constants were 10 and 27, respectively. In-plane XRD measurements indicate that 3nm-thick HfO_2 films with polysilicon gate deposited at 530°C have the crystalline peaks of HfO_2 even without a post-annealing. However, the nanolaminate films of Hf/(Hf+Al)=0.5-0.6 with the post-annealing of less than 900°C have no crystalline peak of HfO_2. Moreover, in case of Hf/(Hf+Al)=0.3, they have no crystalline peak even after the annealing of 1050°C. That is, it is found that the crystallization temperature of these nanolaminate films increases much higher than that of HfO_2 films.

N5.7

ULTRATHIN ZIRCONIUM DIOXIDE CHEMICALLY DEPOSITED AT A LOW THERMAL BUDGET. Stefan Harasek, Heinz D. Wanzenboeck, Helmut Langfischer, Emmerich Bertagnolli, Vienna University of Technology, Institute of Solid State Electronics, Vienna, AUSTRIA.

We report on the metal-organic chemical vapor deposition (MOCVD) of ultrathin zirconium dioxide on (100) silicon using a single-source precursor system. The formation of high-quality ultrathin layers of zirconium dioxide on silicon at moderate temperatures is investigated. Special emphasis is put on the evolution of surface topography and the impact of processing parameters on the chemical composition of the films issuing different deposition temperatures and annealing processes. Electrical characterizations by means of MOS structures have been performed to assess the interface quality and the dielectric properties of the layers. Interface trap density is observed to be around 5.10^{11} cm^{-2}.eV^{-1} at midgap for (100)-oriented substrates and layer thicknesses down to an EOT of less than 2 nm. Leakage currents in the ultrathin regime are several orders of magnitude lower than those found in equivalent SiO_2-layers. Trap density and leakage current are strongly sensitive to the annealing atmosphere. Both are shown to be positively affected by annealing in forming gas rather than in an oxidative atmosphere. All temperatures throughout the gate insulator formation process do not need to exceed 650°C, thus keeping the thermal budget low enough to avoid any unintentional smear out of diffusion profiles.

N5.8

ORIENTED GROWTH OF THIN FILMS OF SAMARIUM OXIDE BY MOCVD. K. Shalini, S.A. Shivashankar, Materials Research Centre, Indian Institute of Science, Bangalore, INDIA.

Metal-oxide-semiconductor (MOS) structures are widely used in modern solid-state electronics. It is expected that, as dimensions of silicon integrated circuits shrink further, silicon dioxide would have to be replaced as the gate dielectric by a material with a higher dielectric constant. This gives rise to the necessity of finding and investigating the properties of new insulating materials. Rare earth oxides are examples of such materials, characterized by high values of dielectric constant (8-20) and by resistivity, and high chemical and thermal stability. However, silicon MOS structures with rare earth oxides have not been investigated extensively. We have, therefore, undertaken the growth of various rare earth oxides by metalorganic chemical vapor deposition (MOCVD). In this paper, we report the growth of thin films of samarium oxide on Si(100) and fused quartz by low-pressure MOCVD using an adducted beta-diketonate precursor developed in house. It is found that the growth is strongly dependent on the substrate material as well as on the growth temperature. As examined by X-ray diffraction, the films of Sm_2O_3 grown at lower temperatures (550°C) on quartz are cubic and display a random grain orientation, while they become highly oriented in the (111) direction as the growth temperature is increased (to 625°C). On Si(100), highly oriented films of cubic Sm_2O_3 are obtained at a substrate temperature of 625°C. When the growth temperature is raised, the phase changes to monoclinic. The morphology of the films grown on both quartz and Si(100) substrates has been studied by SEM and atomic force microscopy, which corroborate the XRD data. The growth of strongly oriented Sm_2O_3 on the disordered surface of fused quartz may be interpreted as being driven by the minimization of surface energy.

N5.9

IMPROVED ALKOXIDE PRECURSORS FOR THE MOCVD OF HfO_2. A.C. Jones, J.L. Roberts, N.L. Tobin, P. Marshall, P.R. Chalker, University of Liverpool, Liverpool, UNITED KINGDOM; M. Schumacher, AIXTRON AG, Aachen, GERMANY; T.J. Leedham, H.O. Davis, P.A. Williams, Inorgtech Limited, Mildenhall, UNITED KINGDOM; L.M. Smith, Epichem Limited, Bromborough, UNITED KINGDOM.

HfO_2 is a promising candidate to replace SiO_2 as the gate dielectric material in sub 0.1μm CMOS technology. Metalorganic chemical vapour deposition $(MOCVD)$ is an attractive technique for the deposition of HfO_2 thin films as it offers the potential for large area growth, good composition control, high film uniformity and superior conformal step coverage. Metal alkoxides are attractive MOCVD precursors, as they generally allow the deposition of high purity oxide films at low substrate temperatures, but the use of alkoxide precursors for the deposition of HfO_2 has been limited, as the majority of $[Hf(OR)_4]$ complexes are oligomeric with low volatility. Although $[Hf(OBu^t)_4]$ is volatile, it is extremely moisture sensitive which limits its shelf life and makes it difficult to handle and use in liquid injection MOCVD. To solve this problem we have developed the volatile monomeric complexes $[Hf(OBu^t)_2(OCMe_2CH_2OMe)_2]$ and $[Hf(OCMe_2CH_2OMe)_4]$, which are significantly less moisture sensitive than $[Hf(OBu^t)_4]$. In this paper we describe the use of these complexes for the liquid injection MOCVD of HfO_2, and compare the properties of the films with those grown using other potential HfO_2 precursors such as $Hf(NMe_2)_4$.

N5.10

PULSED PLASMA ENHANCED MOCVD OF HIGH K Y_2O_3 LAYERS FOR GATE DIELECTRIC APPLICATIONS. B. Pelissier, C. Durand, C. Vallèe, M. Bonvalot, L. Vallier, O. Joubert, LTM, CNRS, Grenoble, FRANCE.

The so-called High k dielectric materials are seriously considered to replace SiO_2 as the gate dielectric in advanced CMOS devices. Many new materials are currently under investigation: rare earth oxides are considered as promising candidates. We present here an innovative MOCVD process to depose highK Y_2O_3 thin layers. It combines the high reproducibility of a pulsed injection liquid source and the advantages of plasma enhanced CVD. Y(thd)3 precursor dissolved in cyclohexane is injected in the liquid phase into an evaporator, flash-evaporated, and brought to the plasma chamber via a carrier gas. The key benefit of this system is the very accurate delivery control of little amounts of precursor without any preliminary decomposition. The plasma assistance using Ar/O_2 gas mixtures allows a low temperature precursor decomposition. Our results show that stoechiometric Y_2O_3 layers (typ. 5nm thick) can be deposited on Si substrate at temperatures as low as 350°C due to the plasma assistance, whereas no Yttrium is detected without plasma activation. In-situ plasma treatments just after Y_2O_3 deposition have also been investigated. They lead to a drastic reduction of the carbon contamination in the highK film without recrystallization and with limited effect on the interface. Comparison with ex-situ annealing at higher temperatures have also been established. XPS and IR characterizations reveal the formation of a silicate type layer at the interface with the substrate. Moreover, this interface layer can be SiO_2 free if the Yttrium precursor flow at the beginning of the deposition is large enough. Due to a higher thermodynamical stability of Y_2O_3 versus SiO_2, we assume that this layer results from a reaction between Yttrium and the underlying Si/SiO_2 substrate. Preliminary C-V measurements have shown encouraging results with an EOT of less than 3nm. Our pulsed injection liquid delivery source is particularly well suited for studying the first stages of the growth mechanisms and some work is underway to understand and reduce the formation of the silicate interface layer which limits the capacitance of the gate stack.

N5.11

ALD HfO_2 SURFACE PREPARATION STUDY. Annelies Delabie, Matty Caymax, Bert Brijs, Thierry Conard, Stefan De Gendt, Marc Heyns, Wilfried Vandervorst, Chao Zhao, IMEC vzw, Leuven, BELGIUM; Jan-Willem Maes, ASM Belgium, Leuven, BELGIUM; Martin Green, Jon Kluth, Wilman Tsai, ISMT residents at IMEC.

High-k materials such as Al_2O_3, ZrO_2 and HfO_2 have been studied

extensively as they are considered as alternative gate dielectric for SiO_2 in (sub-) 100 nm devices. Atomic layer deposition (ALD) is a well suited technique to produce thin layers of these materials. The technique is based on sequential saturating gas-solid reactions, which results in excellent uniformity of the deposited layers and accurate film thickness control. One of the requirements to achieve controlled ALD growth is the presence of well-distributed reaction sites at the starting surface. In unfavorable starting conditions, the metal oxide will grow as islands, causing multiple weak spots in the film. For the deposition of most ALD layers, hydroxyl groups should be present on the surface prior to the exposure of reactant vapors. On the other hand, the presence of SiO_2 at the Si/HfO2 interface (caused i.e. by surface preparation) must be controlled to the absolute minimum as it adds significantly to the EOT (equivalent oxide thickness) of the high-k stack. In the present work, the ALD HfO_2 growth behavior on different types of starting surfaces (Si-OH, Si-H terminated, NH_3 annealed surface) is examined. The amount of Hf at the early stages of the ALD process is measured by means of RBS (Rutherford Back Scattering) and XRF (X-ray reflective fluorescence). The HfO_2 film quality on different starting surfaces was examined with TOFSIMS (Time Of Flight Secondary Ion Mass Spectroscopy), a very surface sensitive technique. An exponential decrease of the Si-intensity is expected when the surface gets covered by a perfectly closed HfO_2 layer. Slower decays and deviations from this exponential decay reflect imperfections in the film. The effect of inserting a thin layer of Al_2O_3 at the starting surface on the growth and quality of HfO_2 is also discussed.

N5.12
A NEW APPROACH FOR METAL OXIDE FILM GROWTH: VAPOR-LIQUID HYBRID DEPOSITION (VALID). Tetsuji Yasuda, MIRAI Project, Advanced Semiconductor Research Center (ASRC), National Institute of Advanced Industrial Science and Technology (AIST), Tsukuba, JAPAN; Ronald Kuse, MIRAI Project, Association of Super-Advanced Electronics Technology (ASET), Tsukuba, JAPAN.

A common problem of CVD-based processes in forming device-quality metal oxides is incorporation of residual ligand impurities resulting from incomplete decomposition of metal-organic or metal-halide precursors. We demonstrate a new deposition process that is intended to overcome this problem. It consists of two half reactions similar to conventional atomic layer deposition (ALD): i) adsorption of metal source molecules, and ii) hydrolysis of the adsorbed species to complete conversion to oxide. The key feature of the new process is that it carries out the hydrolysis reaction by exposing the wafer to *liquid* water rather than water vapor as used in conventional ALD. Adsorption of the metal precursor is performed in a vacuum chamber by delivering its vapor. Thus the process is a hybrid of vapor and liquid depositions (VALID). The liquid-phase hydrolysis expectedly achieves perfect conversion of the adsorbed metal precursor molecules to oxide even at room temperature. Subsurface oxidation, which often causes uncontrolled increase of the equivalent oxide thickness, is limited in the VALID process due to the low hydrolysis temperature. So far we have succeeded in forming ultrathin films of Al_2O_3 and SiO_2 using $Al(CH_3)_3$ and $SiCl_4$ sources, respectively. The deposition rate was 0.05 to 0.1 nm per cycle, comparable to those reported for the conventional ALD processes. Surfaces of the grown oxide layers are as smooth as the initial substrate surfaces (RMS $\sim$ 0.02 nm) which were prepared by UV-O_3 oxidation of H-terminated Si(001). C-V and I-V characterization of the capacitors incorporating an interfacial VALID-Al_2O_3 layer has proven that VALID is a viable technique to form the gate-quality insulators. This study was supported by NEDO.

N5.13
ULTRAVIOLET ASSISTED OXIDATION OF PULSED LASER DEPOSITED HAFNIUM METAL ON SILCON FOR ALTERNATIVE HIGH-k GATE DIELECTRICS. C. Essary, J.M. Howard, V. Craciun, and R.K. Singh, Department of Materials Science & Engineering, University of Florida, Gainesville, FL.

In the search for an alternate high-k dielectric material to replace silicon dioxide, hafnium oxide has shown promise. In this study, hafnium metal has been deposited on silicon wafers using a conventional pulsed laser deposition system. The films were then heated and oxidized in an oxygen rich atmosphere, one set was oxidized in the presence of an array of mercury vapor lamps emitting radiation in the 185 and 254 nm wavelength regions. The samples were then in-situ annealed. Film quality and stoichiometry was assessed using x-ray photo-electron spectroscopy, x-ray reflectivity, and Fourier transform infrared spectroscopy. Electrical properties of the films were checked using current-voltage and capacitance-voltage measurements using platinum electrodes and a comparison between the ultraviolet radiated and non-radiated samples were made. Hi-resolution transmission electron microscopy was used to examine the interfacial differences in the films in order to correlate the finding of the electrical characterization to the structure of the film.

N5.14
EFFECT OF NATURE OF THE PRECURSOR ON CRYSTALLINITY AND MICROSTRUCTURE OF MOCVD-GROWN ZrO_2 THIN FILMS. M.S. Dharmaprakash and S.A. Shivashankar, Materials Research Center, Indian Institute of Science, Bangalore, INDIA.

Thin films and coatings of zirconia are important for a number of modern applications, such as sensors, mirrors, protective coatings, fuel cells, and dielectric layers in microelectronics. Metal-organic chemical vapor deposition is an effective technique for the deposition of ZrO_2 thin films as it offers the potential for growth at relatively low temperatures, large area films with uniform thickness, high film density, high deposition rates, controllable composition, and excellent step coverage. In the present work, thin films of zirconia have been deposited on Si(100) at various substrate temperatures by low-pressure metalorganic chemical vapor deposition in a reactor built in house. Three different precursors, synthesized and characterized in our laboratory, viz., tetrakis(pentadionato)zirconium(IV), [Zr(pd)$_4$], tetrakis(2,2,6,6-tetramethyl-3,5-heptadionato)zirconium(IV), [Zr(thd)$_4$], and tetrakis(t-butyl-3-oxo-butanato)zirconium(IV) [Zr(tbob)$_4$], have been used as the precursor. The relationship between the molecular structures of the precursors and their thermal properties, as examined by TGA/DTA will be presented. The films deposited using these precursors have distinctly different morphology, though all of them are of the cubic phase. The films grown from Zr(thd)$_4$ are well crystallized, showing faceted growth at 575°C, whereas the films grown from Zr(pd)$_4$ and Zr(tbob)$_4$ are less crystalline, and display cracks. These differences in the observed microstructure may be attributed to the different chemical decomposition pathways of the precursors during the film growth, which influence the nucleation and the growth processes. This also evidenced by the different kinetics of growth from these three precursors under identical CVD conditions. The details of thin film deposition, and film microstructure analysis by XRD, SEM, and TEM will be presented. The dielectric quality of the films deposited from different precursors, studied by C-V measurements, will be compared. Dielectric properties at optical frequencies, as measured by ellipsometry, will also be presented.

N5.15
GROWTH AND PHYSICAL PROPERTIES OF MOCVD-DEPOSITED HAFNIUM OXIDE FILMS AND THEIR PROPERTIES ON SILICON. Sven Van Elshocht[a], Matty Caymax[a], Stefan De Gendt[a], Thierry Conard[a], Jasmine Pétry[a], Martine Claes[a], Thomas Witters[a], Chao Zhao[a], Bert Brijs[a], Olivier Richard[a], Hugo Bender[a], Wilfried Vandervorst[a], Richard Carter[a], Jon Kluth[b], Lucien Daté[c], Didier Pique[c], and M.M. Heyns[a]; [a]Imec v.z.w., Heverlee, BELGIUM; [b]International Sematech, Austin, TX; [c]Applied Materials France, Meylan, FRANCE.

The continuous downscaling of the SiO_2 insulator thickness to increase device performance will eventually result in an unacceptably high leakage current. Replacing SiO_2 with so-called high-k materials allows increasing the physical thickness of the insulator material without compromising on capacitance. Several materials are being screened as possible candidates, for example ZrO_2, HfO_2, and their respective silicates and aluminates, with industry mainly being focused on HfO_2. In this paper we will discuss HfO_2 as deposited by metal organic chemical vapor deposition (MOCVD) using tetrakis(diethylamino)hafnium (TDEAH) as precursor on 8" Si (100) wafers. We have studied the influence of the starting surface and deposition temperature on the growth kinetics and physical properties of the HfO_2 layers. Important characteristics such as crystalline state, density, and organic contamination in the layers were found to be dependent on these parameters.
Characteristic for this deposition process is the formation of an interfacial layer underneath the high-k layer. Such an interfacial layer has important consequences since the equivalent oxide thickness (EOT) of the total gate stack is determined by the contribution of both the high-k film as well as the lower-k interfacial layer.
We show that after deposition the interfacial layer has a Hfsilicate-like composition and this for both H-terminated as well as SiO_2 type starting surfaces. The thickness of this interfacial layer is observed to be a function of the starting surface, deposition time and temperature, where the relative importance of these parameters is dependent on the specific thickness of the HfO_2 layers.
Finally, we will show electrical results, including gate leakage current and EOT-values, for HfO_2/polySi gate stacks studying the effects of for example starting surface and post deposition treatments. These results also show that the modification of the interfacial layer into a Hfsilicate increases this layers k-value as compared to SiO_2, lowering EOT-values.

N5.16
ELECTRICAL AND STRUCTURAL CHARACTERIZATION OF

HfO MIM AND MIS CAPACITORS. Fan Yang, David E. Kotecki, University of Maine, Dept. of Electrical and Computer Engineering, Orono, ME; George Bernhardt, Laboratory for Surface Science and Technology, University of Maine, Orono, ME.

Hafnium oxide is a promising dielectric for future microelectronic applications. HfO thin films (< 60nm) were deposited on $Pt/SiO_2/Si$ and Si substrates by DC magnetron reactive sputtering. Top electrodes of Pt were formed by e-beam evaporation through an aperture mask to create MIM and MIS capacitors. Various process conditions (deposition temperature, Ar/O_2 ratio, pressure, DC power, and time) and post-deposition annealing conditions (time and temperature) were investigated. The structure of the HfO films was characterized by X-ray diffraction (XRD) and the electrical properties were characterized in terms of their relative permittivity $\epsilon_r(\omega)$, and leakage behavior, I-V, and I-t. The electrical measurements were performed over a temperature range of -50 to 200°C. For films deposited at low temperatures (< 100°C), the relative permittivity was found to increase by $\sim$ 2X over the measured temperature range. Humidity uptake was found to be an important parameter when performing the electrical measurements.

N5.17
ULTRATHIN HAFNIUM SILICON-OXYNITRIDE FILMS GROWN BY UV/OZONE OXIDATION. P. Punchaipetch, G. Pant, M.A. Quevedo-Lopez, C. Yao, H. Zhang, M.J. Kim, M. El-Bouanani, R.M. Wallace and B.E. Gnade, Department of Materials Science, University of North Texas, Denton, TX.

Hafnium silicate ($HfSi_xO_y$) dielectric films are considered as a potential candidate to replace SiO_2 or SiON as the gate dielectric in CMOS processing. The Hf concentration in the film affects the crystallization temperature and phase stability. [1-2] The addition of nitrogen into this pseudo-binary alloy [3] has been shown to improve their thermal stability, electrical properties, and reduce dopant penetration. [4-5] Nitrided hafnium silicide films were deposited on a H-terminated Si surface by plasma sputtering from a Hf silicide target. The films were subsequently oxidized to nitrided hafnium silicate ($Hf_xSi_{1-x}O_yN_z$) by exposing the wafers to UV radiation in oxygen ambient. This approach produced good quality hafnium silicate films, with no detectible interfacial SiO_2. [6] Rutherford Backscattering Spectrometery (RBS), X-ray Photoelectron Spectroscopy (XPS), and High Resolution Transmission Electron Microscopy (HR-TEM) were used to determine the composition, chemical bonding environment and thickness of the films. The cross-sectional transmission electron micrograph indicates an amorphous $Hf_xSi_{1-x}O_yN_z$ layer with good uniformity. Moreover, there was no low κ-interfacial layer detected by XPS and visible in TEM images. The electrical performances of the as-deposited and annealed films were analyzed using current-voltage (I-V) and capacitance-voltage (C-V) measurements. Results on the effect of several processing parameters, including: sputter gas mixture, UV/ozone oxidation parameters, and post-annealing in different gases (N_2, O_2, NO, N_2O) will be discussed. Implications for high-κ gate dielectric applications will be presented. This work was supported partially by the US Army Soldier Systems Command (Contract #DAAD16-00-C-9273) and the Texas Advanced Technology Program.
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N5.18
INTERFACE QUALITY AND ELECTRICAL PERFORMANCE OF LOW-TEMPERATURE METAL ORGANIC CHEMICAL VAPOR DEPOSITION ALUMINUM OXIDE THIN FILMS FOR ADVANCED CMOS GATE DIELECTRIC APPLICATIONS. Spyridon Skordas, Filippos Papadatos, Steve Consiglio, Eric Eisenbraun, and Alain E. Kaloyeros, University at Albany Institute for Materials, School of Nanoscience and Nanoengineering, Albany, NY; Evgeni Gusev, IBM T.J. Watson Research Center, Yorktown Heights, NY.

A previously developed low-temperature, metal organic chemical vapor deposition (MOCVD) process for the growth of aluminum oxide (Al2O3) thin films has been characterized with respect to electrical properties as a potential alternative gate dielectric layer[1]. The process employs an aluminum -diketonate metal organic precursor [aluminum(III) 2,4-pentanedionate] and water as metal and oxygen sources[1]. It has been optimized using a design of experiment approach, and features dense, amorphous Al2O3 films with carbon incorporation as low as 1 atomic % and hydrogen incorporation as low as 3 atomic %[1]. In this work, two sets of Al2O3 depositions in the 2-10 nm thickness range were carried out on different types of substrates respectively, 0.8 nm silicon (Si) oxynitride / Si(100) substrates and Si(100) substrates. The samples for each substrate type were separated in four splits, three of these splits were subjected to the following different annealing conditions, respectively: a) Forming gas anneal (FGA, 90% Ar, 10% H2) at 550°C for 30 min, b) rapid thermal annealing (RTA) in N2 at 700°C for 30 s, followed by FGA at 550°C for 30 min, and, c) O2 anneal at 550°C for 30 min followed by FGA at 550°C for 30 min. All samples from the resulting eight splits were analyzed by cross-sectional transmission electron microscopy (XTEM) combined with energy dispersive spectrometry (EDS) to investigate the quality of the interface between insulator and semiconductor and check for oxide interfacial layer as well as film continuity. Additionally, metal-Al2O3-silicon capacitor test structures were characterized by capacitance-voltage (C-V) and current-voltage (I-V) measurements in order to compare the electrical performance as a function of substrate and annealing method used. [1]. Spyridon Skordas, Filippos Papadatos, Zubin Patel, Guillermo Nuesca, Eric Eisenbraun, Evgeni Gusev1, and Alain E. Kaloyeros, presented at Symposium B, Materials Research Society Meeting, San Francisco, April 2002

N5.19
DETERMINATION OF THE DIELECTRIC CAPACITANCE OF ULTRATHIN HIGH-K DIELECTRICS. Samares Kar, Indian Inst of Technology, Kanpur, INDIA.

The gate dielectric capacitance, is the most important element, in determining the performance parameters of the MISFETs. Particularly, in the case of the ultrathin gate dielectrics, the extraction of the gate dielectric capacitance from the measured MIS capacitance-voltage, C-V, characteristic, is complicated by: (1) a non-saturating accumulation capacitance, (2) a large dielectric leakage current density, (3) the series resistance, and (4) the polysilicon capacitance. A few techniques exist, which were developed to extract the gate SiO2 capacitance. These techniques operate under a number of assumptions, the common among all these being: (1) The difference between the interface trap charge at flat band and that under strong accumulation can be neglected. (2)The interface trap capacitance is negligible in the 100 kHz or the 1 MHz capacitance. In the case of the high-K gate dielectrics, with their much higher interface trap densities, both the above assumptions may be unjustified, as the results of this investigation indicate. The objective of the present investigation was to develop a C-V extraction technique for the ultrathin high-K gate dielectric capacitance, which will better address the above concerns, and be cost-effective in terms of time. Our technique employs the low frequency C-V, instead of the high frequency C-V, and neither neglects the interface trap charge, nor the interface trap capacitance. (As our technique employs the low frequency C-V, the series resistance issue is also addressed.) This technique yields the dielectric capacitance of ultrathin high-K gate dielectrics, and also an accurate experimental silicon surface potential, as a function of the gate voltage. We have applied our technique and the existing techniques to five different high-K gate dielectrics: The existing techniques did not work well with the high-K gate dielectrics, most likely, because of the higher interface trap density, as mentioned above.

N5.20
THERMAL STABILITY OF HAFNIUM OXIDE AND HAFNIUM SILICATE FILMS DEPOSITED ON SILICON. Vidyut Gopal, Shreyas Kher, Craig Metzner, Edward Principe; Applied Materials Inc., Santa Clara, CA.

Hafnium oxide (HfO_2) and hafnium silicate (HfSiO) thin films were deposited by metal-organic chemical vapor deposition on silicon substrates. The microstructure of films of different thickness and composition, both as-deposited and subjected to rapid thermal anneal treatments, was investigated by grazing incidence x-ray diffraction (GIXRD), atomic force microscopy (AFM), and transmission electron microscopy (TEM). As-deposited HfO_2 films were found to be crystalline. The microstructure of as-deposited HfSiO films changed from crystalline to amorphous with increasing Si mole fraction. AFM measurements revealed that the surface roughness decreased with increasing Si content. Moderate temperature anneals decreased the surface roughness of HfSiO films, but high temperature anneals resulted in increased roughness. The changes in the microstructure of HfO2 and HfSiO revealed by this study have important implications since these films must withstand aggressive thermal treatments during subsequent process steps in integrated circuit fabrication.

N5.21
EXOELECTRON EMISSION SPECTROSCOPY OF TRAPS IN Si_3N_4 ULTRATHIN FILMS. Gil Rosenman, Michael Naich, Michel Molotskii, Dept of Electrical Engineering-Physical Electronics, Tel Aviv University, ISRAEL; Yakov Roizin, Tower Semiconductor, Ltd, ISRAEL.

The energetic and spatial distribution of traps in silicon nitride is of

principal importance for ONO (oxide-nitride-oxide) memories where information is stored as charge in the Si_3N_4 layer. The retention properties of microFLASH, two bit per cell transistors are determined by lateral migration of charge trapped in nitride at opposite channel edges and thus by the activation energy F of deep traps. We developed an original thermally stimulated exoelectron emission spectroscopy method (TSEE) of F measurements and applied it to ultrathin Si_3N_4 films. The technique consists in preliminary filling of traps by electron irradiation and subsequent registration of TSEE currents in the temperature range from 300 to 820K. The temperature spectra of TSEE of 50A nitride films demonstrate several peaks: three low temperature peaks (T1 =373K, T2=423K, T3=498K) and a high temperature maximum at T4 ~750K. The TSEE glow curves were modeled from first principles and used to determine the energy levels of traps. The obtained values are F1=0.65 eV, F2=0.74 eV, F1=0.87 eV, and F4=1.73 eV. TSEE results are shown to be consistent with F estimates obtained from memory transistor measurements. Electrons stored at traps with F4=1.73 eV explain excellent microFlash retention properties.

N5.22
EFFECTIVENESS OF PLASMA NITRIDED SILICON OXYNITRIDE AS A BARRIER LAYER BETWEEN HIGH *k* MATERIALS AND Si SUBSTRATES. Yi-Sheng Lai and J.S. Chen, Department of Materials Science and Engineering, National Cheng Kung University, Tainan, TAIWAN.

The performance of metal-oxide-semiconductor devices depends strongly on the characteristics of the interface between high *k* materials and Si substrate. In recent reports, even the thermally stable high *k* materials like HfO_2, ZrO_2, and silicates still generate an interlayer during the deposition and/or subsequent postannealing process. The cause possibly arises from the initial stage of SiO_x growth on bare Si or the oxygen species diffusing across the ultrathin high *k* matrix to react with the Si substrate. Additionally, the interface states (D_{it}) of high *k* materials is still too high (10^{11} - 10^{12} $cm^{-2}eV^{-1}$) for the usage of MOSFET devices. As a result, engineering of the interface becomes a very challenging issue on high *k* gate dielectrics. Silicon oxynitride (SiO_xN_y), which has good interfacial properties and may act as a diffusion barrier against reaction between Si and high *k* materials, is a promising candidate for gate dielectric applications. In this work, plasma nitridation was conducted using N_2O and NH_3 mixtures to produce an ultrathin SiO_xN_y layer. The bonding structure, distribution, and quantity of nitrogen and its effects on the growth kinetic of SiO_xN_y layers are studied by X-ray photoelectron spectroscopy (XPS). It is found that nitrogen atoms pile at the SiO_xN_y/Si interface at the very beginning of plasma N_2O and NH_3 nitridation. Due to the deficiency of additional Si source and low diffusivity of O or N atoms at low temperature (300 - 500°C), plasma nitridation will form a self-limited growth of SiO_xN_y layer. The linear dependence on the growth rate of plasma nitridation as a function of log(time) is observed. The thicknesses of ultrathin SiO_xN_y layers obtained from XPS show a higher sensitivity than those obtained from high-resolution transmission electron microscopy. Control of the nitrogen content and the thickness below 10 Å of our nitrided samples is therefore realized.

N5.23
ELECTRICAL CHARACTERIZATION AND QUANTUM MODELING OF MOS CAPACITORS WITH ULTRA-THIN (1.7-7 NM) OXIDES AND NITRIDED OXIDES ON SILICON.
Hassan Raza, John P. Denton, Rashid Bashir, School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN.

The scaling of the gate dielectric has emerged as one of the most difficult technological challenges for the CMOS Nanotechnology, where ultra-thin oxides are expected to be gate dielectrics for the next 10-15 years. However, the traditional dielectric (SiO_2) is being sought to be replaced by next generation novel dielectric materials like Si_3N_4, Si_xO_y, Ta_2O_5, ZrO_2, HfO_2. This paper compares electrical properties of conventional dielectric SiO_2 (OX) with those of nitrided thermal SiO_2 or Si_xO_y (NOX) for use as gate dielectrics in CMOS nanotechnology. Extensive electrical characterization of MOS capacitors having ultra-thin OX and NOX (1.7-7nm) has been carried out. In the present study, ultra-thin oxides were grown on $< 100 >$ p-type silicon using thermal oxidation for 30 min at atmospheric pressure in dry oxygen at different temperatures. The oxides were then annealed in ammonia to form NOX at 950°C and 1000°C for 15 minutes. The thickness of OX was confirmed using ellipsometry and by measuring the OX step height using AFM. The thickness of NOX was measured using AFM. The electrical quality of the ultra-thin OX and NOX films fabricated by this approach were studied using MOS capacitors with an area 10^{-4} cm^2 having Aluminum as the gate material. These devices were characterized by studying their capacitance-voltage (C-V), current-voltage (I-V), tunneling, breakdown field and time-dependent breakdown characteristics (both constant voltage & constant current). The phenomenon of soft and hard breakdown was observed for both OX and NOX. It is shown that the NOX films produced by this low cost process are superior to OX in terms of low leakage current, high dielectric constant, yield statistics, and reliability issues. Finally the characterization of tunneling current through OX and NOX is presented and the Fowler-Nordheim (FN) tunneling parameters are extracted from FN plots as a function of thickness for OX and NOX.

N5.24
VUV ELLIPSOMETRY AND OPTICAL CONSTANTS OF SILICON AND SiO2. N.V. Edwards, Stefan Zollner, Darrell Roan, Motorola, Inc, Tempe, AZ; C.M. Herzinger, T.E. Tiwald, J.A. Woollam Co., Lincoln, NE.

As CMOS devices continue to scale, physical layer thicknesses decrease and simple materials (such as silicon dioxide as a gate dielectric or interlayer dielectric) are replaced by more complex materials. Variable-angle vacuum-ultraviolet spectroscopic ellipsometry (VUV SE) from 135 to 1700 nm is an essential technique to characterize ultrathin layer thicknesses and materials properties. First, extending the spectral range into the VUV is essential, since thinner layers have their first interference oscillation at shorter wavelengths. Second, complex oxides usually have a band edge in the UV, therefore measurements up to the VUV yield valuable insights. Before such studies on novel materials are possible, the optical constants of Si and SiO2 need to be determined. For this purpose, we followed the procedure in Ref. 1 and produced a series of Si wafers covered with thermal oxides of varying thicknesses (between 1 and 100 nm). Next, the ellipsometric angles from 0.7 to 9.5 eV were acquired at several angles of incidence. We optimized the accuracy of our rotating-analyzer ellipsometer by acquiring data using a computer-controlled Berek waveplate and both positive and negative polarizer settings. All experimental data were fitted using a parametric semiconductor oscillator model for Si and simple dispersion models for SiO2 (multi-sample, multi-angle, multi-wavelength analysis). With these results, we obtained the complex refractive index of Si and SiO2 up to 9.5 eV with very high accuracy. This data set now allows the study of thin oxide layers on Si and several examples from front-end and back-end CMOS processing will be shown, including complex oxides as potential gate oxides and low-k interlayer dielectrics. 1. C.M. Herzinger, B. Johs, W.A. McGahan, J.A. Woollam, and W. Paulson, J. Appl. Phys. 83, 3323, 1998.

SESSION N6: POSTER SESSION
METAL GATES AND INTEGRATION - II
Tuesday Evening, December 3, 2002
8:00 PM
Exhibition Hall D (Hynes)

N6.1
Abstract Withdrawn.

N6.2
ADVANCED PECVD-BASED ANTIREFLECTIVE COATING FOR 90NM GENERATION INTERCONNECT. Sang H. Ahn, Miguel Fung, Keebum Jung, Lei Zhu, Chris Bencher, B.H. Kim, Hichem M'Saad, Applied Materials Inc., Dielectric Systems and Module, PECVD, Santa Clara, CA.

We successfully developed a plasma-enhanced chemical vapor deposition-based nitrogen-free dielectric antireflective coating for use in 90nm interconnects in conjunction with low k materials. By choosing N-free precursors, it was possible to eliminate any adverse interactions between amine group (NH_2) and DUV 193nm photoresist in contact with an antireflective coating. Thus, photoresist poisoning-induced footing was avoided. The N-free dielectric antireflective coating demonstrated a wide tunable range of its optical properties at 193nm in a PECVD reactor: $1.6 < n < 1.9$ and $0 < k < 1.1$. This wide tunable range enables chipmakers to deposit a dual layer dielectric antireflective coating on low k dielectrics in-situ and cost-effectively in our reactor during a dual damascene process. This dual layer coating which consists of a low-absorbing layer on a high-absorbing layer can keep the substrate reflectivity below 1% across the wafer, minimizing CD swing. Its O_2-ashing resistance can be dramatically improved by an oxide capping layer. Its adhesion with BDI^{TM} is excellent. It can be etched and chemo-mechanically polished as fast as low k dielectrics.

N6.3
CHARACTERISTICS OF ULTRA SHALLOW B IMPLANTATION WITH DECABORANE. Cheng Li, Leszek Gladczuk, Marek Sosnowski, New Jersey Institute of Technology, Dept of Electrical and Computer Engineering, Newark, NJ.

The characteristics of ultra shallow B implantation with

mass-analyzed decaborane cluster ions ($B_{10}H_x^+$) are presented. Depth profiles of B and co-implanted H were measured by SIMS, before and after annealing. Annealing results in the increase in the depth of B distribution, due to diffusion, but most of H diffuses out of Si. Sputtering yield of Si by 12 keV $B_{10}H_x^+$ cluster ions was measured and found to be comparable to the estimated sputtering yield of Si with B^+ ions of the equivalent energy. AFM study showed that the relatively small $B_{10}H_x^+$ cluster ions smooth rather than roughen surfaces, similar to much larger gas cluster ions. This effect indicates a different ion-surface interaction mechanism than that of monomer ions. All other measured effects of Si implantation with $B_{10}H_x^+$ were found to be the same as those with B^+ ions of equivalent energy and dose, which confirms that decaborane implantation is an alternative to the very low energy B implantation for ultra shallow p-type junctions in Si devices.

N6.4

INFLUENCE OF SUBSTRATE TEMPERATURE DURING SPUTTER DEPOSITION ON THE SUBSEQUENT FORMATION OF TITANIUM DISILICIDE. A.S. Ozcan, K.F. Ludwig Jr., Boston University, Physics Department, Boston, MA; C. Cabral Jr., C. Lavoie, J.M.E. Harper, IBM T.J. Watson Research Center, Yorktown Heights, NY.

We demonstrate that the substrate temperature during sputtering influences the evolution of texture formation in TiSi2 thin films. Titanium films of 32 nm thickness were sputtered onto Si(001) at elevated substrate temperatures varying between 100°C and 900°C. After the depositions, in situ x-ray diffraction (XRD) measurements were performed to study the thin film reactions in real time, as the samples were annealed. The XRD results show that the substrate temperature significantly influences the texture of the initial Ti film as well as the texture of the TiSi2 film in C54 phase. The preferred Ti orientation gradually changes from (002) to (101) fiber texture as the deposition temperature increases up to 500°C. Films deposited at 600°C transformed into the C49 phase during deposition while films deposited at 700°C and higher temperatures transformed into the C54 phase during deposition. The series of deposited films was annealed up to 1000°C in He to complete the C54 phase formation while monitoring the texture evolution, in situ, using a position sensitive x-ray detector. The XRD results show that the final C54 phase texture changes from a dominant (311) orientation normal to the substrate to a (010) orientation for substrate temperatures between 600°C and 700°C. The C49-C54 phase transformation temperature is also lowered for these deposition temperatures. Ex situ pole figure analysis of the film deposited at 700°C confirms the dominant C54 (010) texture and shows an in-plane orientation with C54 [001] || Si [-110]. Interestingly, for substrate temperatures 800°C and 900°C, the C54 texture changes back to a dominant (311) orientation. Ex situ XRD measurements show that these films have the same in-plane texture, as do the C54 films obtained from Ti deposited at room temperature.

N6.5

LAMP ILLUMINATION IN RAPID THERMAL ANNEALING OF IMPLANTED DOPANTS IN Si. A.T. Fiory, New Jersey Institute of Technology, Newark, NJ; A. Agarwal and A. Stevenson, Axcelis Technologies, Beverly, MA.

Effects of incandescent-lamp radiation (E $\sim$ 1.4 eV) were studied for the electrical activation of shallow ion-implants of ^{11}B, BF_2, P, and As species in silicon by rapid thermal annealing (RTA). 200-mm wafers were annealed in an RTA chamber that heats wafers from both sides with quartz-halogen lamps. The blanket-implanted test wafers were supported by a heavily-boron-doped holder wafer. The top surfaces of the test wafers were exposed to lamp radiation while the bottom surfaces were shielded by the holder wafer. Wafers were annealed in pairs, oriented with implanted side either up or down, for each RTA recipe: 10-s anneals from 1000 to 1075°C. Differences in sheet resistance (Rs) between members of the wafer pairs ranged from 4 to 60%. N-type dopants yield higher Rs when the implanted side is exposed to the lamps, as though the effective temperature were reduced by 5 to 10°C. P-type dopants yield lower Rs when the implanted side is exposed to the lamps, as though the effective temperature were increased by 5 to 50°C. Differences larger than 5°C are believed to be greater than the uncertainty in temperature control for the experiment.

N6.6

LOW THERMAL BUDGET NiSi FILMS ON SiGe ALLOYS. S.K. Ray, T.N. Adam, C.P. Swann and J. Kolodzey, Dept of Electrical and Computer Engineering, University of Delaware, Newark, DE; G.S. Kar, Dept of Physics, IIT Kharagpur, INDIA.

Group-IV heterostructures based on strained SiGe have become increasingly attractive for high-performance silicon HBT, CMOS, and infrared detector devices. A suitable metal silicide with a low silicidation temperature and Si consumption ratio is essential for processing SiGe ultra-shallow junction devices. In this paper, we present the fabrication and characterization of nickel silicide with a lower formation temperature and silicon consumption ratio compared to titanium and cobalt silicide. NiSi was formed on Si (100) substrates and CVD grown Si0.9Ge0.1/Si layers by the rapid thermal annealing of evaporated Ni films. The phase formation and microstructure of binary silicide and ternary nickel germano-silicide at different annealing conditions were studied using x-ray diffraction, RBS, XPS, and AFM. Electrical properties of the grown silicides were characterized by four-probe resistivity and contact resistance measurements. Although NiSi was found to form at annealing temperatures as low as 400°C, the complete transformation to the low-resistivity NiSi phase only occurred at 600°C. Annealing at higher temperatures resulted in a Si-rich high-resistivity NiSi2 phase. RBS simulations revealed the formation of a ternary nickel germano-silicide phase for the SiGe alloy. A shift of the binding energy of Ge 2p electrons in XPS spectra confirmed the incorporation of Ge into the silicide. AFM analysis of the films as a function of annealing temperature showed a slower grain growth in the Ge-incorporated layer as compared to the binary silicide, resulting in a higher temperature window for the monosilicide phase. This was confirmed by sheet resistivity measurements, where the low-resistivity temperature window was found to be higher for germano-silicides. Sheet and contact resistivities as low as 12-15 $\mu\Omega$-cm and 17.5 $\mu\Omega$.cm2, respectively, were obtained for the silicides. We conclude that a low-resistivity nickel silicide suitable for advanced Si heterostructure devices could be formed on SiGe alloys by rapid thermal annealing.

N6.7

FORMATION OF NICKEL SILICIDE ON Si AND RELATED SUBSTRATES. Ramesh Nath, Mark Yeadon, IMRE, Singapore, SINGAPORE and Dept of Materials Science, National University of Singapore, SINGAPORE; Dongzhi Chi and Michael Loomans, IMRE, SINGAPORE.

We have investigated the early stages of the nucleation and growth of nickel silicide on silicon and related surfaces for advanced CMOS device applications. NiSi is an advantageous silicide for source, drain and gate contacts due to its lower consumption of silicon, and ability to maintain low resistivity even for line-widths down to 0.1um. The transformation of NiSi into the high resistivity disilicide (NiSi2), as well as its agglomeration at elevated temperatures could limit its usefulness in the silicidation process, however. In this paper we present the results of an in-situ investigation of the nucleation, growth and ultimate agglomeration of nickel silicide thin films on Si and related surfaces. In our experiments, nickel layers were deposited by electron beam evaporation in the polepiece of an ultrahigh vacuum transmission electron microscope. The samples were then annealed at elevated temperatures. Microstructural evolution was monitored by transmission electron diffraction and microscopy.

N6.8

ULTRASHALLOW SIMS STUDY OF IMPLANTED DOPANTS IN NiSi/Si(100). Nikolai Yakovlev, Andrew Wong, Doreen Lai, Dongzhi Chi, Institute of Materials Research and Engineering, NUS, Singapore, SINGAPORE.

Nickel monosilicide (NiSi) is an attractive material for local contacts in silicon based electronic devices due to its low resistivity which is maintained even for line width down to 100 nm and due to lower consumption of silicon and smoother silicide/Si interface with respect to $TiSi_2$ and $CoSi_2$. However in contrast to those, NiSi has lower thermal stability; above 700°C, it agglomerates, i.e. the silicide layer becomes not continuous. In this work, we studied nickel silicide layers obtained by annealing of metal Ni layers on substrates implanted with B^+ or BF_2^+. As observed using scanning electron microscopy, after annealing at 700°C, agglomeration of the silicide occurs on B^+ implanted substrate and on a substrate without implantation. If BF_2^+ was implanted, NiSi layer remains continuous after annealing at the same temperature. This leads to the conclusion that the fluorine is responsible for the stability of the silicide film. Distributions of elements through the depth of the films were measured using time-of-flight secondary ion mass spectrometry. After annealing of Ni layer on the implanted substrate, most part of B remains in Si, maximum of B concentration is at the interface between NiSi and Si. The process pushing B out of the growing silicide can be enhanced diffusivity due to injection of vacancies during the reaction at the NiSi/Si interface. The distribution of fluorine is considerably different, here the maximum of F concentration is inside NiSi layer. Most likely, it is situated at grain boundaries, saturates dangling bonds and decreases the boundary energy. This changes the balance between the boundary and interface energies in favour of a stable NiSi layer, according to the model from ref [1]. [1] T.P.Nolan, R.Sinclair and R.Beyers, J.Appl.Phys. 71, 720 (1992).

N6.9

GROWTH TEMPERATURE EFFECTS ON DEEP-LEVELS IN Si

GROWN BY LOW-TEMPERATURE MOLECULAR BEAM EPITAXY. Sung-Yong Chung, Department of Electrical Engineering, The Ohio State University, Columbus, OH; Paul R. Berger, Department of Electrical Engineering, Department of Physics, The Ohio State University, Columbus, OH; Z.-Q. Fang, University Research Center, Wright State University, Dayton, OH; Phillip E. Thompson, Naval Research Laboratory, Washington, DC.

As the International Technology Roadmap for Semiconductors (ITRS) drives CMOS technology forward, the addition of resonant interband tunneling diodes (RITD) offers a new paradigm of computing capitalizing upon transistor/tunnel diode integration. Si-based RITDs, discussed here, utilize δ-doping and low temperature molecular beam epitaxy (LT-MBE). LT-MBE offers the opportunity to realize the high sheet carrier concentrations needed for an interband tunnel diode, but concurrently creates defects, mostly point defects, that lead to an elevated valley current. This leads to a suppressed peak-to-valley current ratio (PVCR) for the RITD. This study examines these defects in an effort to identify their origin. Deep-level transient spectroscopy (DLTS) measurements were performed on Si:Sb and Si:B n+-p step junction diodes grown by LT-MBE at various growth temperatures. The population of electron and hole traps showed strong dependence on the substrate growth temperature. The trap density dependence on growth temperature decreases with increasing temperature. However, segregation and diffusion increase with increasing temperature. Thus, an optimal temperature is sought for enhanced PVCR. No post-growth annealing process has been added for this DLTS study. Electron traps, identified by E1 (0.42-0.45eV) and E2 (0.225eV), were found in Sb-doped layers at a low growth temperature of 320 $^\circ$C and hole traps, identified by H1 (0.38-0.41eV), were found in B-doped layer grown at 370 $^\circ$C, 420 $^\circ$C, 500 $^\circ$C, and 600 $^\circ$C. These traps have been identified by their capture cross-section and trap density. Due to low concentration of impurities in the MBE grown samples, the dominating defects in our samples are expected to be of an intrinsic and/or antimony-related origin. The origins of the identified deep levels are hypothesized as the association of dopants with vacancy defects, E1 level for vacancy-antimony (V-Sb) and V(0/-)pair and E2 level for V(-2/-). The defects are created by reduced adatom mobility on the surface due to the low growth temperatures employed and the localized strain stemming from the differences of atomic radii of Si and the substitutional dopants.

N6.10
CONTROL OF GROWTH MORPHOLOGY IN SELECTIVE EPITAXIAL GROWTH OF Si AND SiGe FOR SELF-ALIGNED CONTACT PAD FORMATION BY UHV-CVD. S.H. Lim, S. Song, T. Park, G.D. Lee, J. Lee[a], E. Yoon, B.C. Lee[b], and S. Choi[b], School of Materials Science and Engineering, Seoul National University, Seoul, KOREA; [a]School of Electrical Engineering and Computer Science, Kyungpook National University, Taegu, KOREA; [b]Semiconductor R&D Center, Samsung Electronics Co. Ltd., Kyunggi-Do, KOREA.

Recently, the Self-Aligned Contact (SAC) technology using low temperature Selective Epitaxial Growth (SEG) is proposed to reduce the aspect ratio of the capacitor contact hole and to retain alignment margins between a contact hole and a contact pad in a giga-bit DRAM cell [1]. In order to apply SEG to contact pad formation, the control of isotropic or anisotropic growth is essential to prevent short circuit between adjacent pads on the field oxide due to lateral overgrowth. However, there were few experimental or theoretical reports on this issue in submicrometer pattern size. In this work, we investigated isotropic/ anisotropic growth and facet evolution of the Si and SiGe SEG at various growth conditions and pattern sizes. Si and SiGe epitaxial layers were selectively grown on oxide patterned Si substrates by cold-wall type UHV-CVD system. In the kinetically limited growth condition, lateral growth behaviors of crystalline Si over field oxide were observed. By the Ge addition in Si epitaxial layer, lateral overgrowth was suppressed, but facet development was enhanced. Ge content and profile were adjusted to control growth morphology for contact pad formation. Theoretical analysis considering both surface migration and total free energy, and comparison with the experiment were performed. [1] H. Koga et al, IEDM Tech. Dig., p.25 (1997).

N6.11
COPPER DIFFUSION CHARACTERISTICS IN SINGLE CRYSTAL AND POLYCRYSTALLINE TaN. H. Wang, Ashutosh Tiwari, X. Zhang, A. Kvit, and J. Narayan, Department of Materials Science and Engineering, North Carolina State University, Raleigh, NC.

TaN has become a very promising diffusion barrier material for Cu interconnection, because of the high thermal stability requirement and thickness limitation for next generation ULSI devices. Due to the complexities of TaN phases, Cu diffusion characteristics vary with different phases and microstructures. We have investigated diffusivity of copper in single-crystal (NaCl-structured) and polycrystalline TaN thin films grown by pulsed laser deposition. The polycrystalline TaN films were grown directly on Si(100), while single crystal films were grown with TiN buffer layers. Both poly and single-crystal films with Cu overlayers were annealed at 500°C, 600°C, 650°C, and 700°C in vacuum to study the copper diffusion characteristics. The diffusion of copper into TaN was studied using STEM-Z contrast, where the contrast is proportional to Z^2C (atomic number), and TEM. The diffusion distances (2) are found to be about 5nm at 650°C for 30 min annealing. The diffusivity of Cu into single crystal TaN follows the relation $cm^2\ s^{-1}$ in the temperature range of 600°C to 700°C. We observe that Cu diffusion in polycrystalline TaN thin films is nonuniform with enhanced diffusivities along the grain boundary.

SESSION N7/T5: JOINT SESSION
THEORY AND MODELING
Chairs: Susanne Stemmer and Darrell G. Schlom
Wednesday Morning, December 4, 2002
Room 202 (Hynes)

8:30 AM *N7.1/T5.1
FIRST PRINCIPLES MODELING OF HIGH-K DIELECTRIC MATERIALS. Gyuchang Jun[a] and Kyeongjae Cho[b], Stanford University; [a]Dept of Materials Science and Engineering, [b]Dept of Mechanical Engineering; Stanford, CA.

First-principles calculations are performed for high-K gate dielectric materials for bulk and interface systems. Detailed electronic structures and atomic configurations are investigated for transition metal (Hf and Zr) oxide, metal doped silicate bulk system and a model Si-silicate interface system. Metal atom-interface interactions are elucidated, and this finding sheds a light on recent experimental observations of intermediate silica layer formation. Pseudo polymorphs of metal oxides are investigated to elucidate basic driving forces in microscopic configurations of metal oxide and silicate in amorphous structure. We studied energetic and electronic structure of metal oxide pseudo morph with varying oxygen coordinations. Dielectric constants of metal oxide and silicate materials are also investigated using the density functional perturbation theory method implemented in ABINIT code. We will discuss on recent progresses of the high-k gate dielectric materials simulations.

9:00 AM N7.2/T5.2
FIRST-PRINCIPLES STUDY OF STRUCTURAL AND DIELECTRIC PROPERTIES OF ZrO_2 and HfO_2. Xinyuan Zhao, David Vanderbilt, Rutgers University, Department of Physics and Astronomy, Piscataway, NJ.

High-K metal oxide dielectrics have recently been the focus of substantial ongoing efforts directed toward finding a replacement for SiO_2 as the gate dielectrics in complementary metal-oxide-semiconductor (CMOS) devices. ZrO_2, HfO_2 and their structure-modified derivatives show great promise for this purpose. We study the structural and vibrational properties of the three low-pressure (cubic, tetragonal, and especially monoclinic) crystalline phases of ZrO_2 and HfO_2, with special attention to the computation of zone-centered phonon modes and the related dielectric properties. The calculations are carried out within the density-functional theory (DFT) using ultrasoft pseudopotentials and a plane-wave basis. Our results show that the dielectric responses are strongly phase-dependent, and the monoclinic phase of ZrO_2 (or HfO_2) has a strongly anisotropic dielectric tensor and a rather small orientationally averaged dielectric constant (approximately 20 and 18 for ZrO_2 and HfO_2, respectively) compared to the values for the tetragonal and cubic phases, because the softest infrared-active phonon modes have weak oscillator strengths. Realistic models of amorphous ZrO_2 are then realized using *ab-initio* molecular dynamics in a "melt-and-quench" fashion. The resulting amorphous ZrO_2 structures are analyzed in order to understand their local bonding geometry and other structural properties, and then used as inputs for a first-principles investigation of the vibrational and dielectric properties of the amorphous ZrO_2 systems.

9:15 AM N7.3/T5.3
EVALUATION OF CRYSTALLINE GATE OXIDES FOR Si MICROELECTRONICS: BAND OFFSETS, ENERGETICS, AND DIELECTRIC PROPERTIES OF Si/BaO, Si/HfO2, and Si/ZrO2 (001) INTERFACES. Gianluca Gulleri and Vincenzo Fiorentini, INFM and Dipartimento di Fisica, Università di Cagliari, ITALY.

The performance needs of modern information technology push Si-based ULSI devices towards nanometric dimensions, mainly because of the need for increasing the capacitance in MOS transistors and capacitors. The main bottleneck is that of gate oxide layers. Larger capacitance means ever smaller thicknesses, and silica, the natural oxide in this context, is already near its very limit down to 2

unit cells in thickness. The selection criteria for a replacement oxide for silica in ULSI Si circuitry are i) larger dielectric constant, ii) interface band offsets to Si as large as, or not much worse than, those of silica, and iii) epitaxy on Si energetically not too costly. We studied the structure, energetics and band offsets of the (100) interfaces of Si with BaO, HfO2, and ZrO2 through first-principles gradient-density-functional calculations, using the VASP code. HfO2/Si and ZrO2/Si are terminated through a mixed Si-metal and a 50% vacant oxygen layer in O-poor conditions, as predicted also by ab initio surface dynamics, and by a plain Si-O interface in O-rich conditions. The valence and conduction band offsets for the favored interfaces are respectively 2.0 eV and 1.9 eV for BaO/Si, 4.1 eV and 0.3 eV for HfO2/Si, 3.9 eV and 0.8 eV for ZrO2/Si, using experimental gap values, and including estimated many body corrections to the bulk bands. We also estimated the static dielectric constant of HfO2, ZrO2, and BaO to be 33 (cubic bulk) and ~17 (Si-epi), 34 (cubic bulk), and 8 (Si-epi) respectively. Despite these high dielectric constant values, these materials may have limited use because of their small injection barriers for electrons. Our search for better candidate oxides continues, on yttrium, lanthanum, ytterbium, and lutetium sesquioxides (X2O3). Work supported by the UE (INVEST project) and by INFM through the Parallel Supercomputing Initiative.

9:30 AM *N7.4/T5.4

ELECTRON MOBILITY IN Si INVERSION LAYERS IN MOS SYSTEMS WITH A HIGH-K INSULATOR: THE ROLE OF REMOTE-PHONON SCATTERING. Massimo V. Fischetti, Deborah A. Neumayer, and Eduard A. Cartier, IBM Semiconductor Research and Development Center (SRDC), IBM Research Division, Thomas J. Watson Research Center, Yorktown Heights, NY.

The high dielectric constant of insulators currently investigated as alternatives to SiO_2 in metal-oxide-semiconductor structures is due to their large ionic polarizability. This is usually accompanied by the presence of soft optical phonons. We show that the long-range dipole field associated with the interface excitations resulting from these modes and from their coupling with surface plasmons, while small in the case of SiO_2, for most high-κ materials causes a reduction of the effective electron mobility in the inversion layer of the Si substrate. We study the dispersion of the interfacial coupled phonon-plasmon modes, their electron-scattering strength, and their effect on the electron mobility for Si-gate structures employing films of SiO_2, Al_2O_3, AlN, ZrO_2, HfO_2, and $ZrSiO_4$ for 'SiO_2-equivalent' thicknesses ranging from 5 nm to 0.5 nm. Material parameters (especially phonon energies and oscillator strengths) are obtained from the literature or by performing FTIR spectroscopy on some these films. We find that the effective electron mobility is severely depressed in systems employing the insulators with the highest κ (namely, ZrO_2 and HfO_2), while nitrides and oxy-silicates still yield satisfactory mobilities, especially for films thin enough to benefit from dielectric screening from the electrons in the polycristalline Si gate. Finally, we show that the electron mobility increases with the increasing thickness of the interfacial oxide layer often present - intentionally or not - in these gate stacks.

10:30 AM *N7.5/T5.5

ATOMIC STRUCTURE, BAND OFFSET ENGINEERING AND HYDROGEN AT HIGH-k OXIDE: Si INTERFACES. John Robertson, Paul W. Peacock, Engineering Dept, Cambridge University, Cambridge, UNITED KINGDOM.

High dielectric constant oxides are needed to replace silicon dioxide as the gate oxide in future CMOS devices. Band offsets should exceed 1V to inhibit leakage currents [1]. Epitaxial interfaces between metal oxides and Si are more complicated that those between III-V semiconductors or NiSi2:Si as the bonding changes from covalent to ionic, and various bonding configurations are possible. The interfaces must satisfy various conditions for good electrical quality; it should be non-polar and have no partially filled Si dangling bond states, as these produce gap states. Atomic models of possible interfaces between Si:ZrO2(100), Si:ZrO2(111), Si:SrO(100), Si:SrTiO3(100) have been made. SrTiO3(100) consists of non-polar SrO and TiO2 layers and so it has a non-polar surface. Nevertheless, the first SrO layer should have a Sr0.5O stoichiometry, as half of the oxygens are terminating Si as Si-O anion groups. The ZrO2(100) surface is polar, but can be made non-polar by change of stoichiometry. Models of Si:ZrO2(100) are made with both Zr-Si and Zr-O bonded interfaces. Si dangling bonds are terminated by oxygen bonds or covalent Zr-Si interaction. Non-polar interfaces can still possess dipole layers. This allows band offsets to be changed by 0.1-0.5V from offsets set by bulk charge neutrality levels. A second problem is that high K:Si interfaces can suffer from a large fixed charge. This is a critical factor which could limit their performance [3]. It could arise from native defects such as vacancies or from hydrogen which is ubiquitous in processing. The fixed charge is generally positive in most candidate oxides, except in Al2O3 in which it is negative. The charge states of hydrogen in the perfect lattices of many oxides has been calculated. The oxides fall into two classes. In most oxides such as ZrO2, TiO2, SrTiO3 or ZnO the hydrogen is only stable as the positive charged state (proton), whereas in the wide gap oxides SiO2 and Al2O3 the negative and neutral state is also possible for higher Fermi level positions. This suggests that hydrogen is a likely cause of the fixed charge in the high K oxides as it naturally accounts for the sign change. [1] R A McKee, F J Walker, M F Chisholm, Phys Rev Lett 81 3014 (1998) [2] J Robertson, J Vac Sci Technol B 18 1785 (2000) [3] eg, S Guha et al, in MRS Bulletin special issue on high K oxides (March 2002)

11:00 AM N7.6/T5.6

OXYGEN VACANCY DEFECTS IN TANTALUM PENTOXIDE: A DENSITY FUNCTIONAL STUDY. R. Ramprasad, Motorola, Inc., Tempe, AZ; M. Sadd, D.R. Roberts, Motorola, Inc., Austin, TX; T.P. Remmel, Motorola, Inc., Tempe, AZ; M.V. Raymond, E.D. Luckowski, S. Kalpat, C.C. Barron, Motorola, Inc., Austin, TX; M. Miller, Motorola, Inc., Tempe, AZ.

Although tantalum pentoxide (Ta_2O_5) has been studied, both experimentally and theoretically, over the past three decades, its real emergence as a dielectric material that can be integrated with conventional CMOS has happened only in the last decade. While interest in high dielectric constant materials, in general, is primarily due to a need to scale down device sizes, the renewed interest in Ta_2O_5 is due to the ability to deposit it using conventional methods compatible with equipment and processes already available in the semiconductor industry. Nevertheless, concerns exist with Ta_2O_5 (and other alternative dielectric materials), one of them being defect densities, and their impact on the leakage currents (via defect or trap levels created in the band gap of the dielectric). The present work attempts to theoretically characterize oxygen vacancy defects in Ta_2O_5. The atomistic structure of Ta_2O_5 was chosen so that it is computationally tractable, while at the same time is representative of deposited films. Several types of O vacancies with qualitatively different types of coordination environments were considered within this model, and the defect or trap levels due to these defects were determined using total energy calculations. Correlations between the coordination environment and the location of the defect levels will be drawn. The stability of variously charged vacancies was also considered, as a function of the vacancy type and the local chemical potential. All calculations to be presented were performed using the density functional theory, within the local density approximation, and ultrasoft pseudopotentials.

11:15 AM N7.7/T5.7

PROGRESS IN THE CHARACTERIZATION OF LAYERED HIGH-K DIELECTRICS AS TUNNEL BARRIERS IN SILICON-BASED NONVOLATILE MEMORIES. Julie D. Casperson, Harry A. Atwater, California Institute of Technology, Watson Laboratory of Applied Physics, Pasadena, CA; L. Douglas Bell, Jet Propulsion Laboratory, Pasadena, CA; Brett W. Busch, Mun Yee Ho, Martin L. Green, Agere Systems, Murray Hill, NJ.

We have modeled and fabricated the layered dielectric barrier structures that address the main performance limitations of floating gate nonvolatile memory devices, such as flash memories and nanocrystal memories, namely the long program time ($\sim 1\ \mu$s) and erase time ($\sim$ 1 ms) achievable via a Fowler-Nordheim tunneling mechanism for charging of the floating gate through a homogeneous tunnel barrier. Silicon compatible layered barrier heterostructures that enable a large drop in the barrier height with applied voltage are an alternative to homogeneous dielectric films as the tunnel barriers for nonvolatile memories. Using a numerical effective-mass model, we have been able to optimize and analyze possible layered structures with real materials parameters. Based on literature values for conduction band offsets, we find from simulation that some of the most promising structures for layered tunnel barriers consist of Al_2O_3 with Si_3N_4 or HfO_2 and we have fabricated such structures. The Si_3N_4 was made by low-pressure chemical vapor deposition, while the Al_2O_3 and HfO_2 were made by atomic layer deposition. We have fabricated the layered barrier structures Si_3N_4 / Al_2O_3 / Si_3N_4 and HfO_2 / Al_2O_3 / HfO_2 as well as single- and double-layered structures using these materials. One of the important results is in the comparison of the I-V characteristics of n-Si / Si_3N_4 / Al_2O_3 / Si_3N_4 and n-Si / Si_3N_4 / Al_2O_3. We find significant asymmetry in the two-layer measurement, the first indication of barrier lowering in a Si-based layered tunneling barrier structure. Internal photoemission experiments will also be discussed as a direct measure of the conduction band offsets of these materials. These measurements give us a better understanding of the electrical properties of the heterostructures.

11:30 AM *N7.8/T5.8

OXIDES AND SILICATES OF HAFNIUM AND ZIRCONIUM AS ALTERNATIVE GATE DIELECTRICS; DENSITY FUNCTIONAL THEORY STUDY. Maciej Gutowski, John Jaffe, Pacific Northwest

National Laboratory, Environmental Molecular Sciences Laboratory, Theory, Modeling & Simulation, Richland, WA.

It is known that the chemistries of hafnium and zirconium are more nearly identical than for any other two congeneric elements. Thus, both zirconia and hafnia, with the dielectric constant K of ca. 21, have emerged as potential replacements for silica (K = 3.9) as a gate dielectric. We have recently found that there is an important difference between the zirconia/Si and hafnia/Si interfaces. The former was found to be unstable with respect to formation of silicides whereas the latter is stable. This surprising difference prompted us to study differences between oxides, silicides, and silicates of hafnium and zirconium. The calculations were performed in the framework of density functional theory with the Perdew-Wang 91 exchange-correlation functional. The ionic compounds were found to be more stable for hafnium than for zirconium with the heats of formation of oxides and silicates being larger by ca. 0.5 eV for hafnium. The higher ionicity of hafnium compounds is also reflected by the band gaps that are larger by 0.5 (oxides) and 0.9 (silicates) eV for hafnium than for zirconium. Unfortunately, some problems still exist with HfO_2 as an alternative gate dielectric. The MeO_2 (Me=Zr, Hf) films become polycrystalline either during growth or after only moderate post-deposition anneals. Mixed metal oxides $MeSi_xO_y$ are anticipated to provide a reasonable compromise between the value of the dielectric constant and the quality of the Si/dielectric interface. Our density functional theory results for the $Me_xSi_{1-x}O_2$ silicate-type materials will be discussed.

SESSION N8/T6: JOINT SESSION
CRYSTALLINE OXIDES FOR GATE DIELECTRICS
Chairs: John Robertson and Rodney A. McKee
Wednesday Afternoon, December 4, 2002
Room 202 (Hynes)

1:30 PM *N8.1/T6.1
HIGH κ GATE DIELECTRICS FOR Si AND COMPOUND SEMICONDUCTORS BY MBE. J. Raynien Kwo, and Minghwei Hong, Agere Systems, Murray Hill, NJ.

Nanoscale device technology is driving intense study of thin dielectric layers on semiconductors. The aggressive scaling of Si CMOS technology calls for identifying high κ dielectrics to replace SiO_2 and oxynitrides in gate related applications. The material requirements for the alternative gate dielectric are very challenging in order to achieve performance comparable to SiO_2. Furthermore, there are demanding issues for process integration compatibility, such as morphology, interfacial structure and reaction, thermal stability, and gate compatibility. Our discovery of a mixed oxide $Ga_{1-x}Gd_xO_3$ (κ=12) and a pure oxide of Gd_2O_3 (κ=14) as low D_{it} oxides for effective compound semiconductor passivation has led to the investigations of rare earth oxides Gd_2O_3 and Y_2O_3 (κ=18) dielectrics as the alternative gate dielectrics replacing SiO_2 in CMOS scaling. Unlike most other work reported, our approach of ultrahigh vacuum deposition from an oxide source demonstrated the absence of SiO_2 or silicate common at the dielectric/Si interface, thus giving a significant thickness saving for the overall dielectric layer. Although the MBE technique is not yet a proven technology for the CMOS manufacture, these amorphous-Si/Gd_2O_3 /crystalline-Si and a-Si/Y_2O_3/c-Si gate stacks of abrupt interfaces and controlled microstructures served as a model system to elucidate critical integration issues. While we show significant progresses have been made in addressing all these issues, more efforts are still needed in order to reach the goal of satisfactory replacement of the gate dielectric. Understanding of the electronic structure and optimization of the electrical properties of the bulk of the dielectric and the dielectric/Si interface are essential to future integration of these new materials into CMOS processing. Work done in collaboration with B. Busch, D.A. Muller, Y.J. Chabal, A.R. Kortan, J.P. Mannaerts, A.M. Sergent, B. Yang, P. Ye, H.J. Gossmann, K. Ng, J.D. Bude, W.H. Schulte, E. Garfunkel, and T. Gustafsson.

2:00 PM *N8.2/T6.2
ULTRATHIN METAL OXIDES ON SILICON AS HIGH-k MATERIAL FOR GATE DIELECTRIC APPLICATIONS. Evgeni Gusev, Doug Buchanan, Alesandro Callegari, Eduard Cartier, Matt Copel, Mike Gribelyuk, Supratik Guha and Harald Okorn-Schmidt, IBM Semiconductor Research and Development Center, T.J. Watson Research Center, Yorktown Heights, NY.

As ULSI dimensions continue to shrink at a phenomenal pace, novel materials are required for deep sub-micron high-performance logic and memory devices. This is especially true for gate dielectric, the heart of MOSFETs. The equivalent thickness of the gate dielectric is already on the order of 2 nm (and thinner) and is projected to be close to 1 nm soon. Direct tunneling currents, reliability, boron penetration from poly-Si gate, mobility degradation, and other fundamental issues are of a serious concern for such ultrathin oxides. In the presentation, we will give an overview of binary metal oxides (such as HfO2, ZrO2, Al2O3, Y2O3) and their silicates and aluminates deposited on silicon by atomic layer deposition, chemical vapor deposition and molecular beam deposition techniques. The materials issues of microstructure, crystallization behavior, thermal stability, dopant and oxygen diffusion, reactivity and interface engineering and their correlation with electrical properties will be addressed.

2:30 PM N8.3/T6.3
CORRELATION OF THE PHYSICAL CHARACTERIZATION WITH THE ELECTRICAL PERFORMANCE OF HAFNIUM SILICATE THIN FILMS. P.S. Lysaght, G. Bersuker, B. Foran, L. Larson, R.W. Murto and H.R. Huff, International SEMATECH, Austin, TX.

One high-k dielectric material of interest, hafnium silicate, has been investigated as a candidate for replacement of conventional SiO2 as the transistor gate insulator layer due to continuous aggressive device scaling. Hafnium silicate films, (HfO2)x+(SiO2)1- x, (of 4.0 nm physical thickness) with various ratios of HfO2: SiO2 (80 and 90 mol.% HfO2) have been deposited on HF-last pre-cleaned 200 mm diameter wafers by MOCVD. Blanket, uncapped films have been annealed at atmospheric pressure in nitrogen ambient over a range of RTA temperatures up to 1000°C for 10 seconds. These films have been characterized by plan view HRTEM and an estimate has been achieved for the volume fraction of crystallinity as a function of temperature for each composition of HfO2-silicate. Samples from the same set of deposited films have been capped with 20 nm of TiN (electrode), annealed by the same RTA processes as the blanket films, etched into capacitor structures and evaluated for electrical performance with CV-IV measurements. The degree of crystalline order in each HfO2-silicate sample set has been directly correlated with capacitor leakage current. Additionally, the onset temperature of crystallization of each film has been estimated as well as the film permittivity and the equivalent oxide thickness, EOT. Measurements designed to evaluate the electrical current pathways associated with grain structures will also be discussed.

3:15 PM *N8.4/T6.4
INTERFACE AND MATERIALS PROPERTIES OF HIGH-K GATE STRUCTURES. S. Sayan, W.H. Schulte, R.A. Bartynski, T. Nishimuri, D. Starodub, M. Croft, X. Zhao, D. Vanderbilt, T. Gustafsson and E. Garfunkel, Departments of Chemistry and Physics, and Laboratory for Surface Modification, Rutgers University, Piscataway, NJ.

In this work we describe recent results using soft x-ray photoemission (SXPS), inverse photoemission (IPE), medium energy ion scattering (MEIS), x-ray absorption spectroscopy (XAS), electron microscopy (TEM) and electrical methods to examine ZrO2 and HfO2 gate dielectrics and their interfaces with silicon and metal layers. In selecting an alternative (to SiO2) gate insulators, many parameters in addition to dielectric constant and thermal stability must be considered, including the barrier heights for tunneling. The SXPS and IPE results are used to determine the densities of states above and below the Fermi energy, in particular to elicit useful information on barrier heights. We find that the densities of states at the band edges (in particular band tail states) make the assignment of a simple threshold voltage somewhat problematic. We have also performed first-principles density functional calculations to study the properties of cubic, tetragonal, and monoclinic phases of HfO2 and ZrO2. The densities of valence and conduction bands are calculated and compared to various experimental measurements. The thickness, layered structure, and crystal phase of the as-deposited and annealed films have been studied by XRD, XAS, MEIS and TEM indicating that films are predominantly monoclinic. Critical electrical and materials behavior occurs during post-processing at elevated temperature. We present new results on interface and oxide film stability for several film compositions and structures at elevated temperature (~1000°C). We show under what conditions excess SiO2 is formed at the interface during post-processing, reducing the interface electrical defect concentration but lowering the overall capacitance. We also discuss the decomposition of the films by SiO desorption in reducing environments. The authors would like to acknowledge useful interactions with colleagues at Agere Systems (B. Busch, G. Wilk, and M. Green), IBM (E. Gusev, M. Copel and D. Buchanan), IMEC (W. Tsai) and NCSU (J.P. Maria, G. Parsons, G. Lucovsky and A. Kingon). We also acknowledge the SRC for financial support.

3:45 PM N8.5/T6.5
EPITAXIAL Pr_2O_3 ON SILICON AS AN ALTERNATIVE GATE OXIDE FOR FUTURE CMOS APPLICATIONS. Sebastian Gottschalk, Horst Hahn, Darmstadt University of Technology,

Institute of Materials Science, Thin Films Division, Darmstadt, GERMANY.

Alternative high-k gate oxides are of great technical interest for advanced CMOS structures. The common approach for new gate materials included so far mostly amorphous binary oxides and silicates. Amorphous structures inhibit the danger of crystallization under working conditions and post-preparation-processing steps. This leads to significant electrical degradation mechanisms because of newly introduced tunnel pathways in the form of grain boundaries. In this work the feasibility of epitaxial growth of Pr_2O_3, an oxide with $k_{bulk} \approx 30$ was demonstrated. Due to very small lattice mismatch the as prepared films facilitate the defect free overgrowth of silicon in semiconductor quality. This feature is very promising for 3 dimensional CMOS structure and SOI (silicon on insulator) designs. Growth of Pr_2O_3 films on p- and n-doped Si (111) substrates was performed in an MBE system. Structural and chemical investigations were performed using XRD, XPS, AFM and TEM. The overgrowth of Si on the deposited films has been shown successfully. Multilayer Si/Pr_2O_3 systems appear to suffer from increased defect concentration in forms of twin boundaries and dislocations with increasing film thickness. Determination of the dielectric constant of as prepared films indicate values comparable to reported bulk values. However interface characterization indicates the existence of Pr-Si-O at the interface region. Supposedly a Pr-silicate is formed at elevated growth temperatures. First results using metallic Pr and atomic oxygen with low kinetic energy from an hyperthermal oxygen source to prepare Pr_2O_3 films will be presented.

4:00 PM N8.6/T6.6

DYNAMIC GROWTH MECHANISM AND INTERFACE STRUCTURE OF CRYSTALLINE ZIRCONIA ON SILICON. S.J. Wang, A.C.H. Huan, Institute of Materials Research & Engineering, SINGAPORE; C.K. Ong, Department of Physics, National University of Singapore, SINGAPORE.

Crystalline oxides on semiconductors, maintaining one-to-one atomic correspondence at the oxide/semiconductors interface, are expected to have excellent physical properties and chemical stability for a variety of potential applications, including gate dielectric, lattice matched Si-oxide-based heterostructures for ferroelectric, piezoelectric, ultrathin silicon-on-insulator or germanium-on-insulator technology, and the potential insulators for GaAs-based microelectronics. However, the issue concerning the dynamic growth process and interface structure of crystalline oxide on semiconductors is a very crucial step for the implementation of this new structure. In this report, we have studied the initial stage of the growth of crystalline yttria-stabilized zirconia (YSZ) films on the natively oxidized Si (100) wafer by pulsed-laser deposition. X-ray photoelectron spectroscopy (XPS) and high-resolution electron microscopy (HREM) show that, for the first few monolayers of crystalline YSZ deposited on Si (100), the dynamic processes appear to be the decomposition of SiO_2 to SiO, the formation of epitaxial ZrO_2, and the desorption of SiO. The native amorphous silicon oxide layer is removed completely with the continued deposition of YSZ and the oxygen in this layer is used as oxygen source for forming stable crystalline oxide film. XPS depth profile and HREM investigation showed that the interface of crystalline YSZ film in contact with silicon was atomically sharp and was commensurately crystallized without an amorphous layer. The interface structure is suggested to have a sequence of -Si-O-Zr-O-. For the film with electrical equivalent oxide thickness 1.46 nm, the leakage current is about four orders lower than that of silicon dixode at 1 V bias voltage. The hysteresis and interface state density in this film are measured to be less than 10 mV and 2×10^{11} $eV^{-1}cm^{-2}$.

4:15 PM N8.7/T6.7

THE INFLUENCE OF DEFECTS ON COMPATIBILITY AND YIELD OF THE HFO_2-POLYSILICON GATE STACK FOR CMOS INTEGRATION. V.S. Kaushik, J. Kluth, A. Kerber, E. Cartier, W. Tsai, E. Young, M. Green, J. Chen, S-A. Jang, S. Lin, International Sematech, Austin, TX; S. DeGendt, R. Carter, M. Claes, E. Rohr, L. Pantisano, O. Richard, C. Zhao, H. Bender, M. Caymax, M. Heyns, Inter-university MicroElectronic Center (IMEC), Leuven, BELGIUM; Y. Manabe, Hitachi, Ltd., Semiconductor & Integrated Circuits, Tokyo, JAPAN.

Hafnium-based dielectrics are under wide consideration for high-K gate applications. For rapid introduction of high-K materials into current CMOS platforms, compatibility of the dielectric layer with conventional polysilicon gate electrodes is critical. In contrast to the case of ZrO_2, the formation of silicides has not been reported for HfO_2. Nonetheless, we have observed that there are several challenges with the HfO_2-Polysilicon gate stack requiring suitable process solutions. Capacitors were fabricated with HfO_2 deposited by ALD and MOCVD, using polysilicon gate electrodes deposited by industry-typical CVD processes. These devices showed leakage failures with yields that were observed to depend on the area, dielectric thickness and annealing conditions during the process. The process used to deposit the polysilicon also affected the yield. Investigation of the root cause of these leakage failures suggested that the leakage failures may be caused by a defect-related mechanism. The implication of this is that the leakage occurs at localized defect sites rather than broadly through the HfO_2 layer. A model was proposed to explain the nature and behavior of these defects in causing electrical leakage failures. Emission microscopy analysis and physical characterization of the HfO_2 film were used to corroborate the proposed model. Defect density was observed to be strongly dependent on the processing of the dielectric film. In order to make Hf-based dielectric stacks compatible with polysilicon for conventional CMOS transistor integration with acceptable yield, further post-deposition treatment may be necessary to eliminate or cure the defects. The observations and process modifications discussed in this paper may also find applicability with other dielectric-electrode gate stacks.

4:30 PM N8.8/T6.8

ELECTRICAL CHARACTERIZATION OF CRYSTALLINE ALKALINE EARTH OXIDES. Curt Billman, Fred Walker, Rodney Mckee, Oak Ridge National Laboratory, Oak Ridge, TN.

The electrical properties of thin-film crystalline alkaline earth oxides on silicon are of particular relevance to such problems as band alignment at an oxide/semiconductor interface. Prior to this work the electrical properties of these oxides were not known in thin-film form because electrical characterization is hampered by their reactivity in air. We have grown thin-film crystalline oxides on silicon by molecular beam epitaxy. Metal oxide semiconductor capacitors have been fabricated using an in-situ ultra-high vacuum (UHV) metal deposition chamber and the electrical characterization was also performed in-situ in a UHV probe station. The first capacitance versus voltage and leakage current measurements for the unique alkaline earth oxide $Ba_{0.75}Sr_{0.25}O$ which is perfectly commensurate with silicon will be presented. The interface state density and dielectric dispersion for these relatively high dielectric constant oxides on silicon will be discussed.

SESSION N9/T7: JOINT POSTER SESSION
CRYSTALLINE OXIDES FOR GATE DIELECTRICS
Chairs: Jon-Paul Maria and Darrell G. Schlom
Wednesday Evening, December 4, 2002
8:00 PM
Exhibition Hall D (Hynes)

N9.1/T7.1

SUPPRESSION OF HYSTERESIS IN CAPACITANCE-VOLTAGE (C-V) CHARACTERISTICS OF YSZ/Si(001) AND ZrO_2/Si THIN FILMS BY Nb-DOPING. Naoki Wakiya, Tomohiko Moriya, Kazuo Shinozaki and Nobuyasu Mizutani, Tokyo Institute of Technology, Dept of Metallurgy and Ceramics Science, JAPAN.

Yttria stabilized zirconia (YSZ) and undoped zirconia (ZrO_2) thin films on Si substrate are attractive buffer layer materials for ferroelectric random access memory (FeRAM) and high-k applications due to their high dielectric constants and diffusion barrier characteristics. However, both YSZ/Si and ZrO_2/Si thin films show ion-drift type hysteresis in capacitance-voltage (C-V) characteristics, which is deleterious for above applications. So far, the reason for the ion-drift type hysteresis was ascribed to the oxygen vacancies. Therefore, it is expected that the hysteresis can be suppressed if the vacancies are disappeared. The purpose of this work is to propose new method to suppress the hysteresis in C-V characteristics by Nb-doping. In this work, all thin films (YSZ, ZrO_2, Nb-doped YSZ and Nb-doped ZrO_2) were prepared by rf-magnetron sputtering. YSZ and ZrO_2 thin films on Si(001) substrate had (001) orientation. The orientation was unchanged by the Nb-do! ping. For both YSZ and ZrO_2 thin films, around 2.0V ion-drift type hysteresis was clearly observed in C-V characteristics. Nb-doping into YSZ brought about the increase of lattice parameter up to 20 mol% of Nb, which suggests that Nb was incorporated into YSZ lattice up to 20 mol%. By the Nb-doping, the hysteresis in C-V characteristics for YSZ thin film was considerable decreased to around 0.1V. Drastic suppression of the hysteresis in C-V characteristics was observed for Nb-doped ZrO_2 thin film. In this case, the hysteresis was completely disappeared. These facts suggest that oxygen vacancies in YSZ and ZrO_2 thin films would be suppressed or disappeared by Nb-doping. This means that Nb is a excellent dopant for both YSZ and ZrO_2 to suppress the ion-drift type hysteresis.

N9.2/T7.2

A STUDY OF Al_2O_3(C) FILMS ON Si(100) GROWN BY LOW-PRESSURE MOCVD. M.P. Singh, S.A. Shivashankar, Materials Research Centre, Indian Institute of Science, Bangalore, INDIA.

Metalorganic chemical vapour deposition (MOCVD) is an attractive process for the fabrication of thin film dielectrics and other coatings because the temperature of deposition can be lowered, but it can lead to the incorporation of hetero-atoms (namely C and H) into the film matrix. As Al_2O_3 is a promising candidate to replace SiO_2 as the gate dielectric in ULSI devices of the next generation, a study of the CVD of Al_2O_3 using carbon-containing precursors is important. In the present work, the deposition of aluminium oxide films was carried out by low-pressure MOCVD on p-type Si(100), using aluminium acetylacetonate as precursor. The focus is the study of the effects of the carbon in the films, which derives from the precursor itself, on the transport properties of the alumina. For the present work, film depositions were carried out in inert as well as oxidizing ambient, to obtain films of different carbon contents. Argon and nitrous oxide were employed as the inert and oxidizing gas, respectively. The films as-deposited comprise nanometer-sized grains of kappa-alumina (~50 nm), as examined by XRD and TEM. The films display a mirror-like sheen as examined by the optical microscopy. An attempt has been made to explore the defects (viz. oxide charge density) in the films using high frequency C-V measurements. We observe hysteresis in the high frequency C-V plots, indicative of charge trapping in the Al_2O_3. The effect of carbon, incorporated into the film from the precursor itself, on the C-V curve of alumina films will be discussed in detail. The chemical nature of carbon, which is graphitic in nature, was characterized and confirmed by various techniques such as Fourier transform infrared (FTIR) spectroscopy, x-ray photoelectron spectroscopy (XPS) and secondary ion mass spectroscopy (SIMS). This observation is used to interpret the C-V measurements.

N9.3/T7.3

GATE DIELECTRIC PROPERTY AND BUFFER INSULATOR CHARACTERISTICS OF ULTRATHIN ZIRCONIUM OXIDE FILMS DEPOSITED BY REACTIVE RF MAGNETRON SPUTTERING. Hoon Sang Choi, Geun-Sik Lim, Jong-Han Lee, Yu Min Jang and In-Hoon Choi, Department of Materials Science and Engineering, Korea University, Seoul, KOREA.

The zirconium oxide (ZrO_2) layer has been reported to have a relatively high dielectric constant and a strong barrier property against diffusion. Therefore, the buffer layer combined with SiO_2 is expected to have a good interface with silicon and a strong barrier property against interdiffusion. The emphasis of the results is twofold: the first is the high quality of the investigated films as evidenced by the small measured values of loss factor, flatband voltages, and surface states density as well as the low dispersion of the relative dielectric constants. This work examines the structural and electrical properties of ZrO_2 thin films deposited by rf magnetron sputtering using a Zr target. The ZrO_2 /$ZrSi_xO_y$ /SiO_2 layer is stoichiometric, uniform, amorphous, and has an equivalent oxide thickness of ~1 nm and a dielectric constant range from 15 to 18 depending upon process conditions and very small C-V hysteresis and low leakage current. The second is that Metal-ferroelectric-insulator-semiconductor (MFIS) structures using zirconium oxide (ZrO_2) layers as an insulating barrier against interdiffusion have been investigated. Strong barrier effect of ZrO_2 layer is demonstrated by both High-resolution transmission electron microscopy (HRTEM) and analysis of Auger Electron Spectroscopy (AES). Coercive field that decisively affects the memory window becomes greater by inserting the ZrO_2 buffer layer between ferroelectric thin film and silicon substrate and thus the memory window also increases with an electric field to the $SrBi_2Nb_2O_9$ (SBN). The memory windows of the MFIS structure were in the range of 0.7 ~ 3.6 V for gate voltages form 3 to 9 V. The maximum memory window was observed in the MFIS with a 12-nm-thick ZrO_2 layer. And the leakage current density was 4.74×10^{-8} A/cm^2 at an applied voltage of 3 V.

N9.4/T7.4

Abstract Withdrawn.

N9.5/T7.5

CONDUCTION MECHANISMS IN $SrTiO_3$ THIN FILMS ON SILICON. Bogdan Mereu, Max Planck Institute of Microstructure Physics, Halle, GERMANY, National Institute for Material Physics, Bucharest-Magurele, ROMANIA; George Sarau, National Institute for Material Physics, Bucharest-Magurele, ROMANIA; Jean Fompeyrine, Gerd Norga, IBM-Zürich, Zürich, SWITZERLAND; Marin Alexe, Max Planck Institute of Microstructure Physics, Halle, GERMANY.

New materials with high dielectric constant are currently being explored to replace silicon dioxide as gate dielectric for device scaling below 0.1 μm. With respect to conventional SiO_2, these high permittivity dielectrics provide the required equivalent oxide thickness (EOT) without of further reduction of the insulator physical thickness, which is a key issue to limit gate leakage current and to maintain comparable MOSFET operation and reliability. Among prospective high-k dielectrics $SrTiO_3$ has a high bulk dielectric constant, as well as a high degree of structural compatibility with Si making epitaxy possible. It has been demonstrated that single-crystal $SrTiO_3$ thin films can be grown on Si substrates by molecular beam epitaxy (MBE) and can provide for MOS devices interface states densities as low as 6x10^{10} states/cm^2 eV. The present paper presents preliminary results on conduction mechanisms in thin epitaxial $SrTiO_3$ films grown by MBE on Si(100). I-V measurements were performed on Metal/STO/Si structures with Al and Pt as gate electrode at temperatures ranging from 30 K to 300 K. At low temperatures the dominant conduction mechanism is F-N tunneling, while at high temperatures Schottky behavior superimposes. Difference work functions of Al and Pt and F-N tunneling fit allow calculation of both m_{ox}, the electron effective mass in oxide and Φ_B, the barrier height for electrons. From Schottky behavior the dielectric constant of STO thin film was estimated taking into account the independence of tunneling current with temperature.

N9.6/T7.6

ELECTRICAL CHARACTERIZATION OF ATOMIC-LAYER-DEPOSITED $SrTiO_3$ THIN FILMS FOR CMOS APPLICATIONS. Seong Keun Kim, Oh Seong Kwon, Cheol Seong Hwang, Seoul National University, School of Materials Science and Engineering, Seoul, KOREA.

$SrTiO_3$ (STO) thin films were deposited by an atomic-layer-deposition (ALD) technique on Si wafer using $Sr(thd)_2$, $Ti(tBuO)_2(thd)_2$ or $Ti(O\text{-}iPr)_2(thd)_2$ as the Sr, Ti precursors, respectively, and remote-plasma activated H_2O or O_3 as oxidant. ALD of STO film was rather difficult due to the very low incorporation rate of TiO_2 into the film even under the deposition conditions where the TiO_2 film growth was successful. This was believed to be due to the low sticking probability of the Ti precursors on the SrO surface. Therefore, process recipe was optimized for growing the stoichiometric STO films. Electrical characterization of Pt/STO/p-Si MOS capacitors was performed using C-V and J-V measurements. Interfacial reactions with the Si substrate during the film deposition and post-annealing were investigated by HRTEM and Auger electron spectroscopy. The dielectric constant of the STO film was measured by the film thickness vs. CET plots. The MOS capacitor showed very promising electrical characteristics even under the absence of any interfacial-reaction barrier layers. Further improvements in CET, by adoption of AlO_x or SiN_x barrier layer, will also be reported.

N9.7/T7.7

HRTEM INVESTIGATION OF EFFECT OF VARIOUS RARE EARTH OXIDE DOPANTS ON EPITAXIAL ZIRCONIA HIGH-K GATE DIELECTRICS. Takanori Kiguchi, Tokyo Institute of Technology, Center for Advanced Materials Analysis; Naoki Wakiya, Kazuo Shinozaki and Nobuyasu Mizutani, Tokyo Institute of Technology, Dept of Metallurgy and Ceramics Science, Tokyo, JAPAN.

ZrO_2 is one of the promising materials for high-K gate dielectrics substituting for a conventional SiO_2 gate dielectric. It has higher K of 25, higher band gap of 7.8, higher ΔEc of 1.4eV, and thermal stability. It is said that the amorphous phase is desired due to the homogeneity. Unfortunately, ZrO_2 is crystallized only above 400°C. The crystalline ZrO_2 is monoclinic phase below about 1100-1200°C, so that pure ZrO_2 gate dielectric layer is polycrystalline film of nano-grains on Si substrates. The grain boundaries in such an ultra thin films plays an undesirable role as the leak current pass. Therefore, single crystal like epitaxially grown gate dielectric layer is thought to be another ideal gate dielectrics. The tetragonal or cubic phase of ZrO_2 doped with some rare earth oxide is useful for the epitaxial gate dielectrics. Such a dopant makes zirconia ion conductive by oxygen vacancy. The oxygen vacancy is source of hysteresis of C-V curve due to ion drift. The ionic conductivity decreases with increase of the ionic radius of rear earth ions from Sc,Y, Lu to Sm. The rare earth ion with larger ionic radius prevents the migration of oxygen and the vacancy, which could be applied to prevent the ion drift. Then, it is considered that the ionic radius of rear earth ions affects the C-V hysteresis property. On the other hands, there is another problem that the low-K SiO_2 layer generated at the ZrO_2/Si interface. It is thought that the rare earth ion with larger ionic radius would be also effective for this problem. In this work, the effect of the radius of rare-earth ions on the interface structure and the C-V property of Sc_2O_3, Y_2O_3 and Sm_2O_3 doped (001) epitaxial ZrO_2 gate dielectrics would be considered by high-resolution transmission electron microscope (HRTEM).

N9.8/T7.8

THERMAL STABILITY OF ATOMIC-LAYER-DEPOSITED HfO_2 THIN FILMS ON THE SiN-PASSIVATED Si SUBSTRATE. Hong Bae Park, Moonju Cho, Jaehoo Park, and Cheol Seong Hwang, School of Materials Science and Engineering and Inter-university Semiconductor Research Center, Seoul National University, Seoul, KOREA; Jaehack Jeong and Kwang Soo Hyun, Ever-tek Co., Kyunggi-Do, KOREA.

HfO_2 thin films were deposited on SiN_x -passivated Si wafers at 300° and 400° using an atomic-layer-deposition technique. Reaction barrier layer, SiN_x films were introduced to suppress the interfacial reactions at HfO_2/Si interface. The SiNx films were deposited by another atomic-layer-deposition process at 595°. The SiN_x films worked as a good barrier to both Si and O diffusion resulting in a small decrease in the capacitance density even after post-annealing at temperatures up to 1000° compared either to the HfO_2 film deposited directly on Si or an Al_2 O_3 -barrier-layer/Si substrate. The decrease in the capacitance density after post-annealing, although relatively small, was due to Hf and O diffusion into the interface layer. Interestingly, post-annealing under an atmosphere containing small amount of oxygen (∼1%) decreased the capacitance density to a smaller degree. However, the interface and bulk capturing of the carrier was serious resulting in a rather large hysteresis (∼100mV) voltage in the capacitance voltage measurements even after post-annealing.

N9.9/T7.9

THE ATOMISTIC ORIGIN OF HIGH DIELECTRIC CONSTANTS OF Ta_2O_5 THIN FILM DEPOSITED ON Ru ELECTRODES.
Tomoyuki Hamada, Takuya Maruizumi, Masahiko Hiratani, Advanced Research Laboratory, Hitachi Ltd, Tokyo, JAPAN.

Ta_2O_5 thin film deposited on Ru electrodes has recently attracted much attention, because it has a substantially larger dielectric constant ϵ ($\epsilon > 60$) than that of Ta_2O_5 in the bulk state ($\epsilon = 22$) and is thought to be a promising material for 1G-bit and post 1G-bit DRAM memory-capacitor applications. However, to date, the microscopic origin of the ϵ enhancement has not been thoroughly investigated. This study is the first attempt to investigate the origin of the enhancement in the film at the atomic level by using a molecular orbital (MO) method. The crystal structure of a Ta_2O_5 thin film deposited on a Ru electrode was investigated by using the electron diffraction (ED) method. The ED experiment clarified that the film had the hexagonal Ta_2O_5 crystal structure and that c axis of the film was aligned perpendicular to the electrode surface. We found that the film had one-dimensional TaO chains in its unit cell and was an aggregate of the chains, the chains of which consisted of alternating atoms of Ta and O and were parallel to c axis of the film. The electronic structure and polarizabilities of the one-dimensional chain were calculated by using the Becke3LYP density functional (DFT) MO methods. The MO calculation results showed that the chain had a one-dimensionally delocalized electronic structure and largely enhanced polarizabilities. ϵ of the film was calculated from the polarizabilities of the chain by assuming that the polarizabilities are the microscopic origin of ϵ. Calculated ϵ (c.a. 58) fairly well agreed with the experimentally observed value (c.a. 60). The results clearly showed that the observed ϵ enhancement has its origin in the one-dimensional electronic structure of the TaO chain. This work was partially supported by ACT-JST.

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ELECTRICAL BEHAVIOR OF EPITAXIAL HIGH-k Y_2O_3 / Si(001) WITH ATOMICALLY SHARP INTERFACES.
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Molecular beam epitaxy could produce metal oxide high-k dielectrics on silicon with controlled interfaces so as to combine low equivalent oxide thickness with high channel mobility in MOSFETs. However, due to enhanced oxygen diffusivity and non-equilibrium surface kinetics during growth, the formation of undesired low-k SiO_x interfacial layer is unavoidable for the majority of the as-grown materials including Y_2O_3 [1]. In this work we show that when the layers are annealed immediately after growth in UHV the larger enthalpy of formation of Y_2O_3 (compared to that of SiO_x) drives the system to a homogeneous equilibrium state re-taking the excess oxygen previously accumulated at the interface to fill oxygen vacancies in the film. This results in atomically sharp interfaces, as evidenced by HRTEM, although small YSi_2 islands are formed at high annealing temperature ∼650°C. Remarkably, in our 6-nm-thick films, the integrity of the interfaces is maintained after exposure to air in contrast to previous reports [2] that Si is easily oxidized in ambient in thin amorphous films. The different behavior is attributed to the crystalline structure of our films, where the mechanism and rate of oxygen diffusion is different compared to amorphous material. The electrical (insulating) properties were investigated using generic metal-insulator-semiconductor capacitors. The observed trend is that the leakage current increases by increasing the temperature of annealing. This is attributed to the absence of an efficient transport barrier (such as interfacial SiO_x with high bandgap), combined with possible oxygen desorption from the metal oxide which make the dielectric layer less resistive. Finally, it is shown here, that Fowler-Nordheim tunneling occurs in epitaxial Y_2O_3 /Si(001) from which the barrier heights in as-grown and annealed samples can be estimated. [1] A. Dimoulas et al., J. Appl. Phys. **90**, 4224 (2001); A. Dimoulas et al., J. Appl. Phys., July 15 issue (2002). [2] B.W. Busch et al., Appl. Phys. Lett. **79**, 2447 (2001).

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Abstract Withdrawn.

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STUDY OF INTERFACE FORMATION OF (Ba,Sr)TiO_3 THIN FILMS GROWN BY RF SPUTTER DEPOSITION ON BARE Si AND THERMAL SiO_2/Si SUBSTRATES.
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With dielectric thickness scaling to 1-2 nanometers, the silicon/dielectric interface becomes an important issue in CMOS technology. Typically, high-K dielectrics react with Si and SiO_2 to form undesirable interface layers that degrade the overall electrical properties. In order to maintain the high quality interface and still provide a high overall capacitance of the stack an ultrathin SiO_2 layer can be used as an underlayer for a high-K film. The present study is aimed at optimization the SiO_2 underlayer in terms of minimization its effect in K yet maintaining interface quality. In-situ characterization of BST films grown on bare and thermally oxidized Si substrates has been accomplished using time of flight ion scattering and recoil spectrometry (ToF-ISARS) and spectroscopic ellipsometry (SE). Electrical characterization has been used for ex-situ studies of capacitors prepared completely in vacuo. Significant reduction of the interface layer on BST/SiO_2 as well as improvement of interface quality has been observed under certain processing conditions. Composition and structural properties have been correlated with analytical electron microscopy. The details of that study are to be presented separatly[1].
[1] Alexandra Suvorova, Martin Saunders, Natalya Suvorova, Alex Mueller, Eugene Irene. Characterization of (Ba,Sr)TiO_3 thin films on bare Si and SiO_2/Si substrates by analytical electron microscopy.