SYMPOSIUM C

Gate Stack and Silicide Issues in Silicon Processing

April 23 – 27, 2000

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TUTORIAL

ST C: TRENDS IN SILICIDES USED FOR ULSI DEVICES AND THE EFFECT OF STRESS ON SILICIDE FORMATION

Sunday, April 23, 2000
1:30 p.m. - 5:00 p.m.
Golden Gate A1 (Marriott)

This tutorial will review the integration of advanced silicides in ULSI devices. The formation mechanisms and kinetics of $TiSi_2$, $CoSi_2$, and NiSi and their effect on device properties such as junction leakage and resistivity will be reviewed. In addition, methods for measuring and modelling mechanical stresses of silicide films and submicrometer silicided lines will be reviewed. The influence of mechanical stress on silicide formation kinetics and device performance will be shown for current and future MOS technologies.

Instructors:
Christian Lavoie, IBM T.J. Watson Research Center
An Steegen, IMEC, Belgium

SESSION C1: HIGH-k MATERIALS
Chairs: Brad Herner and Matthew Copel
Tuesday Morning, April 25, 2000
Salon 5/6 (Marriott)

8:30 AM *C1.1
STABLE HAFNIUM AND ZIRCONIUM SILICATE GATE DIELECTRICS DIRECTLY ON SILICON. Glen Wilk, Bell Labs, Lucent Technologies, Murray Hill, NJ; Robert Wallace, Dept of Materials Science, University of North Texas, Denton, TX.

The area of high-k gate dielectrics has gained considerable interest recently, in large part from rapid CMOS scaling. Most roadmaps now call for a sub-2 nm gate oxide for sub-0.13 micron CMOS technology. There are considerable leakage, reliability and boron penetration concerns, however, for such thin SiO_2 layers. As an alternative, the desirable properties of a gate dielectric which could replace SiO_2 are presented. Based on this list of desirable properties, the silicate materials system, in particular hafnium and zirconium silicates ($HfSi_xO_y$ and $ZrSi_xO_y$), have demonstrated very encouraging electrical and physical properties, are discussed as good candidates to replace SiO_2 as the gate dielectric.

9:00 AM C1.2
ELECTRICAL PERFORMANCE OF PLASMA DEPOSITED ZrO_2-SiO_2 PSEUDO-BINARY ALLOYS. Robert Therrien, Bruce Rayner and Gerald Lucovsky, North Carolina State University, Raleigh, NC.

ZrO_2-SiO_2 alloys were deposited on Si(100) at 300°C. Alloy composition was controlled by varying the relative flows of the respective Zr and Si atom source gases, Zr(IV)-tbutoxide and silane. Alloy composition was determined by Rutherford backscattering, RBS, which provided a primary calibration for on-line Auger electron spectroscopy, AES. AES and off-line X-ray photoelectron spectroscopy, XPS, showed no evidence for Si-Si, Zr-Zr, or Zr-Si bonds, indicating effective oxidation of Zr and Si during film deposition. Films with compositions between SiO_2 and the compound silicate $ZrSiO_4$, were amorphous as-deposited and remained amorphous for annealing in Ar up to 1000°C. In contrast, films prepared close to ZrO_2 were crystalline upon deposition; the crystalline phase was identified by X-ray diffraction, XRD, as ZrO_2. MOS capacitors were prepared on p and n-type Si(100) using poly-Si gate electrodes. ZrO_2-SiO_2 films were deposited on HF-last Si surfaces, as well as Si substrates subjected to a pre-deposition 300°C remote plasma-assisted oxidation that produced ~0.5-0.6 nm of interfacial SiO_2. Capacitance-voltage, C-V, measurements were made on devices with electrical thickness from 3.1 to 3.6 nm in order to study flat band voltage shifts, and stress-voltage hysteresis. Hysteresis after five 3-volt cycles was less than 10 meV for devices fabricated on both HF-last and pre-oxidized n-Si(100). However, these HF-last devices showed a negative relative flat band voltage shift of ~0.15 V. In contrast, devices prepared on p-type Si(100) showed smaller differences in their flat band voltages, ~0.03 eV, but the devices prepared on the HF last Si shown four times the hysteresis of those prepared on the pre-oxidized substrates, ~20 meV compared to ~5 meV. These results indicate that both fixed charge and trapping sites are greater for deposition on HF last substrates, and here are attributed to process gas-substrate reactions that occur during film deposition. Supported by the ONR and SEMATECH/SRC FEP center.

9:15 AM C1.3
THE STRUCTURE OF PLASMA-DEPOSITED AND ANNEALED PSEUDO-BINARY SiO_2-ZrO_2 ALLOYS. Bruce Rayner, Robert Therrien and Gerald Lucovsky, NC State University, Raleigh, NC.

This paper presents a study of the local atomic structure and morphology of plasma-deposited and annealed thin films in the pseudo-binary alloy system SiO_2-ZrO_2. Films were deposited by remote plasma enhanced chemical vapor deposition (RPECVD). The compositional phase diagram of the system is separated into two regions by the compound silicate composition, $ZrSiO_4$; an SiO_2 rich alloy regime extending from SiO_2 to the silicate composition, and a ZrO_2 rich regime extending from the silicate composition to ZrO_2. Alloy compositions were determined by Rutherford backscattering (RBS). Bonding chemistry was determined by on-line Auger electron spectroscopy (AES), X-ray photoelectron spectroscopy (XPS), Raman scattering spectroscopy, and Fourier transform infrared spectroscopy (FTIR). Film morphology was determined by X-ray diffraction (XRD), and high-resolution transmission electron microscopy (HRTEM). As-deposited and annealed films (900°C in a non-oxidizing ambient) in the SiO_2-rich regime were non-crystalline. In contrast, films in the ZrO_2-rich regime were generally non-crystalline as-deposited, but were converted to nanocrystalline diphasic materials following the 900°C anneal. The crystalline phase was identified by XRD as ZrO_2. As-deposited and annealed films showed no evidence for Si-Si, Zr-Si, or Zr-Zr bonds over the entire alloy regime by XPS and AES, thereby establishing the pseudo-binary alloy character, and the effectiveness of the RPECVD process in fully-oxidizing both alloy components. The local atomic bonding arrangements were determined from FTIR and Raman scattering spectroscopies, and were consistent with the equilibrium phase diagram. After the 900°C anneals, the films in the SiO_2-rich regime continuously evolved from a non-crystalline SiO_2 network structure, through a network-modified structure comprised of SiO_2 and partially covalent $ZrSiO_4$ non-crystalline silicate regions. In the ZrO_2-rich regime, the films evolved from a partially-covalent $ZrSiO_4$ non-crystalline silicate structure, through a two-phase regime comprised of nano-crystals of ZrO_2, encapsulated within the partially covalent $ZrSiO_4$ non-crystalline silicate phase, and finally to a nano-crystalline ZrO_2 end-member. Supported by the ONR and SEMATECH/SRC FEP center.

9:30 AM C1.4
ELECTRICAL AND MATERIAL CHARACTERISTICS OF ALCVD ZrO_2 GATE DIELECTRICS. Charles M. Perkins, Paul McIntyre, Dept. of Materials Science and Engineering, Stanford University, Stanford, CA; Krishna Saraswat, Dept. of Electrical Engineering, Stanford University, Stanford, CA; Baylor Triplett, Components Research, Intel Corp., Santa Clara, CA; Marko Tuominen, Suvi Haukka, ASM/Microchemistry Ltd., Espoo, FINLAND.

Due to increasing levels of direct tunneling current, SiO_2 thinner than ~1.5 nm cannot be used as the gate dielectric for CMOS technology. One of the most promising materials predicted to be thermodynamically stable in contact with Si is ZrO_2 [1]. Its stability, along with a dielectric constant of 20-25 and a bandgap of 7.8 eV, make it an excellent candidate for gate dielectric applications. In this study, we have demonstrated ultrathin ZrO_2 gate dielectrics of < 1.5 nm equivalent oxide thickness (EOT) with significantly ($> 10^7$X) lower leakage current compared to SiO_2 of identical thickness. LOCOS isolated MOS capacitors were used in our study. ZrO_2 films of physical thickness of 2 to 7 nm were prepared by atomic layer chemical vapor deposition (ALCVD) at 300°C using $ZrCl_4$ and H_2O as precursors. All films were found to be polycrystalline with a monoclinic crystal structure. The leakage current of the as-deposited films is exceptionally low, with one 5 nm sample yielding a leakage value of 10^{-6} A/cm^2 at a gate bias of -2 V. The same sample resulted in a C_{ox} value of 25 fF/μm^2 at a gate bias of -3 V (corresponding to an EOT value of 1.4 nm without subtracting quantum mechanical effects). Minimal frequency dispersion and good hysteresis properties ($\Delta V_{FB} < 15$ mV for 1 to -2 V sweep) were also observed. Further material analyses include XPS, AES, AFM and TEM studies. [1] K.J. Hubbard, and D.G. Schlom, J. Mater. Res., 11(11) 2757 (1996).

9:45 AM C1.5
ULTRATHIN ZrO_2 GATE DIELECTRIC FOR CMOS PROCESS. Eduard Cartier, Evgeni Gusev, Matt Copel, IBM, Yorktown Heights, NY; Boyong He, University of Minnesota; Mike Gribelyuk, IBM, Analytical Service, Hopewell Junction, NY.

Throughout the history of semiconductor industry, the feature size of IC chip has been continuously scaled to achieve high productivity, lower cost per function and higher IC speed. To scale the feature size beyond 100nm, an oxide thickness of 1.5 nm - 2.0 nm is required, but the tunneling current for these ultrathin oxides is too large to be tolerated. There are also serious reliability and process control concerns for these ultrathin oxides. So the ultimate challenge to scale

the feature size beyond 100 nm is to find an alternative gate dielectric with a higher dielectric constant, an interface and thermal stability compared to SiO_2 on Si. A range of high permittivity alternative gate dielectrics have been studied. In this presentation, the focus is on ZrO_2, which has a 6 times higher dielectric constant than SiO_2 and is predicted to be thermally stable on silicon. The ZrO_2 films with thicknesses from 3 to 10 nm were deposited on differently prepared Si surfaces with thin thermal oxides, oxynitrides and hydrogen termination. The films were characterized with HRTEM and Medium Energy Ion Scattering (MEIS) and AFM. Thermally evaporated Al was used as the gate electrode for electrical characterization. All as deposited films show rather poor electrical properties. However, it is found that post deposition annealing can be optimized to reduce bulk electron trapping, to obtain good interface quality and to significantly reduce gate leakage as compared to SiO_2. Significantly reduced leakage currents were achieved even for films with 1.5 nm equivalent oxide thickness. But the control of the formation of interfacial oxide with a low dielectric constant appears to be the challenge for the fabrication of films with equivalent oxide thickness below 1.5 nm.

10:15 AM C1.6
KINETICS OF SILICON/METAL OXIDE INTERFACE LAYER FORMATION DURING HIGH-K DEPOSITION ON SILICON.
J.J. Chambers, D. Niu, G.N. Parsons, Dept. of Chemical Engineering, North Carolina State University, Raleigh, NC.

A variety of metal oxides and silicates are currently being studied as possible gate dielectrics for sub-100 nm CMOS devices. Based on the thermodynamic properties of bulk materials, several high dielectric constant metal oxides, including those of Hf, Zr, Y, and Al, are stable in contact with silicon. We have studied a novel two-step sputter/ rapid-thermal oxidation process to form thin (<5 nm) yttrium silicates on silicon. The process involves sputtering ~1nm of yttrium metal, followed by rapid (≈15 s) oxidation in N_2O at 900°C. The resulting films are analyzed using XPS, high resolution TEM, and IV/CV electrical measurements. XPS indicates that upon annealing, the yttrium metal first reacts with silicon to form a silicide, and the silicide rapidly oxidizes to form a single layer material that contains Y-O-Si (yttrium silicate) bonds. CV analysis results in equivalent oxide thicknesses less than 11Å can be attained on both n- and p-type substrates, independent of frequency between 10kHz and 1MHz. Gate leakage is less than 10^{-1} Å/cm^2 at 1V in accumulation on n- and p-substrates. For the thinnest layers, threshold voltage shifts are consistent with interface charge, possibly due to residual silicide bonding. We have also deposited aluminum oxide films on silicon by CVD from metal organic precursors, and found from XPS and nuclear reaction profiles, that this process leads to a two-layer aluminum oxide/aluminum silicate structure. These results give important insight into the nature of interface-layer formation reactions that determine the structure of the critical dielectric/silicon interface. We believe that the reaction products during metal oxide deposition are not determined by the thermodynamic stability of the bulk materials, but rather are determined by the kinetics of surface reactions that proceed under non-equilibrium low temperature deposition conditions. These reactions, likely involving metal-silicon bonds or surface OH groups, favor consumption of the silicon substrate, leading to the observed silicate interface. Reactions that consume the substrate are expected to occur in a wide variety of low temperature metal oxide and metal silicate deposition processes.

10:30 AM C1.7
MATERIALS AND PROCESS COMPATIBILITY OF TANTALUM PENTOXIDE AND BST FOR ADVANCED HIGH K GATE STACKS. J. Guan, G. Gale, G. Bersuker, L. Vishnubhotla, G. Smith, A. Karamcheti, V.H.C. Watt, T.Y. Luo, A. Agarwal, P. Lysaght, G. Williamson, B. Nguyen, G. Brown, P. Zeitzoff, F. Shaapur, M. Gilmer, K. Torres, M. Jackson, H.R. Huff, Sematech, Austin, TX; J. Cheng and W. Lee, EKC Technology; K. Christensen, FSI International; Tom Hackett, Ashland Chemicals.

The compatibility of high K gate dielectric materials tantalum pentoxide and BST with various process chemicals was investigated in conjunction with metal gate electrode materials as part of an effort to develop advanced MOSFET fabrication processes. Tantalum pentoxide films prepared by MOCVD exhibited an extremely low etch rate, ~1/300 of silicon dioxide in HF, and are essentially inert in other widely used process chemicals such as SC1, SC2, SPM, and resist stripping solvent chemistries. On the other hand, MOCVD BST films were found to dissolve readily in most aqueous process chemistries, particularly in acidic chemistries such as HF, SC2 and SPM, with an etch rate greater than 100 nm/min. As a result, the processing of gate stacks with tantalum pentoxide or BST as a gate dielectric using a conventional flow normally used for the SiO_2/poly MOS gate stack appears to be very problematic. Among the issues unveiled was that tantalum pentoxide remaining after electrode etch processing for a gate stack of poly/TiN/ Ta_2O_5/Si was very difficult to remove using available wet chemistries, preventing the growth of the screen oxide in preparation for the LDD (or S/D extension) implant as well as making it difficult to electrically contact the S/D. For BST based gate stacks, any aqueous acidic wet clean chemistries will be expected to cause serious undercutting of the gate dielectric due to dissolution. In addition, new electrode materials will certainly pose added complications in processing. Additional issues and potential solutions in the fabrication of high K gate stacks involving chemical processing will also be discussed.

10:45 AM C1.8
ELECTRICAL CHARACTERISTICS OF TaO_xN_y FOR HIGH-k MOS GATE DIELECTRIC APPLICATIONS. Kiju Im, Hyungseok Jeong and Hyunsang Hwang, Department of Materials Science and Engineering, Kwangju Institute of Science and Technology, Puk-gu, Kwangju, KOREA; Dooyoung Yang, JuSung Engineering, Kwangju-gun, Kyunggi, KOREA.

Due to the low dielectric constant and high leakage current of SiO_2, alternative high-k gate dielectrics are necessary. In this paper, we have investigated TaO_xN_y thin film for high-k gate dielectric applications. After standard wafer cleaning, 1 nm-thick SiO_2 layer was grown by PECVD to reduce the high interface state density between Si/ TaO_xN_y. For some samples, plasma nitridation in NH_3 was performed to grow 1nm-thick nitride layer. A 8nm-thick TaO_xN_y was deposited at 400°C by MOCVD using NH_3 and Ta-source. For some samples, rapid thermal reoxidation in O_2 ambient was performed at 800°C for 30sec. After 200nm-thick aluminum deposition, various devices with different gate area were defined by photolithography and etching. To compare the electrical characteristics, conventional MOS capacitors with 8-nm thick Ta_2O_5 was also fabricated. The highest accumulation capacitance value with leakage correction was 24fF/um^2 and minimum equivalent oxide thickness was 1.3nm for sample without nitridation and reoxidation. Considering 8nm-thick TaO_xN_y with 1nm-thick interface SiO_2 layer, the dielectric constant of TaO_xN_y is approximately 100. In addition, the leakage current of TaO_xN_y at -1.5V was less than 10mA/cm^2 which is slightly less than that of Ta_2O_5. The hysteresis was negligible for both TaO_xN_y and Ta_2O_5. We have investigated the thermal stability of TaO_xN_y. Compared with Ta_2O_5, the degradation of capacitance was relatively high for TaO_xN_y with increasing reoxidation temperature. Based on AFM analysis, the surface roughness of TaO_xN_y was significantly degraded with increasing reoxidation temperature above 800°C. Under the constant current stress, we observed less gate voltage shift for TaO_xN_y which indicates less charge trapping. The charge-to-breakdown characteristics of both samples were comparable. In summary, TaO_xN_y exhibit some promises for future high-k gate dielectric applications.

11:00 AM C1.9
THE STUDY OF THE MICROSTRUCTURE AND ELECTRICAL PROPERTIES OF CeO_2 THIN FILM DEPOSITED BY REACTIVE DC MAGNETRON SPUTTERING SYSTEM UPON ANNEALING.
Yun-ha Jeong, Sung-kwan Kang, Seok-woo Nam, Dae-Hong Ko, Dept. of Ceramic Engineering, Yonsei Univ., Seoul, SOUTH KOREA.

Cerium oxide (CeO_2) has been suggested as an intermediate layer between the ferroelectric film and the Si substrate in MFIS structures, or as a gate dielectric material for ULSI CMOS devices due to their high thermal stability and high dielectric constant. We investigated the evolution of the microstructures and the consequent change of the electrical properties upon annealing in the thin film CeO_2 layer deposited on the Si substrate. The cerium oxide layer was deposited by reactive DC magnetron sputtering on the (100) silicon substrate, and subsequently annealed in the Ar gas ambient or in the O_2 gas ambient. The films were analyzed by XRD, HRTEM, RBS, AFM and XPS. The electrical properties were measured by C-V and I-V measurements for MIS structures with a CeO_2 film as an insulating layer. By HRTEM and XPS analyses, we observed the presence of the SiO_2 interlayer between the CeO_2 films and the Si substrate in an as-deposited sample. The interlayer SiO_2 grew upon annealing in O_2 ambient by the oxidation reaction between the oxygen species diffused from the ambient and the Si substrate. We also observed the change of the surface morphology of the CeO_2 films during the annealing treatments. The C-V measurements demonstrated that the capacitance values of the MIS structures with a CeO_2 film as an insulating layer was changed upon annealing in an Ar gas ambient as well as in an O_2 gas ambient. The I-V characteristics of the MIS structure showed that the leakage current level and breakdown voltage were improved upon annealing treatments. Such changes in electrical properties are well matched with the evolution of the oxidation behaviors at the CeO_2/Si interfaces.

11:15 AM C1.10
PEROVSKITE TERMINATED SILICON AS A PLATFORM FOR ALTERNATIVE GATE OXIDES ON SILICON. C.A. Billman, D.G. Scholm, Penn State University, University Park, PA; R.A. McKee, F.J. Walker, Oak Ridge National Laboratory, Oak Ridge, TN.

The growth of alternate gate oxides for silicon microelectronic devices is a difficult challenge, but the heteroepitaxy principles for commensurate oxide/semiconductor systems developed by McKee et. al. may overcome this challenge. The crystalline oxides on semiconductor (COS)-based method was used to grow a $SrTiO_3$ truncation on silicon in a growth chamber at Oak Ridge National Laboratory. The sample was then transported, in ambient air, to a growth chamber at Penn State University where an epitaxial thin film growth of $LaAlO_3$ was obtained using COS-based growth techniques. The thin film growth of $LaAlO_3$ was excellent with single crystal epitaxy being obtained. The results of the epitaxial thin film growth of $LaAlO_3$ on a 3-unit cell perovskite-on-silicon are presented, which demonstrates the robustness of perovskite-teminated silicon fabricated by the COS-based growth technique.

OUTSTANDING YOUNG INVESTIGATOR ORAL PRESENTATION

11:30 AM *C1.11
DYNAMIC STUDIES OF SEMICONDUCTOR GROWTH PROCESSES USING IN-SITU ELECTRON MICROSCOPY. Frances M. Ross, IBM T.J. Watson Research Center, Yorktown Heights, NY.

Many of the surface and interface reactions of interest for microelectronics processing have been studied using in situ electron microscopy, since the ability to observe processes in real time allows microscopists to investigate mechanisms and growth kinetics in a quantitative way. These reactions include silicon oxidation, silicide formation, metal film deposition and the epitaxial growth of GeSi alloys on Si. In this presentation we will show some of our own in situ results and describe the information available from such experiments. Using an in situ chemical vapour deposition system, we observed the growth of self-assembled GeSi islands on Si, following the development of individual islands and measuring the fascinating shape change which occurs during growth. We find that the observations are best fitted by a model in which the islands grow by a modified Ostwald ripening process, strongly influenced by the shape change. This model suggests how growth conditions can be optimized to produce uniform arrays of islands for "quantum dot" devices. The growth of self assembled cobalt disilicide islands follows different kinetics, being rate limited by the surface diffusion of Si, and we find that this makes it more difficult to control the island size and placement. For the case of silicon oxidation, we focused on the motion of Si steps during the reaction. Although surface steps flow during low pressure oxygen etching, the interface steps are immobile during thermal oxidation, suggesting a close relationship between the flatness of the starting surface and the quality of the final oxide layer. We will conclude with a discussion of a different class of growth process - electrochemical deposition of materials from a liquid solution - and show how in situ electron microscopy may allow us to observe the dynamics of liquid/solid interfaces as well.

SESSION C2: NOVEL GATE INSULATORS

Chairs: Stephen A. Campbell and Robert Therrien
Tuesday Afternoon, April 25, 2000
Salon 5/6 (Marriott)

1:30 PM *C2.1
RELIABILITY OF ULTRATHIN GATE DIELECTRICS. J.H. Stathis and D.J. DiMaria, IBM Research, Yorktown Heights, NY.

The microelectronics industry owes its considerable success largely to the existence of the thermal oxide of silicon. Any candidate for an alternative dielectric must meet or exceed the properties of the silicon/SiO_2 system including both performance and reliability. In this talk we will review the physics of oxide breakdown. Electrons tunneling through the gate oxide generate defects until a critical density is reached and the oxide breaks down. The critical defect density is explained by the formation of a percolation path of defects across the oxide. However, only $< 1\%$ of the these paths ultimately lead to destructive breakdown, and the microscopic nature of these defects is not known. The rate of defect generation decreases exponentially with supply voltage, but the tunnel current also increases exponentially with decreasing oxide thickness, leading to a diminishing margin for reliability as device dimensions are scaled.

2:00 PM C2.2
CRYSTALLINE OXIDES AS GATE DIELECTRICS FOR MOSFETS. F.J. Walker, D.P. Norton, O.W. Holland and R.A. McKee, Oak Ridge National Laboratory, Oak Ridge, TN.

The application of crystalline oxides grown commensurately with silicon promises a number of advantages as a gate replacement material for field effect transistors. Because conduction of the channel current takes place near the oxide/silicon interface, the structural and compositional details of this interface become increasingly important as devices are scaled to channel lengths approaching 50 nm. In order to measure the effect of such details on device performance, real devices need to be made. Therefore, we have fabricated FETs on (001) silicon using a single crystal, epitaxially grown strontium titanate as a high dielectric constant gate material. Measurements on a 50 micron square device of channel mobility, leakage current and subthreshold characteristics indicate a high quality silicon-oxide interface has been formed. Research sponsored jointly by the Laboratory Directed Research and Development Program of Oak Ridge National Laboratory, and by the Division of Materials Sciences, Office of Basic Energy Science.

2:15 PM C2.3
FUNDAMENTAL LIMITS TO THE SCALING OF SILICON DIOXIDE GATE DIELECTRICS. D.A. Muller, J. Rosamelia, T. Sorsch, S. Moccio, G. Timp, Bell Labs, Lucent Technologies, Murray Hill, NJ; J. Neaton, Physics Dept., Cornell Univ., Ithaca, NY.

In 1999, a typical gate oxide is about 14 oxygen atoms thick. By 2008, the projected gate oxide thickness will be 4 oxygen atoms (1 nm). From atomic-scale electron energy loss spectroscopy (EELS) of gate oxides between 3 and 30 oxygen atoms thick[1] and ab-initio electronic structure calculations, we have shown that the electrical transition region from Si to SiO_2 occurs over a region that is 0.3-0.4 nm wide, even when the structural transition is atomically abrupt. This puts a fundamental limit of 0.7 nm on the oxide thickness in order for the bulk SiO_2 barrier height to be achieved. Silicon dioxide films thinner than this will not exhibit the bulk dielectric constant or barrier height. Both the theoretical and experimental density-of-states illustrate a serious inconsistency in the standard approximations to tunneling used in device modeling when the oxide thickness is comparable to the transition region viz: The tunneling states in the gap are developed at the expense of states in the main conduction and valence bands. The altered density of states in the interfacial region is likely the origin of the systematic error in ellipsometry for underestimating the oxide thickness on very smooth wafers (there can be compensating errors from large interface roughnesses). The EELS measurements have also illustrated the importance of roughness in controlling the gate leakage current - roughly a little over an order of magnitude reduction in leakage current per 0.1 nm rms roughness reduction.
[1] D. A. Muller, et al, *Nature* **399**, 758-761 (1999)

2:30 PM C2.4
ULTRATHIN GATE OXIDE PREPARED BY NITRIDATION IN ND_3 FOR MOS DEVICE APPLICATIONS. Hyungshin Kwon and Hyunsang Hwang, Department of Materials Science and Engineering, Kwangju Institute of Science and Technology, Puk-gu, Kwangju, KOREA.

Nitrogen incorporation in ultrathin gate dielectrics improve dielectric integrity and dopant diffusion barrier characteristics. Although NH_3 nitridation of gate dielectric can incorporate high concentration of nitrogen at low temperature, significant concentration of hydrogen in dielectric causes a degradation of device reliability such as charge trapping and interface state generation. Recently improvement of hot carrier reliability characteristics was observed after D_2 annealing of MOSFET device. Due to the heavy mass of deuterium, Si-D bonds are more difficult to break than Si-H bonds under the hot carrier stress. In this paper, we present a novel process to incorporate deuterium and nitrogen using ND_3 as a nitridation gas. Conventional polysilicon gate MOS capacitors with 6.0nm-thick gate oxides were fabricated on n-type silicon wafers. Gate oxide was grown in oxygen ambient followed by nitrogen annealing at 980°C for 30min. Nitridation in ND_3 ambient was performed at 800°C for 30min. The process pressure was 0.1atm. For comparison, nitridation in NH_3 was also performed at 770, 800°C. Compared with a post-oxidation annealing in NH_3, annealing in ND_3 ambient improves the reliability characteristics of gate oxide under the electrical stress. Gate oxides annealed in ND_3 ambient exhibit less charge trapping, less generation of interfaces state, and larger charge-to-breakdown under the electrical stress. Since the Si-D bonds are more difficult to break than Si-H bonds due to the heavy mass of deuterium, the improvement of gate oxide annealed in ND_3 can be explained. The ND_3 annealing of gate dielectric provides a good promise for future ULSI device applications.

2:45 PM C2.5
TiO_2 AS GATE DIELECTRIC: PROPERTIES AND INTERFACE CONTROL BY EMPLOYING ULTRA THIN DIFFUSION BARRIERS. A. Cappellani[1,2], B. Sell[1], M. Gutsche[1], D. Schumann[1], T. Pompl[1], H. Wurzer[1] and A. Oneill[2]. [1]Infineon Technologies, Dresden, GERMANY; [2]University of Newcastle, Newcastle, UNITED KINGDOM.

Many compounds with high dielectric constant are being widely investigated. However, better control must be obtained over the film properties and the interface between the dielectric layer and the electrodes. In this study we focus on the implementation of TiO_2 as a gate dielectric. For the first time TiO_2, formed by thermal oxidation of sputtered titanium, has been integrated into a full 0.25 μm CMOS process. Thin diffusion barriers, such as Si_3N_4, SiO_2 and TiN, were used to study the interface reaction between the dielectric and the electrodes. With the focus on grain growth during rutile phase formation and on the interface properties, the thermal stability of these stacks has been also investigated. Results show good control of the interface reaction and roughness with the use of Si_3N_4 and TiN as bottom and top diffusion barriers, achieving a significant reduction of the oxide equivalent thickness.

3:30 PM *C2.6
UNIVERSAL LEAKAGE AND OPTICAL PROPERTIES OF METAL-OXIDE FILMS. G.B. Alers, R.M. Fleming, D.V. Lang, C.D.W. Jones, C.Y. Sung, L.A. Stirling, H. Krautter, R. Opila, Y. Chabal; Bell Laboratories, Lucent Technologies, Murray Hill, NJ; X. Zhang, E. Garfunkel, Rutgers University, Piscataway, NJ.

A review will be given on the common electrical properties of metal oxide films including tantalum oxide, aluminum oxide, binary-metal oxides and ternary-metal oxides. We will report results that compare electrical measurements to optical properties, photo-stimulated current, thermally-stimulated current and XPS. Using a combination of all these techniques for both metal-oxide-metal capacitors and metal-oxide-silicon capacitors we are able to distinguish between the interface dominated electrical properties (Fermi level pinning, interfacial oxides and interface traps) vs. bulk dominated transport. We are able to identify several different leakage current mechanisms that are universal to all of these materials.

4:00 PM C2.7
FUNDAMENTAL STUDIES ON ULTRA THIN METAL OXIDE FILMS. Shriram Ramanathan, Dept. of Materials Science and Engineering, Stanford University, Pinkesh Sachdev, Krishna C. Saraswat, Dept. of Electrical Engineering, Stanford University; Carl J. Maggiore, Ion Beam Materials Laboratory, Los Alamos National Laboratory; Bruce M. Clemens, Paul C. McIntyre, Dept. of Materials Science and Engineering, Stanford University.

New materials are currently being investigated to replace silicon-di-oxide as the gate dielectric. Among these, metal oxides have been considered to be one of the most promising candidates owing to their high dielectric constant. It is however very important to be able to control the thickness of the oxide, the morphology and interfaces between the metal oxide and underlayer to obtain good electrical properties. Usually, thin metal oxide films are grown by first depositing the precursor metal film and then oxidizing by one of many techniques such as natural oxidation, plasma oxidation, etc. It is therefore, very important to study the oxidation process of the metal film and any interfacial reactions occurring between the resulting oxide and the underlayer to be able to control the desired properties. In this talk, we report on the synthesis and characterization of ultrathin metal oxide films fabricated by the technique of UV-Ozone oxidation. Thin metal films (of Al and Zr) are deposited on nitrided silicon wafers by sputtering and subsequently oxidized by exposing the film to oxygen gas in the presence of ultraviolet light. UV radiation facilitates the formation of activated oxygen species, such as ozone, which enhance the oxidation kinetics significantly. The kinetics of oxidation have been investigated by an accelerator-based nuclear reaction analysis technique which is very sensitive to oxygen in the sample. While the ion scattering technique gives valuable information on a macroscopic scale it is also important to study the microstructure at an atomic scale. For this purpose, we have used cross-sectional transmission electron microscopy to study the microstructure and the nature of the metal oxide - nitride - silicon interfaces at atomic resolution. The results of these studies will be discussed in detail.

4:15 PM C2.8
AMORPHOUS MIXED TiO_2 AND SiO_2 FILMS ON Si(100) BY CHEMICAL VAPOR DEPOSITION. Ryan C. Smith, Charles J. Taylor, Jeffrey T. Roberts and Wayne L. Gladfelter, University of Minnesota, Department of Chemistry, Minneapolis, MN; Noel Hoilien and Steven A. Campbell, University of Minnesota, Department of Electrical and Computer Engineering, Minneapolis, MN.

Thin films of composition $(TiO_2)_x(SiO_2)_y$ have been grown by low pressure chemical vapor deposition on silicon (100) substrates using $Si(O\text{-}Et)_4$ and either $Ti(NO_3)_4$ or $Ti(O\text{-}^iPr)_4$ as the sources of SiO_2 and TiO_2, respectively. The substrate temperature was varied between 300 and 535°C, and the precursor flow rates ranged from 5 to 100 sccm. Under these conditions growth rates ranging from 0.6 to 90.0 nm/min were observed. The films were carbon free within the detection limits of Rutherford backscattering spectrometry. RBS also revealed that the ratio of titanium to silicon was dependent upon the choice of TiO_2 precursor. The Ti/Si ratio for films grown using TN ranged from 1.00 to 1.54, while those grown with TTIP displayed Ti/Si ratios from 3.23 to 10.0. All films were amorphous to X-rays and SEM micrographs show smooth, featureless film surfaces. The results of TEM studies and characterization of the electrical properties will be presented.

4:30 PM C2.9
Zr AND Hf OXIDE BASED GATE DIELECTRICS WITH EQUIVALENT SiO_2 THICKNESS OF LESS THAN 1.0 nm. Yanjun Ma and Yoshi Ono, Sharp Laboratories of America, Camas, WA.

Doped and undoped ZrO_2 and HfO_2 films are investigated as an alternative to SiO_2 gate dielectric below 1.5nm. A record maximum accumulation capacitance about 31F/μm^2 with a leakage current of less than 0.1 A/cm2 has been achieved for a 4 nm Zr-O film. Al and Si doping is also investigated as the way to reduce the leakage current and increase the crystallization temperature of the film. Submicron MOSFETs with TiN or Pt gate electrodes have been fabricated with these gate dielectrics with excellent characteristics, demonstrating the feasibility of CMOS process integration.

4:45 PM C2.10
FORMATION OF A STRATIFIED LANTHANUM SILICATE DIELECTRIC BY REACTION WITH Si(001). M. Copel, E. Cartier and F.M. Ross, IBM Research Division, Yorktown Hts., NY.

The search for alternative gate dielectrics for silicon CMOS devices has stimulated intensive research in metal oxide thin films. We describe the formation of lanthanum silicate films by reaction of evaporated La_2O_3 layers with Si(001). Medium energy ion scattering results show that when deposited at room temperature, La_2O_3 does not react with SiO_2. But when heated above 600C, intermixing occurs. Low pressure oxidation at 850C insures formation of stoichiometric $La_2Si_2O_7$, with 20A of La_2O_3/Si transforming into a layered structure consisting of 40A of $La_2Si_2O_7$ atop 13A of SiO_2. The final silicate thickness is controlled by the amount of La_2O_3 deposited, and the SiO_2 thickness is controlled by the oxidation kinetics and initial oxide thickness. Transmission electron microscopy confirms the layering. A distinct pattern of electron diffraction rings is further evidence of a silicate phase. Electrical measurements on samples with Al contacts show leakage currents much lower than an equivalent thickness of SiO_2. Equivalent oxide thicknesses less than 2nm are obtained, and greater capacitances may be achieved by reducing the underlying SiO_2 thickness. Reactive silicate formation offers a new method of fabricating layered structures without resorting to atomic control of deposition. Since the layering occurs as a result of the materials reaction, the dielectric can be considered stratified, with the components self-ordering into the desired sequence, i.e. an SiO_2 passivation layer underneath a high-k insulating layer.

SESSION C3: NOVEL GATE STRUCTURES

Chairs: Larry A. Clevenger and Mark A. Shriver
Wednesday Morning, April 26, 2000
Salon 5/6 (Marriott)

NOTE EARLY START

8:15 AM *C3.1
DAMASCENE METAL GATE FOR HIGH PERFORMANCE TRANSISTORS. Kyoichi Suguro, Kazuaki Nakajima, Atsushi Yagishita, Tomohiro Saito, Seiji Inumiya, Kouji Matsuo, Yoshio Ozawa, Yasushi Akasaka, Hiroyuki Yano, Gaku Minamihaba, Yukiteru Matsui, Yoshitaka Tsunashima, Tsunetoshi Arikado and Katsuya Okumura, Process Eng. Lab., Microelectronics Eng. Lab., Semiconductor Company, Toshiba Corporation, Yokohama, JAPAN.

In accordance with the trend of scaling down transistor size, the thinning of gate insulator thickness to below 2nm is indispensable for developing high-performance transistors to be used in the 21st century. In order to break through the limitations on further thinning of gate insulators, metal gates in which there is no gate depletion and high dielectric constant gate insulators in which the tunneling current is lower than in the case of Si oxides are necessary. In this paper, the technological trend of low-resistivity gates is described and the Damascene gate process recently developed by us is also presented. Fully planarized metal (Al/TiN or W/TiN) gate transistors were uniformly fabricated by using CMP (Damascene gate) process. Damascene metal gate transistors show low sheet resistance. And good MOS characteristics were obtained for Ta_2O_5/SiO_2 or TiO_2/SiO_2 with effective oxide thickness of 2nm. It was found that the variation in crystal plane orientation of TiN affected the gate

work function and resulted in flatband voltage or threshold voltage. Extremely uniform electrical characteristics were obtained by controlling the crystalline orientation in a metal gate deposition process. Applying the Damascene gate process to high performance transistor, the process temperature after gate electrode formation can be lowered to as low as 450 degree C. Therefore, easier application of new metal gates and high dielectric constant gate insulators to high-performance transistors can now be realized.

8:45 AM C3.2
MOLYBDENUM AS A GATE ELECTRODE FOR DEEP SUB-MICRON CMOS TECHNOLOGY. Pushkar Ranade, Yee-Chia Yeo, Qiang Lu, Tsu-Jae King and Chenming Hu, University of California at Berkeley, Berkeley, CA.

Molybdenum has several properties that make it attractive as a CMOS gate electrode material. The high melting point (2610°C) and low coefficient of thermal expansion ($5{\times}10^{-6} cm/cm$°C, at 20°C) are well suited to withstand the thermal processing budgets normally encountered in a CMOS fabrication process. Mo is among the most conductive refractory metals and provides a significant reduction in gate resistance as compared with doped polysilicon. Mo is also stable in contact with SiO_2. In order to minimize short-channel effects, the gate electrodes must have work functions that correspond to E_c (NMOS) and E_v (PMOS) in Si. This would normally require the use of two metals with work functions differing by about 1V on the same wafer and introduce complexities associated with selective deposition and/or etching. In this paper, the dependence of the work function of Mo on deposition and annealing conditions is investigated. Preliminary results indicate that the work function of Mo can be varied over the range of 4.2-5.0V by suitable post-deposition annealing. Mo is thus a good candidate to replace polysilicon gates in deep sub-micron CMOS technology. Processing sequences which might allow the work function of Mo to be stabilized on either end of the Si energy band gap will be explored. The dependence of the Mo work function on crystallite orientation at the metal/dielectric interface and the stability of Mo in contact with high-permittivity gate dielectrics will also be discussed.

9:00 AM C3.3
STRUCTURAL AND CHEMICAL CHARACTERIZATION OF TUNGSTEN GATE STACK FOR 1GB DRAM. O. Gluschenkov, J. Benedict[1], L.A. Clevenger[1], P. DeHaven[1], C. Dziobkowski[1], J. Faltermeier[1], C. Lin[2], I. McStay[2], K. Wong[1]. [1]IBM Microelectronics, Semiconductor R&D Center, Hopewell Junction, NY; [2]Infineon Technologies, Hopewell Junction, NY; DRAM Development Alliance IBM/Infineon, IBM Semiconductor Research & Development Center, Hopewell Junction, NY.

As memory density increases the electrical resistivity of gate electrodes becomes a limiting factor to the proper dimensional scaling of the gates. In order to maintain low capacitance and resistance per unit length the resistivity of the gate electrode material must be in the range of that of a metal. We report on the gate electrode that contains a layer of tungsten. The poly-Si/barrier/W/cap gate stack has been successfully integrated into the standard DRAM manufacturing process. Selective sidewall oxidation was performed in a single wafer tool in the mixture of hydrogen and oxygen. Auger spectroscopy, RBS, XRD, and TEM were used to characterize the gate stack. The effectiveness of the WN diffusion barrier is found be dependent on the anneal ambient and temperature and conditions were determined in which no silicidation and oxidation of W-layer were observed after high-temperature processing. An overall 100% reduction in the sheet resistance of the word line has been demonstrated in comparison with the standard WSi gate stack of the same geometry.

9:15 AM C3.4
EFFECT OF POLYSILICON GATE TYPE ON THE FLATBAND VOLTAGE SHIFT FOR ULTRATHIN OXIDE-NITRIDE GATE STACKS. Zhigang Wang, Dexter W. Hodge, Robert T. Croswell, Nian Yang, Veena Misra, John R. Hauser, North Carolina State University, Dept. of Electrical and Computer Engineering, Raleigh, NC.

In this work, it is shown that the magnitude of flatband voltage (V_{fb}) shift for ultrathin (<2nm) silicon dioxide-silicon nitride (ON) gate stacks in MOSFETs depends on the Fermi level position in the gate material. A series of 18Å equivalent oxide thickness ON gate stack NMOSFETs and PMOSFETs were fabricated with oxides of 0 to 18Å. A linear relationship of negative V_{fb} shift with decreasing thickness of oxide was observed for both NMOSFETs and PMOSFETs. PMOSFETs showed greater negative V_{fb} shifts as compared to the NMOSFETs. This result was confirmed with a series of ON stack capacitors with P^+ and N^+ polysilicon gates on both P and N substrates with 7Å oxide and stack equivalent oxide thickness of 17Å. All capacitors with N^+ gates showed V_{fb} shifts of approximately -100mV, regardless of the substrate type. All capacitors with P^+ gates had V_{fb} shifts of approximately -600mV. The linear V_{fb} shift of NMOSFETs with interfacial oxide thickness appears to be due to a fixed positive charge at the oxide-nitride interface. The much greater V_{fb} shift for PMOSFETs may be due to a high density of donor-like interface states at the polysilicon-nitride interface, much like the interface states reported in literature between silicon and nitride. These interface states are near the valence band energy of the polysilicon. For N^+ poly, the donor-like states are filled (neutral), resulting in no additional V_{fb} shift. However, for P^+ poly, the donor-like states are empty, resulting in a net positive charge at the polysilicon-nitride interface. These interface states have an effect on the flatband voltage because of the small depletion layer developed in the polysilicon gate, thereby putting the interface charge in the effective dielectric.

9:30 AM C3.5
THERMAL STABILITY OF TiN AND WN DIFFUSION BARRIER IN DIRECT METAL GATE WITH Ta_2O_5 GATE DIELECTRICS. Ihl hyun Cho, Chang Hee Han, Joo Woan Lee, Jin Won Park, Hyundai MicroElectronics Ltd., R&D Division, Process Team, Cheongju, KOREA.

In this paper, the thermal stability of TiN and WN in the direct metal gate with Ta_2O_5 dielectrics was investigated. Before Ta_2O_5 deposition, the RTP in NH_3 was pretreated on Si-substrate. The Ta_2O_5 films (10 nm thick) was deposited by MOCVD method using Ta(OC2H5OH)5 and O_2 at 400°C, and were annealed for crystallization in O_2 at 800°C. Both TiN and WN metals were deposited by reactive sputtering with N_2 ambient. The W metal was used for gate electrode. Heat cycle was done on W/Barrier/ Ta_2O_5 from 750 to 950°C. The leakage current was increased with heating temperature when TiN was used for barrier metals. In contrast to TiN, the leakage current was almost constant regardless of heat cycle temperature for WN barrier metals. XPS and SIMS showed that the atomic Ta and O were diffused to TiN films after heating at 950°C , and that oxygen was also observed in TiN films. But the atomic oxygen and tantalum was not observed in WN films. The void was found in Ta_2O_5 films due to loss of Ta and O atoms after heating at 950°C for TiN/ Ta_2O_5/SiN structure. In addition, the interface roughness between Ta_2O_5 and TiN was increased after heating. But the void was hardly observed in Ta_2O_5 films when WN barrier metals was used. Therefore, the interface roughness and diffusion of tantalum and oxygen atoms from Ta_2O_5 to TiN cause the increase in leakage current of W/TiN/ Ta_2O_5 structure. In contrast to TiN, the barrier of WN prevents the diffusion of both Ta and O atoms to WN. It is noteworthy that the capacitance of Ta_2O_5 capacitors was almost constant in both WN and TiN regardless of heating temperature. In conclusion, the WN shows superior barrier properties in W/WN/ Ta_2O_5 MOS capacitors than TiN.

9:45 AM C3.6
MICROSCOPIC MECHANISM FOR THE ENHANCED DIFFUSION OF BORON IN FLUORINATED SILICON DIOXIDE, SILICON NITRIDE AND SILICON OXYNITRIDE ALLOYS. Hong Yang, Gerald Lucovsky, North Carolina State Univ., Raleigh, NC; Richard B. Fair, Duke Univ., Durham, NC.

In a previous publication [1], a model for B-transport through SiO_2, Si_3N_4 and silicon oxynitride alloys was developed in which the transported species were singly-ionized B-ions, B^+. In this model, transport through Si-SO_2 is by a hopping process where dative bonds are formed between B^+. ions and non-bonding pairs on the O-atoms of the Si-O_2 network. The activation energy for diffusion includes the energy of ion formation as well as the effective trap depth of the hopping sites. Ab initio calculations on small molecular clusters were used to obtain bond-lengths and bond energies for these B^+-oxonium centers. The model has explained suppression of B-transport in Si_3N_4 and silicon oxynitride alloys through an increased binding energy of more than 1.2 eV between B^+ and N relative to B^+ and O. In this model, transport of B^+ through Si-oxynitride alloys parallels charge carrier transport by a shallow-trap controlled drift mobility in the presence of deep traps. The O-atoms provide a percolation path for the trap controlled transport, and the N-atoms act as deep traps that immobilize the B-atoms. The model has been extended to include changes in the B^+ binding energies associated with introduction of F-atoms into the oxides and oxynitride alloys. Next-nearest neighbor F-atoms bonded to Si were found to decrease the binding energy of B^+ at O atoms by $\sim$0.8 eV and at N atoms, by $\sim$0.7 eV. These decreases explain enhanced transport of B in oxynitride alloys that contain bonded F-atoms, and are in good agreement with the experimentally determined reductions of $\sim$0.6-0.7 eV for transport activation energies. The model has also been applied to the transport of As and P in oxynitride alloys, where the binding energies for As and P positive ion attachment to N are increased by $\sim$0.9 eV relative to their attachment to O. Supported by the ONR. AFOSR and SRC
[1] H.Yang et al., J. Vac. Sci. Technol. B 17, 1813 (1999).

SESSION C4: ADVANCED GATE DIELECTRICS
Chairs: Brad Herner and Kyoichi Suguro
Wednesday Morning, April 26, 2000
Salon 5/6 (Marriott)

10:30 AM *C4.1
A CLOSER "LOOK" AT MODERN GATE OXIDES. F.H. Baumann, J. Grazul, C.T. Liu, C.-P. Chang, A. Kamgar, Bell Laboratories, Lucent Technologies, Murray Hill, NJ.

As the thickness of the gate oxide in high performance CMOS devices drops below 3 nm, local thinning on the atomic scale can have detrimental consequences on the reliability of the dielectric. In addition, interfacial roughness at the substrate side and at the poly side of the dielectric constitute an increasing part of the total oxide layer. Using high resolution TEM, we investigated different kinds of process induced 'weak spots' in SiO_2 layers: First, we observed thinning in the periphery of the transistor, i. e. near the boundary to the shallow trench isolation. At the boundary to the shallow trench, the Si substrate gradually changes its orientation from $< 100 >$ to $< 110 >$, which results in an unexpected oxidation behavior in this region. Secondly, we observe the intrusion of poly-Si grains from the gate into the gate oxide, resulting in local thinning of the dielectric. Electrical data suggest that theses effects are responsible for higher leakage currents and lower reliability of high performance transistors.

11:00 AM C4.2
CHARACTERIZATION OF ULTRATHIN INTERFACES (TOX<1.0NM) IN OXIDE-NITRIDE STACK FORMED BY REMOTE PLASMA ENHANCED CHEMICAL VAPOR DEPOSITION. Zhigang Wang, Shengqiang Wang, Wenmei Li, Chad Young, Robert T. Croswell, John R. Hauser, North Carolina State University, Raleigh, NC.

A series of 1.5nm to 2.7nm Oxide-Nitride (ON) gate stack metal-insulator-semiconductor (MIS) capacitors were fabricated with Remote Plasma grown interface oxide thicknesses of 0.5nm to 1.7nm. The ON gate stacks were fabricated both with fixed oxidation time and varying nitride deposition time and with varying oxidation time and fixed nitride deposition time. The interface oxides were fabricated by two different techniques, each designed to incorporate a little nitrogen into the interface oxide: Remote Plasma Oxidation with nitrous oxide (N2O) or Remote Plasma Oxidation with oxygen (O2) followed by an N2 plasma anneal at various pressures. High-frequency capacitance-voltage (C-V) measurements have been made on these ultrathin ON MIS capacitors, and the total electrical equivalent oxide thicknesses (Tox) of those ON stacks are extracted from NCSU C-V model. By using linear regression analysis on the ON gate stack data, nitride deposition rate was obtained. Then, the interfacial oxide thicknesses were extracted by subtracting the calculated Tox of the upper nitride layer from the measured Tox of the ON stack. The physical thicknesses of the oxide and nitride layers are confirmed by HRTEM images and compared with C-V extracted equivalent oxide thicknesses. Furthermore, it was shown that the tunneling currents of 1.8 nm ON stacks fabricated with N2O interface oxide and O2 interface oxide followed by 0.3 Torr N2 plasma anneals are comparable.

11:15 AM C4.3
SIGNIFICANT REDUCTION OF LEAKAGE CURRENT IN THE $Al/TiO_2/CeO_2/Si$ STRUCTURE WITH THE CeO_2 INTERMEDIATE LAYER. Geunhag Bae, Youngil Song, Donggeun Jung, Sungkyunkwan Univ, Dept. of Physics, Suwon, SOUTH KOREA; Yonghan Roh, Sungkyunkwan Univ., Dept. of Electrical and Computer Engineering, Suwon, SOUTH KOREA.

Chemical vapor deposited (CVD) TiO_2 films have attracted much interest as a potential high-k gate dielectric because of the higher dielectric constant than that of SiO_2. However, CVD TiO_2 thin films suffer from the high leakage current. In this work, we report significant reduction of leakage current by inserting CeO_2 intermediate layer between TiO_2 and Si. CVD TiO_2 films were deposited on Si(100) or CeO_2/Si(100) substrates using titanium (IV) isopropoxide ($Ti(OCH(CH_3)_2)_4$), and oxygen as precursors. Spectroscopic ellipsometry (SE) has been used to determine refractive indies, extinction coefficients, and thicknesses of TiO_2 and CeO_2 films. Post deposition treatment was performed in O_2 ambient by rapid thermal annealing (RTA). The thickness of TiO_2 was 20 nm and that of CeO_2 was in the 3-9 nm regime. The $Al/TiO_2/Si$ or $Al/TiO_2/CeO_2/Si$ capacitors were fabricated for capacitance-voltage (C-V) and current-voltage (I-V) characterization. Before annealing, both $TiO_2/CeO_2/Si$ and TiO_2/Si structures showed high leakage current. At a gate bias of -2 V, the leakage current density of the untreated TiO_2/Si or $TiO_2/CeO_2/Si$ sample was in the range of 10^{-1}-10^{-2} A/cm^2. After RTA treatment, the TiO_2/Si structure showed only slight improvement of leakage current characteristics compared to the untreated TiO_2/Si structure. However, in case of the RTA treated $TiO_2/CeO_2/Si$ structure, the leakage current was significantly reduced compared to the untreated $TiO_2/CeO_2/Si$. At a gate bias of -2 V, the leakage current density of the RTA treated $TiO_2/CeO_2/Si$ film was in the range of 10^{-7} A/cm^2. The CeO_2 thickness of the $TiO_2/CeO_2/Si$ structure did not affect leakage current reduction significantly.

11:30 AM C4.4
LOW-OXYGEN NITRIDE LAYERS PRODUCED BY UHV AMMONIA NITRIDATION OF SILICON. Mark A. Shriver, T.K. Higman, S.A. Campbell, Department of Electrical and Computer Engineering, University of Minnesota, Minneapolis, MN; Charles J. Taylor, Jeffrey Roberts, Department of Chemistry, University of Minnesota, Minneapolis, MN.

If chemically vapor deposited high permittivity materials such as TiO_2 and Ta_2O_5 are to gain wide acceptance as alternatives to SiO_2 gates in silicon MOSFETs, the interface between the deposited high-K material and the silicon must be abrupt and have a low density of electrically active defects. Unfortunately, the process for depositing these materials often produces an unacceptably thick, low-permittivity amorphous layer at the interface, which reduces the effectiveness of the high-K material and often contains unacceptably large numbers of charge states. One way to prevent this layer from forming is to deliberately introduce a very thin layer of Si_3N_4 to act as a diffusion barrier prior to deposition of the high-K material. Previous work has shown nitrides to have high concentrations of traps and interface states, but these films also had considerable oxygen contamination, particularly at the nitride / silicon interface. In this paper we show that direct thermal nitridation of the silicon surface in ammonia can provide a low interface state density surface that is also an excellent diffusion barrier. A key feature of this process is the various techniques needed to obtain very low oxygen incorporation in the Si_3N_4. Even at the Si_3N_4 / silicon interface, the oxygen content was below detection limits (0.5%). The nitride films were grown in a range of temperatures that resulted in self-limited thicknesses from a few monolyers to a few nanometers. These films were then characterized by Auger, Time-of-Flight SIMS, and in the case of the thicker films, capacitance-voltage techniques on both n- and p-type silicon substrates. The data shows very low levels of oxygen contamination in the nitride films and low interface state densities in capacitors fabricated from this material.

11:45 AM C4.5
LOW TEMPERATURE NITRIDATION OF SiO_2 FILMS USING A CATALYTIC-CVD SYSTEM. Akira Izumi, Hidekazu Sato and Hideki Matsumura, JAIST (Japan Advanced Institute of Science and Technology), Ishikawa, JAPAN.

Nitrided silicon-oxide and oxynitride films are useful for making high-quality metal-oxide-semiconductor gate insulators to suppress boron penetration and hot-carrier damage. Such films should be prepared at low temperatures without plasma enhancement to suppress dopant diffusion and plasma damage. In this work, we propose a low-temperature plasma-less SiO_2 nitridation technology applying gas-decomposition reaction in a catalytic chemical vapor deposition (Cat-CVD) system. In this method, deposition gases are decomposed by catalytic cracking reactions with heated catalyzer placed near substrates, and so that, films are deposited at low temperatures without help from plasma nor photochemical excitation. An NH_3 gas was used for surface nitridation of SiO_2. The gas pressure during nitridation was about 8 mTorr. The flow rate of NH_3 was 50 sccm and nitridation time was 60 min. The substrate temperature was kept at about 300°C and the tungsten catalyzer temperature was kept at 1800°C. XPS measurements revealed that the peak of N(1s) spectrum appeared obviously and nitrogen related peak of Si(2p) was also observed after the nitridation treatment. The results indicate that the surface of SiO_2 was nitrided as low as 300°C. Electrical properties such as I-V and C-V of nitrided films will be presented.

SESSION C5: INTEGRATION ISSUES IN THE FEOL
Chairs: Jorge Kittl and Gene Lucadamo
Wednesday Afternoon, April 26, 2000
Salon 5/6 (Marriott)

1:30 PM *C5.1
INTEGRATION CHALLENGES FOR ADVANCED SALICIDE PROCESSES AND THEIR IMPACT ON CMOS DEVICE PERFORMANCE. Karsten Wieczorek[1], Manfred Horstmann[1], Hans-Juergen Engelmann[1], Akif Sultan[2]. [1]AMD Saxony Manufacturing GmbH, Dresden, GERMANY; [2]AMD-Motorola Alliance Logic Development, Austin, TX.

High performance state-of-the-art logic products demand salicide processes that support ever increasing operation frequencies as well as

high product yield. Currently, $TiSi_2$ and $CoSi_2$ are the materials of choice in high volume CMOS manufacturing. In this presentation, self-aligned $TiSi_2$ and $CoSi_2$ processes will be presented and compared with focus on scalability, device- and product-performance as well as manufacturability. It will be shown that $TiSi_2$ reaches its scalability limitations despite the use of pre-amorphization implant (PAI) techniques at about 0.18μm physical gate-length. In additon, the impact of RTA salicide formation temperatures as well as the use of different PAI implant species and their impact on performance and parametrical yield will be discussed. Judging from parametrical data and TEM analysis, PAI will particularly lead to a less manufacturable process sequence and to degraded devices. To overcome the obvious limitations associated with the integration of $TiSi_2$, an advanced $CoSi_2$ process will be presented in detail. The $CoSi_2$ process yields excellent device performance down to at least 90nm physical gate length with sheet resistance roll off curves indicating stable $CoSi_2$ sheet resistances of $\sim 6\Omega$/Sq. The impact on device- and product-performance as well as on yield of different $CoSi_2$ formation-sequences varying pre-deposition cleaning procedures, initial Co-Thickness, RTA formation cycles and capping layers will be presented. The $CoSi_2$ process will be characterized by means of both parametrical data as well as high-resolution cross-sectional TEM- and EFTEM analysis. $CoSi_2$ processes using optimized initial Co thickness and RTA cycles yield significanly improved device-speed, judging from ring oscillator delays. Both junction leakage sensitivity to initial Co thickness as well as parasitic junction capacitances can be significantly improved by using additional graded junction implants. In summary, optimized $CoSi_2$ processes exhibit superior scalability and device-parametrics as compared to $TiSi_2$ for gate-length at 0.18μm and below.

2:00 PM C5.2
INTEGRATION ISSUES IN EFFECTIVE REMOVAL OF SiON ANTI REFLECTIVE COATING USED IN DEEP SUBMICRON CMOS GATE LAYER DEFINITION. Sagar A. Kekare, Doris M. Hayes, Gurvinder Jolly, David J. Howard, James T. Nugent, Chinh T. Nguyen, Conexant Systems, Newport Beach, CA.

Use of inorganic anti-reflective coating (ARC) in gate definition for deep sub-micron CMOS fabrication poses several process integration challenges. This paper reports on some of the cross module issues that need to be considered while optimizing the removal of silicon oxynitride inorganic ARC (SiON), following the gate etch. Majority of the effort is focused on reliability of gate dielectric along gate edge and efficiency of silicide formation on top of the gate electrode, in light of the old versus the modified removal scheme. The work entailed in this paper tries to evaluate the wet etching of SiON using hot phosphoric acid. The effect of oxygen content of SiON films on etch action of hot phosphoric acid is discussed. Surface treatment that prevents DUV resist footing is discussed in detail for the impact it causes on efficiency of this wet removal scheme. A physical model of the removal process is presented based on a range of experimental observations. A modified scheme for wet removal of SiON is arrived at based on this model. The experimental results with this modified scheme are presented. The morphological and chemical aspects of the removal sequence are studied in depth using ellipsometry, SEM, AFM, and SIMS. Overall impact of the modified removal scheme on device performance is summarized from study of diverse electrical parameters like time-zero dielectric breakdown (TZDB), silicide sheet resistance and contact resistance.

2:15 PM C5.3
DEVELOPMENT OF A POST-SPACER ETCH CLEAN TO IMPROVE SILICIDE FORMATION. Edward K. Yeh, Samit S. Sengupta and Calvin T. Gabriel, Philips Semiconductors, San Jose, CA.

The formation of a uniform, low-resistance silicide is dependent on the contamination level of the silicon surface upon which the Ti or Co is deposited. Contamination may be in the form of embedded carbon and fluorine residues from previous processing steps, such as the LDD spacer etch. The extent to which the spacer etch contributes impurities can be determined by making contact angle measurements, that is measurement of the angle formed by a droplet of water placed on the wafer surface. A clean silicon surface provides a contact angle of $> 70°$, whereas a contaminated silicon surface produces contact angles down to only a few degrees. By using contact angles as a metric, a post-spacer etch clean was developed to remove impurities from the silicon surface without significant gate or junction loss. This clean entails the use of a CF_4/H_2O plasma to treat the wafer directly after spacer etch. The clean process was then evaluated by the formation of a blanket Ti silicide and measuring sheet resistance. By using such a clean, a Ti silicide sheet resistance comparable to that formed on virgin silicon wafers was obtained on wafers that experienced the spacer etch. For comparison, wafers that were subjected to the spacer etch but not the post-spacer clean yielded a higher sheet resistance. Additional study of the post-spacer etch clean process revealed that oxide on the wafer (even the small amount formed during an O_2-based ash process) can prevent the CF_4/H_2O plasma from cleaning the surface, perhaps by blocking H from extracting C and other contaminants from the silicon surface. Co silicide formation is even more sensitive to surface impurities than Ti silicide. Using the same post-spacer etch clean, a uniform, low-resistance Co silicide has been achieved.

2:30 PM C5.4
A TWO-STEP SPACER ETCH FOR HIGH-ASPECT-RATIO GATE STACK PROCESS. Chien Yu, Rich Wise[a], Anthony Domenicucci, IBM Microelectronics, East Fishkill, NY. [a]DRAM Development Alliance IBM/Infineon

Silicon nitride spacer is widely used as the main insulating layer around gate stack to prevent WL to BL shorts in DRAM technology. A highly selective nitride etch is desirable to minimize sidewall oxide erosion and to prevent punchthrough. Stable remaining sidewall oxide and spacer profile are essential to the formation of well-controlled diffusion and Leff. Since the 0.25um generation we have developed and implemented a highly selective nitride etch based on methyl fluoride chemistry with selectivity to oxide at 10:1. This process allows us to achieve almost no loss of sidewall oxide after spacer nitride etch. However, as ground rule decreases and gate stack aspect ratio increases, there is an increasing foot at the base of the spacer with single-step etch. At 0.175um technology it began to impact the device performance. We have since developed a new two-step etch scheme to resolve the profile control problem. Be applying a non-selective fast etch prior to the selective etch we are able to produce straight spacer profile as indicated in the TEM images, and with very stable remaining sidewall oxide as shown in the SPC charts over many different jobs from two different etch chambers. A similar two-step etch scheme is also developed for logic gate stack spacer etch where much thicker spacer is required.

2:45 PM C5.5
DEEP-SUBMICRON TRANSISTORS WITH ELEVATED SOURCE/DRAIN EXTENSION REGIONS FABRICATED BY DUAL-GATE CMOS TECHNOLOGIES. Kohei Sugihara, Naruhisa Miura, Taisuke Furukawa, Takumi Nakahata, Yuji Abe, Shigemitsu Maruno and Yasunori Tokuda, Mitsubishi Electric Co, Advanced Technology R&D Ctr., Hyogo, JAPAN.

In scaling-down of MOSFET's, the influence of the parasitic series resistance in the source/drain (S/D) regions is becoming one of the most serious obstacles in improving the device performance, since the channel resistance decreases with reduction of a gate length. Recently, the elevated S/D technology with Si epitaxial growth technique has attracted attention in S/D engineering to realize the shallower junction and lower resistivity at deep S/D regions. In this work, we investigated the short channel characteristics, drivability, and parasitic resistance of P- and N-MOSFET's with partially elevated S/D extension regions, which were fabricated by deep-submicron dual-gate CMOS technology combined with the selective Si epitaxial growth. The results revealed that the drivability is appreciably improved as a result of the parasitic resistance reduction while keeping the short channel characteristics, which suggests the possibility of enlarging silicided S/D regions in the future, and that the improvement by the S/D elevation is more remarkable for the P-MOSFET's than the N-MOSFET's.

3:00 PM C5.6
DIFFUSION OF Co DURING Si WAFER PROCESSING. Janet L. Benton, Thomas Boone, Dale C. Jacobson, Conor S. Rafferty, Joseph M. Rosamilia, Bell Laboratories, Lucent Technologies, Murray Hill, NJ; Steven R. Weinzierl, Bao Vu, KLA-Tencor, Milpitas, CA.

The introduction of Co silicide into the process flow for Si integrated circuit manufacturing has necessitated a thorough understanding of the effect of Co contamination on the electrical properties of both Si and SiO_2. In these experiments, Co was intentionally introduced into the Si by two methods; either 1MeV ion implantation at doses of 1×10^{11} cm^{-2} or 1×10^{12} cm^{-2} into the backside of the wafers, or by dipping into a Co solution. Quantox corona-oxide-semiconductor characterization and TXRF were used for analysis of metal diffusion during furnace heat treatments. The Co diffused, at either 650°C or 1000°C for 30 minutes, from the back of the wafers to kill carrier recombination lifetime throughout the bulk Si. P/p+ epitaxial wafers gettered the Co, so that the near surface lifetime in the epitaxial layers remained high even after contamination. There was no evidence of Co migration from the surface of wafers to adjoining wafers during furnace heat treatments, 900°C, 30 minutes. Co diffused through 40Å, 100Å, or 1000Å SiO_2 into bulk of Si. Co contamination introduced after oxide growth did not effect electrical properties of the oxides, i.e. Qbd, Dit or oxide tunneling voltages.

SESSION C6: NOVEL SILICIDE PROCESSING

Chair: Paul R. Besser
Wednesday Afternoon, April 26, 2000
Salon 5/6 (Marriott)

3:30 PM *C6.1
SILICIDES FOR 0.13 UM TECHNOLOGIES AND BEYOND.
Karen Maex, IMEC, Leuven, BELGIUM. Also at E.E. Dept., K.U.-Leuven, BELGIUM.

$CoSi_2$ has replaced $TiSi_2$ for many technologies at the moment. The question remains, how scalable the $CoSi_2$ process is for the future advanced technologies. Even though it has been demonstrated to be feasible down to 100nm dimensions on poly-runners, it remains to be proven, whether the process windows in the silicidation process provide enough latitude to achieve a high yielding, robust process. NiSi has been presented several times as a possible alternative. Besides its advantage of reduced Si consumption, it carries, however, some unsolved issues for instance in its phase formation sequence. In this paper, the process window of the $CoSi_2$ process will be discussed when scaling down the dimensions. The issue whether or not NiSi will provide a better alternative will be illustrated and the intriguing question whether there are other silicides around that can outperform a scaled $CoSi_2$ process will be opened.

4:00 PM C6.2
IMPROVEMENT OF COBALT SILICIDE STABILITY USING NITROGEN IMPLANTATION THROUGH Co MONOSILICIDE.
Dong Kyun Sohn, Ji-Soo Park, Jong-Uk Bae and Jin Won Park, ETRI, Taejon, KOREA.

For sub-quarter micron CMOS, dual gate is a key technology to realize high performance MOS devices. Recently, gate electrode usingsmall-grain size poly-Si to dope simultaneously with gate and source/drain has been reported for suppression of gate depletion. However, the thermal stability of Co silicide on fine grain sized poly-Si has not been much studied. In this paper, we will present the effect of gate Si structure on formation and thermal stability of Co silicide on 0.18 micron patterned line. The structure featured amorphous, small, medium and large grain sized poly-Si was controlled by deposition temperature. The salicide process was performed by 2-step anneal method using Ti capping technology. After first RTA and selectively removal process were performed, Co monosilicide was fomred. Then, nitrogen atoms were implanted on monosilicide at 50 $\sim$ 80 keV with 5e14 $\sim$1E15 cm^2 followed by second RTA. The formation temperature and thermal stability of conventional Co silicide increased with grain size of poly-Si. That is, the thermal stability of Co silicide on fine grain sized poly-Si and amorphous Si was greatly deteriorated. The reason is caused by the abnormal high diffusivity of Co atoms during salicidation, which results in irregular formation of Co silicide on fine grain sized poly-Si . To improve the thermal stability without degradation of sheet resistance, nitrogen ions were implanted through Co monosilicide. The thermal stability was greatly improved. In case of the projected ion energy 80 keV located far from the interface of CoSi/poly-Si, the sheet resistance of Co silicide showed constant value after annealing up to 1000°C for 30 s, while conventional Co silicide on fine poly-Si showed thermal stability limit at 850°C. A SIMS profile indicated that the implanted nitrogen atoms segregated at gate oxide interface and acted as diffusion barrier of Co atoms. It was also found that the nitrogen implantation through Co monosilicide can be successfully used for sub-quarter micron dual gate CMOS devices.

4:15 PM C6.3
IN SITU AND EX SITU MEASUREMENTS OF STRESS EVOLUTION IN THE COBALT-SILICON SYSTEM.
G. Lucadamo[a], C. Lavoie, C. Cabral, Jr., R.A. Carruthers, J.M.E. Harper, [a]Lehigh University, Dept. of Materials Science and Engineering, Bethlehem, PA; IBM T.J. Watson Research Center, Yorktown Heights, NY.

The potential use of cobalt silicides as contacts in sub 0.25 micron CMOS devices holds promise for increased performance over titanium silicide metallurgy. Successful integration with current salicide processes may depend on the final stress state of the silicide. The formation of high stresses during processing could introduce defects, such as dislocations, that would be detrimental to device operation. In this study, the biaxial stress of Co / Si thin-films is investigated by measuring wafer curvature during deposition and subsequent annealing. Films are deposited by UHV magnetron sputtering at room temperature on (100)Si and poly-Si substrates. Cobalt thicknesses of 35 nm and 100 nm are chosen to provide sufficient stress (curvature) to enable an accurate measurement. Results indicate that the stress in the as-deposited Co film is tensile and fairly uniform through the layer ($\sim$0.7 GPa on Si (100) and $\sim$0.5 GPa on poly-Si). In addition, the stress evolution is measured during silicide formation under constant heating rate conditions (10°C/s) from room temperatures up to 700°C. Several stress transitions are observed that correlate with Co_2Si, CoSi, and $CoSi_2$ phase formation. Interpretation of these transitions is supplemented using resistance, X-ray diffraction and light scattering measurements, all performed in situ. After the reaction, the room temperature stress in the $CoSi_2$ phase is $\sim$1 GPa (tensile) in the films deposited on Si(100) and $\sim$1.5Gpa (tensile) in the films deposited on poly-Si. In both types of samples, the tensile stress is a result of the higher thermal expansion coefficient of $CoSi_2$ relative to the Si substrate. The higher tensile stress in the poly-Si sample is attributed to the growth of the Si grains during annealing.

4:30 PM C6.4
STRESS BUILD-UP DURING THE Ni-SILICIDATION IN AND AROUND NARROW NiSi LINES.
An Steegen[a], Muriel de Potter[a], Ingrid De Wolf[a], Karen Maex[a,b]. [a]IMEC, Leuven, BELGIUM, [b]Electrical Engineering Department, K.U.-Leuven, BELGIUM.

Recently, several studies about NiSi have demonstrated that NiSi is a promising silicide for sub-micron CMOS process technologies. NiSi has several advantages: a low resistivity, no doping dependency during the reaction, no narrow runner degradation, a wide temperature window and a high resistance to HF solutions. This paper focuses on the in situ stress build-up in NiSi films, on the local mechanical stress in the Si-substrate near narrow NiSi lines and on the influence of a mechanical stress on the NiSi-$NiSi_2$ transformation. This local mechanical stress is studied by using micro-Raman spectroscopy in combination with simulations by finite element modeling. Previous work has already shown that the difference in material properties between $TiSi_2$ and $CoSi_2$ yields different stress levels in the Si-substrate; $TiSi_2$ induces almost twice as much stress than $CoSi_2$ [1]. It will be shown that NiSi induces even less stress than $CoSi_2$ in narrow lines. [1] A. Steegen, K. Maex, I. De Wolf, IEEE Symp. on VLSI Techn., p.200, 1998.

4:45 PM C6.5
FORMATION AND ELECTRICAL TRANSPORT PROPERTIES OF NICKEL SILICIDE SYNTHESIZED BY METAL VAPOR VACUUM ARC ION IMPLANTATION.
XingWang Zhang, Sai Peng Wong, Wing Yiu Cheung, The Chinese University of Hong Kong, Department of Electronic Engineering, Hong Kong, PR CHINA.

Nickel silicide has attracted widespread interest as a contact and interconnect material for silicon based microelectronic devices because of its low electrical resistivity, high chemical resistivity and good thermal stability. Over the last two decades, various techniques, such as ion implantation, solid-state reaction and ion-beam mixing of nickel overlayers on Si substrates, have been reported to synthesize nickel siliside. In this paper, metal vapor vacuum arc (MEVVA) ion source implantation was employed to synthesize $NiSi_2$ on Si substrates. The implantation was performed at an extracted voltage of 65 kV at various beam currents to doses ranging from $2\times 10^{-17} cm^{-2}$ to $8\times 10^{-17} cm^{-2}$. The characterization of the as-implanted and annealed samples was performed using Rutherford backscattering spectrometry (RBS), x-ray diffraction (XRD), electrical and Hall effect measurements. Effects of the preparation parameters on the composition, structure and electrical properties of $NiSi_2$ layers were investigated systematically. The electrical properties of the samples prepared under different implantation conditions were found to be remarkably different, depending on whether isolated $NiSi_2$ islands or a continuous $NiSi_2$ layer are formed. It is shown that continuous $NiSi_2$ layers with good crystal quality and low resistivity can be formed by suitable implantation and annealing conditions.
This work is partially supported by the Research Grants Council of Hong Kong (Ref. No.: CUHK 4405/99E

SESSION C7: POSTER SESSION

Chairs: Larry A. Clevenger and Stephen A. Campbell
Wednesday Evening, April 26, 2000
8:00 PM
Salon 1-7 (Marriott)

C7.1
A STUDY ON THE FORMATION OF POLY $Si_{1-x}Ge_x$ FILMS AND THEIR ELECTRICAL PROPERTIES AS A GATE ELECTRODE MATERIAL FOR ULSI CMOS STRUCTURES.
Sung-Kwan Kang, Dae-Hong Ko, Yonsei Univ, Dept. of Ceramic Engineering, Seoul, KOREA; Tae-Hang Ahn, Tae-Kyun Kim, In-Seok Yeo, Hyundai Electronics Industries Co. Ltd., Kyungki-do, KOREA; In-Kyu Chun, Sung-Jin Whoang, Doo-Young Yang, Chul-Joo Whang, Ju-sung Co. Ltd., Kyungki-do, KOREA.

Polycrystalline $Si_{1-x}Ge_x$ films have been suggested as a promising alternative to the currently employed poly-Si gate electrode for CMOS technology since poly $Si_{1-x}Ge_x$ gate materials show a lower resistivity than the poly-Si, and also their workfunction can be controlled by changing the Ge content in the films. We investigated

the formation of poly $Si_{1-x}Ge_x$ films grown by UHV CVD using Si_2H_6 and GeH_4 gases, and studied their physical properties as well as electrical characteristics using TEM, XRD, RBS, XPS, and SIMS as well as C-V, I-V, and 4-point probe measurements. The deposition process was performed at the temperature range between 575°C and 625°C. The films with Ge content from 0% to 45% were obtained by changing the flux of the GeH_4 gas. In order to reduce the incubation time for the formation of the films, we employed 10nm-thick poly-Si seed layer prior to the deposition of $Si_{1-x}Ge_x$ films. The Ge content of the $Si_{1-x}Ge_x$ films increased linearly with the flux of the GeH_4 gas up to x=0.3, and saturated above x=0.45. The deposition rate of the $Si_{1-x}Ge_x$ films increased linearly with the flux of the GeH_4 gas upto x=0.1, above which it is slightly changed. The grain size of the $Si_{1-x}Ge_x$ films increased with the increase of the process temperature as well as the Ge content. The resistivity of the $Si_{1-x}Ge_x$ films decreased as the Ge content increased, and was about one half of that of poly-Si films at the Ge content of 45%. The C-V measurements of the MOSCAP structures with poly $Si_{1-x}Ge_x$ gates demonstrated that the flat band voltage of the poly $Si_{1-x}Ge_x$ films was lower than that of poly-Si films by 0.2V, and show less gate-poly-depletion-effect than that of poly-Si gates.

C7.2

A LOW-COST BiCMOS PROCESS WITH METAL GATES.
Henk van Zeijl, Delft Institute of Microelectronics and Submicron Technology, Delft, THE NETHERLANDS.

Scaling BiCMOS technology in generally will increase the process complexity. This work proposes a different device architecture that reduces process complexity, featuring high frequency BJTs and MOS devices with metal gates. The source and drain are formed first followed by gate dielectric and gate metal. In this way the thermal budget of Source-Drain formation is uncoupled from gate stack formation which give extra freedom gate stack engineering. Furthermore by forming the gate in a window with inward spacers, sublithographic dimensions can be obtained. The process commences with the deposition of polysilicon on 20 nm silicon oxide. This polysilicon (SD-poly) is heavily doped by ion implantation and will serve as Source-Drain contacts and as extrinsic base of the NPN BJT. Subsequently a nitride layer is deposited on the SD poly followed by a gate window definition in which the nitride and the poly are etched. The silicon oxide under the SD poly is under etched and the cavities under the poly are filled with a polysilicon deposition. The excess polysilicon is removed leaving polysilicon plugs under the highly doped SD-poly. Next nitride spacers are formed followed by a gate window oxidation. In the NPN BJT the gate oxide is removed and the gate window is implanted with arsenic and boron forming the emitter and base respectively. One thermal anneal, applied to diffuse source and drain contacts from the polysilicon, is also used to activate the emitter and base of the NPN. Finally metallization with Al/Si (1%) forming the gate material and the emitter contact complete the devices. The measured cut-off frequency and maximum frequency of oscillation of the NPN BJT is 13 GHz and 20 GHz respectively. For the MOS devices subthreshold slopes of less than 83 mV/decade are obtained, the off currents are less than 1 pA/micron and the threshold voltage is about 0.7 Volt.

C7.3

EFFECTS OF NITRIDATION BY N_20 OR NO ON THE ELECTRICAL PROPERTIES OF THIN GATE OR TUNNEL OXIDES.
C. Gerardi, T. Rossetti, V. Triolo, M. Melanotte, Central R&D, STMicroelectronics, Catania, ITALY; I. Crupi and S. Lombardo, CNR-IMETEM, Catania, ITALY; M. Alessandri, Central R&D, STMicroelectronics, Agrate, ITALY; S. Nesso, Applied Materials, Catania, ITALY.

Nitridation of thin oxides obtained by annealing with nitrous oxide (N_2O) and nitric oxide (NO) is used in CMOS-ULSI technology to improve dielectric reliability. These processes are attractive due to their simplicity and to the absence of hydrogen which is known to generate electron traps. Also, nitridation is investigated with the purpose of reducing stress induced leakage current (SILC) effects which are of great concern in non-volatile memories. It has been reported that nitridation processes are characterized by nitrogen location at the SiO_2/Si interface in a very thin region which has a thickness comparable with the one of the structurally imperfect transition SiO_2 layer near the interface . However it is not clear which is the influence of this treatment on the current flowing across the oxide during electron injection from the nitrided interface. We have studied the effects of nitridation on the current flowing across the oxide in the Fowler-Nordheim regime finding a correlation with the amount of the nitrogen build-up at the interface. The experiments have been performed on thin oxides grown either by wet or dry oxidation and subjected to N_2O or NO nitridation. In addition a comparison of the various processes in view of reducing SILC effects will be reported.

C7.4

CHARACTERIZATION OF $Ti(SiGe)_2$/SiGe AND $(TiNb)Si_2$/Si CONTACTS: MEASUREMENT AND TWO-DIMENSIONAL MODELING.
J. Åberg, S. Persson, P.-E. Hellberg, KTH, Department of Electronics, Kista, SWEDEN; W. Kaplan, ACREO AB, Kista, SWEDEN; S.-L. Zhang, KTH, Department of Electronics, Kista, SWEDEN; U. Smith, Ericsson Components AB, Kista, SWEDEN.

The metal-semiconductor contact was characterized electrically for two different systems, $Ti(SiGe)_2$-SiGe and $(TiNb)Si_2$-Si. The formation of the germano-silicide in the former system and the Ti-Nb silicide in the latter system was realized using the conventional self-alignment technique involving the use of rapid thermal annealing (RTA) in N_2 atmosphere. For the $Ti(SiGe)_2$-SiGe system, p-type SiGe was studied because it gives an extra degree of freedom for threshold voltage design in PMOSFETs. Polycrystalline SiGe films of different compositions ranging from Ge/Si = 0 to 1 were used. The SiGe films, deposited in a low-pressure chemical vapor deposition (LPCVD) reactor at 500-600°C, were in-situ doped with B to a bulk carrier concentration of 1-2 $\times 10^{20}$ cm^{-3}. With regard to the $(TiNb)Si_2$-Si system, the enhanced formation of C54 $TiSi_2$ in the presence of a thin Nb interposed layer prompted a study of the contact to LPCVD polycrystalline Si of both doping types. Focus was placed on the effect of the substrate doping level. In order to accurately control the doping level in the polycrystalline Si layers deposited at 625°C, ion implantation of B and As was used. The doses were chosen to yield a bulk doping concentration of 2×10^{19} - 5×10^{20} cm^{-3}. The formation of germano-silicide/silicide was studied using sheet resistance measurement, x-ray diffraction (XRD), Rutherford backscattering spectrometry (RBS) and atomic force microscopy (AFM). The carrier concentration was determined by means of Hall effect measurements, while the chemical concentration of the dopants was determined using secondary ion mass spectrometry (SIMS). The contact resistance measurements were carried out using cross-bridge Kelvin and tapped-bar transmission-line structures. A two-dimensional model was employed to extract the specific contact resistivity from the measurement results. The electrical results were correlated to the germano-silicide/silicide formation.

C7.5

ULTRATHIN GATE OXIDE PREPARED BY REOXIDATION OF THERMAL Si_3N_4 IN D_2O VAPOR FOR MOS DEVICE APPLICATIONS.
Hyunsang Hwang, Department of Materials Science and Engineering, Kwangju Institute of Science and Technology, Puk-gu, Kwangju, KOREA.

Nitridation of gate oxide in NH_3 has been investigated to improve gate dielectrics integrity. Recently, a new oxynitride process based on the wet reoxidation of thermal nitride was proposed. The reoxidation of thin nitride in H_2O ambient was performed to reduce charge trapping and interface state density. However, reoxidation in H_2O ambient cause excess amount of hydrogen incorporation in gate dielectrics. In this paper, we have investigated the electrical characteristics of oxynitride prepared by reoxidation of thermal nitride in D_2O ambient. Conventional polysilicon gate MOS capacitors with 4.0nm-thick gate oxides were fabricated on n-type silicon wafers. Thermal nitride was formed by rapid thermal annealing in NH_3 at 1050°C for 90s. The thickness of thermal nitride measured by ellipsometer is approximately 3nm. Reoxidations of thermal nitride were performed in D_2O and H_2O ambient at 835°C and 790°C, respectively. For comparison, 4nm-thick wet oxide was grown in H_2O ambient at 790°C. To investigate charge trapping, the gate voltage shift under constant current stress was measured. Compared with H_2O oxynitride, D_2O oxynitride exhibits slightly less hole trapping. The charge-to-breakdown characteristics under the constant current stress was investigated using small area capacitors. The wet oxide and H_2O oxynitride exhibit similar distribution of charge-to-breakdown. In contrast, the D_2O oxynitride provides larger charge-to-breakdown. In addition, compared with H_2O oxynitride, the generation of interface state is slightly less for D_2O oxynitride. In case of the oxynitride formed by D_2O reoxidation, we believe that the dangling bonds at the Si/SiO_2 interface were passivated by deuterium. The improvement of electrical and reliability characteristics can be explained by the deuterium incorporation.

C7.6

THERMAL STABILITY OF HAFNIUM AND HAFNIUM NITRIDE(HfN_x) GATE ELECTRODES ON SILICON DIOXIDE.
G.P. Heuss, North Carolina State University, Department of Materials Science and Engineering, Raleigh, NC; V. Misra, H. Zhong, North Carolina State University, Department of Electrical and Computer Engineering, Raleigh, NC; G. Lucovsky, North Carolina State University, Department of Physics, Raleigh, NC.

Metal and metal nitides are candidates to replace polysilicon as the gate electrodes for CMOS devices with gate lengths less than 100nm. Gate electrodes for these devices must have dopant densities of 10^{22}

cm^{-3}, a workfunction near E_c or E_v to achieve low threshold voltages and thermal stability with the underlying dielectric during subsequent processing. We have investigated the thermal stability of metals and metal nitrides including Hafnium and Hafnium Nitride(HfN_x). Both materials have a workfuction within 0.2eV of the conduction band of silicon which fulfills one of the requirements for the NMOS gate electrode. The metal and reactively sputtered metal nitrides were deposited using DC magnetron sputtering. Annealing of Hf or HfNx gate electrodes on SiO_2 at 400°C or 500°C for 30 mintues in forming gas results in an increase in capacitance equivalent to a dielectric 30% thicker than that measured for the as-deposited gate stack. The gate leakage increases accordingly. Diffusion profiles of metal into the dielectric are measured using Secondary Ion Mass Spectrometry. Interaction of the gate electrode with the dielectric at such low temperatures excludes these films as candidates for use in standard silicon processing where high temperature processing follows gate stack formation.

C7.7

HOT WALL ISOTHERMAL RTP FOR GATE OXIDE GROWTH AND NITRIDATION. A. Laser, J.C. Passefort, E. Vaughan, C. Ratliff, J. Yao, J. Kolk, L. Page, Silicon Valley Group, Thermal Systems Division, Scotts Valley, CA.

A new system that incorporates many benefits of large batch furnaces (high quality films, growth of wet and dry oxides, chlorine capability, low cost) into a single wafer processing module has been developed at SVG Thermal Systems. The problems associated with wafer temperature measurement and control in traditional lamp based RTP systems are avoided by utilizing a hot wall isothermal processing chamber. Unique fixturing is used to minimize thermal stress on the wafer during ramping. High quality gate oxides ranging in thickness from 2nm to 4nm have been grown in this system using both wet and dry oxidation ambients, with and without chlorine. We will present both thermal and process uniformity for these gate oxides. In addition, process uniformity, nitrogen incorporation and reoxidation data for NO and N_2O annealed gate oxides will be reported.

C7.8

TiO_2 FORMATION BY OXIDATION OF SPUTTERED TiN. Hideki Takeuchi, Tsu-Jae King, Chenming Hu, Univ. of California at Berkeley, Dept. of Electrical Engineering and Computer Sciences, Berkeley, CA.

TiO_2 is an attractive alternative gate dielectric because of its higher permittivity as compared to SiO_2 and other dielectrics. In this study, TiO_2 thin films were prepared by furnace oxidation of TiN deposited in a conventional DC magnetron sputter tool. Suppression of oxidation of the Si substrate in order to maintain a small effective gate-dielectric thickness is a key challenge for this process. In this work, methods for forming a SiN diffusion barrier layer at the Si substrate have been studied. Three different pre-treatments (ECR N_2 plasma exposure, RF N_2 plasma exposure, and NH_3 anneal in an LPCVD furnace) prior to TiN sputter deposition, as well as RTA of deposited TiN prior to oxidation, have been examined to form Si-N barrier layers. From high-frequency C-V measurements, this barrier layer was found to play a significant role in preventing diffusion of Ti into the Si substrate. Among the four methods investigated, RTA of TiN resulted in the best barrier properties. By optimizing the Ar/N_2 ratio during sputter deposition and the RTA conditions, Toxeff=4nm was obtained for as-deposited 20nm TiN films. The compatibility of TiO_2 with various gate materials was also examined. While MOS capacitors with Al and WN gates showed good stability after forming gas anneals, drastic decrease in capacitance was observed for TiN-gated capacitors.

C7.9

CONTROLLING $CoSi_2$ NUCLEATION: THE EFFECT OF ENTROPY OF MIXING. Christophe Detavernier, R.L. Van Meirhaeghe, University of Gent, Dept. of Solid State Science, Gent, BELGIUM; K. Maex, IMEC, Leuven, BELGIUM; F. Cardon, University of Gent, Dept. of Solid State Science, Gent, BELGIUM.

It is generally known that nucleation effects strongly influence the CoSi to $CoSi_2$ phase transition. According to classical nucleation theory, the small difference in Gibbs free energy between the CoSi and $CoSi_2$ phase is responsible for the nucleation barrier. Adding elements that are soluble in CoSi and insoluble in $CoSi_2$ will influence the entropy of mixing, and thus change ΔG. In this way, the height of the nucleation barrier may be controlled. By depositing Fe or Ge (respectively replacing Co and Si in the CoSi lattice) in between the Co and the Si substrate, we were able to increase the nucleation barrier. The solubility of Fe and Ge in CoSi is illustrated by the fact that $Co_{1-x}Fe_xSi$ and $CoSi_{1-x}Ge_x$ obey Vegard's law. From the sheet resistance versus annealing temperature plot, it is clear that both Fe and Ge increase the formation temperature of $CoSi_2$ (for 10% of Fe, an increase of about 50 degrees is observed). The nuclei may be observed by phase contrast microscopy. Moreover, once nucleated, the growth of the $CoSi_2$ layer is slowed down. This may be explained by the expelled Fe that precipitates at the $CoSi_2$ grain boundaries, thus slowing down diffusion. For a Co(10nm)/Fe(10nm)/Si system annealed at high temperature, $FeSi_2$ precipitates are observed by XRD. From XRD, we observed an increase in both the $< 111 >$ and $< 220 >$ peak intensity for increasing Fe thickness. This reflects an increase in the $CoSi_2$ grain size. For higher Fe concentration in the mono-silicide, the $CoSi_2$ nucleation will become increasingly difficult. This will result in less nucleation sites than in the normal Co/Si reaction and once formed, the nuclei grow faster, resulting in larger $CoSi_2$ grains. Based on the crystallographic structure of their monosilicide, Mn, Ru, Rh, Re and Os are expected to have a similar behaviour as Fe.

C7.10

EFFECT OF A THIN Ta LAYER ON THE C49-C54 TRANSITION. F. La Via, CNR-IMETEM, Catania, ITALY; F. Mammoliti, M.G. Grimaldi, INFM and Physics Department, Catania, ITALY; S. Quilici, F. Meinardi, INFM and Material Science Department, Milano, ITALY.

On thermally oxidised 5 inches silicon wafers a 150 nm amorphous silicon layer was deposited in a Ultra High Vacuum chamber by e-gun. After this deposition, without breaking the vacuum, thin layers of Ta and Ti were deposited sequentially. The Ta layer ranged between zero and $4.5 \bullet 10^{15}/cm^2$, as measured by Rutherford Backscattering Spectroscopy. The Ti layer thickness (20 nm) was maintained constant for all the samples. On partially reacted samples, both X-Ray diffraction and Transmission Electron Diffraction analysis show a clear evidence of the C49 formation during the reaction. The activation energy of the transition has been found by in situ sheet resistance for the samples with (3.5 eV) and without Ta (4.5 eV). The transition temperature decrease increasing the Ta amount and, for a tantalum dose of $4.5 \bullet 10^{15}/cm^2$ it reaches a value of about 80°C lower than the temperature necessary to have the transition in a Si/Ti sample. This effect has been related to the increase of the C54 nucleation sites, observed by micro-Raman images.

C7.11

SILICIDATION OF TITANIUM-RICH TITANIUM BORIDE DEPOSITED BY CO-SPUTTERING ON Si(100). G. Sade and J. Pelleg, Ben-Gurion University of the Negev, Department of Materials Engineering, Beer-Sheva, ISRAEL.

Titanium boride is known as a good diffusion barrier, in particular against copper, however outdiffusion of boron might deteriorate the semiconductor device. A $TiSi_2$ sublayer prevents effectively boron penetration into the Si substrate. In this study the intention was to form a $TiB_2/TiSi_2$ bilayer film by silicidation of a titanium-rich titanium boride deposited by magnetron co-sputtering from elemental targets. The $TiSi_2$ formation as well as the redistribution of titanium in the boride layer has been investigated by X-ray diffraction (XRD), Auger depth profiling and cross-sectional transmission electron microscopy (XTEM). Contact structure with Cu metallization was prepared to characterize this structure electrically.
The Ti-rich titanium boride film was completely amorphous by XRD up to 700°C. Crystallization of Ti-rich silicides (Ti_3Si, Ti_5Si_3) has started at 750°C, but already at 800°C the crystallization of C54 $TiSi_2$ was completed. TiB_2 begins to crystallize at 800°C. Sheet resistance measurements confirmed these results. The sheet resistance of the as-deposited film was about 16 $\Omega/\square$ and no significant change was detected up to 700 ° C. Then, a remarkable drop in the sheet resistance to $\sim$1 $\Omega/\square$ was obtained after 800°C, and this value was actually unchanged up to 925°C. Cross-sectional TEM revealed the formation of the C54 $TiSi_2$ layer between TiB_2 and Si and additionally, a second C54 $TiSi_2$ layer was observed within the boride film. Current-voltage measurements of the prepared contact structure showed that it was a Schottky diode with very high leakage current.

C7.12

EFFECT OF RETAINED SILICON ON THE THERMAL STABILITY OF C54-$TiSi_2$ THIN FILMS GROWN ON SiO_2. Dongwoo Suh, Hong Seung Kim and Jin-Yeong Kang, Dept. of Compound Semiconductor, Microelectronics Technology Lab., Electronics and Telecommunications Research Institute, Taejon, KOREA.

For the mechanistic understanding of thermal instability of C54-$TiSi_2$ interconnect thin film grown on SiO_2 substrate, we investigated the effect of silicon layer retained at the interface of those. We kept our focus on the very silicon layer by choosing two specimens out of several ones prepared with the same process condition except for the thickness of the silicon layer, which were 90 nm and 140 nm in Specimen-A and -B, respectively. After sputtering Ti layer of 30 nm thick capped with TiN at 650°C, both specimens were followed by rapid thermal anneal (RTA) at 850°C for 30 seconds for polimorphic phase transformation from C49-$TiSi_2$ to C54-$TiSi_2$. The degree of phase transformation were checked up using 4-point probe and X-ray diffraction. The composition profile and cross-sectional microstructure

of the interface were scrutinized using Auger electron spectroscopy (AES) and transmission electron microscopy (TEM). From the results of AES analysis we knew that a silicon layer existed at the interface in Specimen-B whereas retained silicon was hardly detected in Specimen-A where C54-$TiSi_2$ thin film was locally peeled off right after the RTA. The results of TEM analysis were consistent with those of AES analysis for the both Specimens. In particular a lot of Moire fringes, a proof of stress release in thin film, were observed in TEM images of the retained silicon layer in Specimen-B. Given the RTA condition in our study, the thermal stress in Specimen-A was calculated at 1.3 GPa while it was 0.7 GPa in Specimen-B, about a half of that of Specimen-A, showing that a great deal of the thermal stress was released by the retained silicon layer.

C7.13
A STUDY ON THE $CoSi_2$ FORMATION BY USING Ni INTERPOSED LAYER ON Si SUBSTRATE. S.G. Park, J.H. Huh and Hyeongtag Jeon, Division of Materials Science and Engineering, CPRC, Hanyang Univ., Seoul, KOREA.

Metal silicides have received much interest over the years due to their application in microelectronic devices such as contact, gate electrode, and interconnect materials. Among the silicide materials, the $CoSi_2$ has been considered to be one of the most attractive materials for contact and interconnection in next generation devices because of its low resistivity, high thermal stability and process compatibilities. Moreover, the small lattice mismatch with Si is expected to grow a good epitaxial $CoSi_2$. However, the conventional method for the formation of $CoSi_2$ using Co metal alone exhibits many problems, such as the formation of pinholes and rough interfaces due to the nonuniform reaction between Co and Si. To solve these problems, Co/Ni metal bilayer on Si substrate has been suggested in this study. In the case of Ni/Si system, Ni-silicide is formed through the reaction of Ni and Si. At this time, the sequence of Ni-silicide phase formation is Ni_2Si, NiSi, $NiSi_2$ similarly that of Co-silicide. The lattice mismatch of $NiSi_2$ phase to the Si substrate is 0.46%. This value is less than that of $CoSi_2$ phase to the Si substrate(-1.23%). And $NiSi_2$ phase has the same structure of $CoSi_2$ which is the CaF_2 structure. If the $NiSi_2$ phase is uniformly distributed on the Si substrate, it can be expected the formation of epitaxial $CoSi_2$ on the Si substrate. The formed $NiSi_2$ phase will act as a barrier material for Co flux into Si. The reaction between of Co and Si will be retarded by the $NiSi_2$ phase and the $CoSi_2$ phase formed without Co_2Si or CoSi phase. The growth of $CoSi_2$ on the different Si substrate will be also affected by Si surface structure, since the surface structure of Si(100) substrate is different from that of Si(111) substrate. The Ni(5Å - 10Å) and Co(100Å) were sequentially deposited on the Si(100) and Si(111) with a ultra high vacuum dual e-beam evaporation system and followed by furnace annealing from temperatures between 400°C and 800°C with 100°C increments. The phase identification, chemical composition and interface morphology of $CoSi_2$ were characterized by XRD, AES, TEM and a four point probe. The $CoSi_2$ layer with Ni interposed layer on the Si(100) is formed at the lower temperature than that of $CoSi_2$ without Ni interposed layer. The sheet resistance is suddenly dropped at 400°C in the sample with Ni interposed layer. But in the sample with Co only deposited, the sheet resistance is dropped at 500°C. We will discuss the growth of Co-silicide by using the Ni interposed layer on the different Si substrates and the formation sequence of Co-silicide phase based on the thermodynamics and kinetics considerations.

C7.14
THIN Ni-SILICIDES FOR LOW RESISTANCE CONTACTS AND GROWTH OF THIN CRYSTALLINE Si LAYERS. Elena A. Guliants and Wayne A. Anderson, SUNY at Buffalo, Dept. of Electrical Engineering, Buffalo, NY.

Metal silicides as ohmic contacts in Si-based technology continue to be a very topical subject for research. $NiSi_2$ is among the most extensively studied systems because of its perfect thermal stability and small lattice mismatch (0.4%) with Si which makes the Ni disilicide the best suited for the epitaxial growth on a Si substrate. Much effort is focused on the self-aligned silicidation process in which $NiSi_2$ is prepared by Ni deposition on a single crystal Si wafer followed by thermal annealing. We propose a new technological method of producing the Ni silicide with a metal-like conductivity by depositing a thin Si film over an ultrathin Ni prelayer at temperature below 600°C. The interaction of a metallic Ni with Si atoms provided by the deposition source leads to the formation of the Ni-rich silicide phases immediately after the onset of Si deposition. Continued Si deposition results in the transformation of the Ni-rich silicide phases into the more Si-rich ones which implies that the phase composition is controlled by the Ni-to-Si concentration ratio and the diffusion zone thickness rather than temperature. The most favorable $NiSi_2$ phase is formed at temperatures much lower than 700-750°C which was reported for the case of heat treatment of the Ni on c-Si wafer system. After Ni is completely consumed, Si crystals grow epitaxially on the disilicide grains. This technique has advantages in two aspects: provides a high crystallinity Si film and allows fabrication of an ohmic contact directly on the substrate thus leaving the front surface of the film available for the formation of the active device junction. The silicide layer has been studied in detail with respect to both the dynamics of the silicide growth and the resulting interface structure. Questions related to the Ni - Si interdiffuson mechanisms and formation kinetics of particular transition compound phases that nucleate and grow prior to $NiSi_2$ formation will be discussed.

C7.15
RELIABILITY OF REMOTE PLASMA NITRIDED SiO_2 GATE DIELECTRIC GROWN BY AN *IN – SITU* STEAM GENERATION (ISSG) PROCESS. H.N. Al-Shareef, A. Karamcheti, T.Y. Luo, V.H.C. Watt, M.D. Jackson, G.A. Brown, and H.R. Huff , SEMATECH, Inc., Austin, TX; R. Jallepally, D. Noble, and T. Nam., Applied Materials, Santa Clara, CA.

Extensive efforts are currently underway to develop a replacement gate dielectric for conventional SiO_2. It is expected that scaling of SiO_2 thickness will continue down to the 0.15μm technology node. Alternative dielectrics will most likely be needed for the 0.13 μm generation. Examples of these alternative dielectrics currently include a silicon oxide-nitride stack [1] or a nitrided silicon oxide [2]. In this work, we have evaluated the properties and reliability of remote plasma nitrided (RPN) in-situ steam generated oxide (ISSG) as a gate dielectric for the 0.13 μm technology node. Using the RPN process, one can introduce large amounts of [N] into the SiO_2 film while carefully controlling the nitrogen depth profile. This improves SiO_2 resistance to boron penetration and modifies the dielectric constant of the oxide. Excessive amounts of [N] near the Si/SiO_2 interface can, however, lead to mobility degradation.
ISSG oxide films with 1.5-2.1 nm thickness were prepared using an AMAT Centura RTP system with in-situ steam generation capability. The films were grown at 950°C in a 1%H_2 (99%O_2) ambient at 10 Torr. The ISSG oxide films were nitrided in remote high-density N_2 plasma using a N_2/He ratio of 1:4. The RPN temperature was varied between 550-850°C while the RPN process time was either 150 or 240 seconds. Polysilicon gate electrodes were deposited at 720°C in an AMAT RTCVD chamber, clustered to the ISSG chamber.
Electrical performance of the nitrided ISSG oxide was evaluated using MOS capacitor devices. C-V and I-V measurements as well as oxide reliability (including V_{BD}, SILC, Q_{BD}) tests were performed. Initial data indicate that an equivalent oxide thickness (EOT) of 1.6 nm with gate leakage (Jg) around $5x10^{-3}$ A/cm^2 can be achieved. A flatband voltage of $\sim$ -0.80 V is obtained for most samples, which is roughly the expected value for the N^+ poly and p-type substrates used. This indicates good interface quality and negligible fixed charge. The breakdown voltage ranged from 4-5 Volts, depending on the film thickness and RPN conditions. The nitrogen profile in these samples, evaluated using SIMS analysis and the film roughness and thickness, evaluated using AFM and TEM analyses, respectively, will also be reported.
References
[1] S.C. Song et al., IEDM, p.373, 1998.
[2] S.V. Hattangady et al., in Microelectronic Device Technology II, SPIE Proceedings Series, 3506, Bellingham, WA, p.30 (1998).

SESSION C8: SILICIDE FORMATION MECHANISMS
Chairs: Paul R. Besser and Ken-ichi Goto
Thursday Morning, April 27, 2000
Salon 5/6 (Marriott)

8:30 AM *C8.1
MECHANISMS FOR LOW TEMPERATURE FORMATION OF C54-$TiSi_2$ BY INCORPORATION OF TRANSITION ELEMENTS. Christian Lavoie, Cyril Cabral, Jr. and James M.E. Harper, IBM T.J. Watson Res. Ctr., Yorktown Heights, NY.

The C54 phase of $TiSi_2$, widely used for contacts to CMOS devices, does not reliably form on sub-half-micron features due to the lack of nucleation sites in the high resistivity precursor C49 $TiSi_2$. The incorporation of transition elements (Nb, Ta, Mo, W) to increase the C54 nucleation density leads to reliable formation on features below 0.5 μm. The transition elements can either be alloyed with Ti[1], placed as an interlayer between Ti and Si[2,3] or implanted into the Si[4]. The possible mechanisms for the enhancement include increased nucleation density due to a small grained precursor C49 $TiSi_2$ phase, crystallographic templates provided by the added transition element disilicides and pseudomorphic templates provided by the increased stability of the metal rich silicide, Ti_5Si_3. We will review the three techniques for incorporating the transition elements and show the recent evidence[5,6] that supports the template mechanism. 1. C. Cabral, Jr. et al., Appl. Phys. Lett. 71(24) 3531 (1997). 2. C. Cabral, Jr. et al., J. Mater. Res. 12(2), 304(1997). 3. A. Mouroux et al., Phys.

Rev. B, 56(16), 10614 (1997). 4. R.W. Mann et al., Appl. Phys. Lett. 67(25), 3729 (1995). 5. A. Quintero et al., J. Appl. Phys. (1999) in press. 6. M.A. Gribelyuk et al., J. Appl. Phys. 86(5), 2571(1999).

9:00 AM C8.2
ON THE TEMPLATE MECHANISM OF ENHANCED C54-$TiSi_2$ FORMATION. Ludger Kappius, Raymond T. Tung, Lucent Technologies, Bell Labs, Murray Hill, NJ.

Recently, the formation of the C54-$TiSi_2$ phase on Si from sputtered Ti has been shown to be facilitated by the addition of small amounts of refractory metal.This phenomenon has been attributed to a template mechanism: The close lattice matching condition between major planes of the C54-$TiSi_2$ crystal and the C40 $Ti_xRm_{1-x}Si_2$ lattice (where Rm is Ta, Mo,..) is thought to lower the nucleation barrier for the C54-$TiSi_2$ phase. Alternatively, a matching condition between the hexagonal Ti_5Si_3 phase and the C54-$TiSi_2$ phase has also been invoked. In this work, the influence of C40-$Ti_xMo_{1-x}Si_2$ (where x=0.4 or 0.8) and Ti_5Si_3 phases on the nucleation of $TiSi_2$ phase(s) has been studied in isolation. These "template" layers were first formed on oxide layers by co-deposition and annealing in UHV, before amorphous $TiSi_2$ layers were deposited on top and annealed in-situ. Alternatively, the "template" layers were deposited on top of polycrystalline C49-$TiSi_2$. The present results showed a clear effect of the $Ti_xMo_{1-x}Si_2$ layer on the crystallization of amorphous $TiSi_2$ phase. C49 phase with fine grain size nucleated which later transformed to the C54 phase (~650°C) more easily than $TiSi_2$ layer grown without the "template" layer. The Ti_5Si_3 template has no strong effect on the silicide reaction of amorphous $TiSi_2$ layer. Next to pre-existing C49-$TiSi_2$ crystals, however, the presence of either $Ti_xMo_{1-x}Si_2$ or Ti_5Si_3 had no observable effect on the subsequent transformation to the C54-$TiSi_2$ phase. The present results are not supportive of either of the proposed template mechanisms and, instead, are suggestive of the reduction of the C49-$TiSi_2$ grain size as the most important effect of refractory metals on Ti silicide reaction. These results are also compared with the transformation characteristics of pure C49 $TiSi_2$ layers whose grain size has been adjusted through different in-situ nucleation steps.

9:15 AM C8.3
INVESTIGATION ON C54 $TiSi_2$ NUCLEATION AND GROWTH BY MICRO-RAMAN IMAGING. S. Privitera, E. Rimini, University of Catania, Dept. of Physics, Catania, ITALY; F. La Via, CNR-IMETEM, Catania, ITALY; S. Quilici, F. Meinardi, University of Milano-Bicocca, Dept. of Materials Science, Milano, ITALY.

In spite of large investigation on the C49-C54 transition in $TiSi_2$ thin films and narrow lines, the processes of nucleation and growth of the C54 phase are still not clear. To understand and control the process of nucleation a detailed thermodynamical description of the driving force for the transformation and of the nucleation barrier energy is required. The link between the growth kinetics and the driving force is the dynamical evolution of the population of C54 grains growing in the C49 environment. However, all common used techniques are sensitive only to the transformed volume fraction and do not provide any information on the number and the size distribution of the C54 grains. To overcome this limitation we used μ-Raman spectroscopy as a real microscopy technique, obtaining images that show the evolution of C54 grains during the transition. Spectra have been acquired focusing the light of a HeNe laser into a spot of 0.7 μm of diameter. For each sample a total area of 100x50 μm^2 has been analised, collecting spectra in step of 0.5 μm in the x-y-directions. By processing Raman spectra with a software program we obtained images with a minimum detectable C54 area of 0.025 μm^2. From μ-Raman imaging (MRI), converted area fraction has been determined for different annealing time and temperatures and it has been compared with transformed fraction obtained from electrical measurements. The comparison showed a good agreement of the two methods and indicated the reliability of MRI for quantitative analysis. MRI, in addition, is also able to independently measure the density and the C54 grain size. This allowed us to separe the contribution of the processes of nucleation and growth and to evaluate the activation energy for the C54 grain growth velocity, nucleation rate and transient time.

9:30 AM C8.4
SILICIDE ENGINEERING: INFLUENCE OF ALLOYING ELEMENTS ON $CoSi_2$ NUCLEATION. Christophe Detavernier, R.L. Van Meirhaeghe, University of Gent, Dept. of Solid State Science, Gent, BELGIUM; K. Maex, IMEC, Leuven, BELGIUM; F. Cardon, University of Gent, Dept. of Solid State Science, Gent, BELGIUM.

The presence of a 3-7 nm Ti interlayer is known to promote epitaxial growth of $CoSi_2$. Traditionally, this is explained by the ability of Ti to reduce SiO_2 and by the fact that the interlayer acts as a diffusion barrier. In case of a thin Ti interlayer (<1 nm), we observed that the nucleation of $CoSi_2$ is delayed to higher temperature. Moreover, the $CoSi_2$ has a strong preferential orientation and improved thermal stability. For 0.1-0.3 nm Ti, there is a $< 220 >$ and $< 400 >$ orientation, while for thicker Ti (>0.6 nm), there is a strong $< 400 >$ orientation. Similar results are found for a Ti capping layer (Ti/Co/Si system). Especially in the case of a capping layer, it is clear that the traditional explanation based on a diffusion mediating layer is not valid : a different mechanism seems to be at work. Our observations may be explained by the presence of Ti on the CoSi grain boundaries. This will improve cohesion and thus lower the grain boundary energy. Moreover, fast grain boundary diffusion will be inhibited. In this case, heterogeneous nucleation theory can be used to explain the increase of the nucleation temperature and the natural selection of the substrate-matched nuclei. We have found that thin interlayers of Ta, W, Cr, Mo and C show similar effects, delaying $CoSi_2$ nucleation and inducing epitaxial growth. In the presence of sulfur, which is known to cause grain boundary decohesion in metals, the opposite effect is observed : $CoSi_2$ formation is accelerated. These results illustrate the possibility of silicide engineering : the addition of small amounts of impurities (as a capping layer, interlayer or alloyed within the Co layer) may be used to control the silicidation reaction (reaction temperature), and to influence the properties of the silicide layer formed (preferential orientation, thermal stability).

9:45 AM C8.5
IN-SITU REAL TIME STUDIES OF NICKEL SILICIDE PHASE FORMATION. Manisha Tinani, Ying Gao, Alex Mueller, E.A. Irene, Department of Chemistry, University of North Carolina, Chapel Hill, NC; Y.Z. Hu, S.P. Tay, Steag RTP Systems Inc., San Jose, CA.

Metal silicides have recently been investigated as possible gate contact and interconnect materials in the microelectronics industry. As device size decreases, polycrystalline silicon, which is also used as a gate contact material, can degrade the device due to its higher resistance. Metal silicides offer low metal-like resistivities and high temperature stability. For modern applications, the silicides need to have stable phases, low processing temperatures and mechanical compatibility with silicon, in order to reduce defects at the silicon-silicide surface. NiSi, the monosilicide of nickel, fulfills all the criteria for the ideal metal silicide. NiSi has a resistivity of 20μm-cm, low formation temperature and a large formation temperature window of 350-750°C. NiSi surpasses other commonly used silicides, such as $TiSi_2$ and $CoSi_2$[1], in these properties while avoiding problems faced with these silicides[2]. Three nickel silicide phases, Ni_2Si, NiSi, and $NiSi_2$, can form below 1000°C in different temperature ranges. Therefore, in order to use NiSi in practical situations, it is important to be able to detect the formation of NiSi in real time. Our strategy is to monitor and follow the phase formation using in-situ real time ellipsometry that can be used in a rapid thermal environment. First we demonstrate that we can identify the various phases, and the extent of the transformation using the optical data obtained via spectroscopic ellipsometry. An optical database for the three nickel silicide samples is established using ellipsometry and RBS, which is used to monitor the phase changes occurring over time. Secondly, we demonstrate that long time and high temperature processing leads to agglomeration of the silicide, even below the expected agglomeration temperature, which is not desirable since film thicknesses in MOS devices keep decreasing, and a roughness layer at the Si/metal interface can degrade the device. Real time studies to detect NiSi with increasing annealing temperature and time have been done, and the results presented. [1] A. Lauwers, Q.F. Wang, B. Deweerdt, and K. Maex, Appl. Surf. Sci., 91, 12 (1995). [2] Y.Z. Hu, and S.P. Tay, J. Vac. Sci. Technol. A, 16, 1820 (1998).

SESSION C9: SHALLOW JUNCTIONS AND SILICIDES
Chair: Jorge Kittl
Thursday Morning, April 27, 2000
Salon 5/6 (Marriott)

10:30 AM *C9.1
STUDY OF $CoSi_x$ SPIKE LEAKAGE FOR SUB-0.1μm CMOS. Ken-ichi Goto, Fujitsu Laboratories Ltd., Kanagawa, JAPAN.

As CMOS device scaling down to 0.18, many LSI companies are changing their salicide from $TiSi_2$ to $CoSi_2$ because of a lower sheet resistance when gate-width is less than O.l -μm. And, the junction leakage problem caused by $CoSi_x$ spike have been studied and solved by several methods such as (1) high temperature annealing, (2) high temperature Co sputtering, and (3) pre-amorphization. However, there are no reports which have investigated the $CoSi_x$ spike except our group due to the difficulties in observing the spike because of the low density and contrast TEM images. In order to achieve a high yield and stable characteristic, direct observation of $CoSi_x$ spike is very important for controlling of this behavior while optimizing the annealing temperature.

In this work, we have studied the leakage mechanism of Co salicided junction by comparing with that one in Ni salicide, and shown a direct observation technique on the local defects using the combination of Photo Emission Microscopy (PEM), Focused Ion Beam (FIB), and Transmission Electron Microscopy (TEM).

11:00 AM C9.2
ELEVATED SOURCE DRAIN MOSFETS USING SELECTIVE EPITAXIAL GROWTH. Srikanth. B. Samavedam, A. Dip, A.M. Phillips, P.J. Tobin, T. Mihopoulos, Motorola Advanced Products Research and Development Laboratory, Austin, TX.

Elevated source drain (ESD) structure in deep sub-micron complementary metal oxide semiconductor (CMOS) technology can help reduce parasitic series resistance and simultaneously achieve shallow contacting junctions to minimize short channel effects. Silicon selective epitaxial growth (Si SEG) in conventional CMOS processing can be used to achieve a self-aligned ESD structure. The Si SEG step can be inserted either before or after the contacting source/drain junction formation. Some of the issues with Si SEG include additional thermal budget, facet formation, loss of selectivity and pattern loading effects. Device concerns include higher leakage, higher series resistance from undoped epitaxial Si and increased parasitic capacitance. A low thermal budget high quality Si SEG process using $Si_2H_2Cl_2$ and HCl has been demonstrated in a commercial RTCVD reactor. The use of SiH_4 or depositing selective SiGe can further lower the process thermal budget. The pre-clean sequence prior to SEG is the key to controlling facet formation at the Si/spacer edge in deep sub-micron MOSFETs. Low line to line leakage confirms the high process selectivity to nitride and oxide areas. The growth on exposed polysilicon gates leads to gate line-width widening and an apparent lowering of gate sheet resistance. ESD MOSFET parameteric data suggests that the well doping needs to be optimized to counter the slight increase in n+-p diode leakage compared to conventional MOSFETs. Capacitance-voltage simulations indicate that the gate to drain capacitance decreases initially and then increases with SEG thickness.

11:15 AM C9.3
MODELING SELF-ALIGNED SILICIDATION IN 2D AND 3D: GROWTH SUPPRESSION BY OXYGEN DIFFUSION.
Victor Moroz, Klas Lilja, Avant Corporation, Fremont, CA; Takako Okada, Toshiba Corporation, Research and Development Center, Kawasaki, JAPAN.

Typical experimentally observed shape of the self-aligned titanium silicide shows virtually 100% suppression of the lateral silicidation under the oxide spacer. This observation did not receive a satisfactory theoretical explanation, yet it's understanding is necessary for predictive simulation of the silicide shape, which determines source/drain impurity diffusion and stress distribution around the silicide. Simulation of the self-aligned silicidation based on the assumption of constant diffusivity for the silicon atoms, which are the dominant diffusing species in titanium silicide, leads to lateral silicidation, comparable to the vertical silicidation. Similar shape is obtained also if metal atoms are the dominant diffusing species, or if several species are simultaneously contributing to the silicide growth, as long as their diffusivities and reaction rates are constant throughout the silicide. It is known that implanted oxygen or oxygen incorporated into metal during deposition suppresses growth of different types of silicides. We suggest that the growth rate of the self-aligned silicide near the oxide spacer is reduced due to injection of oxygen atoms from oxide into the silicide and suppression of silicon atom diffusivity and reaction rate. Oxygen diffusion in silicide is simulated as a combination of the bulk and boundary diffusion using a generalization of the interface trapping model. Simulated silicide shape using the suggested model shows no lateral silicidation under the spacer, in agreement with the measurements. Simulation of the self-aligned silicidation with a nitride spacer gives similar silicide shape due to the oxygen injection from the thin pad oxide under the nitride spacer. Stresses generated during silicidation, and especially due to the thermal mismatch between silicon and silicide, provide a major contribution to the residual stresses in the MOSFET's channel next to the source and drain p/n junctions. These stresses are known to increase junction leakage current through band gap narrowing.

11:30 AM C9.4
ACTIVATION ENERGY OF ELECTROMIGRATION OF W-PLUG CONTACTS IN DEEP SUBMICRON IC INTERCONNECT. Q. Guo, K.F. Lo, I. Manna, E.C. Chua, X. Liu, Chartered Semiconductor Manufacturing Ltd., Singapore, SINGAPORE.

The paper reports an extensive study of activation energy Ea of electromigration of both W-plug contacts to silicon (N+ contact) and to poly layer (Poly contact) and dependence on failure criterion (FC) and stress current. The structures were fabricated by advanced deep submicron polycide process. The metal stripes connected contacts and pads are of bamboo structure. It is found that the calculated value of Ea of N+ contact strongly depends on the failure criterion. At a stress current of 12mA, it is 1.12eV at FC=1% and then rapidly decreases to 0.94eV at FC=40%. It gradually tends to a saturated value of 0.73eV. As stress current decreases, such dependence still works but is slightly weakened. On contrary, dependence of Ea on failure criterion is not so pronounced in the Poly contact as in N+ contact. At a stress current of 12mA, Ea is found to be 0.9eV at FC=2% and approaches a saturated 0.82eV with increasing failure criterion. As the stress current decreases to 4mA, Ea is almost independent of failure criterion. It is observed by Scanning Electron Microscope that the microstructure change of N+ contact structure is the same as that of Poly contact in electromigration. Therefore, EM mechanism of Poly contact is expected to be similar to that of N+ contact. Activation energy is a very important parameter to describe the atom diffusion mechanism of electromigration. Different Ea projects significantly different EM lifetime. It will be demonstrated that the dependence of Ea on failure criterion and stress current is an artifact which is ascribed to the calculation without considering the ambient temperature dependence effect. The actual Ea is about 0.8eV for both N+ and poly contacts, independent of failure criterion. It suggests that the interfacial diffusion, rather than bulk diffusion, is a primary mechanism of bamboo structure in EM measurement.

11:45 AM C9.5
EFFECT OF H_2/N_2 PLASMA TREATMENT ON THE CHEMICAL COMPOSITION OF CHEMICAL VAPOR DEPOSITED TITANIUM NITRIDE THIN FILMS STUDIED BY X-RAY PHOTOELECTRON SPECTROSCOPY. E.-Gene Garza, Jin Zhao, Process Characterization and Analysis Laboratory, Advanced Micro Devices, Austin, TX; Kinsang Lam, Fab25 Thin Film Module, Advanced Micro Devices, Austin, TX; Clive M. Jones, Process Characterization and Analysis Laboratory, Advanced Micro Devices, Austin, TX.

Titanium nitride (TiN) is commonly used as diffusion barrier in contacts and vias as well as in the interconnect stacks. It also serves as an adhesion for chemical vapor deposited (CVD) tungsten. A good barrier layer must exhibit good step coverage to achieve void free plug formation and adequate barrier thickness at the bottom of the contact or via. The current trend is to replace physical vapor deposited (PVD) TiN by CVD TiN so as to meet the step coverage requirements for sub-0.5μm contacts and vias. Tetrakis-(dimethylamido)-titanium (TDMAT) is a major precursor being used in the chemical vapor deposition process of TiN thin film. When used alone, TDMAT produces TiN films with substantial amount of carbon and low N/Ti ratio. Both of these situations increase the film resistivity. In the present work, CVD TiN thin films, grown by thermolysis of TDMAT codosed with N_2, were treated in H_2/N_2 plasma for 0-50 seconds. The effect of treatment time on film composition and chemical states was studied using X-ray photoelectron spectroscopy (XPS). ALL samples were exposed to air after deposition to allow oxygen absorption throughout the bulk of the film. XPS depth profiles revealed that plasma treatment times of 10-50 seconds failed to treat the full thickness of the deposited films. The depth of treatment proved to be nonlinear with respect to treatment time and decreased in effectiveness for times exceeding 30 seconds. For all treatment times, carbon levels were significantly reduced in the near-surface region but returned to as-deposited concentrations at greater depths. Both organic and carbidic forms of carbon were identified in the topmost regions of the films; the bulk of the films, however, were dominated by carbidic carbon. Absorbed oxygen concentrations in the near-surface region also decreased suggesting plasma induced changes in film density.

SESSION C10: EPITAXIAL SILICIDES
Chair: Larry A. Clevenger
Thursday Afternoon, April 27, 2000
Salon 5/6 (Marriott)

1:30 PM *C10.1
EPITAXIAL SILICIDE CONTACTS AND JUNCTIONS.
Raymond T. Tung, Ludger Kappius, Hans J. Gossmann, Lucent Technologies Bell Laboratories, Murray Hill, NJ.

Epitaxial silicides have long been touted as the ideal contact metallization material because of their excellent thermal stability and layer uniformity. The progress toward the implementation of epitaxial silicide in ULSI devices, however, has not been particularly smooth. In this talk, the present status of epitaxial $CoSi_2$ fabrication techniques are examined. Recent developments in oxide mediated epitaxy (OME) are presented. Specifically, the uses of Ti cap, dilute $CoTi_x(x<1)$ alloy and two-step processing are discussed and their advantages and limitations examined. Very high quality single crystal $CoSi_2$ films have been grown by these methods. Furthermore, it is shown that the voiding problem at edges of oxide pattern can be avoided by optimized processing. A novel phenomenon, concerning the presence of a finite

spread in the exact orientation of epitaxial $CoSi_2$ layers grown with the aid of Ti, is demonstrated and its possible models discussed. Dopant out-diffusion (B, As and P) from epitaxial silicide layers is studied and shown to be comparable to that from polycrystalline silicide films. Very shallow junction depth has been achieved using dopant out-diffusion. The electrical behavior of outdiffused junctions is compared with silicided junctions formed by ion implantation and annealing. These and other results highlight the generally good prospect for epitaxial silicide contacts for ULSI applications.

2:00 PM C10.2
EPITAXIAL $CoSi_2$ FORMATION BY A Cr OR Mo INTERLAYER.
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The presence of a Ti interlayer is known to result in epitaxial growth of $CoSi_2$. A similar effect has been reported for Ta, Hf, C, W and Zr interlayers, while it has been reported that in case of V and Cr interlayers, the solid phase reaction results in polycrystalline $CoSi_2$ (J.S. Byun et al., JAP 78(11) 6784). In literature, the epitaxial growth is usually explained by (1) the ability of Ti to reduce interfacial SiO_2 and by the fact that (2) the Ti interlayer acts as a diffusion barrier, mediating the Co flux towards the substrate. We have studied $CoSi_2$ formation in the presence of a Cr or Mo interlayer or capping layer. We will show that, contrary to what was previously reported, Cr and Mo may be used as interlayers to grow epitaxial $CoSi_2$. However, unlike for Ti, the thickness of the interlayer is very important. If the Cr or Mo interlayer is too thick ($>$ 5 nm), polycrystalline $CrSi_2$ or $MoSi_2$ are formed first and $CoSi_2$ is formed on top of the already formed disilicide. In this way, epitaxial growth of $CoSi_2$ is impossible. However, both XRD and random/channeling RBS results indicate that for a 2-3 nm interlayer of Cr or Mo, $CoSi_2$ forms epitaxially on Si$< 100 >$. For thinner interlayers, there is a preferential $< 220 >$ and $< 400 >$ orientation. This can be explained by the presence of Cr or Mo on the CoSi grain boundaries, which will affect the heterogeneous nucleation of $CoSi_2$.

2:15 PM C10.3
IN-SITU GROWTH AND GROWTH KINETICS OF EPITAXIAL (100)$CoSi_2$ LAYER ON (100)Si SUBSTRATE BY REACTIVE CHEMICAL VAPOR DEPOSITION. Hwa Sung Rhee, Heui Seung Lee, Jong Ho Park and Byung Tae Ahn, Korea Advanced Institute of Science and Technology, Dept. of Materials Science and Engineering, Taejon, KOREA.

Uniform epitaxial $CoSi_2$ layers have been grown in situ on a (100) Si substrate at temperatures above 600°C by reactive chemical vapor deposition of cyclopentadienyl dicarbonyl cobalt, $Co(C_5H_5)(CO)_2$. Co-rich phases such as Co_2Si and CoSi were suppressed during cobalt metallorganic chemical vapor deposition at substrate temperatures above 500°C. A thin carbon layer was found on the top of the epitaxial $CoSi_2$ layer grown on Si substrate due to incomplete decomposition of the cobalt metallorganic source and diffusion of Co into Si substrate. In spite of the existence of a surface carbon layer, an ion channeling minimum yield of 8% in Rutherford backscattering/ channeling spectrometry has been achieved in the epitaxial layer, indicating a nearly perfect epitaxial order. The carbon pile-up on the surface of $CoSi_2$ layer at the initial stage of Co deposition seems to play the role of a cobalt diffusion barrier, avoiding the formation of Co-rich phases. The growth kinetics of an epitaxial $CoSi_2$ layer on a Si (100) substrate was investigated at temperatures raging from 575 to 650°C. In initial deposition stage, plate-like $CoSi_2$ spikes were nucleated along the $< 111 >$ directions in (100) Si substrate with a twinned structure. The discrete $CoSi_2$ layers with both {111} and (100) planes were grown into a uniform epitaxial layer during deposition, resulting in a parabolic relationship between the thickness of epitaxial $CoSi_2$ layer and the deposition time.

2:30 PM C10.4
NICKEL-PLATINUM MONOSILICIDATION INDUCED ELECTRICALLY ACTIVE DEFECTS IN n-TYPE SILICON.
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Recently it has been found that the addition a small amount of Pt (e.g., 5 at. % Pt) significantly increases the thermal stability of nickel monosilicide (NiSi). Despite increasing interest in the potential application of Ni(Pt) monosilicide to ultra shallow junction devices, the effect of the Ni(Pt) monosilicidation on the electrical properties of silicon substrate has not been addressed yet. We have studied electrically active defects induced by the formation of Ni(Pt) monosilicide. 20 nm thick Ni(Pt) films with 5 at. % Pt were evaporated onto CZ n-type $< 100 >$ silicon wafers of 1-10 Ω-cm resistivity by sputtering of Ni(Pt) alloy target. A number of chips cut off these wafers were then subjected to 60 s rapid thermal anneal (RTA) using nitrogen as ambient gas at temperatures of 600 - 800°C. The formation of Ni(Pt)Si after RTA was monitored by X-ray diffraction (XRD) measurement. Deep level transient spectroscopy (DLTS) measurements were carried out to characterize the electrically active defects induced by the Ni(Pt) monoslicidation process. Transmission electron microscopy (TEM) was also employed to monitor the formation of extended structural defects in silicon substrate matrix. Three Ni-related defect levels were detected at Ec - 0.42 eV, Ev + 0.22 eV, and Ev + 0.28 eV after Ni(Pt) mono-silicidation at 600°C or above while two Pt-related defect levels were observed at Ec - 0.28 eV and Ec - 0.50 eV after silicidation at 700°C or above. In addition to the discrete defect levels, a broad DLTS signal spectrum was observed in the sample silicided at 600°C in which {311} type defects with a width between 50 - 100 AA were also observed by TEM. Most of observed electrically active defects were found to be present in near-surface regions ($<$2 μm).