SYMPOSIUM D

Materials, Technology, and Reliability for Advanced Interconnects and Low-k Dielectrics

April 23 – 27, 2000

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* Invited paper

TUTORIAL

ST D-G-H: Cu INTERCONNECTS: WHAT ARE THE ISSUES?
Sunday, April 23, 2000
1:00 p.m. - 4:45 p.m.
Golden Gate B2 (Marriott)

The implementation of Cu in the metallization process of integrated circuits has redirected many research and development projects in universities, research institutes, and industry. A vast amount of data is being collected on the physical and mechanical properties of Cu thin films and lines, on various aspects of its polycrystalline nature. The implementation of Cu also goes hand in hand with the changeover from the physical vapor deposition technique to electroplating of the metal and with the introduction of chemical-mechanical polishing instead of the classical metal dry etch process. The research related to these new process steps has created a need to get more insight into other aspects of materials science.

The aim of this tutorial is to provide an interdisciplinary introduction to the latest evolution in fields relevant to Cu interconnects. An overview will be given of the state of the art of Cu metallization for high-performance Si technology. The importance of electrochemistry for the understanding of electrochemical deposition will be highlighted, and possible mechanisms of Cu corrosion will be discussed.

Instructors:
Robert Rosenberg, IBM T.J. Watson Research Center
Tom Moffatt, NIST
Vlasta Brusic, Cabot Corporation

SESSION D1: MECHANICAL PROPERTIES
Monday Morning, April 24, 2000
Golden Gate B2 (Marriott)

8:30 AM *D1.1
Transferred to D3.2

9:00 AM D1.2
THE USE OF THE FOUR-POINT BENDING TECHNIQUE FOR DETERMINING THE STRENGTH OF LOW K DIELECTRIC/ BARRIER INTERFACE. Ting Y. Tsui, AMD/Motorola Alliance, Austin, TX; J.J. Lee, Bradley Ekstrom, Greg Braeckelmann, Stan Filipiak and Cindy Goldberg, Motorola Inc., Austin, TX.

This investigation explored the applicability of the four-point bend technique for determining the adhesion strength of various low dielectric constant materials in contact with different barrier layers. Time of flight SIMS (TOFSIMS) was used for surface chemical analyses of the delaminated interfaces. The effect of annealing on mechanical strength was coupled with chemical analysis to discern the adhesion properties of different low k/barrier systems. Interfacial layer formation was associated with degraded adhesion characteristics in specific cases. The four-point bend analysis was successfully used to evaluate and compare low k dielectric/barrier stacks. Mechanisms for adhesion failure were proposed for a variety of materials by coupling the mechanical testing results with TOFSIMS.

9:15 AM D1.3
THE EFFECT OF FATIGUE ON THE ADHESION AND SUBCRITICAL DEBONDING OF BENZOCYCLOBUTENE/ SILICON DIOXIDE INTERFACES. Jeffrey M. Snodgrass, Dimitrios Pantelidis, John C. Bravman and Reinhold H. Dauskardt, Stanford University, Department of Materials Science and Engineering, Stanford, CA.

The effect of fatigue on microelectronic thin film interfaces has until now been difficult to quantify. Most industrial fatigue testing uses HAST (Highly Accelerated Stress Testing) protocols. HAST inherently convolutes the effects of mechanical fatigue and the environment. Our work focuses on isolating the deleterious effects of mechanical fatigue on interfaces, which we have found to be substantial. In this study, the integrity of a low-k polymer interface involving benzocyclobutene (BCB) and silica was examined under a variety of loading conditions. First, critical (fast fracture) adhesion values were measured using standard interface fracture-mechanics geometries. Experiments were then conducted to measure the fatigue debond growth rate as a function of the range of strain energy release rate. Generally, our results show that even under room temperature conditions, measurable debond growth occurs at driving forces that are considerably lower than those necessary to cause critical debonding. Results will be presented detailing the effects of parameters such as interface chemistry (adhesion promoters), polymer cure state, and polymer layer thickness on the resistance of the interface to fatigue debonding. Strategies for increasing resistance of dielectric interfaces to fatigue debonding will also be outlined. Finally, high-resolution XPS studies which fully characterize the debond path in these layered systems are presented.

9:30 AM D1.4
A QUANTITATIVE STUDY OF THE ADHESION BETWEEN COPPER, BARRIER AND ORGANIC LOW-K POLYMERS. Filip Lanckman[1], Sywert H. Brongersma, Istvan Varga, Eric Beyne and Karen Maex[1], IMEC, Leuven, BELGIUM. [1]also at E.E. Dept., K.U.-Leuven, BELGIUM.

The integration of Cu and low dielectric constant (k) materials in back end processing will replace aluminium and silicon oxide by offering reduced signal propagation delay, crosstalk and power dissipation. An important issue regarding reliability is the adhesion between metal (barrier) and low-k material. In this work, the adhesion strength is determined quantitatively by shear testing. In this method, barrier and Cu metal are deposited on the dielectric. Cu is deposited by electroplating on a sputtered Cu seed layer. Lithography and wet etching are used to remove the Cu seed layer and barrier selectively to obtain rectangular and circular test structures with a different area and a height of 10mm. During shear testing, a needle pushes laterally against the test structure until failure occurs at the polymer-metal interface. The needle force is monitored continuously. The ratio of the maximum applied force and the area of the test structure is defined as the adhesion force. Two different advanced organic low-k materials are evaluated: an anorganic hydrocarbon (k=2.65) and a polyarylene ether-based polymer (k=2.84). Plasma deposited silicon oxide is used as a reference. Ti/TiN, Ta/TaN and Co are used as barrier metals. Both the dielectric-Cu and the dielectric-barrier/metal interface are studied. The influence of different heat treatments in a nitrogen ambient on the adhesion strength will be discussed. X-ray photoelectron spectroscopy can be used to study the failed interface. In order to enhance the adhesion between dielectric and Cu/barrier, a pretreatment of the dielectric surface is performed. The pretreatment consists of an oxygen or a fluorine containing plasma. These plasma treatments reflect also the modification of the dielectric surface during dry etching. In a second part of the work the adhesion strength between Cu and the different barriers is measured and discussed.

9:45 AM D1.5
ADHESION IMPROVEMENT IN COPPER INTERCONNECT TECHNOLOGY USING COPPER MAGNESIUM ALLOYS. G. Braeckelmann, R. Venkatraman, M. Herrick, R. Cole*, D. Clegg*, Motorola Inc., Advanced Products Research and Development Laboratory, Austin, TX. *Motorola Inc., Final Manufacturing Technology Center, Austin, TX.

Copper has been selected as the interconnect material for the latest technologies due to its lower resistivity and higher electromigration resistance as compared to Al metalization. However, a number of issues needed to be resolved for reliable and defect-free manufacturing. One issue was discovered during packaging of Cu chips. The chip and the bump-to-chip interfaces have to remain intact when testing the joint quality using the die pull test. However, using pure Cu it was observed that a large fraction of the bumps fail at the passivation/Cu interface. This is due to the inherently poor adhesion of Cu to oxides and nitrides.
To improve the adhesion between Cu and SiN_x small amounts of Mg were incorporated into the Cu interconnect structure. In this process, the sputtered seed layer was CuMg rather than the pure Cu normally sputtered. During the following hot process steps, the Mg diffuses to the surface and reacts with SiN_x thereby providing good adhesion. Using CuMg, a reliable package was assembled achieving zero failures in the die pull test for Cu integration.
In addition, characteristics of the CuMg films have been studied in depth. Analyzing the diffusion behavior of Mg through pure Cu showed that Mg readily diffuses and agglomerates at the surface where it reacts with residual oxygen. Furthermore, the adhesion behavior was characterized by studying the wetting behavior of Cu and CuMg on SiO_2. After annealing the films, it was observed that pure Cu dewetted, forming islands on the SiO_2 surface, whereas the CuMg films stayed smooth and no significant increase in roughness was observed.
This presentation will review our work in improving packaging reliability by improving the Cu-SiN_x adhesion and will also show detailed data on Cu alloying with Mg.

10:30 AM *D1.6
STABLE DIELECTRIC FRACTURE AT INTERCONNECTS FROM THERMAL AND ELECTROMIGRATION STRESSES. Robert F. Cook, University of Minnesota, Department of Chemical Engineering and Materials Science, Minneapolis, MN.

Substantial stresses develop in microelectronic interconnection structures from thermal expansion mismatch between the insulating dielectric and the conducting lines (and semiconductor substrate) and from electromigration within an interconnecting line constrained by the dielectric. Fracture in dense silica-based dielectrics from these stresses is usually rare; thermal expansion mismatches with both the lines and substrate leave the dielectric in compression and electromigration stresses, although generating tension in the dielectric, are not large enough at conventional current densities and line dimensions. However, advanced quasi-porous low-k dielectrics have mechanical properties significantly different from silica such that both thermal and electromigration stress levels are expected to exceed those for fracture. In this study, the conditions for cracking in the dielectric adjacent to an interconnection line are examined under thermal mismatch and electromigration conditions, modeling the dielectric as an elastic-plastic material. Attention is focused on the separate conditions for crack nucleation, initiation to stable lengths and propagation to unbounded lengths and on the threshold levels of thermal mismatch and current density for each. Particular consideration is given to the behavior of the low-k silsesquioxane-based spin-on glass materials.

11:00 AM D1.7
NANOSCALE ELASTIC IMAGING OF ALUMINUM/LOW-K DIELECTRIC INTERCONNECT STRUCTURES. Robert E. Geer, G.S. Shekhawat, University at Albany, State University of New York, Albany, NY; Oleg Kolosov, G. Andrew D. Briggs, Department of Materials, Oxford University, Oxford, UNITED KINGDOM.

One of the most difficult challenges in low-k integration in IC processing concerns the significant mismatch of mechanical properties between metals and most low-k dielectrics. Previously, it has not been possible to image on a nanometer length scale the local variation of mechanical properties near dielectric/liner and liner/metal interfaces. Such an ability would greatly facilitate thermal and bias-stress reliability analysis of single and multi-level low-k metallization structures by locating variations in local material modulus due to local compositional variations, stress concentration, etc... Pursuant to this, we report the development of a new technique to image such properties based on ultrasonic force microscopy (UFM). UFM has been used to obtain nanoscale elastic images of single-level damascene interconnect structures consisting of chemical vapor deposited (CVD) aluminum in a benzocylcobutene low-k dielectric matrix. A titanium nitride liner is deposited prior to aluminum CVD. Analyses of these images reveal an elastic modulus gradient in the polymer matrix near the dielectric/liner interface leading to an increase in polymer stiffness near the metal line. Spectroscopy studies of the liner/polymer interfaces reveal that this variation in the mechanical response of the polymer originates in the compositional modification of the polymer surface upon etch processing. Thermal failure studies are also presented relating these local mechanical variations at the polymer/liner interface to failures resulting from local coefficient of thermal expansion (CTE) mismatches.

11:15 AM D1.8
CONCENTRATION AND STRAIN EVOLUTION IN PASSIVATED Al(0.5 at. /% Cu) CONDUCTOR LINES DURING ELECTROMIGRATION FROM IN-SITU X-RAY MICROBEAM FLUORESCENCE AND DIFFRACTION. H.-K. Kao, G.S. Cargill, III, Dept of Materials Science and Engineering, Lehigh Univ., Bethlehem, PA; C.-K. Hu, IBM Research, Yorktown Height, NY.

We have used x-ray microbeam fluorescence and diffraction for in-situ measurements of Cu concentration and strain during electromigration for passivated 10μm-wide, 200μm-long Al(0.5 at./% Cu) conductor lines. These measurements show development of Cu composition gradients during d.c. electromigration, decay of composition gradients after halting current flow, reversal of composition gradients after reversal of current flow, and dependence of steady state composition gradients on the magnitude of current flow. Results from real-time measurements of strain developed in the conductor lines during electromigration will also be discussed. These composition and strain measurements are a continuation of experiments for which initial results were reported in Symposium M of the Spring 1998 MRS meeting (H. K. Kao, G. S. Cargill III, K. J. Hwang, A. C. Ho, P.-C. Wang and C.-K. Hu, "In-Situ X-Ray Microbeam Cu Fluorescence And Strain Measurements on Al(0.5 at.% Cu) Conductor Lines During Electromigration," MRS Symp. Proc. (1999)).

11:30 AM D1.9
PASSIVATION FILM CRACKING IN INTERCONNECT STRUCTURES CAUSED BY TEMPERATURE CYCLING:A NEW MECHANISM. M. Huang, Z. Suo, Mechanical and Aerospace Engineering Department and Materials Institute, Princeton University, Princeton NJ; Q. Ma and H. Fujimoto, Intel Corporation, Santa Clara, CA.

Temperature cycling has long been used as an accelerated reliability test to qualify new electronic products. Many commonly observed failure modes, however, are so poorly understood that the extrapolation of the test results to service lifetime is empirical, loosely based on historical records of similar products. This lack of mechanistic understanding is particularly disconcerting when new interconnect materials are being explored. We have initiated a program to study mechanisms of failure modes under temperature cycling. In this talk, we present our recent study on the cracking in the SiN films near the silicon die corner of a flip-chip package. A new mechanism is discovered. We show that the cyclic temperature, coupled with the shear stress at the die corner, causes the interconnect pads underneath the SiN films to undergo plastic ratcheting. Consequently, in the SiN films the stress builds up as the temperature cycles, leading to cracks. Implications for design rules and qualification tests are discussed.

11:45 AM D1.10
X-RAY MICROTOPOGRAPHY FOR VLSI. P.-C. Wang, IBM Microelectronics Division, Hopewell Junction, NY; I.C. Noyan, S.K. Kaldor, J.L. Jordan-Sweet, E.G. Liniger, C.-K. Hu, IBM Research Division, Yorktown Heights, NY.

X-ray microbeam topography has been developed and employed to characterize the stress transfer between metal thin-film features and their single-crystal substrates. This system is equipped with a tapered glass capillary for condensing x-rays, precision sample translation stages ($\pm 1\mu$m), high-power microscopes, and detectors for collecting diffraction and fluorescence signals for topographic and elemental information. Due to its excellent strain sensitivity ($\sim 10^{-7}$) and strong diffraction signal from substrates, this technique is well suited for real-time probing of minute strain changes at the film/substrate interface resulting from the stress in thin-film features. Local stress distribution in metallization structures can be measured with micron-scale spatial resolution. We describe the application of x-ray microtopography to the study of electromigration in aluminum-based conductor lines.

SESSION D2: INTERCONNECT RELIABILITY
Monday Afternoon, April 24, 2000
Golden Gate B2 (Marriott)

1:30 PM *D2.1
ELECTROMIGRATION CHARACTERISTICS OF MULTILEVEL DAMASCENE ELECTROPLATED COPPER METALLIZATION. H.S. Rathore and D.B. Nguyen, IBM Microelectronics, Hopewell Junction, NY.

Copper metallization has been implemented for BEOL interconnects, and reported by many due to its excellent conductivity which is required for sub-quarter micron high performance products. The process integration of copper metallization will be reiviewed. The reliability data on copper metallization will be reviewed in details on the key concerns like electromigration, stress migration, and studies of copper metallization on electrical and thermal activation energies for current and temperature acceleration dependence. CMOS technology with copper interconnects and up to six copper wiring levels have been built at the minimum pitch of 0.63 um, 1.80 volts. The integrated copper hardware has been successfully tested for reliability. The electromigration data of copper which was deposited by different techniques such as Chemical Vapor Depositopn (CVD), Physical Vapor Depostion (PVD), and Electro-Plated (EP) copper integrated with dual damscene patterning method will be shown. Copper fine line using in this study was encapsulated by conductive metallic liners and the top side is insulated by silicon nitride. Tha sample length is 400 um, and interconnected with higher and lower levels by using dual damascene interlevel vias. The activation energy of electroplated copper for electromigration has been found to be higher than aluminum (delta H = 1.0 eV), and current acceleration coefficient seemed to be lower than aluminum (n= 1.1).

2:00 PM *D2.2
CIRCUIT-LEVEL AND LAYOUT-SPECIFIC INTERCONNECT RELIABILITY ASSESSMENTS. C.V. Thompson, S.P. Hau-Riege, V.K. Andleigh and C.S. Hau-Riege, Dept. of Materials Science and Engineering, M.I.T., Cambridge, MA; Y. Chery and D.E. Troxel, Dept. of Electrical Engineering and Computer Science, M.I.T., Cambridge, MA.

We have developed a methodology and a prototype tool for making computationally efficient circuit-level assessments of interconnect reliability. A key component of this process has been the development of simple analytic models that relate the reliability of the complex structures in layouts to the simpler straight, junction-free lines of

uniform width that are typically used in lifetime tests. We have considered interconnect trees as the fundamental reliability units, where trees can have multiple junctions and limbs, and can also have width variations. We have developed analytic methods for identifying trees which are immune to failure, and have demonstrated that computationally simple techniques lead to the identification of a large fraction of the trees in a circuit as immune to failure (i.e., that they are 'immortal'). These trees therefore need not be considered in further analyses. Using simulations and analytic treatments we have also developed default models which allow estimation of the reliability of the remaining trees. These models have been tested and validated through experiments on simple tree structures with junctions and line-width transitions. Our prototype circuit-level reliability analysis tool projects the reliability of circuits based on specific layouts, and provides a rank listing of the reliability of mortal trees. This allows the user to accept the assessment as is, to carry out more accurate but computationally-intensive analyses of the least reliable trees, or to modify the layout or process to address reliability concerns and reanalyze the reliability.

2:30 PM D2.3
ELECTROMIGRATION RELIABILITY OF DUAL-DAMASCENE Cu/OXIDE INTERCONNECTS. E.T. Ogawa, A. Bierwag, K.-D. Lee, A. Ramamurthi, H. Matsuhashi, P. Justison, and P. S. Ho, Univ. of Texas, Center for Materials Science, Austin, TX; V.A. Blaschke, SEMATECH (Conexant, Inc.), Austin, TX; R.H. Havemann, SEMATECH (Texas Instruments, Inc.), Austin, TX.

Proper assessment of Cu/oxide dual-damascene reliability in terms of test structures, testing system, and methodology will be critical to its successful integration into mainstream interconnect technology. We will present recent results obtained using dual-damascene Cu/oxide test structures designed at UT-Austin and fabricated at Sematech. The novel test structure is designed to examine the presence of critical length effects and has also proved useful to evaluate via and/or CMP-interface reliability under electromigration stress conditions. The advantages of this test structure design include shorter testing periods, sharper failure window, and potentially scalable analysis to ULSI interconnect structures. The linewidth examined is 0.5 μm with line lengths varying from 10 to 300 μm. The samples have been tested at temperatures 220, 275, and 325 $^{\circ}$C using a current density of 1.0×10^6 A/cm^2. The test structures are shown to be more resistant to electromigration damage than in typical Al(Cu)/oxide interconnects, and its lifetime characteristics are also comparable to those observed by others. Failure analysis shows that the failure sites are preferentially associated with the region near the via bottom between metal 1 (M1) and metal 2 (M2) level. Extrusions at the anode end of the interconnect lines are also observed. Another failure mode is the failure of the CMP-interface located at the top of M2 level where the apparent flow of Cu material between adjacent lines generates line shorts. Hence, test structure failure is characterized by a race between the two failure modes. Activation energy and current density exponent have also been examined.

2:45 PM D2.4
ELECTROMIGRATION CHARACTERIZATION VERSUS TEXTURE ANALYSIS IN DAMASCENE COPPER INTERCONNECTS. Thierry Berger, ST Microelectronics, Grenoble, FRANCE; Lucile Arnaud, LETI CEA-G, Grenoble, FRANCE; Roberto Gonella, ST Microelectronics, Crolles, FRANCE; Isabelle Touet, LETI CEA-G, Grenoble, FRANCE; Gerard Lormand, GEMPPM-INSA, UMR CNRS 5510, Villeurbanne, FRANCE.

We have studied the effect of texture and grain size distribution on the electromigration performances of Copper Damascene interconnects. Three different metallizations have been characterized : CVD copper deposited on CVD TiN and electroplated (ECD) copper deposited either on PVD Ta or PVD TaN. All metallizations are passivated using silicon oxide. Texture and its dependence versus linewidth was studied using X-ray pole figures. For wide polycristalline lines (1 to 4μm), ECD copper exhibits a strong $< 111 >$ bottom fiber texture whatever the barrier layer is (i.e the $< 111 >$ crystallographic directions are perpendicular to the bottom of the damascene trench). Moreover, the $< 111 >$ texture is slightly stronger for ECD Cu on Ta. On the other hand, CVD copper deposited on CVD TiN presents a weak $< 200 >$ bottom fiber texture. For narrower lines (width $< 1\mu$m), a $< 111 >$ sidewall fiber texture appears in ECD copper whereas the CVD copper is nearly isotropic. The mean grain size is much larger in ECD copper than in CVD copper. The reliability performance of these interconnects has been evaluated using both Wafer Level Reliability and Package Level Reliability tests on 4 and 0.6 μm wide lines using one metal level test structures. Considering the activation energies (ECD/TaN : 0.45 eV, CVD/TiN : 0.7 eV, ECD/Ta : 0.36 eV) obtained for 4 μm wide lines where the bottom fiber texture is quite similar to what is observed in etched Al-Cu lines, texture and grain size distribution do not seem to be the key factors ruling the electromigration phenomenon : failure analysis gives evidences of interface diffusion for the two metallizations including ECD copper and of grain boundary diffusion in CVD copper. This work has been carried out within the GRESSI consortium between CEA-LETI and France Telecom CNET.

3:15 PM *D2.5
VIA ELECTROMIGRATION LIFETIME IMPROVEMENT OF ALUMINUM DUAL-DAMASCENE INTERCONNECTS BY USING SOFT LOW-K ORGANIC SOG INTERLAYER DIELECTRICS. Hisashi Kaneko, Takamasa Usui, Sachiyo Ito and Masahiko Hasunuma, Microelectronics Engineering Laboratory, Toshiba Corp., Yokohama-City, JAPAN.

The via electromigration (EM) reliability of aluminum (Al) dual-damascene interconnects by using Niobium (Nb) new reflow liner is described. It has been found that the EM lifetime was improved by introducing low-k organic spin on glass (SOG)-passivated structure than the conventional TEOS-SiO_2/SiN-passivated structure. Higher EM activation energy of 1.08 eV was obtained for the SOG-passivated structure than the TEOS-passivated structure of 0.9 eV, even though no significant Al micro-crystal structure difference was found for both structures. It has been turned out that the low-k SOG material has the 1/7 Young's modulus (8 GPa) of TEOS SiO_2 (57 GPa) or thermal SiO_2 (70 GPa). The small Young's modulus means that SOG is more elastically deformable than TEOS or thermal SiO_2. This elastic deformation of the low-k SOG could retard the tensile stress evolution due to the Al atom migration near the anode via, and elongated the time until the Al interconnect tensile stress exceeds the critical stress value for void nucleation. It has been concluded that the small-RC and reliable multi-level Al interconnect can be realized by the Nb-liner reflow-sputtered process with soft and low-k SOG dielectric materials.

3:45 PM D2.6
STRESS MIGRATION BEHAVIOUR OF MULTILEVEL ULSI AlCu-METALLIZATIONS. A.H. Fischer, A. von Glasow, A.E. Zitzelsberger, Infineon Technologies, Reliability Methodology, Munich, GERMANY.

With decreasing geometries of metal lines and contacts, the demands on metallization reliability in ULS-ICs increases rapidly. Besides electromigration additional reliability concerns become severe in connection with stress-induced voiding, influencing lifetime and functionnality of integrated circuits. The driving force of the stressvoiding process is mechanical stress due to thermal mismatch between metallization and encapsulating dielectrics. This paper summarizes investigations on 4-level AlCu-metallizations of a 0.20μm embedded DRAM technology. The first part of investigations was focused on the stressmigration behaviour of meander shaped line structures with different line widths. Critical resistance drifts were observed during high temperature storage tests (HTS) on wafer level in certain metal layers. It was found, that the drift behaviour depends not only on the line width but on the chip position on the wafer as well. Illustrative wafer maps will be presented in the paper. Further on, HTS test were performed at different temperatures. For an estimation of stressmigration-limited lifetime the activation energy of the effective diffusivity E_a was determined using the model proposed by T. Sullivan: $MTF = A \bullet (1/(\Delta T)^2) \bullet \exp(E_a/kT)$ where MTF is the median time to failure of the sample (5% resistance drift defines the failure time of one specimen), A a constant, ΔT the difference between oxide deposition and HTS temperature T, and k Boltzmann's constant. It was proved, that critical resistance drifts were caused by stress voids, developing in the metallization after a HDP SiO_2 process. The appearance of stress-voids could be suppressed reducing the HDP deposition temperature in addition to an anneal, introduced after metal patterning. In the second part HTS tests were performed on different types of stacked-via chains. Critical resistance drifts were found for stack-architectures using small or no landingpads. In contrast, stacks with large or special shaped landingpads showed no critical drifts.

4:00 PM D2.7
A PERCOLATIVE APPROACH TO ELECTROMIGRATION MODELLING. C. Pennetta, L. Reggiani, Gyorgy Trefán, Lecce University, Dept. of Innovation Engineering, Lecce, ITALY; F. Fantini, Modena University, Dept. of Engineering Sciences, Modena, ITALY; A. Scorzoni, Perugia University, Dept. of Electronic and Information Engineering, Perugia, ITALY; I. DeMunari, Parma University, Centro MTI, Parma, ITALY.

We present a new stochastic method which simulates electromigration (EM) damage in metallic interconnects by biased-percolation of a random resistor network. This approach not only reproduces the phenomenological behavior of EM, including Black's law and the log-normal distribution of the times to failure but it also provides an insight in specific stochastic features of degradation e.g. damage patterns, resistance evolutions, noise spectra, etc. The region of degradation in a metallic interconnect is described by a

two-dimensional square-lattice network of initially identical resistors deposited on an insulating substrate. The network is subjected to a constant stress current. The electromigration damage and corresponding void growth is simulated by the generation of defects (broken resistors) introduced according to a thermally activated probability related to the local current. Healing is simulated by recovering network defects by another thermally activated process characterized by a suitable activation energy, in general different from that associated with damaging. The iteration process of defect generation and recovery is repeated until the network breaks down by becoming an open circuit. The simulations yield evolutions of the damage patterns and the network resistance. The damage pattern results show spatial correlations around growing voids. Results on electrical resistance evolutions depending on the current stress exhibit various scenarios. For instance at high currents an abrupt failure occurs, at intermediate currents the failure is preceded by violent resistance bursts, and at low currents steady-state conditions are reached. These resistance evolutions were also observed in EM experiments on Al-0.5% Cu lines. Simulations with a sudden interruption of the stress current were executed where drops in the resistance associated with the role of healing were found. The agreement between simulations and experiments is encouraging. The flexibility of the approach offers new possibilities of improving EM modelling with the aim to include geometrical, compositional and structural effects which are often present during EM.

4:15 PM D2.8
THE RELIABILITY EFFECTS OF DIFFERENT LENGTH RATIOS IN INTERCONNECTS WITH NARROW-TO-WIDE TRANSITIONS. Christine S. Hau-Riege, Carl V. Thompson, Massachusetts Institute of Technology, Cambridge, MA; Thomas N. Marieb, Intel Corporation, Portland, OR.

Interconnect reliability is usually assessed through lifetime tests on straight stud-to-stud lines with fixed widths. However, real interconnects often have junctions with narrow-to-wide transitions. We have carried out experimental and modeling-based studies of interconnects with narrow-to-wide transitions. Two-level Al-0.5%Cu electromigration structures with narrow-to-wide width transitions have been studied as a function of transition location (L_x) while fixing the total line length, and narrow and wide line-widths. The narrow-to-wide transition was found to be a site of atomic flux divergence due to the discontinuity in diffusivities between the narrow and wide segments, which have bamboo and polygranular microstructures, respectively. Consequently, it was found that lifetime decreases with L_x for structures with an L_x below a critical distance, due to an increased interaction between the stress evolution at the electron-source via and the stress evolution at the width transition. Narrow-to-wide structures with an L_x greater than a critical distance have much higher lifetimes which are not a function of transition location due to a lack of interaction between the electron-source via and the width transition. Because the mode of failure was identical for all structures (i.e. failure by voiding at the electron-source via), we are able to couple experimental results with simulations to determine that the critical stress range for void-nucleation-failure is 600 ± 108 MPa.

4:30 PM *D2.9
NOVEL LOW-k MULTIPHASE MATERIALS PREPARED BY PECVD. A. Grill and V. Patel, IBM-T.J. Watson Research Center, Yorktown Heights, NY.

Low-dielectric constant (low-k) materials comprised of Si, C, O and H, (SiCOH films) and prepared by plasma enhanced chemical vapor deposition (PECVD) have been demonstrated by different authors. These ("single phase") materials are characterized by dielectric constants not less than about 2.8, almost independent on the used precursor or deposition system. Further lowering of the dielectric constant could potentially be achieved by increasing/introducing porosity in the films. Such enhanced porosity could be produced by depositing multiphase films containing at least one thermally-unstable phase and annealing the films to remove this labile phase from the material. Dual phase materials have been prepared in the present study by PECVD from mixtures of SiCOH precursors with gases containing mainly C and H. The films have been characterized as-deposited and after thermal anneals of up to 8 hours at 400°C. The atomic composition of the films has been determined by RBS and FRES analysis and their optical properties have been determined by FTIR and n&k measurements. The dimensional stability has been determined by measuring the changes the step heights produced in the films. Metal Insulator Silicon (MIS) structures have been used to test the electrical properties of the dual-phase films. After an initial anneal accompanied by a significant loss of CH and some SiH bonds and a thickness loss of up to 40% the films stabilized. Depending on the deposition conditions and concentration of the CH compound in the feed gas the dielectric constant decreased by 10-15% during the stabilization anneal and reached values as low as 2.4. These initial results indicate the possibility to further reduce the dielectric constant of PECVD produced SiCOH films and the potential to incorporate such films in the interconnect structures of future ULSI chips.

SESSION D3: LOW-k DIELECTRICS
Tuesday Morning, April 25, 2000
Golden Gate B2 (Marriott)

8:30 AM *D3.1
PROCESS OPTIMIZATION AND INTEGRATION OF TRIMETHYLSILANE DEPOSITED a-SiC:H AND SiOC:H DIELECTRIC THIN FILMS FOR DAMASCENE PROCESSING. W.D. Gray, IMEC, Dow Corning Corporation, Midland, MI; M. Loboda, Dow Corning Corporation, Midland, MI; H. Struyf, M. Van Hove, R.A. Donaton, E. Sleeckx, M. Stucchi, T. Gao, W. Boullart, B. Coenegrachts, M. Maenhoudt, S. Vanhaelemeersch, IMEC, Heverlee, BELGIUM; H. Meynen, Dow Corning, Seneffe, BELGIUM; K. Maex, ESAT-INSYS, Katholieke Universiteit Leuven, BELGIUM.

The organosilicon gas trimethylsilane can be used to deposit unique Si-C based alloy films that exhibit desirable properties such as chemical resistance, low stress, low permittivity and low leakage. These film characteristics are ideal for applications in Cu-damascene interconnect technology. In this work, the results of a comprehensive study of trimethylsilane (3MS) PECVD deposited dielectric films are reported. Depositions were performed in commercial production PECVD equipment. Process for a-SiC:H films deposited from 3MS/He mixtures has been optimized for deposition rate, uniformity, and permittivity. The processing parameters can be tuned for relative permittivity down to k≈4.2 making a-SiC:H an attractive substitute for PECVD oxide. Using mixtures of 3MS and N2O, a-SiCO:H films are deposited, with very high deposition rates and film permittivity as low as k≈2.5 suggesting suitability for use as an ILD layer in damascene technology. Physical properties and stability of blanket films have been studied. Measurement of relative permittivity, leakage current, and breakdown voltage was performed on metal/insulator/metal (MIM) structures. FTIR, Auger, and high-energy ion scattering spectrometry (RBS/ERD) were used to determine bonding and film compositions. Integration issues related to DUV lithography, dry etch, strip, and metallization will be discussed. Optimized film processes were integrated into 0.18 μm Cu Damascene interconnect process technology and the electrical results compared to standard PECVD oxide. The results of these studies indicate that the device performance improvements inferred from the blanket film properties can be realized in fully integrated interconnect structures.

9:00 AM *D3.2
ON THE MECHANICAL INTEGRITY OF ULTRA LOW DIELECTRIC CONSTANT MATERIALS FOR USE IN ULSI BEOL STRUCTURES. E.O. Shaffer II, K.E. Howard, M.E. Mills and P.H. Townsend, The Dow Chemical Company, Advanced Electronic Materials, Midland, MI.

Adherence to the prescript of Moore's law continues to drive materials development for new and lower dielectric constant materials for use as back-end-of-line (BEOL) interlayer dielectric in advanced logic IC's. As is the case for the current generation of low-K materials (<3.0), these ultra-low K materials (<2.2) will need to meet the variety of integration and reliability requirements for successful product development. Excluding the incorporation of fluorine to lower the material polarity, further reductions of dielectric constant can only be achieved by reduced density. Based upon the industry's experience with the current class of full density dielectrics, process integration may be challenging for ultra-low K materials. This anticipated difficulty derives from the profound differences in material properties, e.g. mechanical integrity, as one lowers the material density, which in turn confounds existing manufacturing processes that have evolved over 35 years based on silicon dioxide. Minimizing these material and processing differences by extending leveraged learning from previous technology nodes is essential for timely and cost-efficient development cycles. As a result, material selection of a full density low-K is somewhat influenced by the ability of that material to be extended into future generations. Understanding how the material properties will change as its density is lowered is vital to this selection process. In this paper, we present a summary of models for calculating effective properties as a function of density and apply these to current low-K materials with emphasis on mechanical integrity. We will also review experimental methods for measuring the mechanical integrity of ultra-low K materials and compare the results to the various models described herein.

9:30 AM D3.3
STUDY OF SiH4-BASED PECVD LOW-K CARBON-DOPED SILICON OXIDE. Hongning Yang, Douglas J. Tweet, Lisa H. Stecker, David R. Evans and S.-T. Hsu, Sharp Laboratory of America, Camas, WA.

Recent research development indicates that PECVD carbon-doped silicon oxide (SiOC) has been emerging as one of the best low dielectric candidates for delivering the required performance in future IC interconnects. In previous studies, SiOC films were deposited using organosilicon precursor: $(CH_3)_xSiH_{4-x}$ [1]. In this talk, we present the properties of PECVD low-k SiOC films produced by using conventional SiH_4 based gas precursors. Since the precursors are inexpensive, commercially available and convenient to operate for existing tools, the process should not require additional cost as compared with that of PECVD silicon dioxide. The SiH_4 based SiOC films have similar gross physical and electrical characteristics to those of $(CH_3)_xSiH_{4-x}$ based SiOC. The dielectric constant ranges from 2.7 to 3.1 with density from 1.4 to 1.7 g/cm^3 correspondingly. Leakage current is measured in the order of $\sim$ nA/cm^2 at a field of 1 MV/cm. The films are stable against thermal anneal at $>$ 400 C. Post anneal for as-deposited film may not be necessary if appropriate process conditions are chosen. We shall demonstrate the feasibility for the integration of Cu/SiOC on dual damascene interconnection. Two types of dual damascene structures, Cu/SiOC/SiOC and Cu/SiOC/SiO_2, have been studied. Related dry etching issues will be discussed. Finally, the evaluation on electrical performance of the Cu/SiOC based dual damascene structure will be presented. [1] M. Loboda, in Advanced Metallization Conference, Orlando, FL, 1999.

9:45 AM D3.4
CHARACTERIZATION OF $SiO_xC_yH_z$ LOW K FILMS PREPARED BY PECVD OF ORGANOSILANE COMPOUND. Ju-Hyung Lee, Nasreen Chopra, Jim Ma, Yung-Cheng Lu, Ralf Willecke, Tzu-Fang Huang, Wai-Fan Yau, David Cheung and Ellie Yieh, Applied Materials, Santa Clara, CA.

A CVD-based low k film was evaluated for inter-metal dielectric in $<$ 0.18 μm generation devices. The film was prepared by conventional rf PECVD method using organosilane compound and oxidizer. The film was then thermally treated at 400°C to obtain desirable electrical, mechanical and thermal characteristics. The dielectric constant of the film after the thermal treatment was 2.7-2.8. The k value of the film was stable over several weeks and the moisture absorption was minimal. The chemical composition was in the form of $SiO_xC_yH_z$, where the carbon content was less than 10 atomic %. The low carbon content of the film is believed to possess a significant advantage in eliminating potential carbon related integration issues, which includes CMP and ashing difficulties. Blanket films were used to find out the integration characteristics of the film. The largest increase in k value during the integration occurred during etching and ashing steps and it was found that the damage from these steps was limited to within 300 Å at the top surface. The initial low k value, however, was recovered after the top damaged layer was removed by CMP. The deposition temperature dependence of the film characteristics was also determined. The k value was increasing with temperature while the Si-CH_3 and Si-H bonds were decreased. The film density was measured ranging from 1.4-1.6 g/cm^3 as compared 2.3 of conventional SiO_2 film. The AFM images of the deposited film indicate smooth surface morphology and the roughness was comparable to that of the conventional SiO_2 film deposited by PECVD method.

10:30 AM *D3.5
CHARACTERIZATION OF MSQ-BASED LOW-K DIELECTRIC MATERIALS. Michael Kiene, Taiheui Cho, Dongwen Gan, Chuan Hu, Junjun Liu, Jie-hua Zhao, Paul S. Ho, Microelectronics Research Center, University of Texas at Austin, Austin, TX; Changming Jin, Robert J. Fox III, Jeffrey T. Wetzel, SEMATECH Inc., Austin, TX.

In order to identify promising low-k dielectric materials, which satisfy the needs for process integration into Cu low-k interconnect structures extensive efforts have been made to characterize a wide variety of materials. Beside many others dielectric, thermal and mechanical properties are some of the most critical. Among the low-k materials characterized recently at the University of Texas in collaboration with SEMATECH, two groups of materials have been studied extensively. Methyl-silsesquioxane (MSQ)- based porous materials and CVD carbon doped oxides, which have a composition similar to MSQ as well. The chemistry and the carbon content have been investigated using FTIR and XPS, for carbon doped oxides deposited with different precursors and process conditions. These results will be related to the dielectric constant, the thermal and mechanical properties as well as thermal conductivity and adhesion. For the porous materials the dielectric constant is related to the thermal and mechanical properties. As moisture uptake appears to be critical for the materials discussed, direct measurements of the moisture uptake using a quartz crystal microbalance and the dependence of the dielectric constant on various annealing cycles will be presented.

11:00 AM D3.6
SYNTHETIC CONTROL AND PROPERTIES OF PROCESSIBLE POLY(METHYL-SILSESQUIOXANE). J.-K. Lee, H.J. Kim, H.W. Ro, D.Y. Yoo, D.Y. Yoon, Department of Chemistry, Seoul National University, Seoul, KOREA; K. Char, School of Chemical Engineering, Seoul National University, Seoul, KOREA; H.-W. Rhee, Department of Chemical Engineering, Sogang University, Seoul, KOREA.

Processible poly(methyl-silsesquioxanes) (PMSSQ), $(MeSiO_{1.5})_n$, were prepared by acid-catalyzed hydrolytic condensation of methyltrialkoxysilane, $MeSi(OMe)_3$ and $MeSi(OEt)_3$. Molecular weight of polymers was controlled by the molar ratio of water/ methyltrialkoxysilane and catalyst/methyltrialkoxysilane, and polymerization was stopped before the gelation occurred in order to obtain processible polymers. Solvents had a great effect on the polymerization rate, and the relative amount of water and alcohol produced during the polymerization also affected the molecular weight of polymers. Moreover, hydrolysis of alkoxysilane and alcoholysis of hydroxysilane were shown to result in an equilibrium state of molecular weight distribution, as confirmed by NMR and GPC experiments. PMSSQ samples of very narrow molecular weight were then prepared by fractionation of the as-polymerized sample, which exhibits a very broad molecular weight due to the polycondensation process. The effects of the molecular weight fractions on the mechanical, electrical and surface properties of the final PMSSQ films will be discussed.

11:15 AM D3.7
PLASTIC ENERGY DISSIPATION IN DUCTILE POLYMER LOW-K FILMS. Christopher S. Litteken and Reinhold H. Dauskardt, Department of Materials Science and Engineering, Stanford University, Stanford, CA.

New dielectric layers are required to increase the performance and decrease the manufacturing cost of interconnects in microelectronic devices. One strategy is to employ oxides or organic/inorganic hybrids both of which tend to be brittle and have a low fracture resistance. Alternatively, new thermoset polymers (SiLK, Dow Chemical) show promise as a class of low-k materials with associated mechanical ductility and fracture resistance. In the present study, macroscopic adhesion was measured in terms of the critical strain energy release rate (G_c) of a stable debond located at the interface between SiLK and selected barrier or metal layers. In previous work, plastic deformation of ductile metal layers was shown to significantly contribute to G_c, however, the benefit of such energy dissipation is not always observed for very thin layers of interest to the microelectronics industry due to dislocation strengthening mechanisms. Alternatively, polymer yield properties are not dominated by the same strengthening mechanisms and can be controlled with chemistry and curing. Accordingly, the adhesive and mechanical properties of SiLK films were investigated in order to understand the plastic energy contribution to adhesion. The dependence of yield stress and macroscopic adhesion is described in terms of cross-link density, film thickness, and polymer chemistry.

11:30 AM D3.8
THEORETICAL AND EXPERIMENTAL ANALYSIS OF THE LOWER DIELECTRIC CONSTANT OF FLOURINATED SILICA. Alex Demkov, Ran Liu, Stefan Zollner, Dennis Werho, Mike Kottke, Rich Gregory, Semiconductor Product Sector, Motorola, Inc. Mesa, AZ; Matt Angyal, Semiconductor Product Sector, Motorola, Inc., Austin, TX; L.C. McIntyre Jr., M.D. Ashbaugh, Department of Physics, University of Arizona, Tucson, AZ.

The fluorinated silica (FTEOS) is known to have the dielectric constant in the range of 3 to 3.5 that is significantly lower than that of the fluorine free material (4). The reasons behind the reduction of the dielectric constant are not very well understood and are somewhat controversial. It is not known exactly whether the electronic or ionic contributions to the overall screening is being diminished upon the fluorine doping. To shed more light on this phenomenon we have studied FTEOS both theoretically with ab-initio modeling and experimentally with various characterization techniques. Far-IR transmission and spectroscopic ellipsometry measurements gave us the electronic and ionic contributions to the susceptibility. Nuclear reaction analysis was used to measure fluorine composition. XPS and Auger experiments provided the information on the atomic structure of the film. We use a large cell of cristobalite to model fluorinated silica theoretically. The ground state geometry is obtained via the energy minimization. Two types of Fluorine have been found; a bridging fluorine acts just as an oxygen atom, and forms two Si-F bonds (0.159 nm, and 0.162 nm). In addition, we find a terminal fluorine atom that forms only one bond to Si (0.152 nm). As a result a nano-pore forms in the simulation cell. Analysis of the Si-O-Si bond angle distribution in the cell shows that even though the average angle of 147° is still very similar to that in fluorine free cristobalite angles as low as 120° and as high as 170° are introduced to the system. We calculate the vibrational density of states at the Gamma point, and analyzed the modes using the inverse participation ratio (IPR) (IPR indicates localized modes). We find a strongly localized mode at 935

cm^{-1}, this vibration involves the terminal fluorine. The calculated frequency agrees well with the 938 cm^{-1} value measured by far-IR transmission, and with the Si-F stretch reported in the literature [1,2]. The presence of terminal fluorine atoms without the formation of dangling Si bonds puts special requirements on the framework topology, and on the maximum Fluorine concentration resulting in a stable network. We will discuss these geometrical constraints. We compute the electronic and the ionic susceptibilities for models with various fluorine concentrations. The effect of fluoridation on the dielectric constant will be discussed. [1] K. Kim, D. H. Kwon, G. Nallapati, and G. S. Lee, J. Vac. Sci. Technol. A16, 1509 (1998). [2] G. Lucovsky and H. Yang, J. Vac. Sci. Technol. A15, 1509 (1997).

11:45 AM D3.9
PROPERTIES OF THE OXAZOLE DIELECTRIC OxD; INTEGRATION STUDIES INTO DAMASCENE COPPER ARCHITECTURES. Recai Sezi, Guenter Schmid, Infineon Technologies AG, Dept. Corporate Research, Erlangen, GERMANY; Heinrich Koerner, Manfred Engelhardt, Hans Helneder, Michael Schrenk, Markus Schwerd, Uwe Seidel, Infineon Technologies AG, Dept. Wireless Products, Munich, GERMANY.

This paper presents the study of the organic low-k material Oxazole Dielectric (OxD) including its thermal, chemical, electrical and mechanical properties. The suitability of OxD for a damascene architecture has been assessed by investigating its properties after various plasma treatments and by integration of OxD with copper. The precursor of OxD is a Poly(o-hydroxy)amide which is converted to Oxazole Dielectric by thermal cure at $T \geq 350°C$. The dielectric layer adheres excellently to PECVD-SiO_2, -SiN, TaN and TiN. Typical stress values at 25°C are 35 MPa and the layers are thermally stable up to 500°C. The dielectric constant k was determined to be 2.5 by means of impedance spectroscopy. The k-value is almost independent of frequency in the range of up to 10 MHz and it does not change after temperature cycling at 450°C. GC/MS investigations at 400°C showed only low amount of outgassing molecules which do not influence the properties of OxD after being integrated into the damascene structure. The impact of Ar, CF_4 and O_2 plasma treatments on the bulk and surface composition and properties of OxD were determined by XPS spectra and Atomic Force Microscopy. The patterning of OxD is feasible for Single and Dual Damascene architectures. The SEMs demonstrate the excellent selectivity of the OxD patterning process towards SiO_2. Vias and trenches show smooth sidewalls and bottoms. The dimension control of both features is perfect. Electrical characteristics of copper lines embedded in OxD after CMP processing, were investigated. Meander line resistances as well as leakage current measurements between unpassivated copper comb and serpentine structures gave very good results. These results are attributed to proper control of the overall process flow, to a minimum dishing and erosion during CMP processing as well as to the fact that degradation of copper by OxD does not occur during processing.

SESSION D4: LOW-k DIELECTRICS–POROUS MATERIALS
Tuesday Afternoon, April 25, 2000
Golden Gate B2 (Marriott)

1:30 PM *D4.1
CHARACTERIZATION OF NANOPOROUS THIN FILMS USING X-RAY AND NEUTRONS. Wen-li Wu, Eric Lin, William E. Wallace, NIST, Polymer Division, MSEL, Gaithersburg, MD.

A new methodology to characterize nanoporous thin films has been developed. More specifically, the average pore size, pore connectivity, film thickness, pore wall density, coefficient of thermal expansion and moisture uptake can now be measured using this newly developed methodology which is based on a novel combination of small angle neutron scattering (SANS), high resolution x-ray reflectivity (HRXR), and ion scattering techniques. The measurements can be performed directly on films supported on silicon substrates. HRXR is used to accurately measure the film thickness, electron density, and the coefficient of thermal expansion. SANS is used to determine the pore structure and to provide information such as the average pore size, pore connectivity, and moisture absorption. Ion scattering techniques are used to determine the elemental composition of the films. We have successfully determined the pore structure of films less than 0.5 μm thick By combining information from all three of these techniques, we provide the first measurements of important quantities such as the porosity and the pore wall density. So far this method has been performed successfully over a wide range of materials developed by industries for low-k dielectrics.

2:00 PM *D4.2
CHARACTERIZATION OF POROUS LOW-K DIELECTRIC FILMS BY ELLIPOSOMETRIC POROSIMETRY. M.R. Baklanov, IMEC, Leuven, BELGIUM; K.P. Mogilnikov, Institute of Semiconductor Physics, Novosibisrk, RUSSIA.

Ellipsometric porosimetry (EP) is a new, simple and effective method for the measurement of the average pore size, inner surface area, relative amount of open and close pores (pore interconnectivity) and pore size distribution in thin porous films deposited on top of any smooth solid substrate. Because a laser probe is used, small surface areas can be analyzed. Therefore, EP can be used on patterned wafers and it is compatible with microelectronic technology. This method is a new version of adsorption (BET) porosimetry. *In situ* ellipsometry is used to determine the amount of adsorptive which adsorbed/ condensed in the film. Changes in refractive index and film thickness are used to calculate of the quantity of adsorptive present in the film. Ellipsometric porosimetry allows also study the thermal, adsorption and swelling properties of low-K dielectric film. Such type phenomena are demonstrated for the low-K SiLK dielectric film. Comparison of elastic properties of different low-K dielectric films has also been carried out from results of the EP measurements.
Room temperature EP based on adsorption of vapor of some organic solvents has been developed. Method of calculation of porosity and pore size distribution and results of measurements on mesoporous and microporous xerogel films and mesoporous FOx films are discussed. Examination of the validity of Gurvitsch rule for various organic adsorptives (toluene, heptane and carbon tetrachloride) is carried out to assess the reliability of measurements of pore size distributions by ellipsometric porosimetry.

2:30 PM *D4.3
PROBING PORE CHARACTERISTICS IN LOW-K THIN FILMS USING POSITRONIUM ANNIHILATION LIFETIME SPECTROSCOPY. David Gidley, William Frieze, University of Michigan, Department of Physics, Ann Arbor, MI; Terry Dull, Jianing Sun, Albert Yee, University of Michigan, Department of Materials Science and Engineering, Ann Arbor, MI; Todd Ryan, Huei Min Ho, Sematech, Austin, TX; Catien Nguyen, IBM Almaden Research Center, San Jose, CA; Do Yoon, Seoul National University, Department of Chemistry, Seoul, KOREA.

Depth-profiled positronium annihilation lifetime spectroscopy (PALS) has been used to probe the pore characteristics (size, distribution, and interconnectivity) in thin, porous films, including silica and organic-based films. The technique is sensitive to all pores (both interconnected and closed) in the size range from 0.1 nm to 600 nm, even in films buried under a diffusion barrier. PALS may be uniquely capable of deducing pore-size distribution in closed-pore systems where gas absorption methods are not available. In this technique a focussed beam of several keV positrons forms positronium (Ps, the electron-positron bound state) with a depth distribution that depends on the selected positron beam energy. Ps inherently localizes in the pores where its natural annihilation lifetime of 142 ns is reduced by collisions with the pore surfaces. The collisionally reduced Ps lifetime is correlated with pore size and is the key feature in transforming a Ps lifetime distribution into a pore size distribution. In thin silica films that have been made porous by a variety of methods the pores are found to be interconnected and an average pore size is determined (see Gidley et al., Phys. Rev. B60, R5157 (1999)). In a mesoporous methyl-silsesquioxane film with nominally closed pores a pore-size distribution has been determined. The methodology and physical basis for PALS will be presented along with recent results. PALS is a non-destructive, depth-profiling technique with the only requirement that positrons can be implanted into the porous film where positronium can form. This research is supported by the National Science Foundation (ECS-9732804), SEMATECH, and the University of Michigan.

3:15 PM *D4.4
EVAPORATION-INDUCED SELF-ASSEMBLY OF MESOPOROUS BRIDGED POLYSILSESQUIOXANE FILMS WITH INTEGRAL ORGANIC FUNCTIONALITY. C. Jeffrey Brinker, Douglas A. Loy, Hongyou Fan and Darren Dunphy, Sandia National Laboratories, University of New Mexico, Advanced Materials Laboratory, Albuquerque, NM; Yunfeng Lu, Applied Materials, San Jose, CA.

Recently, through combination of sol-gel processing with self-assembly strategies our group has established an evaporation-induced self-assembly (EISA) route to the formation of highly ordered mesoporous films and nanoparticles. Compared to xerogels which may have average pore sizes of over 10-nm and a broad pore size distribution, mesoporous materials are characterized by a uni-modal pore size distribution controllable in the approximate range 2 - 10-nm. In addition, whereas the fractal nature of xerogel networks causes there to be many pendant arms that do not contribute to mechanical strength or thermal conductivity, mesoporous frameworks are completely mechanically and thermally connected. This paper describes extension of our EISA approach to hybrid, bridged

polysilsesquioxanes (BPSQ), in which organic moieties are covalently incorporated as bridging ligands. Starting with an oligomeric sol of BPSQ plus non-ionic surfactant prepared in an alcohol/water solvent with surfactant concentration less than the critical micelle concentration, preferential evaporation of alcohol during spin-coating results in self-assembly of micelles and further self organization into BPSQ/ surfactant liquid crystalline mesophases. Thermal or chemical treatments are used to condense the framework and remove the surfactant templates resulting in hybrid mesophases with integral organic functionality. In contrast to previous hybrids where organic ligands or molecules are situated on pore surfaces, this class of materials necessarily incorporates the organic constituents into the framework as molecularly dispersed bridging ligands. This new mesostructural organization is anticipated to result in synergistic properties derived from the molecular scale mixing of the inorganic and organic components. For example, the introduction of integral organic groups should impart toughness, hydrophobicity, and a reduced dielectric constant to the framework, while at the same time enhancing the thermal stability of the organic constituents.

3:45 PM D4.5

ULTRA LOW K MESOPOROUS SILICA FILMS: SYNTHESIS, DIELECTRIC PROPERTIES AND SINGLE-DAMASCENE EVALUATION. Suresh Baskaran, Jun Liu, Xiahong Li, Chris Coyle, Jerome Birnbaum, Glen Fryxell, Pacific Northwest National Laboratory, Richland, WA; Changming Jin, Sematech, Austin, TX.

Highly porous silica films with pore sizes in the nanometer scale are potentially useful as interlevel dielectrics with k in the range of 1.5 to 2.0. This presentation will discuss properties of mesoporous silica films prepared by the molecular templating approach. In this paper, we present information on (1) obtaining highly porous open-pore structures through control of solution/surfactant chemistry, (2) obtaining low dielectric constant in films synthesized using the surfactant templated approach and subjected to dehydroxylation treatments, and (3) single damascene evaluation of PNNL's mesoporous silica films at SEMATECH. Two primary conclusions at this stage: (1) With control of porosity and the pore surface functionalization, dielectric constants of k 1.90 may be achieved. (2) The mechanical integrity of mesoporous structures indicates significant promise for withstanding mechanical stresses in fabrication of interconnects. Further developmental work required to address potential performance limitations and integration challenges with open-pore structures will be briefly discussed.

4:00 PM D4.6

RECENT DEVELOPMENTS OF NANOGLASS^{TM} FOR LOW DIELECTRIC CONSTANT MATERIALS. H.J. Wu, J. Drage, D. Endisch, R. Katsanes, K. Beres, C.T. Chandler, M. Dinh, R. Roth*, T. Ramos*, S. Wallace*, D.M. Smith* and N. Rutherford, AlliedSignal, Sunnyvale, CA. *Nanopore, Albuquerque, NM.

The requirement for materials with dielectric constant much less than 4 for use in integrated circuits in the near future has been established. AlliedSignal's Nanoglass^{TM}, a nanoporous silica film, offers the ability to tune the dielectric constant from 3 to lower than 2 and thus offers the capability to be used for a number of future technology generations. Considerable progress has been made in the development of Nanoglass^{TM} for inter-metal dielectric (IMD) applications. However, the requirements for the materials in these applications are very stringent and continuous improvement is needed. Thermal stability, mechanical strength, and chemical resistance are among the most challenging requirements, just to name a few. We have recently developed new chemistry/processes to significantly improve mechanical strength, thermal stability, and chemical stability. Stud pull testing of our newly developed Nanoglass^{TM} indicates more than ten times improvement in cohesive strength. Excellent film uniformity as well as thermal stability at 425C are also demonstrated. This presentation will provide discussion on some of the challenges encountered during materials evaluation and integration as well as the properties of the newly developed materials.

4:15 PM D4.7

A MULTILEVEL METAL INTERCONNECT TECHNOLOGY WITH INTRA-METAL AIR-GAP FOR QUARTER-MICRON-AND-BEYOND HIGH-PERFORMANCE PROCESSES. Mark Lin, Chun-Yen Chang, Tiao-yuan Huang, Institute of Electronics, National Chiao Tung University, Hsinchu, TAIWAN; Mout-Lim Lin, United Semiconductor Corp., Hsinchu, TAIWAN; Horng-Chih Lin, National Nano Device Labs., Hsinchu, TAIWAN.

A multilevel metal interconnect with air-gap between metal lines, which has been successfully integrated into a quick turn-around-time 0.25um foundry manufacturing, is described. Three different types of intra-metal dielectric materials, i.e., high-density plasma (HDP) CVD-deposited SiO_2 ($k = 4.4$), low-k hydrogen silsesquioxane (HSQ, $k=3.3$), and the air-gap ($k=1$), were fabricated. Their performance and reliability (i.e., electromigration EM, and stress migration SM) were carefully studied. Samples with air-gap (i.e., voids) were fabricated by carefully tuning the SiO_2 deposition condition to form the voids between the metal lines, followed by another PECVD SiO_2 deposition to serve as the intermetal dielectric. Air-gaps with different sizes and vertical positions relative to the metal lines are reproducibly obtained. The metal lines consist of a 0.6um-thick TiN/AlCu/TiN stack layer. Ring oscillator measurements confirm that the smallest delay time is achieved with the air-gap split, compared to that using either HDP oxide or low-k HSQ. The oscillator delay time is also found to be critically dependent on not only the size, but also the relative position of the air-gap. Best delay time is obtained when the air-gap is positioned in the middle, and extended both above and below the metal lines to effectively reduce the fringing capacitance. EM and SM results show that extrapolated lifetime is over 100 years for all three splits, suggesting that reliable multilevel interconnect with air-gap is obtained. Detailed data will be presented at the conference.

4:30 PM D4.8

FABRICATION OF AIR-GAPS BETWEEN Cu INTERCONNECTS FOR LOW INTRALEVEL DIELECTRIC CONSTANT. Dhananjay Bhusari, Michael Wedlake, Paul Kohl, Georgia Institute of Technology, School of Chemical Engineering, Atlanta, GA; Carlye Case, Fred Klemens, John Miner, Lucent Technologies, Murray Hill, NJ; Byung-Chan Lee, Ronald Gutmann, Rensselaer Polytechnic Institute, Troy, NY; J.J. Lee, Motorola Inc, Austin, TX; Robert Shick, B.F. Goodrich Company, Brecksville, OH.

We present here a method for fabrication of air-gaps between Cu-interconnects to achieve low intralevel dielectric constant, using a sacrificial polymer as 'place holder'. IC compatible metallization and CMP processes were used in a single damascene process. The air-gap occupies the entire intralevel volume with fully densified SiO_2 as the planar interlevel dielectric. The width of the air-gaps between 600nm wide copper lines was 286nm. The effective intralevel dielectric constant was calculated to be 2.19. The thickness of the interlevel SiO_2 and copper lines were 1.1μm and 700nm, respectively. Further reduction in the value of intralevel dielectric constant is possible by optimization of the geometry of metal/air-gap structure, and by use of a low-k interlevel dielectric material. In this method of forming air-gaps, the layer of sacrificial polymer is spin-coated onto the substrate and reactive-ion-etched into the desired pattern using an oxide or metal mask. The intralevel Cu trench is then inlaid by using a damascene process, wherein the Ta/Cu barrier/seed layer is deposited by PVD while the bulk of Cu is electrochemically deposited. After the CMP of copper, interlevel SiO_2 is deposited by plasma-CVD. Finally, the polymer is thermally decomposed with decomposition products permeating through the interlevel dielectric material. The major advantages of this method over other reported methods of formation of air-gaps are excellent control over the geometry of air-gaps, no protrusion of air-gaps into the interlevel dielectric, no deposition of SiO_2 over the side-walls, and no degradation of the interlevel dielectric during the formation of air-gap. The process flow for creation of air-gaps between metal interconnects is described. Various issues pertaining to the thermal decomposition of the sacrificial polymer, diffusion of the decomposition products through the interlevel dielectric, residue left after decomposition of the polymer, effects of growth conditions of the dielectric etc. are discussed.

4:45 PM D4.9

LOW DIELECTRIC CONSTANT POROUS SILSESQUIOXANE FILM. Y.K. Siew, G. Sarkar, X. Hu, Div. of Materials Engineering, School of Applied Science, Nanyang Technological Univ., Singapore, SINGAPORE; Y. Xu and A. See, R&D Dept. Chartered Semiconductor Manufacturing Ltd., Singapore, SINGAPORE.

As the feature size on integrated circuits continues to scale down there is a need for intermetal dielectric materials with extremely low k to reduce crosstalk and allow for gigahertz frequency clock speeds. It is generally agreed that, dense materials, either organic or inorganic, could not deliver dielectric constant (k) < 2.0 without embracing the concept of porosity. As a result, processes to introduce nano-scale or molecular level porosity into existing materials which have acceptable physical properties (other than k) has become the primary focus for next generation dielectric materials. In this study, attempts have been made to prepare nanoporous silsesquioxane films from organic/ inorganic polymer hybrids. Two different low molecular weight, thermally labile organic polymers would be incorporated into hydrogen silsesquioxane (HSQ) resin and spin-coated onto Si substrate. Upon heating to about 300°C, HSQ resin cross-links around the polymer templates. Subsequent thermal treatment at higher temperature causes decomposition of the labile component and thus produces porous films. Thermal characterization tools such as thermogravimetric analyzer (TGA) and dielectric analysis (DEA) would be employed to investigate the effectiveness of these labile components in generating pores. It is very important to optimize the

porosity and morphology of the porous films for application as intermetal dielectric. Porosity of the films would be determined by measuring the refractive index and using the Maxwell-Garnett effective medium theory for spherical particles to calculate the volume fraction of the pores. MIM structure would be prepared for dielectric constant measurement for correlation between porosity and k value. The morphology of the pores would be assessed by XSEM and TEM.

SESSION D5: POSTER SESSION: LOW-k DIELECTRICS

Tuesday Evening, April 25, 2000
8:00 PM
Salon 1-7 (Marriott)

D5.1

PROCESSING, PROPERTIES, AND CMP CHARACTERISTICS OF SPIN-ON POLYMERS: POLY(SILSESQUIOXANES). Wei-Jung Lin, Chang-Jong Yang, Wen-Chang Chen, Department of Chemical Engineering, National Taiwan University, Taipei, TAIWAN.

Poly(Sil- sesquioxanes) such as HSQ, MSQ, and HOSP have potential applications as low k dielectrics. A few questions will be addressed in this study; (1) The relationships between spin coating, curing temperature, electronic properties, and structures of the poly(silsesquioxanes), (2) The CMP characteristics of the poly(silsesquioxanes), and (3) The integration of the poly(silsesquioxanes) with Al and Copper. We have developed a mathematical model to predict the film thickness during spin coating and curing. We also evaluated the transformation of the cage form to the network form for different poly(silsesquioxanes) during curing by FTIR technique. The electronic properties of the studied poly(silses- quioxanes) such as dielectric constant and refractive index strongly affected by the ratio of the cage/network form. Hence, it is possible to monitor the properties of poly(silsesquioxanes) by combinations of spin coating and curing. The CMP characteristics of HSQ, MSQ, and HOSP were studied by using different kinds of slurries and surfactants. The investigated slurries included SiO_2 based slurry (SS-25), ZrO_2 based slurry (A1), and Al_2O_3 based slurry (8104/H_2O). The used surfactants included non-ionic Triton X-100, anionic DSSS, and cationic TMAH. The experimental results suggest that the organic content, the hardness and charge status of the abrasive, the polarity and charge status of the surfactant significantly affect the polishing results.

D5.2

LOW-K SILICON NITRIDE FILM FOR COPPER INTERCONNECTS INTEGRATION PREPARED BY CATLYTIC CVD AT LOW TEMPERATURE. Hidekazu Sato[1,2], Akira Izumi[1] and Hideki Matsumura[1]. [1]JAIST, Ishikawa, JAPAN; [2]FUJITSU Limited, Mie, JAPAN.

As the dimensions of ultra large scale integrated circuits (ULSI) devices continue to shrink, the RC delay of interconnects will limit of the device speed performance. Recently, low resistance Cu interconnects with damascene process integration is introduced to solve this problem. However, conventional Cu damascene process requires plural layers of high-k SiN film for a groove etch-stopper and a barrier of Cu diffusion. Because of high permittivity of SiN, the merit of Cu interconnect has been degraded by the parasitic capacitance effect. Since process temperature is limited only PECVD SiN film. It is often poor barrier properties, but adopt unavoidably. To solve this problem, new low-k SiN film for barrier of impurity diffusion and oxidation ability has been developed with catalytic (Cat-) CVD method at low temperature. In the Cat-CVD method, the deposition gases such as a gaseous mixture of silane and ammonia are decomposed by catalytic cracking reactions with a heated tungsten catalyzer placed near substrates, and SiN films are formed at substrate temperatures blow 400°C without using plasma. In this paper, superior film property of Cat-CVD low-k SiN is presented. The permittivity of Cat-CVD low-k SiN film can be below 6 by adjusting deposition conditions, whereas that of conventional SiN is about 7.8. This permittivity of the film is determined by measurement of the capacitance of MIS structure. Additionally, the film tends to cover the steps or grooves conformally and post-deposited hydrogen treatments using Cat-CVD system can suppress the oxidation of the film. The results demonstrate that Cat-CVD SiN film is expected as a new low-k SiN film.

D5.3

MATERIALS PROPERTIES OF A SiOC LOW DIELECTRIC CONSTANT FILM WITH EXTENDIBILITY TO $k<2.7$. Eugene Lopata, Lydia Young, Silicon Valley Group Thermal Systems, Scotts Valley, CA; John Felts, Nano Scale Surface Systems, Alameda, CA.

One of the greatest material challenges for the microelectronics industry in recent years is the identification of advanced dielectric materials to replace silicon dioxide as an intermetal and intrametal dielectric for back-end-of-the-line applications. While many candidates have been considered as low-k materials, each presents a significant trade-off and none has emerged as a universal solution. The requirements for VLK thin films for future generations of semiconductor devices provide an excellent opportunity to use some of the known plasma polymerization process technology used in other industries to make silicon based thin-films that have organic polymer-like content: SiOC materials. Such an approach offers the promise of tailoring hybrid materials to provide the best properties of silicon dioxide (such as thermal stability, hardness, etc.) with the benefits of organic functionality (low dielectric properties). This paper describes the plasma deposition of an SiOC film and methods of adjusting key parameters to extend the baseline dielectric constant to well less than 3.0. Data at 3.0 shows excellent thermal stability ($<$ 0.5%/hour, for 8 hours at 400C), adhesion to material layers typically used in devices (Si, SiO_2, SiN, SiN over SiOC, TiN, copper, aluminum), and good deposition rates (≈1800 A/min). These k=3.0 data show extendibility to below 2.7.

D5.4

EFFECTS OF TEMPERATURE ON THE MECHANICAL RELIABILITY OF LOW DIELECTRIC-CONSTANT SPIN-ON GLASSES. Yvete A. Toivola, Jeremy A. Thurn and Robert F. Cook, University of Minnesota, Department of Chemical Engineering and Materials Science, Minneapolis, MN.

Spin-on glass films, formed by the polymerization of silsesquioxane (SSQ) oligomers, have great potential as semiconductor interconnection materials due to their low dielectric-constants (2.5-3.3), tunable properties, compatibility with silica chemistry and extendibility to even lower dielectric constant via increased porosity. The mechanical properties of SSQ materials, however, are inferior to those of silica, particularly the resistance to moisture-assisted, residual-stress driven stress-corrosion cracking, leading to interconnection yield and reliability concerns. In addition, the underlying mechanical properties controlling cracking–modulus, hardness, toughness and film stress–are extremely sensitive to the time, temperature and environment used during the polymerizing curing process. In this study, the variation in the mechanical properties of an SSQ material with curing time and temperature were examined, focusing on the transition from the low modulus, high stress, under-cured state to the high modulus, low stress, over-cured state. The development of film stress was determined by in-situ measurement of wafer curvature during curing; modulus and hardness were determined by instrumented (nano-)indentation. The mechanical behavior was correlated with changes in infra-red spectra and compared with similar tests on poly(dimethyl siloxane). An implication of the results is that there is an optimum intermediate curing temperature for maximum SSQ mechanical reliability.

D5.5

ADHESION IMPROVEMENT FOR ORGANIC LOW DIELECTRIC CONSTANT MATERIALS. Yi Xu[1], Simon Y.M. Chooi[1], Jane. C.M. Hui[2], Zhi Gang Han[3], Jian Zhang[3], Charles Lin[2], Mei Sheng Zhou[1] and Subhash Gupta[1]. [1]R&D Advanced Technology, [2]R&D Process Module, [3]Fab2 Thin Film Chartered Semiconductor Manufacturing Ltd., Singapore, SINGAPORE.

Advanced interconnect technology incorporating both low dielectric constant material and copper has been intensively studied as a replacement for the aluminum-oxide interconnects and the copper-oxide interconnects. Besides the need to satisfy the numerous material, electrical, mechanical and thermal properties, the process integration of these low dielectric constant materials into the damascene interconnects is also important. One such integration challenge pertains to the adhesion of these low dielectric constant materials to the various contacting thin films in the damascene interconnect scheme. Poor adhesion issue would cause reliability problem. In this paper, the adhesion between spin-on organic low dielectric constant materials (FLARE from AlliedSignal and SiLK from Dow Chemical) and inter-metal dielectric (e.g. silicon dioxide) or copper-diffusion barrier metal (e.g. titanium, tantalum) would be researched along the following criteria: (1) The relative position of the thin film materials to the organic low dielectric constant material (whether as a base layer or a cap layer), (2) The type of precursors used for the inter-metal dielectric, (3) The deposition temperature in the PECVD of the dielectric (performed on Applied Materials and Mattson equipment). (4) The effect of degassing in the PECVD equipment prior to the deposition of the cap dielectric. (5) The effect of plasma surface treatment in the PECVD equipment prior to the deposition of the cap dielectric. The results of the above studies would be presented and the subsequent adhesion improvement methodologies would be discussed.

D5.6
CHARACTERIZATION OF FLUOROCARBON THIN FILMS FOR LOW DIELECTRIC CONSTANT AND HIGH THERMAL STABILITY. Sang-Soo Han and Byeoung-Soo Bae, Dept. of Materials Science & Engineering, KAIST, Taejon, KOREA.

a-C:F thin films have been studied for low dielectric intermetal layer materials, but thermal stability has been mainly concerned, because low dielectric constant and high thermal stability are reciprocal dependence of composition in a-C:F thin films. Thus, in this study, the optimum condition of composition and molecular structure of a-C:F thin films for low dielectric constant and high thermal stability was investigated. a-C:F thin films were deposited using ICP-CVD with various flow rate ratio of CH_4:CF_4 gasses from 1:1 to 1:10. The dielectric constants of a-C:F films reduced to 2.3 with increasing CF_4 flow rate. The films were annealed at 400°C for 20 minutes in vacuum. ERD-TOF(Elastic Recoil Detection - Time Of Flight) was used for quantitative compositional analysis, and the change of the C-F bonding configuration was observed by FTIR and XPS analyses. The reduction of dielectric constant depends on C-F bonding configuration as well as fluorine content. The optimal conditions to satisfy the low dielectric constant and high thermal stability follows; the film has to have compatible fluorine content, and the C-F bonding configuration has to be C-F_3 & C-F_2 instead of C-F; the structure of fluorocarbon has to be linear and short-chain for low dielectric constant. Therefore, the optimal processing condition will be provided.

D5.7
PROPERTIES OF LOW DIELECTRIC CONSTANT CYCLO-HEXANE-BASED PLASMA POLYMER THIN FILMS DEPOSITED BY PLASMA ENHANCED CHEMICAL VAPOR DEPOSITION. Jaeyoung Yang, Jayoung Choi, Yong Chun Quan, Hyunuk Cho, Donggeun Jung, Sungkyunkwan Univ., Dept. of Physics, Suwon, SOUTH KOREA.

Low dielectric constant (low k, $k \leq 3$) materials are important in reducing interconnect RC delay and cross-talking noise in multilevel metallization of ultra large scale integrated (ULSI) devices. Polymers can be considered as a promising low k material due to the relatively low k values and high thermal stability. Plasma polymers which are formed by gas phase polymerization of monomers by plasma are easy to be introduced into the semiconductor manufacturing process because thin films of plasma polymers can be deposited by widely used plasma enhanced chemical vapor deposition (PECVD). In this work, we report on the investigation of the properties of cyclohexane-based plasma polymers (CHexPP) as functions of the deposition pressure and the plasma power. As the deposition pressure was decreased from 2 torr to 0.2 torr with a fixed plasma power of 60 W, k value of the CHexPP thin film increased from 2.42 to 3.24. CHexPP thin films deposited at lower deposition pressure showed higher thermal stability, and the CHexPP thin film deposited at 0.2 torr was stable up to 400°C. As the plasma lower was increased from 5 W to 90 W with a fixed plasma power of 0.2 torr, k value increased from 2.36 to 3.39. The CHexPP thin film deposited at 90 W were stable up to 450°C. All the deposited films were insulating. Under applied fields $\leq$ 1 MV/cm, leakage current densities were $\leq 10^{-7}$ A/cm^2.

D5.8
HIGH-TEMPERATURE MECHANICAL BEHAVIOR AND PHASE MORPHOLOGY OF POLY(TETRAFLUOROETHYLENE)/ SILOXANE NANOCOMPOSITES USED AS ULTRA LOW-*k* DIELECTRICS. Ping Xu, W.L. Gore & Associates, Inc., Elkton, MD; Shichun Qu, Tom Rosenmayer, W.L. Gore & Associates, Inc., Eau Claire, WI; Min Y. Lin, National Institute of Science and Technology, Gaithersburg, MD.

Poly(tetrafluoroethylene) (PTFE)/siloxane nanocomposites have been prepared as ultra low-*k* dielectrics. These new nanocomposites show excellent high-temperature mechanical properties compared to unfilled PTFE while their dielectric constant almost remains unchanged. Specifically, the data from the dynamic mechanical study indicates that these nanocomposites have the mechanical behavior similar to that of crosslinked polymers. Small angle neutron scattering (SANS) has been carried out to characterize the phase morphology of the PTFE/siloxane nanocomposites and the size of the inorganic networks. It has been shown that no phase separations or orientations appear in these nanocomposites in the range of 16 to 469 nm. These SANS results suggest that these materials are single-phase nanocomposites that are very homogeneous and isotropic. They are basically PTFE-based molecular composites. Results about PTFE/siloxane nanocomposite-based interconnects will also be presented.

D5.9
EVALUATION OF ALLIED SIGNAL'S HOSP AS AN INTER LAYER DIELECTRIC. Anupama Mallikarjunan, Dept. of Materials Science and Engr.; Toh-Ming Lu, Dept. of Physics; Shyam P. Murarka, Dept. of Materials Science and Engr., Rensselaer Polytechnic Institute, Troy, NY; Jengyi Yu, Shi-Qing Wang, Allied Signal Inc., Sunnyvale, CA; Aloknandini U. Roy, Hans Bakhru, Dept. of Physics, State University of New York at Albany, Albany, NY.

Allied Signal's low dielectric constant material HOSP (k = 2.5) is a spin-on hybrid siloxane-organic polymer designed for both copper damascene and subtractive aluminum processing. An investigation of the stability and electrical characteristics of Cu and Al metal layers on HOSP has been carried out.The leakage behavior of Metal/ HOSP/Oxide/Si structures has been evaluated. The I-V characteristic is best described by a power-law equation, and the leakage current density at 2 MV/cm is about 1e-7 A/cm^2 which is adequate for inter layer dielectric (ILD) applications. Bias temperature stressing of the above structure leads to some initial flatband voltage shift, but no successive shift occurs. In order to investigate whether metal diffusion into HOSP occurs, thermal diffusion studies (upto 400°C) with blanket metal/HOSP films were carried out and RBS was used to analyze for metal diffusion. The adhesion and barrier issues between metal-HOSP layers were explored and standard diffusion barriers/ adhesion promoters such as TiN and Ta were evaluated. These results will be discussed in view of the suitability of HOSP as an ILD.

D5.10
STRUCTURAL ANALYSES OF FLUORINE-DOPED SILICON DIOXIDE DIELECTRIC THIN FILMS BY MICRO-RAMAN SPECTROSCOPY. Jeffery L. Coffer and T. Waldek Zerda, Texas Christian University, Ft. Worth, TX; Kelly J. Taylor and Scott Martin, Texas Instruments, Kilby Center, Dallas, TX.

Fluorine-doped silicon dioxide, a dielectric material compatible with copper integration, has received considerable attention for applications requiring a k value in the 3.5 to 4.0 range. Given the influence of structure on desired properties, convenient experimental structural probes of this type of material are of widespread interest. This presentation focuses on Raman spectroscopic analyses of ring defects in fluorine-doped silicon dioxide films prepared by plasma enhanced chemical vapor deposition (PE CVD) as well as high density plasma methods (HDP). These measurements are complemented by ab initio computational simulations of the ring defects in these films and the impact of nearby fluorine on their stability. The impact of aging on these structures and correlations of observed trends with other experimental techniques (such as outgassing and X-ray fluorescence) will also be discussed.

D5.11
STUDY OF DRY PHOTORESIST STRIPPING PROCESSES FOR HYDROGEN SILSESQUIOXANE. Huey-Chiang Liou, Jerry Dual, Vic Finch, Semiconductor Fabrication Materials, Dow Corning Corporation, Midland, MI; Qingyuan Han, Ricky Ruffin, Fusion Systems Division, Semiconductor Equipment Operation, Eaton Corporation, Rockville, MD.

As the minimum geometry of ultra large scale integrated (ULSI) devices moves below 0.2 μm, implementation of low k dielectric materials in device fabrication is needed to reduce the intraline capacitance between metal lines and to increase the signal propagation speed. Among low k materials, hydrogen silsesquioxane (HSQ) has succeeded in the semiconductor device production due to its low dielectric constant (< 3.0), excellent gap fill and planarization capability. HSQ has been used in production for 0.35-0.5 μm device technology. However, the challenge to apply HSQ in < 0.20 μm device technology is the photoresist (PR) stripping step. HSQ films are sensitive to the amine based PR stripper used in wet PR stripping process and oxygen used in the traditional O_2 downstream plasma stripping processes. HSQ film damage leads to via bowing and higher via resistance. Therefore, there is a need for developing a new PR stripping process for HSQ in the applications of deep submicron devices. Recently, the dry PR stripping processes for HSQ have been studied to develop a new effective process to reduce the damage to HSQ. In this study, the impacts of the stripping chemistry and process conditions on the removal selectivity and HSQ film properties have been identified. Better results were observed at lower pressure, higher process temperature, and O_2 free gas chemistry conditions. The processes and film measurement results will be discussed.

D5.12
CURING STUDY OF HYDROGEN SILSESQUIOXANE IN H_2/N_2 AMBIENT. Huey-Chiang Liou, Evan Dehate, Jerry Duel and Fred Dall, Dow Corning Corporation, Semiconductor Fabrication Materials, Midland, MI.

As the minimum geometry in integrated circuits (ICs) continues to shrink to the 0.18-0.25 μm range, the capacitance between metal lines increases dramatically which causes the delay in signal propagation. Low-k dielectric materials can be implemented to reduce the capacitance. Among low k materials, hydrogen silsesquioxane (HSQ)

has succeeded in the semiconductor device production due to its low dielectric constant (< 3.0), excellent gap fill and planarization capability. HSQ has the theoretical chemical structure of $(HSiO_{3/2})n$ before film formation. When thermally processed into films, the Si-H bonds in HSQ disassociate and its structure is rearranged into a random network structure. The degree of Si-H bond loss, which is determined by the process ambient, time, and temperature, will strongly impact the HSQ film properties. It has also been shown that HSQ will lose more SiH bonds when processed in an O_2 ambient and/or higher process temperatures above 400°C. Therefore, it is the objective of this work to investigate if the loss of SiH bond can be suppressed by processing in a H_2 ambient and to understand the impact on the film properties. In this study, HSQ films were cured in N_2 and H_2/N_2 ambient and different temperatures and the resulting film properties, such as dielectric constant and modulus, have been measured. It shows that processing HSQ in a higher percentage of H_2 ambient can suppress the loss of SiH bonds and maintain its film properties at higher process temperature (>400°C). The detail results will be discussed.

D5.13
MICROMECHANICAL CHARACTERISTICS OF POLY(METHYL-SILSESQUIOXANE) THIN FILMS. K. Char, S.-H. Chu and D. Kim, School of Chemical Engineering, Seoul National University, KOREA; J.-K. Lee, H.W. Ro, D Y. Yoo and D.Y. Yoon, Department of Chemistry, Seoul National University, KOREA.

Poly(methyl-silsesquioxane) (PMSSQ) is very attractive for BEOL low-dielectric thin films in advanced ULSI microelectronic devices. In this regard, the micromechanical properties of PMSSQ thin films are quite important since the films should withstand severe mechanical stress conditions generated by chemical mechanical planarization (CMP) processes and thermal expansion mismatch of the multilevel BEOL films with the underlying silicon layer. Using nanoindentor and microvickers tests, we have measured the hardness, modulus and crack-propagation velocity of PMSSQ films prepared from samples with different initial molecular weights and varying chemical structures. Moreover, the details of crack morphology and the effect of PMSSQ chemical structure on surface topography were also examined with atomic force microscopy. The micromechanical characteristics of PMSSQ films are known to depend on the cure conditions as shown by previous works. However, the effects of cure conditions and, more importantly, the final micromechanical properties of cured samples are found to be strongly correlated with the molecular weight and its distribution of initial PMSSQ samples as well as with the details of the PMSSQ chemical structure.

D5.14
CHARACTERIZATION AND INTEGRATION IN Cu DAMASCENE STRUCTURES OF AURORA, AN IN-ORGANIC LOW-K DIELECTRIC. R.A. Donaton, B. Coenegrachts, M.R. Baklanov, G. Beyer, H. Struyf, S. Vanhaelemeersch, M. Schaekers, E. Sleeckx, M. Stucchi, D. De Roest, K. Maex, IMEC, Leuven, BELGIUM; G. Sophie, N. Matsuki, ASM Japan, Tokyo, JAPAN.

The replacement of silicon dioxide by materials with lower dielectric constant in metallization schemes becomes mandatory as the technologies migrate towards the 100 nm node. The use of low-k materials helps to reduce the capacitance between adjacent lines, resulting in the decrease of RC-delay and parasitic capacitances, thus improving device performance. They are also useful for reducing cross-talk.
AURORA is an in-organic low-k material deposited in a ASM EAGLE-10 PECVD reactor. It is a Si-O-C based film with low C concentration (20-25%). A dielectric constant of 2.7 was measured from metal/dielectric/metal capacitors and the film showed leakage values in the order of 10^{-10} A/cm^2 at 0.1 MV/cm. In this paper we discuss the basic film characteristics, such as film stability, degassing properties and adsorption/desorption of chemicals. The AURORA films are integrated in 0.18 μm technology Cu single damascene structures and electrical results - line continuity, meander / fork shorts, interline capacitance and leakage - are presented and compared with the ones of single damascene oxide.

D5.15
Transferred to D4.9

D5.16
MICROSTRUCTURE AND ELECTRONIC PROPERTIES OF THIN FILM SILICA AEROGELS AS A FUNCTION OF PROCESSING METHOD. Christine Caragianis-Broadbridge, John R. Miecznikowski, Dept. of Engineering, Trinity College, Hartford, CT; Jin-ping Han, Wenjuan Zhu, Zhijiong Lu, Dept. of Electrical Engineering, Yale University, New Haven, CT.

Aerogels are nanoporous materials with unique optical, thermal and electrical properties. Silica thin film aerogels demonstrate great potential as low dielectric constant insulators for interlevel dielectric applications. The focus of this research was the fabrication of thin film silica aerogels while utilizing a technique that does not require supercritical drying, freeze drying or a surface modification step before drying. Alcogels, aerogel precursors, were prepared by hydrolysis and condensation of metal alkoxide, tetraethyothrosilicate, and were catalyzed by both acids and bases, according to a standard reaction. The resulting sol-gel solution was applied to bare silicon and silicon dioxide coated silicon wafers, which were divided into three groups. The first group was treated with an adhesion promoter [3-aminopropyl triethoxysilane (1.00 mL), ethanol (10.00 mL) and ethylene glycol (15.00 mL)] that was spin coated onto the wafer surface before sol-gel application. For the second group, the sol-gel solution was applied without adhesion promoter. For the third group, adhesion promoter was applied before sol-gel deposition followed by a post-gel surface modification step. The surface modification was carried out in a solution of n-hexane and trimethylchlorosilane. The microstructure and electronic properties of the silica aerogels were evaluated using non-contact atomic force microscopy (nc-AFM), scanning and transmission electron microscopy (SEM and TEM) combined with electronic measurements [HP4156A precision semiconductor parameter analyzer (Current-Voltage) and 4284A precision LCR meter (Capacitance-Voltage)]. Metal-insulator-semiconductor devices were fabricated from samples representative of each of the processing methods employed. The resulting data reveal that the substrate, substrate preparation method and post-gel surface modification step impact film microstructure (uniformity, adhesion, mean pore size and pore size distribution) as well as the electronic properties (leakage current, breakdown voltage and dielectric constant). Subsequent annealing studies revealed a dramatic temperature dependent effect on both the microstructure and electronic properties of the aerogels.

D5.17
PHOTO-DEPOSITION OF LOW DIELECTRIC CONSTANT POROUS SILICA FILM AT ROOM TEMPERATURE. Jun-Ying Zhang and Ian W. Boyd, Electronic & Electrical Engineering, University College London, Torrington Place, London, UNITED KINGDOM.

As device densities increase and chip dimensions shrink, propagation delay, crosstalk noise, and power dissipation become significant due to resistance-capacitance (RC) coupling. Integration of low-dielectric-constant (k) materials, as means of reducing RC time delays for Si integrated circuits, has been identified for 0.1 μm technology and beyond. Current low-k commercialisation emphasises spin-on glasses (SOGs) and fluorinated silicon dioxide SiO_2 with k>3, and a number of polymers are under development with k in the range of 2-3. These suffer from potential problems including thermal stability, mechanical and electrical properties, low thermal conductivity, and reliability. However, low-k dielectric nanoporous silica with tuned k values from 1-4 have the advantage of facilitating manufacture of higher performance integrated-circuit (IC) devices because of compatibility with standard microelectronic processing and the ability to tune k over a wide range. In this paper we report the formation of porous silicon dioxide films on Si (100) substrates at low temperatures (25-200°C) by photo-assisted sol-gel processing using 172 nm radiation from an excimer lamp. The effects of substrate temperature and lamp exposure time on the properties of the films formed have been studied using ellipsometry, Fourier transform infrared spectroscopy (FTIR), and electrical measurements. The FTIR spectra revealed the presence of a Si-O-Si stretching vibration peak at 1070 cm^{-1} after UV irradiation at 200°C. This is similar to that recorded for oxides grown thermally at temperatures between 600-1000°C. Capacitance measurements indicated that the dielectric constant values of the films found to be between 1.7-3.6 strongly depended on the substrate temperature during irradiation. Dielectric constant values as low as 1.7 are readily achievable at room temperature. The results show that the photochemical induced effects initiated by the UV radiation enable both reduced processing times and reduced processing temperatures to be used.

D5.18
ULTRA LOW-K INORGANIC SILSESQUIOXANE FILMS WITH TUNABLE ELECTRICAL AND MECHANICAL PROPERTIES. Thomas A. Deis, Chandan Saha, Eric Moyer, Kyuha Chung, Youfan Liu, Mike Spaulding, John Albaugh, Wei Chen and Jeff Bremmer, Dow Corning Corporation, Midland, MI.

Low-k dielectric films have been developed using a new silsesquioxane based chemistry that allows both the electrical and mechanical properties to be tuned to specific values. By controlling the composition and film processing conditions of spin-on formulations, dielectric constants in the range 1.5 to 3.0 are obtained with modulus values that range from 2 to 20 GPa. The modulus and dielectric constant are tuned by controlling porosity which varies from 0 to 60%, and final film composition which varies from $HSiO_{3/2}$ to $SiO_{4/2}$. The spin-on formulation includes hydrogen silsesquioxane resin and

solvents. Adjusting the ratio of solvents to resin in the spin-on formulation controls porosity. As-spun films are treated with ammonia and moisture to oxidize the resin and form a mechanically self-supporting gel. Solvent removal and further conversion to a more "silica-like" composition occur during thermal curing at temperatures of 400 to 450°C. The final film composition is controlled through both room temperature oxidation and thermal processing. Final film properties are optimized for a balance of electrical, mechanical and thermal properties to meet the specific requirements of a wide range of applications. Processed films exhibit no stress corrosion cracking or delamination when indented 100%. Films also exhibit high adhesive strength (> 60MPa) and low moisture absorption. Processing conditions, compositions and properties of thin films with thicknesses between 3,000 to 10,000Å will be discussed.

D5.19
LOW DIELECTRIC PROPERTIES OF SPIN-COATED MESOPOSOUS SILICA FILMS. Akira Endo, Shin'ichiro Matsumoto, Masaru Nakaiwa, Takashi Nakane, National Institute of Materials and Chemical Research, Tsukuba, JAPAN; Takeo Yamada, Hao-Shen Zhou, Itaru Honma, Electrotechnical Laboratory, Tsukuba, JAPAN.

Mesoporous silica film is expected to be a candidate for low K material in microelectronics applications. In this study, highly ordred mesoporous silica films, which have different mesostructure with hexagonal, cubic and lamellae, were prepared by rapid sol-gel spin-coating technique using self-assembled surfactant templates and their dielectric properties were measured. The thin films were prepared as follows: The solution for spin-coating was prepared by mixing TEOS, 1-Prpanol, 2-Buthanol, HCl, surfactant(cetyltri-methylammonium chloride, $C_{16}TMACl$). The silicate/surfactant thin film was synthesized by spin coating (2000rpm) on Si substrate at room temperature. After drying at 100°C, the film was calcined at 400°C for removing the surfactant. The structure of the films (mesophase, pore size, porosity and thickness etc.) were characterized by low angle XRD, SEM and gas adsorption technieque. Dielectric properties were measured for the films which have different pore size and porosity using ac impedance technique. Measured K value were compared with the value estimated from the porosity of the films.

D5.20
STRUCTURE AND PERFORMANCE OF ULTRA LOW-K SILSESQUIOXANE BASED DIELECTRIC DURING SUBSEQUENT THERMAL PROCESSING CYCLES. Youfan Liu, Eric Moyer, Kyuha Chung, Thomas Deis, Mike Spaulding, Dow Corning Corporation, Midland, MI.

Porous silica-like ultra low-k dielectric films have been developed by introducing small pores into hydrogen-silsesquioxane (HSQ) based resin for future generation integrated circuit technology. With tunable dielectric and mechanical properties, depending on film porosity and stochiometry, this low-k dielectric offers a great potential to be used for broader interlevel dielectric applications. The films with a porosity of 50 - 60 % and Si-H bond density remaining of 35 - 45% after cure have a dielectric constant and modulus of about 2.0, and 3.0 GPa, respectively. The properties are designed to allow integration of the ultra low-k dielectric into copper damascene applications. In this study, the thermal stability during subsequent thermal processing cycles has been evaluated. The spectroscopic ellipsometry, and infrared spectroscopy techniques were used to evaluate structure impacts on dielectric and mechanical properties. The complex dielectric constant at 1MHz and modulus were determined by performing complex impedance measurements and using nano-indentation technique, respectively. It was demonstrated that the dielectric properties of the ultra low-k dielectric are extremely stable under multiple thermal cycles at 450°C for 60 minutes in N_2. All electronic and atomic contributions to the dielectric constant remained the same although Si-H bond density decreased by 10%. There was no change in film porosity, but the mechanical property was further improved due to the increasingly formed Si-O-Si networks as film modulus increased from 3 to 5 GPa after these thermal cycles. The structure-property-process relationship will be discussed.

D5.21
CHARACTERIZATION OF PORES AND COMPOSITION OF LOW K POROUS THIN FILMS. Wei Chen, Thomas A. Deis, Chandan K. Saha, Eric S. Moyer, Kyuha Chung Dow Corning Corporation, Midland, MI; Eric K. Lin, Gary W. Lynn, Wen-li Wu, Polymer Division, National Institute of Standards and Technology, Gaithersburg, MD.

Until recently porous silica thin films were the primary candidates of inorganic low k materials for interlayer dielectric applications. A new class of meso-porous silica-like thin films (based on Dow Corning hydrogen silsesquioxane (HSQ) resin platform), with a wide range of electrical and mechanical properties, has been developed. This new class of low k films is produced by the ammonia treatment followed by a thermal cure near 400°C of a pre-spun film. The pre-spun films are generated from mixtures of solvents and HSQ resin. The dielectric constants (k) of the films may be tuned between 1.5 and 3.0 with an encouraging set of mechanical properties by adjusting the ratio of the solvents and the resin, subsequent cure conditions, and reaction time. The low k and high mechanical properties have created needs for in-depth characterization of the films to establish a correlation between film characteristics and properties. The film characteristics such as composition, pore dimension, and pore structure are of great interests. Rutherford backscattering, forward recoil elastic spectro-scopy, infrared spectroscopy were employed to determine the film composition and chemical structure. A new method consisting of X-ray reflectivity (XR) and small angle neutron scattering (SANS) was reported to characterize nano-pores in low k dielectric thin films [1] and subsequently, to determine density, average pore dimension, and porosity of the thin films. This method was applied to characterize the new class of meso-porous films of approximately 1 μm in thickness manufactured by Dow Corning Corporation under various processing conditions. The composition analyses of these films reveal hydrogen content between 20-27 atomic percent (at.%), silicon between 20 and 26 at. %, and oxygen between 40 and 46 at. %. The overall film density varies from 0.745 to 0.95 g/cm^3 depending on how the films are processed. The characteristic dimensions of the pores in the films varies between 2.4 and 2.8 nm., with the porosity between 57 % and 62%. Also, as a comparison, positron annihilation lifetime spectro-scopy (PALS) was used to further investigate the pore characteristics in these films. The results from XR/SANS and PALS are in good agreement. The excellent electrical and mechanical properties are attributed to the film composition and well dispersed fine pores.
1. W.L. Wu, W.E. Wallace, E.K. Lin, G.W. Lynn, C.J. Glinka, E.T. Ryan and H.M. Ho, submitted to J. of Appl. Phys.

D5.22
CHARACTERIZATION OF LOW-K DIELECTRIC POROUS THIN FILMS DETERMINED BY HIGH RESOLUTION X-RAY REFLECTIVITY AND SMALL ANGLE NEUTRON SCATTERING. Eric K. Lin, Wen-li Wu, William E. Wallace, Gary W. Lynn[1], National Institute of Standards and Technology, Gaithersburg, MD. [1]Univ. of Tennessee, Knoxville, TN; E. Todd Ryan and Huei-Min Ho, SEMATECH, Austin, TX.

Nanoporous thin films have been identified by the microelectronics industry as an important class of materials for use as low-k interlevel dielectrics needed for next generation electronic devices. Unlike traditional homogeneous materials, the structure of the porous network critically affects properties needed for their integration into current fabrication lines. We have developed a methodology combining small angle neutron scattering (SANS), high resolution x-ray reflectivity (HRXR), and ion scattering to determine important structural information about porous films on silicon wafers. This methodology is used to provide quantitative measurements of the average pore size, pore connectivity, film thickness, matrix material density, coefficient of thermal expansion, moisture uptake, and film composition. These properties are provided to aid industry in the selection of candidate materials and processes to be used in next generation integrated circuits.

D5.23
GRAZING INCIDENCE SMALL ANGLE X-RAY SCATTERING (GISAXS) STUDY ON LOW DIELECTRIC THIN FILMS. C.-H. Hsu, Hsin-Yi Lee, Tang-Eh Dann, Keng S. Liang, Synchrotron Radiation Research Center, Hsinchu, TAIWAN; D. Windover, T.-M. Lu, Center for Integrated Electronics, Electronics Manufacturing and Electronic Media, Rensselaer Polytechnic Institute, Troy, NY; C. Jin, Texas Instruments, Dallas, TX.

Highly porous silica films with pore size in the nanometer scale are being extensively studied as potential candidates for interlevel dielectrics. Because the dielectric materials appears in the form of thin films with a thickness of only several hundred Angstroms, conventional techniques can not be readily applied to study their structure and porosity. We employed small angle scattering in the grazing incidence geometry in this study. Using high resolution x-ray beamline with synchrotron radiation source, the average pore size and its distribution can be readily obtained. The porous properties of sol-gel derived silica - xerogel films on silicon substrate studied by GISAXS will be presented.

D5.24
CHARACTERIZATION OF POROUS SILICA DEVELOPED BY UNION CHEMICAL LABORATORIES. C.J. Wang, Y.T. Chen, T.Y. Lou, L.M. Chen, Union Chemical Laboratories, Industrial Technology Research Institute, Hsinchu, TAIWAN ROC.

Porous silica can be used in ILD applications owing to its lower dielectric constant and tunable property. In the light of its feasibility in application to different technology node, Union Chemical

Laboratories (UCL) has developed several precursors of porous silica using different formulations. The new formulations assure simplification in thin film fabrication process. Optical properties of porous silica films deposited on Si are characterized by variable angle spectroscopic ellipsometer (VASE). The feasible curing conditions were obtained by inspecting the responses such as film thickness, porosity, and refractive index. A two-phase solid structure model could explain the spring-back property which makes the skeleton more resilient to stress. This is confirmed by the linear relationship between thermal stress and temperature, which is measured by bending beam method. The structure evolution upon thermal treatment is examined by FTIR analysis. After curing at 400°C, the desired functional group for modification still exists. The dielectric constant read from CV curve in MIS measurement is well below 2.0. The films coated on Si, PETEOS SiO_2, Si_3N_4, TiN and Ta all pass the tape test.

D5.25
PROCESSING, CHARACTERIZATION, AND RELIABILITY OF SILICA XEROGEL FILMS AS LOW DIELECTRIC CONSTANT MATERIALS. Anurag Jain, Svetlana Rogojevic, Feng Wang, William N. Gill, Peter C. Wayner, Jr., Joel L. Plawsky, Dept. of Chemical Engineering, Rensselaer Polytechnic Institute.

Xerogel films of wide range of porosity (25-90 %) and uniform thickness (0.4 - 2 microns) were fabricated on various substrates. Precise control of the evaporation of ethanol from the film during spin coating allows for porosity control over such a wide range. A relation was developed between the final film porosity and the ethanol vapor concentration in the spin coating ambient. Mechanical reliability as a function of aging time and temperature was determined by measuring the fracture toughness using the edge-lift-off technique. Films should be aged at the highest possible temperature to get the maximum fracture toughness and there appears to be an optimum aging time at 60 C to obtain maximum fracture toughness. Thin ($\sim$ 500 Å) films of Copper, Tantalum and Tungsten were deposited on xerogel films and subjected to thermal annealing. No diffusion was observed within the limits of RBS if the annealing was done in a completely inert, oxygen free, environment. SIMS analysis of Cu films annealed on xerogel and thermal oxide films showed significant Cu diffusion into the thermal oxide yet no diffusion into surface-modified xerogels. Biased thermal stress testing of Si/SiO2/Xerogel/Cu structures was performed to amplify and quantify any trace amounts of copper that may diffuse through surface-modified xerogels.

D5.26
SOL-GEL DERIVED SILICA LAYERS FOR LOW-k DIELECTRICS APPLICATIONS. Sylvie Acosta, André Ayral, Christian Guizard, Laboratoire des Matèriaux et Procèdès Membranaires, E.N.S.C. Montpellier, FRANCE; Charles Lecornec, Gèrard Passemard, Mehdi Moussavi, LETI/DMEL/TCI, Grenoble, FRANCE.

Porous silica exhibits attractive dielectric properties which make it a potential candidate for use as insulator into interconnect structures. A new way of preparation of highly porous silica layers by the sol-gel route was investigated and will be presented. The synthesis strategy was based on the use of low cost and low toxicity reagents and on the development of a simple process without gaseous ammonia post-treatment or supercritical drying step. Defect free layers were deposited by spin coating on 200 mm silicon wafers. They were characterized using Fourier transform infrared spectroscopy, scanning electron microscopy, residual stress analysis, nitrogen adsorption, ellipsometry and dielectric constant measurements. Layers exhibiting a total porosity larger than 70% with an average pore size of 5nm were produced. The dielectric constant measured under nitrogen flow on these highly porous layers is equal to $\sim$ 2.5, which can be compared to the value theoretically expected from the measured porosity, $\sim$ 1.75. This difference is explained by the presence of water adsorbed on the hydrophilic surface of the unmodified silica. The effect of the synthesis and deposition parameters (sol composition, hydrolysis conditions, aging time and aging atmosphere) on the porosity and related properties of the final layers will be discussed.

D5.27
STRUCTURE AND PROPERTIES OF LOW-DIELECTRIC POLY(SILSESQUIOXANE) FILMS. EFFECTS OF MONOMER STRUCTURE, INITIAL MOLECULAR WEIGHT AND CURE TEMPERATURE. D.Y. Yoon, Seoul National Univ, Dept of Chemistry, Seoul, KOREA; C.V. Nguyen, ELORET, Inc, Sunnyvale, CA; R.L. Jaffe, NASA Ames Research Ctr, Moffett Field, CA; K. Chung, E. Moyer, C. Yeakle, Dow Corning Corp, Midland, MI.

We have investigated the local structures of poly(hydridosilsesquioxane) (PHSSQ) and poly(methyl-silsesquioxane) (PMSSQ) films of various initial molecular weights as function of cure temperature. Changes in the measured IR spectra were analyzed using quantum chemistry calculations of predicted vibrational frequencies and IR intensities for model molecules representing various cage- and ladder-type structures. PHSSQ starts from more symmetric cage like structures and transforms to highly non-symmetric structures due to the loss of Si-H groups as the annealing temperature increases above 300 C. In comparison, the initial structures of PMSSQ films vary significantly with molecular weight, but when heated to 430 C, all films show more non-symmetric ladder-like structures with no dependence on the initial molecular weight. Dynamic mechanical measurements carried out during the initial heating process show that the films become vitrified due to intermolecular cross-linking chemical reactions in the solid state. The nature of intermolecular cross-linking varies significantly with the initial molecular weight. Moreover, these changes in local structures are found to be manifested in the dielectric and mechanical properties of PHSSQ and PMSSQ films as function of their curing temperatures.

D5.28
MECHANICAL STRESS ANALYSIS FOR DUAL INLAID COPPER INTERCONNECT STRUCTURES IN SEMICONDUCTOR DEVICES. Yusheng Feng, Computational Technologies Lab, Motorola Inc., Austin, TX; Paul Besser, AMD-Motorola Alliance, Austin, TX; Matt Herrick, APRDL, Motorola Inc., Austin, TX; Jeff Wetzel, SEMATECH, Austin, TX.

Since interconnect structures will limit the device performance for sub-0.25 micron devices, the semiconductor industry has investigated interconnect structures other than aluminum and silicon oxide. One of the alternate technologies is Cu interconnects with low k dielectrics. However, Cu interconnect structures, dual inlaid or damascene structure in particular, post various challenges in terms of manufacturability and reliability. One major challenge has been mechanical integrity, including stress-induced failures and material compatibility. In this presentation, we will characterize mechanical stress in Cu damascene structures with X-Ray Diffraction. A finite element model will address temperature and linewidth effects on the mechanical stress, in order to understand the evolution of stress during the deposition and annealing process. The microstructure (texture and grain size) will also be related to mechanical and thermal stress. The results show that the principal stress components in the Cu line are linearly dependent on the post-plating annealing temperature. We also find that the inter-layer dielectric strongly affects mechanical stress, along with other factors such as process conditions and interconnect geometry.

SESSION D6: BARRIER AND SEED LAYER–DEPOSITION TECHNIQUES
Wednesday Morning, April 26, 2000
Golden Gate B2 (Marriott)

8:30 AM *D6.1
WHAT ARE THE LIMITS OF IONIZED PHYSICAL VAPOR DEPOSITION? Jeffrey A. Hopwood, Electrical and Computer Engineering Department, Northeastern University, Boston, MA .

Integrated circuit interconnects formed using the damascene process consist of high aspect ratio trenches and vias that are etched in an interlayer dielectric and subsequently filled with diffusion barrier materials and metal conductors. Unfortunately, magnetron sputtering – the former industry workhorse for film deposition – is not capable of directly depositing material into high aspect ratio features encountered in modern ICs. One of the most widely employed techniques of extending the usefulness of magnetron sputtering is ionized physical vapor deposition (IPVD). In IPVD, sputtered atoms are ionized by a high density plasma prior to being deposited at the substrate. The electric field present in the plasma sheath adjacent to the substrate accelerates ionized sputtered species perpendicular to the wafer. The flux of collimated ions produced by IPVD is capable depositing high-quality films into deep, narrow structures.
This presentation will discuss the use of IPVD in the deposition of copper seed layers, as well as titanium and titanium nitride diffusion barrier layers. The physical mechanisms occurring in the plasma will be described both through experiments and models. Key issues are limited deposition rate, the degree of ionization, and imperfect ion collimation. These physical descriptions of IPVD will be evaluated in terms of improvements to IPVD tools and the fundamental limits of the IPVD technique as applied to interconnect fabrication.

9:00 AM *D6.2
ADVANCES IN DEPOSITION TECHNOLOGY FOR Al AND Cu INTERCONNECTS. John Forster, Applied Materials, Santa Clara, CA.

Much of the "glamour associated with microelectronics has long been the creation of ever faster and smaller transistors, with interconnect technology being a boring, but unavoidable companion. The trend in integrated circuit manufacturing towards more and more metal layers

has transformed interconnect technology from a poor relation of front end processing to a glamorous equal, complete with all the dedicated symposia, conferences, etc.
Advances in interconnect technology have occurred due to advances in deposition and etch technology, and due to introduction of new materials. This talk will describe advances in the metallization portion of interconnect technology.
Contrary to the popular belief, interconnect technology based on conventional W plugs is alive and well. The challenges facing conventional W plug technology include developing processes and hardware to fill ever shrinking feature sizes, as well as lowering of process temperatures for integration with lower k dielectrics. An example of a successful new technology has been the integration of ionized Ti PVD with CDV TiN to form the liner/barrier prior to W plug fill.
Conventional Al technology is used for slab applications and plug fill. The use of ionized Ti PVD underlayers prior to Al slab deposition can improve the Al film properties. New Al PVD sources help in depositing the cold Al seed layer used for Al plug fill.
A major advance in interconnect technology is the introduction of copper. This has involved the introduction of several new technologies; ionized Ta or TaN PVD is used as a diffusion barrier. Ionized Cu PVD is used as a seed layer for subsequent fill by Cu electroplating. The introduction of new materials always involves lengthy studies to evaluate reliability and integration issues.

9:30 AM D6.3
SEED LAYER DEPOSITION FOR SUB 0.25 MICRON Cu METALLIZATION USING A LINE CUSP MAGNETRON PLASMA SOURCE. Sunil Wickramanayaka, Hanako Nagahama, Yukito Nakagawa, Masao Sasaki, Shinya Hasegawa and Yoichiro Numasawa, Anelva Corporation, Tokyo, JAPAN.

In Cu interconnect technology, the deposition of Cu seed layer for electroplating is a critical process, particularly in sub 0.25 micron via holes with aspect ratio > 5. Further, deposition of uniform Cu seed layer over the entire surface of Si wafer and uniform side coverage in via holes regardless of their position on the wafer are also important to eliminate faulty interconnects. Taking all these facts into consideration, a magnetically enhanced capacitively coupled plasma source with a planer Cu target (electrode) was developed for 200 mm wafer processing. In this sputter source, magnets were arranged on the upper surface of the Cu target in radial lines with alternate polarity to generate line cusp magnetic fields below the Cu target. With this magnet arrangement, a magnetic field free environment can be obtained for wafer processing at around 50 mm distance from the Cu target. In addition, magnets are arranged to yield a uniform plasma at the wafer level in order to yield a uniform deposition and to eliminate possible charge-induced damages. The Cu target is given 60 MHz rf power and the process is carried out at pressures in the range of 6 Pa to 8 Pa. Use of magnetic field and high frequency rf power results in an increase plasma density and thereby an excellent side and bottom coverage. The deposition rate obtained is > 200 nm/min while the film nonuniformity over 200 mm wafer lies < ±10%. The sheet resistivity of the Cu film is < 2 micro ohm cm. The bottom and side coverage of 0.25 mm via hole with aspect ratio 6 are observed as ~30% and ~10%, respectively.

10:15 AM *D6.4
ATOMIC LAYER CVD FOR CONTINUOUSLY SHRINKING DEVICES. Suvi Haukka, Kai Elers, Marko Tuominen, ASM Microchemistry Ltd, Espoo, FINLAND.

The continuous shrinking of semiconductor devices makes great demands on thin film deposition methods. The deposition method should enable the growth of uniform ultra-thin films on large surface areas with atomic layer accuracy. Furthermore this atomic layer accuracy should also be realized in extremely high aspect ratio vias and on irregular shaped surfaces to attain the best device performance. One possible technique to meet this challenge is Atomic-Layer-Chemical-Vapor-Deposition (ALCVD). The ALCVD technique was developed in Finland in the early 1970's by Dr. Tuomo Suntola. Dr. Suntola's very simple and revolutionary idea was to introduce the precursors sequentially to the surface and allow the reactive sites at the surface to control the film growth. This was contrary to conventional CVD where the precursors are introduced at the same time to the surface and the growth is controlled by the precursor flux intensity or the time of the growth. It has been shown in practice that the surface control in ALCVD (atomic layer-by-layer growth) can be realized when the following conditions are fulfilled: 1) In the growth temperature window, a covalent bond between the reactive site on the surface and the precursor is formed (chemisorption). No condensation or decomposition of the precursor is allowed to take place. 2) An excess of precursor molecules is introduced to the surface to complete the reaction with all available reactive sites, i.e. to ensure surface saturation. 3) After each reaction the surplus precursor molecules and the reaction by-products are removed by sufficient inert gas purge. It will be shown in the presentation that the systematic utilization of these three principles in the thin film growth provides the means for processing of pinhole free, conformal ultra-thin films on large area substrates.

10:45 AM D6.5
STRUCTURAL AND CHEMICAL CHARACTERIZATION OF TiN THIN FILMS DEPOSITED BY ALCVD AS BARRIERS FOR Cu METALLIZATION. Alessandra Satta, Gerald Beyer, Karen Maex, IMEC, Leuven, BELGIUM; Kai Elers, Suvi Haukka, ASM Microchemistry Ltd., Espoo, FINLAND; André Vantomme, K.U. Leuven, IKS, Leuven, BELGIUM.

The application of copper as interconnect metal in advanced multi-level metallization schemes needs the prevention of Cu diffusion into the active area and into interlevel dielectrics by total encapsulation of Cu with barrier films. Critical requirements for diffusion barriers are very thin thickness, low resistivity, low deposition temperature, conformality on high aspect ratio trenches and vias.
For this purpose, TiN films deposited by Atomic Layer Chemical Vapour Deposition (ALCVD) were proposed and compared to TiN films deposited by Ionized Metal Plasma technology (IMP). The structural and chemical characterization of ALCVD and IMP TiN films was carried out by means of resistivity measurements, ellipsometry, Rutherford backscattering spectroscopy, X-ray diffraction, TEM, AFM.
ALCVD TiN films, deposited at 400°C exhibit a resistivity range of 150-250$\mu\Omega$·cm as well as IMP TiN films in the same range of thickness (10-30nm), but ALCVD TiN deposited at 350°C show resistivity values of 400-500$\mu\Omega$·cm. The density of ALCVD films deposited at 400°C is very close to the bulk value, higher than IMP films and ALCVD TiN films deposited at 350°C. Cl residue of ALCVD TiN deposited at 400°C is 1.5%, but at the process temperature of 350°C it is twice as much as at 400°C (3%). Both ALCVD and IMP TiN films show columnar structure and texture of $< 100 >$ strong orientation, but different surface morphology and grain size distribution. ALCVD films are characterized by a fine-grained microstructure and by a surface roughness lower than IMP TiN films that exhibit a larger distribution of distinctively developed grains. A very high level of conformality on trenches and remarkable thickness uniformity characterize ALCVD TiN films deposited at the two different temperatures. These properties give a clear advantage over the sputtered IMP TiN whose coverage in high aspect ratio vias is known to be limited for the future IC technology.

11:00 AM D6.6
A NOVEL SCHEME OF CVD-DIFFUSION BARRIER FOR Cu METALLIZATION. Kyoung-Ho Kim, Young-Ho Lee, Soo-Hyun Kim, Se-Joon Im, and Ki-Bum Kim, School of Materials Science and Engineering, Seoul National University, Seoul, KOREA.

We have investigated the effect of a thin Al interlayer deposited in between chemical vapor deposited (CVD) diffusion barrier (TiN and TaN) and Cu on diffusion barrier performance in Cu metallization. Both CVD-TiN and CVD-TaN films were thermally deposited using tetrakis-dimethyl-amido-titanium (TDMAT) and pentakis-diethyl-amido-tantalum (PDEAT) as a precursor, respectively, on (100) Si substrate. Then, Al and Cu were sputter deposited onto barrier film without breaking vacuum in a DC magnetron sputtering system. The thickness of Al layer was varied from 0 nm (Cu/barrier/Si), 5 nm, 10 nm, and 20 nm. The thickness of Cu was 300 nm in all the samples. The sputtering conditions were as follow: the base pressure of deposition chamber was lower than $5.0\text{x}10^{-6}$ Torr, the deposition pressure was 4 mTorr using Ar as a plasma gas, and sputtering power was 30 W for Al (deposition rate: 20 nm/min) and 100 W for Cu (deposition rate:100 nm/min), respectively. To test the diffusion barrier properties, all the structures were annealed under the vacuum below $5.0\text{x}10^{-6}$ Torr, and at the temperature ranging from 500°C to 700°C for 1 hour. Diffusion barrier properties were characterized by sheet resistance measurement with a four-point probe, X-ray diffractometry (XRD), etch-pit observation by scanning electron microscopy (SEM), and cross-sectional transmission electron microscopy (XTEM). It was identified that a thin Al interlayer with a thickness of about 10 nm significantly improved the barrier property of the layer. For instance, the 20 nm-thick CVD-TiN layer which failed after annealing for 1 hour at 500°C did not fail even after 650°C annealing with a thin Al interlayer. The improvement of the barrier property is also demonstrated in the case of CVD-TaN layer.

11:15 AM D6.7
A STUDY ON CVD TaN AS A DIFFUSION BARRIER FOR Cu INTERCONNECTS. Se-Joon Im, Soo-Hyun Kim, Sung-Rae Cho, Ki-Bum Kim, School of Materals Science and Engineering, Seoul National University, Seoul, KOREA; Ki-Chul Park, Samsung Electronics Co. Ltd., Kihung, KOREA.

Tantalum nitride film was deposited by chemical vapor deposition with the aid of ion beam (ion-beam induced CVD, IBICVD). The IBICVD system consists of two parts. One is the deposition chamber and the other is the ion beam source. The ion beam source is composed of the plasma tube and two grids. The upper grid is electrically floated to repel most of the electrons and attract ions from the plasma. The lower grid is biased to 1kV in order to extract and accelerate the ions. The ion beams are used to bombard the film surface during film growth and thereby increase the film density. The ions have the energies between 115eV and 127eV.[1] Ion current density is about $7.7 \sim 13.9 \mu A/cm^2$[1] as lower grid bias is changed. TaNx films were deposited using pentakis(diethylamido)-tantalum-(PDEAT) as a precursor under the bombardments of N-, Ar- or H- ion beam. For comparison, two kinds of thermally-deposited TaNx films were prepared. One was deposited using PDEAT as a single precursor and the other used was PDEAT as a precursor with hydrogen. In case of N_2 IBICVD, deposition rate leveled off in the whole temperature range. In case of thermal CVD, the deposition rate was controlled by the surface reaction with an activation energy of about 1.0eV. The activation energy of Ar and H_2 IBICVD was about 0.3eV. The film resistivity was decreased with increasing deposition temperature except Ar IBICVD case. It also showed that the film resistivity of IBICVD TaNx was lower than that of thermally grown TaNx. The minimum resistivity of TaNx films was about $600 \mu\Omega$-cm, which was deposited at 350°C by using Ar-ion beam. TaNx films (50nm) deposited at 325°C were tested as diffusion barriers for copper. After 650°C annealing, all the sheet resistance increases dramatically.

11:30 AM D6.8
THE 2,2,6,6-TETRAMETHYL-2-SILA-3,5-HEPTANEDIONE ROUTE TO THE CHEMICAL VAPOR DEPOSITION OF COPPER FOR GIGASCALE INTERCONNECT APPLICATIONS.
Rolf U. Claessen, John T. Welch, Paul J. Toscano, Kulbinder K. Banger, Andrei M. Kornilov, Eric T. Eisenbraun and Alain E. Kaloyeros, NYS Center for Advanced Thin Film Technology, University at Albany, SUNY, Albany, NY.

A new class of copper(II) precursors has been developed for the chemical vapor deposition (CVD) growth of copper for applications in ultralarge scale integration interconnect schemes, including conformal seed layer for gigascale Cu integration and ultrathin Cu lines with enhanced conductivity characteristics. The synthesis is described of the sila-β-diketone 2,2,6,6-tetramethyl-2-sila-3,5-heptanedione (tmshdH) in good yields, (60%) via a Claisen type condensation of acetyltrimethylsilane with trimethylacetylchloride. Copper acetate was allowed to react with the ligand to yield the precursor $Cu(tmshd)_2$, which has been sublimed and characterized by thermogravimetric, elemental and crystallographic analysis and mass spectrometry. $Cu(tmshd)_2$ is appreciably more volatile than nonsilylated analogs such as $Cu(tmhd)_2$ and $Cu(tmod)_2$ (tmhdH = 2,2,6,6-tetramethyl-3,5-heptanedione; tmodH = 2,2,7-trimethyl-3,5-octanedione). The complex crystallized in the orthorhombic space group Pbca with a = 10.255(3) $\AA$, b = 11.692(3) $\AA$, c = 22.928(6) $\AA$, V = 2749.3(12) $\AA^3$, and Z=4. The packing diagram reveals that the molecules are well-separated in the solid suggesting that the intermolecular separations are slightly greater than that of $Cu(tmhd)_2$ or $Cu(tmod)_2$. The CVD process employs $Cu(tmshd)_2$ as the metalorganic precursor and hydrogen as reducing and carrier gas. The deposition tool was a custom - made, cold wall, stainless steel CVD reactor equipped with electronic mass flow controllers, and appropriate delivery systems. Copper films were produced at a substrate temperature of 250 - 320 °C, hydrogen flow rates of 20 - 100 sccm, deposition pressure of .2 - 1 Torr, and source temperature of 120 - 135 °C. The films were analyzed by x-ray photoelectron spectroscopy, cross - section scanning electron microscopy, transmission electron microscopy, four-point resistivity probe, Rutherford backscattering spectrometry and Auger electron spectroscopy. Keyfindings from these studies will be reported and discussed. In particular, resistivities as low as 2 $\mu\Omega$·cm were achieved for 40-nm-thick films.

11:45 AM D6.9
A SEEDLESS ELECTROCHEMICAL PLATING PROCESS FOR Cu-BASED INTERCONNECTS.
Chia-Hsuan Lo, Wei-Tsu Tseng, Shih-Chin Lee, Dept. of Materials Science & Engineering, National Cheng-Kung University, Tainan, TAIWAN.

Since the advent of Cu-based metallization for sub-0.25um ULSI interconnects, electroplating or electroless (i.e., electrochemical) plating technique has replaced sputter as the mainstream deposition process for Cu. Both processes, however, require the deposition of a sputtered Cu seed layer from concerns over uniformity and micro-structural quality. This inevitably raises the process complexity and cost of ownership for process integration. In this study, a simple one-step seedless electrochemical deposition process for Cu thin films is developed and characteristics of resulting Cu films are analyzed. Cu bath containing buffered HF, nitric acid, and Cu ions is adopted and the TaN/Ta/oxide wafers are used as the substrate. A resistivity of 2.2 uohm-cm and a deposition rate of ~220 nm/min can be constantly achieved. For comparisons, substrates with a 30 nm PVD Cu seed layer on TaN/Ta barrier are also included. Heating of the substrate before deposition was found to effectively improve the adhesion of the Cu deposited. Chemical analysis employing NMR and ESCA will be performed to characterize the change in chemistry of the bath, and the results would help understand the basic deposition mechanism. This seedless deposition process will be applied to fill in MIT density patterned wafers with minimum feature of 0.25 um. Organic-based surfactant will be added to improve the gap filling capability. The properties between the bulk and damascene Cu will be compared. Last but not the least, the CMP behavior of the Cu deposited will be evaluated.

SESSION D7: INTERCONNECTS
Wednesday Afternoon, April 26, 2000
Golden Gate B2 (Marriott)

1:30 PM *D7.1
FABRICATION AND PERFORMANCE LIMITS OF SUB-0.1 μm Cu INTERCONNECTS.
T.S. Kuan, C.K. Inoki, G.S. Oehrlein, Dept of Physics, Univ at Albany, SUNY, Albany NY; K. Rose, Y. Zhao, G.C. Wang, Rensselear Polytechnic Institute, Troy, NY; S.M. Rossnagel, C. Cabral, IBM T.J. Watson Research Center, Yorktown Heights, NY.

As the on-chip interconnect linewidth and film thickness shrink below 0.1 μm, the size effect on Cu resistivity becomes important, and the electrical performance deliverable by such narrow metal lines needs to be assessed critically. From the fabrication viewpoint, it is also crucial to determine how structural parameters affect resistivity in the sub-0.1 μm feature size regime. We have fabricated test structures containing 50-nm-wide Cu lines wrapped in Ta-based liners and embedded in insulating SiO_2 using e-beam lithography, high-density plasma etching, ionized PVD Cu deposition, and chemical-mechanical planarization processes. Direct current (16 ρA) resistance measurements from these 50-nm-wide Cu lines indicate a distribution of resistivity about 3 5 times that of bulk Cu values. To evaluate quantitatively the scaling of resistivity with thickness and to determine the scattering parameter ρ at the Cu/liner interfaces, we have also fabricated a series of $Ta/Cu/Ta/SiO_2$ thin film structures with Cu thicknesses ranging from 1 μm to 20 nm. As film thickness decreases from 60 to 20 nm, a standard model predicts a 25% to 75% increase in resistivity, assuming 100% diffuse scattering (ρ = 0) at atomically flat Cu surfaces. However, a far larger (~2.5 χ) size effect is measured from our sub-0.1-μm-thick, Ta-clad Cu films. Cross-sectional TEM and surface AFM observations suggest that the observed larger resistivity increase can be attributed to Cu/Ta surface roughness and limited grain growth in ultra-thin Cu films. Monte Carlo simulations are used to demonstrate the effect of carrier scattering at Cu/Ta interfaces and to quantify the extra resistivity resulting from interface roughness.

2:00 PM D7.2
FAILURES INDUCED BY BIAS-TEMPERATURE STRESS IN Cu/BCB INTERCONNECTS.
Taiheui Cho, Paul S. Ho, Microelectronics Research Center, University of Texas at Austin, Austin, TX; Sang U. Kim, Volker Blaschke, Sematech Inc., Austin, TX.

Copper/low-k interconnects are proposed to replace Aluminum/SiO_2 based interconnects for improving performance and density of deep submicron interconnects. Since Cu easily diffuses into an adjacent dielectric material, a highly efficient barrier is needed to avoid interconnect failures induced by Cu diffusion. In order to study Cu/low-k interconnect failures, Divinyl Siloxane Bisbenzocyclobutene (DVS-BCB) as an interlayer dielectric and Ta as a barrier layer were used to form single level test structures to evaluate the electrical reliability of Cu/low-k interconnects. When the interconnect structures were tested under bias-temperature stress (BTS) conditions to accelerate Cu diffusion, two types of device failures were observed. One type was early-failure due to defects in the diffusion barrier. Although the Ta barrier was supposed to cover Cu lines completely, Cu diffused quickly through defects in the barrier under BTS at 200 deg.C in these devices. The activation energy for Cu drift was found to be 0.91eV, which is similar to the activation energy found for structures without barrier. Another type of failure occurred due to Cu diffusion through grain boundaries in the barrier layer, for devices where the barrier covered the Cu lines well. The failure process was much slower than for the early-failures and the time-to-failure was almost comparable to that in single damascene Cu/SiO_2 interconnect structures. In this case, the time-to-failure is determined mostly by the barrier material and not the dielectric.

2:15 PM D7.3
TANTALUM-NITRIDE DIFFUSION BARRIER STUDIES USING THE TRANSIENT-ION-DRIFT TECHNIQUE FOR COPPER DETECTION. Thomas Heiser, Christophe Brochard, Univ. Louis Pasteur, Laboratoire PHASE-CNRS, Strasbourg, FRANCE; Mario Swaanen, STMicroelectronics, Crolles, FRANCE and Royal Philips Electronics, Eindhoven, THE NETHERLANDS.

Although diffusion barriers are a key part of the copper interconnect technology, a quantitative method to evaluate the barrier efficiency against copper diffusion in terms of metal contamination is still missing. In this work we show that the recently developed transient-ion-drift (TID) technique, which can detect a bulk copper concentration as low as $10^{12}cm^{-3}$, is particularly well suited for diffusion barrier investigations. The method estimates quantitatively the copper concentration from the capacitance transients of a Schottky barrier which arise when copper ions drift out of the depletion region towards the quasi-neutral region. The permeability of a 5 nanometer thick Tantalum-Nitride film has been studied by monitoring the bulk copper concentration, with TID, after various heat treatments. The spatial correlation between the copper contamination and the localized copper source is used to distinguish between background contamination and copper impurities that have crossed the barrier. Defining the efficiency of the barrier in terms of the ratio between the copper concentration and its solubility limit at the annealing temperature, we can follow the barrier breakdown as a function of the thermal stress. For instance, no copper is detected after two hours at 500°C, while at 600°C the copper solubility ($7\times10^{14}cm^{-3}$) is reached within about two hours. Combining the quantitative characterization of the barrier efficiency by TID with already existing analytical tools will allow us to investigate the relationship between barrier breakdown kinetics and film microstructure.

2:30 PM D7.4
RELIABILITY OF TANTALUM BASED DIFFUSION BARRIERS BETWEEN COPPER AND SILICON. Tomi Laurila, Kejun Zeng, Jorma Kivilahti, Helsinki University of Technology, Lab of Electronics Production Technology, Espoo, FINLAND; Jyrki Molarius, Ilkka Suni, VTT Microelectronics, Espoo, FINLAND.

Recently considerable interest has been paid to use Cu as on-chip metallisation in microelectronic devices - mainly due to its lower electrical resistivity and higher electromigration resistance as compared with aluminium. In order to reliably utilize copper metallisation in integrated circuits a diffusion barrier layer must be used to cap the copper conductors from all sides. Refractory metals such as tantalum are clear choices for these barrier layers due to their high melting points and other favourable properties. However, according to our investigations elemental tantalum may not posses sufficient thermal stability when in contact with Si and Cu. In order to improve the performance of the barrier layers it is essential to understand the underlying mechanisms leading to the failure of the chosen metallisation system. This can be achieved by using a combined thermodynamic and kinetic approach. By utilizing this method it was found that the use of binary tantalum compounds like tantalum nitride could improve the performance of the barrier layers. In this paper reaction mechanisms in the Si/Ta/Cu and $Si/Ta_xN_{1-x}/Cu$ metallisation systems and their relation to the microstructure of the thin films are discussed on the basis of the experimental results and the assessed ternary Si-Ta-Cu, Si-Ta-N and Ta-N-Cu phase diagrams at 973 K.

3:15 PM *D7.5
MICROSTRUCTURAL ANALYSIS OF COPPER INTER-CONNECTIONS USING PICOSECOND ULTRASONICS. J.M.E. Harper, H.J. Maris*, S.G. Malhotra, C. Cabral Jr., C. Lavoie, H.-Y. Hao* and W. Homsi*, IBM-T.J. Watson Research Center, Yorktown Heights, NY. *Department of Physics, Brown University, Providence, RI.

Picosecond ultrasonic measurements are shown to provide detailed information on the physical properties of copper interconnection structures. The technique generates several types of response in the time-resolved optical reflectivity, spanning time scales from picoseconds to nanoseconds. The responses can be broadly separated into the mechanisms of electron heating (psec), acoustic wave generation and propagation (10 to 1000 psec) and thermal coupling to the substrate (100 to 3000 psec). With blanket thin films, these signals may be analyzed for information on film thickness, roughness, resistivity, microstructure and interface integrity. Additionally, with patterned copper interconnection structures, resonant oscillations of the copper lines are observed, which relate directly to the line dimensions. Finally, we describe a long-lived oscillation pattern which appears in arrays of narrow lines. The limits of detection for various microstructural features are described.

3:45 PM D7.6
STUDY BARRIERS' EFFECTS ON THE RELIABILITY OF Cu INTERCONNECT: MICROSTRUCTURES AND STRESS. X. Zhang, H. Solak, F. Cerrina Electrical and Computer Engineering and Center for Nanotechnology, University of Wisconsin-Madison, WI; B. Lai, Z. Cai, P. Ilinski, D. Legnini, W. Rodrigues, Advanced Photon Source, Argonne National Laboratory, Argonne, IL.

Copper has been chosen as the interconnect material to replace aluminum-based alloys for advanced IC circuits. It has lower resistivity and higher electromigration resistance. Many research efforts have been put into this area for the past two decades and will be put into for many years to come. Cu technology is much more complicated than Al interconnect technology. It requires diffusion/drift barriers to prevent Cu from diffusing into dielectrics and Si substrate. Many candidates have been evaluated for this purpose, such as Ti, TiN, Ta, TaSiN, W, *etc.* Most previous research is focused on these materials' adhesion promotion and barrier effect. It is also well known that these refractory metals usually introduce huge stress in their thin film stackes. In our experiment, we will focus on how these thin film barriers affect Cu microstructures and stress in the Cu interconnect lines, and therefore affect the reliability issues of Cu wires.
Our Copper interconnects were fabricated using lift-off process. A Leica electron beam lithography tool was used to directly write all the patterns. Five different linewidths were used in this experiment, varied from $2\mu m$ to $0.25\mu m$. The length of all lines was $800\mu m$. Electron beam evaporation was used to deposit Cu(350nm) and various barriers on these wafers. $SiN(0.2\mu m)$ and $SiO(0.4\mu m)$ were deposited as passivation layer using plasma-enhanced chemical vapor deposition at 350°C. All samples were annealed at 450°C for 30 minutes in a $N_2(90\%)/H_2(10\%)$ mixture.
An Atomic Force Microscope was used to investigated the microstructures of Cu film. Various microstructures has been observed in our initial experiment. Significant grain growth after annealing was also observed. Various methods have been used to measure the stress in Cu film, including wafer curvature method and X-ray diffraction. From our initial data, we found that the stress in Cu film has a strong relationship with it environment and its process history.
Electromigration tests have been conducted on various samples. Our results shows that microstructures of interconnect lines affect the lifetime of Cu interconnect. The interconnect with smaller linewidth showed longer lifetime, since narrower lines usually have bamboo or near-bamboo structures which have less grain boundaries. Electromigration activation energy of one kind of sample has been obtained at this moment. The activation energy of our $2\mu m$ wide Cu(350nm)/Ti(20nm) lines is 0.71eV. The stress effect and linewidth effect on Cu reliability is under further investigation.

4:00 PM D7.7
NEAR-FIELD PHOTOLUMINESCENCE AND RAMAN SPECTROSCOPY OF DEFECTS AND STRAIN IN COPPER DAMASCENE INTERCONNECT STRUCTURES. Grover C. Wetsel and Austin J. Cunningham, The University of Texas at Dallas, Richardson, TX; James B. Spicer, Johns Hopkins University, Baltimore, MD; Robert Kraft, Texas Instruments, Inc., Dallas, TX.

Demands for higher speed and lower power consumption in the next generation of semiconductor logic and memory devices dictate that interconnect dimensions shrink to 150 nm or less and that new materials and processes be used in integrated-circuit manufacture. Early identification and control of the process-induced defects and strain to a positional accuracy in harmony with the diminishing design features will be required to allow device yield and reliability to reach acceptable commercial levels. In this context we report on the use of near-field optical spectroscopy to measure process-induced defects and strain. Spatial measurements of copper concentrations across sectioned Cu-xerogel damascene structures relate to Cu confinement across different Ti-, Ta- and Si-N barrier combinations and contact points. Near-field-optical techniques, where the lateral definition is of the order of the size of the aperture, are required in order to accommodate the submicrometer design rules. A near-field scanned optical microscope (NSOM) capable of measuring simultaneous topographical and optical images is being directed to this application. This NSOM was previously used to measure the photoluminescence in porous Si with an optical definition of the order of 20 nm; operated as a nano-Raman spectrometer, the NSOM-measured Raman shift allowed determination of mean microcrystallite sizes as small as 2.8 nm in porous Si. In addition, an apertureless near-field-optical probe (ANSOM), which uses a sharpened metal probe, is being developed to improve the lateral optical definition to the order of 1 nm or better. Results will be reported on Cu diffusion across barriers of different thickness, on strain, and on delamination at nitride-barrier low-k dielectric interfaces. Preliminary results on strain measurements before and after annealing will be included.

4:15 PM D7.8
QUANTITATIVE METROLOGY STUDY OF IC Cu/SiO_2

INTERCONNECT TECHNOLOGY USING NANOSCALE X-RAY MICROSCOPY. X. Su, C. Stagarescu and D.E. Eastman, James Franck Institute, University of Chicago, Chicago, IL; B.P. Lai, Z. Cai, I. McNulty and S. Frigo, Advanced Photon Source, Argonne National Laboratory, Argonne, IL; I.C. Noyan and C.-K. Hu, IBM-T.J. Watson Research Center, Yorktown Heights, NY.

We will describe nondestructive measurements of multilayer submicron Cu/SiO_2 interconnect BEOL structures and electromigration defect structures using nano-scale SXTM (Scanning X-ray Transmission Microscopy) and SXFM (Scanning X-ray Fluorescent Microscopy). We have used tunable x-ray beams ($\sim$ 2 kev and 10 kev) at the 7 Gev Advanced Photon Source (APS) that were focused to $\sim$ 150 nm diameter with Fresnel Zone Plates (FZP). Quantitative measurements have been made on multilayer BEOL structures with widths, lengths and thicknesses (heights) of copper and tungsten lines and vias with lateral dimensions down to 300 nm and heights down to 200 nm. Typical measurement uncertainties are $\sim$ 60 nm for widths and lengths and $\simeq$ 10% for thickness. We have quantitatively studied electromigration depletion of submicron vias and lines and can nondestructively measure buried voids with good accuracy. These new x-ray microscopy techniques are facilitated by the brilliance of the third generation APS synchrotron radiation source together with instrumentation advances (e.g., nanoscale FZP beam focusing). Measurements of specific elements in multilayer structures are optimized by selecting suitable x-ray energies, especially using SXFM which is very element-specific with high sensitivity. SXFM has the convenience of using un-thinned Si wafer substrates, whereas SXTM requires substrate thinning to 5-10 μm. We have also performed scanning x-ray diffraction measurements and have determined lattice constants and strains of single crystal grains in 300 nm copper lines. These new techniques are expected to be very powerful in nondestructive characterization of the physical, chemical and electrical structures of nanoscale materials and their substructures. This work is supported by the DOE under Contract No. W-31-109-ENG-38.

SESSION D8: POSTER SESSION: INTERCONNECTS

Wednesday Evening, April 26, 2000
8:00 PM
Salon 1- 7 (Marriott)

D8.1

INTEGRATED CVD-PVD Al PROCESS FOR SUB-QUARTER MICRON DEVICES: EFFECTS OF THE BARRIER METAL ON THE VIA FILLING AND THE MICROSTRUCTURE OF THE ALUMINUM FILM. Won-Jun Lee, Jun Ki Kim, Jin Won Park, Hyundai MicroElectronics Co, Ltd, R&D Div, Cheongju, KOREA; Sa-Kyun Rha, Taejon National Univ of Technology, Dept of Information and Communication-Computer Engineering, Taejon, KOREA.

The integrated CVD-PVD Al process was successfully applied to sub-quarter micron devices for the simultaneous formation of plugs and wires. The effects of the barrier metals on the via filling and the microstructure of the integrated CVD-PVD Al films were investigated. The Ti films deposited by the ionized PVD (I-PVD) method and the MOCVD TiN films stacked on the I-PVD Ti films (Ti/TiN) were examined as the barrier metal. The effects of thin PVD Al layer between the barrier metal and the CVD Al film were also investigated. The morphology, texture and sheet resistance of the CVD-PVD Al films were analyzed using the blanket wafers, and the filling capability and the electrical and reliability characteristics were evaluated using the device wafers. Excellent via filling was achieved by employing the Ti/TiN film as a barrier metal. However, the degree of the $< 111 >$ texture of the CVD-PVD Al film decreased with increasing the thickness of the MOCVD TiN film. Reducing the thickness of the MOCVD TiN film below 5 nm was essential to obtain the excellent $< 111 >$ texture of the Al film. The deposition of the PVD Al film prior to the CVD Al improved the $< 111 >$ texture and surface morphology of the CVD-PVD Al film, especially on the Ti/TiN barrier metal. The CVD-PVD Al process showed lower via resistance and better electromigration resistance than the standard W plug process. The implementation of the CVD-PVD Al process to 1-Gigabit DRAMs will be also presented.

D8.2

$TiCl_4$-BASED PECVD Ti/CVD TiN CONTACT BARRIER LAYERS FOR TUNGSTEN BIT LINE APPLICATION. Yoon-Jik Lee, Jun Ki Kim, Jin Won Park, Hyundai MicroElectronics Co, Ltd, R&D Div, Cheongju, KOREA; Sa-Kyun Rha, Taejon National Univ of Technology, Dept of Information and Communication-Computer Engineering, Taejon, KOREA.

Tungsten is a very promising material for the bit line application in the advanced DRAM technology owing to its lower resistivity than conventional W-polycide and the capability of forming the ohmic contacts to both N+ and P+ active areas. However, high thermal budget after the bit line formation can easily degrade the contact characteristics on the active region, especially in the COB (Capacitor Over Bit line) type DRAM. In this point of view, we have extensively developed the thermally stable W bit line structure using PVD Ti/PVD TiN as a barrier layer and RTP for the formation of silicide contact. In this work, the barrier structure of PECVD Ti/CVD TiN was investigated to solve the step coverage problem of PVD method and reduce the total process steps by in-situ silicidation. The properties of as-deposited Ti thin films were examined using various characterization methods, such as XRD, SEM, ESCA, AFM and TEM. The roughness of Ti silicide/Si interface and Si consumption during Ti deposition were controlled by adjusting process parameters, especially $TiCl_4/H_2$ flow ratio for the reliable junction property. Based on the contact resistance and junction leakage current data, we optimized the process and thickness of PECVD Ti/CVD TiN and successfully integrated with CVD W for the bit line application in the deep sub-quarter micron DRAM.

D8.3

A SHIFTING PHENOMENON OF INTERCONNECTION LINES ON BPSG FILM DUE TO SUBSEQUENT THERMAL PROCESS FOR SUB-QUARTER MICRON CMOS FABRICATION. Sung-Kwon Lee, Hyun-Cheol Kim, Jong-Woo Kim, Hyung-Dong Lee, Sook-Rak Ma, Gug-Seon Choi, Kwang-Sik Son, Memory Research and Development, Hyundai MicroElectronics Industries Co., Ichon-si, Kyoungki-do, KOREA.

Recently the density of semiconductor devices has increased due to the advances of device and process technology including the planarization technology. We investigated quantitatively, for the first time, the shifting phenomenon of polysilicon interconnection lines on planarized BPSG (Borophosphosilicate Glass) film after subsequent thermal process. The shifting of polysilicon interconnection lines apparently due to BPSG film reflow, which resulting in the interconnection line bridge and thus device failure, was not observed in the cell region but in the periphery region. The shifting distance of interconnection lines becomes more than 0.30um depending on the topological differences, pattern density and on the process temperatures. The shifting was even observed in the CMP (Chemical-Mechanical Polishing) planarized BPSG film. The device failure originating from this phenomenon makes its detection almost impossible unless the appropriate test patterns are provided. For quantitative study, the various process temperatures (e.g. 800°...850°), and the Boron and Phosphorous contents in BPSG film were extensively examined for several different line and spacing interconnections (Design Rule: 0.18um to 0.55um). Also, to find out the process conditions for minimum shifting distance without adding extra process steps (e.g. Formation of metal contact spacer), the experimental study for various dielectric materials (e.g. LP-TEOS, PE-TEOS and USG film etc.) including the optimal BPSG Etch back was conducted. Our combined process integration offered very stable process tools with high reliability for manufacturing sub-quarter micron CMOS devices and beyond technology.

D8.4

BACKSIDE COPPER CONTAMINATION ISSUES IN CMOS PROCESS INTEGRATION - A CASE STUDY. K. Prasad, K.C. Tee, School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore, SINGAPORE; L. Chan, A.K. See, Chartered Semiconductor Manufacturing Ltd., Singapore, SINGAPORE.

Experimental results are presented on the effects of deliberately contaminating the backside of silicon wafers with fully functional MOS devices. MOSFETs with various channel lengts down to 0.25 μm were fabricated on silicon using conventional twin well process. Conventional SALICIDE process was implemented. The wafers were thinned down to 250 μm by back grinding. The backside of the sample was deposited with 200 nm PVD-Cu. The samples were subsequently annealed in nitrogen ambient at 400°C for times up to 10 hours. Various MOS parameters such as the threshold voltage V_{T0}, transconductance g_m, drain saturation current I_{DSAT}, off-current I_{off}, and gate leakage current I_{Gleak} were monitored during the annealing. Also monitored was the leakage currents of n+/p and p+/n junction diodes. The experimental results show that the presence of copper on the backside of the wafers during annealing did not affect the MOS parameters. MOSFET parameters remained unchanged even after 10 hours of annealing. Also, the junction leakage currents did not change after 10 hours of annealing. Conventional calculations of copper diffusion depth show that copper should diffuse all the way through the wafer after only 30 minutes of annealing. If so, the device properties should show degradation. However, the results from our study show that copper has not diffused all the way into Si. To

investigate the diffusion of copper, SIMS analysis was performed after 10 hours of annealing. Copper was stripped from the backside of the wafer before SIMS analysis. SIMS results show that copper has diffused into silicon only over a very short distance of around 300 nm from the backside of the wafer. X-ray diffraction studies revealed that a layer Cu_3Si was formed at the backside of the wafer. We believe that the formation of copper silicide, in addition to any copper precipitation in silicon, is responsible for slowing down the diffusion of copper into Si. Copper concentration beyond 300 nm from the backside of the wafer was below the SIMS detection limit. Similarly, the Cu concentration on the front side of the wafer was, again, below the detection limit. Thus, the regions where the active devices are present have either no copper or very little copper, well below the SIMS detection limit. As a result, the electrical parameters of MOSFETs and leakage currents of p-n junctions are not affected despite the presence of backside copper contamination. Thus, we believe that the backside copper contamination may not pose serious problems in copper integration.

D8.5
MEASUREMENT OF LOCALIZED STRAINS IN NARROW INTERCONNECTS BY CONVERGENT-BEAM ELECTRON DIFFRACTION. R.R. Keller, National Institute of Standards and Technology, Materials Reliability Division, Boulder, CO; J.A. Nucci, S. Krämer, Max-Planck-Institut für Metallforschung, Stuttgart, GERMANY.

Convergent beam electron diffraction (CBED) was used to investigate localized lattice strains in both sputtered aluminum and damascene copper interconnects of width ranging from 0.3 to 2.0 μm. This method provided measurements from areas of approximate diameter 10 to 100 nm, which enabled evaluation of triaxial strain states within individual grains. Lattice parameters were determined by measuring the higher order Laue zone (HOLZ) line positions in experimental zone axis patterns and subsequently comparing them to kinematical and dynamical simulations. Quantitative comparison was accomplished using a least squares analysis of distances between line intersections. The precision in strain determination was zone axis dependent, and ranged from approximately 2×10^{-4} to 1×10^{-3}, depending on the HOLZ reflections present. The Al interconnects locally exhibited large elastic strains due to thermal mismatch with the substrate and the corresponding stresses were much higher than the bulk yield strength. Deposition-induced strains in electroplated copper lines resulted in lattice distortions up to 3×10^{-3}. In addition to enabling analysis of localized strain states, another advantage of using CBED is that the microstructure and strain state can be simultaneously evaluated. This technique yields results complementary to those obtained by global methods such as X-ray diffraction and may provide insight into localized failure phenomena.

D8.6
IN-SITU ELECTROMIGRATION INDUCED STRAIN MEASUREMENTS FROM SINGLE GRAINS IN PASSIVATED ALUMINUM CONDUCTOR LINES BY X-RAY MICRO-DIFFRACTION. K.J. Hwang, G.S. Cargill III, Lehigh Univ., Dept. of Materials Science and Engr., Bethlehem, PA; T. Marieb, Components Research, Intel Corp., Santa Clara, CA.

X-ray microdiffraction is a powerful tool for investigating materials on a micron length scale, particularly for direct measurement of strain in encapsulated interconnect structures. We used microdiffraction for the study of electromigration-induced strains in interconnects on the BNL-NSLS bending magnet beamline X6A with a 7 μm x 10 μm white x-ray beam formed by pinhole collimation, with a useful energy range of 6 keV to 30 keV. Energy-dispersive diffraction measurements were made for Al single grains in symmetric-reflection and asymmetric-reflection modes to map out the triaxial strains in a polycrystalline 2.6 μm wide, 300 μm long, 0.5 μm thick Al conductor line under 1.5 μm SiO_2 passivation. Four sets of (hkl) Al planes were measured to determine the local triaxial strain at four positions along the interconnect. All reflections were tracked in both real and reciprocal space during electromigration. Measurements were made on the conductor line under electromigration stressing (270°C, $4 \cdot 10^5$ A/cm^2) in both forward current and reverse current conditions. Resistance measurements were made concurrently to correlate electromigration damage with measured local strain. Results for electromigration strain development will be discussed.

D8.7
EXPERIMENTAL STUDIES OF THE RELIABILITY OF INTERCONNECT TREES. Stefan P. Hau-Riege and Carl V. Thompson, Massachusetts Institute of Technology, Dept of Materials Science and Engineering, Cambridge, MA.

The electromigration resistance of simple straight-line interconnects is usually used to estimate the reliability of complex integrated circuits. This is generally inaccurate, and overly conservative at best. The shapes and connectedness of interconnects is not accounted for in standard reliability assessments. We have identified the interconnect tree as the fundamental reliability unit. An *interconnect tree* consists of connected conducting line segments lying within a single layer of metallization, and terminating at two or more nodes at which there is a diffusion barrier such as a W-filled via. We performed electromigration experiments on the simplest tree structures, such as L- and T-shaped interconnects, as well as straight lines with an additional via in the middle of the line, passing currents of different magnitudes and directions through the limbs of the trees. We found that metal limbs ending in other limbs can act as reservoirs for electromigrating metal atoms. Passive reservoirs, which are limbs that do not carry electrical current, are generally beneficial for reliability, whereas limbs that do carry electrical current, called active reservoirs, can be beneficial or detrimental, depending on the direction and magnitude of the current in the reservoir. However, our experiments show that bends in interconnects do not affect their reliability significantly. We also found that the reliability of an interconnect tree can be conservatively estimated by considering void-growth and void-nucleation-limited failures at the most heavily stressed junction in the tree, which can be found by analyzing the geometry and current configuration. Our experimentally verified model for tree reliability can be used with layout tools for reliability-driven computer-aided design (RCAD), through ranking of the reliabilities of trees in order to identify areas at risk from electromigration damage.

D8.8
GRAIN ORIENTATION AND STRAIN MEASURMENTS IN MICRON WIDE PASSIVATED INDIVIDUAL Al AND Cu TEST STRUCTURES. A.A. MacDowell, R. Celestre, H.A. Padmore, N. Tamura, Advanced Light Source, Lawrence Berkeley National Lab., Berkeley, CA; R. Spolenak, W. Brown, Lucent Technologies, Murray Hill, NJ; T. Marieb, Intel Corp., Portland, OR; B. Valek, J. Bravman, P. Flinn, Material Science Dept., Stanford Univ., Stanford, CA; B.W. Batterman, J.R. Patel, Advanced Light Source, Lawrence Berkeley National Lab., Berkeley, CA and SSRL/SLAC, Stanford Univ., Stanford, CA.

At the Advanced Light Source Berkeley we have, over the last few years developed equipment and systems for measuring orientation and strain of individual grains within passivated thin film interconnects with a spatial resolution at the micron and sub micron level. A white x-ray beam of typical dimensions of 1 micron in size is generated when synchrotron radiation is focused using elliptically bent Kirk Patrick-Baez mirrors in a grazing incidence geometry. With white beam, Laue patterns of individual grains of Cu or Al can be recorded in $\sim$ 1 sec. For monochromatic light a four-bounce crystal monochromator can be inserted into the beam without disturbing the original beam position on the sample. Strain measurements are made by determining the energy of the diffracted beam with high accuracy. Using a silicon single crystal standard for calibration our goal is to achieve lattice parameter measurements with a precision of 10 ppm. The experiments can be carried out at elevated temperatures and under the stress of an electrical current. Strain gradient measurements made with these facilities in passivated Cu and Al lines under electromigration stress will be described.

D8.9
THE INFLUENCE OF STRESS-INDUCED VOIDING ON THE ELECTROMIGRATION BEHAVIOUR OF AlCu INTERCONNECTS. A.H. Fischer and A.E. Zitzelsberger, Infineon Technologies, Reliability Methodology, Munich, GERMANY.

Stress-induced voiding in metal interconnects is an important aspect of reliabilty methodology. The phenomenon was observed in multilevel ULSI AlCu metallizations, leading to voids in the metal line before electrical operation. The appearance of stress voids could be suppressed reducing the deposition temperature of a HDP CVD SiO_2 process. The influence of pre-existing stress voids on the electromigration performance is investigated in the paper.
Electromigration tests were performed on samples with as well as without pre-existing stress voids, using C1M1 via line teststructures, one with a short 30m and the other with a long 400μm metal line respectively. In the first part, the activation energy E_a and current density exponent n were determined. Between both samples no significant differences in E_a, median time to failure or shape factor σ of the lognormal failure distribution were found. However, n is slightly smaller for samples with stress voids (short lines 1.4, long lines 1.0) in comparision to those without stress voids (n=1.7).
The second part of the investigations was focused on short C2M1 structures. Here, typical bimodal failure distributions were found at 250°C for both samples, having two clearly distinguishable branches belonging to two different physical failure modes. The early branch corresponds to electromigration voiding in the line and the late branch to voiding just at the via. The data sets could be fitted well assuming a superposition of two lognormal distributions. The bimodality was further investigated at various temperatures. It was

found, that failure distributions for samples with pre-existing stress voids showed a distinct bimodal behaviour down to 170°C, whilst those without stress voids became monomodal at lower temperatures. The implications of smaller current density exponents in stress void damaged lines on the extrapolated lifetime will be discussed in the paper as well as the consequences of bimodality.

D8.10
SIMULATION OF THE ROLE OF COPPER IN ELECTRO-MIGRATION OF A DILUTE Al(Cu) INTERCONNECT.
Saad Abdeslam, Cynthia Volkert, Max Planck Institut fuer Metallforchung and Institut fuer Metallkunde, University of Stuttgart, Stuttgart, GERMANY.

To improve the understanding of the effect of Cu in Al(Cu) alloy in electromigration, the electromigration process in Al(Cu) lines is simulated using 1D model. General fluxes expressions of both Al and Cu derived from microscopic parameters are used. In this simulation the parameters used are: temperature, Cu concentration, electro-migration driving force, mechanical driving force, and chemical driving force. Our results are qualitatively in accordance with some experimental observations and the time to reach a given stress is increased due to the addition of Cu. Such result can explain the beneficial effect of Cu on electromigration damage in Al(Cu).

D8.11
ELECTROMIGRATION-INDUCED STRESS INTERACTION BETWEEN VIA AND POLYGRANULAR CLUSTERS.
Young-Joon Park, Korea Institute of Science and Technology, Thin Film Technology Research Center, Seoul, KOREA; Young-Chang Joo, Seoul National Univ., School and Materials Science and Engineering, Seoul, KOREA.

Electromigration-induced failures are one of the most important threat to microelectronic devices. For near-bamboo interconnects, via and polygranular clusters are two most important sites of electro-migration flux divergences. Electromigration behaviors of these flux divergence sites have been studied separately, and little has known about the interaction between via and polygranular clusters. Conventionally, it is believed that the worst case lifetime occurs when via is just below (or above) the polygranular clusters. We have studied the interaction between via and cluster using electromigration simulation which calculates 1-dimensional stress evolution and diffusivity change during electromigration. By changing the location of the cluster with respect to the via, it has found that the worst case lifetime does not occur when polygranular cluster is just below the via, contradictory to the conventional knowledge. It can be explained by the fact that electromigration-induced stress gradient at the via depends on the distance between via and cluster. The dependence on current density, cluster length are also discussed.

D8.12
RESISTANCE DEGRADATION IN EARLY STAGE OF ELECTROMIGRATION OF Al-Cu METAL LINE. Q. Guo, K.F. Lo, I. Manna, X. Zeng, H.K. Yap, Chartered Semiconductor Manufacturing Ltd., Singapore, SINGAPORE.

Resistance drop in the early stage of electromigration (EM) of Al-0.5%Cu metal line with width ranging from 0.45um to 10um has been systematically investigated using high resolution resistance measurement (HRRM) whose temperature stability is better than 0.02C and voltage measurement resolution is better than 200ppm. EM tests were performed at the ambient temperatures in the range of 150C and 250C with a series of current from $1MA/cm^2$ to $5MA/cm^2$. It is observed that the resistance drop in the early stage consists of two parts. One is due to the temperature stress (refer to Rt), the other results from the current stress (refer to Ri). Both Ri and Rt strongly depend on the temperature. Generally, Ri decreases as temperature decreases. On contrary, Rt greatly increases as temperature is reduced from 250C to 150C. Ri strongly depends on the width of metal line. It is a main part in the wide metal line, but it is almost negligible as the width decreases to 0.45um. It will be demonstrated in the paper that Ri results from Cu diffusion along grain boundary, while Rt is probably attributed to microstructure variation and/or Cu precipitation. So it is very important to separate two different effects in the data analysis of the early resistance degradation. Otherwise, the compensatory effect will lead to an incorrect explanation. Absence of Ri part in narrow line indicates that the mechanism of resistance drop in narrow line with bamboo structure is significantly different from that in the wide line. There are considerable studies on the resistance drop in the early stage (usually referred to be incubation time). Most of them were in wide metal line. Our finding indicates that previous theory can not be simply applied to deep submicron metal lines.

SESSION D9: POSTER SESSION:
INTERCONNECTS–TEXTURE
Wednesday Evening, April 26, 2000
8:00 PM
Salon 1-7 (Marriott)

D9.1
TRENCH AND VIA FILLING WITH ELECTROPLATED COPPER: EFFECT OF CURRENT DENSITY AND PULSE WAVEFORM.
C.H. Seah, Thin Film Dept, Chartered Silicon Partners Pte Ltd, Singapore, SINGAPORE; S. Mridha, Div of Material Engineering, School of Applied Science, Nanyang Technological University, Singapore, SINGAPORE; L.H. Chan, Research and Development Dept, Chartered Semiconductor Manufacturing Ltd, Singapore, SINGAPORE.

Numerous authors have reported the successful filling of via hole and line trench with copper using normal pulse plating, however, no significant investigation has been conducted to study the effect of current density and pulse waveform on trench filling. In this study, the effect of these two parameters on the filling of via and trenches for sub-0.25 μm devices has been investigated. Normal pulse plating of copper was performed onto Si wafers patterned with line trenches and via holes of aspect ratio 2:1 and the growth pattern of these films were characterized. There is no difference in the growth pattern for the copper films deposited using 0.05 and 0.1 A/cm^2 current density. Small grains nucleated uniformly across both the line and via trenches after 1 sec of electroplating. When deposited for 2 sec, a slight buildup of the film thickness was observed in both trenches without significant increase in the size of the copper grains. Grain growth occurred after 5 sec involving the coalescence of small grains and finally after 10 sec of deposition, a further buildup in thickness and fill up of the trenches occurred. When the Si wafers were plated with a pulse waveform of 3 ms on + 0.5 ms off, the trench filling was not completed after 30 sec. Complete filling of the trenches without voids was achieved within 30 sec of electroplating using an on-period of 6-8 ms and an off-period of 1-2 ms., however when the on-period was further increased to 9.9 ms, void was found to be present at the centre of the via.

D9.2
THIN SMOOTH Cu FILMS DEPOSITED IN DEEP SUBMICRON TRENCH BY PLASMA CVD REACTOR WITH H ATOM SOURCE.
Masaharu Shiratani, Hong Jie Jin, Yasuhiro Nakatake, Kazunori Koga and Yukio Watanabe, Kyushu University, Dept. of Electronic Device Engineering, Fukuoka, JAPAN.

Thin smooth films of high-purity copper in deep submicron trench structures are a fundamental requirement in formation of metal interconnects in ULSI by using electrolytic Cu deposition. To deposite such thin smooth Cu films in trenches, we have developed a plasma CVD reactor equipped with an H atom source in order to control independently the concentration of H atoms and the degree of dissociation of $Cu(hfac)_2$, since H atoms are extremely effective in removing impurities within the film and in reducing film surface roughness, and deposition rate and film conformality presumably depend on the degree of dissociation of $Cu(hfac)_2$. High-purity Cu films (100%) with the low resistivity of 2 $\mu\Omega$cm can be deposited, even with a low H_2 gas volume fraction of 50–67%, by using the H atom source, while high-purity films are obtained only for an H_2 gas volume fraction above 90% for the CVD reactor without the source. In order to evaluate Cu conformality in trench structures using the plasma CVD reactor with the H atom source, coverage shape of the Cu film deposited in a trench 0.4 μm wide and 3.25 μm deep is examined. While the coverage at the bottom of trench is 0% for the main discharge power P_m = 80 W, it increases with decreasing P_m to reach 95% for P_m = 15 W. These results show that a decrease in P_m leads to a reduction in the surface reaction probability of Cu-containing radicals, a low value of which is essential for the achievement of conformal deposition in extremely small width and high aspect ratio trench structures. We also have succeeded in depositing smooth Cu films about 100 nm thick in a trench 0.3 μm wide and 1.8 μm deep using such control.
1) H. J. Jin, et al., Jpn. J. Appl. Phys. 38 (1999) 4492.

D9.3
THE INFLUENCE OF DUAL DAMASCENE STRUCTURES ON THE CRYSTALLOGRAPHIC TEXTURE AND ROOM TEMPERATURE RECRYSTALLIZATION OF ELECTROPLATED COPPER. D. Walther[1], M.E. Gross[1], K. Evans-Lutterodt[1], R. Spolenak[1], W.L. Brown[1], S. Merchant[2], M. Oh[2], S. Lytle[2]. [1]Bell Labs, Lucent Technologies, Murray Hill, NJ; [2]Bell Labs, Lucent Technologies, Orlando, FL.

The introduction of Cu for high performance IC interconnects represents a revolutionary change in material and architecture. Cu is being deposited by electroplating into damascene (recessed) templates etched in SiO_2. The implications of the damascene topography on the

materials properties and, ultimately, the reliability of the interconnects are not well understood. Studies of Cu in single damascene (trench) structures from 0.3 to 5.0 μm in width have shown a significant influence of topography on both the crystallographic texture and room temperature recrystallization process. A new sidewall texture component was identified using X-ray diffraction pole figure analysis corresponding to (111)-textured Cu deposited on the sidewalls.[1] Topography also plays a role in providing nucleation sites at the upper corners of the trenches for the room temperature recrystallization of the electroplated Cu.[2] Dual damascene architectures with trenches aligned over vias introduce additional topography into the deposition process. In this paper, we report results on the influence of dual damascene architectures on the texture and recrystallization of electroplated Cu. X-ray diffraction pole figure analysis of the Cu in the damascene structures reveal the importance of process sequence, i.e., whether overlying Cu is removed before or after recrystallization, on the final texture of the Cu. Focused ion beam plan view and cross-section images were analyzed to identify the nucleation sites for recrystallization and to derive kinetics as a function of trench width and via spacing for features down to 0.2 μm.
[1]C. Lingk, M.E. Gross, W.L. Brown, Appl. Phys. Lett. 74, 682 (1999).
[2]C. Lingk, M.E. Gross, J. Appl. Phys. 84, 5547 (1998).

D9.4
ROOM TEMPERATURE RECRYSTALLIZATION AND GRAIN GROWTH IN ELECTROPLATED AND SPUTTER-DEPOSITED COPPER THIN FILMS. M.E. Gross[1], D. Walther[1], S. Merchant[2], M. Oh[2]. [1]Bell Labs, Lucent Technologies, Murray Hill, NJ; [2]Bell Labs, Lucent Technologies, Orlando, FL.

Electroplated (EP) Cu films undergo recrystallization at room temperature that is related to additives in the plating bath used to achieve good fill characteristics and smooth surfaces for integrated circuit applications. Typically, a thin (<1,000Å) film of sputtered (PVD) Cu is deposited on the device wafer prior to plating to serve as the cathode. Although the grain sizes are comparable in the two types of Cu, sputter deposited Cu does not recrystallize at room temperature. Yet cross-section transmission electron microscopy (TEM) analysis of the PVD/1μm EP Cu interconnect structures after the room temperature recrystallization revealed a single, homogeneous, large-grained film with no distinction between the two Cu layers. In this paper, we report that at room temperature the recrystallization of an EP Cu film will induce grain growth in PVD Cu layers that are twice as thick, resulting in grains as large as 5-10μm across. Cross-section FIB images show that recrystallization nucleates in the EP layer and extends laterally and vertically through that layer before extending into the PVD layer. The kinetics of the recrystallization process as a function of the thickness of the PVD and EP layers offer insights into the mechanisms of the recrystallization process. In the absence of the EP Cu layer, temperatures in excess of 500°C would be needed to achieve similar growth in the PVD film.

D9.5
X-RAY MICROBEAM MEASUREMENT OF TRI-AXIAL STRAIN IN Al INTERCONNECTS IN FABRICATED MICROCHIPS. B.C. Larson, W. Yang, G.E. Ice, J.D. Budai and J.Z. Tischler, Oak Ridge National Laboratory, Oak Ridge, TN; N. Tamura, Advanced Light Source, Lawrence Berkeley National Laboratory, Berkeley, CA; J.-S. Chung, Materials Research Laboratory, University of IL, Urbana-Champaign, IL; W.P. Lowe, Howard University, Washington, DC.

Collaborative development of submicron x-ray beam diffraction capabilities on the MHATT-CAT beam line of the Advanced Photon Source and collaborative development of white/monochromatic analysis software at ORNL and LBNL have made possible direct measurement of grain orientation and tri-axial deviatoric strain in metal interconnects. We have combined white and monochromatic microbeam x-ray diffraction techniques to investigate inter- and intra-granular orientation and tri-axial strain in passivated Al interconnects in fabricated microchip devices. Critical aspects of the measurement and analysis techniques will be discussed, and results of strain measurements in interconnects of varying sizes and shelf-time after manufacture will be presented.
Research sponsored by the U.S. Department of Energy under contract DE-AC05-96OR22464 with Lockheed Martin Energy Research Corp. The x-ray measurements were performed on the MHATT-CAT beam line at the APS. The APS is supported by the DOE Office of Energy Research under contract W-31-109-ENG-38.

D9.6
FORMATION OF $Al_xO_yN_z$ BARRIERS FOR ADVANCED SILVER METALLIZATION. Y. Wang and T.L. Alford, Department of Chemical, Bio and Materials Engineering, NSF Center for Low Power Electronics, Arizona State University, Tempe, AZ.

Silver has been explored as a potential candidate for future advance interconnects due to its lowest electrical resistivity, when compared with Al and Cu. As in the case of Cu metallization, an additional layer between the Ag film and underneath dielectric is necessary in order to improve adhesion and to block the diffusion of Ag atoms. In this study, thin aluminum oxynitride ($Al_xO_yN_z$) diffusion barriers have been formed in the temperature range of 400-725 °C by annealing Ag/Al bilayers on oxidized Si substrates in ammonia ambient. Rutherford backscattering spectrometry showed that the out-diffused Al reacted with both the ammonia and oxygen in the ambient and encapsulated the Ag films. Higher processing temperatures and thinner original Al layers showed to improve the resistivity of the encapsulated Ag layers. The resulting Ag resistivity values are ~1.75 ± 0.35 $\mu\Omega$-cm. The thermal stability test of these diffusion barriers showed that these barriers sustained the interdiffusion between Cu and Ag up to 620 °C at least for 30 min in either vacuum or flowing He-0.5% H_2. This temperature is a 200 °C improvement over previously reported values for the self-encapsulated Cu and Ag films. X-ray diffraction spectra showed no formation of any high resistive intermetallic compounds, i.e., Ag_3Al, Ag_2Al, and $AlAg_3$.

D9.7
KINETICS MODEL FOR THE SELF-ENCAPSULATION OF Ag/Al BILAYERS. T.L. Alford, Y. Wang and J.W. Mayer, Department of Chemical, Bio. and Materials Engineering, NSF Center for Low Power Electronics, Arizona State University, Tempe, AZ.

A model is proposed to describe the temperature dependence of the aluminum oxynitride ($Al_xO_yN_z$) diffusion barrier formation during a silver self-encapsulation process. These barrier layers form in the temperature range of 500-725 °C during anneals of the Ag/Al bilayers on oxidized Si substrates in an ammonia ambient. Experimental results show that temperature has a significant effect on the kinetics of this process. In this investigation, the diffusion of Al atoms through the Ag layers during self-encapsulation process is modeled using an analytical solution to a modified diffusion equation. This model shows that higher anneal temperatures will minimize the retardation effect by i) reducing the chemical affinity between Al and Ag atoms, and ii) allowing more Al atoms to surmount the interfacial energy barrier between the metal layer (Ag) and the newly formed $Al_xO_yN_z$ diffusion barriers. The theoretical predictions on the amount of segregated Al atom correlate well with experimental results from Rutherford backscattering spectrometry. This model in addition confirms the self-passivating characteristics of $Al_xO_yN_z$ diffusion barriers formed by Ag/Al bilayers annealed between 500-725 °C.

D9.8
INVESTIGATION OF DIFFERENT DIFFUSION BARRIER LAYER DEPOSITION BY PULSED EXCIMER LASER ABLATION FOR Cu METALLIZATION TECHNOLOGY. M. Vedawyas, A. Kumar, P. Nagar, University of South Alabama, Dept. of Electrical & Computer Engineering Mobile, AL; M. Shamsuzzoha, University of Alabama, Dept. of Metallurgical and Material Engineering, Tuscaloosa, AL.

An inter-diffusion barrier layer is necessary to inhibit the Cu diffusion into Si, which degrades the device performance. In this work we attempt to address this issue of the barrier layers between Cu and Si(100). We have grown TiN and TaN films as diffusion layers between Cu and Si substrate, by the pulsed laser ablation technique. The structural properties have been evaluated by X-ray diffraction, which reveal the crystallinity of these films. The surface morphology of the films were investigated by atomic force microscopy (AFM). The transmission electron microscopy (TEM) studies on the inerfacial properties reveal the smooth interfaces between Si substrate and the subsequent barrier and Cu films on it. The Auger electron spectroscopy (AES) were done to understand the diffusion behavior of the films. It is shown that Cu diffusion in Si is minimized. The mechanical properties of these films were evaluated using the nano-indentation technique. The electrical properties of Cu with TiN and TaN as barrier layer are studied by the four probe electrical conductivity technique. The studies reveal the enhancement in the electrical behavior of Cu because of the presence of the barrier layers. The details are discussed in the paper.

D9.9
DIFFUSION BARRIER PROPERTIES OF ZrN BETWEEN SILICON AND Cu COPPER. Jwayeon Kim, Byung-Chul Cho, Dept of Materials; Euijung Yun, Dept of Control Engineering, Hoseo Univ, Asan, Chungnam, KOREA.

We have studied sputter-deposited ZrN thin film as a diffusion barrier between Cu film and Si substrate. ZrN and Cu films were grown by DC and sputter-deposited systems, respectively. The resistivities of ZrN film are on the order of 100-150 $\mu\ \Omega$ -cm. And ZrN film has a good diffusion property between Cu and Si compared with that of TiN film. The effectiveness of ZrN film as a diffusion was expored using sheet resistance mesurement, auger electron spectroscopy,

transmission electron microscopy and X-ray diffractometry technologies.

D9.10
CRYSTAL GROWTH STUDIES OF METALLIC SEEDING FOR ELECTROLESS PLATED Cu ON THE Ta-INSULATED SiO_2 FILM BY PIII. J.H. Lin, National Tsing Hua University, Dept of Materials Science and Engineering, Hsinchu, TAIWAN; T.L. Li, National Chiao Tung University, Dept of Materials and Engineering, Hsinchu, TAIWAN; Y.Y. Tsai, X.W. Liu, J.W. Hsue, H.C. Shih, National Tsing Hua University, Hsinchu, TAIWAN.

Selective copper plating was carried out using Pd and Cu as metallic catalysts by plasma immersion ion implantation (PIII) on which Cu was electroless plated. The metallic catalysts was sputtered from a negatively biased target and ionized in an argon inductively coupled plasma (ICP). The metal ions were adequately implanted into the substrate with a highly pulsed negative bias (~6 kV). The substrate has a layer of previously coated Ta on SiO_2 as a diffusion barrier by the sputtering deposition before PIII (~0.2 μm). The implantation doses of the specimens were analyzed by SIMS and RBS measurements. The crystallographic texture of the electroless plated copper on the sample was analyzed by X-ray diffraction pole figure. TEM, AFM and SEM were used to elucidate the growth mechanism of the copper film on Pd-seeded layer and on Cu-seeded layer by PIII. A high deposition rate and improved adhesion strength were achieved when copper film on the PIII seeded specimens was deposited by electroless plating.

D9.11
THE INTEGRATION OF LOW-k DIELECTRIC MATERIAL HYDROGEN SILSESQUIOXANE (HSQ) WITH NITRIDE THIN FILMS AS BARRIERS. Yuxiao Zeng, Linghui Chen, T.L. Alford, Center for Low Power Electronics, Dept of Chemical, Bio, and Materials Engineering, Arizona State Univeristy, Tempe, AZ.

HSQ is one of the promising low-k dielectric materials used in VLSI technology as an intra-metal dielectric to reduce capacitance-related issues. Like any other dielectric materials, the integration of HSQ in multilevel interconnect schemes has been of considerable technical importance. In this study, the compatibility of HSQ with different nitride barrier layers, such as PVD and CVD TiN, PVD TaN, and CVD W_2N, has been investigated by the use of sheet-resistance measurement, x-ray diffraction, transmission electron microscopy, Rutherford backscattering spectrometry, elastic resonance scattering, and forward recoil spectrometry. The refractory metal barriers, Ti and Ta, are also included for a comparison. The degradation of HSQ films indicates a strong underlying barrier layer dependence. With CVD nitrides or refractory metals as barrier, HSQ exhibits a better structural and property stability than that with PVD nitrides. In addition, the structure and property of the barrier layers have undergone significant changes due to the interaction between HSQ and these barriers. The possible mechanisms have been discussed to account for these observations.

D9.12
CHEMICAL VAPOR DEPOSITION OF TUNGSTEN NITRIDE DIFFUSION BARRIERS. Roy G. Gordon, Sean T. Barry, Randy Broomhall-Dillard, Harvard University, Cambridge, MA.

Tungsten nitride, WN_x, is a potentially important material for barriers to diffusion of copper in integrated microcircuits. A novel process will be presented for the chemical vapor deposition (CVD) of WN_x. The synthesis of the liquid precursor will be described, along with its physical properties, including its viscosity, solubility, vapor pressure, molecular weight and spectra, as well as its chemical reactivity. Temperature and pressure conditions for the CVD process will be given, along with the resulting film composition, growth rate, electrical conductivity, step coverage and effectiveness as a barrier to diffusion of copper.

D9.13
A COMPARATIVE STUDY OF Ti/LOW-k HSQ (HYDROGEN SILSESQUIOXANE) AND Ti/TEOS (TETRAETHYLORTHO-SILICATE) STRUCTURES AT ELEVATED TEMPERATURES. T.L. Alford, Yuxiao Zeng, Center for Low Power Electronics, Dept of Chemical, Bio, and Materials Engineering, Arizona State Univeristy, Tempe, AZ.

For the benefit of reducing capacitance in multilevel interconnect technology, low-k dielectric HSQ (hydrogen silsesquioxane) has been used as a gapfill material in Al-metallization-based non-etchback embedded scheme. The vias are consequently fabricated through the HSQ layer followed by W plug deposition. In order to reduce the extent of via poisoning and achieve good W/Al contact, thin Ti/TiN stack films are typically deposited before via plug deposition. In this case, HSQ makes direct contact with the Ti layer. The reliability of the Ti/HSQ structures at elevated temperatures has been systematically studied in this work by using a variety of techniques, including four-point-probe sheet resistance measurement, x-ray diffraction, Rutherford backscattering spectrometry, elastic resonance scattering, forward recoil spectrometry, secondary ion mass spectrometry, and thermal desorption spectroscopy. These results are also compared with those from Ti/TEOS (Tetraethylorthosilicate) structure, where TEOS is a conventional intra-metal dielectric. When the temperature is below 550°C, a significant number of oxygen atoms are observed to diffuse into the titanium layer. The primary source of oxygen is believed to come from the HSQ film. When the temperature is above 550°C, HSQ starts to react with Ti. At 700°C, a $TiO/Ti_5Si_3/HSQ$ stack structure forms. The Ti/HSQ system exhibits a higher reactivity than that of the Ti/TEOS system. The significance of these results has been discussed in terms of the practical applications.

D9.14
HIGH DENSITY PLASMA SILICON CARBIDE AS A BARRIER FILM FOR COPPER DAMASCENE INTERCONNECTS. Hichem M'saad, Seon-Mee Cho, Manoj Vellaikal, Zhuang Li, Dielectric Deposition Division, Applied Materials Inc., Santa Clara, CA.

A low k dielectric barrier/etch stop has been developed for use in copper damascene application. The film is deposited using methane, silane and argon as precursors in a HDP-CVD reactor. The film has a dielectric constant of 4.2 which is lower than the dielectric constant of conventional SiC or plasma silicon nitride (>7). Film characterization including physical, electrical, adhesion to ILD films, etch selectivity, and copper diffusion barrier properties show that this film is a better barrier than silicon nitride for low k copper damascene interconnects. As the CH_4/SiH_4 gas flow ratio increases, the refractive index of the film decreases and saturates at a value of 1.7 (Fig. 1). This trend indicates that film composition does not change appreciably above a CH_4/SiH_4 ratio of six. The dielectric constant for the HDP-SiC film is tunable and can be much lower than that of conventional SiC films (k>7). Since the refractive index (n) is a measurement of the dielectric constant at the optical frequency, the measured dielectric constant at 1 MHz increases with increasing n. Figures 1 and 2 show that low k values can be obtained at high CH_4/SiH_4 ratios. This process regime corresponds to a carbon-rich SiC film. Therefore, it is the substitution of silicon with carbon, which has a lower electronic polarizability than Si, that results in a lower overall dielectric constant. We have determined that as the HDP-SiC film becomes carbon-rich, the leakage current density decreases, and the barrier properties to copper diffusion improves. From SIMS profiles, HDP-SiC barrier to Cu is better than for PE or HDP SiN (Fig. 3). Carbon-rich HDP-SiC contains considerably more $Si\text{-}CH_3$ and $Si(CH_2)_n$ bonds (Fig. 4). In summary, we have developed an HDP-CVD based SiC film as a barrier/etch stop in Cu damascene applications. This film consists of a refractive index in the range of 1.70 to 1.90, a dielectric constant of 4.0-4.5, a compressive stress of 150-200 MPa, and a leakage current of $3.0\text{x}10^{-10}$ A/cm^2 at 1 MV/cm. When integrated in-situ with HDP-FSG, an effective dielectric constant of 3.5 can be achieved (Fig. 5).

D9.15
PHOTOACOUSTIC INTERFEROMETRY FOR METAL FILM MEASUREMENT. Mehrdad Nikoonahad, Haiming Wang, Shing Lee, Film and Surface Technology Division, KLA-Tencor Corporation, San Jose, CA.

We describe a novel photoacoustic technique which is based on common- path interferometry for metal film thickness measurement in IC processing. Pulses 60 to 100 fs wide, from a Ti-sapphire laser at 800 nm, are focused to a 5-micron spot on the surface, generating picosecond acoustic pulses in the sample through the thermoelastic effect. Echoes from film interfaces, upon arrival at the surface, lead to a surface displacement of the order of 0.1 Å. This displacement alters the optical path length and hence the phase of a probe beam. The acoustic pulse at the surface also changes the reflection coefficient leading to an additional phase change in the probe beam. We have developed a common path interferometer, which measures the phase change at the surface as induced by the echoes. A reference pulse is applied to the surface immediately before the pump, and after reflection from the wafer, is delayed by approximately 1 ns. After the pump pulse, the probe pulse of the interferometer is applied and it is the interference of the reference and the probe pulses which results in the output signal. Given that the interferometer is common-path and the temporal separation between the pump and probe is short, we can achieve extremely high sensitivities and detect phase changes of the order of a few parts in 10^4 radians in a 10 Hz bandwidth. Results obtained from film stacks used in aluminum and copper metalization technologies are presented. It is shown that the technique has extremely good sensitivity for tungsten and aluminum but does have limitations for copper and its associated barrier layer. Fundamental physical limitations for copper metrology are discussed. Furthermore, it is shown that while a second harmonic pump would marginally help

thermoacoustic generation, it does not radically enhance measurement capability for copper and its barrier layer.

D9.16
EVOLUTION OF SURFACE MORPHOLOGY DURING Cu(TMVS)(HFAC) SOURCED COPPER CVD. Daewon Yang, Jongwon Hong and Timothy S. Cale, Rensselaer Polytechnic Institute, Chemical Engineering Department, Troy, NY.

Even though chemical vapor deposition (CVD) of Cu has been studied for the last several years, many important physical processes associated with CVD Cu film growth are still not well understood. Many properties of thin films are directly controlled by surface morphology, which in turn is largely determined by the initial stages of deposition.
Our study describes effects of changes in process variables on evolving surface morphology during Cu(TMVS)(hfac) sourced Cu CVD on TaN substrates using an LPCVD system. The effects of water vapor as a co-reactant are also studied in terms of surface morphology. We present surface morphology variations for each process variable with RMS roughness, grain size, short-rage roughness, and normalized roughness (RMS roughness divided by film thickness). Surface roughness increases quickly at deposition temperatures above 473 K. Within the ranges of conditions studied, the lowest normalized roughnesses are achieved at 473 K substrate temperature.
In an effort to improve surface morphology by enhancing the nucleation stage of deposition, water vapor is introduced during deposition. High nuclei density with uniform size can be achieved by introducing water vapor. Depositions with water vapor during the initial stage result in lower roughnesses, larger grain sizes, and lower short-range roughnesses as compared to depositions without water vapor. From this study, we conclude that water vapor enhances Cu nucleation and that a relatively small amount of water vapor before or during the initial stage of deposition improves surface morphology in terms of roughness and grain size.

D9.17
STUDIES OF Cu SURFACES MODIFIED BY THERMAL AND PLASMA TREATMENTS. Gerald P. Beyer, Michail Baklanov, Thierry Conard, Karen Maex, IMEC, Leuven, BELGIUM.

The purpose of this experiment was to study the effect of either a heat treatment or hydrogen plasma or a combination of both on the surface of Cu films. The chemical state of the Cu surface is of interest as it may influence the adhesion of dielectric diffusion layers to Cu or the electromigration of Cu in damascene structures. Prior to the treatment Cu films had been deposited by sputtering and stored in the clean room for several weeks. It was found that the main desorption products due to the two minute thermal treatment at 350°C were oxygen, water, carbon monoxide, and carbon dioxide as determined with a mass spectrometer. The desorption occurred in two steps, which is interpreted as being due to the desorption of first loosely bonded species on the surface of Cu followed by the desorption of chemisorbed species. When the Cu surface was first exposed to a hydrogen plasma and then thermally treated no desorption products were found during the second treatment. This shows that the plasma also removes the adsorbents. From photoelectron spectroscopy studies it was found that the Cu surface contains both ionised and neutral electronic states. After either treatment only the neutral state of Cu is present. The surface concentration of Cu increases whereas the concentration of O decreases. The desorption and spectroscopy results point to a chemical state of the Cu surface which is most likely a mixture of Cu hydroxides and carbonates. As demonstrated those compounds can efficiently be removed by both treatments. Ellipsometric studies before and after the various treatments confirm that the cleanness of the Cu surface improves due to the thermal and the plasma treatment. The results also indicate that the surface roughness of the Cu increases for the latter treatment, but remains unchanged for the former.

D9.18
STUDY OF Ta AS A DIFFUSION BARRIER IN Cu/SiO_2 STRUCTURE. J.S. Pan, Institute of Materials Research and Engineering, SINGAPORE; A.T.S. Wee, C.H.A. Huan, National University of Singapore, Dept. of Physics, SINGAPORE; J.W. Chai, Institute of Materials Research and Engineering, SINGAPORE; J.H. Zhang, Nanyang Technological University, School of Mechanical and Production Engineering, SINGAPORE.

Copper is an attractive material for ULSI metallization due to its lower resistivity and higher electromigration resistance compared to Al and its alloys. However, the implementation of Cu metallization requires the use of a barrier layer since Cu diffuses easily into Si and SiO_2, leading to an increase in device leakage. Also, Cu lacks the ability to adhere to SiO_2 and most insulating substrates. Thus thin film layers should be used between Cu and SiO_2 to improve the adhesion of Cu to the SiO_2 layer. There has been a considerable effort to identify a suitable diffusion barrier for Cu metallization. Among these barriers, Ta-based barriers have been of increasing interest because Ta does not react with Cu and the diffusion of Cu through Ta into the oxidized Si substrate does not occur up to 700°C. In the present study, Ta thin films of about 35 nm thick were investigated as a barrier material between Cu and SiO_2 using X-ray diffractometry (XRD), Auger electron spectroscopy (AES) and X-ray photoelectron spectroscopy (XPS). After annealing at 600°C for 1h in vacuum, no reacted phases such as Ta-Si or Cu-Si compounds were observed by XRD. Furthermore, no evidence of interdiffusion was found in the AES depth profiles. Therefore, the Ta diffusion barrier effectively prevented the interdiffusion of Cu and Si up to a temperature of 600°C. However, XPS depth profiling indicates that elemental Si appears at the Ta/SiO_2 interface after annealing. In-situ XPS studies show that the Ta/SiO_2 interface was stable at 500°C, but about 50% of the interfacial SiO_2 was reduced to elemental Si at 600°C. Upon cooling to room temperature, some elemental Si recombined to form SiO_2 again, leaving only 6.5% elemental Si. Ta oxide also dissociated at 600°C and recombined upon cooling. These temperature-dependent interfacial reactions are discussed in the paper.

D9.19
ORGANIC SOLUTION DEPOSITION OF COPPER SEED LAYERS ONTO BARRIER METALS. H. Gu, T.J. O'Keefe, M.J. O'Keefe, Univ. of Missouri-Rolla, Dept. of Metallurgical Engineering and Materials Research Center, Rolla, MO; K.D. Leedy, Air Force Research Laboratory, Sensors Directorate, Wright Patterson AFB, OH.

Electrochemical deposition of copper for use as the interconnect metal on integrated circuits has been extensively investigated in recent years. In order to prevent the copper from diffusing into the surrounding dielectric layers and active silicon devices, thin barrier layers such as Ti, TiN, W(N), Ta and Ta(N) are deposited by sputtering prior to copper deposition. A seed layer of copper is deposited onto the barrier layer before electrolytic copper plating. Sputter deposition of copper seed layers has been the most commonly used technique but other methods, such as electroless copper deposition, may be better able to scale with shrinking feature sizes, increased aspect ratios and larger wafer sizes. Electroless copper deposition usually requires a two step process, activation of the barrier layer surface by a Pd or Pd/Sn solution followed by electroless copper deposition. In this investigation the feasibility of an electrochemical process using a metal bearing organic solution to directly activate the metallic barrier layer for subsequent electroless and/or electrolytic copper deposition was studied. Preliminary results indicate that small, discrete particles of metal, including copper, can be directly deposited onto unpatterened metal barrier layers from organic solutions. The resulting surfaces were found to be compatible with both electroless and electroplating copper processes. A discussion of the organic solution chemistry and influence of processing parameters on copper deposition will be presented along with future applications and directions.

D9.20
STRESS, MICROSTRUCTURE AND TEMPERATURE STABILITY OF REACTIVE SPUTTER DEPOSITED W(N) THIN FILMS. Kevin D. Leedy, Air Force Research Laboratory, Sensors Directorate, Wright-Patterson AFB, OH; Matthew J. O'Keefe, University of Missouri-Rolla, Dept. of Metallurgical Engineering, Rolla, MO; John T. Grant, Research Institute, University of Dayton, Dayton, OH.

Tungsten nitride thin films possess the thermal stability that is required in high power, high temperature semiconductor device applications such as Schottky barriers on GaN or in diffusion barriers between Cu and Si. Because of the high stability of tungsten nitride films, it is important to understand the thin film properties as a function of deposition conditions and elevated temperature exposure. In this investigation, the influence of nitrogen content and post deposition annealing on the stress, microstructure and resistivity of W(N) films was analyzed. W(N) thin films were deposited by reactive dc magnetron sputtering of a W target in Ar/N_2 gas mixtures. With an increasing N_2 to Ar flow ratio, the as-deposited crystal structure of the films changed from α-W to β-W to a nano-crystalline W_2N phase. The as-deposited W(N) stress, grain size and resistivity of these films were found to be strongly dependent on the phase(s) present. Film stress was measured $in-situ$ as a function of annealing temperature up to 650°C in flowing N_2 using a laser reflectometry system. Stress mechanisms associated with metastable phase transformations occurring at elevated temperatures were identified. Microstructural characterization using transmission electron microscopy and x-ray diffraction and chemical analysis by x-ray photoelectron spectroscopy and Auger electron spectroscopy of the W(N) films were used to identify the as-deposited and transformed phases.

SESSION D10/G7: JOINT SESSION:
GRAIN EVOLUTION OF METALS
Thursday Morning, April 27, 2000
Golden Gate B2 (Marriott)

8:30 AM *D10.1/G7.1
TEXTURE, MICROSTRUCTURE, AND ROOM TEMPERATURE RECRYSTALLIZATION IN ELECTROPLATED COPPER FOR ADVANCED INTERCONNECTS. M.E. Gross, Bell Labs, Lucent Technologies, Murray Hill, NJ.

Cu is rapidly being adopted as the primary metallization for interconnects in extreme large scale interconnect (XLSI) devices. The interfaces, microstructure, and texture of the Cu all factor into producing an interconnect that is reliable at dimensions from 0.16μm at the lowest metallization level to several microns at the uppermost levels. Cu interconnects are today being fabricated by electroplating Cu into dual damascene structures consisting of trenches and vias etched in SiO_2. A thin (<1,000Å) sputtered Cu seed layer over a refractory metal-based diffusion barrier serves as the cathode for plating. The texture of the barrier layer as well as the topography of the damascene structure both influence the texture of the electroplated Cu. A new sidewall texture component was identified in damascene Cu samples.[1] Following plating, the electroplated Cu undergoes recrystallization at room temperature that advantageously produces large grains for improved electromigration resistance. This recrystallization process is likewise influenced by the damascene topography.[2] Interestingly, the recrystallization of the EP film at room temperature can also drive grain growth in sputtered Cu underlayers that can be as much as twice the thickness of the EP layer. In this talk, I will review recent results on various aspects of the texture, microstructure, and room temperature recrystallization of electroplated Cu in damascene and dual damascene architectures, with a consideration of the underlying mechanisms. [1]C. Lingk, M.E. Gross, W.L. Brown, Appl. Phys. Lett. 74, 682 (1999). [2]C. Lingk, M.E. Gross, J. Appl. Phys. 84, 5547 (1998).

9:00 AM D10.2/G7.2
MACRO- AND MICROTEXTURE OF COPPER METALLIZATION LAYERS MEASURED BY ACOM IN THE SEM. R.A. Schwarzer, A. Huot, Dept. of Physics, Technical Univ. Clausthal, GERMANY; A.H. Fischer, RM MET, Infineon Technologies GmbH, Munich, GERMANY.

Control of (crystal) texture is important for process optimization of metallization layers. Conventional pole-figure measurement by x-ray diffraction (XRD) is limited to areas larger than 0.1 mm wide. By oscillating the specimen under the stationary primary beam, a spatial average from about 1 cm^2 is obtained. A uniform area scan, however, and hence an unbiased macrotexture is not guaranteed. An additional inconsistency of x-ray pole-figure data may be caused by the variation of information depth with specimen tilt. A further draw-back is the limited availability of x-ray texture goniometers.
Automated Crystal Orientation Measurement (ACOM, EBSD) in the SEM is now widely used for studying microtexture in interconnects on a grain specific scale. Commercial EBSD systems with digital beam scan, however, are not made for scans across large specimen areas at low SEM magnifications. A mechanical stage scan (OIM), on the other hand, is too slow, although the scanned field size is only limited by the travel of the stage.
With the ACOM system named ORKID, both the position of the pattern center (which marks the reference directions) and the specimen-to-screen distance are calibrated automatically, as well as the lens focus is corrected dynamically from scan point to scan point when the beam travels across the steeply tilted surface [1]. Therefore specimen areas as large as with XRD can be scanned to acquire large populations of grains, in addition to mapping small areas at single line width resolution, without sacrificing accuracy of orientation measurement or spatial resolution. At present, speed of ACOM with digital beam scan exceeds 20,000 orientations per hour.
From the ACOM database, the ODF and pole figures have been calculated for comparison with x-ray measurements. The benefits and limitations of texture determination by ACOM will be discussed.
[1] R.A. Schwarzer: Micron 28(1997)249-265

9:15 AM D10.3/G7.3
MICROTEXTURE OF ELECTROPLATED COPPER INTERCONNECTS. R. Spolenak[1], D.L. Barr[1], M.E. Gross[1], W.L. Brown[1], A.A. Macdowell[2], N. Tamura[2], R. Celestre[2], H.A. Padmore[2], B. Valek[3], J. C. Bravman[3], P. Flinn[3], T. Marieb[4], B.W. Batterman[5] and J.R. Patel[5]. [1]Bell Labs, Lucent Technologies, Murray Hill, NJ, [2]Advanced Light Source, Lawrence Berkeley National Lab., Berkeley, CA, [3]Dept. of Materials Science and Engineering, Stanford University, Stanford, CA, [4]Intel Corporation, Portland, OR, [5]ALS/LBL, Berkeley, CA & SSRL/SLAC, Stanford University, Stanford CA.

Future generations of ULSI technology will rely heavily on micron and sub-micron Cu interconnections fabricated in damascene architecture. Damascene Cu structures are typically formed by electroplating Cu into trenches etched into SiO_2. Observations of the texture of Cu in these structures have been made non locally by broad-beam x-ray diffraction (XRD) and locally by electron back-scatter diffraction (EBSD). New texture components have been observed that originate from the sidewalls of the trenches[1]. In this work the technique of x-ray micro-diffraction (XRMD) was applied. White x-rays were focused to a micron spot size by Kirk Patrick-Baez mirrors. The sample was stepped under the micro-beam and a Laue image was obtained at each sample location utilizing a CCD area detector. In order to demonstrate the effect of sidewall on the texture, lines with widths ranging from 0.3 μm to 5 μm and depths of either 0.5 μm or 1 μm were investigated. Subsequently, the lines were examined by broad-beam XRD, focused ion beam (FIB), and EBSD. We will compare the local volume information from XRMD to average volume information from broad-beam XRD and to surface orientation information from EBSD to quantify the microstructure of damascene copper.
[1]C. Lingk, M.E. Gross, W.L. Brown, Appl. Phys. Lett. 74, 682 (1999)

9:30 AM D10.4/G7.4
THE ROLE OF ASPECT RATIO ON MICROSTRUCTURE DEVELOPMENT IN DAMASCENE PROCESSED INTERCONNECTS: MODEL PREDICTIONS AND EXPERIMENTAL RESULTS. John E. Sanchez, Jr., Juan Dominguez, Materials Science and Engineering, University of Michigan, Ann Arbor, MI.

Advanced interconnect structures consist of damascene-processed trench metallization lines in which the aspect ratio, defined as trench depth to linewidth, is significantly greater than 1. Concern for interconnect reliability requires the optimization of both line grain size and texture orientation. Given the anisotropic surface and interfacial energies of the FCC Al and Cu choices for metallization, minimum energy orientations of bamboo grains in the damascene lines are a function of aspect ratio (β) and damascene processing details. We have modeled the competition between driving forces arising from surface trench + bottom interface energy minimization and trench sidewall interface energy minimization. Energetic competitions between variously oriented bamboo grains are illustrated. Results of global energy minimization indicate that (111) out-of-plane + (110) sidewall oriented grains are preferred when the aspect ratio is less than 2, while (110) out-of-plane + (111) sidewall oriented grains are preferred when the aspect ratio is greater than 2. A preferred (100) out-of-plane + (100) sidewall texture orientation is predicted at the transition aspect ratio = 2. Grain texture evolution in high aspect ratio trenches is therefore driven by the minimization of trench sidewall interfacial energy, whereas the grain structure in within low aspect ratio lines is determined by surface and trench bottom interface energy minimization. Comparisons of this model are made to recent experimental results of crystallographic texture and grain size in damascene-processed Al and Cu interconnects. The drag effect of grain boundary grooving on bamboo boundary mobility is described. The surface groove drag places a minimum energetic driving force required for bamboo boundary motion which is dependent on damascene line aspect ratio. The groove drag therefore limits in general the competition between misoriented bamboo grains. However the global minimum energy grain orientations, (111) out-of-plane + (110) sidewall at low aspect ratio and (110) out-of-plane + (111) sidewall at high aspect ratio, are maintained. The effects of groove drag and damascene sequence processing options on damascene microstructure development are described.

10:15 AM D10.5/G7.5
CHARACTERIZATION OF THE MICROSTRUCTURE OF Cu-Al ALLOY/SiO_2 INTERFACES. Pei-I Wang, S.P. Murarka, G.-R. Yang, E. Barnat and T.-M. Lu, Center for Integrated Electronics, Electronics Manufacturing and Electronic Media, Rensselaer Polytechnic Institute, Troy, NY.

Low resistivity (< 6 $\mu\Omega$-cm)Cu-Al alloys have been recommended for application as the diffusion barriers/adhesion promoters for advanced copper based metallization schemes. This approach to barrier formation is to generate an ultra-thin interfacial layer through Cu alloying without significantly affecting the resistivity of Cu. In this paper the microstructure of the bilayers of Cu/Cu-5at.%Al and vice versa sputter deposited on SiO_2 before and after thermal annealing is investigated by x-ray diffraction (XRD) and transmission electron microscopy (TEM). The x-ray diffraction spectra of Cu-5at.%Al on SiO_2 show that the addition of Al into Cu tends to favor the Cu (111) texture. The Al peak appears on x-ray diffraction spectra after annealing indicates that Al segregates at the interface to promote the interfacial reaction of Cu-Al alloy/SiO_2 interface. These results and TEM microstructure data will be presented and discussed, and will show that films of Cu doped with Al appear to act as a suitable barrier and adhesion promoter between SiO_2 and Cu.

10:30 AM D10.6/G7.6
EARLY STAGES OF SURFACE AND MICROSTRUCTURE DEVELOPMENT DURING GROWTH OF POLYCRYSTALLINE THIN FILMS. John E. Sanchez, Jr., Adriana E. Lita, Materials Science and Engineering, University of Michigan, Ann Arbor, MI.

Surface roughness, grain size and morphology, and crystallographic orientation are important microstructural features of deposited polycrystalline films that often determine the performance and reliability of microelectronic devices. Factors such as surface curvature, grain boundary curvature and surface and/or interfacial energy minimization may separately drive the evolution of structure, while processing and substrate material effects further complicate understanding of film evolution. We evaluate the competing effects of surface curvature minimization, grain boundary groove pinning, surface energy minimization and size-dependent normal grain growth during the early stages of deposited film growth. In addition the effects of substrate material properties such as crystallographic texture and surface energy on deposited film structure are evaluated. Surface roughness, columnar grain size and crystallographic texture were determined for sputter deposited pure Al films on SiO_2 and Al-0.5% Cu films on SiO_2 and Ti substrates using atomic force microscopy, transmission electron microscopy and x-ray pole figure analysis, respectively. Results for sputter deposited Al on SiO_2 substrates illustrate the surface roughness decrease during film growth up to 0.3 μm thickness due to the grain size increase and optimization of Al (111) texture via combined normal and secondary grain growth mechanisms. Results for Al-0.5% Cu films on SiO_2 below 0.1 μm thickness similarly show surface smoothing as the film achieves continuity and which persists as grain growth continues and as Al (111) texture evolves. Al-0.5% Cu films on Ti substrates achieve continuity at a film thickness below 10 nm, and maintain a smaller grain size than Al-Cu films on SiO_2. The development of 5 degree offset Al (111) texture on SiO_2 occurs prior to film continuity, seeding the (111) offset texture in the fully continuous film. In contrast, the 10 nm fully continuous Al films on Ti substrates are randomly oriented with exact Al (111) texture evolving due to combined normal and secondary grain growth. These results suggest that film bulk processes such as size and orientation dependent grain growth, rather than surface capillary forces, are primarily responsible for polycrystalline film surface and structure development.

10:45 AM D10.7/G7.7
OBSERVATION OF LONG-RANGE ORIENTATIONAL ORDERING IN METAL FILMS EVAPORATED AT OBLIQUE INCIDENCE ONTO GLASS. David L. Everitt, X.D. Zhu, Univ of California-Davis, Dept of Physics, Davis, CA; William J. Miller, Univ of California-Davis, Dept of Chemical Engineering, Davis, CA; Nicholas J. Abbott, Univ of Wisconsin, Dept of Chemical Engineering, Madison, WI.

We studied long-range orientational ordering in polycrystalline Au films (10 nm - 30 nm) that are evaporated at oblique incidence onto a glass substrate at room temperature. By measuring the averaged optical second-harmonic response from the films over a 6-mm diameter region, we observed a transition from the expected in-plane mirror symmetry at 10 nm to a surprising three-fold in-plane rotational symmetry at 30 nm. X-ray pole figure analysis performed on these films showed the strong $< 111 >$ fiber texture typical of fcc films, but with a restricted, three-fold symmetric, distribution of crystallite orientations about the fiber axis.

11:00 AM D10.8/G7.8
GRAIN BOUNDARY CURVATURE IN POLYCRYSTALLINE METALLIC THIN FILMS. Alexander H. King, Purdue University, School of Materials Engineering, West Lafayette, IN.

Annealed thin films are typically observed to have mean grain diameters that are approximately equal to the film thickness. The standard explanation of this sheet thickness effect is that it results from a balance of grain boundary curvature in two different directions which, in turn, results from pinning at grain boundary grooves. TEM experiments have been performed to assess this model, and it is found that the predicted curvature about axes in the film plane, is absent. Alternate explanations of the sheet thickness effect are considered. Acknowledgement: this work is supported by the National Science Foundation, grant number DMR 9530314.

11:15 AM D10.9/G7.9
PRECIPITATION IN SUB-MICRON Al(Cu) INTERCONNECTS DURING ELECTROMIGRATION. C.A. Volkert, C. Witt and E. Arzt, Max-Planck-Institut für Metallforschung, Stuttgart, GERMANY.

Studies of θ-phase precipitation during annealing and electromigration of passivated sub-micron Al(0.5wt.%Cu) interconnect segments have been performed in-situ in an SEM. On applying a sufficiently large current density, precipitates nucleated and grew at the anode ends of the segments and dissolved at the cathode ends. By reversing the direction of the current, this process could be reversed. The kinetics of nucleation, growth, and dissolution were studied at 250°C for a range of current densities, as well as in the absence of an applied current. In all cases, the behavior was well described by a model in which the motion of Cu in solution is driven by both the electromigration force and by the solute concentration gradient. A clear barrier to nucleation was observed, at a supersaturation of roughly twice the equilibrium solubility, after which precipitate growth was diffusion rate-limited. By comparing precipitate dissolution kinetics with and without an applied current, values for the effective charge and the diffusion coefficient of Cu were determined. Since the measured Cu diffusion coefficient was several orders of magnitude larger than that in the bulk lattice, and since the interconnect segments have an almost perfect bamboo structure, it is likely that Cu diffusion occurs predominately along the interfaces. The precipitates formed at different sites at the anode ends during each current cycle, suggesting that the microstructure does not determine the nucleation site. It was also observed that precipitates dissolved without leaving voids behind, indicating that the Al moved backwards to replace the Cu either due to a stress-gradients or due to coupling between the Cu and Al fluxes. The implications of these results on the understanding of precipitation, particularly in small dimensions, will be discussed. In addition, it is hoped that results of the temperature dependence will be presented and provide further insights into the dominant mechanisms.

11:30 AM D10.10/G7.10
SIMULATION OF THE $TiAl_3$ FORMATION AT INTERFACES IN INTERCONNECTS. X. Federspiel, M. Ignat, INP, Grenoble, FRANCE; C. Bergman, P. Gas, LMCT, CNRS, Marseille, FRANCE; R. Olligier, CEA, Grenoble, FRANCE; H. Fujimoto, T. Marieb, Intel Components Research, Hillsboro, OR.

It is well known that solid state reactions forming intermetalics in interconect systems, will degradate their electrical reliability and produce mechanical stresses which in certain circumstances will induce damage. For example islands of a $TiAl_3$ compound can be nucleated at the interfaces of stacks of Al and Ti thin films under the effect of heating, producing the above mentioned awkward effects. A solution to avoid these undesirable effects is to produce, prior to the definitive manufacture of a device, a controlled thin layer of the compound, which will remain stable during any further thermo-mechanical solicitation. We have analysed the kinetics of $TiAl_3$ formation, from diferent sort of Al/Ti layered systems. Some of them presented diferent Al/Ti thickness ratio, while others were obtained with intentionally induced pollutions during the films obtentions. A numerical model for $TiAl_3$ growth based on interfacial diffusion mechanisms was confronted to in-situ experiments and observations by TEM, to SIMS analysis and DSC experiments.

SESSION D11/E8: JOINT SESSION:
PROCESS INTEGRATION AND
MANUFACTURABILITY
Chair: Rajeev Bajaj
Thursday Afternoon, April 27, 2000
Golden Gate B2 (Marriott)

1:30 PM *D11.1/E8.1
CMP OF METALS. S. Kordic, H. Banvillet and R.M. Gonella, ST Microelectronics. *Philips Semiconductors, Crolles, FRANCE.

An overview is given of chemical mechanical polishing (CMP) of copper, aluminum and tungsten. Issues concerning the consumables selection, such as pads and slurries are discussed as well as their impact on process performance. Dual damascene integration and CMP issues of low-k dielectrics and Cu or Al metallization are discussed. Examples of electromigration performance of dual damascene Cu and Al are given.

2:00 PM D11.2/E8.2
TECHNIQUE OF SURFACE CONTROL WITH THE ELECTROLYZED DI WATER FOR POST CMP CLEANING. Mitsuhiko Shirakashi, Kenya Itoh, Ichiro Katakabe, Masayuki Kamezawa, Sachiko Kihara, Ebara Corporation, Precision Machinery Group, Kanagawa, JAPAN; Takayuki Saitoh, Kaoru Yamada, Ebara Reserch Ltd, Center for Technology Development, Kanagawa, JAPAN; Naoto Miyashita, Masako Kodera, Yoshitaka Matsui, Toshiba Corporation, Semiconductor Company, Kanagawa, JAPAN.

Recently, CMP is used for planalization for manufacturing of devices with multi-layer interconnects. Metal CMP processes have many subjects to look at because surface of wafer to be polished is composed of several materials - wiring material, interlayer dielectric,

etc. In general, wafers after CMP process are contaminated with particles and metallic impurities. In post metal CMP cleaning process, it is important that wafers are cleaned without damages to each materials. In this paper, we report the basic characteristic of the electrolyzed DI water, and its effect on the wafer surface when used for cleaning after metal CMP by analyzing the wafer surface with XPS and other instruments.

2:15 PM D11.3/E8.3
STUDIES ON SELECTIVITY TOWARDS BARRIER LAYER IN COPPER CMP. Cue Wei, Dnyanesh Tamboli, Vimal Desai, Sudipta Seal; Advanced Materials Processing & Analysis Center (AMPAC), University of Central Florida, Orlando, FL.

Copper CMP is used to form interconnects in multi-level device fabrication with dual-damascene architecture. Copper is typically deposited on a oxide inter-level dielectric layer with a Ta/TaN barrier layer in between. One of the critical issues in copper CMP is to minimize dishing of metal lines during CMP. Dishing of copper lines is enhanced by low CMP removal rates for tantalum compared to copper, due to widely different mechanical and electrochemical behavior of copper and tantalum. Use of a slurry, which provides similar removal rates for both copper and the barrier layer, can minimize metal dishing in CMP. In this study we will examine the factors that affect the removal rates in copper and tantalum. In this study, CMP will be carried out with both copper and tantalum under identical conditions of polishing. Ex-situ and in-situ electrochemical measurements as well as X-ray Photoelectron Spectroscopy (XPS) are used to determine the removal mechanism in CMP of copper and tantalum. Based on these fundamental studies, slurries are designed to maximize the removal rates of both copper and tantalum.

3:00 PM *D11.4/E8.4
DEVELOPMENT OF A MANUFACTURABLE MULTI-LEVEL COPPER CMP PROCESS. Rajesh Tiwari, Greg Shinn, Vincent Korthuis, Somit Joshi, Texas Instruments, Dallas, TX; and Rajeev Bajaj, Fritz Redeker, Yutao Ma, Applied Materials, Inc. - CMP Division, Santa Clara, CA.

The dual damascene approach for forming copper interconnects has enabled the simultaneous formation of sub-0.25μm vias and trenches that are etched in dielectric prior to barrier, seed and bulk Copper deposition and subsequent CMP to remove the excess material. Additivity of topography with every subsequent metallization level, poses serious challenges on CMP process capability. Intermediate dielectric planarization is necessary to eliminate topography created during Cu CMP. This additional step adds cost and negates one of the potential advantages of dual damascene processing. There exists a need for Cu CMP process that meets the low topography requirements of multi-level damascene and meets device performance requirement for interconnect metal remaining. Process performance of high and low selectivity barrier removal slurries was evaluated for multi-level damascene applications. Initial topography was generated through the tungsten CMP process step. Experimental results show that underlying W CMP related topography has a detrimental impact on the polish performance at the first Cu layer CMP step. Overpolish requirements, to accommodate the underlying topography, for the high and low selectivity processes are different. Final topography achieved with both approaches are compared. Physical and in-line electrical data from the two selectivity processes will also be discussed.

3:30 PM D11.5/E8.5
REMOVAL RATE, UNIFORMITY AND DEFECTIVITY STUDIES OF CHEMICAL MECHANICAL POLISHING OF BPSG FILMS. Benjamin A. Bonner, Boris Fishkin, Jeffrey David, Chad Garretson and Tom Osterheld, Applied Materials, CMP Division, Santa Clara, CA.

Borophosphorosilicate glass (BPSG) is currently a film of choice as pre-metal dielectric. The addition of phosphorous to silicate films may lower the migration of alkali ions, while boron addition lowers the glass transition temperature of the film allowing it to flow at lower temperatures to give better local planarity. The move toward sub-0.25 micron line width requires global planarity to achieve good depth of focus. This global planarization can be achieved by chemical mechanical polishing (CMP). The current study involved CMP of 200mm BPSG films. The dopant concentrations in the films ranged from 3.5 to 6.5 percent. Changing the concentration of boron and phosphorous had little effect on the uniformity of post-polished wafers, but had a strong effect on the CMP removal rate. In general the removal rate increased as the total concentration increased, with boron dopant concentration having a much stronger influence on the rate than phosphorous dopant concentration does. Information regarding the mechanism of the effects of dopant concentration on removal rate will be discussed. Defectivity was studied during the course of this project. Post-polish defect levels of BPSG films were lower than reference TEOS films, with few or no CMP microscratches. Analysis of the defects was performed using light scattering techniques and optical review.

3:45 PM D11.6/E8.6
POLISHING STUDIES ON MATERIALS RELATED TO SiO_2/Ti/TiN/W MULTILAYER STACKS. V.S. Chathapuram, K.B. Sundaram, V.H. Desai, D.C. Tamboli, S. Seal.

Multilayer interconnections involving tungsten will consist of SiO_2/Ti/TiN/W layers. In the CMP process of tungsten, the polishing studies of these layers are very critical. In this study a detailed investigation is conducted on the polishing rates of these four layers by using bulk high purity targets. The parameter studied in this investigation is the polishing rate as a function of the applied pressure, table speed and slurry used.

4:00 PM D11.7/E8.7
USING WAFER-SCALE PATTERNS FOR CMP ANALYSIS. Brian Lee, Terence Gan, Duane S. Boning, Dept of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, MA; Jeffrey David, Benjamin A. Bonner, Peter McKeever, Thomas H. Osterheld, Applied Materials, Santa Clara, CA.

Wafer-scale patterns [1] in CMP have previously shown promise as a tool to study CMP dependencies. A new set of wafer-scale patterns have been designed for detailed analysis and modeling of key CMP effects. The goal of this work is to explore the development of a methodology to characterize the planarization capability of a CMP process using these wafer-scale patterns; to determine a method of characterizing a pad deflection limitation that would affect the polish of particular patterns; and to explore the potential use of wafer-scale analysis to simulate the effects of nanotopography on CMP. There are two major avenues to approach for characterization of planarization performance. It is possible to determine the planarization length of the process via analysis of the trench removal for various feature sizes. Alternatively, planarization length may also be determined by analysis of the post-CMP transition region of the trench edge, after complete trench step height removal. Analysis of the deflection limitations of a particular pad can be performed by experimentation using different pads, step heights, and time splits. Post-CMP profilometry scans of the trenches will demonstrate the shape and deflection of the pad as it deforms into the trenches, and provide insight on flexing limitations of the pad. Nanotopography refers to the existing nanometer-scale surface variations that may be present on bare silicon wafers [2]. CMP of conformal films on such wafers can result in variation concerns in later stages of the process. Proper simulation of the effect of nanotopology on a post-CMP film can lead to analysis and diagnosis of potential problems. A methodology of using wafer-scale patterns for CMP analysis will be described. Implementation of wafer-scale patterns via traditional, as well as alternative means, will also be discussed. [1] Peter Burke, MRS 1996 [2] K.V. Ravi, Future Fab International, Issue 7, pp. 207.

4:15 PM D11.8/E8.8
NEW TECHNIQUES FOR IN-SITU CMP END-POINT METROLOGY. Mehrdad Nikoonahad, Shing Lee, Guoheng Zhao, Kalman Kele and Kurt Lehman, Film and Surface Technology Division, KLA-Tencor Corporation, San Jose, CA.

A new technique for in-situ end point metrology in chemical mechanical polishing (CMP) is reported. This technique is based on a recently developed self-clearing objective (SCO) in conjunction with multi-angle reflectometry at a single laser wavelength. The SCO sets up a small local jet of DI water in the vicinity of the wafer during CMP and it offers a number of advantages. Firstly the slurry and any debris in the optical path are essentially removed and hence we make the in-situ measurement through DI water. Furthermore, the SCO alleviates the need for a soft window and all problems associated with it. These advantages enable us to preserve angular resolution and hence perform multi-angle reflectometry during CMP. The wafer is illuminated at 9 separate angles simultaneously and, using the multi-angle data, we solve for the film thickness, which is report dynamically during CMP. It is, therefore, clear that end-point detection is a subset of the overall end point metrology. Without the SCO the diffuse scattering in a potential soft window material together with scattering resulted from surface scratches lead to a significant cross-talk and hence loss of angular resolution between adjacent channels. The basic design of the SCO is discussed and considerations for avoiding slurry dilution are presented. It is shown that this technology has zero impact on the CMP process. Typical results from copper and oxide (ILD and STI) CMP are presented and excellent agreement between the measurement and theoretical prediction is demonstrated. We stress that agreement between theory and experiment is essential so that data may be inverted to compute film thickness during polish. This strategy is fundamentally different

from empirical end point detection this is the present-day approach in techniques that use a single beam at single wavelength through a soft window. Finally advantages of multi-angle over multi-wavelength for data inversion are presented.

4:30 PM D11.9/E8.9

PLANARIZATION OF COPPER DAMASCENE INTERCONNECTS BY SPIN-ETCH PROCESS: A CHEMICAL APPROACH.

Shyama P. Mukherjee and Joseph A. Levert, Allied Signal Electronic Materials, Sunnyvale, CA; Donald S. DeBear, SEZ America Inc, Phoenix, AZ.

During the metallization of dual damascene structures, excess copper is electrodeposited on field areas in order to achieve a complete filling of vias and trenches. The removal of excess copper and planarization of the surface is typically achieved by chemical-mechanical polishing (CMP), where mechanical force in the form of downward pad pressures and chemical effects in the form of a dispersion of ceramic particles are utilized. In this work, we present a chemical planarization approach, Spin-Etch Planarization (SEP) to accomplish the dual tasks of planarization and excess material removal. The present approach is based on the controlled wet chemical etching and polishing of the copper layer. The chemical etching solution, having no ceramic particles is dispensed onto the wafer's surface while it is spinning. The physico-chemical nature of the etchant and processing conditions such as the spin-speed of the wafer and dispense pattern of the etchant are selected to simultaneously achieve uniform removal of copper and planarization of local recesses of the different feature sizes in the plated copper surface over the entire 200mm wafer. This process is based on controlled wet-chemical etching, which involves a higher metal dissolution-rate at surface projections, and on peak areas and a lower metal dissolution-rate at crevices or in recesses. This technique leads to a leveling of the as-deposited surface features. Once planarization of the surface topography by the uniform and selective removal of copper is achieved, a different etchant is used for the selective removal of the barrier layer(s). At this step, the exposed planarized copper features are kept passivated while the removal of barrier layer is achieved. In this work, we will present the basic concepts and process principles of SEP and the results of planarization obtained with 200 mm electroplated patterned copper wafers. We will also describe the key features of the SEZ Spin-Etch system that contributes to process performance and manufacturability.