SYMPOSIUM H

Silicon Carbide—Materials, Processing, and Devices

November 27 – 29, 2000

Chairs

Anant K. Agarwal  
Cree Research Inc  
Durham, NC 27703  
919-313-5539

James Cooper, Jr.  
School of ECE  
Purdue Univ  
1285 EE Bldg  
West Lafayette, IN 47907-1285  
765-494-3514

Erik Janzen  
Dept of Physics & Measurement Tech  
Linkoping Univ  
Linkoping, S-58183 SWEDEN  
46-13-281797

Marek Skowronski  
Dept of MS&E  
Carnegie Mellon Univ  
Pittsburgh, PA 15213  
412-268-2710

Symposium Support
	†Cree Inc.  
	II-VI, Inc.  
†MMR Technologies, Inc.  
Sterling Semiconductor, Inc.  
†2000 Fall Exhibitor

Proceedings published as Volume 640
of the Materials Research Society
Symposium Proceedings Series.

*Invited paper
9:00 AM #H1.1
SIC CRYSTAL GROWTH FROM THE VAPOR AND LIQUID PHASE. Deter Hofmann, Matthias Bickermann, Boris Epelbaum, Thomas Strumpf, Oliver Wielandt, Albrecht Winnacker, University of Erlangen-Nürnberg, Dept of Materials Science 6, Erlangen, GERMANY; Lev Kadomski, Markus Selder, Dept of Fluid Mechanics, University of Erlangen-Nürnberg, Erlangen, GERMANY.

Recent advances of SIC based innovative devices in high power/high temperature electronic and optoelectronic applications in III-Nitride optoelectronics are pushing both commercial SIC wafer suppliers and related research institutions to improve crystal quality for future industrial needs and understanding of the SIC bulk growth process, respectively. Although a considerable decrease of defect densities in 4H- and 6H-SiC wafers and increase of crystal diameter have been accomplished actually, micropipe elimination, reduction of dislocation density and stress, increase of yield and improvement of dopant non-uniformity are of permanent relevance in research and development. In this paper at first SIC crystal growth by physical vapor transport (PVT) is addressed. Characterization results of n- and p-type 4H- and 6H-SiC boules are presented with regard to crystalline defect density and distribution. Micropipes, dislocations, stress fields, parasitic polycrystals and lateral/longitudinal dopant variations. The impact of PVT process parameters is analyzed with the support of numerical modeling. The simulation tools include heat transfer, mass transfer, crystal growth processes and stress generation. The influence of thermal and constitutional fields are discussed concerning both crystalline defect formation and dopant incorporation. The status of the development of SIC liquid phase growth at our institute is introduced. Experimental results on achievable growth rates, crystal geometry and crystalline defect densities are shown. Of special interest is the evident discrepancy of micropipe propagation in SIC vapor and liquid phase growth. During PVT crystallization micropipes are propagating generally along the c-axis through the whole crystal whereas this defect can be closed during liquid phase processing. Finally experimental facts and models for the actual understanding of filamentary void formation (micropipes, tube defects) and elimination during vapor and liquid phase growth, respectively will be presented.

9:30 AM #H1.2

The development of a novel SIC crystal growth technique, generally described as High Temperature Chemical Vapor Deposition (HTCVD) is reviewed. In contrast to other optical and electrical properties of SIC wafer demonstrators are investigated with the aim of developing high frequency device quality semi-insulating SIC substrates. Carried out at temperatures above 2100°C, the HTCVD technique uses, as a C sources, SiH4 and C5H6 (silane and cyclopentadienyl) diluted in a carrier gas) as source material. The growth process can, however be described as "Gas Fed Sublimation" and is shown to proceed by the gas phase nucleation of $\text{Si}_x\text{C}_y$ clusters, followed by their sublimation into active species that are condensed on a seed crystal. 4H and 6H-SiC crystals with diameters up to 40 mm have been obtained with growth rates of 0.5 to 0.7 mm/h.

Owing to the purity of the source material used in the HTCVD technique, 4H-SiC prepared from undoped crystals (with vanadium concentration lower than $5 \times 10^{17}$ cm$^{-3}$) exhibit semi-insulating behaviour with a bulk resistivity higher than $5 \times 10^{18}$ Ω cm at room temperature. The temperature dependence of the resistivity shows that the compensation mechanism is either dominated by a single deep level (1.1 eV) or by two levels (~0.5 and 1.1 eV) in 4H-SiC. The possible origin of these levels is investigated, together with their thermal stability. The structural quality of high-resistivity wafers and the various methods controlling micropipe defects formation are investigated. Specific process steps such as in-situ seal surface preparation and micropipe closing have in particular enabled growth of semi-insulating crystals with micropipe densities lower than 30 cm$^{-2}$.

10:30 AM #H1.3

Mechanical damage of seed surfaces due to cutting, lipping and polishing has been known to result in increased dislocation densities in single crystals. The standard process for SIC epitaxy includes an in situ HCl or hydrogen etch to remove the damage. It is difficult, however, to incorporate such an etching step into the sublimation growth process. The effect of SIC seed surface preparation on dislocation densities in SIC overgrowth has been assessed by KOH etching, x-ray topography and Atomic Force Microscopy. In situ etching procedures with very low dislocation densities have been used as seeds. Growth surfaces have been prepared by either mechanical polishing with diamond paste (one um grit size), chemomechanical polishing (CMP) or colloidal silica, and so forth. After epitaxial growth an etching step was performed to remove the dislocations generated in the seed. Dislocation densities in material grown with the CMP and chemical polishing showed a significant improvement over the material grown with the diamond paste. On the other hand, dislocations in material grown with the CMP were removed. However, dislocations generated on the seed, together with those generated during growth, were not completely removed. Therefore, the surface preparation of seed material is less essential compared to the surface preparation of the seed substrate.

11:00 AM H1.5
NEW CRYSTALLINITY DESIGN FOR SINGLE CRYSTAL GROWTH BY SUBLIMATION. Shin-ichi Nakahama, Hirokata Yamaguchi, Tomohisa Kato, M. Nair Khan, Kazuo Araki, UPR, Electronic Materials Laboratory, Tokai; Antonio Pascual, Elisabeth Blanquet, Roland Maudr, Etienne Pernet, Claude Bernard, Institut National Polytechnique de Grenoble, FRANCE; Cecile Meulin, Philippe Grosse, Christian Faure, LETI-CEA Grenoble, FRANCE.

The silicon carbide SiC semiconductor material is proving today, from intense scientific and industrial development, its potential to replace and outperform silicon in several or all electronic devices for high power, high frequency and high temperature applications. The potential of this material has been known since the fifties. The main reason for its late emergence is the difficulty to grow large electronic grade 6H-SiC single crystals. The continuing improvement observed so far is mainly the result of extensive experimental work. However, different computational tools have allowed to obtain important additional information to the wide experimental knowledge. The phenomena involved in the sublimation growth process are quite complex, they include heat transfer by electromagnetic heating, radiation, conduction and convection, multicomponent species transport and gas/surface chemistry. In particular, there is a strong need of a better control of the phenomena and the heat transfer mechanisms. The first step has proved its efficiency for the optimization of the local temperature field but its does not allow the direct determination of the growth rate and shape of the growing ingot. For this purpose, heat transfer must be coupled with gas species transport. In this presentation, the different models developed so far will be first described. The standard geometry for the simulation of SiC boules and the experimental verification of the computations will be presented. Secondly, the influence of some design modifications on heat transfer will be discussed. Thirdly, tentative simulations of the relations between process parameters, crystal shape, defect appearance and crack propagation will be proposed with more or less generic computations. Experimental results of recent SiC bulk growth process development will complete the presentation and are included all along in order to verify experimentally the validity of the models.
in a growth cavity. In addition, crystal growth rate has a strongly connection with temperature distribution and its gradient in a growth cavity. It is possible to control the grown crystal shape by modifying the temperature distribution inside a growth cavity. From these points of view, new crucible design, which is a double-crucible with inner-cone form, for SiC bulk single crystal growth by sublimation was proposed, and its effect was confirmed by experiments. With this type of double-crucible, the uniformity of temperature distribution on the growing surface was so improved that a growing surface shape became flat in comparison with a case of standard crucible which grown surface was not flat. In the case of a double-crucible, temperature distribution inside a SiC source powder became more parallel to horizontal than in a case of standard crucible. These results were sublimated uniformly for time and space. It deduced that a crystal growth rate kept constant. On the other hand, in case of standard crucible, crystal growth rate changed by time because temperature distribution and its gradient changed during the growth.

11:15 AM H1.6

The studies of the last decade decade clearly has shown that sublimation of silicon carbide crystals as well as the properties of the grown material are entirely controlled by a particular temperature distribution inside the growth system. Normally, direct modeling is used to optimize the thermal field in a growth system. For this purpose, coupled heat and mass transport are simulated for chosen geometries of the growth system to be designed. In fact, such a trial-and-error approach is based mainly on tentative optimizations and rule of thumb of growth engineers. Direct modeling is, therefore, time consuming, rather expensive and likely ineffective in multi-factor optimization. In this paper we employ the inverse-problem modeling for optimization of SiC bulk crystal growth system. This approach allows one to minimize handwork in the computations, to redesign quickly the system geometry for the solution of a particular growth problem by simple modification of a target function only. Upcaling of the growth system to get the crystal of a larger diameter becomes much more easy. The results reported provide a family of the growth systems optimal in terms of prescribed temperatures in the reference points, temperature gradients in the growth cavity and SiC powder, etc. A sensitivity of optimal configurations to variation of the material properties and to choice of target function and bound constraints is analyzed. A concept of multi-factor optimization is discussed. As the optimization target not only the temperature profiles but also some other factors can be considered, for instance, absence of undesirable poly-Si deposits near the seed.

11:30 AM H1.7
6H-SiC BULK CRYSTAL GROWTH BY NOVEL SOLID PHASE EPITAXY. Motohiro M., Y. Asakura1, T. Tanaka1, T. Yotsuyanagi, A. Nagao1, S. Seno2, T. Kameko2, Nippon Pillar Packing Co., Hyogo, JAPAN; "Kwansei Gakuin University, Dept. of Physics, Hyogo, JAPAN.

Silicon carbide is a material of great technological interest for high power, high frequency and high temperature device applications. The bulk SiC crystals have been grown mainly by sublimation method. However, the improvement of the crystal quality still remains a critical issue in terms of the reduction in microcracks and the enlargement in substrate size. In this research, we propose a novel growth method which is based on solid phase epitaxy to achieve microcrack-free 6H-SiC surface on a seed substrate. The experiments were conducted in a high temperature atmospheric annealing chamber employing a simple material configuration. The materials used were a CVD-grown polycrystalline 3C-SiC(111) wafer as a source to be recrystallized and a 6H-SiC(0001) seed substrate wafer. These wafers were simply aligned in pie vertically followed by mirror-polishing and chemical treatment. By increasing the process temperature up to 2700℃, the recrystallization of 3C-SiC(111) to 6H-SiC occurred at the surface where a small temperature gradient was inserted to maintain the substrate at lower temperature. The maximum growth rate exhibited 300μm/h. The most notable phenomenon during this growth was the blue gradient light brightness in the grown layer. The growth process was characterized by means of electron microscopy as well as optical microscopy and Raman spectroscopy. We will discuss this novel growth mechanism in detail. This work was supported by the grant Advanced Technology Initiative for New Industry.

11:45 AM H1.8
INVESTIGATION OF SILICON CARBIDE GROWTH ON THE C-TERMINATED FACE OF 6H SILICON BY PHYSICAL VAPOR TRANSPORT. Detlev Schulz, Jürgen Doerkisch, Institut für Kristallzüchtung, Berlin, GERMANY.

SiC epitaxial layers and crystal wafers were grown by the modified Lely method. The C-terminated faces of 6H-SiC have been used as seeds. As-grown surfaces and axial cuts of crystals were examined by atomic force microscopy (AFM), optical microscopy (OM) as well as cathodoluminescence (CL). Studies of Schröder et al. indicated that, regardless of the seed polytype the 4H polytype had always been obtained using the C-terminated face during sublimation growth [1]. Koga et al. concluded from a detailed study that 4H crystal growth on C-terminated 6H seeds is favoured at lower temperatures, higher source-seed temperature difference and lower source pressure compared to 6H crystals [2]. Koga et al. investigated the polytype stability on both polar faces of 6H seeds by varying the temperature and the pressure. It is known that 4H crystals were only obtained on the C-terminated face at high temperatures. To shed new light on these contradictory results, polytype changes have been examined dependent on the growth conditions. There is a strong influence of the seed orientation on surface morphology. Using off-oriented substrates different step arrangements are visible for 4H to 6H, 4H to 2H transitions, however 4H to 6H transitions are nearly flat. While growing crystals on both kinds of seeds the 6H polytype is maintained under low supersaturation. Instead of obtaining 4H crystals, inclusions of 15R are occasionally observed. In contrary, 4H to the 6H to the 4H transition has been increased. Especially during initial growth stages the 4H appearance is very sensitive to the growth pressure. During the evaporation period for the growth start the 4H polytype formation is favoured at lower pressures as well. No source-seed induced polytype changes result in the deterioration of the crystalline quality. A lot of microcracks can be seen in such regions. [1] R.A. Stein, P. Lueg, S. Lehnhart, Mser. Sci. Engineer. B11 (1992) 65; [2] M. Koga, T. Yui, Fujishige, A. Miyazaki, Appl. Phys. Lett. 58 (1991) 56; [3] K. Koga, T. Yui, Fujishige, Prog. Crystal Growth Character. 23 (1991) 127-151.

SESSION H2: SiC EPITAXY

Chair: Hirohiko Matsunami and Alexandre E. Ellisson

Monday, November 27, 2000

Room 202 (Hynek)

1:30 PM H2.1

A critical issue in SiC crystal growth technology is the formation of microcracks. During epitaxial growth for device structures, microcracks propagate into the epitaxial layer, thus creating dielectric or electrical obstacles for large-area applications. We have previously shown that by using LPE on C-terminated 6H-SiC substrates, microcracks can be cured and they do not evolve in the subsequently grown sublimation epitaxy layer. In this work we study defect evolution in similar structures by including results from growth on C-terminated surfaces with the aim to find optimal conditions for buffer layers reducing the microcracks and thus giving device quality top layers. The results were analyzed using optical microscopy, SEM images, and x-ray topography in bulk reflection mode. Line patterns from large-area topographs were taken as well. The results show that nearly all (90%) of the microcracks in the substrate are terminated in the LPE layer while changes in the threading dislocation density can be clearly resolved. We have observed dislocation networks uniformly distributed over the sample, which are not seen in the top layer grown by epitaxy sublimation epitaxy. However this layer exhibits rough surface reflecting the roughness of the LPE layer, with morphological features characteristic of microropic step bunching and facet related defects. The dislocation appearance is different from that of the substrate with the buffer layer, although the etch pits dislocation density is slightly lower. We have found that most of the microcracks pointing out the growth direction and shell-like etch pits. We relate these imperfections to growth disturbances on the rough buffer layer surface. The experimental findings are discussed in respect to the optimal buffer layer thickness, and the formation mechanism of microcracks originating in the top layer. The interpretations are in agreement with the earlier suggested model for microcrack healing. A relation between the LPE layer thickness, microcrack size and healing efficiency is proposed.
1:45 PM H2.2
HOLLOW DEFECT ELIMINATION DURING SOLUTION GROWTH OF 6H SiC: C. M. Gehrke, D. Hofman, M. Miller and A. Winnacker, University of Erlangen-Nuremberg, Dept. of Materials Science 6, Erlangen, GERMANY.

SiC solution growth was shown to be a promising technique to close micropipes and macrodefects in SiC wafers prepared by the PVT technique [1]. Using the top-seeded solution growth method we investigated systematically hollow defect elimination during 6H SiC solution growth, the temperature range from 1500°C to 2100°C. High-temperature experiments at 1800-2100°C were performed under pressurized argon atmosphere (100-130 bar) in order to prevent silicon melt evaporation [2]. Effective control of supersaturation was achieved by a precise adjustment of temperature gradients in the crucible and by forced melt convection. In the report comparative analysis of two different growth approaches will be given: epitaxial (LPE) growth of thick 50-100 μm layers on PVT grown substrates containing micropipes and macrodefects [3] and growth of bulk SiC crystals using point seeds cut from hollow-defect-free Lely plates [4]. LPE experiments were accomplished on (1110) 6H wafers grown in our laboratory. Growth samples were investigated using optical microscopy, AFM and SEM. At LPE-grown layers all hollow defects existing in a substrate show an evident tendency to act as growth centers and after an adequate period of liquid phase treatment they are overgrown. Growth morphologies observed in epitaxial and the vicinity of hollow defects are rather different depending on defect type (mainly on dislocation content), substrate polarity and growth rate/supersaturation. Classification of hollow defects based on these observations will be presented, corresponding closing mechanisms will be discussed [5]. Growth platelets are in closer agreement to morphology typical for Lely-grown, [6] exhibit a more rough surface because of pronounced step-bunching. Typical defects of these crystals are flat silicon inclusions. Number of inclusions increases in size and their size are strongly dependent on forced melt convection [1].


2:00 PM H2.3
GROWTH OF MESFET STRUCTURES BY HOT-WALL CHEMICAL VAPOR DEPOSITION
Linneman, A. Henry, and E. Jarno, 2 Dept of Physics and Measurement Technology, Linköping University, Linköping, SWEDEN; 2 Solid State Electronics, Royal Institute of Technology, Stockholm, SWEDEN.

The hot-wall SiC CVD reactor was developed in our group several years ago to be able to grow thick low-doped layers with good morphology for power devices. The aim of the present study is to find out whether the use of hot-wall reactors compared to cold-wall reactors will improve the performance of high frequency devices as much as for high-voltage devices.

We will here report doping and abruptness of MESFET structures grown in hot-wall CVD reactor with a SiC-coated susceptor on both semi-insulating and n-type 4H-SiC substrates. The growth parameters have been optimised for growth of thin (≤20 nm) layers with good doping and thickness uniformity. By using relatively low growth rate (≤4 μm/h), very abrupt doping profiles have been obtained for both p- and n-type layers.

SIMS measurements have been performed of both nitrogen and aluminum concentrations in a MESFET structure with a cap layer (n-type, 0.9 μm), a channel layer (n-type, 550 nm) and a buffer layer (p-type, 1000 nm). We observe a transient behaviour of the aluminum concentration at the interface substrate/buffer (over 100 nm) which could be due to an initial reaction between TMA and oxygen in the beginning of the growth. The nitrogen interface between the channel/cap layer does not show any tendency of transient behaviour and is very abrupt.

Commercially available structures have shown concentration peaks at the interfaces of micrometer containing layers. These peaks have been up to one order of magnitude higher in doping than the layer itself. The peaks may cause an accumulation of charges that could affect the performance of the device. The structures we have grown in the hot-wall CVD reactor do not show any tendency to concentration peaks and exhibit excellent thickness profile and doping uniformity.

2:15 PM H2.4
INVESTIGATION OF LO-HILLO AND DELTA-DOPED SILICON CARBIDE STRUCTURES: A. O. Konstantinov, S. Karlsson, C. Ales and C. E. Harris, ACREO AB, Stockholm, SWEDEN.

Lo-hil-lo doping is a useful tool in semiconductor device technology. This technique is used in high efficiency MESFETs and IMPATT devices. Silicon carbide devices could potentially benefit from the use of the lo-hil-lo doping. However, thin doped layers with high precision doping control have traditionally been a problem in silicon carbide technology. Epitaxial growth was used in this work as one technique of obtaining lo-hil-lo profiles. Growth was performed in the hot-wall CVD reactor manufactured by Norsk Hydro. Doping profiles were controlled using capacitance-voltage techniques. Steep and almost exponential doping transients were obtained using nitrogen donors. A peak width of around 25 nm can be achieved. Aluminum doping profiles are somewhat more complicated, however, the peak widths achieved were comparable to that of nitrogen. An alternate way to form lo-hil-lo structures is a shallow dopant implantation with subsequent regrowth. This technique was found to result in degradation of deep portions of the epitaxial layer. The implanted nitrogen concentration was optimized for maximum nitrogen implants. Desorbed regions can be be up to 2 micron deep. Multiphase capacitance-voltage plots indicates conversion of the original implant into n-type. Investigations of the boron profiles grown has been performed. The results demonstrate that lo-hil-lo structures are easier to terminate than conventional p-n junctions. This facilitates investigation of the material imperfections responsible for early breakdown of silicon carbide devices.

2:30 PM H2.5
ELECTRONIC PROPERTIES OF NITRIGEN DELTA-DOPED SILICON CARBIDE LAYERS: Toru Kashiwada, Yasuhiro Komine, Yukishige Takashiki, Takashi Ueno, Osaka University, Osaka, Japan.

We demonstrate, for the first time, a nitrogen delta-doped silicon carbide (SiC) by chemical vapor deposition (CVD). We report on electronic properties of delta-doped SiC and propose the application for field-effect transistor (FET). Doping distributions with high peak concentrations and narrow width using sub-wavelengths for high mobility and high breakdown voltage. Delta-doping in CVD was performed by a pulse doping method using a pulse valve. The valve can open and close within very short period less than 10 μs. The nitrogen gas as p-type dopants was injected into the reactor through the pulse valve. The capacitance-voltage measurements were carried out. The doping distribution profile of the delta-doped SiC had stringly narrow width of 10 nm. The peak concentration in the high 1-1018 cm-3 range. By Halley-effect of the delta-doped SiC, the temperature dependence of a Hall mobility and a carrier concentration was investigated. The mobility enhancement was observed for the delta-doped structure over the corresponding uniformly doped SiC. The enhancement factor of 2 to 3 was obtained for the delta-doped SiC. The self-consistent calculation by the coupled sets of Poisson and Schrödinger equation suggests that the high mobility is related to the overlap of the electron wave-function of the delta-doped layer with high purity SiC layers. The high mobility attracts considerable interest in FET having the delta-doped channel. Delta-doped channel MESFET was fabricated. The SET suppresses any n+ cap layer on top of the delta-doped channel to decrease ohmic contact resistance. The recess gate was formed by etching an n+ cap layer using reactive ion etching. The device had large drain-gate break down voltage of 120 V, high drain current capability and easy control of the threshold voltage with a good pinch-off characteristics.

2:45 PM H2.6
A NEW SUBLIMATION ETCHING FOR REPRODUCIBLE GROWTH OF EPITAXIAL LAYERS OF SiC ON Si SUBSTRATES: A CVD SYSTEM Rongjuan Wang, Paul Chow and Ishwar Bhat, ECSE Department, Rensselaer Polytechnic Institute, Troy, NY.

A horizontal water-cooled cold-wall reactor for SiC epitaxial growth was recently installed at RPI. In-situ H2 etching studies and epitaxial growth of SiC on both 4H-SiC and 6H-SiC substrates have been carried out in this system. Epitaxial layers with excellent surface morphology and thickness up to 12 μm were grown reproducibly on both 4H- and 6H-SiC, 1.375 μm diameter substrates using metal-carbide-coated graphite susceptor. N-type layers are obtained using nitrogen as the dopant. The surface morphology of H Etched SiC was found to be very smooth (rms roughness less than 0.2nm over 2μm x 2μm) examined by atomic force microscopy (AFM). The films are characterized using SIMS and C-V measurements. Films with background concentration less than 1·1015 cm-3 can be obtained using this new system. Excellent layers with reproducible growth were possible due to a new susceptor cleaning method we developed, which is based on the principle of sublimination etching. This method is found to be much more effective than pure hydrogen etching. The deposition on a metal-carbide-coated graphite susceptor formed during a three-hour epitaxial growth can be completely removed in less than 30 minutes at temperatures less than 1540°C. By using this method prior to each growth run, we were able to increase the epitaxial growth reproducibility and also were able to extend the lifetime of the susceptor.

3:30 PM H2.7
CRYSTALLOGRAPHIC CHARACTERIZATION OF Si EPITAXIAL LAYERS GROWN ON POROUS Si SUBSTRATES.
The presence of microcracks and dislocations in SiC wafers used as substrates for SiC epitaxial growth may cause formation of lattice defects in the epilayers. The objective of this research was to develop a CVD growth process on porous SiC substrates in order to reduce the concentration of structural defects in SiC epilayers. We have reported on the growth and crystal quality of CVD epitaxial layers grown on porous SiC (PSC) substrates [1]. A layer of porous SiC was fabricated by surface anodization of commercial 4H and 6H SiC (SiC(0001)) substrates. 4H and 6H SiC epilayers were grown on porous SiC (PSC) substrates using atmospheric pressure CVD at 1500 °C and a Si to C ratio of 0.3. Results of X-ray diffraction, RHEED, SEM and AFM characterization demonstrated good surface quality of the films grown on porous material. PL data indicates a greatly improved defect structure in the epilayers grown on PSC as compared to control samples [1]. TEM investigation on cross-sectional specimens of the CVD epitaxial layers thus grown revealed that the presence of pores in the substrate does not lead to the formation of any micropipes in the epilayer. The investigation also failed to detect any of the usual dislocation density on the basal plane of the epitaxial layer. Based upon the results of various analytical techniques applied to the samples, we propose that the density of dislocations in the epitaxial layer is less than 5x10^4 cm^-2. It should be noted that the density of similar types of dislocations in the initial substrate obtained from the TEM was 1x10^6 cm^-2, so this preliminary result indicates that the epitaxial layers grown on PSC may have a reduction in dislocation density of more than an order of magnitude over those grown on conventional SiC substrates that are not porous. In this paper we will present characterization data from X-ray and TEM experiments performed on this material in which we have further characterized not only the epitaxial layer but the PSC/epi layer interface.


3:45 PM H2.8

We report on new developments in the study of SiC vapor-phase epitaxy on porous silicon carbide (PSC) substrates formed by electrochemical anodization of both n-type and p-type 6H-SiC. The effects of anodization conditions on the properties of the porous SiC substrate and the quality of the epitaxial growth will be discussed. Polarized micro-Raman scattering is shown to be an effective probe of the epitaxy, and indicates that the regrown films are of the 6H polytype and are of high quality [4]. The effect of anodic etching on the epitaxial SiC growth on porous 6H-SiC pertaining to isotropy, microfabrication and epitaxial lift-off are discussed.


4:00 PM H2.9
GROWTH OF SINGLE CRYSTALLINE CUBIC SiC ON Si USING POROUS Si AS A COMPLIANT SEED CRYSTAL. A. Bok, D. Purser, D. Liu, F. Vaccaro, and M.-A. Hasani, and M.R. Sardeliz Jr.*, C.C. Cameron Applied Research Center & The Department of Electrical and Computer Engineering, University of North Carolina, Charlotte, NC;*Materials Research Laboratory, University of Illinois, Urbana, IL.

Single crystalline 3C-SiC layers were grown on porous Si seeded using a single gas source, trimethylsilane. The method is environmentally friendly, utilizes a non-toxic gas, and is economical. Conversion of porous Si into SiC was also attempted using methane but the process did not lead to the formation of continuous layers. The porous Si layers were made utilizing 4H-SiC(001) wafers in a mixture of hydrofluoric acid and ethanol. The SiC was grown in a UVH system that was converted into a low pressure CVD reactor and was fitted with a reactive heating stage capable of heating the samples up to 1200°C. The formation of stoichiometric SiC was confirmed by secondary ion mass-spectrometry (SIMS) and Fourier transform infrared spectroscopy (FTIR) while the crystal structure was examined by transmission electron microscopy (TEM) and X-ray diffraction. FTIR showed a strong peak at 880 cm^-1 which corresponds to the Si-C vibrational mode. Atomic force microscopy (AFM) showed the formation of rough surfaces for thick SiC layers and flat terraces for the SiC layers. TEM selected area electron diffraction (up to 20µm on several areas on the sample) indicates the formation of fully relaxed single crystalline 3C-SiC(100) on Si(100) wafers. However, large area X-ray diffraction suggests the presence of other crystal orientations within the dominating SiC(100) layer. Heterojunction Si/SiC diodes were fabricated, which displayed a soft breakdown voltage as high as 375V.

4:15 PM H2.10
SURFACE MORPHOLOGY OF 6H-SiC ON VARIOUS A-PLANE USING Si2Cl6-C2H4-H2 BY CHEMICAL VAPOR DEPOSITION. Shinsuke Nakih, Yusuke Matsunaka, Shoichi Ushikami, and Ichiro Jacki, Department of Electronics and Information Science, Faculty of Engineering and Design, Kyoto Institute of Technology Mutsugasaki, Sakyoku, Kyoto, JAPAN.

To realize the devices, it is important to know the morphological dependence of the epilayer on various orientation of the substrates. Most of the homoeopitaxial growth is carried out on the 6H-SiC (0001) Si basal plane off cut toward <11-20> direction. Recently epilayer on a-plane (11-20) is also focused because of high channel mobility of MOSFET was achieved [1]. We already reported morphological dependence of epilayer on a-plane prepared by Si3N4-C3H6-H2 system [2]. In this presentation, we show the morphological dependence of epilayer on two different substrates such as a-plane (11-20), (1-100) using Si2Cl6-C2H4-H2 system. Crystal growth was carried out at substrate temperature of 1500°C using Si2Cl6-C2H4-H2 by atmospheric CVD. The CVD system in this study was made from a horizontal quartz tube with water cooling jacket. a-plane substrates were placed on Si coated graphite susceptor. Typical growth condition was as follows: flow rate of Si2Cl6=0.45 sccm, C2H4=0.3 sccm, H2=30 sccm, growth pressure=1000 mTorr. The growth rate varied from 5 to 15 nm/min. The growth rate was mainly limited by flow rate of Si2Cl6 and independent of flow rate of C2H4. When we choose appropriate parameter, very smooth surfaces appeared on the epilayer of (11-20) plane. Smooth surface epilayer appeared on (11-100) plane, however, a parallel fringe pattern was observed along <11-20> direction. Buffer layer effect will be presented in detail. Polytypes of the epilayer was characterized by PL and Raman spectroscopy. [1] T. Kimoto et al. Proc. ICSMCM89 [2] S. Nakih et al. in "Amorphous and Crystalline Silicon Carbide" 3rd, (1992). Springer-Verlag p. 363.

4:30 PM H2.11
MODELING OF EPITAXIAL GROWTH AND DEPOSITION CHARACTERISTICS OF SiC LAYER. Gang Zhou, Wei Ji, Christen Hallin and Peter Logfgen, ABB Corporate Research, Västers, SWEDEN.

A comprehensive chemical vapour deposition model, including gas-phase and surface chemistry coupled with reactor fluid dynamics and heat transfer, has been used to predict the growth rate and the morphology of epitaxially grown silicon carbide (SiC) in a Si-C-H(AR) system. Hydrogen and heptane slightly diluted with argon are used as carrier gases. The precursors are silane (SiH4) and propane (C3H8). A local 'etching' model, taking care of the reversible surface adsorption at its higher temperatures, is based on the interactive gas phase and surface chemistry model, which resulted in a significant improvement between predicted growth rate and experimental data. The deposition characteristic of SiC film growth has resulted using a sequential coupled local thermodynamic equilibrium model. The equilibrium calculation has been carried out at near adjacency of the surface, based on the steady-state simulation solution of heat and mass transfer coupled gas-phase and surface chemistry in a SiC chemical vapour deposition process. The simulated deposition of SiC, both growth rate and morphology, is corresponding well to our experimental measurements at relatively low temperatures. Several simulation results corresponding to different carrier gases, organic compounds, reactor geometry, and operating conditions will be reported and discussed in this presentation.

4:45 PM H2.12
GROWTH OF THICK 3C-SiC EPILAYERS IN A VERTICAL RADIANT-HEATING REACTOR. Hidetsu Tsuchida, Isako Kuma, Tomotada Jikimoto, Kunikazu Izumi, Central Research Institute of Electric Power Industry, Yokosuka Research Laboratory, Koganei, JAPAN.

We report on growth of very thick 3C-SiC epilayers in a vertical radiant-heating reactor. The reactor consists of a vertical hot-wall and an axial susceptor. We used a susceptor with a small window for input gases. In this reactor, induction current flows only in the hot-wall, so that the susceptor and substrates are heated by radiation from the hot-wall. This heating method achieves an inverse temperature gradient, as the substrate temperature is slightly higher than the susceptor temperature. The temperature gradient prevents a backside
SESSION H3: SiO₂/Si Interfaces

Chairs: Clark-Mikel G. Zetterling and Heinz Lendenmann
Tuesday, November 28, 2000
Room 202 (Hynes)

8:30 AM *H3.1 CHALLENGES AND STATE-OF-THE-ART OF OXIDES ON SiC. Leri Ljakic, Murali Das and John Palmour, Cree Research, Durham, NC.

The material characteristics of SiC make this semiconductor an outstanding choice for power devices that carry high current, control high voltages or amplify at high frequencies. In addition, devices that operate at higher temperatures are possible. However, the challenge of synthesizing a fully passivated, high-performance, low-complexity SiC device is an ongoing research project. The current consensus is that the inclusion of a channel MOSFET is controlled by interface states near the conduction band. At these interfaces, the oxide dominates the oxide, which is lower than the oxide in the conduction band. The oxide in the conduction band has been accompanied by multi-gap dielectrics and post oxidation anneals. However, the density of interface states near the band edges remain quite high. While not an ideal solution, some success has been achieved by implanting the channel to lower the doping or to create a buried channel. In addition to the high density of electrically active states, other concerns exist for device optimization and for gate insulation. Breakdown field strength, long-term reliability, and the oxide peak have been investigated and in some instances improved with some of the processing solutions implemented for reduced interface density. A general overview and history of oxides and insulators on SiC will be presented along with current trends in processing and measurement techniques.

9:00 AM *H3.2 TRAPS AT THE SiC/SiO₂ INTERFACE. Gerhard Penal, Michael Basler, Florin Chibuc, University of Erlangen-Nuremberg, Institute of Applied Physics, Germany, Walery Afanasiev, K.U. Leuven, Laboratory for Semiconductor Physics, Belgium, Hiroshi Yano, Tsunobu Kimoto, Hiroshi Vano, Department of Electronic Science and Engineering, Kyoto University, Kyoto, Japan.

The progress in the development of SiC-based devices is due to the huge improvement of the crystal quality of SiC substrates and to the favorable factor that device processing can be partially taken from the silicon technology, e.g. the formation of thin insulating SiO₂-films by thermal oxidation. In comparison with Si/SiO₂-MOS structures, the trap density at SiC/SiO₂-interfaces (D_it) is enhanced in the whole band gap by at least two orders of magnitude. This enhancement of D_it is assumed to originate from carbon precipitates at the interface, which are formed during the oxidation process. Moreover, it is experimentally demonstrated that D_it decreases as a function of the oxidation temperature in the SiC/SiO₂-MOS devices. We have obtained experimental evidence that these energetically shallow traps are caused by new interface traps located in the oxide close to the interface. Because of the higher band gap of the SiC-SiO₂ polytype, the energy position of these shallow traps are within the band gap of this polytype; they can capture free electrons and can, in addition, reduce the channel current by Coulomb scattering. In this talk, we review the progress on understanding the role of interface traps in different SiC polytypes (4H, 6H and 15R-SiC) and report on the effect of hydrogen on interface states. We further discuss the open question whether operation at temperatures above 600K leads to a degradation of 4H/6H-SiC-MOS capacitors.

9:30 AM *H3.3 BONDING, DEFECTS, AND DEFECT DYNAMICS IN THE SiC/SiO₂ SYSTEM. ST. Pantelides, R. Buczkó, G. Duscher, SJ. Pennycook, L.C. Feldman, Vanderbilt University, Nashville, TN and Oak Ridge National Laboratory, Oak Ridge, TN; M. D. Ventura, S. W. Henager, K. Chen and J. A. Wallis, Vanderbilt University, Nashville, TN; G.Y. Chang, C.C. Tin, T. Inoane-Smith, J.R. Williams, Auburn University, Auburn, AL.

Interface defects at the SiC-SiO₂ interface reduce carrier mobility and act as carrier traps, limiting the potential usefulness of SiC for power devices. This talk will report comprehensive first-principles atomic-scale calculations, atomic-resolution Z-contrast TEM images and energy-loss spectroscopy that provide microscopic understanding of the SiC/SiO₂ system and account for the observed passivation of interface defects by N. The atomic-scale processes that underlie the oxidation of SiC and possible interface defect structures, including C clusters, are identified. The results elucidate the mechanisms by which C is removed as CO. C clusters can be passivated by both H and Na, on defects, and Na can be trapped in the oxide in the form of defect complexes and can subsequently be dissolved. Investigations of the global bonding of the SiC-SiO₂ suggest that a mixed-phase transition layer is required at the interface. Atomic-resolution Z-contrast images show an abrupt termination of crystalline SiC, but EELS reveals a mixed-phase transition region that contains C and is quite extended. The work was supported in part by a joint grant from DARPA and EPRI.

10:00 AM *H3.4 EPITAXIAL GROWTH OF SiC NON-TYPICAL ORIENTATION AND MOS INTERFACES. Hisayuki Shimizu, Tsunobu Kimoto, Hiroshi Vano, Department of Electronic Science and Engineering, Kyoto University, Kyoto, Japan.

Epitaxial growth of 4H and 6H-SiC on [0001] Si planes with off-angle has been extensively carried out on Si substrates. Breakdowns of this plane, however, include micropipe penetration from substrates and possible inclinations. On SiC growth on SiC substrates, perpendicular to [0001] planes, has advantages of perfect epitaxy (for polycrystalline materials) and possible absence of micropipes. The authors have succeeded to grow high-quality homoepitaxial layers on SiC (110) planes and investigated device fabrication systematically. In this paper, details of epitaxial growth and impurity doping are described. The physical properties of epitaxial layers and MOS (metal-oxide-semiconductor) interfaces on both [1120] and [0001] Si planes are elucidated. The growth rate of SiC and impurity doping are described. The growth rates of epitaxial layers and MOS (metal-oxide-semiconductor) interfaces on both [1120] and [0001] Si planes are elucidated. Epitaxial growth was carried out using atmospheric-pressure CVD in a SiH₄+C₂H₆+H₂ system at around 1500-1600°C. The growth rate was similar to that on Si substrates. Surface morphology examined by optical microscopy and an AFM profiler is described together with crystal quality analyzed by X-ray diffraction. Doping characteristics and Schottky-barrier performances are discussed based on electrical measurements. The most striking results on the performance of MOS interfaces are focused on in the presentation. N-channel MOS field effect transistors were fabricated on polytype epilayers grown on (1120) and (0001) Si planes of different substrate orientations. A similar approach was performed to fabricate MOS interfaces with an oxide thickness of 400nm on both planes. Dramatic increase of inversion channel mobility (from 3.5x10⁴ cm²/Vs to 9.5x10⁴ cm²/Vs for [1120] Si planes) is explained together with the temperature dependence of inversion channel mobility and threshold voltage. The results for the [1120] Si planes were confirmed (in detail) using simulation techniques.

11:00 AM *H3.5 NITRIDE PASSIVATION OF INTERFACES NEAR THE CONDUCTION BAND IN SiC ON CARBIDE. G.Y. Chang, C.C. Tin, T. Inoane-Smith and J.R. Williams, Physics Department, Auburn University, Auburn, AL; K. McDonald, M. Di Vincenzo, S.T. Pantelides and L.C. Feldman, Department of Physics and Astronomy, Vanderbilt University, Nashville, TN [Also at Oak Ridge National Laboratory, Oak Ridge, TN]; L.A. Weller, Department of Electrical Engineering and Computer Science, Vanderbilt University, Nashville, TN; O.W. Holland, Solid State Division, Oak Ridge National Laboratory, Oak Ridge, TN.

Two significant problems appear to hinder the development of silicon carbide inversion metal-oxide-semiconductor field effect transistors: (1) epitaxial surface roughness introduced due to oxidation by high temperatures and (2) large, broad density of interface sites. The two significant problems appear to hinder the development of silicon carbide inversion metal-oxide-semiconductor field effect transistors: (1) epitaxial surface roughness introduced due to oxidation by high temperatures and (2) large, broad density of interface sites.
states that exist at about 2.9 eV above the valence band edge in all the hexagonal polytypes. These problems adversely affect the silicon dioxide/silicon interface and limit the device characteristics that can be achieved for inversion mode devices. Our paper is concerned with the second of these problems. The interface density near the conduction band is much higher for 4H silicon carbide compared to 6H and this situation is now considered a primary reason for the lower channel mobilities that are reported for 4H devices. These interface states have been observed and characterized in several laboratories since they were first described by Schomer et al. [1].

Interface act as the conduction band in n-SiC under the assumption that p-type material has a similar distribution of states. Over the past year, much attention has been focused on finding ways to improve these state densities and passivate. We will describe a nitrogen-based passivation process that is performed using post-oxidation, high temperature anneals in either nitric oxide or ammonia [2]. This process reduces the interface state density near the conduction band in SiC/SiC by almost one order of magnitude, from $10^{13}$ to approximately $2 \times 10^{12} \text{cm}^{-2} \cdot \text{eV}^{-1}$. Initial measurements for passivated n-channel mode devices have yielded channel mobilities of approximately 50 cm$^2$/V·s. This result represents a significant improvement compared to the single digit mobilities often reported for 4H inversion mode devices. We believe that it may be possible to achieve 4H channel mobilities in the range of 75 to 100 cm$^2$/V·s using an optimized passivation process together with improved implantation/patterning techniques that minimize epitaxial surface roughness. [1] R. Schomer, P. Friedrichs, D. Peters and D. Stephani, IEEE Electron Device Lett. 20 (1999) 241. [2] Y.G. Chung, C.C. Tin, J.R. Williams, K. McDonnell, M. DiVentra, S.T. Pantelides, L.C. Feldman and R.A. Weller, Appl. Phys. Lett. 76(13) (2000) 1713.

11:00 AM H3.6
NITROGEN INCORPORATION IN SiO$_2$/4H-SiC BY NO AND NH$_3$

Although 4H-SiC has a higher electron mobility than other polytypes, metal-oxide-semiconductor (MOS) devices made from 4H-SiC exhibit a large density of interface trap states ($D_{it}$) near the conduction band which reduce channel mobility. Recently, using in situ 4H-SiC MOS capacitors in NO or NH$_3$ annealing has been described to substantially reduce $D_{it}$ near the conduction band, promising higher mobility. Using nuclear reaction analysis (NRA), Rutherford backscattering spectrometry (RBS), and secondary ion mass spectrometry (SIMS), we have made a quantitative determination of the nitrogen profile in SiO$_2$/4H-SiC incorporated by NO and NH$_3$ annealing. We also shall show the relationship between $D_{it}$ and nitrogen content. Although the $D_{it}$ results are similar for both NO and NH$_3$, the location and amount of nitrogen for similar anneal conditions are completely different.


11:45 AM H3.7
PROFILING OF THE SiO$_2$ - Si INTERFACE USING X-RAY PHOTOELECTRON SPECTROSCOPY. R.N. Ghosh, S. Ethibhavan, and B. Golging, Center for Sensor Mterlink, Michigan State University, East Lansing, MI; M.I. Mikkopuloyri, N. Minakov and P. Joshi, Mechanical & Nuclear Eng, Wright State University, Dayton, OH; M.K. Das, Cree Research Inc., Durham, NC; J.A. Cooper, Jr., School of Electrical & Computer Engineering, Purdue University, Lafayette, IN.

Recent advances in silicon carbide device technology have enabled the implementation of SiC based sensors and electronics for operation in harsh, high temperature environments. Understanding the properties of the SiO$_2$ - Si interface is crucial for effective device design, if x-ray photoelectron spectroscopy (XPS) we have studied both the abruptness of the interface as indicated by sub-oxide species and the possible presence of carbon at the interface in the form of oxycarbides or even discrete clusters. Samples consist of device-quality thermally grown 500 nm oxides on both 4H and 6H SiC substrates with electrically measured interface state densities near mid gap and fixed oxide charge densities below $1 \times 10^{11} \text{eV/cm}^2$ and $1 \times 10^{12} \text{eV/cm}^2$ respectively. A very shallow wedge (< 0.05 nm) was mechanically polished to expose the oxide-SiC interface. An AXIS Ultra scanning XPS system was used to obtain Cls, O1s and Si2p photoelectron spectra of the samples and the centers. The Si2p signal showed distinct chemical shifts in the SiC and SiO$_2$ regions. An oxide species, possibly a thin native oxide, was observed on the nominally bare SiC surface and some C was present as an impurity on the oxide surface. We also obtained spatially resolved photoelectron images of the samples which show microscopic changes in the wedge region in terms of variations in composition and chemical state as a function of distance from the interface. Comparison of XPS images of samples with different electrically active defect densities should yield information on the micromechanical origin of the interface mobility reduction in the SiO$_2$ - Si system.

SESSION H4: SIC DEVICES
Chairs: Amrit K. Agarwal and James A. Cooper, Jr.
Tuesday Afternoon, November 28, 2000
Room 202 (Hyenas)

1:30 PM H4.1
PERFORMANCE AND RELIABILITY OF HIGH POWER 4.5 kV DIODES. Heinz Lendenmann, Per-Ake Nilsson, Fanny Dalsgard, J. Peder Bergman, ABB Corporate Research, Vasteras, SWEDEN.

SiC devices with 10-fold breakdown strength compared to Si are expected to improve power electronic systems such as inverter transmission. Good basic device properties such as forward voltage (3.4V), low leakage currents (1e-6Acm$^{-2}$) and high current switching (400A, 1250V) for large area (4 inch$^2$ and 4 inch$^4$) PIN diodes for the 2.5 kV range as well as for theoretical performance for Imm$^2$.

2.1-2.8A, 4H diodes are reported. Moreover, the PIN diodes were successfully scaled to 4kV blocking voltage. These diodes with implanted layers were fabricated on 4H SiC wafers, with low 1e-6Acm$^{-2}$ n-type doped hot-wall CVD Epi layers of 30 - 50um thickness. For voltage termination an implanted JTE with an oxide surface passivation layer is used. Blocking reliability testing (1000h) at high-temperature (250°C), showed stable leakage currents in the range of 10$^{-5}$ to 10$^{-1}$ A/cm$^2$. However, constant current operation revealed a new drift phenomenon of the forward voltage drop in bipolar diodes. Drifting diodes may increase in $V_F$ from ~1 mV to several 100mV (or more under severe conditions). Diodes with a drift (hours-days), exhibit with slow- and non-drifting (3-4 hours). The increase in forward voltage is accompanied by a reduction in the electrical minority carrier lifetime and by regions with reduced photoluminescence. These areas are also related to changes in the crystal material. It was found, that the substrate material as well as process uniformity can make marked differences in the occurrence of this phenomenon. In contrast to bipolar PIN diodes, the unipolar JBS type diodes do not exhibit this phenomenon. In the summary we propose our imperfections are justified by a detailed analysis of minor and major non-ideal device properties. Most device non-idealities (forward and reverse) can be explained in terms of the total substrate quality causing Epi defects.

2:00 PM H4.2
SILICON CARBIDE BIPOLAR POWER DIODES - POTENTIALS AND LIMITS. Rambir Singh, John W. Palmour, Cree Inc., Durham, NC.

To exploit the tremendous advantages offered by SiC for bipolar power devices, it is important to understand the relevant current carrier fundamental limits and their technological realization. It is essential to develop this technology commercially. The operation of a device at a high current density ($>300 \text{ A/cm}^2$) to increase total current with reasonable yield, the poor reliability of MOS at high temperatures, and the relatively low channel mobilities obtained in 4H SiC MOSFETs may make certain bipolar devices more attractive even as low as 1700 V. Depending on the operating conditions, the maximum on-state current capability, at any one of the three factors: (a) the heat dissipation limit of the package (commercial packages limit the continuous current density to about 400 A/cm$^2$ at $V_F=15 \text{V}$; (b) the contact resistance of anode or cathode, especially if one of these contacts is p-type; and (c) the heat dissipation limit of SiC, rising only in very high pulsed current ($>10^8 \text{ A/cm}^2$) applications. Bipolar devices made with SiC offer 20-50X lower switching losses as compared to conventional semiconductors. Another very significant property of SiC bipolar devices is their lower differential on-state voltage drop than similarly rated Si bipolar device, even with an order of magnitude smaller carrier lifetimes in the drift region.

This property allows high voltage ($>20 \text{kV}$) to be far more reliable and thermally stable as compared to those made with Silicon. The switching losses and the temperature stability of bipolar power devices depends on the physics of operation of the device. The two major categories of bipolar power devices are: (a) single injecting junction devices (for example BiJFET and IGBT); and (b) double injecting junction devices (like Thyristor-based GTO/MTJ/ICT/ FCT and PIN diodes). Detailed analysis of these devices will be presented at the conference. Detailed measurements on devices with record breaking voltage and current ratings will be presented at the conference. These include 4H-SiC 6.6 kV PIN diodes, 605 V/1 A buried gate FCT and >1.2 kA p-channel IGBTs.

2:30 PM H4.3
MICRO-MACHINING TECHNIQUES FOR 3C-SiC MEMS.
SIC is well known for its excellent mechanical, electrical, and chemical properties, making it a leading material for microfabricated sensors and actuators designed for environments too harsh for Si-based devices. However, the very properties that make SIC attractive for harsh environments, make it a challenging material to micromachine. Bulk micromachining of SIC is particularly difficult, since anisotropic wet-etch processes have not been demonstrated and deep reactive ion etching is still in its infancy. In the area of surface micromachining, recent advances in SIC deposition and patterning techniques have led to the development of processes that yield both single and two-layer devices. A fabrication process for a fiberoptic power detector is described that uses a novel, microlithography-based bulk and surface micromachining process for SIC MEMS devices. SIC bulk micromachining, SIC deposition, mechanical polishing, and Si wet chemical etching are used to fabricate free-standing polycrystalline SiC (poly-SiC) components from Si molds fabricated by deep reactive ion etching. A similar concept is used for SiC surface micromachining, where polysilicon and silicon dioxide thin films are deposited on sacrificial layers, patterned into micromolds by reactive ion etching, filled with poly-SiC, planarized by mechanical polishing, and eventually dissolved and released in selective wet chemical etchants. We are using the microlithography technique as the basis for a four-layer, poly-SiC surface micromachining process that we call the MUSC (MultiUser SIC) process. The extended paper will detail each micromachining process, discuss the issues related to microlithography patterning, and highlight several examples of fabricated devices.

3:30 PM H4.4
INFLUENCE OF INTERFACE STATES ON THE OUTPUT CHARACTERISTICS OF 4H-SiC MESFETs ON SI SUBSTRATES
Nabil Ghnier, Abdellkader Soufi, Jean-Marie Bluet, Gerard Guillot, Institut National des Sciences Appliquees de Lyon, Laboratoire de Physique de l’Universite, Villeurbanne, FRANCE; Olivier Nohlec, Christian B. Hjulius, THOMSON-CSF, Laboratoire Central de Recherches, Orsay, FRANCE.

The development of 4H-SiC MESFETs for power amplification in L-band requires the use of Si substrates in order to reduce parasitic losses. Unfortunately, the structural quality of Si substrates is still poor in comparison with conductive ones leading to limitation in the power densities in comparison to the expected values. Improvement in the devices performance is then strongly linked to the optimization of the buffer layer. Toward this end, a clear understanding of the impact of defects layer at the Si substrate/buffer layer interface is of great relevance. Herein, we strongly need to explore this field. In this study we discuss the correlation between “alumina behaviour” observed on DC output characteristics and trapping/detrapping phenomena. The transistors have different geometry (gate length ranging from 3.5 to 50 μm, and gate width between 200 μm and 4 mm), and were realized directly on Si substrates or using n or p-type buffers. The dV/dt characteristics have been recorded at various temperatures (300K- 600K). For each temperature the measurements have been done either by increasing or decreasing the gate bias. At 300K, a strong hysteresis effect is observed for devices without buffer. Indeed, a decrease of the drain current is obtained when the gate voltage (Vg) is swept from high to low values. This behavior can be due to negatively charged interface traps acting as a parasitic gate near the substrate. The hysteresis effect disappears progressively for increasing temperatures in agreement with a thermal ionization of the electron traps. To confirm the presence of deep traps, Random Time-Of-Flight (RTOF) measurements have been performed and show that a discrete current fluctuation is possible only for high gate voltages (i.e. when the current flows near the interface). The parasitic phenomena described above are drastically reduced when n or p-type buffer layers are used.

3:45 PM H4.5
DESIGN AND PROCESS ISSUES FOR SILICON CARBIDE POWER DIODES
S. sende-Yng, K. Agarwal and John W. Palmour, Cree, Inc., Durham, NC.

High voltage power DiMOSFETs (Duochip implanted MOSFETs) in silicon carbide (SiC) are very attractive because they have potential to match silicon IGBTs on state-of-the-art, but offer superior switching speed and higher operating temperatures. In SiC power DiMOSFETs, the peak electric field in the blocking region is designed to be 30% greater than the Si IGBTs. This means that the DiMOSFETs can be considered as high voltage, high current devices that can deliver high performance at high temperatures. The DiMOSFETs are fabricated using the Duochip technology, which allows for the implementation of a high-voltage, high-current MOSFET in a single chip. The Duochip technology is based on the use of a high-voltage, high-current MOSFET, which is fabricated using a double-layer, high-voltage, high-current MOSFET. The Duochip technology allows for the implementation of a high-performance MOSFET in a single chip, which can be used for a variety of applications. The Duochip technology is a proprietary technology that is protected by a number of patents. The Duochip technology is also a mature technology, which has been used in a number of applications. The Duochip technology is a highly reliable technology, which has been used in a number of high-reliability applications. The Duochip technology is a highly efficient technology, which has been used in a number of high-efficiency applications. The Duochip technology is also a highly cost-effective technology, which has been used in a number of low-cost applications. The Duochip technology is a highly scalable technology, which has been used in a number of highly scalable applications. The Duochip technology is also a highly modular technology, which has been used in a number of highly modular applications. The Duochip technology is a highly customizable technology, which has been used in a number of highly customizable applications. The Duochip technology is also a highly configurable technology, which has been used in a number of highly configurable applications. The Duochip technology is a highly flexible technology, which has been used in a number of highly flexible applications. The Duochip technology is also a highly versatile technology, which has been used in a number of highly versatile applications.
the minority carrier lifetime revealed a local reduction, from about 400 ns to below 200 ns, in the regions of stressed diodes, correlated to the crystalline defects observed in CL and SWIFT. This indicates that the created crystalline defects, or defects connected to these, are electrically and optically active. The electrically observed increase in forward voltage drop in these diodes can partly be related to the reduction of minority carrier lifetime.

4:30 P M H4.8
ELECTRO Luminescence FROM 4H SiC SCHOTTKY DIODES.

Electroluminescence is normally not observed from Schottky diodes, since minority carriers are not injected, but can be possible under certain conditions such as at low doping levels and with high barrier heights. Under these conditions an inversion layer is formed under the Schottky contact and minority carriers are formed close to the contact. To study the electroluminescence from Schottky diodes provides an easy and additional technique for defect characterization of epitaxial layers. In this work we report the result from spectral and time resolved electroluminescence measurement of 4H Schottky diodes in the temperature range from 2K to 300K. We compare this with corresponding measurements of photoluminescence on the same material. The diodes were n-type epitaxial wafers with a doping of law $10^{15}$ cm$^{-3}$ with Ni or Au as Schottky contacts. Electroluminescence was observed from the sample under a relatively high current density in the order of 100 A/cm$^2$. The spectrum in the band gap region was dominated by the luminescence from the nitrogen bound excitons and free exciton, where the latter dominates at higher temperatures, together with their respective phonon replicas. The donor-acceptor pair emission lines at 1.49 and 1.21 eV are also clearly seen in the spectra. In addition we also observe a broad emission with its maximum around 5200 Å. This emission is not seen in the low temperature photoluminescence of the same material, but has previously been observed in electroluminescence of p-diodes. At low temperatures we can also observe the D spectra with a higher relative intensity than in the corresponding photoluminescence measurements of the same material. The increase of the relative intensity for the DL as well as for the Al-related emissions are most likely related to the higher injection density in the case of electroluminescence compared to photoluminescence.

4:45 P M H4.9
CHARACTERIZATION OF LIGHT EMISSION FROM 4H AND 6H SiC MOSFETS.
P.J. MacFarlane, R.E. Stahlschmidt, Naval Research Laboratory, Washington, DC.

While SiC devices are an attractive alternative to Si in high power applications, interface trap densities measured in SiC MOSFETS are significantly larger than in Si ones. Here, we study SiC MOSFETS using a method to characterize the emission produced by alternately driving the channel between accumulation and inversion. Emission is due to interface state and bulk electron-hole recombination. The measurement on the channel can be done by adjusting the time the channel is cycled into inversion, $t_{	ext{inv}}$. For small $t_{	ext{inv}}$, only interface traps in the regions around the source and drain emit. Increasing $t_{	ext{inv}}$ enhances the emitting area until light is observed from under the entire gate. Due to lower mobility and higher interface state densities in 4H devices, the electron flow in 4H MOSFETS is 100 to 1000 times slower than that in 6H transistors. We will discuss a model for electron diffusion that is characterized by a travelling electron front, which progresses into the channel by first filling interface traps along a sharp boundary create by the front edge. These results provide an estimate for the interface trap density in the MOSFETS. This imaging technique is also useful for identifying extended defects such as 3C inclusions and the effects the inclusions have on the electron flow in the channel. In addition, we will report on the energy dependence of bulk and interface state emission for both 4H and 6H devices. While the energy dependence of the interface trap emission is the same in 4H and 6H MOSFETS, bulk recombination emission spectra of the two polytypes differ. Sources of the emission peaks will be discussed. We thank J.A. Cooper and M.K. Durr for providing the SiC MOSFETS. This work is supported by the ONR Power Electronics Program.

SESSION H5 POSTER SESSION
SiC MATERIALS, CHARACTERIZATION, AND DEVICES
Tuesday Evening, November 28, 2000
8:00 PM
Exhibition Hall D (Hyves)
H5.4 DELOCALIZATION CONTENT OF ETCH PITS IN HEXAGONAL SILICON CARBIDE. Igor Khelevkov, Mohsen Banianemam-Lari, Robert T. Bondokov, Tangali S. Sadrshirin, Univ of South Carolina, Dept of Electrical Engineering, Columbia, SC.

4H- and 6H-SiC crystals grown on the Si-face were chemically etched on the n-side (virgin) surface and the c-face (sliced side). The etching of both the surfaces revealed a strong relationship between a variety of etch pit morphologies and the morphology of the growth surface. Several different types of etch patterns were revealed. On the Si face, we observed small, medium, and large hexagonal shaped pits and a linear array of small etch pits. However, the C face contained only small pits and a linear array of small pits. We observed individual or group of dislocations that were connected from the Si face to the opposite C face of the wafer. Also, etch pit lines oriented along specific crystallographic directions were seen for our experimental conditions, indicating an anisotropy of the physical and chemical properties in SIC. An analysis of our observations shows that a correlation exists between the distribution of different size etch pits and the condition of the growth crystal process.

H5.5 SUBLIMATION GROWTH OF 6H-SiC Bulk On VARIOUS A-PLANE SUBSTRATES. Shigeru Nishino, Toru Nakahigashi, Tomonori Harusho, Toshiyuki Shimizu and Makoto Suzuki, Department of Electronics and Information Science, Faculty of Engineering and Design, Kyoto Institute of Technology, Matsugasaki, Sakyoku, Kyoto, JAPAN.

Recently, SIC epilayer on (11-20) plane is focused because high channel mobility of MOSFET was reported [1]. However, bulk growth of SiC layer is difficult. We already reported the preliminary results of a plane growth [2]. In this presentation, we focus on 6H-SiC bulk on (11-20) and (1-100) planes. We established the bulk growth by sublimation method and found optimum condition to get 2 inch bulk. In this time, we cut crystal was put perpendicular to the growth direction, c(0001), from the bulk SIC grown on (0001) basal plane. Cross sections of the substrates were carefully examined by X-ray diffraction and two a-planes, (11-20) and (1-100), were selected as the substrates. The crystals were set in a 1 cm cube and it was heated by rf induction. Sublimation growth was carried out following conditions: source temperature: 2200°C, substrate temperature: 2200°C, and inner argon pressure: 150 Torr. Growth rate was about 0.6 mm/h. The grown layer on (11-20) was a roofshaped and the top of the roof directed to <11-20> direction. The grown layer on (1-100) was also almost flat. Growth rate of the bulk on (11-20) substrates was a bit faster than the (1-100) substrate. X-ray rocking curve was measured for the substrate cut from the substrate to the top of the bulk. Better crystal quality was obtained on the top of the bulk. Enlargement of the bulk was not enhanced even though long run. Crystal defects were characterized by molten KOH and Ramon spectroscopy and Raman spectra were measured. [1] Asanuma, S., et al. ProC. ICS/SM99. [2] Nishino et al. in "Amorphous and Crystalline silicon Carbide 3", (1992), Springer-Verlag. p.15.


In view of its excellent thermal, mechanical and electronic properties, silicon carbide is the semiconductor material of reference for high temperature, high frequency and high power devices. The 4H-SiC polytype is considered as the most attractive for the fabrication of such devices, and great applications have made tremendous progress primarily because of the commercial availability of SiC substrates of ever increasing diameter and quality. The growth of thick epitaxial layers with low defect density is essential to achieve a constant quality of the epitaxial layer. The growth mechanism of the c-plane is not well understood. In this work, we have developed a two-dimensional computational model that computes the mass and heat transfer between the substrate and the reactor. The model is used to simulate the growth of SiC layers on a large area substrate. The model allows us to optimize the growth conditions for a large area substrate. The model is based on the conservation equations of mass, momentum and energy. The model is solved using a finite difference method. The model is validated by comparing the model predictions with experimental data. The model predictions are in good agreement with the experimental data. The model is used to simulate the growth of SiC layers on a large area substrate. The model is validated by comparing the model predictions with experimental data. The model predictions are in good agreement with the experimental data.
200°C, was aimed to grow epitaxial SiC films at a temperature lower than that required by thermal CVD. Several films of polycrystalline SiC were deposited on (110)-Si and (111)-Si wafers by the ECR-CVD technique, using SiH4 and CH4 as gas precursors at different flow rates, temperatures and microwave powers. The films were characterized by X-ray diffraction, transmission-electron microscopy, photoluminescence, and fast Fourier transform spectroscopy to verify the internal structure, while Fourier-transform infrared absorption and Rutherford backscattering spectrometry were applied to evaluate the chemical composition of the films. All the samples showed a polycrystalline structure and lateral dimensions of the 3C-SiC grains in the range of 300-2000 nm, which strongly depend on film composition and growth history, showing in optimized conditions a preferential orientation close to that of Si substrate. A correlation between film structure and deposition conditions (included substrate surface preparation) is presented and discussed.

H5.10 EPITAXIAL GROWTH OF SiC ON AIN / SAPPHIRE USING HEXAMETHYLDISILANE BY MOVPE. Kanki Teker, Ki Hoon Lee, Pirouz Pirouz, Case Western Reserve Univ, Dept Materials Science and Engineering, Cleveland, OH; Chisato Jacob, Shigeru Nishino, Kyoto Institute of Technology, Dept of Electronics and Information Science, Kyoto, JAPAN.

High quality SiC and AlN films allow the fabrication of metal/AIN/SiC MIS structures and SiC-AlN heterostructures that require a low lattice mismatch and excellent thermal stability. Epitaxial SiC on AlN is grown using hexamethyldisilane (HMDS) by MOVPE. 3H-AIN is epitaxially grown on sapphire by MOVPE, and subsequently SiC is deposited on it. The growth of high quality SiC was achieved by one-step process without any nucleation step using diborane (12% B2H6-Ar) as a carrier gas, which is less explosive than pure H2. The effect of growth temperature, thickness of AlN, concentration of source precursors on the SiC crystal quality and the surface smoothness was studied. All films were analyzed using reflection high energy electron diffraction (RHEED), Nomarski differential interference contrast microscopy (NDIC), X-ray diffraction (XRD), and atomic force microscopy (AFM). Optimum temperature for SiC growth was between 1300°C and 1350°C. At temperatures between 1200°C and 1300°C, the films show strong epitaxial relationship with AIN and very smooth surface (RMS ~0.1-0.75 nm). Below 1300°C, the film becomes polycrystalline. At 1400°C, it was highly textured, observed by XRD. In the RHEED, however, weak rings appear superimposed on the spot pattern, which implies the films are highly textured but polycrystalline. In order to evaluate the effect of AIN on the SiC film, AlN layers with various thicknesses (50, 200, 400 nm) have been used at 1350°C. The SiC film on a 50 nm thick AIN layer shows a very smooth surface (RMS ~0.1 nm) compared to the SiC film on a 400 nm AlN layer (RMS ~0.75 nm). This seems to be caused by the increasing roughness of AIN, as it becomes thicker. However, all films show high optical growth features, which imply that SiC is sufficient to relieve the mismatch strain of the underlying AlN/sapphire.

H5.11 EFFECT OF TMG ADDITION ON THE EPITAXIAL GROWTH OF 3C-SiC ON Si(100) and Si(111) USING HMDS BY MOVPE. Ki Hoon Lee, Kanki Teker, Ju Yong Chung and Pirouz Pirouz, Dept of Materials Science and Eng, Case Western Reserve University, Cleveland, OH.

Epitaxial crack-free 3C-SiC film was successfully grown on Si(100) and Si(111) by one step without any nucleation or carbonization step at a low temperature of 1200°C by MOVPE. The growth was achieved by using hexamethyldisilane (HMDS) with the addition of a small amount of trimethylaluminum (TMAl) with dilute hydrogen (12% H2 + Ar) as a carrier gas. The addition of TMAl during growth, epitaxial growth of SiC on Si was only possible at temperatures above 1300°C with a nucleation step at 1250°C. After growth, all the films were analyzed by cross-sectional transmission electron microscopy (TEM), X-ray diffraction (XRD), scanning electron microscopy (SEM) and X-ray photoelectron spectroscopy (XPS). It is observed by XPS that only a small amount of Ga is contained in the SiC film, which means Ga component of TMGa is not incorporated much in SiC film, in spite of the relatively high ratio of TMGa/HMDS. To investigate the effect of TMAl flow rate, various amount of TMAl (0.5 ~ 5mccm, 1mccm ~ 30mccm) was added during SiC deposition. Below 0.5 sccm of TMAl flow rate, SiC film shows epitaxial growth, as observed by TEM and XRD. Above 1 sccm of TMAl flow rate, the film shows smaller and broader, as the flow rate of TMAl increase. This result implies that the SiC lattice is being strained gradually with the TMAl addition. It is also observed by XRD that at the initial stage of growth, nucleation is much facilitated with the addition of TMAl. The deposition rate with the addition of TMAl at 1200°C is 500 nm/hr, which is much larger than the rate without TMAl addition (300 nm/hr). Thus, it is believed that TMAl addition make a positive effect on the nucleation and HMDS decomposition during deposition.


Carbonized buffer layers were formed on Si [100] oriented nominally and 2° off substrates with propane diluted in palladium purified hydrogen, using different temperatures and holding times. The growth of SiC on the carbonized substrate was shown to be stable and continuous, with an increase in the surface roughness being observed after some time due to the growth of SiC. Subsequent SiC layers were grown using silane and propane as atmospheric pressure with growth temperature ranging from 1150°C to 1350°C. The layers obtained were characterized by Raman spectroscopy, XRD, transmission electron microscopy, and optical microscopy. A series of experiments was performed to study the effect of etch pits density, the minimization of the residual strain on both sides of the SiC/Si heterointerface and the suppression of interfacial voids. Drastic influence on the interface morphology was evidenced depending on the transition step between the carbonization and the SiC epitaxial growth. We have also paid particular attention to the graphite susceptor condition by regularly reconditioning its surface, using an aging process and in situ SiC coating. As a result, we have developed a two-step carbonization process leading to very high quality SiC films grown at 1200°C.

H5.13 INTERACTION OF OXYGEN WITH 4H- AND 6H-SILICON CARBIDE. Y. Song and F.W. Smith, Dept. of Physics, City College of New York, Graduate Center, City University of New York, NY.

The ability to grow passivating SiO2 surface coatings on SiC is an important advantage of this material in both electronic and ceramic applications. The SiC oxidation reaction leading to the formation of SiO2 is complicated, however, by the presence of carbon. A thermochemical model describing the interaction of O2 with SiC will be used to predict the possible vapor and solid phase components formed and their locations in a CVD phase diagram. At high T and low CO pressures, the Si3C1 surface is etched, with the volatile SiO and CO species being formed. At intermediate T and P(O2) the products are solid SiO2 and CO, while at low T and high P(O2) only solid products are predicted to be formed, i.e. SiO2 and C. The unexpected prediction that solid C is a thermodynamically-stable product of the interaction of oxygen with SiC at low temperatures and high CO pressures will be analyzed and its implications for the growth of passivating SiO2 films on SiC will be discussed. The results of experimental investigations of the interaction of oxygen with the Si- and C-terminated (0001) surfaces of 4H- and 6H-SiC will also be presented. It has been found that the C-terminated surface not only oxidizes faster but also oxidizes more rapidly than the Si-terminated surface. Oxide decomposition via the reaction 2SiO2 + 4C → 2SiO2 + CO has also been observed, with interesting differences found for the 4H- and 6H-SiC substrates studies.

H5.14 STRUCTURAL AND ELECTRICAL CHARACTERIZATIONS OF OXYNITRIDE FILMS ON SOLID PHASE EPITAXIALLY GROWN SILICON CARBIDE. L.K. Bennett, W.K. Choi, Laboratory, Department of Electrical and Computer Engineering, National University of Singapore, SINGAPORE; D. McNeill, Department of Electronics and Electrical Engineering, The Queen's University of Belfast, BELFAST, UNITED KINGDOM; S.K. Bag, Department of Physics and Meteorology, Indian Institute of Technology, Kharagpur, INDIA; S. Chatterjee, and C. Maiti, Department of Electronics and Electrical Communication Engineering, Indian Institute of Technology, Kharagpur, INDIA.

The potential applications of silicon carbide [SiC] films in high temperature, high power and high frequency MOSFET devices require high-quality epitaxy. We present here structural and electrical results of as-prepared and rapid thermal oxynitride films on C⁺ implanted solid phase epitaxially grown SiC. The oxynitride was grown using N2O. The C concentration of the samples was estimated to be 1, 2 and 5 % from the infrared spectra, samples with 1 and 2 % carbon showed an absorption peak at 615 cm⁻¹ which indicates that the carbon is substitutionally incorporated into the silicon lattice. No precipitation of SiC form of Fe was observed at around 784 cm⁻¹. However, for the 5 % C sample, some precipitation was observed as indicated by a broad peak at ~800 cm⁻¹. The oxynitride films showed the Si-O-S stretching mode at 1076 cm⁻¹ and the amide-I mode at 1660 cm⁻¹, due to the O-Si-N bond. The peak at 810 cm⁻¹ is due to the Si-N and Si-Al bonds and C-O complex vibrational mode was
also observed at 663 cm$^{-1}$. The refractive indices of the oxide films with 1, 2 and 5 at. % C substrate were found to be 2.12, 2.18 and 2.40, respectively. The oxidation of the carbide films was carried out using the MOS capacitor structure. The interface state density was found to range between $5 \times 10^{11}$ to $5 \times 10^{12}$ cm$^{-2}$V$^{-1}$ and increases with an increase in the C concentration. The electrical breakdown field was found to be in the range of 9-17 MV cm$^{-1}$ and increases with an increase in C concentration. All the samples showed electron-trapping characteristics with the trap generation rate higher for lower C content samples. The charge-to-breakdown was measured to be 0.25 HC cm$^{-2}$ and decreases with an increase in C concentration.

H5.15 OXIDATION STUDY OF HYDROGENATED AMORPHOUS SILICON CARBIDE FILMS. W.K. Choi and L.P. Lee, Microelectronics Laboratory, Department of Electrical and Computer Engineering, National University of Singapore, SINGAPORE.

Hydrogenated amorphous silicon carbide ($n$-Si$_{1-x}$C$_x$H) films have attracted significant research interests due to their potential applications in optoelectronic devices. We present here results of an oxidation study of $n$-Si$_{1-x}$C$_x$H films prepared by the plasma enhanced chemical vapor deposition of silane and acetylene. The composition (i.e. x) of the samples was determined by the flow rates of silane and acetylene. Oxidation was carried out at 400 to 600°C in dry oxygen ambient. IR spectra of the as-prepared films showed the intensity of the Si-C peak decreases and the Si-CH$_3$ peak increases as x increases. The Si-H peak shifts to higher frequency as x increases. Note that the oxidation of CH$_3$-H radicals has shown to introduce voids and increased the porosity of the films. The IR spectra of the oxidized samples showed clear Si-O stretching and rocking/vibrational modes for $n$-Si$_{1-x}$C$_x$O$_{1-y}$H$_y$ and an absent of such modes for $n$-Si$_{1-x}$C$_x$O$_{1-y}$H$_y$ films. We suggest that growth of oxide on $n$-Si$_{1-x}$C$_x$H is a result of voids that facilitate the diffusion of oxidents into the film. For sample oxidized at 400°C, we observed a super linear and a parabolic regime in the oxide thickness vs oxidation time plot. For sample oxidized at 500 and 600°C, only the parabolic regime was observed. The Si-O stretching peak of oxidized films were found to be at 1056-1071 cm$^{-1}$ for films oxidized at 400 and 500°C. This shows that the oxides are rather porous and slightly oxygen deficient, i.e. $n$-SiO$_x$ and SiO$_y$, for the 400 and 500°C oxidized samples. The capacitance vs voltage (C-V) curves of the AlOx/SiO$_2$/Si capacitors fabricated from oxidizing the $n$-Si$_{1-x}$C$_x$H films at 1000-1000°C showed a large flatband shift (>11 V) and big hysteresis (10-15 V). This indicates the oxide contained large amount of trapped charge.

H5.16 QUALITY OF THERMALLY GROWN OXIDE IN 4H-SiC OVER NITROGEN AND PHOSPHORUS IMPLANTED REGIONS. J.A. Khan, B. Um, M. Moin, M.A. Capasso and J.A. Cooper Jr., Purdue University, Department of Electrical and Computer Engineering, West Lafayette, IN.

Recent studies of the dielectric strength of thermally grown oxides reported in the literature have been over non-implanted epilayers [1]. The oxide strength was found to be less than 10 MV cm$^{-1}$ at room temperature [1]. The electrical characteristics of oxides typically over implanted regions, however, have not been investigated extensively. Oxide quality over implanted regions is important for metal-oxide-semiconductor field-effect transistors (MOSFETs) that have a gate electrode which overlaps the implanted source/drain regions. For n-channel MOSFETs, phosphorus and nitrogen are the preferred species for source/drain implantation. The quality of oxides over these regions can potentially affect the performance of the device. Low dielectric strength of the oxide can cause excessive gate leakage currents in the on-state, resulting in total failure of the device or poor device transfer characteristics. Furthermore, excessive injection of carriers in these regions can significantly affect the life of the device by creating a short between the source/drain and the gate. In this talk, we present the results obtained from the electrical characterization of capacitors formed thermally grown oxides over implanted regions in 4H-SiC. The implanted samples were annealed at 1200°C for 30 min in argon. The oxide over these regions has a much lower breakdown field as compared to the non-implanted regions. For nitrogen and phosphorus implanted breakdown of the oxide at room temperature occurred at about 75 MV cm$^{-1}$, and for phosphorus capacitors it occurred at about 2.5 MV cm$^{-1}$. The results are compared with a control sample from the same wafer that is processed along with the above samples, but does not go through the implant step. This sample had a breakdown field close to 9 V cm$^{-1}$. Additional measurements of the oxide leakage current taken at 100-200°C will be reported. The implications of these results on the performance of MOSFETs will be discussed.


Surface passivation is a central issue in successful SiC device applications. Thanks to the exceptional properties of silicon dioxide, the most promising passivation is expected to be achieved by surface oxidation. However, the latter might result in mixed Si and C oxides products for SiC due to the presence of a binary compound. We investigate the oxidation of the SiC(0001) surface with a high-resolution scanning electron microscopy (SEM) at atomic scale. The STM study of oxygen interaction with the cubic 3C-SiC(0001) surface is found to be significantly anisotropic with a propagation faster along dimer rows. Initial oxygen atoms interact with surface defects leading to the formation of other defects having the same nature. The latter defects become active sites upon further oxygen deposition leading to a self-propagating oxidation process. For hexagonal 6H-SiC(0001) surface, the STM study indicates an isotropic propagation of the oxidation in contrast to the cubic 3C-SiC(0001) surface behavior.

The oxidation process by oxygen exposures at surface temperatures between 300 K and 900 K. Unlike silicon surfaces, 6H-SiC(SiC(0001)) oxidation is taking place already at low oxygen exposures. The oxidation kinetics are significantly enhanced at increasing surface temperatures. The results also indicate that the direct oxidation of the 6H-SiC(0001) surface leads to SiO$_2$ formation at low temperatures (800 K) with a non abrupt interface having significant amounts of SiO$_x$-O$_x$ and intermediate (Si$_3$, Si$_2$, Si-O) products. In contrast, C-free and abrupt SiO$_2$/6H-SiC(0001) interface formation is achieved when pre-deposited Si overlayer is thermally oxidized at low oxygen exposures and low temperatures (800 K).

H5.18 AB INITIO STUDY OF SI/METAL POLAR INTERFACES: RELATION BETWEEN INTERFACE STRUCTURE AND SCHOTTKY-BARRIER HEIGHT. Shingo Tamaka [SWING], Masanori Kobayashi, Osaka National Research Institute, Dept of Material Physics, Osaka, JAPAN.

Ab initio study of the Si/metal polar interfaces has been performed based on a pseudopotential and a supercell method using the technique of the first-principles molecular dynamics method. SiC is very important for high-performance electronic and optoelectronic devices. For such applications, it is essential to fabricate SiC/metal interfaces with good electronic properties. Recently, our group has performed ab initio calculations for such interfaces as the SiC/Al and SiC/Si system and obtained interesting results. The difference of interface dipole and Schottky-barrier height (SBH) for different terminated atom pairs. SBH is sensitive for atomic and electronic structures at the reactive interface and is difficult to discuss with traditional simplified models. In this paper, we mainly discuss the SBH with the calculated work functions for both the SiC-slab and metal-slab. Stable atomic configurations, charge distributions, local density of states and SBH are presented for the 3C-SiC(0001)/Al, 3C-SiC(0001)/Si and 3C-SiC(111)/Ti polar interfaces, both the Si-terminated and C-terminated are dealt with. Results show that the C-terminated interfaces have strong covalent (p-band) metallic bonding and large adhesion energies and small SBH. We thus say a good candidate for terminated atom in SiC devices with Al or Ti contacts is the carbon.

H5.19 ALUMINUM-NICKEL AND ALUMINUM-TITANIUM COMPOSITE CONTACTS TO p-TYPE SILICON CARBIDE DIFFUSED LAYER. Xiaolin Wang, Stavan Soloviev, Ying Gao, Tanguh Sudarman, Univ of South Carolina, Dept of Electrical Engineering, Columbia, SC, John R. Williams, Auburn Univ, Leach Nuclear Science Center, Auburn, AL, John Crofton, Physics Department, Murray State University, Murray, KY.

The outstanding physical properties of silicon carbide allow utilizing this material for high temperature, high power, high frequency electronic devices. To achieve the highest performance of these devices stable ohmic contacts with as low as possible specific resistance are necessary. In this paper, results for the contact resistance of 6H-SiC material with a diffused p-type layer.
The p-type layer was fabricated by diffusion from vapor phase into both p-type and n-type substrates. Surface concentration of holes in the diffused zone was about $10^{18}$ cm$^{-3}$ for the n-type substrate with a low doping level of about $10^{16}$ cm$^{-3}$ without diffused layer was formed. Two types of metal structures (Al/Ni and Al/Ti) with thermally evaporated aluminum and sputtered nickel and titanium layers, respectively, were studied. Before placement in deposition chamber samples were cleaned by standard RCA process. Annealing of the samples was realized either by an electron beam in vacuum or in a tube furnace with argon atmosphere at 1100°C. The values of specific resistance for this type of diffusion were estimated by using a two-terminal resistor structure (Cox and Strack method), while the values of specific resistance for n-type substrate with a phosphorous diffusion layer measured using the transmission line method (TLM). To implement the Cox and Strack method an array of metal dots of diameter varying from 20 to 240 μm was fabricated on the top of a wafer and bottom side of the substrate was fully metallized. The influence of annealing conditions for each metal structure on the values of specific contact resistance is discussed in this report.

H5.20

Nickel Sulfide (NiS2) is investigated as possible Ohmic contact to heavily nitrogen doped n-type 4H-SiC and 6H-SiC. Nickel sulfide was deposited with various thicknesses on both Si and C faces of the SiC substrates. The NiS2 contacts were formed as room temperature as well as at elevated temperatures (900°C to 1000°C). Contact resistivities and I-V characteristics were measured at temperatures between 100°C to 300°C. To investigate the electric properties, I-V characteristics were studied and the Transmission Line Method (TLM) was used to determine the specific contact resistance for each sample at each annealing temperature. Both Rutherford Backscattering Spectroscopy (RBS) and Auger Electron Spectroscopy (AES) were used for depth profiling of the NiS2/Si, and C X-ray Photoemission Spectroscopy (XPS) was used to study the chemical structure of the NiS2/SiC interface. Acknowledgment Research sponsored in part by the NASA, - Alabama Space Grant Consortium, Ctr. For Irradiation of Materials of Alabama & M University and by the U.S. Department of Energy under contract DE-AC05-00OR22725 with the Oak Ridge National Laboratory, managed by UT-Battelle, LLC.

H5.21
COMPARISON OF CURRENT-VOLTAGE CHARACTERISTICS OF N AND P TYPE SiC SOTCHKO DIODES. Qinghun Zhang, Vijay Madanagari, and T gargi S. Sadashiva, University of South Carolina, Dept. of Electrical Engineering, Columbia, SC.

Current-voltage (I-V) characteristics of N and P type SiC Schottky diodes were measured with forward currents at room temperature, with the diodes in a temperature range of room temperature to 400°C. The results indicate that the I-V characteristics of the N type Schottky diode are more linear than those of the P type Schottky diode. The forward current of the Schottky diodes was measured to be greater than the reverse current. The I-V characteristics of the P type Schottky diode showed a non-linear behavior even after turn-on, indicating a variation in the on-state resistance with increase in forward current. The on-state resistance of the P type Schottky diode, resulting in a non-linear increase in the forward current, is attributed to the activation of impurity acceptors with increase in temperature due to high current density. Though the voltage drop across the P type Schottky diode is initially higher than that across the N type Schottky diode, it decreases as the current increases. For high temperature measurements, the on-state resistance of the P type Schottky diode decreases with increase in temperature until a 'knee temperature', above which the resistance increases in the case of N type Schottky diodes. Further, high temperature measurements clearly indicate that the on-state resistance of the Schottky diode increases with increase in temperature, the on-state resistance of P type Schottky diodes decreases with increase in temperature until a 'knee temperature', above which the resistance increases in the case of N type Schottky diodes. The knee temperature was found to be strongly dependent on the Schottky contact diameter, decreasing with decrease in contact diameter. Techniques such as 'current spreading' doted to reduce the threshold voltage of P type SiC Schottky diodes so as to exploit the observed negative resistance behavior will be discussed in detail in the paper.

H5.22
LOW TEMPERATURE FORMATION OF NiS2 CONTACTS TO SiC. A.H. Hoser, C.W. Deeb, H. Kahn, Case Western Reserve University, Dept. of MS&E, Cleveland, OH.

Thermodynamically stable, low specific contact resistance electrical contacts to SiC are essential to the application of such devices in high power or high temperature applications. Nickel disulfide (NiS2) is very useful for this application, as contacts can be formed on SiC by reacting a sacrificial layer of n-type silicon on p-type silicon (n+ on p) with a layer of sputtered nickel at 300°C. Using sacrificial n, NiS2 forms directly, this is not the case when Ni reacted with single crystal Si or with polycrystalline, more Ni-rich disilicides initially form. Thin film resistivity and specific contact resistivity were measured using circular TLM devices. This NiS2/NiS2 interface has also been characterized using high resolution TEM.

H5.23
OPTICAL ABSORPTION OF DOPED AND UNDOPED BULK SiC. H. Miller, J. Dunn, W.L. Zhang, M.O. Mason, Department of Electrical and Computer Engineering, University of New Mexico, Albuquerque, NM; J.C. Ferreira, J.C. Ferreira & Associates, Engineering Research & Engineering, SINGAPRE; I. Ferguson, E3CORE Corporation, Jerusalem, NJ.

Optical absorption spectra of undoped, n-type, and semi-insulating 6H and 4H bulk SiC were obtained in the spectral range of 200 - 3200 nm (2.60 - 0.3875 eV). Several features were observed in the absorption spectra collected for various samples. A sharp peak below the band gap was observed in 4H SiC. The intensity of this peak was observed to increase in samples that exhibit larger absorption due to free carriers, which leads us to conclude that the defect responsible for this peak is also the source of the free carriers in this material. Additionally, a series of optical absorption peaks separated by approximately 21 meV were observed around 0.9185 eV (1350 nm). Based on preliminary analysis, these peaks may be due to s-p transitions in SiC - related defects. The optical absorption above the band edge was observed to be sample dependent. The optical absorption measurements of the band gap show that 4H SiC has a larger band gap as compared to 6H SiC. In all doped samples, the band gap is decreased as the doping density is increased. The variation of the band gap as a function of temperature is also observed to be sample dependent. In certain samples, the band gap was found to be approximately independent of temperature in the entire range of 100 - 300 K.

H5.24

We present the first ellipsometric measurements of both the ordinary ($e_1 \pm e_2$) and extraordinary ($e_1 \pm e_3$) dielectric functions of 4H- and 6H-SiC in the spectral range from 0.7 to 9.0 eV. Two sets of samples were measured for material of different quality, with the [11-20]-direction and (210)-direction normal to the surface. Optical axes were determined by reflection difference spectroscopy and samples were aligned during subsequent ellipsometric measurements such that a 90° rotation of the [110]-oriented sample yielded spectra equal that obtained for the [1-10]-oriented sample and vice versa. Results indicated that parallel components of e differ most dramatically from perpendicular components at energies above 5 eV and that this difference is greater for 4H- than for 6H-SiC, consistent with expectations based on the physical structure of the polytypes and with current theoretical predictions. E.g., we observed that the effects of polytypeism are more pronounced in the perpendicular components than in the parallel components for this effect is more pronounced in the imaginary parts of $e_1 \pm e_3$ and that there is a relative decrease in the number of well-defined peak structures in $e_3 \pm e_3$ for 6H relative to 4H, as expected. We will discuss these and other differences in the context of the observed spectral features and their relationship to SiC bandstructure. E.g., preliminary results from both real and reciprocal space analysis of ellipsometric line-shapes indicates that the controversial shoulder observed near 5.5 eV in $e_1 \pm e_1$ for 4H-SiC is indeed a critical point $E_g = (5.74 \pm 0.05)$ eV with $\Gamma = (240 \pm 50)$ meV, with the $\Gamma$ peak of the same shape located at $E_g = (6.87 \pm 0.01)$ eV with $\Gamma = 179$ meV.

H5.25
CALCULATION OF POSITION CHARACTERISTICS IN SiC CARBIDES. Bernardino Barbiellini, Northeastern Univ, Dept of Physics, Boston, MA; T.J. Karpowicz, Ohio State Univ, Dept of Low Temperature Physics, Prague, CZECH REPUBLIC; W.H. Arrasmith & R. Brasier, Research Center Rossendorf, Institute of Ion Beam Physics
and Materials Research, Dresden, GERMANY.

Positron affinity calculations performed by a first-principles approach based on density functional theory reveal, contrary to many other semiconductors, that free positrons and positronium can escape from SiC. It is found that the treatment of the electron-positron interaction plays a crucial role when calculating the annihilation characteristics. These characteristics originating from both valence and core electrons, combined with the corresponding measurements, yield a very useful tool for surface studies and point defect identification in the bulk. Calculations will be compared with experimental data obtained for positron annihilation in dislocations and the Si-C-dielectricity which were created by ion implantation and subsequent annealing.

H5.26
THEORETICAL INVESTIGATION OF INTRINSIC DEFECT COMPLEXES IN α-SiC. Evon Rauls, Zoltan Hajnal, Thomas Franzke, Meinolf Petersen, Meinolf Petersen, Theoretische Physik, University of Technology and Economics, Dept of Atomic Physics, HUNGARY.

Properties of isolated intrinsic defects in SiC are widely studied and their atomic and electronic structure is already known. Although further experimental evidence shows the presence of defect complexes, only a few of them could be clearly identified up to now. In binary semiconductors n-type pairs play a special role. In SiC it is expected to be a defect with high formation energy, however, it is likely to be created during irradiation, or non-equilibrium growth. The properties and role of these defects in diffusion, in growth as well as their interaction with point defects deserves attention. Therefore, we describe first the atomic structure and properties of selected vacancy-defect complexes calculated within a self-consistent charge density functional based tight binding scheme (SCC-DFTB). Since no pair formation in the perfect lattice is very unlikely to occur, we then systematically investigate the lowering of its formation energy and barrier in the presence of other intrinsic defects. Besides carbon vacancies, we find V_2C-CV complexes to particularly promote formation of an n-type pair. Its formation energy and barrier are reduced by over 1.0 and 4.5 eV, respectively. Since the calculated absolute energies are still too high to be relevant for thermal processes, further work is in progress to identify energetically more favourable routes.

H5.27
STUDY OF Ga IMPLANTED p-TYPE 4H-SiC FOR OHMIC CONTACT METALIZATIONS. M.D. Prentice, A.A. Bialas, University of Maryland, Dept of Electrical and Computer Engineering, College Park, MD; M.C. Wood, M. Derenge, B. Geil, and K.A. Jones, Army Research Laboratory, Adelphi, MD.

The development of high quality ohmic metallizations on p-type SiC is of critical importance to the performance of high temperature/high power SiC devices. Our previous work indicated that the use of Ga focused ion beam metalization and contact resistivity on p-type SiC significantly [1]. During the application of the focused ion beam surface modification, Ga was found to be incorporated within the top 100 nm of the sample. In the present work, we have employed focused ion beam implantation techniques to perform shallow (30 nm) Ga implantations on p-type 4H-SiC, and examined the physical and electrical properties of the system under high temperature annealing. The implantations were carried out at an energy of 70 keV and doses ranging between 10E15 and 10E16 per cm2. Samples were annealed between 1000 and 1600 C. SIMS analysis was employed to verify the implanted profiles and identify the changes in the distribution of the elements, while AFM surveys were performed to identify morphological changes of the surface prior to and after treatment. An AlN layer of approximately 50 nm was also deposited by pulsed laser deposition (PLD) on the surface of the samples, in order to serve as a protective layer during annealing. The results showed that significant oxidation of Si and redistribution of Ga occurred through the AlN layer at 1500 C. As-implanted and annealed samples were electrically evaluated for contact resistance by the TLM method. The electrical and physical evaluation of the p-Ga-SiC metallization system will be reported and the implications of the incorporation of Ga into the SiC lattice will be discussed. [1] A.A. Bialas et al., EEM, Vol. 29, No. 3, pp 139-140, 1999

H5.28
STRUCTURAL, CHEMICAL AND ELECTRICAL CHARACTERIZATION OF 4H-SiC IMPLANTED BY N+ IONS AT 30000 °C AND ANNEALED AT 1700 °C. R. Sporti, M. Boccoli, CIN-LAMEL, Bologna, ITALY; G. Mattei, CIN-LAMEL, Roma, ITALY; A. Cerrara, INFN and Universita degli Studi di Padova, Padova, ITALY.

4H-SiC on-axis and off-axis wafers were implanted at 30000 °C by N or Al ions at different energies between 300 keV and 3 MeV and different fluence values so to produce 1 mm thick doped layers with a doping concentration modulated across the value 5 x 10^15 cm^-3. Penetration and range were intentionally controlled in this box shape profile. All the samples were annealed at 1700 °C for 30 min. The structural characterisation of the as-implanted and annealed samples was done by Rutherford Back-Scattering spectrometry (RBS-C) and the (001) r-channeling geometry and by confocal micro-Raman spectroscopy (m-R) (Ar laser 514.5 nm). Only micro-Raman allow us to estimate the thickness of the damaged layer by taking into account both the integrated intensities of the 780 cm^-1 band and of the broad background signal, which as function of the heating defocusing distance from the sample surface. After the annealing the crystalline quality was restored as measured by RBS-C and m-R and no material losses detected as shown by the comparison of the doping profiles in the as-implanted and annealed samples as measured by Secondary Ion Mass Spectrometry (SIMS). m-R cross measurements of the annealed samples allowed us to study the behaviour of O and phosphor-phason mode from which information on the depth distribution of the free carrier density was extracted.

H5.29
DIFFUSION IN SECONDARY DEFECTS BETWEEN HIGH ENERGY B+ AND Al+ IMPLANTED 4H-SiC. Toshiyuki Ohno, Ultra-Low Loss Power Device Technology Research Body (UPI/R&D) Association for Future Electronic Devices (FED), Tsukuba, Ibaraki, JAPAN; Naoto Koyanagi, UPI/Electronical Laboratory, Tsukuba, Ibaraki, JAPAN.

B+ implanted pn-junction has small reverse leakage current than that in Al+ implanted one. This result has some relation with the residual defects in implanted layers but the detailed reason is not clear. In this paper, report on the cross-sectional TEM observations in high-energy B+ or Al+ implanted 4H-SiC and show the difference in the structure and density of secondary defects between the two implanted layers. For the similar dopant concentration, B+ implanted samples have larger size of secondary defects compared to Al+ implanted ones. For example, when the dopant concentration is 2 x 10^15 cm^-2 (dose of 7 x 10^15 cm^-2 for 2.0-0.15 MeV B+ implantation and dose of 2 x 10^15 cm^-2 for 2.0-0.5 MeV Al+ implantation) and annealing temperature is 1700 °C, the defect size in B+ implanted samples is 4-20nm and that in Al+ implanted one is 2-4nm. In B+ implanted sample, the structure of the defects larger than 12nm is disturbed along with an extrinsic Si-Cliger parallel to (001) (type-A) and those smaller than 12nm have no extra plane and show strained contract (type-B). On the contrary, defects in Al+ implanted sample are all type-B. When Al+ dose is increased to 2 x 10^15 cm^-2, the size of defects grows 3-15nm. In this sample, the defects with the size larger than 12nm are type-A and others are type-B. Secondary defects in implanted layers of 4H-SiC are probably formed by agglomeration of interstitials, generated by implantation and when enough amount of them are inserted on the basal plane, type-A defects are formed. Above mentioned results suggest that agglomeration kinetics of interstitials are different between B+ and Al+ implanted layers and interstitials can cluster easier in B+ implanted ones. This work was performed under the management of FED as a part of the MITINSS Program (R&D of Ultra-Low Loss Power Device Technologies) supported by NEDO.

H5.30
PHYSICAL AND ELECTRICAL CHARACTERIZATION OF RESIDUAL IMPACT DAMAGE IN 4H-SiC DOUBLE IMPLANTED BIPOLAR TECHNOLOGY. N.G. Wright, C.M. Johnson, S. Ortolini, A.B. Horwatt, K. Adachi, A.G. O'Neill, Dept of Electrical Engineering, University of Newcatter, UNITED KINGDOM; P.G. Coleman, Dept. of Physics, University of Bath, UNITED KINGDOM; A.P. Knights, Dept of Electrical Engineering, University of Surrey, UNITED KINGDOM.

The effects of post-implant anneal conditions on the level of residual damage resulting from nitrogen and boron impunts after different anneal processes are investigated using the PAS and RBS techniques. It is shown that after implantation there is a substantial depth dependence concentration significantly below the range of the implants. However such damage is almost completely recovered after anneal in contrast with the damage close to the implant range point. Such residual damage has a strong effect on the electrical characteristics of double implanted bipolar transistors - principally through reduction in carrier mobility and lifetime. It is shown that the precise implant and anneal conditions can play a strong role in the electrical characteristics of such devices and a methodology for optimising such conditions is suggested.

H5.31
IMPURITY ACTIVATION IN N+ NON-IMPLANTED 4H-SiC WITH PULSED LASER ANNEALING METHOD. O. Egusa, A. Acymia, K. Ake and K. Nakashima, Dept. of Electrical and Computer Engineering, Nagoya Institute of Technology, Nagoya, JAPAN.
We have succeeded in pulsed laser annealing of N⁺ ion implanted 6H-SiC, which induces little redistillation of implanted impurities after annealing with low laser energy density without melting the surface region, the ion-implanted impurities was electrically activated. SiC substrates with impurity concentration of 7.6 x 10¹⁷/cm³ were implanted with 30 keV N⁺ ions with dose of 4.8 x 10¹⁴/cm² (N concentration at dose 1 x 10¹⁵/cm³). After pulsed laser annealing, a contact resistance was measured to be 5.7 x 10⁻³Ω cm² using Al electrodes deposited on the N⁺-implanted layer. Using the time resolved optical reflectivity measurements, we have obtained information during laser annealing. The vibration of the reflectivity was observed during the laser annealing on samples which were amorphized by ion-implantation. We consider that this vibration should be caused by interference of optical reflections from both the surface of the substrate and that of the self-propagating liquid layer, moving in the amorphous SiC towards the interface between the amorphous layer and the crystalline substrate. 

In the case of laser irradiation on the sample implanted with such a low dose of ions as that does not induce an amorphous layer, the change of the reflectivity was slight, and the vibration of the reflectivity was not observed. Present results show that the impurity-implanted layer with a high current concentration can be formed by both ion-implantation and pulsed laser annealing methods at the room temperature.

H5.32 EFFECT OF C/B SEQUENTIAL IMPLANTATION ON THE B ACCEPTORS IN 4H-SiC. Yoshiaki Nakano, Tetsu Kuchi, Hiroshi Tadano, Toyota Central R&D Labs, Inc., Aichi, JAPAN; Rajesh Kumar Malhotra, Denso Corp, Aichi, JAPAN.

Ion implantation technique is important as a selective area doping process in SiC electronic devices. Boron (B) is one of the promising gap-closing IIIA group impurities for n-type doping at the near surface level and deep level. B-related deep defect can lead to the degradation of the device electrical characteristics in long term; therefore, a suitable process is needed to suppress the deep defect level, known as D-center. Breddel et al. have demonstrated that sequential implantation of C/B can suppress the formation of the D-centers based on a site-competition effect. In this study, using thermal admittance spectroscopy (TAS) and deep level transient spectroscopy (DLTS), we have systematically investigated the effect of sequentially co-implanted C on the formation of shallow and deep level defects introduced by the C/B sequential implantation. (0001)-oriented 4H-SiC P⁺/P⁺ epitaxial wafers were used. The background SiC impurity concentration and thickness of the epitaxial layer were 1 x 10¹⁵/cm³ and 5 μm, respectively. Multiple step C and B implantations with suitable ion energies was performed at 1000°C (depths 0.75 μm). The mean B concentration in the implanted region was 1 x 10¹⁵/cm³. The C concentration was varied from 1 x 10⁶ to 1 x 10¹⁰/cm³. The samples were annealed at 1700°C in Ar to activate the dopants. Finally, TAS and DLTS measurements were performed on fabricated Schottky diodes. The density of D-centers was found to start decreasing with increasing concentration of C implantation and to be completely suppressed for the C and B ratio of 1/1. However, a new deep level defect shows up at about 45 kV/cm for the C and B ratio of 1/1, i.e., C-rich condition. The C-V results also indicate a decrease in the concentration of N⁺-implanted impurities in C-rich condition. As a result, the concentration of co-implanted C is found to be very sensitive to the formation of B acceptors and deep levels.

H5.33 PULSED LASER PROCESSING ON SiC SUBSTRATES AND ITS APPLICATION TO UV SENSORS. Kenshiro Nakashima, Osamu Eruy and Yuriko Nakashima, Nagoya Institute of Technology, Dept. of Electrical and Computer Engineering, Nagoya, JAPAN; Masahiro Watanabe, Ion Engineering Institute Corporation, Osaka, JAPAN.

Silicon Carbide (SiC) devices are expected for use in high temperature environments with high power and low loss conditions. Several sensor applications such as ultraviolet sensitive diodes (UV sensors) and gas sensors are other fields of targets for SiC devices under the high temperature environment. Although SiC diodes are suitable for detecting UV emissions around 300 nm because of the wide band gap energy of the material, they need shallow junction depth less than about 100 nm for optimum detection of the UV emission. Additional refinements of impurity-implanted layers are necessary for fabricating such a shallow junction using conventional impurity-implantation and subsequent annealing. In addition, ohmic electrodes prepared with the high temperature annealing procedure easily penetrate the thin junction region to destroy the diode characteristics. For these reasons, it is important to develop a laser processing method to improve the impurity-doping techniques and to lower the device processing temperature. This paper describes results on controlling SiC dopant profiles in n-type 6H-SiC with the pulsed laser processing using a KrF excimer laser with pulse energy of 100 mJ/cm² and a laser spot size of 100 μm. As a result, high-quality Si-C acceptor properties of SiC impurities in the n-doped state were confirmed with both Hall effect measurements and photocurrent measurements due to the electron transition from the conduction band to the acceptor band. As shown in the present process, laser annealing is an effective method of processing SiC UV sensors. The laser processing techniques have made it possible to fabricate SiC Schottky-barrier contacts with a narrow contact transition region on the 6H-SiC substrate in addition to those obtained with laser annealing. The emission characteristics of P+ junction diodes were measured with a spectral response in the wavelength range from 300 nm to 430 nm. Preliminary external quantum efficiency is estimated to be 40% at 340 nm without surface passivation.

H5.34 OPTICAL PROPERTIES AND MICROSTRUCTURE OF ION-IMPLANTED SiC. F. W. Smith and Y. Song, Dept. of Physics, City College of New York, NY.

Ion implantation is the preferred method of introducing dopants into SiC. Depending on the level of implantation, the resulting damage can lead to the amorphization of this material and the loss of chemical order. Chemical ordering in SiC corresponds to a high concentration of Si-C bonds and is observed in deposited amorphous SiC films. When ion implantation of SiC occurs at low T, however, the disordered region may not be able to reach a relaxed amorphous state of lower free energy. As a result, significant concentrations of like-natom bonds, i.e. Si-Si, C-C, and Si-C bonds, are likely to be present. The presence of these bonds can be detected optically since Si-Si and C=C bonds absorb below the optical energy gap of SiC. Measurement of the optical dielectric function in the implanted region can serve as a useful probe of the microscopic structure of the disordered material and also its evolution with the degree of implantation and annealing. Effective medium models have been used to describe the dependence of the optical response of the damaged SiC on its microstructure. Such a model based on a homogeneous mixture of four components (amorphous Si with Si-Si bonds, amorphous C, C=C bands, amorphous SiC with Si-C bonds, and void regions) will be used to determine whether the local bonding is random, chemically ordered, or phase-separated. The predictions of this model will be presented and compared with existing experimental results to determine how the volume fractions of these four components vary with the level of implantation and with annealing.

H5.35 HIGH HOLE LIFETIME (3.8 μs) IN 4H-SiC DIODES WITH 5.5 kV BLOCKING VOLTAGE. Pavel A. Feoktistov, Michael E. Lemonides, Scobeltsr, Ramyantsev, Jeff Cook, State Electronics Division, St. Petersburg, Russia; Kenneth G. Irvine, Ole Kordine, John W. Palmour, Rishar Singh, Cree Inc, Durham, NC.

Pulse current-voltage characteristics and minority carrier lifetime at high injection level have been measured in 4H-SiC p⁺-n diodes with 5.5 kV blocking voltage. The voltage-blocking n-layer (base) was 50 μm thick and had a donor doping concentration N⁺-N = 6 x 10¹⁵/cm³. The doping level in the p⁺-emitter directly above the junction was 3 x 10¹⁶/cm³. The structure diameter was 500 μm. To estimate the effectiveness of base modulation by minority carriers, isothermal forward current-voltage characteristics of the diodes were measured in the temperature range from 269 to 550 K. Current-voltage characteristics and current densities were obtained at 4 x 10⁻³ Ohm⁻² cm⁻². Meanwhile, the charge of the non-modulated base was |R| = Wₓ / μ₁ ρₓ ≃ 6 x 10⁻⁷ Ohm cm², i.e., 15 times higher than the experimentally observed value, provided that μₓ = 800 cm²/Vs and nₓ = 4 x 10¹⁴ cm⁻³. Hence, the charge-voltage characteristics of the base strongly depend on the high level of base resistance modulation. Hole lifetime τ in the n-base of the diodes has been measured in the temperature range from 269 K to 550 K using Open Circuit Voltage Decay technique. The τ increases monotonically from ~ 0.6 μs at 390 K to ~ 4 μs at 550 K. To the best of our knowledge, the above values of τ are the highest reported for 4H-SiC.

H5.36 FABRICATION OF 2.4 kV HIGH VOLTAGE N-TYPE 4H-SiC SCHOTTKY BARRIER DIODES USING THICK EPITAXIAL LAYERS. Takashi Tsuji, Hiroki Fujisawa, Shunji Ogino, Fuji Electric Corp., R&D Ltd., Yokosuka, JAPAN; Hidekazu Tsuchida, Isao Kominami, Tatsuo Mikiyama, Kenji Fujita, Central Research Institute of Electric Power Industry, Yokosuka, JAPAN.

Fabrication and characterization of n-type 4H-SiC Schottky barrier diodes using 27 μm thick epitaxial layers with the carrier concentration of 2 x 10¹⁷/cm³ grown by low pressure chemical vapor deposition are presented. These Schottky barrier diodes have a current density of 10⁶ A/cm² on the guard ring of 100 μm width and 0.5 μm depth, which were made by boron ion implantation followed by the 30 min annealing at 1700°C. The Schottky barrier diodes with the diameter of 4mm showed the breakdown voltages more than 800V and the leakage
currents of $1 \times 10^{-3} \text{A/cm}^2$ at 600V. Breakdown voltage 2.4kV, which was 55% of the ideal parallel plate breakdown voltage, was obtained on a 1.4% Si-doped Schottky barrier. It showed Schottky barrier height of 1.01eV with an ideality factor of 1.01. The on-resistance was 12.7mOcm, which is a little higher than that of the substrate is 5.7mOcm. Optical beam induced current analysis was done to clarify the origin of the high leakage current over the wide range from $1 \times 10^{-6} \text{A/cm}^2$ to more than $1 \times 10^{-4} \text{A/cm}^2$. Many bright spots were recognized in the high leakage current SBDs.

H5.37 TEMPERATURE DEPENDENCE OF CHANNEL MOBILITY IN 4H-SiC MOSFETS. Shinsuke Harada,1,2 Ryoji Kosugi1,3, Yumiko Senzaki1,3, Seiji Suzuki1,2, Won-Ju Cho1,2, Kenji Fukai1,2, Kanso Araki1,2,3. 1Ultra-Scale Power Device Technology Research Body, 2R&D Association for Future Electronic Devices, 3Electrotechnical Laboratory, Ibaraki, JAPAN.

4H-SiC metal-oxide-semiconductor field effect transistor (MOSFET) is a promising candidate for high power electronic devices due to excellent physical properties of 4H-SiC. However, some problems still exist to achieve the high quality 4H-SiC MOSFETs. The most important is the low channel mobility of electrons in the surface inversion layers. 4H-SiC MOSFETs with a thermally grown oxide gate have a channel mobility less than 10 cm²/Vs, which is much lower than that of bulk 4H-SiC ($\approx 8000$ cm²/Vs). Recently, Schömer et al. have analyzed the temperature dependence of the channel mobility in p-type 4H-SiC MOSFETs, and proposed that interface states near the conduction band edge has a great influence on the low channel mobility. In this study, we have investigated a thermal activation process for the channel mobility in 4H-SiC MOSFETs. The MOSFETs were fabricated on p-type 4H-SiC (100) wafers. A gate oxide was grown by thermal oxidation in an oxygen and dry O$_2$ atmosphere, resulting in a thickness of $40$ nm. Electrical characteristics of the samples were performed by current-voltage and capacitance-voltage measurements at temperatures up to $250^\circ$C. Channel mobility and threshold voltages were determined from $I_d$/$V_d$ and $I_d$/$V_d$ plots using a $V_g$ in the saturation region. The channel mobilities in both dry and wet oxidized samples were less than 10 cm²/Vs at room temperature, and increased with increasing temperature. On the other hand, the threshold voltage decreased drastically as temperature is increased because the negative charges decreased at the SiO$_2$-Si interface. These measured activation energies for the channel mobilities were less than 0.1 eV. Thus, this suggests that the observed increase in the channel mobility with temperature is originated from the reduction of Coulomb scattering due to the activation of electrons from the interface state traps within 0.1 eV from the conduction band edge.

H5.38 INTERFACE EFFECTS ON THE RAMAN SPECTRA OF SiC/Si SUPERLATTICES. E.F. Bezzera, A.G. Souza Filho, J. Mendes Filho, V. Lemos, V. N. Freire, Departamento de Física, Universidade Federal de Ouro, Fortaleza, BRAZIL. Y. Ikoma, T. Kawanishi, M. Kawanishi, T. Hanaoka, Keio University, Yokohama, JAPAN.

Among the several polytypes, only the cubic 3C-SiC can be grown epitaxially on Si(100) substrate. The inverse heteroepitaxial growth of SiC on 3C-SiC was recently demonstrated by the use of a pulsed supersonic free jet technique, thus making it possible to obtain multilayer structures, whose interfacial regions were observed to have nanometric thickness by high resolution transmission electron microscopy measurements [1]. Here, we present calculations of the Raman spectra of (3C-SiC)$_n$(3C-SiC)$_n$(3C-SiC)$_n$(3C-SiC)$_n$ superlattices for several values of interface thickness, $\delta$, [in units of monolayers]. The dispersion relations were obtained using a linear chain model with the alloyed interface considered in the virtual crystal approximation. A modified bond-polarized tight-binding model was used to calculate the spectra. The analysis of the corresponding atomic displacements for the ideal superlattice allowed us to describe all the acoustic modes as extended through the whole superlattice. The optical modes, however, were seen to be localized as frequencies approached $\omega_{LO}$ for both optical modes, accidentally degenerated at $\omega = 518$ cm$^{-1}$ are quasiconfined in the Si layers. The modes occurring in the frequency range of 518-620 cm$^{-1}$ are quasiconfined in the 3C-SiC layers. Completely confined modes of the superlattices occur in the 800-1000 cm$^{-1}$. In the Raman spectrum of $\delta = 0$ superlattices the two dominant peaks are at $\omega = 518$ cm$^{-1}$ and $\omega = 969$ cm$^{-1}$ corresponding to the Si-Si and the 3C-SiC modes, respectively. Only very weak peaks were present in the Si layers, consistent with the existence of an interface region, however, several new peaks arise in this region, with increased intensity as the interface becomes thicker. For an interface thickness $\delta < 3$ some of these peaks have intensity comparable with the peaks originating from the superlattices. The appearance of the new peaks can be attributed mainly to modes confined in the interfacial transition regions, mainly. Y. Ikoma, T. Endo, T. Watanabe, and T. Motooka, Appl. Phys. Lett. 75, 2977 (1999).

H5.39 RAMAN SCATTERING AND DEPTH PROFILING ON EPIAXIAL SILICON CARBIDE STRUCTURES. Z. C. Feng, Institute of Materials Research & Engineering, SINGAPORE; L.T. Hwang, G. Kananm, S.J. Chen, National University of Singapore, Centre for Optoelectronics, K.P.J. Williams, G.D. Pett, Renishaw plc, UNITED KINGDOM.

In recent years, research and development on SiC have been greatly enhanced. Commercial 4H and 4H SiC bulk and epitaxial wafers are now available. To meet various electronic and optoelectronic applications it is needed to non-destructively assess the quality and properties of these structural wafers. In particular it is challenging how to evaluate the variation along the growth direction without damaging the wafer. In this report, we are focusing on developing the Raman scattering depth profile technique for its application in 4H/4H- and 6H/3H-SiC homo-epitaxial structures. By computer-automatically adjusting the sample stage, the laser focusing parameters can be changed to obtain the Raman spectra at different depth in the normal direction of the sample in the micrometer scale. The Raman scattering depth profiles of un-doped and doped SiC films of 4H- and 6H-SiC grown on homo-type substrate are acquired. Strong transverse and longitudinal optical (TO) phonons as well as the LO-phonon coupling modes are shown. Features from the heavily doped substrate and lightly doped epilayer can be distinguished through the shape, frequency and intensity of the A1 symmetry LO mode. Through the theoretical modeling and fitting of the LO-phonon coupling modes, the free carrier concentration can be determined at different depths. The doping variation in the film normal direction, therefore, can be obtained non-destructively. We have performed the Raman depth profile measurements on a series of 4H/4H- and 6H/3H-SiC samples and obtained the free carrier concentration and doping levels in the order of 10th power of 18 to 19 per cubic centimeters for substrate and 10th power of 16 to 17 for epilayer. These are consistent with the results measured by other methods. Further efforts are pursuing to raise the accuracy of this measurement technology.

H5.40 CHEMOMECHANICAL POLISHING AND RAPID THERMAL ANNEALING OF SiC: RAMAN SPECTROSCOPY AND ESCA (XPS) STUDIES. Bahram Rougheii, Unma Ramadass, Diana Phillips, Science and Mathematics Department, Kettering University, Flint, MI; W.C. Mitchell, and C.I. Nelsen, Air Force Research Laboratory, Materials and Manufacturing Directorate, Wright-Patterson AFB, OH.

Raman scattering and ESCA (XPS) studies on Nitrogen doped SiC samples revealed changes due to mechanical, chemomechanical polishing (CMP) and rapid thermal annealing (RTA) on surface and bulk properties of our samples. The SiC wafers were standard commercial grade 4H-SiC(67),C. M. L. West, in Materials Science and Engineering, Kyushu University, Fukuoka, JAPAN.

Among the several polytypes, only the cubic 3C-SiC can be grown epitaxially on Si(100) substrate. The inverse heteroepitaxial growth of SiC on 3C-SiC was recently demonstrated by the use of a pulsed supersonic free jet technique, thus making it possible to obtain multilayer structures, whose interfacial regions were observed to have nanometric thickness by high resolution transmission electron microscopy measurements [1]. Here, we present calculations of the Raman spectra of (3C-SiC)$_n$(3C-SiC)$_n$(3C-SiC)$_n$(3C-SiC)$_n$ superlattices for several values of interface thickness, $\delta$, [in units of monolayers]. The dispersion relations were obtained using a linear chain model with the alloyed interface considered in the virtual crystal approximation. A modified bond-polarized tight-binding model was used to calculate the spectra. The analysis of the corresponding atomic displacements for the ideal superlattice allowed us to describe all the acoustic modes as extended through the whole superlattice. The optical modes, however, were seen to be localized as frequencies approached $\omega_{LO}$ for both optical modes, accidentally degenerated at $\omega = 518$ cm$^{-1}$ are quasiconfined in the Si layers. The modes occurring in the frequency range of 518-620 cm$^{-1}$ are quasiconfined in the 3C-SiC layers. Completely confined modes of the superlattices occur in the 800-1000 cm$^{-1}$. In the Raman spectrum of $\delta = 0$ superlattices the two dominant peaks are at $\omega = 518$ cm$^{-1}$ and $\omega = 969$ cm$^{-1}$ corresponding to the Si-Si and the 3C-SiC modes, respectively. Only very weak peaks were present in the Si layers, consistent with the existence of an interface region, however, several new peaks arise in this region, with increased intensity as the interface becomes thicker. For an interface thickness $\delta < 3$ some of these peaks have intensity comparable with the peaks originating from the superlattices. The appearance of the new peaks can be attributed mainly to modes confined in the interfacial transition regions, mainly. Y. Ikoma, T. Endo, T. Watanabe, and T. Motooka, Appl. Phys. Lett. 75, 2977 (1999).
material of next generation. And SiC is called environment free semi-conductor material (heat, radiation, chemical and emission resistance). But, on manufacturing point of view, SiC is very tough material. Because, SiC has characteristics of very high physical hardness, and quite high chemical stability, it seems very tough to make micro-lithography onto SiC substrate. We use to reported several etching methods of SiC and showed possibility of micro-lithography, by photochemical reactions of CIF3 or NF3 gases. But, it is very difficult to handle those reaction gases. We developed a photo etching method of SiC, which is using hydrogen peroxide (H2O2) and hydrogen fluoride solution. We used a photo activated species, to run etching process easily and safely. Put small mount of mixed solution of hydrogen peroxide and hydrogen fluoride on SiC substrate then put sunshine window onto solution to make thin liquid layer above the SiC surface. KeF excimer laser beam was projected through patterned photo mask, vertically. The area where the laser beam was projected, activated oxygen was produced by photoysis of hydrogen peroxide. And also, SiC surface was excited by UV light from laser beam. Then activated oxygen was oxidized Si and C of excited SiC surface producing SiO2 and CO2. CO2 was released to the Air gas, but SiO2 was left on substrate. This produced SiO2 was etched by hydrogen fluoride, which exists in mixed solution. For example of our experiments, when 10,000 shots of KeF Laser, energy density was 600mJ/cm2 and mixture rate of solution was 10:1 (H2O2 : HF), etch depth was 40nm.

H5.42 REACTIVE ION ETCHING OF SiC USING CF3I/O3 INDUCED VIVELY COUPLED PLASMA Sung-Min Kim, Byung-Tae Lee, Chonnam National Univ, Dept of Metallurgical Engineering, Kwangju, KOREA.

Etching characteristics of n-type 6H-SiC and 4H-SiC using CF3I/O3 inductively coupled plasmas have been investigated as a function of ICP power, RF power, substrate bias (800W), substrate bias (800W), substrate bias (800W), substrate bias (800W), substrate bias (800W), substrate bias (800W), substrate bias (800W), substrate bias (800W), substrate bias (800W), substrate bias (800W), substrate bias (800W), substrate bias (800W), substrate bias (800W), substrate bias (800W), substrate bias (800W), substrate bias (800W), substrate bias (800W), substrate bias (800W), substrate bias (800W), substrate bias (800W), substrate bias (800W), substrate bias (800W), substrate bias (800W), substrate bias (800W), substrate bias (800W), substrate bias (800W), substrate bias (800W), substrate bias (800W), substrate bias (800W), substrate bias (800W), substrate bias (800W), substrate bias (800W), substrate bias (800W), substrate bias (800W), substrate bias (800W), substrate bias (800W), substrate bias (800W), substrate bias (800W), substrate bias (800W), substrate bias (800W), substrate bias (800W), substrate bias (800W), substrate bias (800W), substrate bias (800W), substrate bias (800W), substrate bias (800W), substrate bias (800W), substrate bias (800W), substrate bias (800W), substrate bias (800W), substrate bias (800W), substrate bias (800W), substrate bias (800W). The etch rate increased gradually with rf bias power and O2 concentration resulting in 200nm/min etching rate at the optimum condition of 800W ICP power, 800W ICP power, 40mTorr and 60% O2 concentration. The etching profile is highly isotropic and the etched surface of SiC was clean. Root-mean-square (RMS) roughness was 2 ~ 10 nm for etched SiC over wide range of etching conditions. Micron-scale etch rate and trenching effect were observed in the case of high bias power conditions. Recent at the LV test and AES analysis will be also discussed in the presentation.

H5.43 SURFACE CHARACTERIZATION OF 3C-SiC FILMS GROWN BY CVD ON Si(001) AND [211] SUBSTRATES B.A. Gravels, M.K. Graves, and J.T. Wolfe, Dave C. Swalm School of Chemical Engineering, Mississippi State University, Mississippi State, MS; M.R. Hedbон and S.E. Sadow, Emerging Materials Research Laboratory, Department of Electrical & Computer Engineering, Mississippi State, MS.

In this study the outermost atomic layer, near-surface region, and film substrate interface of amorphous thin 3C-SiC films grown on a 50nm (2.4μm) diameter Si(001) and 2 cm square Si(211) substrates have been investigated. Two sets of 3C-SiC films were investigated. First a carbonization process was used to create the film in a RF induction-heated horizontal atmospheric-pressure chemical-vapor-deposition (APCVD) reactor utilizing a propylene-hydrogen mix (3% CH3 is in ultrahigh purity hydrogen) was added to the carbonized layer to effect a 3C-SiC film via standard silane-propylene 3C-SiC growth methods [1]. Angle-resolved X-ray photoelectron spectroscopy (ARXPS), Auger-electron spectroscopy (AES) and ion sputtering spectroscopy were used to analyze the films. Chemical data identification, in-depth elemental distribution profiles and outermost atomic layer compositions of the thin-films are presented. Several structure sensitive techniques including atomic force microscopy (AFM), x-ray diffraction (XRD) in T-22 and T-Trocking curve measurements as well as low temperature photoemission (PL) and scanning electron microscopy (SEM) to examine crystal structure, surface morphology and film thickness where performed and will be presented [1]. E.S. Sadow, M.E. Okhaya, M.S. Meehan, M. Dudley, X.R. Huang, W. Huang and M. Shamsuzzoha, Proceedings of the Materials Research Society, Boston, MA, Nov. 1998.

H5.44 IRAS ANALYSIS OF THE EARLY STAGE OF THERMAL OXIDATION ON A SiC SURFACE Tomomi Kikumoto, Hidekazu Tsuda, Isao Kuma, Kunitaka Inuma, Central Research Institute of Electric Power Industry, Yokosuka Research Laboratory, Koganei, JAPAN.

To control the electrical properties of SiO2 film on SiC, it is important to understand the relationship between the structure of the SiO2/SiC interface and the electrical properties. In this study, we investigated the early stage of thermal oxidation of the SiC surface using infrared reflection absorption spectroscopy (IRAS). Experiments were carried out in the CIVF system with IRAS equipment. The base pressure was below 5 × 10^-6 Pa, and the dew point of oxygen used was -118°C. We compared IRAS spectra of oxide film formed on 6H-SiC(001) and Si(100). The varying thickness of the oxide layer was obtained by adjusting the oxidation time. In the case of oxide films on 6H-SiC(001), the LO mode (at 1250 cm^-1) of Si-O-Si stretch vibration is almost constant with increasing oxide thickness from 0.5 nm to 2 nm. On the other hand, the LO mode for the oxide layer on a Si(100) surface become lower with decreasing oxide thickness. These results indicate that there is considerable difference in the optical constant near the interface between a thermally grown oxide layer formed on SiC and one formed on Si.

H5.45 CHEMICAL AND ELECTRICAL ANALYSIS AT THE SILICON DIODE - SILICON CARBIDE INTERFACE K.J. Chung, L.M. Porter, Carnegie Mellon University, Department of Materials Science and Engineering, Pittsburgh, PA; Q. Wu, Linköping University, Department of Physics, Linköping, SWEDEN.

The ability to grow stoichiometric SiO2 on SiC by thermal oxidation is an important advantage for the development of metal-oxide-semiconductor field effect transistors (MOSFETs), which are important devices for high power and high frequency applications. However, high interface state densities are associated with the low channel mobilities in these devices. Thermal oxides were grown on n-type 6H-SiC(001) at 1100°C in a wet oxygen ambient for 4 hrs after cleaving the substrates using the simple RCA cleaning process. High carbon concentrations at distal regions at severe thermally-grown SiO2/6H-SiC(001) interfaces have been detected by electron energy loss spectroscopy (EELS). The interface state density (Dit) in metal-oxide-SiC(100) (Dit = 7x10^12 cm^-2 eV^-1). In contrast, carbon rich regions were not detected from EELS analysis of thermally-grown SiO2/SiC interfaces nor of plasma CVD-deposited SiO2/SiC interfaces. Moreover, layers adjacent to the thermally-grown SiO2/SiC interface were found to be silicon-rich by EELS. The C/Si ratio and the change in stoichiometry may be associated with the higher than desirable interface state densities and the low channel mobilities in SiC-based MOSFETs. Different processing conditions, including chemical and plasma cleaning of the SiC surface, have been investigated. The effect of these conditions on the composition and electrical properties of the interface will also be presented.

SESSION H6: IMPLANTATION/RADIATION DAMAGE

Chair: Mirek Skowronski and Roustam Yikimov
Wednesday Morning, November 29, 2000
Room 202 (Hyne)

8:30 AM H6.1 ION IMPLANTATION FOR SILICON CARBIDE ELECTRONIC DEVICES. Michael A. Capone, Purdue University, School of Electrical and Computer Engineering, West Lafayette, IN.

As the demands on electronic systems intended for high temperature, high power or high frequency operation increase, silicon-based electronics are being pushed to their fundamental material limits. Consequently, continued improvement in system level performance for these applications requires new semiconductor materials. Silicon carbide (SiC) is a candidate material for the applications listed above, but considerable materials, processing, and device research is still needed. This presentation focuses on ion implantation processing of SiC, and attempts to illustrate specific problems associated with ion implantation and how they may be solved. Data from a series of experiments relevant to SiC MOSFETs are presented for this purpose. Ion implants into SiC are discussed first to show how a strategy for improving the acceptor activation ratio from less than 1% to nearly 100% is developed. The annealing temperatures (1000°C) needed to attain high activation ratios lead to severely roughened surfaces. Results from experiments designed to present new ion implantation techniques have been encouraging from a purely materials perspective. Atomic force microscopy data to be presented will demonstrate low surface roughness following high temperature annealing. However, these results have not translated into improved transport characteristics for SiC MOSFETs. An investigation of inversion layer mobility in 4H-SiC MOSFETs will be presented to illustrate this point and close out the talk.
9:00 AM H6.2 STRUCTURAL DEFECTS IN ION IMPLANTED SiC. Per O. Persson, Lars Holtman, Thin Film Physics Division, Dept of Physics, Linköping University, Linköping, SWEDEN.

For the purpose of producing SiC planar devices, selective area doping is necessary. The choice of technique today is mainly ion implantation. The implantation process damages the crystal by inducing vacancies and interstitials from collisions between the implanted ions and the lattice. The implanted ions predominantly occupy interstitial lattice sites where they are electrically inactive. To activate these and to restore the implantation induced damage, the sample is subject to thermal annealing. Studies show that annealed SiC samples, irradiated by a dose of ions slightly lower than the amorphization threshold, contain structural defects. It is the intention of this paper to present results on studies of the evolution of these defects after high temperature annealing. In the present study samples of different implantation, 12 series of samples were investigated, using a series of different implants, respectively, at energies ranging from 100-200 keV. Most samples were subject to annealing studies, in which the annealing time and temperature was varied. The samples were studied by DELS, cross sectional and Phra-view TEM. At low temperature implantations, the entire volume affected by the implantation contains damage loops. However, after implantation at elevated temperatures only the volume in which the dopant concentration is above a threshold level (21-18) contain loops. It was concluded that the dislocation loops contain self-interstitials. These originate from a supersaturation of excess interstitial atoms, which are created in a process where an implanted ion occupies a substitutional site, after having kicked out a native atom and thereby forming a self-interstitial, according to the 1 model. It is shown that when an implanted sample is annealed the excess interstitials start to cluster. As soon as equilibrium between point defects and vacancies has been established, the excess clusters have been observed according to the Ostwald ripening theory for planar precipitates, with an activation energy of 5.7 eV.

9:15 AM H6.3 MULTI-AXIAL CHANNELING STUDY OF DISORDER IN GOLD IMPLANTED 6H-SiC. W. Jiang, W. L. Weber, S. Thevuthasan, V. Shatsevandian, Pacific Northwest National Laboratory, Richland, WA.

A single-crystal wafer of 6H-SiC has been implanted in different areas with 2.0 MeV Au ions to low fluences of 0.01, 0.1 and 0.2 ions/cm² at room temperature. This experimental condition was selected in order to produce low-level disorder, thus avoiding significant lattice strains from occurring in the implanted crystal. The disorder on both the Si and C substrates has been analyzed using in-situ Rutherford backscattering spectrometry combined with nuclear reaction analysis along <001>, <10T1> and <11T2> axial channeling directions. Depth profiles of the implantation-induced disorder, as measured along the three axes, will be quantitatively compared and possible mechanisms for point defect formation will be discussed. Thermal annealing experiments at 570 K (20 min) for the implanted samples show different recovery rates, as viewed along the different axes. A comparable minimum yield for the Si and C substrates in both axes are found. Post-implantation analysis has been observed along <001>, while a higher value on the C substrate has been observed along <11T2>. In addition, the half-widths of the angular profiles around the three axes appear to become smaller as a result of the Au implantation. The results along with detailed analysis will be presented and discussed.

9:30 AM H6.4 DEFECT STRUCTURES IN NEUTRON IRRADIATED 6H-SiC STUDIED BY X-RAY DIFFRACTION LINE PROFILE ANALYSIS. Christoph Seitz, Andreas Mieger, Kristalllographie und Strukturphysik, Univ of Erlangen-Nuremberg, Erlangen, GERMANY; Hans-Heinrich Hellig, Angewandte Physik, Univ of Erlangen-Nuremberg, Erlangen, GERMANY.

Nuclear transmutation by neutron irradiation can be applied to dope SiC by phosphorus. This method is useful to achieve a homogeneous doping in large crystal volumes. As a disadvantage, however, radiation induced defects occur, mainly by high energy neutrons. We have investigated in detail the peak shape of several Bragg reflections in irradiated 6H-SiC samples by high resolution X-ray diffraction. The effects of different neutron fluences, neutron spectra and annealing treatments have been studied. A detailed line profile analysis demonstrates a clear correlation of the defect densities of second kind with the measured line profiles. Procedures for the determination of the defect densities and of the density change of the defects on annealing have been developed. Further qualitative information on crystal damage is obtained from x-ray diffusivity, a technique which allows to determine quantitatively the diffusivity and to elucidate a change of the character of the defects on annealing. Further qualitative information on crystal damage is obtained from x-ray diffusivity. A new method for the determination of the density change of the defects on annealing has been developed based on the knowledge of the density change of the defects on annealing. A new method has been developed based on the knowledge of the density change of the defects on annealing. We find that the pronounced diffuse scattering in irradiated samples becomes largely reduced and that 001 Bragg peaks may be split after high temperature annealing cycles.

9:45 AM H6.5 ELECTRON IRRADIATION OF 4H SiC: AN OPTICAL STUDY. W. G. Smith, P. O. A. Persson, J. P. Bergman, E. Janánek, Department of Physics and Measurement Technology, Linköping University, Linköping, Sweden; Geraint Evans, J. W. Seely, Department of Physics, University of Bristol, Bristol, UK.

We present an optical study of the defects created by low energy electron irradiation from a TEM, using photoluminescence (PL) and time resolved measurements techniques. The motivation for this work is to obtain a better understanding of the defect spectra, seen immediately after irradiation and even ion-implantation. Recently, a report [Ref:1: T. Egilsson et al., Phys. Rev. B 50, 80008 (1999)] on PL of 4H-SiC irradiated with 2MeV electrons, showed multiple series of peaks, of which Al, Si and C defects were due to excitonic recombination at isoelectronic centers related to silicon vacancies. By using a 20000 eV TEM as the irradiation source in our study, we aimed to displace only the atoms in the carbon sublattice. A low-doped 4H-SiC epilayer was irradiated for 8hrs with the TEM resulting in an electron dose of about 10¹⁴ cm⁻², which is the same dose as was used in ref.1. Low temperature PL measurements show the presence of at least seven series of lines. The luminescence decay times were measured at 2K for all the series of lines and varied from a 0.5 to 625 micro-seconds for the lines identified with transitions from the ground states of the bound excitons and from 0.3 to 7 micro-seconds for the excited state. Such a long lifetime is indicative of recombination at isoelectronic centers. In addition, the observation of excited states with relatively long lifetimes, indicates a slow relaxation process between the excited state and the ground state. The most interesting candidate, associated with the silicon vacancy are not observed in our epilayer which supports our assumption of displacement of atoms in only the carbon sublattice. Results on epilayers irradiated with different electron energies along with the annealing behavior of these defects will be presented.

10:00 AM H6.6 UNDERSTANDING AND CONTROL OF RADIATION DAMAGE OF 4H AND 6H SiC. John Seides, Francesca Ceresolla, Geraint Evans, Madhahir Ismail, Wolfgang Voegeli, Physics Department, University of Bristol, Bristol, United Kingdom.

We have used a 300 keV transmission electron microscopy to carry out small area, voltage controlled, temperature controlled, near-threshold, electron displacement damage of 4C, 4H, 6H and 15R SiC. After irradiation the samples were examined by low temperature photoluminescence microscopy employing 325 nm and 488 nm lasers, to arrive at a new understanding of the radiation damage processes that occur in these materials. Studies have included both n- and p- doped materials, epilayers and substrates from a number of different sources. Carbon displacements have been distinguished from silicon displacements by choice of the accelerating voltage used. At voltages above 180 kV silicon, while carbon, is displaced with only 30% of the displacement and carbon displacements, by accelerating voltage, is down to 90%. Diffusion of the point defects, created during irradiation, outside of the irradiated region has been measured by photoluminescence imaging using Renishaw micro-Raman system fitted with Oxford Instruments cryogenic stages. Annealing characteristics have been studied independently for the two different sublattice elements. Regions of polytype non-uniformity in 4H and 6H SiC have been mapped out and other inhomogeneities have been identified. Some of the samples studied had been implanted with high energy nitrogen ions and annealed at high temperatures. These exhibited the well-known D2 luminescence. By appropriate subsequent electron irradiation of these implanted samples a procedure has been worked out to eliminate the D2 luminescence.

10:45 AM H6.7 DEFECTS IN 6H SiC AND 4H SiC INDUCED BY HIGH ENERGY HELIUM IMPLANTATION. Evarist Oliviero, Marie France Beaufort, Alain Declercq, Jean Francois Barbot, Laboratoire de Metallurgie Physique, UMR 6693, Futuroscope-Chasseneuil, FRANCE, Eider Naczewski, Gilbert Blonder, CBRI CNRS, Orleans, FRANCE.

Convergent Beam Electron Diffraction (CBED), high energy electron diffraction and X-ray diffraction have been used to study the defect formation in crystalline-type 6H SiC implanted at high temperature with helium at a dose of 2×10¹⁸ cm⁻² at 1.6 MeV, following an anneal at 800°C for 30min. In contrast to what was observed in silicon, the damage layer did not show any bubble formation but consists in a dislocation array of 10 nm in diameter. This layer is surrounded by a strong contrasted zone which is impossible to solve using conventional microscopy (TEM). A
run of CHED patterns from the surface toward the bulk along the [0001] direction followed by the analysis of the distortion of the Holz lines contrast changes of the perturbed zone is between 3 and 44 µm. X-ray diffraction experiments (α-6q), a shoulder is present in the low angle side, which result to the dilution of about 1% of the c-axis lattice. These results are discussed and compared to the defect formation in crystalline n-type 4H-SiC implanted with helium at a dose of 10^13 cm^-2 at 1.6 MeV. In the last case a continuous damage layer of 766nm width is observed which can be divided in three different regions. With the central band consisting of an amorphous area and a lot of small bubbles (1-2 mm in diameter). The study is still in progress.

11:00 AM H6.8
CHARACTERIZATION AND MODELING OF p-TYPE 4H-SiC IMPLANTED SURFACES. Yu Zeng, Warren Welch, Marvin H. White, Lehigh University, Sherman Fairchild Center, Bethlehem, PA.

In recent years, a considerable amount of work has been performed on Silicon Carbide (SiC) MOS devices; however, much of this work has focused on the characterization of epitaxial SiC layers. Since MOS devices, such as DMSOS and IGBTs, employ implanted regions, an understanding of the implanted, p-type, SiC surface is imperative. The purpose of this work is to examine the influence of ion implantation and high temperature activation anneals on n-type SiC surfaces. Lightly-doped, p-type epitaxial layers on n-type 4H-SiC substrates have been implanted with aluminium to form shallow, highly doped, p layers, which are annealed at temperatures ranging from 1100°C to 1400°C. These implanted layers are characterized by capacitance-voltage (C-V) and conductance (G-V) measurements, a supply of inversion layer carriers is provided and the implanted G and C-V measurements are used to determine activation percentage and interface trap densities.

11:15 AM H6.9
SELECTIVE ETCHING OF 4H-SiC BY ALUMINUM/BORON CO-DIFFUSION. Ying Guo, Shunsuke Nishio, Xinbin Wang, Vojin Magandragi, Tadashi Shishikawa, Univ of South Carolina, Dept of Electrical Engineering, Columbia, SC.

Selective doping plays a significant role in semiconductor device fabrication. Due to the lack of a suitable active mask for thermal diffusion, selective doping is currently realized by ion implantation followed by high temperature annealing to reduce the lattice damage and obtain reasonable percentage of electrical activation of impurities. However, the inherent drawbacks of ion implantation limit the potential features offered by SiC. Using a high temperature mask developed in our laboratory we have successfully fabricated pn diodes based on selective boron diffusion. The good rectification characteristics confirmed the feasibility of this process except that the forward voltage drop is much larger due to high ionization energy (340 mV) of boron acceptor. On the other hand, Al has lower ionization energy (200 mV) and diffusion coefficient compared to B. This is why we have more selective co-diffusion of boron and aluminum in order to form a shallow p⁺-layer (Al) and a deep, linearly graded p⁺-layer (B) simultaneously. A vertical double wall water-cooled quartz chamber with inductive heating was used to realize the diffusion process. The diffusion temperature was varied from 1800 to 2100°C. Graphite film was deposited on the sample surface as protection mask to provide selectivity of the doping process. A mixture of elemental boron, aluminum, silicon and carbon powder was used as the source of dopants. Cathodoluminescence and photoluminescence measurements were done to identify the local doped regions. Anodic oxidation technique combined with the Hall measurement as well as SIMS were employed to confirm the acceptor concentration profiles. The existence of the intrinsic layer due to boron compensation is confirmed. I-V characteristics of the pn diodes based on both B and Al co-diffusion are compared.

SESSION H7
METALIZATION/CHARACTERIZATION. Charles, Michael A. Cushing and Gerard Fenaal
Wednesday Afternoon, November 29, 2000
Room 202 (Hynes)

12:30 PM H7.1
MECHANISMS FOR OHMIC CONTACT FORMATION TO SILICON CARBIDE. Lim S. Porter, Taeoon Jung, Carnegie Mellon University, Dept of MSE, Pittsburgh, PA.

The fabrication of reproducible ohmic contacts with low contact resistivities to p-type SiC is a critical problem for many devices. The traditional approach of annealing an Al-contact (e.g. TiAl) on highly-doped SiC at 900-1000°C. Another approach employs one or more Si layers along with a transition metal to react with the Si and C in the substrate in equal ratios. We have investigated thin (~100 Å) Si interlayers and metal overlayers with microstructural, chemical and electrical characteristics. Both the structure and resulting chemical phases formed with the metal overlayers depend on the deposition and annealing temperature, and these in turn affect the quality of the ohmic contacts. Because the homogeneity of the interface affects the reproducibility of the contacts, it is important to control the interfacial morphology and the extent of chemical reaction. In this study we deposited transition temperatures varied from R.T. to 500°C and annealing temperatures from R.T. to 1000°C. The electrical behavior ranges from strongly rectifying to ohmic, while the microstructure ranges from amorphous to crystalline as a function of the deposition and annealing temperatures. The interfacial homogeneity also depended strongly on the processing conditions. The correlations observed among the electrical, microstructural and reaction characteristics will be presented along with the implications for fabricating reproducible ohmic contacts to SiC.

2:00 PM H7.2
TITANIUM/TUNGSTEN (TiW) METALS FOR OHMIC CONTACTS TO p-TYPE 4H-SiC. S.-K. Lee, C.-M. Lee, KTH, Royal Institute of Technology, Department of Electronics, Kista, SWEDEN.

Metal-semiconductor contacts have many considerable interests in developing devices for high power, high temperature, and high frequency applications using a wide bandgap semiconductor. For p-type contacts, very few works have been reported for both Schottky and Ohmic contacts to p-type 4H-SiC. We have recently reported and proved that both n- and p-type TiW Schottky contacts had excellent rectifying characteristics after annealing at 500°C with a thermally stable ideality factor of 1.08 and the Schottky barrier height of 1.22 and 1.93 in the range of 34-300°C using IV and C-V characteristics [n- and p-type respectively, J. Appl. Phys. vol 87, p 8039 (2000)]. In this work, we extensively investigated sputtered titanium tungsten (TiW) contacts for both Schottky and Ohmic contacts to p-type 4H-SiC. We achieved an average contact resistivity (ρc) of 4x10^-5 cm² and sheet resistance (Rs) of 1.35 kΩ/sq. from the linear TLM measurements after 980°C 6s RFA. Epitaxial layers with a doping concentration of 1x10^16 6x10^16 cm^-3 were used, as well as Al ion implanted samples (700°C implant, 1700°C anneal) with a dose of 3x10^14 cm^-2 and an energy of 180keV. We found some variation of the specific contact resistance and the sheet resistance from our TLM measurements. We will discuss this variation behavior with the measurement of BVS. RBS measurement was also performed to analyze Ti and W composition, thickness of TiW, and reaction at the interface for as-deposited and 980°C annealed contacts.

2:15 PM H7.3
ENGINEERING THE AL-TI OHMIC CONTACT TO p-SiC FOR OPTIMAL PERFORMANCE. Je-Yi Lin, S.E. Mohney, The Pennsylvania State University, Materials Science and Engineering, University Park, PA; J. Crofton, Murray State University, Department of Physics and Engineering Physics, KY; J.R. Williams, T. Isaac-Jones, Auburn University, Department of Physics, Auburn, AL.

Al-Ti alloys are widely used as ohmic contacts to p-type SiC. Until our study was performed, however, little was known about the performance of these contacts as a function of composition. We have examined alloy compositions with 90, 70, 60, and 19 weight % Al. Only the compositions with 90 and 70% Al provided ohmic contacts to p-SiC (p = 7 x 10^18 cm^-3) after annealing at 1000°C. Interestingly, the Al-Ti alloy containing the composition that provided ohmic contacts had Al present as a liquid phase during annealing. The Al present in the more Ti-rich contacts was in high melting point aluminum carbides. Upon removing the annealed contacts with a chemical etchant and examining the exposed SiC surface with scanning electron and atomic force microscopies, we found that the ohmic contacts had non-uniform metal/semiconductor interfaces. On the other hand, the non-ohmic contacts with 60% Al had much smoother interfaces. Specific explanations for these research results will be presented. From the point of view of reproducibility, we further found that the alloy with 70% Al is the best. Finally, in past work we have observed that the composition of the contact changes during annealing due to evaporation of Al. To allow the use of Al, we have explored the use of a conductive chromium oxide cap during annealing. Electrical and materials characterization of the Al-Ti contacts annealed with the caps will also be presented.
230 PM H7.4

Based on its thermodynamic compatibility and other properties, TaC with one or more metallic overlayers was investigated as a thermal stability contact to 6H-SiC. As expected, high resolution transmission electron microscopy (TEM) analyses revealed no reaction between TaC and SiC after annealing at 1000°C for 15 min, to form an ohmic contact. After annealing at this temperature, the average specific contact resistivity (SCR) of TaC contacts with W/VC overlayers was 6.5×10^{-8} Ω·cm² on 7.5×10^{-3} Ω·cm doping level. The SCR of these samples remained constant within the experimental error after annealing at 800°C for 100h. Significant increases in the SCR were not observed until the samples were annealed at 1000°C for a few hundred hours. Electrical measurements were correlated with microstructural and chemical analyses of the W/VC/TaC/SiC contacts to understand the conditions associated with both the stability and degradation. The stability of the contacts at elevated operating temperatures (to 1000°C) was also measured. Changes in the electrical characteristics coincided with decomposition of the WC layer as a result of annealing at 1000°C for 60 h.

Investigation of the W/VC/TaC/SiC interface by conventional and high resolution TEM with electron energy loss spectroscopy (EELS) indicated that a reaction between the layers had occurred. Little reaction of the film with the SiC substrate was observed; however, atomic-scale resolution seemed to be concentrated adjacent to grain boundaries in the reacted film. From Auger and SIMS depth profiles, it was also found that incorporation of O (as a function of annealing conditions) affected the electrical properties of the TaC-based contacts. These implications on the development operating limits for SiC high temperature devices. Distinctions between the two main stability factors will be presented through correlations of the electrical measurements with the reactions and oxygen incorporation in the film.

245 PM H7.5
THERMOCHEMICAL CONSIDERATIONS FOR THERMALLY STABLE CONTACT METALLIZATION ON CRYSTALLINE SiC. Robert S. Kojieč,1 Dorothy Lokcoč,2 Carl Salgado,3 David Spiry,3 and Jeff Krohnen3
1NASA Glenn Research Center, Instrumentation and Controls Division, Cleveland OH; 2AYT Corporation; 3Akima Corporation, Fairview, PA.

In high temperature and extreme vibration environments, which are typical in aerohydrodynamic propulsion systems, the device contact metallizations undergo irreversible microstructural changes that even under relatively low thermal stress. These failure mechanisms include interdiffusion between different metal layers, contact oxidation, and thermomechanically induced phase transformations. As a result, the contact metallization becomes a fundamental requirement. The thrust of this work is to develop an in-depth understanding of thermodynamic issues in high temperature contact metallization schemes being developed at NASA-Glenn. As a result of this effort we have developed a thermodynamically stable Ti (1000°C)/TaSi2 (200°C)/Pt (3000°C) high temperature metallization on both 4H and 6H-SiC. The diffusion barrier mechanisms allow specific contact resistance values of (10^5-10^6) Ω·cm and Schottky barrier heights (SBH) to remain practically constant after heat treatment in air at 600°C for over 500 hours. Scanning electron microscopy (SEM) used to evaluate the surface morphology of the contact metallization revealed a network of two-dimensional oxidation growth patterns as a function of time at temperature. Analysis spectroscopy (AES) enabled identification of three diffusion barrier mechanisms. One is the decomposition of TaSi2 and subsequent outward migration of silicon during thermal treatments in nitrogen forming a silicide of platinum, which provides critical protection against oxygen transport. The second is the formation of titanium silicide adjacent to the decomposed TaSi2. The third is the formation of quasi-epitaxial titanium carbide on the new interface with silicon carbide after the initial nitrogen anneal, as revealed by High-resolution transmission electron microscopy (HRTEM), similar to that observed in [1].

Theoretical analyses of the thermochemical reactions at the free surface and the metal/SiC interface indicate that diffusion-limited mechanisms prevail, thereby implying parabolic growth rates. Using the Demco-Grove [2] and Niclot-Bartur [3] approximations at the free surface and metal/SiC interface respectively, parabolic reaction rates after fifty hours at 800°C for silicon oxide (3.1×10^{-11} cm/s), titanium silicide (3×10^{-12} cm/s), and tantalum silicide (1.78×10^{-12} cm/s) formation are obtained. The theoretical model appears to correlate well with experimental data. Detailed results will be presented.


3:00 PM H7.6

SiC is a promising semiconductor material for high power and high temperature device applications. It has been reported that most SiC based electronic devices which can not sustain a long-term operation at an elevated temperature and/or power level suffered deterioration of their metal/SiC contacts. Thus, formation of low resistance Ohmic contacts with good thermal, chemical, and mechanical properties is important for realizations of SiC electronics. Ni/SiC Ohmic contacts to n-SiC are widely used and have been deemed the industry standard due to their reproducible low specific contact resistance. Fabrication of Ni Ohmic contacts requires a post deposition high temperature anneal in order to form Ni3Si and achieve Ohmic behavior. Unfortunately, the annealing process causes carbon accumulation at the metal-SiC interface and throughout the metallization layer, contact broadening, poor interface morphology laden with Kirkendall voids, and substantial roughening of the contact surface. These features are detrimental to device reliability and will ultimately lead to device failure after exposure to long term high power and high temperaturedevice operational stresses. In order to retain the low specific contact resistance and suppress the undesirable characteristics of Ni Ohmic contacts we have directly deposited Ni3Si, the thermodynamically stable interface phase between Ni and SiC, onto (0001) 6H-SiC. The material properties of the Ni-deposited and annealed Ni3Si-SiC contacts were quantitatively assessed via AFM, FESEM, AES, RBS, and TEM. The reliability of this contact metallization in response to pulsed high power switching, was assessed via ac pulse thermal fatigue testing. Our results demonstrated that the Ni-deposited and 700°C annealed contacts were non-Ohmic, while the 500°C annealed contact exhibited excellent Ohmic behavior. All samples possessed smooth surface morphologies and abrupt metal-SiC interfaces. The electrical, compositional, and structural integrity of the contact-SiC interface suffered minimal degradation after exposure to pulsed thermal fatigue testing. Details of the aspects of contact formation and the results of the pulsed thermal fatigue testing will be presented and discussed.

3:45 PM H7.7
COMPARISON OF F plasma CHIMESTRY FOR DEEP ETCHING OF SiC. K.P. Lee, Univ of Florida, Dept of MSE, Gainesville, FL; P. Ranganathan, Bell Labs, Lucent Technologies, Reading, PA; S.J. Pearson, Univ of Florida, Dept of MSE, Gainesville, FL; P. Ren, Univ of Florida, Dept of Chemical Engineering, Gainesville, FL; S.N. Chiu, Bell Labs, Lucent Technologies, Murray Hill, NJ; C.-M. Zetterling, Royal Institute of Tech. [KTH], Dept of Electronics, Kista, SWEDEN. *Current address is Lucent Technologies, Reading, PA.

A number of F2-based plasma chemistries (NF3, SF6, PF5, BF3) were investigated for high rate etching of SiC. The most advantageous of these is SF6, based on the high rate (0.6 mm/min1) it achieves and its relatively low cost compared to NF3. Changes in electrical properties of the new-surface region are relatively minor when the incident ion energy is kept below approximately 75 eV. At a process pressure of 5 mTorr, the FIC etch rate falls off by ~15 % in 30 μm diameter holes compared to larger diameter holes (~60 μm diameter) or open areas on the mask.

4:00 PM H7.8
STRUCTURE AND DYNAMICS OF SILICON CARBIDE SURFACES FROM FIRST PRINCIPLES SIMULATIONS. Galia Gali, Lawrence Livermore National Laboratory, CA; Alessandra Castellani, MAESTRO, Parma, ITALY; F. Gigi, Lawrence Livermore National Laboratory, CA.

Using first principles molecular dynamics, we have studied the structural and electronic properties of SiC(0001), [01-5] and zero and finite temperature. In particular, we have investigated different reconstructions of Si-terminated [3-4] and C-terminated [1,5] SiC(0001), focusing on how the presence of stress and defects can influence the surface structure. Furthermore we have studied the deposition of nitrogen on SiC(0001), to investigate the early stages of nitride growth on silicon carbide [6], and we have simulated the structural properties of an amorphous silicon carbide surface [7]. A zero and finite temperature analysis of the results will be presented, with focus on the comparison between ab-initio calculations and recent photocemission and STM experiments.
Optical Anisotropy of the SiC(001) Surface: Evidence for the Two-Dlayer Asymmetric Dimer Model

4:15 PM H7.0

Much attention has recently been focused on the properties of SiC growth planes, for both fundamental reasons and due to their technological importance. The SiC(001) surface, exhibiting three major surface phases, (2x2), (1x1), and (3x2), serves as a prototype in that respect. It has been intensively investigated by both experiment and theory. However, despite considerable efforts, the atomic structures of these surface phases are still not clear. This holds in particular for the Si-rich (3x2) reconstruction, which results from Si adsorption on the Si-terminated SiC substrate. To our knowledge, no less than four reconstruction models have been suggested, namely the single dimer row model (SDRM), the alternate dimer row model (ADRM), the double dimer row model (DDRM), and the two-dlayer asymmetric dimer model (TADDM). First-principles calculations of the energetics of this surface give contradicting results and no experiment thus far could either prove or disprove any of the above models. The present work aims at resolving these controversies by computing the reflectance anisotropy spectra from first principles and comparing the calculated results with experimental data. All of the four candidate models were considered. The results for the TADDM give two main peaks and one dip in the experimental energy window, which is in very good agreement with experimental data. The other three models, SDRM, ADRM, and DDRM, lead to negative features in the anisotropy spectra that are not observed in experiments. The surface structures that dominate the optical anisotropy signal have been identified in each case, providing a detailed picture of the origin of optical anisotropy for this surface. The present results show that a combination of optical anisotropy measurements and calculations can be used to determine the atomic reconstruction patterns for complex, severely reconstructed surfaces.

4:30 PM H7.10

Behavior of Aluminum and Nitrogen in Compensated 4H-SiC Epitaxial Layers


Silicon carbide (SiC) is a recognized wide bandgap semiconductor for high-power, high-frequency, and high-temperature electronics. For p-type layers aluminum is used as dopant since it gives a shallow acceptor level. In growth of n-type layers aluminum may be unintentionally introduced from the growth environment. Nitrogen is always present to some extent and creates a shallow donor level. Compensation makes the property control more complicated. We have studied epitaxial layers containing aluminum and nitrogen. The aluminum concentration was in the range 1E15 to 1E18 atoms/cm² and nitrogen was in 1E16 order. Impurity concentrations were determined by secondary ion mass spectrometry. Electrical, low-temperature photoluminescence, and cathodoluminescence techniques have been used for studying the epilayers. The samples were grown by sublimation epitaxy with growth rates from 50 to 100 μm/h in the temperature range of 1750 to 1800°C. We report a comparative study on the influence of compensation on luminescence of bound excitons and A:N donor-acceptor pairs in n- and p-type 4H-SiC. Photoluminescence measurements of the luminescence from nitrogen bound excitons is sensitive to the aluminum concentration in the epilayers. The intensity of nitrogen bound excitons decreases with increasing aluminum concentration while the intensity of aluminum bound excitons increases. The ratio of the N bound exciton to A:N phonon lines to the aluminum bound exciton lines shows a proportional dependence to the aluminum concentration. This is more clear in n-type samples. The compensation level was evaluated from C-V measurements and knowledge of acceptor and donor concentrations. Cathodoluminescence was used to analyze donor-acceptor pair emission around 420 nm which is commonly related to the presence of aluminum and nitrogen in SiC. An effect of compensation on the optical properties of 4H-SiC epilayers is demonstrated. The results from the characterization techniques are combined for further understanding the complex interplay of aluminum, nitrogen and boron in compensated material.

4:45 PM H7.11

Deep-Level Luminescence at 1.0 eV in 4H SiC.


We have studied the infrared luminescence around 1.0 eV from an unidentified defect center, which we label UD-1, found in our nas-grown high-temperature CVD 4H SiC samples. The grown material is transparent and usually has high resistivity, even when it is not intentionally doped with vanadium. The UD-1 luminescence has a similar intensity as the vanadium-related luminescence at 0.75-0.85 eV. Some other sharp luminescence lines (UD-2 at 1.1 eV, UD-3 at 1.35 eV) are usually also observed in the infrared region but not so strong as the UD-1 and vanadium. We tentatively ascribe the high resistivity of the material as due to the UD-1 defect.

The luminescence of the UD-1 consists of three sharp no-phonon lines at 0.894, 1.000 and 1.001 eV. In this report we will present the optical properties in more detail together with the electronic structure of the center. The results are to a large extent based on Zeeman measurements in the range from 0 to 5 T and on photoluminescence (PL) measurements using below bandgap excitation. The measurements allow us to make a rough estimate of the ground-state level of the center in the bandgap by varying the excitation energy.

The UD-1 center is never observed in our systematic annealing studies of electron irradiated pure CVD layers. However, in commercial substrates the UD-1 center is present before but not after irradiation unless the substrates are annealed (≥ 750°C). This behavior suggests that the UD-1 center is related to impurities rather than to intrinsic defects.