SYMPOSIUM A

Materials Issues in Novel Si-Based Technology

November 26 - 28, 2001

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*Invited paper
SESSION A1: GROUP IV ALLOY AND STREAINED MATERIALS AND DEVICES
Chair: James C. Monday Morning, November 26, 2001 Room 202 (Hynes)

8:30 AM #A1.1
STRAINING Si/SiC/SILICON GERMANIUM MATERIALS AND DEVICES. Judy L. Hoyt, Microsystems Technology Laboratory, Dept. of EECS, Massachusetts Institute of Technology, Cambridge, MA.

MOSEFTs fabricated on tensil strained Si layers grown on relaxed SiGe exhibit significant enhancements in electron and hole mobility, and current drive, at a given channel length. Such devices are promising candidates as a means of extending the performance limits of silicon MOSFETs, for both digital and analog applications. However, challenging materials and process integration issues remain, including those associated with the relaxed SiGe layer itself. Several groups have recently pursued the formation of relaxed SiGe on insulators, which has the potential to provide the advantages associated with Si on insulator (e.g., reduced capacitance), while simultaneously improving integration issues associated with the thick relaxed SiGe layer. Simplified device isolation and reduced junction leakage currents are expected for strained Si MOSEFTs fabricated on relaxed SiGe on insulator. After a brief review of strained Si MOSEFTs, the formation of relaxed SiGe on insulator by bonding and H determination, and etch back techniques will be reviewed. Preliminary results indicate that the electron mobility in strained Si MOSEFTs fabricated on such material matches that obtained for devices fabricated on thick relaxed SiGe layers. Key device processing issues associated with strained Si MOSEFTs, such as diffusion of dopants in relaxed SiGe on insulators, and silicide formation will also be discussed.

9:00 AM #A1.2
STABILITY OF STRAIN ON RELAXED Si,-, Ge, BUFFER LAYERS. P.M. Mooney, S.J. Koester, J.A. Ott, J.O. Chu, and J.L. Jordan-Sweet, IBM Research Division, T.J. Watson Research Center, Yorktown Heights, NY.

Strained Si/SiGe is of interest for future generations of CMOS technology, since both electron and hole mobility is enhanced in Si under biaxial tensile strain. The thermal stability of strained Si layers grown on relaxed SiGe buffer layers was investigated using high resolution x-ray diffraction, micro-Raman spectroscopy and planar view transmission electron microscopy (TEM). The samples, consisting of step-graded relaxed Si,-, Ge, buffer layers, were grown on Si(001) by UHV/CVD at temperatures in the range 500-550°C. They were subsequently annealed at 1000°C for times as long as 300 sec. The x-ray measurements were performed at beamline X20 at NSLS using a triple-axis configuration with an 8 keV incident beam. The large dynamic range of the synchrotron enabled the diffraction peak of the strained Si cap layer to be observed in addition to the relaxed SiGe buffer peak. Micro-Raman spectra taken using 488 nm excitation revealed that the sample showed a strong peak corresponding to the relaxed SiGe buffer layer and a less intense peak (or shoulder at lower x) corresponding to the strained Si cap layer. Both the x-ray and micro-Raman measurements show that the thickness of the strained Si cap layer decreases with increasing annealing time, a result that we attribute to interdiffusion at the Si/Ge interface. However, no significant relaxation of the strain in the Si cap layer was detected by either method. This latter result is confirmed by TEM which shows a negligible misfit dislocation density at the SiGe/SiGe interface after annealing. #The National Synchrotron Light Source at Brookhaven National Laboratory is supported by the US Department of Energy, Division of Materials Sciences and Division of Chemical Sciences.

9:15 AM #A1.3
STRAIN-INDUCED INSULATOR (STRAIN-SOI) MOSEFTS - CONCEPT, STRUCTURE AND CHARACTERIZATION. Shintaro Takeshita, Tsutomu Tsuru, Tomohisa Minami, Naoharu Sugiyama, Atsushi Kurobe, Advanced LSI Technology Laboratory, Toshiba Corp., Kawasaki, JAPAN.

Attention is being paid to MOSEFTs with high mobility channel, in order to relax several fundamental limitations of CMOS scaling. Strained Si CMOS is an attractive device structure among them, because of high electron and hole mobility and compatibility with Si CMOS processing. Strain-induced MOSFETs are the device structure using the strained-Si channel, strained-SiO2-SiON insulator (strained-SOI) MOSEFT, applicable to sub-100 nm Si CMOS technology nodes. This device includes thin strained-Si relaxed-SiGe layers formed by ion-irradiation etches. The device structure and the advantages of strained-Si MOSEFTs and strained-SiO2 CMOS are presented. The combination of the SIMOX technology and regrowth technique of strained Si films realizes this device structure. It is demonstrated that strained-Si MOSFETs with Ge content of 13% have mobility of 1.6 and 1.3 times as high as the relaxation mobility, respectively. Furthermore, we propose a new technique to fabricate ultrathin gate insulator (SOI) virtual substrates with higher Ge content, which is mandatory for realizing fully-depleted SOI MOSFETs with higher mobility. This fabrication technique is based on the enrichment of Ge content in SiGe films by using an oxidation-diffusion process to form a buried oxide layer. The Ge concentration is increased to more than 50% of the total Si thickness and SiO2 /SiGe top layer. The rejection of Ge atoms from oxidized layer into remaining SiGe films and the blockage against Ge diffusion into SiGe by buried oxide enable to realize ultrathin SOI MOSFETs with higher Ge content. A 10 nm SOI layer with Ge content larger than 50% are successfully fabricated by this technique. Using this substrate, strained-SOI structure with total Si thickness of 21 nm is achievable, which is sub-100 nm fully-depleted strained SOI CMOS is accomplished.

9:45 AM #A1.4

With the rapid proliferation of commercial SiGe HBT (hetero bipolar transistor) devices, incompatibilities with mainstream integration technologies become an important issue. A common problem in device processing is transient enhanced diffusion (TED) of boron out of the base region due to poly-emitter implantation and annealing. It has been shown that co-doping of the Si,-, Ge, base with C can very effectively counteract TED of B. However, the use of C at high concentration results in too many defects and thus is limited by TED of C, which overcompensates the interstitial diffusion paths for B. Hence, C co-doping leads inherently to a broad C distribution throughout the active device. Moreover, the required C concentrations exceed the solid solubility of C in Si, and are thus incompatible with SiGe. It is therefore essential to characterize the structural and electronic behavior of C co-doping under realistic process conditions. For this purpose we combined Fourier Transform Infrared spectroscopy (FTIR), very fasted annealing and SIMS experiments to investigate which form C presents, after thermal treatment of Si,-, C, layers with and without ion-implanted poly-Si emitter. The FTIR technique is sensitive to substitutional C, coherent and incoherent Si precipitates and some C containing complexes via their characteristic local vibration modes. With this technique we followed the evolution of SiC precipitate formation upon annealing at typical process temperatures between 750 and 1100°C, and correlated these results with strain relaxation in the Si,-, C, layers. The results suggest that low thermal budgets are an essential precondition for employing C containing epitaxial layers in device structures.

10:30 AM #A1.5

Relaxed SiGe-on-insulator (SGOI) is a very promising technology as it combines the benefits of two advanced technologies: the conventional SOI technology and the disruptive SiGe technology. The SOI configuration offers various advantages associated with the insulating substrate, namely reduced parasitics and some COC using complex wafers, and reduced short-channel effects, etc. High mobility strained-Si or strained-SiGe MOSFETS devices are fabricated in SGOI substrates and further processed into III-V photodetector devices. Different experimental approaches were investigated: SiGe-handle wafer direct bonding and SiGeoxide-handle wafer bonding. Two different ways to thin down the bonded wafers were used: etch-back utilizing a 20% Ge layer as a natural etch stop and “smart-cut” process using hydride etch-pit initiation. Bonding conditions were optimized for strong bond energy. The resultant SiGe film quality was compared among the different approaches. Epitaxially strained SiGe MOSFETs were fabricated on the SGOI substrates. Epitaxial regrowth was used to produce the upper portion of the relaxed SiGe and the surface strained Si layer. The measured electron mobility shows significant enhancement over both the unstrained and the strained silicon MOSFETs. This SGOI process has a low thermal budget and thus is compatible with a wide range of Ge contents in SiGe layer.
10:45 AM A.1.6 RELAXATION PHENOMENA IN Si$_{x}$-Ge$_{y}$ BUFFER LAYERS ON Si[001] BY He$^+$ ION IMPLANTATION. S.H. Christiansen, P.M. Mooney, J.O. Chu, A. Grill, IBM Research Division, T.J. Watson Research Center, Yorktown Heights, NY.

Transmission electron microscopy (TEM) in planar view and cross section and x-ray diffraction have been applied to study the relaxation characteristics of relaxed (>80%) thin [Si1-xB] films on Si substrates obtained by a process developed at IBM. The relaxed layers have been obtained through a 3-step process: (I) a pseudomorphic SiGe layer was deposited on a Si[001] substrate using ultra high vacuum chemical vapor deposition (UHV-CVD); (II) He$^+$ was implanted into the substrate; (III) the sample was annealed at elevated temperatures. As a result of this process, 3-dimensional defects that act as internal interfaces for dislocation half-loop formation are formed. The different defects have been evaluated with regard to their shape and spacing potential for dislocation nucleation and the formation of threading dislocations. The different relaxation mechanisms in step-grown and implanted buffer layers are discussed.

11:00 AM A.1.7 BEHAVIOR OF ION-IMPLANTED N-TYPE DOPANTS IN SILICON GERMANIUM. Sowashi Egashi, Judy L. Hoyt, Massachusetts Institute of Technology, Microsystems Technology Lab, Cambridge, MA. Christopher W. Leitz, Eugene A. Fitzgerald, Massachusetts Institute of Technology, Dept of Materials Science and Engineering, Cambridge, MA.

An understanding of the behavior of ion implanted n-type dopants in SiGe is essential for the development of novel silicon-based technologies, such as strained Si on relaxed SiGe CMOS. In this work, the diffusivities of ion-implanted n-type dopants, phosphorus and arsenic, are observed to be enhanced in relaxed Si$_{0.8}$Ge$_{0.2}$ compared to Si, in contrast to the diffusion of boron, which is known to be retarded in SiGe relative to silicon. We discuss the effective diffusivities of phosphorus and arsenic under long time annealing conditions. We also report arsenic diffusion under transient conditions in SiGe, and compare to measurements in similarly processed Si samples. SIMS data is compared to TSUPREM-4 simulations. Simulation profiles are calculated using the interface trap model, which is required to account for the observed drop-off of dopant depth as a function of oxide/Si and oxide/SiGe. Under long-time annealing conditions, the extracted effective diffusivity enhancement factor (measured relative to the extracted dopant diffusivity in silicon) for phosphorus is about three, while the effective diffusivity enhancement factor for arsenic is roughly 10. The diffusion of arsenic in SiGe is enhanced more than that of phosphorus in SiGe. However, the absolute diffusivity value of phosphorus is still roughly 4 times higher than that of arsenic in SiGe. Under transient annealing conditions at 900°C, arsenic diffusion in SiGe is comparable to that in Si, suggesting that using arsenic, short-time annealing may be used to obtain similar junction depths in ion implanted Si and SiGe.

11:15 AM A.1.8 ELECTRICAL PROPERTIES OF Si$_{x}$-Ge$_{y}$ FILMS GROWN BY PLASMA-CVD AT A LOW SUBSTRATE TEMPERATURE. Shoshei Nogi, Tatsuya Okahisa, Atsuko Yamada, Masaaki Konagai, Tokyo Inst of Tech, Dept of Physical Electronics, Tokyo, JAPAN.

We have successfully grown Si$_{x}$-Ge$_{y}$ films and widely investigated on their electrical properties. Epitaxial Si$_{x}$-Ge$_{y}$ films were grown on Si[001] by the plasma-CVD using a gas mixture of SiH$_4$, H$_2$, and SiH$_4$ (CH$_3$)$_3$. PH$_3$ was used in doping gases. The substrate temperature and the growth rate were maintained at 210°C and 0.5 Å/s, respectively. The n-type Si$_{0.5}$-Ge$_{0.5}$ films were obtained and electron concentration could be linearly controlled up to 1 x 10$^{19}$ cm$^{-3}$ by varying the doping ratio of PH$_3$/SiH$_4$. In the n-type films, the electron concentration of C-doped films (1% C) was the half value of the Si film at the same doping ratio (PH$_3$/SiH$_4$), while the values were almost one order of magnitude lower than that of the Si film when the C concentration was higher than 1%. On the other hand, after annealing at 800°C, the electron concentration of both Si and Si$_{0.5}$Ge$_{0.5}$ showed the same value. However, the values of the Si$_{0.5}$-Ge$_{0.5}$ films whose C concentration was higher than 1% were still one order of magnitude smaller than that of Si film. In our previous work, we found that almost all C atoms located at the Si substrate interface in the annealed sample with total C composition of lower than 1% at the annealing temperature of 700°C. On the contrary, the interstitial C content was increased with increasing the total C composition higher than 1% after annealing. Thus, the behavior of the electron concentration following annealing could be explained as follows: The interstitial C atoms form the defect complex with P atoms and suppress the donor activation, resulting in the reduction of the electron concentration.

11:30 AM A.1.9 STRAINED GERMANIUM CHANNEL P-TYPE MOSFETS FABRICATED ON Si$_{x}$-Ge$_{y}$/Si VIRTUAL SUBSTRATES. Minjoo Lee, Christopher Leitz, Arthur Pitera, Gianni Tranchi, Eugene Fitzgerald, MIT, Dept of Materials Science and Engineering, Cambridge, MA. Dimitris Assimacopoulos, MIT, Dept of Electrical Engineering and Computer Science, Cambridge, MA.

Low defect density relaxed SiGe alloys on Si have created a new platform for high mobility electronic devices as well as integration of optoelectronics on Si. Strained silicon n- and p-type MOSFETs on relaxed Si$_{x}$-Ge$_{y}$/Si virtual substrates exhibit mobility enhancements of 1.25 to 2 times that of bulk devices. But just as in bulk Si, the p-MOS mobility lags the n-MOS considerably. Compactly strained Si$_{0.5}$Ge$_{0.5}$ channels on Si$_{0.5}$Ge$_{0.5}$ (y=0.5) have thus been used to attain even higher hole mobilities. However, the highest hole mobility should be realized with a compactly strained, pure germanium channel due to reduced intervalley scattering and the lack of alloy scattering. Strained-GaGe layers on Si$_{0.5}$Ge$_{0.5}$ have previously been used to fabricate high mobility and high transconductance MODFETs, but all of these devices utilized Shottky gates. Germanium oxide’s hygroscopic nature and the high interface state density which results when SiO$_2$ is deposited onto Ge surfaces has historically prevented the development of germanium MOS technology. To circumvent this, the Ge channel in our devices is capped with a thin epitaxial silicon layer. Despite the intrinsic mismatch of over 28% and great relaxation, our optimized growth process yields a top Si layer with fully planar morphology. This Si layer protects the Ge-rich heterostructure from standard etching processes and also provides a high-quality interface with the gate SiO$_2$. Our Ge MOSFETs show a mobility enhancement of more than 7 times that of coprocessed bulk Si devices with a peak effective mobility of 1100 cm$^2$/V.s. At sufficiently high vertical fields, the top Si layer was shown to conduct as a parallel hole channel, resulting in slightly degraded mobility enhancement. But since the compressive Ge channel strongly confines holes, minimizing the top Si thickness allowed the mobility enhancement to be maintained at fields as high as 0.6 MV/cm.

SESSION A2: ADVANCED CMOS: SOI AND VERTICAL DEVICES

Erin Jones

Monday Afternoon, November 26, 2001
Room 202 (Hynes)

1:30 PM A.2.1 CHALLENGE FOSTERS FOR FUTURE SOI CMOS DEVICES. Scott Crowder, Semiconductor Research & Development Center, IBM, Hopewell Junction, NY.

There are several important technical challenges in the design of future SOI CMOS transistors. This talk will focus on the processing issues related to scaling today’s SOI transistors into the 0.07-micron generation and beyond. Topics will include the challenges in relaxing silicon film thickness, including the following trapezoids of SOI, integrating DRAM into SOI logic and building novel devices that offer advantages over the current device structure.

2:00 PM A.2.2 MATERIALS REQUIREMENTS FOR FUTURE THIN-BODY SOI MOSFETS. Ta-Jue Lee, King Department of Electrical Engineering and Computer Science, University of California at Berkeley, Berkeley, CA.

As the MOSFET is scaled down to gate lengths below 30 nm to achieve continued improvements in cost and performance, alternative transistor structures such as thin-body FETs will eventually be used in order to adequately control sub-threshold leakage current and short-channel effects. Existing technological challenges for single-gate and double-gate fully-depleted SOI CMOS transistors must be overcome before they can be used in the manufacture of high-density integrated circuits, however. This paper describes the materials requirements for control and enhancement of thin-body SOI FET performance in future CMOS technologies.
2:30 PM A23
THE STUDY ON THE FORMATION OF THIN SOI STRUCTURE BY SIMOX WITH WATER PLASMA. Jing Chen, Meng Chen, Xiang Wang, Yemin Dong, Zhihong Zheng, Xi Wang, Ion Beam Laboratory, Shanghai Institute of Metallurgy, Chinese Academy of Sciences, CHINA.

The biggest drawback of the widely application of SOI material is high cost which mainly due to the long implantation time by conventional beamline implanter. An implanter without ion mass analyzer is used to reduce SOI material cost by water implantation using water plasma based on the consideration that the masses of the three ions of H\textsuperscript{+}, O\textsuperscript{+} and O\textsuperscript{2+} are quite close, their depth profiles in as-implanted wafers will not disperse much, that makes it possible for the formation of SOI layer by choosing appropriate implantation energy and dose. The process provides shorter implantation time, lower cost and preferential potential for large size wafers. Single crystal silicon wafer was implanted with 50-80 keV water ions density of 1 \times 10\textsuperscript{17} to 7 \times 10\textsuperscript{17} cm\textsuperscript{-2} at 680°C. Capped with 500 nm SiO\textsubscript{2} layers by LPCVD, the samples were annealed over 1300°C for 5 hours in a flowing 99.9% Ar 0.5% O\textsubscript{2} ambient. The structure of as-implanted and annealed samples was investigated by XTEM, HTEM, SIMS, and RBS, respectively. The results show that it exists a dose window at fixed implantation energy to form desirable thin or even ultra-thin SOI structure with the buried oxide layer free of silicon islands and smooth interfaces. Compared to conventional SIMOX, the samples implanted at the same dose and energy have thicker BOX layers, which may be caused by the hydrogen-induced defects, for there are two hydrogen enrichment peaks around both sides of the projected range (R\textsubscript{p}) of oxygen in the as-implanted wafers by SIMS measurements. The hydrogen effect in the formation process will be discussed.

2:45 PM A34
A PATTERNED SOI BY MASKED ANNEAL FOR SYSTEM-ON-CHIP APPLICATIONS. G.M. Cohen and D.K. Sudha, IBM T.J. Watson Research Center, Yorktown Heights, NY.

System on a chip (SoC) requires the integration of logic and memory circuits on the same chip. While for logic circuits the driving force is primarily speed, for memories, and in particular dynamic random access memories (DRAM), it is the circuit density. Logic circuits implemented in conventional silicon-on-insulator (SOI) technology exhibit a significant improvement in the device speed due to the reduction in the junction capacitances. High density DRAM is built using deep trench capacitors, which are not compatible with SOI technology, and are implemented with conventional bulk Si wafers. Combining logic and memory on the same chip would therefore require a mixed SOI and bulk Si wafer technology.

In a recent work [R. Hamann et. al, 2000 Symposium on VLSI Technology, p. 66, 2000] a 64 Mb DRAM and logic circuits were integrated on a patterned SOI wafer which was fabricated by the patterned SIMOX [separation by implantation of oxygen] process. In the case of oxygen, the internal thermal oxidation [ITOX] during the annealing plays an important role in the BOX formation. A patterned SOI structure is created when the implanted oxygen dose is low enough such that the BOX forms only where ITOX occurs, i.e., in an open mask region where the oxygen supply from the ambient is not blocked by the hard mask) and no BOX forms under the mask region where ITOX occurs. When the implanted dose is high the patterned SOI contains a thick BOX under the unmasked region and thin BOX under the masked region.

3:30 PM *A25
INTEGRATION CHALLENGES FOR DOUBLE-GATE MOSFET TECHNOLOGIES. Witko P. Mooney, AMD, Sunnyvale, CA.

Device modeling data and some early experiments suggest that fully-depleted MOSFET devices where channel is controlled by two opposing gates rather than one gate or the entire channel, will provide better scalability than the classical devices with one gate on one side of the channel. However, formation of such devices requires complex, non-conventional and sometimes exotic geometry and processing, raising a number of concerns about handling bulk MOSFETs. In this talk, we will present a range of integration concepts, including selective wet-etched channels with triangular cross-section, that can provide a pathway toward realizing scalable MOSFETs with excellent scalability and scalability. We will also discuss the challenges and opportunities associated with the development of these devices, including the need for new materials and processing techniques.

4:00 PM A26
WAVER BONDING OF DIAMOND FILMS TO SILICON FOR Si/SiO\textsubscript{2} ON-INSULATOR TECHNOLOGY. Gleb N. Yashin, Scott D. Walter, Alex Kvit, Zhitko Sitar, North Carolina State Univ, Dept of Material Science, Raleigh, NC; John T. Farmer, Army Research Office, Research Triangle Park, NC, B.R. Stoner, MCNC, Material and Electronic Technologies Division, Research Triangle Park, NC. At present, the fabrication of silicon-on-insulator (SOI) devices by wafer bonding (WB) is in a very early stage. WB offers reduced defects in the SOI layer, which leads to better electrical characteristics. Conventional SOI technology employs silicon dioxide as a buried insulator. However its low thermal conductivity limits the performance of the high power devices due to the resulting thermal runaway. Diamond is known to be a better thermal conductor than silicon dioxide and can be used as a buried insulator in SOI technology. In this paper, we present our recent efforts on the growth of high quality diamond films on silicon substrates using wafer bonding techniques.

4:15 PM *A27

We have demonstrated the Vertical Replacement-Gate (VRG) MOSFET, the first MOSFET ever built in which 1) all critical transistor dimensions are controlled precisely without lithography, 2) the gate length is defined by a deposited film thickness, independently of lithography and etch, and 3) a high-quality gate oxide is grown on a single-crystal Si channel. In addition to this unique combination, the VRG-MOSFET includes self-aligned source/drain extensions formed by solid source diffusion (SSD), small parasitic capacitances, and a replacement-gate approach to enable alternative gate stacks. All of this is achieved using current manufacturing methods and tools, and high-performance devices with 50 nm gate lengths have been demonstrated with precise gate length control without advanced lithography. In the VRG process, a stack containing a sacrificial gate layer sandwiched by two dopant source layers is deposited. A trench is etched through this stack and it is filled with single-crystal Si to form the device body. Si allows self-aligned source/drain extensions to be formed directly from the source. The sacrificial gate layer is removed, a gate oxide is grown on the exposed Si, and the gate is deposited in place of the sacrificial layer. This replacement-gate approach allows for the fabrication of high-quality gate oxides on a variety of 100–140 μm Si surfaces, where conventional processes are limited by oxide thickness. This flow is mechanically scalable to sub-30 nm gate lengths with excellent control. Since both sides of the device drive in parallel, the VRG drive currents can far exceed that of advanced planar MOSFETs. Our 100 nm VRG-MOSFETs with 25 Å gate oxides drive 80% more current than specified in the 1999 ITRS Roadmap. Our 50 nm VRG-MOSFETs with 25 Å gate oxides approach the 1.0 V roadmap drive current target of 350 μA/μm without the need for a hyperfr (≤ 20 Å) gate oxide.

4:45 PM A28
ENHANCED MOBILITY IN 100 NM STRAINED SiGe VERTICAL MOSFETs FABRICATED BY UHVCVD. Satrajit Banerjee, Srinivas Jayaraman, Freek Prins, Xueqiang Chen, University of Texas, Austin, TX.

Recently, strained silicon-germanium MOSFETs are receiving considerable attention due to the enhancement of in-plane hole mobility, as well as out-of-plane electron and hole mobilities over conventional silicon MOSFETs. In the direction normal to the growth plane, strain effects in SiGe vertical MOSFETs are important. The process of fabricating SiGe vertical MOSFETs is a complex one that involves the integration of high-quality SiGe and silicon layers. In this talk, we will present our recent efforts on the growth of high-quality strained SiGe vertical MOSFETs. We will discuss the challenges and opportunities associated with the development of these devices, including the need for new materials and processing techniques.
deposition (UHV CVD) at 500 °C using SiH₄ and GeH₄. PH₃ and B₂H₆ were used for this purpose. The x-ray diffraction (XRD) rocking curves of the SiGe layers demonstrate that the SiGe layers do result in compressive strain. The germanium profile, with a mole fraction of about 0.55, is uniform over the entire device. Atomic force microscopy (AFM) of the SiGe and silicon sample surfaces shows the RMS roughness increases from 0.08 nm to 0.18 nm. These results are used to define the mean of the vertical MOSFET. A 10 nm silicon cap layer was grown by UHV CVD before growing a 4 nm gate oxide by wet oxidation at 750 °C. The drive current for the vertical SiGe MOSFET was enhanced, which is consistent with the enhanced gate oxide thickness compared with the silicon control device, in both the forward and reverse modes of operation. The drain induced barrier lowering (DIBL) for the SiGe device was observed to be higher than the silicon device, since silicon-germanium has a lower bandgap, thus that of silicon. The sub-threshold slopes of the silicon and silicon-germanium devices were 105 and 180 mV/decade, respectively.

SESSION A3 POSTER SESSION

SILICON-BASED SUBSTRATES AND DEVICE PROCESSING

Chair: Tze-Lue King
Monday, November 26, 2001
8:00 PM
Exhibition Hall D (Hyves)


We report on a study of homeopitaxial Si layer growth performed by R.F. Plasma-Enhanced Chemical Vapor Deposition (R.F. PECDVD) on Si(100) from a gas mixture of SiH₄, He, and Ar at temperatures between 325 and 500 °C. The transition from epitaxial to dendritic growth at a critical thickness was investigated at various growth conditions by changing the growth temperature, the gas flow rates and the substrate bias voltage. The depth profiles of the Si disorder and of the impurity concentrations (O, N, C and Ar) were determined by 1.4 MeV 16O⁺ Rutherford Backscattering Spectrometry (RBS) in a 2.5 MeV He⁺ Elastic Recoil Detection Analysis (HR-EELD) using 230 MeV 23Na⁺ ions, and by Secondary Ion Mass Spectroscopy (SIMS). In addition, the films were analyzed by Raman Spectroscopy and Scanning Electron Microscopy (SEM). A striking similarity was found between the Si disorder profiles evaluated from the RBS channeling spectra and the impurity profiles determined by HR-EELD and SIMS. Concurrent with the breakdown of the epitaxial growth a strong increase of the hydrogen concentration is found at the same depth position. Raman spectra and SEM cross-section images show that at this thickness limitation of epitaxial growth coarsely shaped precipitates of amorphous SiHx are being nucleated. The dependence of the critical thickness on the growth parameters can be understood within the framework of a model recently proposed by Thiesen et al. [1]. The model predicts the critical thickness due to a hydrogen supersaturation of the growth surface which is balanced by the incident hydrogen flow and the diffusive transport into the substrate. In accordance with this model we observe a significant concentration of hydrogen that has diffused into the Si substrate. [1] J. Thiesen, H.M. Brunz, R.S. Grannich, Appl. Phys. Lett. 77, 3569 (2000).

A3.2 FABRICATION OF HIGH INTEGRITY THIN BURIED OXIDE LAYERS FROM CRYSTALLOPTIC COMBINATION. Chen Meng, Chen Jing, Wang Xiang, Dong Yeming, Liu Xinghui, Yu Yuewei and Wang Xi, Chinese Academy of Sciences, Shanghai, PR CHINA.

It is of great interest in low-dose (dose<1.0x10^18 cm⁻²) separation of implanted oxygen (SIMOX), because the thin BOX SIMOX has been shown to improve wafer quality in all aspects as discussed for the full dose SIMOX wafers due to the lowered oxygen dose by reducing the implantation time. However, the low dose SIMOX materials usually have higher density of Si islands and pinholes in BOX layer, which have been reported to be responsible for increased electrical leakage current through the BOX, or in extreme cases, its dielectric breakdown. In this paper, we report directly formation of device grade low dose SIMOX materials at an energy of 45- 160 keV with a dose of 1.8 - 13.5x10¹⁷ cm⁻². The materials were characterized by RBS, SIMS, TEM, HRTEM, SECCO, Coupling and MOSS capacitance. The results reveal a series of good matches of dose-entenary combination for formation of device-grade low dose SIMOX materials with high crystal quality of top silicon layer, low silicon islands density and pinhole density in BOX layer. Minimal yield X₅₀, from RBS measurement are 3.82 - 4.47%, which are comparable with that of virgin silicon. TEM reveals high integrity BOX layer is likely to be formed in a good match of dose-entenary combination. HRTEM reveals a strong dependence of upper interface on dose-entenary match. SECCO characterization indicates that samples fabricated at optimum dose-entenary matches have a threading dislocation density lower than 10⁸ cm⁻². Coupling reveals that the samples implanted at optimum dose-entenary matches have a pinhole density lower than 3 cm⁻² which is much lower than those implanted outside of optimum dose-entenary match. Breakdown field determined from MOS capacitance is about 6 MV/cm. Furthermore, the higher the implanted energy required for the formation of Si-land free BOX. The effect of dose-entenary match is due to the oxygen profile in n+ implanted wafers, which is consistent with dose-entenary match. This work also indicates a possibility to suppress unwanted thickness of both SOI and BOX layer by choosing an optimum match of energy-dose combination. Furthermore, it can be used to fabricate ultra-SIMOX materials by optimizing low-energy ion implantation that meet the requirements of fully depleted CMOS circuits and system-on-a-chip on SOI wafers, easily realize the patterned SOI structure, and improve the throughput capacity in the SIMOX wafer manufacturing without additional products cost.

A3.5 ELECTRICAL PROPERTIES OF ULTRA SHALLOW JUNCTIONS ON N-TYPE Si WAFER USING DECARBORIZING ION IMPLANTATION. Ji-Hoon Song, Won-Kook Choi, Koren Institute of Science and Technology, Thin Film Technology Research Center, Seoul, KOREA; Duk-Kyun Choi, Hanyang Univ, Dept of Inorganic Materials Engineering, Seoul, KOREA.

The junction depth should be less than 0.05 μm to fabricate sub 0.1 μm devices, which requires less than 1 keV ion implantation energy. However, in this case, the implantation time is too short to low ion beam current. In addition, boron as a type dopant for MOSFET has high diffusivity and thus easily diffuses into Si wafer even in rapid thermal processing. To manipulate this problem on boron implantation, decarborizing (H₃PO₄) for boron source was implanted to make p+ junction on n-type Si wafer. Ionized decarborization by thermo-electron bombardment was accelerated at 115
kV and implanted up to doses from 1 x 10^11/cm² to 5 x 10^12/cm².

Afterward, B implanted Si wafers were post-annealed for 10 sec at 800°C, 900°C, respectively. Through RBS characterization, it was observed that the amorphous Si layers with 4 nm in depth and boron ions are implanted up to 1-5 nm in depth from MS analysis. These p-implantations showed 125-I-base, and kV characteristics of 0.3V turn-on voltage and +1 V breakdown voltage. From these results, ultra shallow junction below than 10 nm can be assembled by this technique.

A3.6 GROWTH AND CHARACTERIZATION OF UHV-CVD SiGe STRAINED-LAYER SUPERLATTICE ON BULK CRYSTAL Si SUBSTRATES. Shuang Sheng, Institute for Microstructural Sciences, National Research Council of Canada, Ottawa, ON, CANADA; Michel Dion, SiGe Semiconductor Inc., Ottawa, ON, CANADA; Sen P. M. Kater, Institute for Microstructural Sciences, National Research Council of Canada, Ottawa, ON, CANADA.

The development of advanced Si-based electronic and optical devices and thermoelectric generators incorporating Ge, would be enhanced by the availability of high-quality, low defect density substrates with an adjustable lattice parameter and band gap between Si and Ge. Such substrates would permit the growth of tensile-strained Si on Ge layers, giving rise to a type II band alignment required for developing SiGe/Si devices based on electron confinement. Single crystal SiGe would be an advantage as the lattice-matched substrate material, instead of Si for high quality epitaxial growth. Here, we report the first growth of high-quality UHV-CVD SiGe/Si strained-layer superlattices at 530°C on commercially available high-quality 4H-SiC substrates (~10-7 cm"2 bulk crystal SiGe superlattices grown using a modified Czochralski technique by Virginia Semiconductor Inc., rather than using thick virtual substrates. These strained-layer superlattices were characterized by high-resolution x-ray diffraction (XRD), Auger electron spectroscopy (AES), atomic force microscopy (AFM), transmission electron microscopy (TEM) and photoluminescence (PL) spectroscopy. XRD rocking curve analyses show uniform layer thickness and low-composition roughness in the superlattices of 5 periods, in good agreement with Auger profile analysis. The Ge concentration determined by both XRD and AES are nearly the same as that for SiGe substrates. Neither strain relaxation nor threading dislocations were observed by XRD. AFM images show similar RMS roughness of much less than 1 nm for both the top layer surface and the substrate surface, indicating very smooth surfaces. Details of this work along with the data of interfacial abruptness, dislocations and defects will be presented. This study demonstrate that the use of bulk crystal SiGe substrates, combined with low temperature epitaxy, leads to high-quality strained-layer SiGe superlattices, and may open up many new device applications.

A3.7 Abstract Withdrawn.

A3.8 POLY-SiGe TFTs FABRICATED BY LOW-TEMPERATURE CHEMICAL VAPOR DEPOSITION AT 450°C. Kosuke Shimizu, Jianjun Zhang, Jeong soo Lee and Jun-ichi Hiram, Imaging Science and Engineering Laboratory, Tokyo Institute of Technology.

Low temperature growth of poly-SiGe has been investigated using reactive thermal chemical vapor deposition (RTCVD) method, which is a newly developed technique for preparing poly-SiGe by using redox reactions in a set of source materials, i.e., disilane (SiH₄) and germanium trifluoride (GeF₃). The technique gives quite uniform films as well as no polymeric silicon particles, which can be applied to large-area electronic devices such as TFT arrays for flat-panel display devices and solar cells. This is because the source gases are activated thermally at the vicinity of the substrate surface and react with each other, resulting in film growth on the substrate as in the case of thermal CVDs. Moreover, in this CVD, germanium trifluoride plays an important role to crystal growth at a low temperature of 450°C. In order to prepare Si-rich poly-SiGe (Si > 50 wt.%), total pressure, gas flow rate and reaction time were optimized. The typical condition is as followed: the gas flow rate of SiH₄/GeF₃ = 5/0.5/1000 (sccm), the reaction pressure of 5.0 Torr and substrate temperature of 450°C. In this condition, the film uniformity (>90%) and reproducibility was well established. Bottom gate-type n-channel TFTs have been fabricated with 200nm thick films of poly-SiGe with various grain sizes on the glass substrates. The TFTs were treated with atomic hydrogen after fabrication by using hot water admittance. The TFTs of L/d = 400/10um showed a field effect mobility of 5.30 cm²/Vs with an increase in the grain size of 500-900nm. Threshold Voltage (Vth) is around 2±0.5V, and On/Off ratio is more than 10⁶.


Plasma etching of silicon plays a critical process role in the fabrication of a large variety of devices from microelectronics to systems to integrated circuits. As such, plasma etching has been the subject of research and study for several years in an effort to not only control but improve the surface properties of silicon. In-situ near-edge x-ray absorption fine structure analysis (NEXAFS) and x-ray photoelectron spectroscopy (XPS) is used to study the surface properties of silicon in a plasma environment. XPS is used to determine the silicon oxidation state while NEXAFS is used to determine the chemical state and concentration of surface species. In-situ x-ray diffraction offers a unique tool for the study of surface structural evolution during plasma etching. Using a synchrotron x-ray source, we have examined Si (100) and (111) surfaces undergoing Ar⁺ bombardment at a constant ion energy (100 to 500 eV) and temperature (50 to 400°C). Grazing-incidence small-angle x-ray scattering (GISAXS) shows that the surface morphology evolution varies significantly with ion energy in this range. In some parameter ranges, a single roughness length scale apparently dominates the surface morphology while in others at least two separate length scales appear. The results of the in-situ characterizations are supplemented by ex-situ atomic force microscopy (AFM) of the processed surfaces. Features of interest are observed by AFM on the processed surfaces that agree well with the length scales determined by the in-situ measurements.


Strained Si and SiGe-based heterostructures MOSFETs grown on relaxed SiGe virtual substrates exhibit dramatic electron and hole mobility enhancements over bulk Si, making them promising candidates for next generation CMOS devices. The most heavily investigated heterostructures consist of a single strained layer grown upon a relaxed SiGe substrate. While this configuration offers significant MOSFET and nMOSFET performance gains, hole mobility is still much lower than electron mobility. By contrast, the combination of buried compressively strained SiGe layers and tensile strained Si surface layers grown on relaxed SiGe, hereafter referred to as dual channel heterostructures, offers nearly symmetric electron and hole mobilities without compromising nMOS device performance. To investigate these heterostructures, we study the effects of alloy scattering, channel thickness, and surface morphology on channel mobility in long channel MOSFETs. In these experiments, MOSFETs are fabricated by a novel short flow process utilizing a deposited gate dielectric and only one lithography step. This type of device allows us to measure effective mobility at vertical fields approaching 1 MV/cm, thereby enabling us to quickly explore the impact of materials parameters on channel mobility at fields approaching those of state-of-the-art MOSFETs. With this approach, we have achieved hole mobility enhancement factors over bulk Si of 5x15 for dual channel heterostructure devices. By employing different virtual substrate compositions, we can decode the effects of strain and alloy scattering in both tensile surface channels and compressive buried channels. Direct measurements of the impact of alloy scattering on channel mobility in both of these layers will be presented. Mobility enhancements in hole channels will also be correlated to changes in channel morphology resulting from large compressive strain levels. We will demonstrate that dual channel heterostructures provide excellent performance gains for both pMOS and nMOS devices and explore the useful design space of these structures.

SESSION A4: MiLC MATERIALS GROWTH FOR CMOS AND TFT
Chair: Man-Han Chu, Tuesday, November 27, 2001, Room 202 (Hynes)

8:45 AM A4.1 GRAIN QUALITY ENHANCEMENT OF NICKEL-CRYSTALLIZED POLY-SI FILM IN QUANTUM-WIRE STRUCTURES. W.M. Cheung, Hongmei Wang, Sing Jager, C.F. Cheng, M.C. Poon, Masaan Chu, Dept. of Electrical & Electronic Engineering, Hong Kong University of Science & Technology, Sai Kung, HONG KONG.

Methods for forming high quality recrystallizing polysilicon films are being actively studied due to their ability to provide significant improvement to polysilicon Thin-Film-Transistors (TFT). Recently, a simple Metal-Induced Lateral-Crystallization (MiLC) method with
nickel, together with high temperature annealing, can result in single crystal-like polycrystalline silicon films [1]. TTFs fabricated on this so-called Large-gate-length Silicon-On-Insulator (LPSOI) can achieve SOI MOSFET performance especially at small dimensions. This paper reports that the silicon grain quality can be further enhanced by crystallizing the polycrystalline silicon film into the shape of long-wire. The crystallization procedure, which is a regular MLC process at 560°C, was described in [1]. The film is then etched into narrow wires parallel to the direction of nickel propagation. The second anneal at 850-900°C is then performed on these silicon wires. Through surface energy minimization, silicon self-rearrangement into a single-crystal silicon film taking place. The deep submicron region is observed for these wires where the epitaxial TTFs formed on the same MLC film. Experiment results show that the isolated wires formed by the parallel combination of the wires give a 100% current drive as a TTF on the same MLC film. The result is shown in Figure 2. The MLC film on which the single-crystal silicon film is likely the same thickness as the MLC film on which the polycrystalline silicon film is formed. Then the silicon films will be much better than the single-crystal silicon film taken from the same MLC film. This work shows that the thin film transistors fabricated by the proposed method showed considerably improvement in the electrical characteristics, which directly reflect the quality of polycrystalline silicon film used. It is believed that super TTFs with SOI CMOS performance and good uniformity can be obtained through the reduction in channel dimensions and optimized process conditions.

9:30 AM A4.4 EFFECTS OF DOPANTS ON METAL INDUCED LATERAL CRYSTALLIZATION RATE. Gu-Dam Kim, Yeo-Geun Yoon, Ji Soo Ahn, Hyo-Hyang Park, Min-Sung Kim, Woosock Park, Seung-Ki Joo, School of Materials Science and Engineering, Seoul National Univ., Seoul, KOREA.

Polycrystalline silicon thin film transistors (poly-Si TFTs) technology is very attractive for the applications of active matrix liquid crystal devices (AMLCDsand integrated peripheral driven circuits fabricated on glass substrates. So many works have been concentrated on improving the crystallization performance of poly-Si TFTs. Metal induced lateral crystallization (MILC) process has been previously introduced, by which the amorphous silicon thin films can be crystallized below 500°C. In this works, the effects of dopants on the rate and behavior of MILC were investigated. When n-Si was doped with boron, MILC rate increased to about twice of intrinsic n-Si and the front edge of crystallized silicon became rugged. But the p-Si doped with boron showed no improvement in MILC rate. On the contrary, in case of phosphorus dopant p-Si, MILC rate decreased about 75%, and there still some i-Si islands in the crystallized silicon region. The role of dopants in MILC rate, specially the mechanism of boron-doped p-Si is discussed in terms of activation energy for crystallization of i-Si and microstructure.

9:45 AM A4.5 LATERAL EPITAXIAL OVERGROWTH OF Si AND SiGe ON SiO2 USING BURNING LOW-TEMPERATURE (T<500°C) SOLID-METAL-MEDIATED EPITAXY, T.J. LaFave, N. Lokhandwala, and M.-A. Hase, C.C. Cameron, Applied Research Center & The Department of Electrical and Computer Engineering, University of North Carolina, Charlotte, NC.

Buried lateral epitaxial overgrowth of Si on thin SiO2 layers (<100 nm) using a thick solid Al layer as growth medium was demonstrated using a newly developed solid metal-mediated epitaxy (SMME) method. The experiments were carried out at growth temperatures T<500°C using electron-beam evaporation of Al from an effusion cell. Si(100) wafers were thermally oxidized and patterned to provide oxide stripes ranging from 2/2 to 50/500 microns. Each oxide stripe was repeated within an area of approximately 100 mm. The wafers were then thermally etched at T=900°C under UHV conditions to expose the remnant native oxide from the seed area, followed by deposition of Al at room temperature. Si was then deposited onto the resulting structure at T<500°C. The growth occurred epitaxially at the buried Al/Si interface and growth was extended laterally on the oxide layer. Initial TEM results demonstrated lateral growth of single crystalline Si over the oxide layer. This SMME method described above is based on SMME. In SMME, Si grows epitaxially on a buried Al/Si interface during thermal evaporation of Si. At N atomic layers diffuse through the Al layer to the interface where low-energy atomic Si sites act as sinks for the diffusing Si atoms. This process is fundamentally different from surface assisted growth at non-abrupt interfaces, in which small concentration of a metal (typically a fraction of a monolayer) is used to enhance epitaxial growth. In SMME, the Al layer can be thousands of monolayers thick (solid). The new findings may lead to new silicon-on-insulator fabrication methods. Also, it provides a procedure for combination metallization and heavy p-type doping, e.g. in MOS device structure. Applications of this method in device fabrication will be discussed.

SESSION A5. NANOCRYSTAL MEMORIES

Chair: Sandip Tiwari
Tuesday Morning, November 27, 2001
Room 202 (Hyatt)

10:30 AM A5.1 NANOCRYSTAL MEMORIES AS ELECTRONIC AND PHOTONIC DEVICES. Harry A. Atwater, Caltech, Pasadena, CA.

Si nanocrystal memories in which a dense Si nanoparticle array comprising the floating gate of a nonvolatile field effect device have potential for pervasive application in electronics and photonics. In this talk, I will describe recent advances in both nanocrystal memory fabrication, and also efforts to enhance the read/write performance through the use of heterostructure tunneling barriers to achieve nondestructive erase times with...
archival retention times. We are currently investigating optical reading and writing of nanocrystal memories as a tool to understand the physical basis of this phenomenon and to assess the potential of using
nanocrystal memories to function as optically addressable nonvolatile
device.

11:00 AM A5.2
FUTURE SILICON NANOCRYSTAL NONVOLATILE MEMORY TECHNOLOGY. Michele L. Ostran, Jan De Bhaene, Agere Systems, Murray Hill, NJ.

A great deal of research interest is being invested in the fabrication and characterization of nanocrystal structures as charge storage memory devices. In these thin film memory devices, it is possible to measure threshold voltage shifts due to charge storage of only a few electrons per nanocrystal at room temperature. Although a variety of methods exist to fabricate nanocrystals and to incorporate them into device layers, control over the critical nanocrystal dimensions, tunnel oxide thickness and nanocrystal/particle semiconductor isolation difficult to achieve. This control is vital to produce reliable and consistent devices over large wafer areas. To address these control issues, we have developed a novel two-stage ultra thin reactor in which the Si nanocrystals are generated as single crystal, nonagglomerated, spherical aerosol particles from slurry decomposition at 950°C in concentrations exceeding 10¹⁵ cm⁻³ at sizes below 10 nm. Using existing aerosol instrumentation, it is possible to control the particle size to approximately 10% on diameter. Particles are passivated with a high quality oxide layer with peak thickness controllable from 0.7 to 2.0 nm. The two-stage aerosol reactor is integrated to a 200 mm wafer deposition chamber such that controlled particle densities can be deposited thermophoretically. With nanocrystal deposits of 10¹⁵ cm⁻³, contaminate of transition metals and other elements can be controlled to less than 10¹⁴ atoms cm⁻³. We have characterized high aerosol concentration floating gate memory devices using conventional MOS ULSI processing on 200 mm wafers. The aerosol nanocrystal memory devices exhibit normal transistor characteristics with drive current 30 µA/µm, subthreshold slope 200 mV/dec, and drain induced barriers lowering 100 mV/V, typical values for thick gate dielectric high substrate doped nonvolatile memory devices. Uniform Fowler-Nordheim tunneling is used to program and erase these memory devices. Despite thin tunnel oxides, threshold voltage shifts of ± 2 V have been achieved with microsecond program and millisecond erase times at moderate operating voltages. The aerosol devices also exhibit excellent endurance capability with no window closure observed after 10⁶ cycles. Furthermore, reasonable disturb times and long nonvolatility are obtained, illustrating the inherent advantage of discrete nanocrystal charge storage. No drain disturb was detected even at drain biases of 4 V, indicating that little or no charge conduction occurs in the nanocrystal layer. We have demonstrated promise for aerosol nanocrystal memory devices. However, numerous issues exist for the future of nanocrystal devices. These technology challenges and discussions will be discussed as directions for future work.

11:30 AM A5.3
ELUDING METAL CONTAMINATION IN CMOS FRONT-END FABRICATION: NANOCRYSTAL DEPOSITION. Zengtao Liu, Changhoo Lee, Gen Pei, Venkat Narayanan and Edwin C. Kan, School of Electrical and Computer Engineering, Cornell University, Ithaca, NY.

Use of metals in nanoscale CMOS structures offers many attractive device features. Metal gate is void of poly depletion or dopant penetration, and provides the design choice of work function to eliminate threshold adjustment by channel doping [1]. Nondegenerate doping in nanoscale devices may suffer from position/function fluctuations and insensitivity for fully depleted SOI. Metal nanocrystal floating gate EEPROM cells are much less subject to interface fluctuation and offer lower voltage/longer retention operation. However, their performance depends on source/drain contacts by thin-films [2] or nanocrystals [4] that can eliminate the need for doping entirely in CMOS and reduce the sheet/ front contact resistance [5].

However, metals are conventionally forbidden in the front-end fabrication before the relatively thick CVD oxide (≈1000 Å) is deposited over poly gate layers, especially for short-channel and shallownanogate devices. Metals can contaminate oxide and Si by junction spiking, grain boundary widening, mismatched expansion and deep diffusion during later thermal cycles, which can cause serious damage to channel mobility, minority lifetime, interface states and oxide quality [6]. We have demonstrated that metal contamination can be eliminated with careful prealignment by the use of metal in RTA (also called nanocrystal self assembly or ripening). If nanocrystal formation dominates over the other processes during RTA, later thermal cycles including source/drain dopant activation will not cause metal nanocrystals to decompose. This assumption is corroborated by monitoring MOSC deep depletion holding time (for minority lifetime), accumulation-to-inversion transition (for interface states), gate leakage current (for oxide traps), and MOSFET channel universal mobility (for Si traps) for structures containing metals (Al, Ag, Pt, and W) on thin gate oxide (≈7 nm). This newly observed phenomenon has provided an effective integration option for using metals in the front-end process. Thicker continuous metal films can also potentially be achieved by thinning thin metal layers or nanocrystals.

11:45 AM A5.4
CAPACITANCE-VOLTAGE HYSTERESIS IN THE METAL- OXIDE-SILICON-CONDUCTOR OR ELECTRONIC INSTABILITY (MOSCEI) EFFECT ON SILICON NANOCRYSTALS DEPOSITED BY THE GAS EVAPORATION TECHNIQUE. Puspamie Mishra, Shinji Nokami, Ryuta Sakurai, Hiroshi Morishki, Hiroshi Onda, Kazuo Uchida, Department of Electronic Engineering, The University of Electro-Communications, Tokyo, JAPAN.

Capacitance-voltage (C-V) hysteresis was observed in the metal-oxide-semiconductor (MOS) capacitor with silicon nanocrystals. The MOS capacitor was fabricated by thermal oxidation, and the silicon nanocrystals, which were deposited on an ultrathin thermal oxide grown previously on a p-type Si substrate. The Si nanocrystals were deposited by the gas evaporation technique with a supersonic jet nozzle. This technique has been developed to deposit Si nanocrystals at the supersonic speed resulting from the differential pressure between the evaporation and the deposition chamber. The size of nanocrystal is precisely controlled by the gas pressure and the distance of the nozzle from the evaporation boat. The size uniformity and crystallinity of the Si nanocrystals are found to be better than those fabricated by the conventional gas evaporation technique. The MOS capacitor consists of 2 nm tunnel oxide and 13 nm oxide with 3-5 nm nanocrystals and exhibits hysteretic kink in the C-V characteristics. In contrast, the MOS capacitors without the nanocrystal do not show any hysteresis. The hysteresis is attributed to electron charging and discharging of the nanocrystal, which function as a charge storage. Positive and negative charges are achieved at small gate voltages in the direct tunneling regime. The flat band shift depends on the size and density of the nanocrystal and the gate voltage. Higher positive gate voltage leads to greater flat band shift, indicating storage of more number of electrons in the nanocrystals. The retention characteristic of the above structure has also been studied. The MOS structure with Si nanocrystals deposited by the gas evaporation technique has proved to be a good candidate for nanocrystal memories.

SESSION A6: GROWTH OF NONSTRUCTURED MATERIALS
Chair: Michele L. Ostran
Tuesday Afternoon, November 27, 2001
Room 202 (Hyne)

1:30 PM A6.1
LOW PRESSURE CHEMICAL VAPOR DEPOSITION OF Si NANOCRYSTALS FOR NON-VOLATILE MEMORIES. B. Rao, K. Scheer, G. Malyvannitham, R. Muralidhar, M. Rosson, B. Nguyen, B. White, Materials and Structures Labs, Materials SPS, Austin, TX.

Si nanocrystal based non-volatile memories are increasingly attracting research effort due to their low voltage operation, long retention and fast write times. A critical technology issue in the fabrication of these devices is the uniform deposition of a high density (of the order of 10¹⁵cm⁻³) of Si nanocrystals without inducing conductence. Such a high density of Si nanocrystals is not easily achieved on SiO₂ substrates. Numerous efforts have focused on obtaining a high density of nanocrystals through a variety of deposition techniques including aerosol technique, sol-gel technique, ion-implantation, low pressure chemical vapor deposition (LPCVD), molecular beam epitaxy and cluster beam evaporation. We have grown Si nanocrystals on SiO₂ and Si₃N₄ substrates by LPCVD and characterized the size and density of these nanocrystals using atomic force microscopy, scanning electron microscopy and transmission electron microscopy. This paper will explore the nucleation and growth mechanisms of Si nanocrystals deposited by LPCVD on dielectric surfaces. Specifically, the nucleation curves from incubation to confluence will be compared on different substrates, the influence of precursor gas partial pressure and substrate temperature on the nucleation and growth characteristics will be investigated in terms of the size and density of the Si nanocrystals. Furthermore, the influence of different precursor and carrier gases will also be compared.

1:45 PM A6.2
GROWTH OF Si NANOCRYSTALS VIA PHYSICAL AND CHEMICAL VAPOR DEPOSITION. T. Lorch, G. Malyvannitham, Jinzhong Zhu and D. Ekerdt, Department of Chemical Engineering, University of Texas, Austin, TX, R. Rao, K. Scheer, R. Muralidhar, B. Nguyen, B. White, M. Rosson, Materials and Structures Labs,
2:00 PM A06.3

**SILICON QUANTUM DOTS ON DIELECTRICS: ELUCIDATING KINETICS OF NUCLEATION FORMATION, NUCLEATION AND DOT GROWTH**

W. Thomas Leech, Jianzhong Zhu, John G. Ekerdt, The University of Texas at Austin, Dept. of Chemical Engineering, Austin, TX.

Routes to high density and uniform size Si quantum dots on SiO2/ and Si3N4/Si(100) substrates for use in quantum dot flash memory applications are presented. The kinetics of nucleation formation, nucleation and dot growth are studied by depositing Si quantum dots onto the substrates through conventional thermal chemical vapor deposition (CVD) with disilane and by physical vapor deposition from a hot wire over which disilane is cracked. A computer simulation is presented that predicts dot density and size distributions based on growth conditions, and correlation with our other published data is demonstrated. Finally, we describe theoretically how to fabricate high-density dots of uniform size by controlling the substrate flux onto the substrate and the diffusion length. Dots grown according to these principles are presented with densities as high as \(9 \times 10^{12}\) dots/cm².

2:15 PM A06.4

**LPCVD DEPOSITION TECHNIQUES FOR NANOGRAIN SUB-10NM POLYSILICON ULTRA-TIN FILMS**

Serge Ecco, Didier Bouvet, Adrian M. Ionescu, Pierre Fazan, Swiss Federal Institute of Technology, Electronic Laboratories, Lausanne, SWITZERLAND.

This work evaluates the limits of three different approaches to achieve the deposition of a nanograin ultrathin (<1 nm) polysilicon film for Single-Electron Device (SED) (i) Direct polysilicon (poly-Si) deposition. Because of the high deposition rate of poly-Si around 620°C, films become porous for thickness below 30 nm, though grain sizes between 30 nm and 300 nm are good. A good choice to reduce porosity is to dilute the silane in hydrogen, helium or nitrogen to decrease the growth rate, a tuning of the deposition temperature allowing a good control of the grain size. (ii) Hemispherical Silicon Grain (HSG) deposition. The size and density of the HSG are influenced by deposition temperature and time during deposition and in-situ annealing of the film. The paper demonstrates the feasibility of HSG with sizes around 50nm and the potential extension of the proposed method for sizes less than 10nm. (iii) Amorphous silicon (a-Si) deposition followed by a crystallization anneal. The key factor to obtain a uniform layer with the a-Si crystallization process lies in a good control of the nucleation phase at the early stage of deposition. At 550°C, with a silane pressure of 15 mTorr, the film appears to be porous for a 10 nm thick layer. Hence, we identified three different ways to raise the density of nuclei: replace the Si2H6 by Si2H8, increase the pressure of silane, or dip the wafer into a 10% H2 Si2H6 solution prior to deposition. We have succeeded in the deposition of uniform poly-Si layer ranging from 5 nm to 10 nm with equivalent grain sizes. As a conclusion, it is worth noting that the deposition of nanograin, ultrathin polysilicon films involves processes not in both nucleation and milling phases. It was found that the a-Si crystallization process seems to be the best candidate for polysilicon films and grain sizes less than 10 nm.

2:30 PM A06.5

**Si/SiGe NANOSTRUCTURES FABRICATED BY ATOMIC FORCE MICROSCOPY OXIDATION.** Xing-Zhong Bu, Leonid Robinson, Huizhan Yin, D.C. Tsui, J.C. Sturm, Center for Photonics and Optoelectronic Materials, Department of Electrical Engineering, Princeton University, Princeton, NJ.

There is a great interest in the ability to pattern Si/SiGe structures with small features using processes which do not cause radiation or etching damage. Recently, silicon has been locally oxidized by atomic force microscopy (AFM) writing in air with feature size down to 1.830 nm. In this work, we have extended this method of AFM oxidation to strained SiGe alloys using a controlled humidity environment. The writing creates a raised surface feature because of the volume expansion associated with oxidation. The effects of oxidation parameters, such as bias voltage on the microscope tip, tip writing speed, and tip tapping amplitude on the line-width and oxide height on SiGe have been investigated and compared with oxidation on Si. It was found that when bias voltage increases, and for when the tip writing speed decreases, the oxidation height of silicon germanium increases. Minimum line widths of 25 nm were achieved both in the oxide feature and in the SiGe after the oxide was removed by wet etching. Typical writing speed are about 0.1-1 micron per second. In contrast to conventional thermal oxidation, the oxide height on SiGe alloys is slightly less than that on Si. Finally, this method was used to successfully cut SiGe quantum well lines with high resolution and confirmed electrically, which demonstrated the first use of AFM writing to pattern Si/SiGe device structures. This work was supported by ARO-MURI DAA04-01-1-0270.

2:45 PM A06.6


Using several self-organizing processes we grow the smallest Si-based nanostructures currently known. They consist of a cylindrical Si core and nanorod Si-based envelope. A morphology of the envelope as well as its crystalline structure are controlled by changing growth conditions such as a growth temperature, rate of Si-atoms flux, etc. The heterostructures were characterized by different high-resolution instruments (CM 200UT Philips, EM1000EX Joel, IM6 4Fiber, PHI 600 Perkin-Elmer, etc.) and reveal a high stability of their physical properties.

SESSION A7: NANO-SCALE DEVICES

Chair: Harry A. Atwater, Tuesday Afternoon, November 27, 2001

Room 202 (Hynes)

3:30 PM A7.1

**SILICON SINGLE-ELECTRON TRANSISTORS AND SINGLE-ELECTRON CCD.** Yasuo Takahashi, Akira Fujiwara, Yukinori Uno, Hiroshi Inokawa, and Kenji Yamazaki, NTT Basic Research Laboratories, Atsugi, JAPAN.

Single-electron transistors (SETs) are advantageous for future large-scale integration because of their ultralow power consumption and small size. The most difficult issue in fabricating SETs is to make a nano-scale two-dimensional Si wire sandwiched between tunnel capacitors at both ends. We have developed a method called PADOX (Pattern-Dependent Oxidation) [1,2], that exploits a special phenomenon that occurs when a Si nanostructure is thermally oxidized. PADOX converts a small one-dimensional Si wire to a tiny SET in a self-aligned manner. The basic mechanism of this conversion is that the oxidation causes huge stress to accumulate in the middle of the wire. This produces a potential dip in the middle of the wire since the strain due to the stress reduces the band-gap energy. In addition, the quantum size effect in the whole wire increases the effective bad gap there. This result in a potential profile for a SET. We have demonstrated the integration of SETs to embody various circuits, such as a half-adder and multi-level binary logic circuits [3].

We have also developed another device that enables us to manipulate a single electron without attaching tunnel capacitors [4]. The device utilizes small Si wire MOSETs connected in series, and an elemental change can be transferred like in a CCD. In addition, we can sense the existence of the elemental charge (single hole) by using electron current since the device employs the electron-hole-coexistence system where electrons and holes are separated in space by large electric...

4:00 P.M. A7.1

We developed a novel patterning technique for ultrathin, single-crystalline CoSi2 layers to produce functional silicon/Si structures. The method, involving only conventional optical lithography and standard silicon processing steps, uses controllable-stress engineering to exploit the synergetic effects of the CoSi2 layer on the silicide structure. The silicide/silicon interface is atomically abrupt and the CoSi2/Si layers are grown simultaneously on 44 nm, and typically 55 nm, thick Si substrates by using molecular beam epitaxy (MBE). Commercial SOI layers were doped using a furnace oxidation process. High quality, thermally stable single-crystalline silicon layers were produced on both types of substrates.

4:15 P.M. A7.2
HETEROGENEOUS ELECTRICAL PROPERTIES OF SiGe NANOSTRUCTURES DETERMINED BY ELECTRIC FORCE MICROSCOPY. E. B. Baranowski, P. Raghebrecht, D. E. Savage, M. G. Lagally, M.A. Eriksson, University of Wisconsin-Madison, Madison, WI.

Future integrated circuits may exploit nanostructures and nanoelectronics in place of conventional materials in CMOS devices. Arrays of electrically isolated SiGe self-assembled 3D quantum dots (QDs) could provide exceptionally thin and well-controlled nanostructured gates. The use of electrically isolated layers on SOI wafers can enable electrical isolation of neighboring QDs from each other. Electric force microscopy (EFM) allows measurements of electric field gradients, providing a powerful method for investigating the nanoscale electrical properties of SiGe QDs. We have patterned thin SOI (5 nm silicon) into various with widths ranging from 5 to 20 nm. When germanium is deposited on these mesas, the resulting QDs grow in concentric rings beginning at the edge of the mesas; the QDs vary in size across the mesas, with the largest QDs found near the edge. Atomic force microscopy and transmission electron microscopy measurements indicate that QDs in the outer rings are separated from each other by oxide, whereas QDs toward the center of the mesas are connected by a thin silicon layer. EFM measurements support this interpretation, indicating that the outer rings of QDs are significantly different from the QDs in the inner rings. In comparison, QDs grown on patterned bulk silicon display a uniform EFM signal. This work supported by NSF.

4:30 P.M. A7.4
LAYERED TUNNEL BARRIERS FOR SILICON BASED NONVOLATILE MEMORY APPLICATIONS. Julie D. Camperon, Harry A. Atwater, California Institute of Technology, Pasadena, CA; I. Douglas Bell, Jet Propulsion Laboratory, Pasadena, CA; Brett W. Busch, Laila Mandal, Martin L. Green, Agere Systems, Murray Hill, NJ.

Among the main performance limits of floating gate nonvolatile memory devices, such as flash memories and nonvolatile memories, are the long program time (~1 μs) and erase time (~1 ms) achievable in a Fowler-Nordheim tunneling mechanism. We demonstrate that by using a floating gate through a homogeneous tunnel barrier. An interesting alternative to homogeneous dielectric tunnel barriers is a silicon compatible layered tunnel barrier, which enables a large drop in the barrier height with applied voltage. To assess the performance of layered tunnel barriers, we have performed simulations and experiments with amorphous dielectrics on Si[100]. Tunneling probability simulations for layered tunnel barriers have been performed using an effective mass model. By numerically solving over all angles and energies, we naturally include a wide range of possible transport mechanisms such as thermionic emission, Fowler-Nordheim tunneling, and tunneling through the Schottky barrier of the layer. Within this simulation, transmission properties are calculated using numerical methods allowing for analysis of resonant tunneling effects and localized charge densities in potential minima.

Using this model we have calculated the current-voltage (I-V) characteristics so that we can optimize the layered tunnel structure.

Ideal we would like the ratio of the current density at some maximum voltage to the current density at some minimum voltage to be at least as large as 10^6 to correspond to a device with a retention time of at least 30 years and a programming time of about 1 μs. Using this model, we have investigated different transport mechanisms as a function of layer thickness in order to optimize the tunnel barrier structure for a thin middle barrier. We expect an appreciable direct tunneling current, and for a thicker structure we expect thermionic emission to dominate.

Several specific barrier structures have been investigated, including SiN4 / Al2O3 / SiN4 and ZrO2 / Al2O3 / ZrO2. We have performed calculations on a 6 nm SiN4 / 6 nm Al2O3 / 6 nm SiN4 / n-Si dielectric heterostructure with assumed conduction band offsets with respect to the Si conduction band of 2.4 eV and 2.8 eV for the SiN4 / Al2O3 / SiN4 respectively. As long as the model is identical structure on p-type silicon where the valence band offset is 1.8 eV and 4.9 eV respectively. For these structures, the tunneling probability varies much more rapidly with applied bias than for a homogeneous silicon barrier. For p-type silicon tunneling barrier.

For example, in an applied bias for the described 3-layer structure from 0 V to 2.5 V the p-type SiO2 yields a theoretical change in tunneling probability by 15 orders of magnitude compared with only 8 orders of magnitude obtainable with a single 6 nm Al2O3 layer.

We have fabricated the layered barrier structures SiN4 / Al2O3 / SiN4. The SiN4 was made by low-pressure chemical vapor deposition, and the Al2O3 was made by physical vapor deposition and atomic layer deposition. We have also fabricated single-layer barriers of Al2O3 and double barriers of SiN4 / Al2O3. A comparison of the current-voltage and capacitance-voltage characteristics of these two structures will be discussed as well as the structural characteristics.
A8.4 MATERIAL ISSUES IN Si/Ge QUANTUM CASCADE STRUCTURES. T. Roch, M. Meduna, J. Stengl, T. Fromherz, G. Baurer, Physics Dept., University of Vienna, AUSTRIA; G. Delinger, L. Diehl, U. Genmer, G. Gerstlmaier, LM-PHI, SWITZERLAND.

Si/Ge based quantum cascade (QC) emission structures exhibiting well resolved electroluminescence at about 105 mV involving heavy hole intersubband transitions have been reported recently (Delinger et al., Solid Stat. Com. 114, 2927-2931 (2001)). In order to improve their properties we have designed, grown and studied several quantum cascade structures with overall thicknesses of about 900 nm and Ge contents in the SiGe wells of more than 40%. In the SiGe QC emission devices the active region consists of an injector, the active quantum well and the collector, which is repeated four times and forms a QC block. The entire structure consists of four such QC blocks. Graded SiGe layers and 100Å thick Si spacer layers were introduced to reduce the Ge content to about 10% to avoid plasma relaxation. Using x-ray diffraction (XRD) scans and reciprocal space maps we show that such structures can be grown completely pseudomorphic on (001) Si at 350°C. With XRD maps we probe the entire layer stack and a sample area of several mm is illuminated.

Our results prove together with TEM investigations the absence of extended defects. From specular x-ray reflectivity scans (dynamic range >8 orders of magnitude) and reflectivity reciprocal space maps we determine that the entire system of QC stacks exhibits negligible thickness fluctuations, an rms interface roughness which increases from 2Å at the first interface only to 2.5Å the top of the entire cascade structure. From the reciprocal space maps we derive the reflectivity reciprocal space maps and their simulation we deduce that the interface morphologies within one cascade block are vertically correlated.

A8.5 SIZE AND SURFACE-DEPENDENT ELECTRICAL TRANSPORT IN SILICON NANOWIRES. Lincoln J. Lashley, Yi Cui, Charles M. Lieber, Harvard University, Department of Chemistry and Chemical Biology, Cambridge, MA.

The future of electronics continues to be in miniaturization, and nanoelectronic devices are emerging as a viable technology for nanoscale interconnects and devices. A key concern of nanoscale devices, regardless of fabrication method, is the increasing dominance of interfacial over bulk properties in determining device performance. In particular, the potentially deleterious consequences of surface scattering and interfacial trapping need to be addressed. We have studied the size dependence of the field effect mobility in n and p-type silicon nanowires grown by nanosphere-confined chemical vapor deposition. We have measured mobilities comparable to and even exceeding bulk values for wire diameters as small as 5 nm. These findings demonstrate the viability of using ultrasmall silicon nanowires as interconnects. In addition, the wire conductance is found to be highly sensitive to the state of the surface oxide. Chemical functionalization of this oxide may therefore be used to [1] mitigate environmental effects for utilization as interconnects; [2] rationalize the previously-built environmental sensor functionality into the wire itself. The ultimate sensitivity limits of the smallest nanowire sensors will be discussed.

A8.6 PHOTOLUMINESCENCE OF Si-SC HETEROSTRUCTURES AND QUANTUM DOTS. E. Ribeiro, Laboratorio Nacional de Luz Sincrotron, Campinas, SP, BRAZIL; E. F. da Silve Jr., Departamento de Fisica, Universidade Federal de Pernambuco, Recife, PE, BRAZIL; V. A. Freire, V. Lemos, Departamento de Fisica, Universidade Federal de Fortaleza, Fortaleza - CE, BRAZIL; Y. Itoha, F. Watanabe, T. Motooka, Department of Materials Science and Engineering, Kyushu University, Hikosaki, Fukuoka, JAPAN.

SiC is an important semiconductor material for the fabrication of high-power electronic devices, designed to work at elevated temperatures and high voltages. The cubic silicon carbide, 3C-SiC, was found to be the only polypeptide which can be epitaxially grown on Si(001) substrate. Several studies report on the growth of 3C-SiC on Si substrates but just a few have successfully achieved the reverse epitaxial growth on 3C-SiC. This makes it possible to fabricate Si-based quantum devices, such as tunneling diodes, using very thin 3C-SiC films as electron barriers [1]. Due to the lattice mismatch between 3C-SiC and Si, it is possible to obtain Si quantum dots embedded into 3C-SiC, which could be useful for developing light-emitting devices and Si-based LEDs. We present low-temperature photoluminescence (PL) of a thin film of 3C-SiC grown on Si(100) substrate, capped with Si (sample 1), and of Si quantum dots embedded in 3C-SiC (sample 2). The 3C-SiC layer was grown by the pulsed supersonic free jets method [1]. PL emission of sample 1 is shifted to lower energies compared to the bulk 3C-SiC, due to the tensile strain. Considering the experimental values for the bulk 3C-SiC and for its elastic constants, together with theoretical predictions, we determined a tensile strain in the 3C-SiC layer to be 2.7% (strongly relaxed). For sample 2, the PL peak is broader and also shifted to lower energies, again indicating the presence of a tensile strain. To evaluate the strain in this situation, it would be necessary to develop a model considering the shape of the 3C-SiC capping layer, and how the film interacts with this strain. [1] Y. Itoha, T. Endo, F. Watanabe and T. Motooka, Appl. Phys. Lett. 75, 3977 (1999).

A8.7 QUANTUM CONFINEMENT ON THE VIBRATIONAL PROPERTIES OF SILICON NANOWIRES. C.R. A. Adv. S. Bhattacharya, and P.C. Bhakta, Dept. of Physics, Pennsylvania State University, University Park, PA; E. Fischer, Department of Material Science and Engineering and Laboratory for Research on the Structure of Matter, University of Pennsylvania.

We present results of Raman spectroscopy (RS) and Photo-luminescence (PL) on silicon nanowires prepared by pulsed laser vaporization of hot targets in an inert atmosphere. Targets of Si:1% Au, Si:1% Fe and Si:1% Ni were used to produce crystalline Si nanowires in the diameter range 5-15 nm and with lengths exceeding 1μm. The materials were observed to be highly crystalline via the observation of well defined, periodic HREM fringes extending over long distances. A large redshift, up to 25 cm⁻¹, of the first order Raman-active transverse optical phonon compared to bulk silicon has been observed along with an increase of line width of ~30 cm⁻¹. The nanowire phonon linewidth is in terms of the narrowing of the 139 cm⁻¹ phonon branch dispersion and the range of allowed q vectors activated by quantum confinement. This signature of strong phonon confinement in the wires is supported by our PL emission data in the red region (1.61 eV) where, a blue shift is observed relative to bulk Si. This work was supported by NSF MRSEC (UPenn).

A8.8 CV AND G-V MEASUREMENTS SHOWING SINGLE ELECTRON TRAPPING IN NANOCRYSTALLINE SILICON DOT EMBEDDED IN MOS MEMORY STRUCTURE. Shuyan Huang, Souj Sriberse, Shunori Oda, Tokyo Institute of Technology, Research Center for Quantum Effect Electronics, Tokyo, JAPAN.

The mechanism of single electron trapping in nanocrystalline silicon (nc-Si) dot has recently attracted great interest for further understanding the single electron memory (SEM) device performance [1]. Fast write/erase and long charge retention time, which are strongly influenced by the interface and barrier states, are major concerns. Capacitance-Voltage (C-V) and Conductance-Voltage (G-V) measurements are useful tools to study semiconductor interfaces and charge trap mechanism as well as the charge storage behavior in nanostructures. The SiO₂/nc-Si/SiO₂ sandwich Metal-Oxide-Semiconductor (MOS) diode has been prepared on 100Å thick nc-Si layer with an ultrathin SiO₂ layer of 2nm in thickness. The remotePECVD method is employed to fabricate nc-Si dots of 8nm in diameter [2]. The dots thus prepared have a narrow spread and a density of about 10⁸ cm⁻². A comparatively thicker upper oxide was deposited by TEOS PECVD technique. The CV and G-V characteristics were obtained by sweeping the voltage up and down between inversion and accumulation region. Clockwise hysteresis in both C-V and G-V characteristics were observed. Notable in the C-V curve is the presence of a peak that flips to the flat band voltage, in forward and backward measurement, indicating that a trap event has occurred. In contrast, neither obvious hysteresis in C-V nor a peak in G-V characteristics was observed in the samples without dots. The results of C-V associated with G-V indicate a single electron trapping per n-Si dot leading to a clear memory effect. In the time dependent capacitance measurement, a memory retention time exceeding 10⁵ s was confirmed in this memory device. The charge storage mechanism in this memory device will be discussed in detail [1]. [1] M. Detchprohm et al., Mat. Res. Soc. 2000 Fall Mtg. F2.2, Proceedings 388 in press [2]. T. Hikuto et. al. Jpn. J. Appl. Phys. 36 (1997) 4031.

A8.9 ELECTRICAL CHARACTERIZATION OF CARRIER CONFINEMENT AND THERMALIZATION IN Si/SiGe NANOSTRUCTURES. F.S. Fish, D.E. Swango, P. Huegh, K.A. Schierle, M.A. Ericsson, D.P. Ehrat, University of Wisconsin-Madison, Madison, WI, Y. Zhao, Keithley Instruments, Cleveland, OH.

Semiconductor quantum dots have been studied intensely because of their potential for nanoelectronic or optoelectronic devices. In particular, understanding of the transport properties of SiGe-based quantum dots is increasingly vital, as applications are seen in devices such as integrated electronic memories and II detectors. To design these structures, fundamental quantities, such as the carrier energy
levels, band offsets, and Coulomb charging effects, are needed. We report here the results of space charge spectroscopy of ensembles of SiGe quantum dots grown using UHV-CVD. The quantum dot ensembles were grown, with densities ranging from $10^{10}$ to $10^{11}$ cm$^{-2}$ and lateral sizes from 15 nm to 70 nm, in the neutral region of Schottky diodes on highly p-doped wafers. Admittance spectroscopy was performed in voltages ranging from 0 to 1 V and temperatures from 20K to 300K. Changing the applied bias sweeps the Fermi level through the dot's energy levels, allowing direct modification of the diode's conductance. Energy levels within the dots are then characterized using the equivalent parallel circuit model. We compare these results to carrier emission from regions of lateral confinement created by local stressors on a SiGe quantum well. We use a hybrid ensemble of quantum dots as the stressors. By varying the thickness of the Si spacer layer separating the dots and the well, we can controllably adjust the 'depth' of the strain-induced quantum dots (SiQDs) while maintaining the precise control of thickness and composition in the quantum well. Research supported by AFOSR and NSF.

SESSION A9 Advanced CMOS Gate Stack and Metallization
Chair: William G. En
Wednesday Morning, November 28, 2001
Room 202 (Hynes)

8:45 AM A9.1 EQUILIBRATION OF CATIONIC METALS FOR DUAL-METAL GATE CMOS USING HIGH-K GATE DIODELECTRICS

As the MOSFET gate lengths are scaled down to 50 nm or below, the expected increase in gate leakage will be countered by the use of a high dielectric constant (high K) material. The series capacitance from the polycrystalline gate dielectric depletion becomes a significant fraction of the actual capacitance from the gate dielectric as the dielectric thickness is scaled down to 15 Å equivalent oxide thickness (EOT) or below. Metal gates promise to solve this problem and address other issues like boron penetration and increased gate resistance that will have increased focus as the polycrystalline gate electrode dimensions are scaled down further. Extensive simulations have shown that the optimal gate work-functions for the sub-50 nm channel lengths should be 0.2 eV below (above) the conduction (valence) band edge of silicon for n- and p-MOSFETs (p-MOSFETs).

In addition to the work-function requirements, the metal gate and the high-k gate dielectric should be mutually compatible and not inter-diffuse or react at the MOSFET thermal budget. This study evaluates the dielectric, TaSiN, WSi, and TaSi as candidate metal for dual-metal gate CMOS using high-K gate dielectric. The work-functions of different fixed charge levels were determined by fabricating MOS capacitors with varying dielectric thicknesses. The metal-dielectric compatibility and thermal stability was studied by annealing the capacitors at different temperatures and backside etching the TaSiN and X-ray diffraction. Of the metals evaluated, TaSiN shows most promise as a candidate gate electrode for HfO$_2$ p-MOSFETs. None of the metals studied had work-functions suitable for HfO$_2$ n-MOSFETs.

9:00 AM A9.2 INITIAL GROWTH OF SILICON GERMANIUM FILMS ON ZIRCONIUM ON THE D. W. Kim, F. E. Pines, H. Y. Lee, K. C. Vawter, M. A. Beller, B. M. Johnson, Westinghouse electronics Research Center, The University of Texas at Austin, Austin, TX.

Recent efforts on scaling silicon dioxide in standard complementary metal-oxide-semiconductor (CMOS) technology have focused on alternate gate dielectric materials. However, most high-k dielectric materials are not thermally stable in direct contact with silicon. An interface layer between the high-K dielectric materials, Si substrate and Si poly gate is necessary to prevent the interface reaction. Therefore, the investigation of alternate gate electrode materials is desirable. Polycrystalline silicon-germanium (poly-SiGe) has recently been shown to be a potential alternative to polycrystalline silicon (poly-Si), for advanced submicron devices. The advantages of poly-SiGe over poly-Si include low process temperature, low activation energy of dopants, in-depth, more appropriate gate work-function and higher current drive. However, the use of poly-SiGe film formation and nucleation which are known to control the film structure and hence film properties are not clearly understand. In this study, the initial growth characteristics of a SiGe film realized by ultrahigh-vacuum chemical vapor deposition (UHV-CVD) using Ge$_4$ and disilane on high-K gate oxide, ZrO$_2$, has been investigated within the temperature range from 450$^\circ$C to 500$^\circ$C. The interface surface reaction on growth characteristics such as the incubation of growth, roughness distribution of SiGe, and the interface reaction of the SiGe film with ZrO$_2$ are specially focused on. For this purpose, atomic force ranging field (AFM), Auger electron spectroscopy (AES), X-ray photoelectron spectroscopy (XPS) and transmission electron microscopy (TEM) were used. From our analysis we conclude that ZrO$_2$ reacts with Si and forms zirconium silicide in the temperature range of 450$^\circ$C to 500$^\circ$C. The surface roughness of the morphic SiGe layers increase from 0.5nm to 1.5nm with increasing Ge content from 0.1 to 0.3. A further increase in surface roughness is observed from 1nm to 5nm as SiGe layer transfer transition from amorphous to poly crystalline layer.

9:15 AM A9.3 STRUCTURE AND STABILITY OF ALTERNATIVE HIGH-K GATE DIODELECTRICS ON SILICON S. Steiner, Department of Mechanical Engineering and Materials Science, Rice University, Houston, TX; D. W. Kim, J.-P. Merin and A.I. Kingon, Department of Materials Science and Engineering, North Carolina State University, Raleigh, NC.

Technology roadmaps predict that continued scaling of complementary metal-oxide-semiconductor devices will eventually require a gate dielectric with a capacitance equivalent to that of SiO$_2$ of less than 1.5 nm thickness, a thickness regime where tunneling current becomes unacceptable high for many applications. Replacing SiO$_2$ with a material with a higher dielectric constant (high-K) material would allow physically thinner films to achieve the required capacitance values. Two important issues are the thermal stability of the alternative gate dielectric on silicon and the electrical quality of the interface. To investigate these issues in a microstructural characterization method is required that not images gate stacks but that can also analyze the composition and electronic structure with atomic spatial resolution. Here we use electron energy-loss spectroscopy (EELS) in transmission electron microscopy with a sub 0.2 nm probe. We have investigated La$_2$O$_3$/SiO$_2$/Si and ZrO$_2$/SiO$_2$/Si structures with well-characterized electrical and dielectric properties before and after rapid thermal annealing. ERT at different temperatures and oxygen partial pressures. Results show that after RTA at 600$^\circ$C, the La$_2$O$_3$ layer on a thermal SiO$_2$ remained amorphous. After 850$^\circ$C RTA, crystallizes were observed in the original La$_2$O$_3$, and the total oxide layer thickness increased by 17%, most likely due to oxygen diffusion and reaction at the Si/SiO$_2$ interface. EELS showed that RTA at 600$^\circ$C did not cause significant La diffusion into the SiO$_2$ layer, whereas some amorphous oxidation was observed at 800$^\circ$C. Equivalent oxide thickness (EOT) estimated from the microstructures are found to closely correspond to results from capacitance-voltage measurements. For example, a La$_2$O$_3$ layer grown on a chemical SiO$_2$ and subjected to RTA at 1000$^\circ$C showed an EOT of 1.8 nm. We investigate the interfacial composition of ZrO$_2$/SiO$_2$/Si structures, and quantify the amount of interfacial ZrO$_2$ ZrO$_2$SiO$_2$ in four different annealing atmospheres. Results of EELS fine-structure analysis of interfaces will be presented and provide an understanding of the electrical and dielectric behavior of the films.


Silicon nitrides are commonly used in microelectronic applications where achieving a targeted stoichiometry is crucial for successful operation of the device. For example, resistive coatings in lithography, gate dielectrics, and final passivation require either silicon rich, nitrogen rich, or stoichiometric SiN films. Stoichiometry is primarily determined by Rutherford Backscattering Spectroscopy (RBS), because it requires no standard. However, RBS is not a viable option for quick, in-line measurements. This work focuses on the film stoichiometry determined by spectroscopic ellipsometry (SE), a non-invasive technique in which the Total Gap (ET) is related to composition. Measurements were performed on a set of films whose nitrogen ratios range from 38% to 56% as determined by RBS. Ellipsometric angles (psi and Delta) were obtained from 1500 to 5000 nm on a Jarrell-Ash variable angle spectroscopic ellipsometer (VASE) with a compensator. The data was modeled with a Tauc-Lorentz oscillator model and the optical properties n and k were calculated from the fitted data. Determining n and k from SE allows us to calculate the direct bond density using a model, which was corrected by Rend and Wansier to the Si/N ratio determined by electron microprobe measurement. We compare the
cutoff wavelengths determined by a commercial Hewlett-Packard UV/VIS spectrometer and our ellipsometer. We also compare the stoichiometry from (1) the calibration curve, (2) directly measured by our RBS analysis, and (3) the Taue gap using Jellison's correlation between the Taue gap and the stoichiometry.

9:45 AM A9.5 INTERFACIAL DIFFUSION STUDIES OF Hf AND Zr INTO Si FROM THERMALLY ANNEALED Hf AND Zr SILICATES.
Washington University in St. Louis, USA and University of North Texas, Denton, TX, L. Colombo, M. Bevan, M. Douglas, and M. Vacay. SI Technology Research, Texas Instruments Incorporated, Dallas, TX.

Thermal stability of high-κ gate dielectrics on silicon is an important issue for future CMOS devices due to the fact that the dielectric must withstand the very short, but relatively high (~530 s @ 900°C) 1000-hour activation anneal. The high-κ dielectrics used in the device structure are thick (~100 Å) and are thus more susceptible to interfacial defects. High-κ dielectric materials are therefore ideal for testing the effectiveness of the interfacial regions between the dielectric and the Si substrate.

10:45 AM A9.7 POSITION ANNihilation LIFETIME SPECTROscOPY (PALS) APPLICATION IN METAL BARRIER LAYER INTEGRITY FOR POROUS LOW-K MATERIALS. Simon Lin, Jin Xing Sun, David W. Gidley, Jeffrey T. Wetzel, K.A. Mennig, Simon Jung, Doug Yu, and M.S. Liang.
Institute of Physics, University of Michigan, MI 48109.
* Taiwan Semiconductor Manufacturing Co., HsinChu, TAIWAN, ROC.

Cu and low-k dielectric are both applied in the damascene integration in order to reduce RC delay so as to increase the device speed. As dielectric constant [k] is needed less than 2.2 for the 0.1 mm technology as shown in the ITRS roadmap, porous instead of dense low-k is the only way to achieve the goal from the present suppliers. Application of porous low-k into integration introduces the problems of metal barrier integrity. Traditional PALS is introduce to evaluate barrier layer integrity in the early stage. The correlation between PALS screening and single damascene integration for various Silicided-based low-k results is presented. The criterion to achieve good barrier integrity between the barrier thickness and the pore sizes is also discussed. The paper demonstrates that PALS is a useful tool to pre-screen a metal barrier integrity for porous low-k dielectrics. Large scale mono-porous (> 50 Å) low-k will encounter Cu diffusion problems when using SEMATECH in-house PVD Tsi 250a as barrier layer for trench dimension smaller than 0.25 mm. Postcopper (PS) leakage is coregative to bridge current leakage in the electrical tests in pin-holes in the barrier layer. For small scale microporous (< 20 Å) low-k porous barrier, Cu diffusion was observed even with Ta 50A as the barrier layer, which is contributed from sidewall diffusion to close up pores after etch and ash. No PS leakage from pattern wafer by PALS is also correlated to the chemical analysis and cross-sectional TEM analysis. The viable porous low-k (< 50 Å) will be preferential for future technology.

11:00 AM A9.8 DIFFUSION CHARACTERISTICS OF COPPER IN TiN THIN FILMS. Abhishek Gupta, Alex V. Kvit, T.K. Nath and J. Narayan, NSF Center for Advanced Materials and Smart Structures Department of Materials Science and Engineering, NCUST, Raleigh, NC.

We have investigated the diffusion characteristics of copper in monocarbide, polycrystalline and single crystal TiN thin films, which is being used as a diffusion barrier for sub-quarter micron metalization. These films were synthesized on Si < 100 > substrate by first sputtering monocrystalline TiN and then sputtering amorphous copper targets using Pulse Laser Deposition. The three different crystalline structures of TiN were achieved by growing the films at different substrate temperatures, where higher temperatures (~650°C) leads towards epitaxy. Then a uniform thin layer of copper was deposited at room temperature for all the three depositions above. Each sample was annealed at three different temperatures (400°C, 500°C and 600°C) to study the effect of coupling the oxygen diffusion barrier effectiveness of TiN. Study of diffusion profile and the copper concentration measurement were performed using Scanning Transmission Electron Microscopy-Z contrast (0.1 nm resolution), Secondary Ion Mass Spectroscopy, Electron Energy Loss Spectroscopy and Rutherford Backscattering Spectrometry techniques. These data were used to plot the measured concentration of copper with respect to the temperatures for the three crystal structures of TiN to calculate the diffusion coefficients and were compared to study the effect of microstructure of TiN thin film on the diffusion of copper after annealing.

11:15 AM A9.9 Mg EFFECTS ON AGGLOMERATION, ADHESION, RESISTIVITY OF Ag/Mg/SiO2/Si MULTILAYERS. Bongjoo Kang, Yeonkyu Ko, Heejung Yang, Jaegub Lee, Kookmin Univ, School of Metallurgical and Materials Engineering, Seoul, KOREA, Chang-Ho Jeong, Samsung Electronics Ltd, AMD/CDI/Daviex, KOREA.

Ag has received attention as a potential interconnection in ultra-large scale integration and large area T/L/LC because it shows the lowest resistivity among metals and high electromigration resistance. However, several issues such as agglomeration, poor adhesion to SiO2 have to be addressed to implement Ag metadlization into integrated circuits and T/L/LCs as well. The effects of Mg in Ag/Mg/SiO2/Si multilayer films on Mg ion, passivation and, resistivity after annealing in vacuo at 200°C to 500°C have been investigated. Heating Ag/Mg/SiO2/Si multilayer films above 300°C produced surface MgO layer in the Ag interface in MgO/Ag/MgO/SiO2/Si structure. The presence of surface MgO improved the mechanical properties such as high strength, better resistance to diffusion flux and also provided the passivation layer against air, thus leading to the significant enhancement of resistance to agglomeration. In addition, adhesion was remarkably improved due to...
the formation of interfacial \( \text{MgO} \) resulting from the reaction of \( \text{Mg} \) with \( \text{SiO}_2 \). However, the interfacial reaction proceeded to a limited extent and the reaction generated from the reaction has the negligible solubility into \( \text{Ag} \). This limited interfacial reaction between \( \text{Mg} \) and \( \text{SiO}_2 \) in \( \text{Ag} \) is not changed with the unlimited interfacial reaction occurring in \( \text{Cu} \) (\( \text{MgO} \)/\( \text{SiO}_2 \)). The reactivity of \( \text{Ag}(\text{1.5at% Mg}) \) continued to decrease with increasing the temperature and was 2.6 \( \mu\text{m} \text{cm} \) after heating at 500°C.

11:30 AM A9 10

TEXTURE DEVELOPMENT IN Ti-Ta ALLOY DISILICIDE FILMS
A. S. Ong, K. F. Ludwig, Jr., Boston University, Dept. of Physics, Boston, MA; C. Liscoe, C. Cabral, Jr., J. M. E. Harper, IBM Research Division, Yorktown Heights, NY.

The development of texture in blanket Ti-Ta (0.6 at.%) disilicide films has been studied both in situ and ex situ with x-ray diffraction. For pure Ti films on Si(001) substrates, the C49 Ti2Si2 phase develops with [110] poles primarily in the film plane. The final C54 Ti2Si2 texture is dominated by orientations with C54(110) and C54(-110) parallel to Si(111). This suggests that local faceting on Si(111) planes may play an important role in the C54 formation. The addition of Ta causes a change in textures with C54(110) becoming the dominant orientation normal to the substrate. This texture change becomes complete with the addition of 6 at. % Ta, which is an effective alloy composition for the reduction of the C54 formation temperature. On Si(001) substrates, there is also an in-plane preferential orientation with C54(111) || Si(110). In-situ studies show that the C54 texture can evolve during the C54 formation process, possibly due to strain gradients in the film, which are favorable orientations relative to the substrate have the highest growth velocity. This work has been partially supported by NSF-ECR-9515181.

SESSION A10: POSTER SESSION

ADVANCED CMOS GATE STACKS AND METALLIZATION
Wednesday Evening, November 28, 2001 8:00 PM
Exhibition Hall D (Hyatt)

A10.1

Abstract Withdrawn.

A10.2

SYNTHESIS OF TITANIUM SILICATE (Ti-x,SiO2) AS A HIGH-k DIELECTRIC MATERIAL BY O2 IMPLANTATION INTO TITANIUM SILICIDE (TiSi2) FILM
D. F. Sarker, E. Dobrinescu, R. W. Payne and B.L. Stensland, INRS-Materiak and Energy, Varennes, Quebec, Canada.

Recently, a great deal of attention has been paid to finding an alternative gate dielectric material as a substitute for \( \text{SiO}_2 \) in future MOSFET devices due to the expected leakage current through an ultrathin \( \text{SiO}_2 \) layer. The dielectric constant of \( \text{SiO}_2 \) is 3.9 which is very low, while that of \( \text{TiO}_2 \) is 80 which is too high for future applications. We have attempted to synthesize titanium silicate, which should have a dielectric constant between that of \( \text{SiO}_2 \) and \( \text{TiO}_2 \) by implanting \( \text{O}_2 \) into titanium silicide. The titanium silicide film was grown on a crystalline Si(100) substrate by rapid thermal annealing (RTA) of a 20 nm Ti film at 800°C. The sheet resistance of the silicide film is 0.98 \( \Omega\text{f} \). An XPS depth profile shows that the stoichiometry of the film is Ti\( \text{Si}_x \text{O}_{2-x} \) implanted in the silicide film by means of a plasma ion implanter with an energy of 15 keV and a dose of \( \sim 5\times10^{17} \) ions/cm\(^2\). An XPS depth profile has also been obtained from the \( \text{O}_2 \) implanted silicide film. The surface of the \( \text{O}_2 \)-implanted silicide film is contaminated with \( \text{TiO}_2 \) and \( \text{SiO}_2 \) as confirmed by the binding energy of the Ti 2p\( _{3/2} \)/peak (459.0 eV), Si 2p (103.5 eV) and O 1s (530.4 and 532.2 eV). After sputtering for 300 seconds (~5 nm), a Ti 2p\( _{3/2} \)/peak appears at 458.6 eV, a Si 2p component at 103.0 eV and an O 1s peak at 531 eV. The binding energy of the Ti 2p\( _{3/2} \) peak therefore increases while that of Si 2p is reduced in the \( \text{O}_2 \)-implanted silicide as compared to their oxide states; this is characteristic of silicon materials. The dielectric constant of the \( \text{O}_2 \)-implanted silicide film is estimated by measuring the \( \ell \)-V characteristics and fitting the data using the Schottky emission model; and the value obtained is about 30.

A10.3

BIPHOSPHOSILICATE GLASSES FOR SILICON DEVICES
SOL-GEL SYNTHESIS AND SPECTROSCOPIC CHARACTERIZATION

Biphosphosilicate glasses (BPBG) thin films are used in semiconductor manufacturing for insulation between metal interconnections and silicide gate structures because of their low flow tendency and strong interaction toward getter \( \text{N} \) impurities. The detailed glass property behavior in the as-deposited state strongly depends on the elemental composition. In order to understand the dependence of glassy properties on composition, the preparation of BPBG monoliths at different B and P concentrations has been pursued by the sol-gel method. The sol-gel method allows to prepare glasses with a high degree of homogeneity and purity. BPBG have been prepared so far as powders [1] or as monoliths from sol-gels [2], but this is the first time that bulk transparent glasses free of crystals were obtained from sol-gels. Xerogel was prepared by evaporation and condensation in water/methanol of Al(OCH\( _3 \))\(_4\), B(OCH\( _3 \))\(_4\), and P(OCH\( _3 \))\(_3\). Boron and phosphorus contents in the range of 12 mol% percent were considered. The density of xerogel to glasses was performed by a thermal treatment at 973 K in flowing oxygen alternated to reduced oxygen pressure in order to burn residual carbon, to eliminate solvents and to avoid glass cracking. Glass formation was followed by infrared and Raman spectroscopy. Raman-induced point defects were identified by optical absorption and electron paramagnetic resonance (EPR) spectroscopy. Phosphorus-oxygen-hole centers (POHC) [3], boron-oxygen-hole centers (BOHC) [4] and Si\(_2\)-centers were identified, to be correlated with the \( \text{N} \)-related effect. [1] J. T. Kim and P.N. Kamat, J. Phys. Chem. B, 102 (1998) 5734-5738. [2] T. Wainwright, J. Philpott and J. Lizyjcki, J. Non-Crystalline Solids, 63 (1984) 115-120. [3] D.L. Gristom et al., J. Appl. Phys., 54 (1983) 3763-3767. [4] W. Warren et al., Appl. Phys. Lett., 67 (1995) 956-957.

A10.4

FIRST PRINCIPLES - STRUCTURE - FUNCTION RELATIONSHIPS OF NITRIDED OXIDES AND OXYNITRIDES
A. D. Gasparre and P. Takoudis, University of Illinois at Chicago, Department of Chemical Engineering, Chicago, IL.

Thermally grown Si\(_3\)N\(_4\) films in Si\(_3\)N\(_4\) are known to have a higher dielectric constant and a higher \( N \)-concentration than silicon oxides/oxynitrides, but they incorporate \( H \) atoms that induce hot electron carriers during subsequent high temperature processing. Further, silicon nitride is difficult to grow over films thick due to self-limiting growth. One alternative is \( \text{SiO}_2 \) and \( \text{SiN}_x \) films post-nitrided with \( \text{NH}_3 \).

In this work we study the different bonding states in nitrided oxide and oxynitride films with X-ray photoelectron spectroscopy (XPS) and Fourier transform infrared (FTIR) spectroscopy as well as process-state relationships in ambient containing \( \text{NO}, \text{N}_2 \text{O} \) or \( \text{O}_2 \) at 1000°C. Critical parameters of interest also include the \( N \) and \( O \) concentration profiles in nano-scale thin dielectric films and how these profiles change in different processing environments. Experimental data suggests that the presence of \( N \) at different positions within the dielectric films impacts different advantages like retarding boron penetration when present near the dielectric surface or better strain relaxation when present near the dielectric substrate interface.

The detailed concentration profiles of \( N \), \( O \), and \( \text{Si} \) within the dielectric layer with different sputtering times by secondary ion mass spectrometry coupled with the binding energies and bonding states at different depths through our FTIR and XPS spectroscopic studies will be shown to be essentially in agreement with nano-dielectrics with desired \( N \) concentration profiles and in understanding related process-state-function relationships.

A10.5

FILM PROPERTIES OF HIGH-PERFORMANCE FSG FILMS
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FSG films are widely used not only Al-based Technology but also Cu-based devices. New materials for FSG films in recent years. However, there are some requirements for FSG films such as good chemical withstandability against acids, high thermal stability and good adhesion to Cu or Al. In this study, we developed the advanced FSG film (k=8.4), which shows excellent film properties. The feature of new PE-CVD tool as follows. Firstly, the chamber consists of parallel plate electrode, and the RF power is applied from the upper and lower electrode, 60MHz and 2MHz respectively. Furthermore, the FSG processes require a well controlled wafer temperature. The heating method with ESC can easily control the wafer temperature during deposition. The advanced FSG film appears to be superior to the HDP-FSG film by a wide margin in the following tests. The moisture absorption test by TDS (after 4 days of air exposure); about 10%. The best was 8X by the hydroscopicity (after 1 hr. boiling); 3X less. These differences are
mainly due to the good water penetration resistance of the advanced FSG film. The results of RBS measurement show that Si-OH peak is about 90% less in SiOVD FSG film. These properties suggest that it depends on the local structure of FSG films. Further investigations such as EXAFS spectra studies are in progress.

A10.6 Abstract Withdrawn.

A10.7 ALUMINUM OXIDE BASED THIN HIGH-K DIELECTRICS. Pallavi Katiyar, Alex V. Kvit, D. Kumar, J. Narayan, NSF Center for Advanced Materials and Smart Structures, NC A&T and N.C. State University, Burlington Labs, Raleigh, NC.

Conventional scaling of the SiO$_2$ gate oxide thickness has enabled MOS gate dimensions to be reduced to 100 nm or less. We have successfully deposited stoichiometric aluminum oxide between room temperature and 580°C using a pulsed laser deposition technique. The thickness of the deposited oxide was varied from 1-100 nm. Microstructural as well as electrical measurements of aluminum oxide thin film was done in order to study the dielectric properties. The quality of the film was found to strongly depend on the laser and substrate parameters. The high resolution transmission electron microscopy (HRTEM) and electron energy-loss spectroscopy (EELS) were used to study the interface structure of the films. The HRTEM studies showed a sharp and uniform interface between AlO$_x$ thin film and the silicon (100) substrate. The electron energy-loss spectroscopy (EELS) studies showed the absence of any intermixing SiO$_2$ layer. The high and low frequency Capacitance-Voltage (C-V) and current-voltage (I-V) measurement revealed a low leakage current. These results show that AlO$_x$ films are suitable for high-k dielectrics to replace the conventional SiO$_2$ gate oxide.

A10.8 STRUCTURE AND CRYSTALLIZATION OF ULTRATHIN ZrO$_2$ AND Zr SILICATE FILMS. Debra L. Kaiser, Igor Levin, Charles Poulik, Mark D. Vastin, NSF, Ceramic Division, Gaithersburg, MD.

ZrO$_2$ and Zr silicate are leading materials for the replacement of SiO$_2$ gate dielectrics. We have studied the crystallization behavior, structure, and compositional homogeneity of Zr oxide and Zr silicate thin films using high resolution TEM, extended x-ray absorption fine structure (EXAFS) and grazing incidence x-ray diffraction. The films for these studies were fabricated in-house by a metalorganic vapor deposition technique and had thicknesses in the range 2.5 nm to 5 nm. The onset of crystallization in the ZrO$_2$ films occurred at about 500°C; the EXAFS results suggest the presence of two crystalline ZrO$_2$ phases above 500°C.

A10.9 THEORETICAL INVESTIGATION OF THE TUNNELING THROUGH A 1.4 nm MOS AND A DOUBLE BARRIER SiO$_2$-Si$_3$N$_4$-SiO$_2$ STRUCTURES. A.A. Demkov and Xiondong Zhang Physical Sciences Research Labs., Motorola, Inc., Tempe AZ.

We describe a consistent methodology to create structural models of the Si-dielectric interface with a realistic atomic geometry. To construct a Si-SiO$_2$ interface we use a direct quantum molecular dynamics oxidation of the Si (001) surface [1]. A similar approach is used to investigate the initial decomposition of NO on the Si surface. The resulting structures show the interfacial sub-oxide region that amounts to about 0.4 nm. We have constructed several structural models with the dielectric thickness ranging from 0.6 to 0.15 nm. These structures are similar to those of ultra small transistors described in a recent report from Bell Laboratories. In addition, we investigate silicon oxynitrides SiO$_x$N$_y$ which are often observed in the interfacial regions e.g. between the oxide and the nitride. The Internal Center for Materials Research at Notre Dame studied the scaling of CMOS devices will stop about the year 2012. The main reason for this is the leakage through the silicon dioxide gate with a thickness below 4 nm. The modification of the oxide layer to improve the dielectric constant coupled with the understanding of the microscopic nature of the leakage may extend the current materials technology for a few device generations before we will ultimately have to switch to high-k gate dielectric. We investigate the leakage current in ultra thin MOS structures and tunneling through SiO$_x$-SiO$_2$ double barrier structures constructed using the interface models described above. The Landauer ballistic transport theory is used to model the conduction. We employ a t-matrix approach to construct a model that does not use the effective mass approximation and is essentially exact within the LCAO formalism chosen here. In addition, we investigate the effects of the local atomic structure changes, caused by the presence of nitrogen at the interface, on the elastic properties of this fundamental element of the CMOS technology. In summary, we are able to build atomistic models of the interfaces, capacitors and double barrier structures and go all the way up to estimate their transport properties. This is an example of the "bottom up" engineering, where the understanding of the microscopic quantum transport theories can make a real impact. 1. A.A. Demkov and O.F. Sankey, Physical Review Letters 83, 2038.

A10.10 A COMPARATIVE STUDY OF GADOLINIUM OXIDE, GALLIUM OXIDE AND YTRRIUM OXIDE AS HIGH K DIELECTRICS ON SiGe. S. Pal, S.K. Ray, Department of Physics and Meteorology, IIT Kharagpur, INDIA; B.K. Chanda, Nether Physical Laboratory, New Delhi, INDIA; S.K. Lakhi, Department of Electronics and Electrical Communication Engineering, IIT Kharagpur, INDIA; D.N. Bose, Advanced Technology Center, IIT Kharagpur, INDIA.

Enhanced hole mobility and the compatibility of the strained SiGe material system with silicon have attracted considerable attention for applications in complementary metal oxide semiconductor (CMOS) technology. Conventional high temperature (>700°C) thermal oxidation for the growth of gate oxide is not suitable for strained Si$_x$Ge$_{1-x}$ layers as it causes strain relaxation and Ge segregation at the oxide-semiconductor interface. Thus the search for a suitable CMOS gate dielectric continues. Here we report a comparative study of the electrical properties of some novel oxides e.g. Ga$_2$O$_3$, Ga$_2$O$_3$ (Ga$_2$O$_5$) deposited from GGG, Y$_2$O$_3$ and Ga$_2$O$_3$ as gate dielectrics for strained Si$_x$Ge$_{1-x}$ CMOS devices. Experiments were carried out on epitaxial layers of strained Si$_x$Ge$_{1-x}$ (x=0.8) grown by ultra high vacuum chemical vapor deposition (UHVCVD) on an epitaxial Si buffer layer (500 Â) at 580°C on (100) Si (5-1000 cm$^{-2}$) substrates using Si$_2$H$_6$ and Ge$_4$H$_4$. The layers were doped doped in-situ at 1 × 2 ×10$^{17}$ /cm$^3$. Secondary Ion Mass Spectrometry (SIMS) of the Ga$_2$O$_3$ (Ga$_2$O$_5$) / SiGe sample showed significant amount of Ga$_x$O$_{y}$ and Ge$_x$O$_{y}$ along with Ga$_x$ and Ge$_x$ signals. The depth profile taken for O, Si, SiO, Ga, Ge & GaO showed a sharp interface at about 20 nm. C-V and G-V measurements showed that though Ga$_2$O$_3$ and Y$_2$O$_3$ had highest resistivity and breakdown strength, Ga$_2$O$_3$ (Ga$_2$O$_5$) was found to be most effective for surface passivation of SiGe giving lowest interface state density. Pure Ga$_2$O$_3$ on the other hand was found to be incapable of passivating the SiGe surface. The positive fixed charge interface state density for Ga$_2$O$_3$ (Ga$_2$O$_5$) was found to be 8.4 ×10$^{10}$/cm$^2$ and 4.8 ×10$^{11}$/Vcm respectively which are the lowest among all the oxide films. Constant current stressing experiments showed all the oxides exhibited hole trapping during current injection through the gate.


Using grazing incidence x-ray diffraction (GID), we find a fourfold modulation of the sharp diffraction peak (FSDP) of the amorphous structure factor of SiO$_2$ over Si(001) in a 100 Å film grown by furnace oxidation. We propose a model for the SiO$_2$/Si interface structure in which the SiO$_4$ tetrahedra, which form the building blocks of the amorphous network, are locked into the diagonal of the Si surface unit mesh. The model is supported by a-x-ray Reflectivity measurements which reveal an intermediate interfacial layer with an enhanced density, which is confirmed by the radial position of the FSDP. In-plane measurements at reflections of the underlying Si lattice also show distinct effects of the SiO$_2$ layer and the strain accompanying it. Research supported by the DOE on DE-FG02-07ER.

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