SYMPOSIUM E
E: Fundamentals of Novel Oxide/Semiconductor Interfaces

December 1 - 4, 2003

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*Invited paper
SESSION E1: Characterization of Novel Oxides on Silicon
Chair: Matt Copel
Monday Morning, December 1, 2003
Room 207 (Hynes)

8:30 AM E1.1
Inelastic Electron Tunneling Spectroscopy (IETS) Study of HFO2/Si and HfAlOx/Si, T.P. Ma and Wei He; Electrical Engineering, Yale University, New Haven, Connecticut.

High-K dielectrics must resolve many issues, such as thermal instability, high densities of oxide charge and traps, and interface traps, before any of them can replace SiO2 as the gate dielectric for future CMOS technology. It is very important to be able to have effective diagnostic techniques to probe the underlying mechanisms behind these challenges. A promising technique is Inelastic Electron Tunneling Spectroscopy (IETS), which probes the MOS structure by detecting the interaction between the tunneling electrons and the energy-loss modes caused by lattice vibrations (phonons), impurities, and defects in the gate dielectrics. The principle of the IETS technique is based on the fact that, as the bias voltage brings the Fermi level of the injecting electrode to reach the characteristic energy of an energy-loss mode in the tunnel barrier, an inelastic interaction of tunneling electrons with this energy-loss mode opens up an additional tunneling channel on top of the elastic tunneling current background, and the current-voltage (I-V) curve will increase its slope at that bias voltage. By taking the second derivative of the I-V curve, a peak shows up where the slope changes in the I-V curve. Thus the IETS technique basically takes the 2nd derivative of the I-V characteristic to reveal inelastic interactions between tunnel electrons and energy-loss modes in the tunnel barrier. The energy where a peak occurs corresponds to the characteristic energy of that particular mode, whether it is due to a phonon, an impurity, or a particular defect, and the area of the peak is directly related to the intensity.

In this paper, we will report some IETS spectra that contain a wealth of information on the chemical bonding and composition of ultra-thin HfO2 and aluminum doped HfO2 (HfAlOx) as high-k gate dielectrics in MOS capacitor structures. We will also show the effects of traps on the IETS spectra, and the use of IETS to study the trap-assisted current transport mechanisms, the creation of traps by electrical stress, as well as the microscopic origins of stress-induced-leakage-current (SILC).

9:00 AM E1.2
Point defects in thin HfAlOx films probed by monoelectronic postion beams. Akih Ueda1, R. Misukhishi2, A. Horii2, K. Tori2, M. Goto2, K. Yamane2, K. Yasuda2, R. Sumiki4, T. Ochiai4 and T. Mikado4
1. Institute of Applied Physics, University of Tsukuba, Ibaraki 305-8573, Japan; 2. Semiconductor Leading Edge Technologies, Inc., Tsukuba, Ibaraki 305-8550, Japan; 3. Nano Technology Research Laboratory, Waseda University, S13, Waseda Tsurumaki, Shinjuku, Tokyo, Japan; 4. National Institute of Advanced Industrial Science and Technology, Tsukuba, Ibaraki 305-8568, Japan.

Hafnia (HfO2) and its related alloys such as HfAlOx, are possible replacements for silicon dioxide as the gate dielectric materials for CMOS transistors. Since the electric properties of such "high-k" materials are very sensitive to the presence of point defects, it is crucial to have knowledge about behaviors of the defects in high-k materials. The position annihilation technique is an established means of studying point defects in materials. When a positron is implanted into solids, it annihilates with an electron, and emits γ quanta. The motion of the positron-electron pair causes a Doppler shift in the energy of the quanta. A positron may be localized in a vacancy-type defect due to Coulomb repulsion from ion cores. Since the momentum distribution of the electrons in such defects is different from that in the bulk, one can detect the defects through measurements of Doppler broadening spectra of γ quanta. The change in the spectrum is characterized by the P parameter, which mainly characterizes the fraction of the annihilation of positron-electron pairs having a low momentum distribution. The value of P differs depending on the specific type of defects. Information useful for identifying vacancy-type defects can also be obtained by measuring the lifetime spectra of positrons. The present study used monoelectronic positron beams to investigate defects in HfAlOx films. The samples were 7nm thick HfAlOx films deposited on Si substrates by atomic layer deposition technique. Trimethylaluminum and hafnium tetrachloride were used as precursors, and water vapor was used as an oxidizing agent. After the deposition, the samples were annealed at 1050°C (1 s) in O2/N2 atmosphere. For the as-deposited film, the annihilation modes of positron were measured, and the lifetime data were obtained to be 281 ps and 592 ps (95%), respectively. Since those lifetimes were longer than the typical lifetime of positrons annihilated from the free state in metal oxides, it can be concluded that two different kinds of open spaces were present in the as-deposited film. After annealing in 0.02% O2 atmosphere, the value of P for HfAlOx film decreased, and its annihilation mode became one; the positron lifetime was 412 ps. The results can be attributed to the shrinkage of open spaces due to the change in the matrix structure of HfAlOx, during annealing. We observed a clear correlation between the mean size of vacancy-type defects and the amount of oxygen in annealing atmosphere. From the detailed analysis of the P-S relationships, negatively charged defects near the HfAlOx film were also detected. The present results show that a monoelectronic positron beam can be used to study behavior of defects in thin high-k films deposited on Si substrates. In particular, the potential of positron annihilation for detecting vacancy-type defects in the high-k films makes it a powerful tool for the development of the high quality high-k materials.

9:15 AM E1.3

Electron energy-loss spectroscopy (EELS) is a powerful probe of the local chemistry, electronic structure and bonding in a range of materials via analysis of the fine structure, energy loss near-edge structure (ELNES), present on the ionisation edges. Moreover the technique can be used to analyse samples on a sub-nanometre length scale when carried out in a suitable scanning transmission electron microscope. In this paper we will summarise the results of our experimental investigations of the oxygen K-edge ELNES in HfO2, ZrO2, HfSiO4, ZrSiO4 and SiO2. This work was supplemented by a study of co-deposition methods for the formation of these standards which will allow us to investigate the influence of semi-amorphous or nanocrystalline structures on the observed ELNES. In order to fully interpret the data obtained we have utilised band structure methods to model the experimental edges. Building on the results of our fundamental study on these bulk standards, we will report the results of EELS spectrum experiments carried out on range HO2 layers grown on silicon using both MOVCVD and ALD. We will demonstrate that variations in the local electronic structure and bonding can be detected using ELNES and that these can be directly related to changes in physical and chemical changes that occur within the layers and at the interfaces during processing.

10:00 AM E1.4
Electron Spin Resonance Characterization of Defects at Interfaces in Stacks of Ultrathin High-k Dielectric Layers on Silicon. Andre Stepanov and Valery V Afanasyevic; Physics, University of Leuven, Leuven, Belgium.

The scaling of metal-oxide-semiconductor (MOS) based devices in integrated circuit technology, entering the 100nm technology node, drives materials and technological requirements to ever new extremes. A most challenging issue concerns the intended replacement of the traditional SiO2 gate dielectric by one of substantially higher dielectric constant k, which, as projected, would need to be introduced in devices by 2005. Various potential alternative dielectrics, such as the binary metal oxides Al2O3, ZrO2, HfO2, TiO2, and La2O3, have been or still are intensely studied. The exposed research efforts are impressive: multiple top analyzing techniques are combined to explore compositional and structural characterization. Incorporation of MOS structures and devices, electrical probing methods reveal the occurrence of defects and charge traps-3,4 which detrimentally affect the electrical merit of the new high-k layers. Interface traps also appear to play a prominent role.5 The current work reports on the application of the electron spin resonance technique (ESR), a key physical noscale-identification tool of point defects in solids5. It is applied here to the investigation of (100)/Si/insulator structures with ultrathin high-k layers, including stacks of nm-thin SiOx and layers of ZrO2, HfO2, TiO2, and La2O3, and by open various chemical vapor deposition methods. Results will be overviewed with particular emphasis on occurring interface defects and charge traps. Generally, after hydrogen photooxidation, prominent trinitron-Si interface defects (Pho, Phi) Si dangling bond type centers are observed at the (100)/Si/dielectric interfaces. This Pho, Phi fingerprint, generally unique for the thermal (100)/Si/SiO2 interface, indicates that the as-deposited (100)/Si/metal oxide interface is not intermixed and also that the three different preparation methods of the (100)/Si/HfO2 structure shows the Pho-type defect signature, and hence the interface, to be sensitive to the kind of deposition process. The Pho-type defects may serve as atomic probes utmost sensitive to the strain state of the interface, which will be discussed. Also is addressed the influence of post-deposition thermal treatment. This will include, among others, the effect of annealing in H2 on the interface defects [present efficiency of the multilayer structure in general. Parallel electrical analysis reveals the correlation of Pho-type defects and fast interface traps. A general
The thermal stability, and microstructure of yttrium aluminum oxide (YAO) and lanthanum aluminum oxide (LAO) mixed oxides were evaluated. The films were prepared by chemical solution deposition (CSD) using a solution prepared from yttrium, or lanthanum butoxycetyl, and aluminum butoxycetyl dichloride in butyl chloride. The films were spun to SiOxNy or SiOxNy+Hx+n substrates and furnace annealed at temperatures between 500-1200°C in oxygen for 30 minutes. The microstructure and electrical properties of YAO and LAO films were examined as a function of Y2O3/La2O3 ratio and annealing temperature. The films were characterized by X-ray diffraction, FTIR, RBS and AES. At low (<25)% Y or La concentrations at anneal temperatures less than 800°C, an amorphous γ-alumina-like material was observed in the YAO and LAO films. Crystallization of γ-alumina and α-alumina in YAO and LAO films was observed at higher Y or La concentrations and at anneal temperatures > 800°C. The YAO and LAO films were observed to react with the underlying silicon at the interface to form silicates. Lanthana in the film form more readily upon annealing than yttria silicate. Dielectric Constant was observed to be dependent on Y and La concentrations.

Influence of nitrogen bonds on electrical properties of HfAlOx films fabricated through LL-DKA process using NH3-ammonolysis. We have developed a Layer-by-Layer Deposition and Annealing (LL-DKA) process for growing HfAlOx as high-k gate dielectrics [1]. This process features that RTA treatments are inserted during ALD cycles and effective to remove residual impurities in the high-k/low-k layer interface. Also, this process can control the extent of nitrogen incorporation in the HfAlOx layer by using an optimal NH3 annealing. In this paper, we report on the nitrogen bonding features in HfAlOx films prepared by LL-DKA process using NH3 in N2 ambient, which were analyzed by XPS, N 1s XPS and TEM-EELS measurements. Poly-Si gate HfAlOx MOS capacitors and nMOSFETs were fabricated to reveal the influence of nitrogen incorporation on the electrical properties. HfAlOx films were prepared by the LL-DKA process, in which a sequence of 0.8nm-thick HfAlOx film growth by ALD and subsequent NH3 annealing was repeated. NH3 annealing was carried out at different temperatures for 550, 650, and 750°C. It was shown that the nitrogen concentration of HfAlOx films prepared by 850 and 950°C is about one order of magnitude higher than the case of 550°C samples as confirmed by XPS measurements. The XPS data indicated that the Hf-O bonds were formed in HfAlOx network when annealed at 850 and 950°C by using NH3 ambient. It is preliminary shown that excessive incorporation of nitrogen results in a significant increase in leakage current through HfAlOx films. This work was supported by NEDO [1] T. Nabatame et al., VLSI Symp. Tech. Dig., p. 25 (2003).
optical properties of oxide materials permits the direct study of the interband transitions from the valence to the conduction band states. In the past year, there has been much progress in the quantitative analysis of transmission electron energy loss spectroscopy in the electron microscope and we are extending this work for analysis of thin oxide films on semiconductors. Here we employed reflection electron energy loss spectroscopy (REELS) and ultraviolet-visible (VUV) spectroscopy to determine the optical properties and electronic structure of oxide materials, i.e. Al2O3, ZrO2 and SiO2. The surface and bulk plasmon resonances for these oxide materials have been determined from VUV and REELS, along with the influence of primary electron energy on the REELS results. Once the multiple scattering has been removed from the REELS spectra we have used Kramers-Kronig dispersion transforms to determine the complex optical properties. The relative contribution of surface and bulk plasmon oscillation in REELS has been investigated. Comparison with VUV results and existing TEELS results indicate that Kramers-Kronig analysis can also be applied to REELS spectra and the corresponding conjugate optical properties can be obtained.

Quantitative studies of the electronic structure and optical properties of thin surficial films using VUV and REELS or TEELS, represent a new means to determine the properties of these increasingly important films. This work was partially funded by NSF Award DMR-0110022 in cooperation with EU Commission Contract G3RD-CT-2001-00886.

11:45 AM E1.10 Process dependent band structure changes of transition-metal (Ti, Zr, Hf) oxides on Si (100). C. C. Fulker1, G. Lucovsky1 and R. J. Nemravich1
1Physics, North Carolina State University, Raleigh, North Carolina; 2Materials Science & Engineering, North Carolina State University, Raleigh, North Carolina.

In this study we have deposited Ti, Zr and Hf oxides on ultrathin (~0.5 nm) SiO2 buffer layers and have identified metastable states which give rise to large changes in their band alignments with respect to the Si substrate. The high-k oxides were formed by electron beam evaporation of a transition metal film at 700°C, followed by oxygen plasma oxidation. These films were then characterized by x-ray and ultraviolet photoelectron spectroscopy (XPS and UPS), which provided information about band bending, chemical bonding and valence band maxima. We observed a potential across the interfacial SiO2 layer, significant band bending and large shifts in the high-k valence band. The magnitude of the shifts differed for the three materials where ZrO2 showed the largest shift, HfO2 was intermediate, and TiO2 showed the smallest shift. We have also observed that the magnitude of the shift was inversely related to the thickness of the buffer layer. With increased buffer layer thickness the resulting electronic shift decreased. We propose a model in which excess oxygen accumulated near the high-k = SiO2 interface providing electronic states, which are available to electron states tunneling from the substrate. Research supported by SRC.

SESSION E2: High-K Oxides on Silicon
Chairs: Eugene Gusev and T.P. Ma
Monday Afternoon, December 1, 2003
Room 207 (Hynes)


Interface formation is critical to integration of alternative gate dielectrics for Si-based CMOS. This talk will describe recent advances in the understanding of high-k/silicon structures. Typically, metal oxide stacks rely on a thin SiO2 or SiONx buffer layer to passivate the Si surface. Once created, the stability of the interfacial oxide is far from certain as the interface metastable states can be found to deplete this barrier, such as silicon oxide formation, growth-induced reduction and high temperature reduction. Silicate formation is highly dependent on metal species, with Y and La oxides undergoing a facile reaction compared to Hf and Zr oxides. In the extreme case of yttrium, buffer layers can be entirely consumed by silicate formation during UHV high temperature annealing. For HfO2, we see little evidence of silicate formation, but do see interactions with SiO2.

Deposition of high-k oxides on Si by MBE conditions can cause rapid reduction of SiO2, even with a high oxygen overpressure. Detailed kinetic studies suggest that oxygen vacancies generated during growth are responsible. Understanding the stability of buffer layers is critical to successful integration of such high-k oxides. Alternatively, removing interfacial oxide may provide a route to higher capacitance structures, but this will only prove viable in the unlikely event that we can learn how to passivate and integrate these fragile structures.

2:00 PM #E2.2 Properties of Ultra-Thin Silicon Nitride Barriers. Katherine Bachleitner, Hisashi Takeuchi and Tae-Jae King; Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, Oakland, California.

Metal oxides such as HfO2 and ZrO2 are known to form interfacial layers at the Si interface, resulting in an undesirable increase of EOT (effective oxide thickness). It has been reported that Ni3S2 pre-storage is effective for the HfO2 barrier. However, detailed properties of the silicon nitride layer are not well understood. In this study, properties of 0.8 - 1.3 nm Si3N4 formed by RTN (rapid thermal nitridation) were measured. First, interface properties of the nitride layer were characterized by surface charge analysis, which can extract interface state densities, fixed charge densities, and near-interface trap densities without suffering from high leakage. It was found that high temperature annealing (900-1100°C) of the silicon nitride layer in an inert atmosphere reduces trap density at least a factor of two (~5×1011 cm−2 eV−1). In addition, only electron traps and negative fixed charges were observed for the nitride, whereas only hole traps and positive fixed charges were observed for ultrathin SiO2 films. Next, immunity to boron penetration from p-poly-Si was characterized. After a high thermal budget anneal in various ambient gases, the resulting doping profiles measured by spreading resistance and observed that a nitride interface, which is the junction depth caused by annealing to only 24% of that of a control sample with no nitride. Finally, application of the nitride layer to ultra-thin oxide layer formation was proposed. L-V characteristics of the poly-Si gated MIS capacitor showed leakage current of the same order of magnitude as that of the diodes with no nitride, indicating that boron diffusion can be suppressed without degrading forward diode current.

2:15 PM #E2.3 Material Science and Integration of A New Hybrid TiAlxN/Al Layer As An Alternative Gate Oxide For Sub-100 nm CMOS Devices. Orlando Aucilla1, Wei Fei1,2, Bernd Kubin1, John M. Hiller1, Santaj Saha1, John A. Carlisle3, Syouyuu Y. Li1, Vishnu P. Drawid1, Robert P.H. Chang2, Cirillo Lopez3, Eugene A. Irene1, Ruil A. Burghardt3 and Charles A. Dakes4; 1Materials Science, Argonne National Laboratory, Argonne, Illinois; 2Materials Science, Northwestern University, Evanston, Illinois; 3Chemistry, University of North Carolina, Chapel Hill, North Carolina; 4Materials Science, University of Virginia, Charlottesville, Virginia.

A new TiAlxN/Al (TAO) oxide layer developed in our laboratory, produced by sputter-deposition, exhibit the combination of properties required for the next generation of integrated circuit gate oxides, namely: (a) a dielectric constant k ~ 30 (higher than that of current leading, amorphous gate oxides); (b) high temperature stability when integrated with Si [a SiO2 interface layer < 1 nm thick, depending on the oxidation temperature in the room temperature range to 500 °C, is formed between TAO and Si]; (c) bandgap ~ 3.9 - 4.4 eV (may be tunable when optimized); (d) leakage current ~ 10−7 A/cm² for a TAO layer with equivalent oxide thickness (EOT) ~ 1.7 nm and ~ 4.2 A/cm² for TAO with EOT of 0.8 nm; and (e) relatively low density of electrically active defects at the oxide/Si interface (not optimized yet). Chemical analysis via x-ray photoelectron spectroscopy and near-edge x-ray absorption spectroscopy, respectively, reveals a distinct equilibrium in oxygen binding to Ti and Al atoms, as well as Ti-Al bonding, resulting in a fully oxidized amorphous TAO structure that inhibits a strong reaction of oxygen with Si that is characteristic of other gate materials currently under investigation. Cross-sectional high-resolution transmission electron microscopy and spectroscopic ellipsometry provide evidence for an atomically sharp TAO/Si interface. Oxidation in atomic oxygen at room temperature enables a TAO layer with a negligible Si oxide content. The amorphous microstructure of the TAO layer plus its chemical state results in the excellent electrical properties, revealed by C vs. V, leakage current, interface trap measurements. * This work was supported by the US Department of Energy, BES Materials Science, under Contract W-3.19-165-ENG-38; NSF/ONR under Contract N00014-98-J-1178 (UNG-CH).

3:00 PM #E2.4 Stability of Nitrogen in High-k Dielectrics. I.J. Blumsool, Universidade Federal do Rio Grande do Sul, UFRGS, Porto Alegre, RS, Brazil.

The use of metal oxide and silicate films on Si as high-k replacement for silicon oxide and covalent oxide gate dielectrics is advanced VLSI technology presents several difficulties concerning interface density of states, chemical and structural stability in further processing steps following high-k deposition, oxidation of the Si substrate, and migration of metallic species in the dielectric/metal region, as well as transport of Si into the high-k film. Recent investigations...
indicated that incorporation of nitrogen into the metal oxide and silicate films provided substantial improvements in the direction of overcoming the above-mentioned difficulties. However, nitrogen, when mainly incorporated into metastable configurations in these oxide and silicate films, the integration of nitrided high-k dielectrics into the fabrication process relies on the stability of N in these materials during further processing steps [e.g., Si, Al, and Hf atomic transport and exchange processes during thermal processing of nitrided aluminum oxide and hafnium silicate films on Si]. The profiles of the light elements were determined, before and after thermal processing. Two approaches by numerical calculation and profilometry with sub-nanometer depth resolution. Strong N removal and redistribution of the remaining N were observed following thermal processing. The major mechanism responsible for N removal being N-O exchange. N redistribution, on the other hand, seems to be the result of a complex reaction-diffusion mechanism which will be discussed. Oxygen migration and amounts of oxidation and nitridation of the Si substrate during different thermal processing routines were also assessed by profilometry.

3:30 PM E2.5
Study of HfAlOx Films Deposited by Layer-by-Layer Growth for CMOS High-K Gate Dielectrics. Akira Toriumi1,2, Yasuhiko Nabatame1, and Tsuyoshi Horkawa2.1 Materials Science, The University of Tokyo, Tokyo, Japan; 2AIST, Tsukuba, Japan; 3ASET, Tsukuba, Japan.

We have investigated ternary metal oxides for possible high-k gate dielectrics by using layer-by-layer deposition & annealing method so as to keep the dielectric constant of the film high with no crystalline. In fact we have prepared HfAlOx films by alternating deposition of HfO2 and Al2O3 atomic layers. It is a key for controlling the film quality to understand the intermixing process between two layers by the XPS analysis. And then, we focused on the diffusion and structural change of the HfO2/Al2O3 superlattice film as a function of annealing temperature by changing the Hf/Al composition ratio. In case of the film with HfO2/Al2O3=13/83% cycle, the superlattice perfection was observed below 750°C (HfO2 layered stack). Above 750°C, the Al2O3 layer was damaged, and then the orthorhombic or tetragonal structure was detected. These results indicate that the intermixing in HfO2/Al2O3 films occurs between 750°C and 850°C. The intermixing onset temperature was increased with increasing Al content in HfAlOx ratio. Next, the MOS characteristics with HfAlOx films prepared by this method are discussed in terms of the quality improvement and the profile design inside the dielectric film. Finally, prospects of these oxides for CMOS high-k gate dielectrics are also addressed.

4:00 PM E2.6
Measurement of the Band Offset Between Amorphous Lanthanum Aluminate and Silicon. Lisa Friedman Edge1, D G Schrom2, S A Chambers2, C Hinkle3, G Taucovska3, Y Yang4, S Steurer5, and M Copel6.1 Materials Science and Engineering, Pennsylvania State University, University Park, Pennsylvania; 2Fundamental Science Division, Pacific Northwest National Laboratory, Richland, Washington, USA; 3Department of Physics, North Carolina State University, Raleigh, North Carolina; 4Materials Department, University of California, Santa Barbara, California; 5IBM T.J. Watson Research Center, Yorktown Heights, New York.

LaAlO3 is a promising alternative gate dielectric for the replacement of SiO2 in silicon MOSFETs. Single crystalline LaAlO3 is known to have a dielectric constant of 9 and an optical bandgap of 5.6 eV. It has also been shown that single crystalline LaAlO3 is stable in contact with silicon under standard MOSFET processing conditions (1026 °C for 20s). An important additional characteristic for alternative gate dielectric applications is knowledge of the band offsets between LaAlO3 and Si. These have been predicted to be in the range 1.0 to 2.1 eV for electrons and 1.9 to 3.5 eV for holes.1, 2 By investigating the oxidation kinetics of Al and La, both individually and together (codeposition), to determine the minimum oxygen partial pressure required to achieve fully oxidized lanthanum aluminate, we have found a regime in which we can deposit amorphous lanthanum aluminate on Si without any interfacial SiO2. These films are made by molecular beam deposition (MBD) in a low temperature / excess oxidant regime. XPS analysis of the amorphous lanthanum aluminate films as thin as 10 Å are fully oxidized and show no SiO2 at the interface, even after prolonged exposure of the films to air. Using XPS we have measured the band offsets for these abrupt amorphous lanthanum aluminate films with Si. The measured band offsets are 1.35 ± 0.03 eV for electrons and 3.15 ± 0.1 eV for holes. The band offsets are independent of doping concentration in the Si substrate material, as the thickness of the amorphous lanthanum aluminate film.1, 3 J. Robertson, MRS Bull. 27, 317 (2002). 2 P. W. Peacock and J. Robertson, J. Appl. Phys. 92, 4712 (2002).

4:15 PM E2.7
Maximization of the Crystallization Temperature and


Currently in the search for an alternative high-k dielectric material to replace silicon dioxide, hafnia oxide has shown promise due to its thermodynamic stability on silicon and higher dielectric constant. However, hafnia crystallizes at relatively low processing temperatures which results in leakage path formation at the grain boundaries. To improve the crystallization of hafnia with alumina and gadolinia using a multi-target pulsed laser deposition technique. In this study, thin films of various compositions in the ternary were deposited, including the pure endpoint components, to compare band gaps, dielectric constant changes, and the effect on the crystallization temperature. Film stoichiometry and quality was assessed using x-ray photoelectron spectroscopy and Fourier transform infrared spectroscopy. Crystallization temperatures were determined by x-ray diffraction with high temperature capabilities up to 900°C. Electrical properties of the films were compared using capacitance-voltage and current-voltage measurements with platinum electrodes. From these results, the optimal composition which maximized the dielectric constant and the crystallization in this ternary system was determined.

4:30 PM E2.8
Physico-chemical and electrical characterisation of HfO2 layers deposited on strained SiGe by Atomic Layer Deposition. Jean-François Demelencour1, Olivier Weber2,3, Jens-Michel Hartmann1, Frederique Ducrocq1,4, and Marie-Noelle Sebban5.1 CEA-LETI, LEPH, CEIRG, Grenoble cedex 9, France; 2LPM, INSA-Lyon, Villeurbanne.

Recent results have shown that High-K materials, such as HfO2, are very promising materials for the replacement of silicon dioxide as the dielectric stack of MOS transistors, in order to achieve a lower leakage current for the same Equivalent Oxide Thickness (EOT). However, the use of HfO2 on Si led to a strong mobility degradation. Enhanced hole mobility in Si0.75Ge0.25, under compressive strain has been reported and could be an alternative to the mobility degradation. This paper focuses on the growth of HfO2 by Atomic Layer Deposition (ALD) at 350°C on pseudomorphic Si0.75Ge0.25 thin film (x=0.5 and 0.25). Three different Si0.75Ge0.25 preparing process (Chemical oxidation, HF dip of HfO2 film and HfO2 + in situ hot water pulses) have been investigated to obtain the best HfO2 film quality with the thinnest interfacial layer. The startup of the ALD growth on these different surfaces has been analysed by Total X-Ray Fluorescence. No nucleation retardation has been observed even for HF dip SiGe treated surfaces. We assume that this is due to the greater Ge oxidation potential. We have also seen, by X-ray Photoelectron Spectroscopy, that HF-dipped SiGe surfaces were very convenient to obtain high quality HfO2 films. The structure of the interfacial layer has been precisely analysed: it is made of a Ge/Si mixed oxide layer. The evolution of this interfacial layer has been studied as a function of subsequent annealing treatments. This HfO2 layer was 3.5, 5, 5 and 8 nm thick deposited on strained layers were analysed by mercury probe. An EOT as low as 0.7 nm was obtained for a 2.5 nm-deposited HfO2 film. Results on the physico-chemical and electrical characterisation of HfO2 layers deposited by ALD at 350°C directly on pure Ge layers will be also presented.

4:45 PM E2.9
Chemical and Electrical Characteristics of HfSiOxNy HfAlOx Gate Dielectric MOSFETs. Cheong-Hee Lee, Sundar Gopalak, Jeff Peterson, Jim Gut, Hong-Jhy Li, Fiz Lyanght and Mark Gardner, Advanced Gate Stack Project, SEMATECH, Austin, Texas.

Various high dielectric constant materials such as Ta2O5 [1-2], Al2O3 [3-4], TiO2 [5], and SiO2 [6] have been researched for gate dielectric application. Ta2O5 was shown to have interfacial reactions with Si substrate [7]; while TiO2 and SiO2 were not thermally stable in direct contact with the silicon substrate. Al2O3 is compatible with the silicon substrate, but the overall dielectric constant is less than 10; therefore, achieving an equivalent thickness of EOT of less than 10Å may not be feasible using Al2O3. Recently, HfO2 and HfSiOxNy have received industry attention due to their thermal stability on Si and moderately high dielectric constant [12 ~ 50]. Ako, they believe to have a wide band gap of ~5.5 eV with electron and hole barrier heights of 4.9 and 3.7 eV, respectively. The low crystallization temperature of HfO2 (~500°C) creates a problem for conventional planar CMOS integration. There have been many attempts to improve the crystallization temperature of EOT of less than 10Å by adding nitrogen, Si and aluminum [8-9], including a Hf0.3Al0.7O2, HfAlOx and HfSilOxNy gate dielectric MOSFET with poly silicon gate, in which the laminated layers are intermixed after the source/drain activation anneal [10]. Scaling below 14 Å TiO2 EOT will be 9 Å, 15 Å HfO2 poly Si gate is extremely difficult, as leakage becomes considerably high. By

SESSION E3: Poster Session: Fundamentals of Novel Oxide/Semiconductor Interfaces
Chair: George Abdnoury and Efrem Gusev
Monday, December 1, 2003
8:00 PM
Exhibition Hall D (Hynes)

E3.1 Scanning Tunneling Spectroscopy Characterization of Oxide/Silicon Interfaces. Louis Nemzy and Fredy R. Ypmaan; Physics, Yeshiva University, New York, New York.

We will present results on the effects of imperfections on performance of quantum multi-layered materials. More concretely, we have quantified the dependence of current-voltage (I-V) curves on interface roughness. The I-V curves, for a new type of quantum structure has been designed based on silicon and oxygen. These semiconductor-atom structures (SAS) are built by alternating layers of silicon and films of oxygen, thus creating structures similar to the traditional superlattices. These SAS have good optical electronic and photo-luminescence and may therefore form the basis of future all-Si integrated circuits with both electrons and photons. Due to their novelty, the I-V curves are only qualitatively satisfying. TEM images show that SAS have stacking faults and dislocations in substantial quantities as to affect response time and transmission. Substantial experimental work has been done to understand why is SAS, silicon may grow epitaxially after the oxygen barrier. This is not the case in Si/SiO2 interface where oxygen is the surface layer of the CoOx barrier. A large number of defects is generated in bulk silicon. However, by controlling the oxygen rate supply, it is possible to produce silicon on both sides of the oxygen interface which is shown below. Although the interface disorder and strain on SAS current-voltage curves. Their quality factor is extremely sensitive to the presence of imperfections. We will present results for structures made of alternating layers of materials. The I-V curves will be calculated within Tight Binding (TB) Theory. As a spin-off of the TB calculations, we have extracted a value of an effective silicon-oxide barrier height.

E3.2 Oxide-Semiconductor Interface Characterization Using Kelvin Probe-AFM In Combination With Corona-Charge Deposition. Bert Lager, Max Daniely Aynal, Elena Oksorin, Andrew M Hoff and Rodney Schild; Electrical Engineering, University of South Florida, Tampa, Florida.

Corona charge deposition methods in combination with spatially resolved surface potential measurements have become an essential tool for Si oxide quality control. The combination of these techniques provides a means of oxide semiconductor interface parameters such as surface barrier height, oxide thickness and oxide charge density can now be monitored in situ. This combination also allows the control of commercial devices. The ongoing downsizing of integrated circuits is driven by sub-100 nm regime making the development of high resolution oxide screening methods increasingly important. However, currently available commercial devices are limited in their spatial resolution since they employ the traditional vibrating Kelvin probe technique, restricting their lateral resolution to several µm [2]. In order to increase the lateral resolution of this measurement method we have combined the Kelvin probe technique with Kelvin Probe AFM. We present initial results of this novel measurement technique and demonstrate its feasibility by measurements on lithographically prepared oxide patterns on Si wafers with different oxide thicknesses. [1] D. K. Schroder, M. Sci. Technol 12/3, R16 (2001). [2] L. Kranz, Y. Shapira, Surface Science Reports 37, 1 (1999).

E3.3 Field-induced Reactions of Water Molecules at Si-dielectric Interfaces. Leonidas Ntziachristos*, Xing Zhou*, Ronald D Schrimpf*, Daniel M Fleetwood* and Solicrtes T Panteleakis**; *Physics and Astronomy, Vanderbilt University, Nashville, Tennessee; **Electrical and Computer Engineering, Vanderbilt University, Nashville, Tennessee; Water molecules are to a varying degree present in SiO2 and other dielectrics and at Si-dielectric interfaces. Their presence, even in small concentrations, constitutes a critical reliability problem for present day ultrananoelectronic devices. Here we present first-principles density functional calculations that probe the reactivity of water molecules at the Si-dielectric interface. Even though these molecules are generally non-reactive at room temperature, they become active in the presence of strong electric fields that produce a hole inversion layer, as in a p-channel MOSFET. We report results on different possible reaction pathways for water at the interface, including dissociation of water that can lead to the release of H⁺ ions. The released protons can move away and deplete conduction bands. Results are also presented for the reaction of water with a number of defects, including a passivated bond, a substitutional bond, and a hydrogen migrating laterally along the interface. We thus obtain the atom-scale mechanisms for the creation of interface traps and oxide trapped charge, the two features that give rise to negative bias temperature instability (NBTI), a well-known reliability phenomenon that occurs in MOSFETs under normal operating and stress conditions.

E3.4 Kinetics of thermal oxidation at the Si(001)-SiO2 interface: Revisited from high-temperature data. Hira Omi, Masato Umemoto, Hiroki Kagehashi and Toshihiro Ogino; Device Physics, NTT Basic Research Laboratories, Atsugi, Kanagawa, Japan.

An understanding of thermal silicon oxidation is essential for further developments of semiconductor science and technology. It is particularly important to reveal the mechanism of morphological evolution between the growing thermal silicon oxide layers and Si(001) substrate during oxidation to obtain an abrupt interface on an atomic scale. Despite all of the work that has been done on the Silicon/SiO2 interface formation, however, there is little quantitative understanding of the oxidation kinetics at the interface. In this presentation, we will show the first quantitative scanning tunnelling microscopy analyses of the interface kinetics of thermal silicon oxidation at 1100 - 1300 degrees C. We systematically studied the morphological evolution of the Si(001)-SiO2 interface during oxidation in Ar atmosphere containing a small fraction of O2 using atomic force microscopy (AFM) and reflection high energy electron diffraction (RHEED) technique. O2 fraction, and substrate miscut angle. The interface morphology was observed by AFM after removal of the thermal silicon oxides in dilute HF solution. Scanning analyses on the interface evolution show that the interface width W(110) during oxidation scales as L1.0 and l0.25 at 0.2% O2 atmosphere, and L0 and l0 at 2% O2 atmosphere at 1200 degrees C, where L is length and t is oxidation time. The scaling laws we obtained tell us that the Si diffuses inside the growing silicon oxide during the oxidation. The diffusion coefficient derived from the emergence of step-terrace morphology at the interface is close to that of the Si self-diffusion in silicon oxide film. The above results are consistent with a model that involves diffusion of Si species emitted from the substrate and reacting with oxygen in the oxide film.

We believe that these findings will help us to understand the kinetics of thermal oxidation at the Si(001)-SiO2 interface below 1100 degrees C.

E3.5 The Oxidation of Si-Ge Alloys and Analysis of Sub-Bonded Si Implication for Thin Film Oxidation of Si. Ralph Jacobson* and Steve J. Kilpatrick**; *Lehigh Univ., Bethlehem, Pennsylvania; **U.S. Army Research Laboratory, Adelphi, Maryland.

An experimental study of the oxidation of Si-Ge alloys grown on Si was undertaken to explore conditions under which oxides of mixed composition, i.e. SiO2-GeO2, were obtained. By combining the oxidation studies with coexposure to different partial pressures of oxygen, we obtained the oxidation rate law for SiGe, which is very useful for the design of new oxide materials. We also studied the oxidation of SiGe films in situ in a Scientia ESCA-3000 system with partial pressure of oxygen varied by using a high precision mass flow controller. The oxidation rate law was determined to be 1.8% to 16% Ge Dry oxidations were carried out in situ in a Scienta ESCA-3000 system with partial pressure of oxygen varied by using a high precision mass flow controller. The oxidation rate law was determined to be 1.8% to 16% Ge to obtain the rate law for SiGe. We also studied the oxidation of SiGe films in situ in a Scientia ESCA-3000 system with partial pressure of oxygen varied by using a high precision mass flow controller. The oxidation rate law was determined to be 1.8% to 16% Ge. Dry oxidations were carried out in situ in a Scientia ESCA-3000 system with partial pressure of oxygen varied by using a high precision mass flow controller. The oxidation rate law was determined to be 1.8% to 16% Ge.
monolayer absorption to actual oxide formation. Films grown up to 10 nm were analyzed by angle resolved x-ray spectroscopy. These studies were used to investigate the influence of oxide thickness on the electronic properties of Si. Mined oxides were found to be poorer than the pure SiO2 grown on the same alloy. This implication of the work on early oxidation of Si will be suggested!!

E3.6 Nanoscale analysis of local leakage currents in stressed gate SiO2 films by conducting atomic force microscopy.

Hiroki Konishi1,2, Shigeaki Yuki1,2,3
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3 Toyota Central R&D Labs., Inc., Nagakute, Aichi, Japan.

Reliability of thin gate dielectrics is one of serious problems in recent ULSI technologies. It is well-known that stress induced leakage current (SILC) occurs at an early stage of the dielectric fatigue caused by applying the high electric field. Although SILC and subsequent dielectric breakdown are considered to take place locally in the film, degradation mechanisms at each local site have not been well understood and only macroscopic measurements have been done so far. In this work, we have developed a nanometer scale observation method for local leakage currents induced in stressed gate SiO2 films in metal-oxide-semiconductor [MOS] capacitors. Detecting local leakage sites with a nanometer scale area in current images by conducting atomic force microscopy (C-AFM), we studied leakage current properties at respective defect sites and their distributions in gate SiO2 films. For this purpose, with a structure of a Cu-polysilicon gate electrode/gate SiO2/p-Si substrate, we used. Gate SiO2 films with a thickness of 11.3 nm were thermally grown at 800°C in pyrogenic oxidation ambient. As a result of Fowler-Nordheim (FN) constant current stress with a current density of 100 mA/cm² and a stress time of 100 sec (gate bias was negative), SILC was observed in the current-voltage [LV] characteristics of MOS capacitors. After the poly-Si gates were removed and the SiO2 films were thinned chemically to be 5.2 nm thick, current images were observed with a negative substrate bias for both stressed and non-stressed gate SiO2 films by C-AFM. Only for stressed SiO2 films, nanometer scale leakage sites were clearly observed. No concavity was confirmed at corresponding positions in a concurrently-observed morphological image and thus the observed leakage sites were not originated from the thickness fluctuation of SiO2 but reflected locally-generated defects in the film of the applied stress. As the stress FN observations were repeated at the same area with the same bias condition, average currents of the local leakage sites decreased gradually and, finally, the sites were no longer observed. Converting the number of sites into a current flow time [τ], the leakage current is found to decrease inversely proportional to τ. After the leakage sites disappeared, the C-AFM tip was scanned with a positive substrate bias at the same area. Interestingly, the disappeared leakage sites were detected again at the same position. From a similarity to the macroscopically-measured leakage current property, the observed leakage sites are associated with a leakage current known as a transient-SILC. We deduce that appearance and disappearance of the leakage is depending on the tip-substrate bias condition is attributed to the hole injection and emission which occur from stressed induced defects in the gate SiO2 film.

E3.7 First-principles investigation for Reacation of Oxygen at Ulathin SiOx/XI/Interface. Tenori Aikawa1,2 and Hiroyuki Kageshima1.

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Silicon thermal oxidation is of great interest and importance as a key process in the fabrication of Si-based devices. Even if conventional gate oxides in MOS technology are formed by direct thermal oxidation, these are replaced by oxynitride or high permittivity dielectrics, thin oxides might still play a role as a buffer layer in order to reduce defect levels at the interface. In dry oxidation, it is widely believed that silicon oxidation consists in two different processes, the oxide growth and its reaction process at the interface. Therefore, a number of experimental studies have been intensively carried out for both the diffusion and the interfacial reaction processes, but theoretical investigations have been mainly focused on the interfacial process. The non-oxide mechanisms such as the reaction pathway and its energy barrier for oxygen insertion at the interface are still unclear. In this work, we perform a first-principles electronic structure calculation to clarify the reaction mechanism of oxygen atoms and molecules at the SiOx/Si(100) interface. It is found that in the oxide region of the interface oxygen molecules are more stable than O atoms with the energy gain of 1.0 eV. Moreover, the energy barriers for incorporation of oxygen molecules into the Si substrate are lower than those of O atoms. From these results, it is shown that oxygen molecules diffusing in the oxide directly react with the substrate, indicating that oxygen molecule reactions are the dominant reason at the oxide interface.

E3.8 Atomic mechanism of B diffusion in gate SiOx.

Mitsuru Otsuji, Kenji Shirasaki and Atsushi Oshiyama, Institute of Physics, University of Tsukuba, Tsukuba, Japan.

Due to the recent nano-scale miniaturization of silicon devices, penetration of B dopants through ultra-thin gate oxide (SiO2) has become serious. Experimentally the diffusion of B atoms in SiO2 has been extensively studied [1], and several empirical recipes for suppression of B penetration have been proposed. However, the atomic mechanism of B diffusion is still unclear, although Fair proposed a diffusion model in which the B atom diffuses in SiO2 via peroxo linkage defect (PLD), Si-O-Si≡O [2]. Very recently, we have performed first-principles calculations and investigated the diffusion mechanism of a B impurity in perfect SiO2 [3]. We found that the B atom takes a variety of stable and metastable geometries depending on its charge state and that it can diffuse by forming and breaking a bond configuration in SiO2 networks [3]. It is well known that the gate oxide contains interstitial defects such as O interstitial and O interstitial, since it is formed by thermal oxidation. In this study, to clarify the role of defects for the B impurity and its diffusion, we have performed first principle total-energy calculations of the B atom complicated with two types of defects in SiO2. In one case, the B atom is bound with PLD (an O interstitial), and in another bound that binds with an O vacancy. We have found that the B atom bound with the O vacancy is rather unstable than that in the perfect crystal or the B atom bound with PLD. Our result also shows that the B atom forms a bond with an interstitial O atom (B-O complex), becoming three-fold coordinated with surrounding O atoms. Contrary to the Fair's model, we have found that B-O complex diffuses along the bond networks of SiO2 and calculated activation energies are close to those for the B atom diffusion in perfect SiO2. [1] T. Aoyama, T. Hashio, and K. Suzuki, (1999) J. Electrochem. Soc. 146, 1879 and references therein. [2] R.B. Fair, IEEE Electron Device Letters, 17, 242 (1996) [3] M. Otsuji, K. Shirasaki, and A. Oshiyama, (2003) Phys. Rev. Lett. 90, 075901.

E3.9 Ultrathin Shallow Incorporation of Nitrogen into Gate Dielectrics by Pulse Time Modulated Plasma.

Seichi Fukuda1,2, Yoshimune Suzuki3, Tomoyuki Hirano1, Takayoshi Kato1, Akihide Kashigawagi1, Mano Saikoku1, Shingo Kodomura1, Yoichi Minamata1 and Seiji Shimomura4.

1 Micro System Engineering Center, Tsukuba University, Ibaraki, Japan; 2 Tsukuba University, Ibaraki, Japan; 3 Tohoku University, Sendai-shi, Miyagi, Japan.

Pulse time modulated plasma was studied for formation of ultrathin silicon oxynitride for gate application. Pulse time modulated plasma which has been studied to provide a new plasma etching technology with low radiation damage has potential to serve a new technology to incorporate nitrogen atoms into gate dielectrics such as silicon dioxide (SiO2) and high-k materials. In order to obtain a controllability in the nitrogen depth profile in the gate oxynitride gate dielectrics which has been known to have a strong effect on MOS reliability, micro second order pulse plasma was used to control the coupling plasma source in our pulse time modulated plasma. The radio frequency (RF) of source plasma and pulse frequency were 12.56 MHz and 10 kHz (100 micro second), respectively. Pulse duty ratio was varied from 20 to 100%. 1.2hm thick thermal silicon dioxide films were subjected to the pulse time modulated plasma and analyzed by SIMS to see the depth profile of nitrogen. A new finding is that both the concentration and the peak position of nitrogen atoms in silicon dioxide films depend on the pulse duty ratio and plasma radiation time. In other words, we found, for the first time, that the nitrogen profile can be finely controlled by our pulse time modulated plasma. For evaluation of nitrogen penetration depth of 0.5 nm deep from the oxide surface can be obtained at any desirable peak concentrations with a high controllability by tuning the pulse duty ratio and RF power. This new technology is promising to form reliable gate dielectrics for 65nm node and beyond where suppression of boron penetration and gate leakage current are the stringent requirements. In this paper, we will also describe extendibility of the new technology to application to...
Hf silicate.

E3.10 First-principles study of behaviour of excess Si atoms around ultra-thin SiOx/Si interfaces, Hiroaki Kageyama1, Toru Akiyama2, Kazuto Akagi3, Masaumi Umemoto1, Kenji Shirakawa1 and Shinji Tsuneyuki1; 1NTT Basic Research Labs, NTT Corp., Atsugi, Kanagawa, Japan; 2Dept. of Physics, Univer. of Tokyo, Bunkyo, Tokyo, Japan; 3Dept. of Physics, Univer. of Tsukuba, Tsukuba, Ibaraki, Japan.

The atomic-scale behaviour of excess Si atoms in the bulk Si crystal, namely Si self-interstitials, has been investigated experimentally and theoretically from both scientific and engineering viewpoints and much information has been obtained. However, actual Si crystals have surfaces and interfaces. Since excess Si atoms flow in and out of the interfaces and across the surfaces, an understanding of their behaviour around these surfaces and interfaces is important. Especially, the recent quantum technology is used to fine control the quality of gate oxide layer and the oxide/substrate interface as well, that is the dopant distribution in the shallow junctions neighbouring to the gate oxide. In this contribution, we investigated the stability of excess Si atoms at the SiOx/Si interface using the first-principles calculation and a Si(100) substrate surface covered with a 2-molecule-layer SiOx. The results show that the excess Si atoms are more stable both in the oxide layer and at the substrate side of the interface than in the deep substrate. The excess Si atoms appear as the self-interstitials at the substrate side, but they can transform into much stable O-vacancies in the oxide layer. Such a stability indicates high solubility of excess Si atoms at the substrate side and in the oxide layer and suggests that they segregate near the interface and flow into the oxide across the interfaces during thermal treatment. It is natural to consider that such excess Si flow into the oxide occurs across both the non-oxidizing and the oxidizing SiOx/Si interface indiscriminately. Since O-vacancies can introduce unknown defects in bulk SiOx and are often regarded as the source of charge traps, this suggests that the excess Si atom flow into the oxide layer causes degradation of gate oxide quality in case of the non-oxidizing interfaces. On the other hand, the O-vacancies appear to disappear by recharging with the incoming oxygen in case of the oxidizing interfaces. Alternately, the flow into the oxide is thought not to be negligible and to modulate the growth rate of the oxide layer thickness by the excess Si atoms are known to emit from the interfaces during the thermal oxidation.

E3.11 Degradation of Ultrathin SiO2 Films by Dynamic Stress — A Local Study by Scanning Probe Microscopy/Spectroscopy, Kim Xie, Jinbin Xu, Jin Chen and Jin An; Electronic Engineering, The Chinese University of Hong Kong, Hong Kong, Hong Kong.

The reliability of the insulting characteristic of gate oxide is a continuing concern in the development of semiconductor devices. Though much endeavor has been dedicated to address the mechanism of SiO2 film degradation and degradation resisting mechanisms are available yet. Since most devices in integrated circuits (ICs) are usually biased under variable timing conditions, the local study of ultrathin SiO2 degradation by dynamic stress may give a more realistic scenario. Before the degradation work, we applied a continuous pulse voltage at the sample (ultrathin SiO2 film) to induce dynamic electrical stress. The pulse frequency is selected to be out of the response frequency of the scanning tunneling microscopy (STM) feedback loop. The ultrathin SiO2 films were prepared by in-situ thermal oxidation of silicon in ultrahigh vacuum and ozone thermal oxidation in ambient. The local I-V characteristics of the SiO2 before and after the stress process were measured and compared. It shows that under the dynamic stress, the oxide degradation has a relaxation effect that could be explained by the hydrogen-relief degradation model. Moreover, we have also studied the frequency dependence of the degradation in the case of the atomic force microscopy (AFM). The result showed that the wear-out process had greatly prolonged after high frequency pulse stress.

E3.12 Conductance Transient Comparative Analysis of ECR-PECVD Deposited SiNx, SiO2/SiN, and SiO2Ny Dielectric Films On Silicon Substrates, Heleen Castelein1, Salvador Dueñas2, Juan Barbolín3, Álvaro del Prado2, Enrique Sim Andrews4, Ignacio Murillo2 and German González-Díez3; 1Electromagnetic Laboratory, Universidad de Valladolid, Valladolid, Valladolid, Spain; 2Física Aplicada I, Universidad Complutense de Madrid, Madrid, Valladolid, Spain.

We present a study of MIS structures based on SiN, SiO2/SiN, and SiO2Ny films deposited on silicon by electron cyclotron resonance plasmon-enhanced chemical vapour deposition (ECR-PECVD). PECVD techniques use plasma to generate active precursors for low temperature deposition. ECR technique allows a very efficient activation of the precursors, reducing the ion bombardment damage. For SiN/Si and Al/SiN/Si films, we deposited a 10 nm-thick SiO2 layer of silicon dioxide over a half of the samples by using an Astex ECR plasma source on n-type Si substrates. After that, all the samples underwent an ECR-PVD SiNx/Si deposition. Gases employed were N2 and SiH4. In this way, we obtained two kinds of samples: one with a silicon oxide film and another without it. As for Al/SiO2Ny/Si MIS structures, precursor gases were N2, O2 and SiH4. We made a CV and DLTS characterisation of all devices. Room and low temperature CV/curve hysteresis phenomena for the samples, thus indicating that interface state distribution fits to the Discarded-induced gap state (DIGS) model. When defects are not only located at the interface but they are spatially distributed into the insulator, we called DIGS or slow traps, and conductance transients are detected when driving MIS structures from deep to weak inversion. We observe that interface trap density is higher for silicon nitride and oxide films for the same oxide content. Surprisingly, the interface characterisation of Al/SiO2Ny/SiO2/Si samples seems to be poorer than for Al/SiN/Si devices. Conductance transients contribute to clarify this: Al/SiN/Si devices exhibit the highest DIGS density, whereas the lowest one corresponds to Al/SiO2Ny/SiO2/Si. Silicon oxynitride MIS capacitors show an intermediate behaviour. We detect that for Al/SiO2Ny/SiO2/Si samples there are DIGS defects up to depths of only 20 Å into the insulator bulk beyond which DIGS density is equal to silicon conduction band edge, around 2×1012 cm⁻² electrons⁻¹. However, for Al/SiN/Si devices the maximum DIGS density, located at the same energy, is about one order of magnitude higher (1×1014 cm⁻² electrons⁻¹). Moreover, DIGS are reach depths of 35 Å into the dielectric bulk. An overall comparison of DLTS and GDS measurements allows us to conclude that defects in samples with a SiO2 layer are preferentially located at the interface SiO2/Si, whereas in those with silicon nitride and silicon oxynitride films there are DIGS states spatially located further from the interface. Moreover, although Al/SiO2Ny/Si MIS show higher interface state density than Al/SiN/Si devices, they exhibit lower DIGS density values. Therefore, better understanding of the mechanisms applied to Al/SiO2Ny/SiO2/Si samples reduce the DIGS density to values even lower than those corresponding to Al/SiN/SiO2/Si devices.

E3.13 Ultrathin oxynitride films formed by using pulse-time-modulated nitrogen beams, Soji Suzuki1, Yoschii Mineyama2 and Seishi Fukuda3; 1Institute of Fluid Science, Tohoku University, Sendai, Japan; 2Sony Corporation, Kinugawa, Japan.

Ultra-thin SiO_N_x (SiO_2Ny) films have been identified as leading candidates to replace conventional SiO2 gate dielectrics for present and future ultra-large-scale integrated circuits. Remote plasma processes for top surface irradiation of thermally grown oxides have been developed and applied in complementary MOS device applications. However, it is much difficult to control the concentration and position of nitrogen in ultrathin SiO_N_x oxynitride by using plasma processing and this is highly problematic as plasma radiation damage and increases in interface state density due to N penetrating the SiO2Ny interface. We investigated how the N concentration profile in a thin SiO2Ny film could be precisely controlled using a pulsed N2 neutral beam. To inject N into thin SiO2Ny films, a neutral energy beam of more than a few eV is indispensable. Under the pulsed N2 beam, N2 was only injected into the SiO2 film during the pulsed plasma-on time. The N peak position strongly depended on the pulse-on time and the IPC source power, and the N peak concentration was determined by total beam flux. As a result, the N peak position and N peak concentration were independently controlled by using a pulse-time-modulated N2 neutral beam of a few tens of ps. The substrate temperature was also important in determining the N concentration profile in the SiO2Ny film by combining the N2 neutral beam and a high substrate temperature of 300 degrees, the N concentration profile in a 3-mm SiO2Ny film could be precisely controlled. A neutral beam irradiation system can also drastically minimize the radiation damage caused by ions and ultraviolet photons when nitriding the top surface of thermally grown oxides.

E3.14 Thermally Grown and Reoxidized Nitrides as Alternative Gate Dielectrics, Alexandra Kakhkhar Loudad2, Heike Dietl2, Harald Oser2, Christopher Schick2, Dominik Menzel2, and Ingmar Eisele1; 1Institute of Physics EIT 9, University of the Bundeswehr Munich, Neubiberg, Germany; 2Matraca Thermal Products GmbH, Dormstadt, Germany.

The use of high-k materials as gate dielectric still meets a lot of unsolved problems such as thermal instability during post deposition anneals resulting in the formation of interfacial oxide layers or bad process compatibility. As long as these requirements are not
accomplished alternative gate dielectrics have to be formed by oxynitrides or gate stacks built of oxynitrides and some high-k materials. In the case of a low energy ion beam (EOT) it is necessary to grow homogeneously thin oxynitrides which are nitrogen-rich and which have a high interface quality. Therefore we have studied the growth of thin nitrides and oxynitrides (EOT = 1.2-3 nm) formed by rapid thermal nitridation in NH3 and wet reoxidation. By varying the partial pressure of NH3 in the process gas ambient NH3/Ar the nitride quality could be optimized: it was found that an optimized ratio of NH3 and Ar during nitridation improves the electronic properties of the nitrides and oxynitrides significantly. Interface state densities as low as those of dry thermal oxides and leakage current densities reduced by four orders of magnitude compared to SiO2 of the same thickness have been obtained. Due to the high incorporation of nitrogen into the oxynitride by rapid thermal nitridation and following reoxidation the leakage current densities are also lower than those of most oxynitrides reported in literature. In addition we present data concerning the suppression of hysteresis by applying a gas mixture of NH3 and SiH4 during oxidation. In general the oxynitride developed oxynitrides are suitable to bridge the gap between common SiO2 and new alternative gate dielectrics or to form gate stacks in combination with high-k materials.

E3.15 Low-temperature growth of HfO2 dielectric layers by plasma assisted MOCVD. Giovanni Bruco1, Marianna Luchetti1, Pietro Capezzuto1, Mario Lascialfari2, Fabio Barreca3, and Ermengildo Tendella3.

Alternative gate oxides are required to minimize leakage current while maintaining high capacitance for scaling down of MOS and sub-100 nm MOSFETs. HfO2 is considered as one of the most reliable materials to satisfy such requirements because of its high oxide constant (~25), large band gap (~6 eV), and good interface stability with Si. In this contribution, we present data on the characterization and growth of HfO2 dielectric layer on p-type Si(100) by r.f. (15.56 MHz) plasma assisted metallicorganic chemical vapor deposition conditions are used: typically a pressure of 0.3 Torr, a r.f. power of 5-20 W, and a mixture of ~2:1 U:Ar gas flow rate in the range 1:50 sccm with a hydrogen-t-atmosphere. A few minutes of SiO2 growth allows full coverage of the HfO2 plasma is that it allows growth of HfO2 even at room temperature avoiding oxygen deficiencies into the layer. In the present study, the deposition temperature is investigated in the range 250-700°C. We found that by lowering the deposition temperature the sub-micron oxidation of the Si substrate is minimized. In particular, the effect of surface temperature and plasma power on the thickness of the interfacial SiO2 layer and on the microstructure of the HfO2 layer going from amorphous to microcrystalline film is investigated. Structural and optical properties of the HfO2 layers are investigated by spectroscopic ellipsometry (SE) in the photon energy range 0.75-6.6 eV. Particular attention is given to the interface between the Si substrate and the HfO2 film using SE. It is a reliable, non-destructive technique for the investigation of the interface layers. SE data are corroborated by XPS, XRD, AFM and C-V characterization. XPS and SE spectra clearly show that fully oxidized HfO2 layers are obtained at RF because of low oxygen density of O-atoms from the plasma that reduces oxygen deficiency within the layer which contributes to the dielectric leakage. The optical functions of the HfO2 layer are characterized as a function of film thickness and microstructure. The thickness at maximum refractive index is determined. By control of the plasma phase, i.e., oxygen atoms density, hafnium precursor fragmentation is carried out by optical emission spectroscopy and mass spectrometry allowing correlation between the precursors densities and films properties. Another key point of the present study in the discussion of spectroscopic ellipsometry data used to study in real time structural and optical modifications of the HfO2/Si interface reactivity upon deposition of the HfO2 film. Investigation of the Si density as a function of the thickness yielded an increase of the density of structural defects, yielding an increase stability and resistance to oxidation of Si.


As the lateral size of Si devices decreases, the thickness of individual film layers must also decrease. The interfacial roughness of such films should correspondingly affect device performance. Although many techniques (e.g. scanning probe microscopy) characterize surface morphology, there are very few methods for quantifying the roughness of buried interfaces. By tuning synchrotron-produced x-rays either away from or towards the absorption edge, we may distinguish between the roughness of the Si template layer on silicon-on-insulator (SOI) and the silicon/buried-oxide interface in a nondestructive fashion. We calculate that for a 50 nm Si film on a semi-infinite SiO2 layer, resonant scattering cannot adequately resolve the roughness of the buried interface. In the case of thin oxidizing, during oxidation, the surface or the interfacial roughness should yield distinguishable reflectivity profiles. We show initial results of resonant scattering on model SOI systems to determine the buried interface roughness. Supported by NSF and DARPA.


Based on the classical Deal-Grove oxidation model, we propose a simple two layer model for describing silicon oxide growth during the re-oxidation of silicon nitride (SiO2-N) previously deposited (in N2O). Using this two layer model and our experimental results, we determine the activation energy for the diffusion coefficient of oxygen through the nitride oxide layer by applying 3.67 eV which is much higher than for diffusion of oxygen in SiO2. We explain this high activation energy as due to the presence of nitrogen within the SiO2-N layer.

E3.18 On the Interface Quality of MIS Structures Fabricated from Atomic Layer Deposition of HfO2-SiO2, Ta2O5, and Nb2O5/Ta2O5-Nb2O5 Dielectric Thin Films. Salvador Duran1,2,3, Helen Casas1, Hector Garcia1, Juan Barbolla1, Kairo Kuki1,2,3, Mikko Ritvaa1 and Markku Leckebsh1.

Atomic layer deposition (ALD) is one of the most promising techniques to obtain high quality high-k dielectric films. This method allows very good control of the film thickness. Gate dielectrics deposited by ALD show important leakage reduction with respect to conventional silicon dioxide. Among the candidates to substitute silicon dioxide, metal oxides with high band gap like HfO2 and Ta2O5 have been widely studied. These dielectrics have relative dielectric constants of about 18-20 and 25-30, respectively. In this work we present a study of MIS structures (Metal-Insulator-Semiconductor) based on HfO2, Ta2O5, HfO2-Ta2O5, Ta2O5-Nb2O5 dielectric thin films deposited on silicon substrates by ALD. We focus our attention on interface quality and defect density in the dielectric. Interface states limit the carrier mobility in the MOSFET channel, whereas defects in the dielectric cause leakage currents that degrade important features of MOS devices. The interface states as well as defects inside the gate dielectric layer were measured by using capacitance-voltage (CV), deep level transient spectroscopy (DLTS) and conductance transient (Gt) techniques. When defects are spatially distributed in the insulator, the gate oxide is regarded as a disordered material and the number of defects can be evaluated by the number of trapped carriers. The number of traps N is directly related to the density of defects d.


The crystallinity and wet etching behavior of ultrathin (~10 nm) HfO2 films grown by metal organic chemical vapor deposition (MOCVD) were characterized as a function of growth temperature, deposition film thickness, and post-deposition annealing conditions. As-deposited films grown at 450-500°C to a thickness of 3 nm were amorphous (as evidenced by the absence of x-ray diffraction peaks) and slowly etchable in aqueous HF. After a post-deposition anneal at 700°C, these films became insulating to HF and etchable at an average 111 reflection of monoclinic HfO2. In contrast,
thicker (7-10 nm) films deposited at the same growth temperatures were typically impervious to HfO2, as-deposited and showed a moderate x-ray reflection peak at about 90°, indicating high dielectric constant and low dielectric loss resulting from post-deposition annealing. Films produced by thicker these thicker films back to 3 nm had the same crystallinity and wet etch properties as films grown to 3 nm and annealed after deposition. Implications and mechanisms will be discussed.

E3.20

GaSb high quality substrates with thin uniform oxide layers are critical to the development of low-power epitaxially-based GaSb electronic and electro-optic devices. In this material system the thickness and elemental composition of the oxide layers are a strong function of the surface preparation method. Here, a way of determining the thickness variations and qualitative composition of an oxide layer on GaSb has been developed using bromine ion beam assisted etching (Br–IDA). Initial measurements show that the etch rates of most oxides formed on GaSb are much slower than that of GaSb, on the order of 1.5 Å/minute. Hence, nano and sub-nano fluctuations of the oxide thickness due to the oxide surface and substrate/oxide interface, result in amplified roughness fluctuations in the etched GaSb substrate. Furthermore, the overall thickness and composition of the oxide determines the etch depth, given fixed etch times and Br–IDA parameters. In two GaSb samples with identical oxides, atomic force microscopy (AFM) images show that both 90 and 10 minute etch sample have nearly the same roughness (~20 Å RMS), indicating that the Br–IDA process does not change the surface morphology as a function of etch depth. The oxide thickness fluctuations in these samples are calculated to be ~0.35 Å. To determine the effect of overall thickness and compositional variations, another sample prepared with each half having a different oxide, with thicknesses of 11.3nm and 28.6nm respectively. After etching both regions for 10 minutes, the etch depth of the thinner 11.3nm oxide was ~1.2µm deeper than the thicker 28.6nm region, indicating that the compositions of the oxides were vastly different. In this paper we develop the Br–IDA etching technique as a way of characterizing oxide layers on GaSb. This method can be extended to a number of material systems.

E3.21
Theoretical study of reaction mechanisms of ZrCl4 with hydrated and hydrolyzed Si(100) surfaces. Max Peterson, Arcocles, Inc., San Diego, California.

The ever increasing need of device integration in semiconductor technology has driven voltage and power densities across the widely used SiO2 gate dielectric becomes an issue. The most promising approach to overcome this limitation is to replace SiO2 with materials with higher tunnel barriers - the so-called high k materials. One such candidate in this group of materials is ZrO2, typically grown by highly controlled growth mechanisms such as atomic layer deposition (ALD). In the ALD experiment the growing surface is exposed alternately with ZrCl4 and H2O. One of the technological challenges to avoid the formation of SiO2 at the interface to the Si(100) substrate. Therefore the reaction of ZrCl4 with the Si(100) surfaces might be a first step to understand how this interface might form. Hydrated and hydrolyzed Si substrates are studied in order to understand any deterioration of the Si–ZrO2 interface due to formation of SiO2. Particularly, a synchronous transit method combined with density functional theory is used to locate transition states of these reactions. The simulation results show a mechanism for Si–ZrO2 formation that involves the presence of the Si–ZrO2 interface, whereas reactions at hydrated substrates in energetically clearly disfavored.

E3.22
High-k ZrO2 Gate Dielectric on Strained-Si. Sekhar Bhatnagar, S. K. Sumant, S. Chatterjee, J. McCarthy, B. M. Armstrong, H. S. Gamble, C. K. Maiti, T. Perova and A. Macek, School of Electronic and Electrical Engineering, The Queen’s University of Belfast, Belfast, United Kingdom; 1Department of Electronics & ECE, IIT, Kharagpur, Kharagpur, India; 2Department of Electrical and Electronic Engg, Trinity College, University of Dublin, Dublin, Ireland.

Fundamental limits to MOS scaling are rapidly approaching as devices are scaled below 50 nm range. New methods and materials for MOS fabrication are being investigated to allow continued device improvement. [1] Gate leakage reduction in ultrathin gate dielectrics is the main motivation for the search of high-k materials. ZrO2 is being considered as a potential candidate for the replacement of SiO2 due to its high dielectric constant and low dielectric loss.

Recently, the use of strained-Si has attracted considerable attention for advanced CMOS devices because of enhancement in in-plane mobility of both the electrons and holes compared to bulk-Si [2]. In this paper, we present the results of our study on the growth surface characterization of UVH-compatible LPCVD grown strained-Si layers (on both step- and linearly-graded relaxed SiGe virtual substrates) on which high-k ZrO2 ultrathin films have been deposited using microwave plasma CVD at a low temperature of 350°C. The strained-Si layers have been characterized using AFM, TEM and Raman spectroscopy. The layers are 20 nm in thickness and have been characterized with a strain of 0.55%. The electrical properties of the deposited ZrO2 films are also presented. The C-V and G-V characteristics have been used to calculate the interface trap density, near the midgap energy, and the fixed charge density. These are found to be 2.5x10^{12} and 1.4x10^{11} per cm2, respectively. The ZrO2 films also show linear relationship between current density and the applied bias. The conduction mechanism is found to be dominated by the Poole-Frenkel mechanism. The computed dynamic permittivity of the ZrO2 films was found to be ~9.4. We have demonstrated the feasibility of integration of high-k ZrO2 gate dielectric with strained-Si layers for the first time, as a possible candidate for future strained-Si CMOS applications. [3] International Technology Roadmap for Semiconductors, 2002 Update [4] C. K. Maiti et al., Solid State Electron., vol. 41, 1997, p. 1805.

E3.23
Praseodymium silicate formation by post-growth high temperature annealing. Akira Saka1, Shigeki Sakashita, Mitsuo Sakashita, Shigeki Zama, Yukio Yasuda and Seiichi Miyunuki; 1Department of Crystaline Materials Science, Graduate School of Engineering, Nagoya University, Nagoya, Japan; 2Center for Composite Research in Aeronautics, Nagoya University, Nagoya, Japan; 3Department of Electrical Engineering, Graduate School of Advanced Sciences of Matter, Hiroshima University, Hiroshima, Japan.

Research on new high-k dielectric materials to replace SiO2 gate dielectrics has been recently accepted by continuous miniaturization of Si metal-oxide-semiconductor MOS (Si-MOS) devices. This is because the scaling to the diminished size of MOS structures requires simultaneous reduction of SiO2 gate dielectric layer thickness, leading to an increase in tunneling leakage current and degraded dielectric reliability. In the regime of exploring and developing new high-k materials compatible with the MOS device manufacturing, the stability of high-k layers in contact with Si during high temperature annealing is one of crucial factors. It is generally reported that the thermal instability results in the growth of unwound low-k interface layers, such as SiO2 and silicate, and a noticeable decrease in the effective k value is eventually obtained. Thus the preparation of thermally-robust high-k layers is an urgent issue to meet the stringent requirement for generation of next generation MOS technology. In this work, we focus on praseodymium silicate (Pr2SiO5) which meets both requirements for having a high dielectric constant and high thermal stability. We present an approach to form Pr2SiO5 by using decomposition of PrO2 or Pr3O7 under high temperature post-growth rapid thermal annealing (PORTA). In experiments, Pr2O3 films with a thickness ranging from 7 to 10 nm were deposited on hydrogen-passivated Si(111) substrates at a temperature between 300-400°C using a high rate pulsed laser deposition system with a base pressure of 1x10^{-7} Torr. A powder-packed ceramic Pr2O3 was used for electron beam evaporation. The pressure during deposition was in the range of 10^{-6} Torr and, in some cases, an oxygen gas was intentionally introduced up to 5x10^{-7} Torr. These films were then subjected to PORTA at a temperature of 1000°C for 1 minute in an N2 environment. It has been revealed by transmission electron microscopy that re-deposited films typically have a hexagonal or cubic Pr2SiO5 phase grown epitaxially on Si(111) with high-quality interface layers. Structural variation depending on the growth condition was also seen; lowering the temperature and the oxygen partial pressure during deposition promotes epitaxy. However, the films grown under the oxygen deficient conditions frequently show high leakage currents in current-voltage characteristics. On the contrary, PORTA drastically alter the film structure into an amorphous phase. The obtained film is completely homogeneous and has no interface layers. We used X-ray photoelectron spectroscopy to measure chemical composition of the films and confirmed the intermixing of Si into Pr2O3 to form Pr2OxSi1-x alloys [5]. We also present preliminary results of the electrical properties and a leakage current density for Pr2SiO5 grown under an optimal growth condition are 20 and 3x10^{-9} A/cm2 at +1 V relative to flat band voltage for an equivalent oxide thickness of 1.8 nm, respectively.

E3.24
Analysis of N2, NH3 annealing effect on HfAlO2 gate dielectric...
dielectric films grown by chemical vapor deposition using a single molecular precursor. Suk Won Lee, Joohee Park, Hong Bae Park, Rong-Chan Chang, and Sung-Jin Hong, School of Materials Science & Engineering, Seoul National University, Seoul, South Korea.

HfAlOy gate dielectric films were deposited on Si and HF-cleaned Si wafers by chemical vapor deposition (CVD) method using Hf-Al single molecular precursor [HfAl (OC(Si)3)]2 [OC(SiH2)3]2. HfAlOy was treated under N2 and NH3 atmospheres by rapid thermal annealing at 600 °C for 30 s, respectively. The C-V characteristics of the films were measured at different temperatures during N2 and NH3 rapid thermal annealing up to 800 °C and then gradually decreases at 900 °C. Flat band voltage slightly increased with the increasing annealing temperature. However, the flat-band voltage was remained at the initial value of 600 and 700 °C rapid thermal annealing. The reflectivity of the capacitor structures became significantly higher at high bias voltage than those in the capacitor structures with lower bias voltage. The reflectivity (XRR) measurements. In this work the film microstructure will be compared to the microstructure of films deposited by LAMO at room temperature.

E3.21 Room Temperature Fabrication of Al2O3/TiO2(Ta2O5) /Al2O3 Nanolaminate for High Dielectrics, Wei Fan1, Jian Zhou1,2, Y. L. Edge2, C. H. Peng2,2, Y. A. Liu2,2, R. Milliner2, D. Huang2, M. Fontana2, D. A. Burns2, and Y. A. Liu1,1. 1School of Materials Science and Engineering, Penn State University, University Park, Pennsylvania; 2Institut für Schichten und Grenzflächen ISG-IT, Forschungszentrum Jülich, Germany. The application of ultra-high k (ε_r > 50) TiO2 as a gate dielectric is hampered primarily by its high leakage current as the result of a close zero offset barrier to Si and its instability with Si and the polysilicon gate on CMOS. The other band, Al2O3 with low permittivity (ε_r ~ 10) exhibits a large band gap (E_g ~ 6.8 eV) and excellent thermal stability with Si. To take advantages of the combined properties of Al2O3 and TiO2, nanolaminate Al2O3/TiO2/Al2O3 and Al2O3/TiO2/Al2O3 multilayers were developed for a dielectric structure with high permittivity and good thermal stability. The layered dielectric stacks were fabricated by two different methods: a) post-deposition oxidation of sputter-deposited AlTi/Ti[Al]/Al metal multilayers with high-temperature oxygen plasma; b) oxidation of the same multilayers by co-deposition of O2 and Al or Ti in an MBF system. For the first method, the top Al2O3 layer inhibits oxidation of the Ti[Al]/Al metal stack by preventing oxygen diffusion, resulting in a two-way dielectric stack due to the incomplete oxidation of the central Ti layer. A modified two-step oxidation process, involving oxidation of the Ti[Al]/Al structure followed by deposition and oxidation of the top Al layer, was employed in this work to overcome the incomplete oxidation problem of the central TiO2 layer, while preventing the formation of SiO2 at the Si interface. For the second method, molecular beam deposition (MBD), we investigated the uniaxial oxygen pressure dependence of Al and Ti sputter deposition and the combination (to avoid producing a SiO2 interlayer), using a quartz crystal microbalance. Fully oxidized Al2O3/TiO2/TiO2/Al2O3 dielectric layered structures with a Si, 1 nm EOT were achieved on Si as compared to the results using both methods described above. A detailed comparison between the structural and dielectric properties of sputter- and MBD-deposited dielectric layers will be discussed.

This work was supported by the US Department of Energy, BES/Matter Science Under Contract W-31-109-ENG-38.

E3.22 Characterization of Titanium-Aluminum Oxide Thin Films for New Generation of CMOS Gases via Spectroscopic Ellipsometry, Ciro M Lopez1, N A Swovick2, W Pan3, O Aucelli2 and E A Irene4, 1Chemistry, University of North Carolina-Chapel Hill, Chapel Hill, North Carolina; 2Materials Science Division, Argonne National Laboratory, Argonne, Illinois. New titanium-aluminum oxide thin films were fabricated on Si(100) substrates by ion-beam sputter deposition of a Ti-Al alloy target and subsequent oxidation at temperatures ranging from 725 °C-500 °C. These thin films are being investigated as candidates for the new generation of gate oxides, since they exhibit properties compatible with the requirements of next generation CMOS gates. A combination of Rutherford backscattering analysis to obtain film composition and cross-sectional transmission electron microscopy to reveal thickness and the film stack structure were used to provide information, in order to construct an optical model for the material, based upon SE and SES data. Spectroscopic ellipsometry on Ti-Al alloy oxide films with various thicknesses yielded the optical properties of these films. The optical properties were also modeled using Lorentz oscillators. Physical thickness of titanium-aluminum oxide and interface SiO2 thicknesses were determined from the model and compared with values obtained from other analytical techniques. From a Tan plot the band gap was estimated to be 3.8 eV. This work was supported by the US Department of Energy, BES/Matter Science, Under Contract W-31-109-ENG-38 NS/ONR under Contract N00014-98-J-1178 (UNG-CI).

E3.23 High-k Dielectric Characterization by combined VUV Spectroscopic Ellipsometry and X-Ray Reflectometry, P. Bohrer1, P Ferrand2, G Deffieux2, A Darragon1, Linhong Sun2, J C. Futter5, J L. Sehle6, E Bidal7 and H Bender1, 1SPRRA Inc, Acton, Massachusetts; 2ESSPA SA, Bois Colombes, Paris, France;

Materials Science Division, Argonne National Laboratory, Argonne, Illinois. The application of ultra-high k (ε_r > 50) TiO2 as a gate dielectric is hampered primarily by its high leakage current as the result of a close zero offset barrier to Si and its instability with Si and the polysilicon gate on CMOS. The other band, Al2O3 with low permittivity (ε_r ~ 10) exhibits a large band gap (E_g ~ 6.8 eV) and excellent thermal stability with Si. To take advantages of the combined properties of Al2O3 and TiO2, nanolaminate Al2O3/TiO2/Al2O3 and Al2O3/TiO2/Al2O3 multilayers were developed for a dielectric structure with high permittivity and good thermal stability. The layered dielectric stacks were fabricated by two different methods: a) post-deposition oxidation of sputter-deposited AlTi/Ti[Al]/Al metal multilayers with high-temperature oxygen plasma; b) oxidation of the same multilayers by co-deposition of O2 and Al or Ti in an MBF system. For the first method, the top Al2O3 layer inhibits oxidation of the Ti[Al]/Al metal stack by preventing oxygen diffusion, resulting in a two-way dielectric stack due to the incomplete oxidation of the central Ti layer. A modified two-step oxidation process, involving oxidation of the Ti[Al]/Al structure followed by deposition and oxidation of the top Al layer, was employed in this work to overcome the incomplete oxidation problem of the central TiO2 layer, while preventing the formation of SiO2 at the Si interface. For the second method, molecular beam deposition (MBD), we investigated the uniaxial oxygen pressure dependence of Al and Ti sputter deposition and the combination (to avoid producing a SiO2 interlayer), using a quartz crystal microbalance. Fully oxidized Al2O3/TiO2/TiO2/Al2O3 dielectric layered structures with a Si, 1 nm EOT were achieved on Si as compared to the results using both methods described above. A detailed comparison between the structural and dielectric properties of sputter- and MBD-deposited dielectric layers will be discussed.

This work was supported by the US Department of Energy, BES/Matter Science Under Contract W-31-109-ENG-38.

E3.24 Characterization of Titanium-Aluminum Oxide Thin Films for New Generation of CMOS Gases via Spectroscopic Ellipsometry, Ciro M Lopez1, N A Swovick2, W Pan3, O Aucelli2 and E A Irene4, 1Chemistry, University of North Carolina-Chapel Hill, Chapel Hill, North Carolina; 2Materials Science Division, Argonne National Laboratory, Argonne, Illinois. New titanium-aluminum oxide thin films were fabricated on Si(100) substrates by ion-beam sputter deposition of a Ti-Al alloy target and subsequent oxidation at temperatures ranging from 725 °C-500 °C. These thin films are being investigated as candidates for the new generation of gate oxides, since they exhibit properties compatible with the requirements of next generation CMOS gates. A combination of Rutherford backscattering analysis to obtain film composition and cross-sectional transmission electron microscopy to reveal thickness and the film stack structure were used to provide information, in order to construct an optical model for the material, based upon SE and SES data. Spectroscopic ellipsometry on Ti-Al alloy oxide films with various thicknesses yielded the optical properties of these films. The optical properties were also modeled using Lorentz oscillators. Physical thickness of titanium-aluminum oxide and interface SiO2 thicknesses were determined from the model and compared with values obtained from other analytical techniques. From a Tan plot the band gap was estimated to be 3.8 eV. This work was supported by the US Department of Energy, BES/Matter Science, Under Contract W-31-109-ENG-38 NS/ONR under Contract N00014-98-J-1178 (UNG-CI).
At present, new high-k dielectric materials are being intensively investigated to replace the silicon dioxide as gate dielectric for the next generation of electronic devices. Several candidate materials (such as HfO2, HfAlO3, and deposition processes are currently under investigation. Because the layer thickness which is required in the next generation of devices is of the order of few nanometers, a precise determination and control of each thickness will be mandatory. Although spectroscopic ellipsometry (SE) is an established non-contact, non-destructive and precise technique for determining thickness and optical properties of thin films, it becomes more difficult to get this information simultaneously and simultaneously for ultra-thin films with traditional SE alone because of possible high correlations between film structure and optical properties. In this study, a complementary non-destructive Grazing X-ray reflectometry (GXR) was introduced to extract the thickness of such thin films. Finally, the optical properties of the films were determined using Vacuum Ultraviolet Spectroscopic Ellipsometry (VUV-SE), which covers a wide spectral range down to 10-nm wavelength. Within the VUV range, all the high-k dielectric materials under evaluation are no longer transparent. This enhances the capability of using SE for such high-k dielectric film characterization. HfO2, HfAlO3 and HfAlOx films were deposited on silicon substrates with Atomic Layer Deposition (ALD) and Hf(II) complex precursors with H2O were used as precursors for HfO2 and HfAlO3 respectively. ALD concentration in HfAlOx was varied by changing the relative number of HfCl4 and Al(CH3)3 cycles [2:1, 1:1 and 1:2]. The characterization results show a strong aluminum concentration dependent and optical constants (refractive index and extinction coefficient) in VUV range. This proposes a way to quantitatively determine ALD concentration in HfAlOx films and their thickness.

**E3.30**

Strontium Titanate Thin Films on Thermally Oxidized and Bare Si Substrates. Natalia A. Savcović1, Ciro M. Lopez1, Alexandra A. Savcović2, Marcin Saunders2 and Eugene A. Irene1.

1Department of Chemistry, University of North Carolina-Chapel Hill, Chapel Hill, North Carolina; 2Centre for Microscopy and Microanalysis, University of Western Australia, Crawley, Western Australia, Australia.

Among the choices for the high dielectric constant (K) materials for future generation MOSFET application, strontium titanate (STO) is one of the promising candidates for alternative gate oxide. Deposition of STO thin films, however, poses several problems. The major one is a production of high level of interface states (Dit) compared to that of SiO2 on Si. An insertion of a thin SiO2 layer prior the growth of STO thin film is a simple solution that helps to limit the interface states. Si substrate and attains a high quality interface. However, the combination of two thin films reduces the overall K of the dielectric stack. An optimization of the STO underlayer in order to maintain the interface quality yet maximal the effect on K is the focus of this work. The results from our study are presented with emphasis on the key process parameters that improve the dielectric film stack. For in-situ growth characterization of STO film grown on thermally oxidized Si substrates spectroscopic ellipsometry has been used. Studies of material properties have been complemented with analytical electron microscopy. Electrical characterization has been employed using the Pt/STO/Si structures. From conductance-voltage analysis, the interface trap density Dit was observed to significantly decrease for the capacitors grown on oxidized Si substrates and annealed in forming gas.

**E3.31**

Optical and Dielectric Properties of Eu- and Y-Polycrystalline Thin Films Grown by RF Sputtering on Si Substrates. Vladimir Vasiljev1, Alvin Drehman1, Helen Dauphais1, Lionel Bouthillet2, Mark Roland2, Alex Volkov2 and Stefan Zbinden2.

1Semiconductor Products Sector, Motorola, Inc., Tempe, Arizona, 2Sematech, Austin, Texas, 3Institute of Microelectronics, AFB, Massachusetts, 4Solid State Scientific Co., Hollis, New Hampshire.

We report further results of our study of one family of thin film rare-earth polycrystalline thin films, REuOz, 9 (REEu, Tb, Y, Mn, Nd), which exhibit highly efficient photo-luminescent characteristics. Earlier we have [1] shown that the crystalline films of stoichiometric Eu-Y polycrystalline thin films (Eu, Y, 1-x, Tb, EuO0.1) can be grown by RF magnetron sputtering on Si, fused silica and sapphire substrates. These films exhibited an intense red emission under UV excitation. Because Tb and rare-earth oxides are currently being considered as an alternative to silicon dioxide as high-k gate dielectric for CMOS devices scaling below 0.1 µm, these films of rare-earth polycrystalline could be of interest as new materials with high dielectric constant. This study is a first attempt to investigate basic physical properties of thin films of polycrystalline containing Eu, Y, and their solid solutions. Films with the thickness of 30 to 500 nm were deposited on Si substrate at room temperature by RF magnetron sputtering in Ar atmosphere and post-annealed in oxygen at 900 to 1000 °C. Using x-ray diﬀractometry, AFM, SEM, HR-TEM, spectroscopic ellipsometry, and standard dielectric testing procedure, the thickness of films, surface roughness, refractive index, low-frequency dielectric constant, and breakdown and leakage current were determined for the deposited amorphous and post-annealed crystalline films. Also we have studied structural and morphological properties of the Film/SiO2/Si interface, and compared that to luminescent and dielectric measurements. Supported by the Air Force Office of Scientific Research, through the National Research Council at the University of Virginia, V.Vasiljev, A. Drehman and L. Bouthillet, Characterization of Eu- and Y-polycrystalline Films Deposited by RF Diode Sputtering. MRS Symp. Proc., Vol. 749, W5.8.1.

**E3.32**

Characteristics of hetero structures composed of oxides and foreign compound materials on Si for the future novel devices. Nao Yamaoka1, Takeshi Kashiwagi2, and Tatsuo Yamaguchi1,2,3.

1Nanomaterial Assembly Group, National Institute for Materials Science, Tsukuba, Ibaraki, Japan; 2CREST, JST, Japan; 3FUJ Electric Corporate Research and Development, Yokosuka-shi, Japan.

Over the last decade, there has been increasing interest in the development in functional oxide devices, such as ferroelectric memories and optoelectronics. One of the most fundamental but fascinating structures for device applications is heterojunction between oxides and foreign materials, where metals are involved. To fabricate such devices, selecting proper substrates is also crucial, but it does not only affect the device performance, but also open new possibilities for realizing novel devices. In this respect, Si must be one of the highest potential substrates due to matured process technology. In this presentation, we demonstrate two types of heterostructures on Si, namely oxide/silicide and metal/oxide hetero structures respectively. First, heterojunction composed of SrTiO3 and wide bandgaps (4.5 eV) are fabricated on p-Si and their structural and electrical properties are investigated. The second, heterostructures composed of metal alloy on ZnO are fabricated and their electrical properties are described. Combinatorial method is applied for the quick optimization and the systematic study of those obtained heterostructures in both experiments.

**E3.33**

The adoption and infiltration of Al2O3 interlayer for improving thermal stability and flat-band behavior of HfO2 gate dielectric films grown by atomic layer deposition. Hong Bae Park, Moonju Cho, Joshoo Park, Suk Woo Lee and Cheol Seong Hong, School of Materials Science and Engineering, Seoul National University, Seoul, South Korea.

HfO2/Al2O3 gate dielectric thin-film stacks were deposited on HF-cleaned Si wafers using an atomic-layer-deposition (ALD) technique. A 2.3 nm-thick Al2O3 interlayer was grown at 450°C using Al(CH3)3 and O3, and 4 to 5-nm-thick HfO2 films were grown on Al2O3 at 510°C using HFC4 and H2O as a precursor and an oxidant. The Al2O3 interlayer was treated under a NH3 atmosphere at 790°C for 48 sec prior to HfO2 deposition with and without the r-f plasma. The plasma-nitridation increased the Al2O3 interlayer thickness by approximately 0.9 nm and decreased the overall capacitance, whereas thermal-nitridation did not increase the Al2O3 interlayer thickness, and the overall capacitance was the same as that of the non-treated HfO2/Al2O3 stack. The thermal stability of the capacitance density was also improved by the nitridation of the inter-layer. The flat-band voltage was controlled to the ideal value, and the hysteresis in the current-voltage plots of the HfO2/Al2O3 stack became very small as a result of thermal-nitridation. Furthermore, the flat-band dielectric capacitance of the sample with the nitrided Al2O3 inter-layer decreased from that of the non-treated sample by almost one order of magnitude.

**E3.34**


Thin oxide films exhibit many attractive properties such as colossal magnetoresistance, ferroelectricity, and superconductivity. SrTiO3, in particular, has been suggested as a possible candidate to replace SiO2 in electronic devices [1]. The strong interplay between the atomic and electronic degrees of freedom makes the control of the
microscopic structure of oxide-oxide interfaces is an important challenge for practical applications. In this context, a detailed analysis of the epitaxial growth of strontium titanate on the MgO(001) surface is performed [2], based on the density-functional theory. Several configurations for the ad-layers are considered. We show that the cubic-on-cube TiO2/MgO contact is favoured among all the studied stoichiometric configurations, because of the formation of quite strong interfacial bonds favouring stress relaxation. The SrO/ TiO2 adlayer shows many analogies with much thicker disordered SrTiO3 films. We also analyse the relevance of chemistry on the stability of the interface, considering the most frequent defects, such as O vacancies (on both sides of the interface) and stacking faults in the SrO/TiO2 systems, better known as Ruddlesden-Popper phases SrO_xTiO_2-x. The electronic properties of these interfaces are in general strongly dependent on the local atomic environment.


CENTER FOR SUPERCONDUCTIVITY RESEARCH, UNIVERSITY OF MARYLAND, COLLEGE PARK, MARYLAND; 3US ARMY RESEARCH LABORATORY, ADENPHI, MARYLAND.

AI has excellent properties of high breakdown strength, a thermal conductivity and dielectric constant. It grows epitaxially on 6H-SiC, as they have hexagonal crystal structure. In this work we report the passivation of SiC-based devices by a high-temperature process. A high-temperature deposition technique of SiC on SiC-based devices is developed. A novel technique of off-axis rotation is utilized to cover the sidewalls to achieve the deposition of the best quality AIN on side walls of devices. In second approach, we use RF Sputtering of AIN from a high purity Al (99.999%) pellet in Ar and N2 atmosphere. The technique of sputtering provides sufficient coverage of sidewalls than the pulse laser deposition. A comparison is made between the crystalline quality of AIN films deposited by two techniques using X-ray diffraction. The morphology of the film, which is expected to be uniform, is monitored by scanning electron microscopy. The relative merits of the pulsed laser deposited and RF sputtered AIN films are investigated from the point of view of aspect ratio, leakage characteristics and interface properties.

SESSION E4: High-K Oxides, Metal Gates and Integration

Chair: Andre Steensma and Akira Toriumi

TUESDAY MORNING, DECEMBER 2, 2003

ROOM 17 (Hynes)

8:30 AM E4.1 Thermal Stability and Electrical Properties of Ru Films by Selective MOCVD on AlD HfO2 and ALD LaAlO3.

Jagdish Gaurani1, Daeung Gu1, Anishan Das1, Wei Cao1, Sandip K. Dey1, Steven Marcus2, Henk de Waard2 and Chris Verheijen2.

1Arizona State University, Tempe, Arizona; 2ASML America, Inc., Phoenix, Arizona.

Selective deposition of Ruthenium (Ru) films was carried out on patterned HfO2 and LaAlO3 surfaces (deposited by atomic layer deposition or ALD) using a liquid-source metalorganic chemical vapor deposition (MOCVD) technique. The Ru films (30-200 nm) were deposited on the ALD and kinetically controlled regions at temperatures (Tsubstrates) between 250 and 350 °C and a total pressure of 1 Torr. Note, oxygen-assisted pyrolysis was used to decompose the Bis (2.2-dimethylbutylacetylene) ruthenium (1-cyclooctene) Ru (or Ru/(THF))2COD) precursor to reduce carbon contamination. In the kinetically controlled regime (250-350 °C), the activation energy was 136 kJ/mol, and Ru films deposited in this regime exhibited no interfacial Ru coverage. The Ru films deposited at Tsubstrates of 260 °C showed a highly dense and polycrystalline microstructure (grain size: 2.5 nm) with amorphous grain boundaries and an interfacial layer between HfO2 and RuO2; from RBS, XPS, HRTEM, and EELS, the amorphous layer was found to be RuO2.

However, the higher sticking coefficient of Ru/(THF)2COD in the mass transport controlled regime at 350 °C resulted in poor step coverage of 80% or less. Moreover, even when a layer was raised to 150 °C, a very high oxygen flow-rate of 500 sccm was used, phase-pure and polycrystalline RuO2 was deposited on HfO2. The electrical resistivity (ρ) for the as-deposited Ru films (75-100 nm) was ∼15 μΩ cm, but it increased negligibly below 50 °C due to the low vacuum. For Pt on 1050 °C in vacuum, showed a higher degree of (001) texture, stronger temperature dependence of ρ and higher residual resistivity ratio (RRR = ρ300K/ρ at 300K) of ∼10 compared to as-deposited films. The work functions by selective MOCVD of HfO2 and LaAlO3 surfaces, determined from the capacitance-voltage measurements, were ∼5.3 and ∼4.9 eV, respectively. The variation of the work function after various annealing treatments will be presented and discussed.

8:45 AM E4.2 Schottky Barriers at Transition-metal/Stannite-titanate Contacts. Marcoz Mrovec1 and Christian Elsesser2.

1Fraunhofer IWM, Freiburg, Germany; 2IZBS, University of Karlsruhe, Karlsruhe, Germany.

Local electronic structures at coherent interfaces between cubic (001)-oriented SrTiO3 substrates and transition-metal films have been studied by means of the density functional theory with the mixed-basis pseudopotential approach. The main focus of this work is to investigate the influence of the chemical composition, atomistic structure and externally applied electric fields on the Schottky barrier of the studied metal/ceramic contacts. The calculations have been performed for six transition metals from groups VI A (Cr, Mo, W) and VII B, Ni, Pt, Pd) in order to analyse the effects of both size and different electronic structure. Furthermore, in the cases of Ni and Cr the role of intermediate oxide monolayers is examined.


1Motorola Inc., Tempe, Arizona; 2Kintech Technologies Ltd., Moscow, Russian Federation; 3Motorola Inc., Austin, Texas.

The work functions of Mo, TiN, HfN, and TaN have been calculated on SiO2, HfO2, and vacuum using first-principles techniques, and compared to experimental values. The electronic properties calculated for the model structures strongly depend on the atomic level structure of the model. Since the atomic structure in most cases cannot be determined by a direct experiment, the model structures need to be chosen with great care. We will show how total energy calculations and simple thermodynamic arguments can be used to make a reasonable selection. The impact of a bonding configuration on the metal work function will be discussed. We will also show how the bulk-derived Fermi level pinning parameters and the charge neutrality level for HfO2 and SiO2 compare with values extracted from the data and interface calculations. Finally, we will identify Fermi level pinning properties that are intrinsic to the dielectric and those that are connected to the metal gate through comparison between different metal gate dielectrics and from our previous results for Polysil/SiO2 interfaces.

9:15 AM E4.4 Thermal Stability of PVD TaSiN with high-k dielectric. Michael Gravelios1, Alessandro Callegari2, Cyril J. Legrand2, Vijay Narayanan2, 4Semiconductor Research and Development Center, Microsystems Division, IBM, Hopewell Junction, New York; 5Semiconductor Research and Development Center, Research Division, T. J. Watson Research Center, IBM, Yorktown Heights, New York.

Gate stacks consisting of Si/HfO2 dielectric/TaSiN are shown to be thermally stable during high temperature annealing. The stacks have been analyzed by a combination of high resolution TEM and small probe electron energy loss spectroscopy (EELS). The high k dielectrics studied were ALD grown ZrO2, A12O3 and HfO2. The TaSiN/dielectric interface was found to be rough due to damage incurred during PVD TaSiN deposition. As-deposited, TaSiN is predominantly amorphous with some small crystal areas less than 2 nm in diameter. Stacks annealed at 1000°C in nitrogen showed no sign of a TaSiN/dielectric interfacial reaction both by EELS and HRTEM, thus proving that the material is thermally stable on high-k oxide films. A work function of ~ 4 eV was measured on capacitors produced from these stacks using the ViBe vs EOT measurement method. The data has also shown flat band shifts and wide hysteresis, which may be due to fixed charges formed during PVD TaSiN deposition, high-k film deposition or due to insufficient post metal anneals of a TaSiN/dielectric gate stack. To reduce damage during electrode deposition alternative deposition methods might have to be considered for successful implementation of TaSiN as potential gate material in future generations of CMOS devices.
10:00 AM E4.5
Study of metal gate work function modulation using plasma and SiH4 treated TiN thin films. Fillos Frederic1, Sylvain Maitrejean2, Thierry Ferjot2, Bernard Guillaume2, Bernard Chevrel2 and Gerard Passmenard3.1 DTS, CEA-LETI, Grenoble, Grenoble, France, 2UMR 5628, LMG-CNRS, Grenoble, Grenoble, France.

As gate oxide thickness decreases, the capacitance associated with the depleted layer at the oxide interface becomes significant. It is necessary to control alternative gate electrode materials. TiN films elaborated with TiCl4 precursor are widely studied as gate metal in MOSFETs. In this work, we investigated the impact of TiN gate metal deposited by MOCVD using TDMA precursor on the electrical properties of the N2H2 plasma application and SiH4 treatment after TiN thin film growth. We also studied the physical properties of this gate metal. The electrical properties of the gate metal were then compared to the oxide thickness. A series of TiN gates were deposited in a chamber using a commercial 8 inch wafer deposition tool. In these experiments, structural and compositional properties of TiN were correlated with work function measurements. The evolution of the composition (Carbon content) was studied with spectroscopy (AES, SIMS) as a function of plasma and SiH4 treatments; details on the microstructure (XRR, XRD, AFM) will also be given. Secondly, MOS structures were processed on uniformly doped p-type wafers. C-V curves of capacitors are used to estimate the flat band voltage and to extract the work function, the fixed charges in oxide and the density of interface states. It is shown that as-deposited amorphous films exhibit a work function of 4.45 eV. Slight discharges are shown to increase this work function. Thin film properties are not impacted by anneal treatments. Work function stability is tested at 500°C, 900°C and 1050°C. Thermodynamic compatibility with gate oxide was verified thanks to experimental results and calculations.

10:15 AM E4.6
Mechanism of Self-Organized Decomposition of the Si Template Layer in Ultrathin Silicon-on-Insulator: Jin Yang1, Pengpeng Zhang1, Feng Liu2 and Max G Lagally1. 1University of Wisconsin-Madison, Madison, Wisconsin; 2University of Utah, Salt Lake city, Utah.

Silicon-on-insulator (SOI) is rapidly becoming a mainstream substrate in microelectronics fabrication. SOI technology greatly reduces the power consumption and improves the performance of CMOS transistors. The Si template layer on ultrathin SOI (0.1μm), which can be as thin as several nanometers, is thermally unstable and decomposes at high temperatures into 3D silicon islands that show a unique pattern.[1,2] We have used AFM, SEM, and low-energy electron microscopy (LEEM) observations of the decomposition of ultrathin SOI in real time to investigate the mechanisms of self-organizational decomposition. The decomposition starts from defect sites, such as pinholes and sites where threading dislocations exit the film, and proceeds outward from these sites. Plastic relaxation in the 3D directions, which should be the easiest directions to relax the stress associated with the defect sites, is at later stages, Si islands form along <013> directions into a pattern with good long-range order. The 3D island diameter is on the order of one hundred nanometers, depending on the initial Si template layer thickness and the rate of decomposition. Real-time LEEM observation has revealed the detailed mechanisms and processes for such island formation and ordering. Si atoms first diffuse away or evaporate to form individual trenches with stable [111] side facets. Consequently, the trenches extend along <013> directions. As two adjacent trenches expand in width, a narrow ridge with [111] facets forms along the [013] direction. The ridge eventually breaks into isolated silicon islands due to the Rayleigh instability [3], leading to the final island patterns. [1] B. Legrand, V. Aigrain, J. P. Nys, V. Senez, and D. Stevieen, Appl. Phys. Lett. 76, 3271 (2000); [2] R. Nuryadi, Y. Ishikawa, and M. Takebe, Appl. Phys. Lett. 121, 121 (2008); [3] D. K. Rayleigh, London Math. Soc. Proc., Ser. 1, 10, 4 (1879). Supported by ONR, NSF, and DOE.

10:30 AM E4.7
Structural Comparisons of SiOx and Si/SiOx Formed by Passivation of Single-Crystal Silicon by Atomic and Molecular Oxygen. Maja Kan1, Judith C. Yang1 and Ray D. Twesten2.
1Materials Science and Engineering Department, University Of Pittsburgh, Pittsburgh, Pennsylvania; 2Frederick Seitz Materials Research Laboratory, Center for Microanalysis of Materials, Urbana, Illinois.

The structural characteristics of a silicon layer and Si/SiOx interface formed on Si single-crystal by oxidation in hyperthermal atomic oxygen (AO) and molecular oxygen (MO) at 850°C were compared by High Resolution Transmission Electron Microscopy (HRTEM), Electron Energy Loss Spectroscopy (EELS), Atomic Force Microscopy (AFM), Rutherford Backscattering Spectrometry (RBS), Scanning Electron Microscopy (SEM) and X-ray Photoelectron Spectroscopy (XPS). The thermal oxidation AO process created the pulsed laser deposition of oxygen gas. We previously determined by RBS and HRTEM that AO forms an amorphous oxide on Si(100) and this oxide is nearly twice the thickness and approximately two times rougher surface than formed by MO. Here we report that the silicon layer formed on Si(111) by AO is also nearly twice the thickness and about seven times rougher surface than formed by MO. The oxide formed by AO and MO is both amorphous in electron diffraction (SAED). However, the oxide formed by AO has a less random distribution of silicon and oxygen atoms compared to the oxide formed by MO. Evidence for SAED and EELS spectra. In contrast to MO formed silicon, initial EELS spectra across the Si/SiO2 interface revealed no region of sub-oxides near the interface in the AO formed silicon. SEM and AFM experiments were performed at the MIEE Division, University of Pittsburgh, HRTEM, EELS, XPS and RBS experiments were carried out in the Center for Microanalysis of Materials, University of Illinois, which is partially supported by the U.S. Department of Energy under grant DEFG02-91ER45439.

10:45 AM E4.8
Electronic and Optical Carrier Injection in Layered High-K Dielectric Structures. Julie D. Camporesi1, Marcin J. Wolny2, Heiner B. Förster3, Brett W. Busch4, Min Yue He4, Murin L. Green4, Roy Gordon1 and Harry A. Answer1. 1Applied Physics, California Institute of Technology, Pasadena, California; 2Jet Propulsion Laboratory, Pasadena, California; 3Chemistry, Harvard University, Cambridge, Massachusetts; 4Agera Systems, Murray Hill, New Jersey.

We have modeled and fabricated silicon-compatible layered high-k dielectric constant structures that enable carrier injection from a silicon channel to a floating gate, and thus threshold voltage or contact electrode voltage to be modulated by an applied bias. We utilize an effective mass tunneling model to predict the current-voltage characteristics and carrier distributions in layered tunnel barrier structures under applied bias. Experimental characterization of tunneling and band offsets has been performed using current-voltage and capacitance-voltage measurements and internal photoemission spectroscopy measurements to obtain band offsets. We find from our simulations that some of the metal-insulator barrier structures for layered tunnel barrier of Al2O3 with SiN4 or HFO2 and we have fabricated such structures. The Si2N4 was made by low-pressure chemical vapor deposition, while the Al2O3 and HFO2 were made by atomic layer deposition. We have fabricated and characterized the layered barrier structures Si2N4 / Al2O3 / SiN4 and HFO2 / Al2O3 / HFO2 as single- and double-layered structures using these materials. These heterostructures are designed to enable carrier injection into floating gate structures with dramatically increased programming speeds in nonvolatile memory devices, such as flash memories and microcrystalline memories. Such silicon-compatible layered barrier heterostructures that enable a large increase in the barrier height with applied voltage are promising candidates to reduce the power dissipation and increase the performance of floating gate memory devices for nonvolatile memories. Since voltage-dependent barrier lowering may also form the operating principle for a new class of photodetectors with electrically tunable cutoff wavelength. Internal photoemission spectrosopes have been fabricated on metalsemiconductor structures with semi-transparent gates in order to directly measure the band offsets of layered tunneling barrier structures, using a chopped multiple wavelength illumination. Our measurements indicate band offsets for SiO2 and Al2O3 to be 3.5 eV and 3.1 eV, respectively. Our measurements for other single dielectrics and heterostructures will be presented.

11:00 AM E4.9
Nitrated Hafium Silicate Film Formation by Sequential Process Using a Hot Wall Batch System and Its Application to Hot Carrier Transistor. Tomonori Aoyama1, Takahiro Yagisawa2, Masahiro Mitsukura3, Takeshi Mieda4, Satoshi Kuriyama3, Atsushi Horuchi5, Hiroshi Kitajima5 and Tsuneto Ariikado1, Research Dept. 1, Semiconductor Leading Edge Technologies, Inc., Tsukuba, Japan.

We have developed the novel high-k gate dielectric formation process. Si pre-oxidation (t1 = 0.5μm), HfSiOx, MOCVD and post deposition annealing are sequentially performed using a hot wall batch-type LP-CVD system in order to suppress contamination between processes. HfSiOx, MOCVD with gate length 100nm with using a hafnium tetracetoxide and dilimine mixture. The post deposition annealing consists of oxidation and nitridation using O3 and NH3, respectively. O3 oxidizes carbon remained in the HfSiOx film and NH3 treatment incorporates nitrogen into the film to improve the thermal stability. Analyses using RBS and SIMS reveal that this film is HfO_xSi_yO_zN_m. Distribution of equivalent oxide thickness (EOT) and composition are uniform enough to within only a 30nm wafer but also within a batch. In addition to control film contamination, suppression...
this sequential process has an ability to achieve high throughput from pre-oxidation to NH$_3$ treatment. These dielectrics (3nm HSiON/10nm SiO$_2$) were applied to MOSFET NMOS and PMOS were fabricated using the CMOS process except for the gate dielectrics. In order to accomplish higher reliability, the gate dielectrics should keep amorphous after activation of dopants [P and B] implanted into the substrate and the poly Si gate. NiSi$_2$ nitridation at 700°C for 10min improves thermal stability of HSiON so that the film keeps amorphous condition even after 1050°C low annealing. EOT of 1.47um and low leakage current of 1.3mA/cm$^2$ at 1.1V could be obtained. These results show that the expected target values for 65nm-node LSITP CMOS technology. In addition, high electron and hole mobility were obtained.

11:15 AM E4.10
Band Offsets at the SrTiO$_3$/Si Interfaces.
Ahn Shu-Chung, Win, Fabrice Amy and Antoine Kahn, Electrical Engineering, Princeton University, Princeton, New Jersey.

The continuous drive toward faster electronics and scaling down of MOSFET device dimensions requires alternatives to SiO$_2$ for gate dielectrics. High-k dielectrics have therefore received considerable attention from industry and the scientific community. Cerium-based perovskite oxides such as SrTiO$_3$ and BaTiO$_3$ are of special interest and offer several advantages. First, they can be MBE-grown lattice-matched to Si (or Ge) substrates with very low interface state density. Second, they can serve as a buffer layer for the growth of semiconductors, opening possibilities for integrating Si electronics and III-V optoelectronics. However, several issues concerning these materials remain to be fully addressed, among which band offsets with Si and other semiconductors.

In this work, we use a SrTiO$_3$ (100) /BaSnO$_3$ (11 1) /Si structure grown by MBE, and X-ray and UV photoemission spectroscopy to study core level and valence band states. Dependent on surface preparation, including ex situ UV-ozone, O$_2$ or H$_2$O treatments, the valence band minimum position shifts by more than 2 eV, whereas the effect is observed to be small on core levels. These data indicate that surface composition and morphology are of paramount importance in the UPS determination of electronic structure, and may explain discrepancies between results reported in the literature. An investigation of self- and stoichiometric SrTiO$_3$ surfaces indicates that its conduct band minimum is located 0.4 eV below the one of Si. An in-depth investigation of the role of surface preparation is being pursued, and results on BaTiO$_3$/SrTiO$_3$/Si samples will be reported. I. P. A. McKeel, F. J. Walker, and M. F. Chisholm, Phys. Rev. Lett. 256, 406 (2001)

11:30 AM E4.11
Abstract Withdrawn

11:45 AM E4.12
In situ Investigation of Me,O$_3$/Si (Me=Hf, Al, Yb) Interfaces with PLD-XPS. Andrei Zenkevich and Yuriie Lebedinski, Moscow Engineering Physics Institute, Moscow, Russian Federation.

SiO$_2$ as the gate dielectric material in Si-based CMOS technology is to be replaced eventually with a higher dielectric constant (high-k) material. Metal oxides would allow an increase in thickness in real products. At such thickness of overlayer x-ray photoelectron spectroscopy is a technique that allows to monitor simultaneously chemical bonding in the growing oxide film and metal oxide/silicon interface. Reactive pulsed laser deposition (PLD) by ablating metal in reduced oxygen atmosphere ($10^{-2}$-10$^{-7}$ Torr) allows to vary metal/oxygen concentration ratio in the film, deposition rate and substrate T as independent parameters and to control the growing layer thickness with submonolayer accuracy. To investigate the initial stages of high-k dielectric/Si interface formation and its evolution during annealing both in vacuum and in oxygen, reactive PLD combined with in situ XPS analysis is advantageous. We present computer-aided data on the chemical bonding at Me$_3$O$_3$/Si interface (Me=Hf, Al, Yb) during RT growth and further annealing in vacuum as well as in oxygen. Lateral- and layer-growth phases during reactive PLD is established with XPS and confirmed with ex situ AFM. During the growth of a Me$_3$O$_3$/Si film within monolayer only is observed at the interface. The thickness of SiO$_2$ interlayer as a function of annealing T is presented. The conversion of interfacial SiO$_2$ into metal silicate is found to depend on the regular Me$_3$O$_3$/Si system and oxygen concentration in metal oxide layer.

SESSION E5: Theory of Novel Oxide/Semiconductor Interfaces

Chairs: Peter Bledo and David Vanderbilt
Tuesday Afternoon, December 2, 2003
Room 207 (Hynes)

1:30 PM E5.1
Dielectric Permittivity of Atomic-layer Thick SiO$_2$ Films or Interlayers on Silicon Substrates. Feliciano Giordano, 1, 2, 3, Pohl, Umar 1, 2, and Alfredo Pugnaloni, 1, 2, 1 TTP [Institut des Theories des Phénomènes Physiques], EPFL [Ecole Polytechnique Federale de Lausanne], Lausanne, Switzerland; 2 IRMA [Institut pour Recherche Numerique sur les Matériaux], Lausanne, Switzerland.

To address the dielectric effect of a thin silicon interlayer between silicon and high-k oxides, we investigated the dielectric permittivities of atomic-layer thick SiO$_2$ films using a density functional approach. We constructed several model structures of the Si/SiO$_2$ interface with oxide thickness varying between 3 and 12 Å, and for each of them we calculated both the static and high-frequency permittivities. We found that in a classical three-layer model (including the silicon substrate, a 3 Å thick suboxide, and the pure SiO$_2$ oxide) reproduces to a high degree of accuracy the results obtained from first principles. This suggests that the evolution of the screening properties from Si to SiO$_2$ is rather abrupt, and essentially takes place within the suboxide region. To check the validity of this conclusion, we investigated the microscopic polarization induced at the interface by an external electric field. We found that the local polarization is approximately constant in the substrate and in the pure oxide, and that the transition essentially occurs within the suboxide. This result provides a truly microscopic justification for the classical three-layer model. Static and high-frequency permittivities of the suboxide layer were found to be significantly larger than the corresponding values of bulk SiO$_2$ (3.8 and 0.8 instead of 2.9 and 2.8, respectively). To interpret this enhanced screening, we analyzed the interface from a chemical point of view. Following the Berry-phase theory of polarization, we determined the maximally localized Wannier functions of the system, and noticed that with respect to the individual components, the enhanced screening of the suboxide layer must arise from the chemical grading. Similar conclusions hold for the ionic screening. Metal-induced gap states are shown to contribute to the polarization of the suboxide, but their role in enhancing the SiO$_2$ permittivity in proximity of the suboxide appears less prominent than previously suggested. The enhanced screening of the suboxide implies that the effect of a thin silicon interlayer between silicon and high-k dielectrics is less severe than expected on the basis of the bulk SiO$_2$ permittivity.

1:45 PM E5.2
Ab-initio study on the $\gamma$-Al$_2$O$_3$ surfaces and interfaces. Henry Paul Pinto and Simon David Elliott; Physics, NMRC, University College, Cork, Cork, Ireland.

The controlled growth of aluminium films by atomic layer deposition (ALD) is of great interest to the electronics industry, as high-k dielectrics are being sought for the next-generation MOSFETS [1]. Many aspects of the surface structure and reactivity of alumina are still unknown, but are amenable to computation. We present a theoretical study of the aluminium polymorph $\gamma$-Al$_2$O$_3$. The calculations are based on density functional theory (DFT). The predicted bulk structure for $\gamma$-Al$_2$O$_3$ has the Al$_4$ vacancy sites widely separated, which is in agreement with other theoretical predictions [2].$\gamma$-Al$_2$O$_3$ has been found to be a good candidate for the next generation of trench isolation layers. The energy of several several $\gamma$-Al$_2$O$_3$ surface (111), (110) and (150). The $\gamma$-Al$_2$O$_3$ surfaces (111) is compared and discussed with the $\alpha$-Al$_2$O$_3$(0001). The presence of H$_2$O within the (111) surface is studied and compared with the results when the water is inside the bulk. Besides, the interaction of a H$_2$O onto the (111) surface is considered. Finally, a model for $\gamma$-Al$_2$O$_3$(111)/AlOOH-like interface is proposed and the atomic structure and the ideal work of adhesion are computed. In addition, we study the hydrogen diffusion and the water influence within the interface and these results are discussed in light of available experimental data. References: [1] G.D. Wilk, R. M. Wallace, J. Anthony, J. Appl. Phys. 89, 2001 (2001); [2] C. Wohler, K. C. Hass, Phys. Rev. B 63, 204120 (2001). 2:00 PM E5.3
Lattice Dielectric Properties of ZrO$_2$ and HfO$_2$. David Vanderbull 1 and Xinyuan Zhu 2, 1 Physics and Astronomy, Rutgers University, Piscataway, New Jersey; 2 School of Physics, Georgia Institute of Technology, Atlanta, Georgia.

We have investigated the structural, electronic, and lattice dielectric properties of crystalline ZrO$_2$ and HfO$_2$. The calculations have been carried out within the local-density approximation using ultrasoft pseudopotentials and a plane-wave basis. Our calculations on cubic, tetragonal, monoclinic, and orthorhombic phases indicate the dependence of the lattice dielectric susceptibility and its anisotropy on the choice of crystal phase. For example, we find a large in-plane susceptibility for the tetragonal phase. Significant differences in the
The electronic density of states and band gaps are also reported. The calculated non-center phonon frequencies yield good agreement with infrared and Raman measurements. The Fermi level pinning and optical data are also reported. Preliminary results on a model of amorphous $\text{ZrO}_2$ generated via melt-quench first-principles molecular dynamics reveal a distribution of coordination numbers for both $\text{Zr}$ and $\text{O}$ atoms. Implications for potential high-k applications of these materials will be discussed.

2:30 PM E5.4 Theoretical Analysis of Oxygen Diffusion in Monoclinic $\text{HfO}_2$. Minoru Ikeda,1 Georg Kreise,2 Toshihide Nishime3 and Akira Toriumi.4,5 1MIRAI, Association of Super-Advanced Electronics Technologies(ASET), Tsukuba, Ibaraki, Japan; 2Institute for Materials Research, University of Tokyo, Sendai, Miyagi, Japan; 3MIRAI, Advanced Semiconductor Research Center(ASRC), National Institute of Advanced Industrial Science and Technologies(AIST), Tsukuba, Ibaraki, Japan; 4Department of Materials Science School of Engineering, University of Tokyo, Tokyo, Japan; 5University of Tokyo, Tokyo, Japan.

Recently, $\text{HfO}_2$ (hafnia) grown on $\text{Si}$ substrates is widely studied as a potential candidate for replacing silicon dioxide as the gate dielectric in scaled CMOS. At the interface between $\text{Si}$ and hafnia, the interfacial layer has been formed, and this layer thickness increases by the post deposition annealing [1]. This indicates that oxygen diffuses through hafnia. Foster et al. reported the interstitial oxygen diffusion in hafnia and concluded that the $O^{2-}$ diffuses in the bulk $\text{HfO}_2$ [2]. In this report, we present the detailed analysis of the interstitial oxygen ($O^{2-}$, $O^-$) diffusion in hafnia using the Projector Augmented Plane Wave method [3,4] with the Ultrasoft pseudopotential techniques. In the interstitial oxygen atom at the $3\times3\times3$-fold site and the $3\times3$-fold site. And the newly kicked-out interstitial oxygen atom jumps to the nearest neighbor site and couples again with the atom at the crystal sites. This kick-out is valid for the whole range of compositions of the interstitial oxygen in monoclinic $\text{HfO}_2$. The interstitial $O^{2-}$ forms a trimer with the two neighbor $3\times3\times3$-fold sites $O$ atoms. And the neutral interstitial $O^-$ forms the dimer coupled with the one nearest neighbor $3\times3\times3$-fold site. Contrary to these two cases, the $O^-$ forms new $3\times3$ fold site combining with an vacancy (V$^+$) defect pair. We can simulate such a pair annihilation process in hafnia. In the higher range of $E_F$, $O^-$ might contribute. And for the lower range of $E_F$, we think that the actual experimental situation satisfies this condition, the $O^{2-}$ only contributes to the diffusion process in hafnia. This work was supported by NEDO. References [1] T.Nishime, T.Yusuda, M.Nishizawa, M.Ikeda, T.Horikawa and A.Toriumi. Extended Abstracts of SSDM 2002, p.64. [2] A.S.Foster, A.I. Shuger, and R.M.Niemen. Phys.Rev.Lett. 89, 205001(2002) and A.S.Foster,E.L.Lopez Gejo, A.I. Shuger, and R.M.Niemen. Phys.Rev.B65,174117(2002). [3] G.Kresse and J. Hafner. Phys.Rev.B47,558(1993) and G.Kresse, T.U.W. Thies, (1993). [4] P.E. Blöchl and J. Phys. Condens. Matter 10, 139(1998). [5] D.Joubert, Phys.B59,1758(1998). [6] G.Henkelman and H. Joonson, J.C.P. Vol 113, 957B(2000).

2:45 PM E5.5 Bonding and Epitaxial Relationships at High-K Oxide/Si Interfaces. John Robertson and Paul W Pencock; Engineering, Cambridge University, Cambridge, United Kingdom.

High dielectric constant oxides are needed to replace silicon dioxide as the gate oxide in future CMOS devices. Also, functional oxides with ferroelectric, ferromagnetic, CMR, or superconducting properties are desired for future devices [1]. However, the interfaces between oxides and silicon are not easily described because of the change from ionic bonding in the oxide to covalent bonding in Si. We have studied the interfacial bonding at epitaxial interfaces of Si/\text{SiO}_2 and Si/\text{SiO}_3 with Si for a wide variety of orientations and terminations see in experiment [1-4], using total energy calculations. The results can be explained within simple rules. The key requirement is for the interface to be insulating and have no interface gap states. We show that the oxide face must actually be polar, to satisfy the Si dangling bonds. Both oxygen-last but metal-last are possible. The oxygen-last interfaces tend to be insulating, if our stoichiometry rules are followed, whereas the metal-last interfaces often have interface gap states. Oxygen-last interfaces are protected by saturating all the surface Si dangling bonds by oxygens, and then adding non-polar constructed surfaces for [100], [110] or [111] oxide. This gives a net oxygen-rich interface. For \text{SiO}_2, the bonding results follow the rules found by Yoshimato [3] for fluoride on Si systems such as Si/$\text{ZrO}_2$/[100], $\text{Si}$[100]$/\text{ZrO}_2$/[110] and the similar cases of [111] epitaxy in the bodycentered cubic [YLi]$_2$O$_3$ series. The band offsets are calculated for each case. For $\text{SiO}_2$/[100], the offset is found to be relatively independent of orientation and also close to the value determined from bulk charge neutrality level [5]. 1. R A McKenzie, F J Walker, M F Chisholm, Science 293 468 (2001) 2. V Narayanan et al, J Appl Phys 89 2521 (2001) 3. M Yoshimato, Jpn J Appl Phys 39 2521 (2000) 4. X Hu et al, App Phys Lett 82 258 (2003) 5. J Robertson, J Vac Sci Technol B 18 1785 (2000).

3:30 PM E5.6 High dielectric constant materials: a band line-up problem. Alex DeMikin1,2,3, Leonardo Raspena2, Otto F. Sankey2 and John Tomberlin2; Motorola, Inc., Austin, Texas; Motorola, Inc, Tempe, Arizona; Arizona State University, Tempe, Arizona.

To insure continuous downsizing of CMOS technology the semiconductor industry must make a transition from the Si-SiO$_2$-oxide complex. The higher thin silicon dioxide dielectric constant of the new gate dielectric will allow maintaining the gate capacitance and therefore the drain-source saturation current without the thickness reduction of the oxide. The integration of this new stack into the current CMOS flow is one of the most urgent tasks of today’s electronics. The oxide’s gate action, among other factors, depends on the barrier height (same as band discontinuity) at the oxide-semiconductor and oxide-metal interfaces. The band alignment is often estimated within the so-called metal-induced gap states (MIGS) model. The MIGS model describes both Burstein and Schottky limits and intergradeates between the two in a linear fashion, provided that electron affinities, charge neutralities and the pinning fact or are known. The theory was also successfully used to describe the band discontinuity in heterojunctions between covalent semiconductors. It is not obvious whether this approach should work for junctions between Si and high-k dielectrics. A consistent procedure to determine the charge neutrality level is also not clear. We use the complex band structure of several prospective gate dielectrics, SiO$_2$, Si/TiO$_2$/HfO$_2$, and AlO$_3$ to estimate their charge neutrality levels, and compute band offsets for each. Results of these model calculations are then compared to those obtained with direct experimental structure methods and available experiment. It appears that charge neutrality level thus obtained indeed provide a consistent picture. However, the uncertainty in the conduction band position inherent in the local density approximation may render the theory inadequate for the engineering support. Despite this limitation, linear scaling of the charge neutrality level with high-k band gaps has shown excellent agreement with experimental data.

3:45 PM E5.7 A View of Sr Adsorption on Si(001) from First Principles Calculations. Christopher R Ashman1, Clemens J Evert3,4,5, Karlheinz Schwartz3 and Peter E Blöchl1; 1Institute for Theoretical Physics, Clausthal-Zellerfeld, Germany; 2Institute for Materials Chemistry, Vienna University of Technology, Vienna, Austria.

The initial stages of metal deposition on silicon are critical to understanding the growth of high-K oxides on silicon with abrupt interfaces. We performed state-of-the-art electronic structure calculations and ab initio molecular dynamics simulations of the adsorption structures of Sr on Si(001). The atomic and electronic structures and the energetics depending on the Sr-coverage will be discussed and compared with existing experimental information. The adsorption can be explained by a series of structural motifs which derive from the chemical binding.

4:00 PM E5.8 Ab-initio Simulations on Initial Growth Steps of High-K Oxides on Silicon: SrTiO$_3$/Si(001). Peter E Blöchl1, Christopher R Ashman1, Clemens J Evert3,4,5 and Karlheinz Schwartz3; 1Institute for Theoretical Physics, Clausthal-Zellerfeld, Germany; 2Institute for Materials Chemistry, Vienna University of Technology, Vienna, Austria.

State-of-the-art electronic structure calculations and ab initio molecular dynamics simulations have been performed to investigate the growth of SrTiO$_3$ on Si(001). I will briefly touch on the adsorption of Sr on Si(001). Then, I will explain the formation of the first SrO layers on silicon and describe the atomic and electronic structure of the SrTiO$_3$/Si(001) interface. The structural changes upon variation of the oxidation partial pressure have been investigated. Based on these results, a method to engineer the band offsets in order to obtain an acceptable injection barrier will be proposed.

4:30 PM E5.9 Structure and dielectric properties of the high-k oxides Co$_2$O$_3$ and MgAl$_2$O$_4$. Gianluca Gulli and Giancarlo Finocchio; Dipartimento di Fisica, University of Cagliari, Monserrato, Italy; 3DMD-INFM Lab, Agrate, Italy.

We study the structural stability, effective charges, and ionic dielectric
445 PM E5.10
First-Principles Study of the LaAlO$_3$(001)/Si(001) Interface.
A. Kudinov,$^1$ I. Isaksson,$^2$ B. Englund,$^3$ B. Potapkin,$^2$ L. R. C. Freas,$^1$ A. Kaikka,$^1$ Motorola Inc. Templo, Arizona; $^2$Kistekh Technologies Ltd, Moscow, Russian Federation.

LaAlO$_3$ has been considered as a possible high dielectric constant candidate for the next generation of MOSFET devices but very little is known about its electronic properties. We perform first-principles calculations of its bulk and surface properties, and studied the LaAlO$_3$(001)/Si(001) interface structure. We calculated a dielectric constant of ~30 for crystalline LaAlO$_3$, which is similar to hexagonal LaAlO$_3$, and is in good agreement with experimental data. In the case of LaAlO$_3$(001) slabs, a net nonzero dipole moment arises as a result of non-similar surfaces. This problem was addressed and several ways of eliminating the net dipole moment are presented. We show that the migration of an oxygen anion is a favorable technique for compensating the LaAlO$_3$(001) surface dipole. The model structures of LaAlO$_3$(001) surfaces with compensated dipole moments were used to study LaAlO$_3$(001)/Si(001) interface properties. We investigated the stability of these interfaces and found that lanthanum-terminated LaAlO$_3$(001) cases are in general more stable than aluminum-terminated cases for both the oxidized and unoxidized Si(001) surfaces. Using density-functional techniques we found that the O/Si interface result in a significant reduction of the LaAlO$_3$(001)/Si(001) valence band offset due to the creation of interface dipoles. The analysis of the interface states density showed that dipoles bonding forming at the LaAlO$_3$/Si(001) interface do not create interface states in the silicon band gap, in contrast with Zr(Hf)/Si bonds studied previously in m-Zr(Hf)O$_2$/Si(001) model systems.

SESSION E6 Poster Session: Fundamentals of Novel Oxide Semiconductor Interfaces II
Chair: Dorell Schom and Susanne Steemer
Tuesday evening, December 2, 2003
8:00 PM
Exhibition Hall D (Hyne's)

E6.1 p-type in Zn$_x$O$_{1-x}$N by codoping with Cr.
Elisa Kaminska,$^1$ Anna Piotrowska,$^2$ Jaroslaw Kozak,$^2$ Renata Barlute,$^2$ Wioleta Dobrowolska,$^2$ Ewa Bochenk,$^2$ Adam Golub,$^2$ Elzbieta Dynowska,$^2$ Rafał Jakelski$^2$ and Dorota Wawer$^2$.

1. Institute of Electronic Technology, Warsaw, Poland; 2. Institute of Physics, PAS, Warsaw, Poland.

There is a growing interest in the use of transparent-oxide electronics with the potential advantages of invisble electronic circuits, high-temperature performance and radiation hardness. The majority of transparent conducting oxides (TCOs), however, are n-type semiconductors. Despite the considerable amount of work on the growth of p-type TCOs, relatively few results have been reported. As for ZnO, it is commonly accepted that fabrication of p-type material is a formidable technological challenge if possible at all [1]. With this fact in mind we have attempted to fabricate ZnO with p-type conductivity by oxidation of nitrogen-doped zinc metallic films and zinc nitride films. The starting materials were grown either by magnetron sputtering or by molecular beam epitaxy. Quarts, sapphire and thin GaN films on sapphire were used as substrates. We present results of secondary ion mass spectrometry and x-ray diffraction analysis of the oxidized layers, which indicate that formation of ZnO does take place. The layers of ZnO obtained by oxidation of metallic Zn so far were always found to be either highly resistive or showed n-type conduction. In contrast to that, oxidized layers obtained from zinc nitride were found to be p-type (the carrier concentration $\sim 10^{18}$ cm$^{-3}$ and mobility $\sim 5$ cm$^2$/Vs at room temperature) when the starting material before oxidation was additionally doped with Cr. The transparency of 82% thick ZnO:N films in the whole visible wavelength spectrum reached 80%. The energy gap as inferred from transmission measurements, was 3.27 eV. Work supported by grant from the European Commission NANOPHO (contract IST-2001-39121) within the 5th Framework Programme and by grant from the State Committee for Scientific Research PBZ-KBN-04/P03/2001. [1] S.B. Zhang, S.H. Wei, and A. Zunger, Phys. Rev. B 63, 072420R (2001).

E6.2 Microstructure and Electrical Properties of Zinc Oxide Thin Film Varistors Prepared by RF Sputtering.
Kangming Chiang$^1$, Chaung-pu Liu$^2$, and Ching-ming Tsai$^2$.
1. Department of Materin Science and Engineering, National Cheng Kung University, Tainan, Taiwan; 2.Beslon Technology Corporation, Taipei, Taiwan.

The thin film varistors of ZnO-Bi$_2$O$_3$ multilayer junctions were fabricated by RF sputtering. The nonlinear I-V characteristics and nonlinear coefficient a, under the reverse bias were examined and they were affected by composition and structure of the multilayer varistors. The threshold voltage can be adjusted by altering the donor density in ZnO, which was achieved by varying doping concentration Bi and sputtering conditions. In addition the structure and thickness of Bi$_2$O$_3$ layer in thin film varistors determine the threshold voltage. The higher leakage current and lower nonlinear coefficient associated with the ZnO films doped with Al (ZnO:Al) can be improved by inserting another ZnO layer doped with selective transparent metal interlayer in mid-varistor. The formation mechanism of the varistor is also investigated in detail and related to the performance of the electrical properties. The interface states in the ZnO films were examined by electron energy-loss spectroscopy (EELS) in a transmission mode, using scanning electron microscopy. The EELS data along with the doping concentration by Hall measurement were also used to explain the electrical properties.

E6.3 Properties of ZnO and Aluminium doped ZnO thin films grown by pulsed electron deposition.
1. Center for Superconductivity Research, University of Maryland, College Park, Maryland; 2. Nocera Inc, Belmont, Maryland.

The technique of pulsed electron deposition (PED), which is based on channel spark discharge and magnetically-confined pulsed electron beam, is applied to grow thin films of ZnO with and without Al doping on c-Al$_2$O$_3$ and Si (001). The films are deposited at a discharge pulse voltage of 15 kV, repetition rate of 5 Hz, and background pressure of 60 mTorr of forming gas (95% Ar + 5% H$_2$). The film properties are investigated by various techniques such as Rutherford back scattering, ion channeling, x-ray diffraction, UV spectroscopy, atomic force microscopy, and four probe resistivity measurement. These films are p-type oriented, electrically conducting, and optically transparent with transmittance close to 75% in the visible and IR region of the spectrum. The band gap is 3.4 eV. The transparence of these films will be examined using a broad range of pulse laser deposited films. The structural, transport and optical properties of these films will be discussed in details. Work Supported by Maryland Industrial Partnership (MIP) program.

E6.4 Electronic Structure of Zn$_x$Mn$_{1-x}$O - A Resonant Photoemission Study.
Florinda Gubelj,$^1$ Rok Fajfar,$^2$ Blaž Jakopin,$^2$ Martin Sadowski,$^2$ M. Erce Gubelj,$^1$ and Zigahelm Golobic.$^2$
1. M grille, LOs Alamios National Laboratory, Los Alamos, New Mexico; 2. Institute of Physics, Polish Academy of Sciences, Warsaw, Poland; 3. Niess Bator Institute (FUG), Grazed Laboratory, University of Copenhagen, Copenhangen, Denmark; 4. MAX-lab, Lund University, Lund, Sweden; 5. Institute of Electronics Technology, Warsaw, Poland.

Ferromagnetic properties of ZnO with 3d transition-metal impurities have been widely investigated in the past. Expecially, incorporation of Mn into semiconductor ZnO attracts considerable attention because an antiferromagnetic ordering in n-Zn$_x$Mn$_{1-x}$O and a ferromagnetic ordering in p-Zn$_x$Mn$_{1-x}$O at room temperature has been predicted. In addition, a high solubility of Mn is Mn$_x$O$_{2x}$ has been confirmed. These features make Zn$_x$Mn$_{1-x}$O a good material for transparent magnets and for new applications in spintronics. We have investigated an electronic structure of Zn$_x$Mn$_{1-x}$O surface alloy by means of resonant photoemission spectroscopy. Four of manganese monolayers were deposited on Zn(001) single crystal and next Mn$_x$O$_{2x}$ system was annealed up to 5000°C. The scanning Auger measurements taken after annealing show no metallic film and confirm the Zn$_x$Mn$_{1-x}$O surface alloy of 20 Angstroms thickness has been created. Resonant photoemission spectra near the MnSpin-MnSpin absorption edge taken before and after annealing show resonant enhancement of Mn3d states within 1.0 eV of the Fermi edge. An experimentally obtained Mn3d partial density of states change surprisingly in a resolved manner. The relative intensity of satellite/minor ratio decrease after annealing from 0.89 to 0.43 giving evidence of higher degree of hybridization between the Mn3d states and the ZnO valence band. The comparison
with previous resonant photocurrent results show that the hybridization effect in ZnMnO surface alloy is similar to that in ZnMnSe and the band gap decreases with the oxidation of Mn to ZnMnTe. We have also measured photocurrent from the Mn3p core level. Photoemission spectra show two Mn3d components separated by about 4 eV. The relative intensity of these two components is different before and after annealing. These results imply the coexistence of a metallic surface on a nonmetallic bulk. Understanding the coupling between various degrees of freedom on surfaces and interfaces is required to create materials with the desired transport properties necessary for the next generation of electronic devices.

**E.6.5** Fabrication of SrRuO$_x$ Epitaxial Thin Films on YBa$_2$Cu$_3$O$_y$ / CeO$_2$ / YSZ-buffered Si Substrates by Pulsed Laser Deposition. Takamitsu Higashi, Koki Mochizuki, Setsuya Inawashita, Masaya Ishida and Tatsuya Shishido, Technology Finance Research Center, SEIKO EPSON CORPORATION, Fujimi-machi, Nagaokakyo, Japan.

Much attention has been paid to SrRuO$_x$ epitaxial thin film electronics, because of its high electrical and magnetic properties of perovskite-type ferroelectric or piezoelectric oxides on the SrRuO$_x$ epitaxial thin film electronics would bring about an increase in resistivity or piezoelectric constant. However, it is quite difficult to fabricate SrRuO$_x$ epitaxial thin films directly on Si substrates due to the formation of a SiO$_2$ layer on the Si substrate. Therefore, metal oxides-buffered Si should be used as substrates. In general, however, the epitaxial growth of such metal oxides on Si has been realized at a low oxygen partial pressure ($P_{O_2}$) and a high substrate temperature ($T_s$), where the SiO$_2$ layer on Si is easily removed. In the present study, epitaxial growth of yttria-stabilized-zirconia (YSZ) buffer layer on a Si (100) substrate was demonstrated at a relatively high $P_{O_2}$ and a metal-organic chemical vapor-deposited (MOCVD) SrRuO$_x$ (100) epitaxial thin film was fabricated on a YBa$_2$Cu$_3$O$_y$ / CeO$_2$ / YSZ-buffered Si substrate by PLD. Reflected high energy electron diffraction (RHEED) observation of the YSZ and the SiO$_2$ layers with the thickness of 5 nm epitaxially grown on a naturally oxidized Si substrate with the process conditions of a relatively high $P_{O_2}$ ($P_{O_2}$ = 5 x $10^{-6}$ Torr) and a relatively low $T_s$ ($T_s$ = 700 °C) compared to previously reported data, and that an orientation relationship of YSZ (100) / Si (100) and YSZ / SiO$_2$ (100) / Si (100) was established. Accounting for the Gibbs free energy change, the vapor pressure of SiO$_2$ and the growth rate for the thermally oxidized SiO$_2$ on the Si substrate surface, it is suggested that the epitaxial growth of YSZ on the metal-oxidized Si is caused by the oxidation of SiO$_2$ on Si by Zr with a rate larger than the growth rate of SiO$_2$, and by evaporation of Si as SiO. The second deposition of the CeO$_2$ buffer layer with the thickness of 10 nm resulted in an orientation relationship of CeO$_2$ (110) / Si (110) and CeO$_2$ (101) / Si (110). The third deposition of the YBa$_2$Cu$_3$O$_y$ buffer layer with the thickness of several nm played an important role to bring about a (100) orientation of a perovskite-type cubic unit cell. The last deposition of SrRuO$_x$ resulted in a pseudomorphic (100) epitaxial thin film, exhibiting an orientation relationship of SrRuO$_x$ (100) / Si (100) and SrRuO$_x$ (110) / Si (110). This result shows that the SrRuO$_x$ epitaxial thin film on the YSZ-buffered Si substrate is promising for high performance electronic devices.


Strong coupling between electronic, ionic, orbital and spin degrees of freedom in transition metal oxides has attracted significant interest in exploiting their immense potential for oxide electronic devices with novel functionalities. Understanding the fundamental physics of reduced dimensionality involved in surface/interface properties is vital for the realization of such devices. Here we investigate the surface electronic structure of the layered perovskite Ca$_{1-x}$ Sr$_x$ Ru$_2$O$_7$. First-principles calculations and optical spectroscopy were used to determine the electronic structure and magnetic properties of these surfaces studied by temperaturedependent scanning tunneling microscopy (STM), scanning tunneling spectroscopy (STS), and low-energy electron diffraction (LEED) measurements.

**E.6.7** Elementary Processes during the Epitaxial Growth of Oxides: the Case of MgO. Gregory Geneste$^1$, Joseph Merzillo$^2$, Fabio Finocchi$^3$ and Marc Houyoux$^4$. 1 CEMES, CNRS, TOULOUSE, France; 2 GIPS, University Paris 67 and CNRS, PARIS, France; 3 LSU/CREAM/DSM, CEA, PALAISEAU, France.

Metal oxides are nowadays used in many applications (microelectronics, magnetic devices, etc.) They may appear as epitaxially grown thin films on various substrates, substrates, or both of them. Due to the intense and rapidly varying microscopic electric field, their electronic properties are very sensitive to the atomic structure, such as the surface flatness and to the detail of the interfaces with other materials. The understanding of the basic mechanisms (adsorption, diffusion, etc.) that govern the epitaxial growth is therefore important for technological applications. We focus on oxide on oxide growth studied by means of first-principles and empirical simulations. We performed an overall study of the elementary processes in MgO growth by Pulsed Laser Deposition (PLD), considering three different epitaxial growth conditions of the MgO (001) surface [1], as considered as deposited species atoms (MgO) or small molecules ([O$_2$, MgO, MgO$_2$]) that may occur in multistep plasma epitaxy or sputtering. We show that the electronic and atomic structures play a crucial role in determining the energy landscape that is seen by the diffusing species, diffusion close to atomic steps can be qualitatively and quantitatively different from that on flat terraces whereas onto the flat surface the diffusing species are the Mg adatoms and MgO admolecules, the situation is reversed along the [001] step, the mobile species being now the O adatoms. Also we show that there is no Schoeder barrier across the [001] step, which favors 2D growth. Moreover, the study of various charge-transfer reactions between the ad-molecules and/or the ad atoms reveals that the actual surface stoichiometry results from a subtle interplay between their reactivity and diffusional behaviour. For example, the O atom sticks to the surface forming another O$_2$ molecule, while the Mg adatom leaves the surface forming a very stable peroxide bond. The Mg + O$_2$ → MgO reaction at the surface must then proceed with a strong local rearrangement. We show that this reaction (including change transfer) occurs at very short distances but without any extra barrier thus that for Mg diffusion. The computed core-level shifts of the adspecies can be compared to the outcome of X-ray photoemission spectra taken during the growth, thus permitting the identification of the adspecies on the samples. The nature of adsorption and the nature and structure of the adclusters are also studied. Finally, we outline a possible scenario for large-scale homo-epitaxy and compare our simulations to available experimental data with particular emphasis on the growth of Sr$_2$CuO$_2$Cl$_2$ on the Cu$_2$O(111) surface. In addition, the reactions of the adspecies are also studied.

**E.6.8** Optical, Electronic and Interface Studies of ZrO$_2$ and HfO$_2$ Thin Films on Si and Amorphous SiO$_2$. Ciro M Lopez$^1$, N A Suvorova$^2$, C 2 A 2 Suvorova$^3$, A A M Saunders$^4$, and E A Irene$^5$. Chemistry, University of North Carolina-Chapel Hill, Chapel Hill, North Carolina, 2Centre for Microelectronic Materials and Devices, University of Western Australia, Crawley, Western Australia, Australia.

Zirconia, ZrO$_2$, and hafnium, HfO$_2$, thin films were grown on single crystal MgO (100), Si (100), and amorphous SiO$_2$ substrates by double-sided deposition of the parent metal and subsequent oxidation at various temperatures. The optical properties for the ZrO$_2$ and HfO$_2$ films as well as the spater-deposited metals were determined by in situ spectroscopic ellipsometry (SE) and electron diffraction (LEED). It is found that the bond angle between the SrRuO$_x$ surface oxygen in the rotation of RuO$_x$ octahedron relative to bulk perovskite structure is enhanced by reduced oxygen bond length and shifting the surface phonon energies. The substitution of Sr ions in Ca$_{1-x}$Ru$_2$O$_7$ crystals results in a rotation plus a tilt of the RuO$_x$ octahedra creating a Mottni-insulator phase. Particulate Sr$_x$Ru$_2$O$_y$ exhibits a metal to Mott-insulator transition below ~15K in bulk single crystals; however, with STS and High Resolution Electron Energy Loss Spectroscopy (HREELS), we observe a metal to Mott-insulator transition at the surface of single crystal Sr$_x$Ru$_2$O$_y$, below ~120K, surprisingly lower than the transition temperature in the bulk. The lowering of transition temperature is intimately related to different lattice distortions at the surface, indicating a strong electron-phonon coupling in addition to electron-electron correlations. These results imply the coexistence of a metallic surface on a nonmetallic bulk. Understanding the coupling between various degrees of freedom on surfaces and interfaces is required to create materials with the desired transport properties necessary for the next generation of electronic devices.
pure dielectric layer. The growth dynamics for these layers was
determined. Electrical measurements were performed on fabricated
Pt/ZrO2/ITO/Si capacitors prepared in situ, in order to determine the
fixed charge and dielectric constant for the overall film stack.
Interface trap state density ($D_{it}$) was determined via the conductance
method. Variation of $D_{it}$ with various annealing procedures (via
post-oxidation and post-metallization anneals) was also studied.

**E6.0**
Precise Characterization of Silicon on Insulator (SOI) and
Strained Si on Insulator (SIO) Stack with Spectroscopic
Ellipsometry. Limching Sun1, 2, C.J. Forster1, C. Defranoux3, J.L. Steinhilber2 and H.J. Hovel1, 2
1SOPRA SA, Bois Colombes, Paris, France; 2T. J.
Watson Research Center, IBM Corp., Yorktown Heights, New York.

Further improvements in CMOS circuit performance such as switching
speed and power reduction will rely on the use of silicon on insulator
(SOI) substrates. The thickness of the silicon layer is a
fundamental parameter. According to the International Technology Roadmap
for Semiconductors (ITRS), the silicon and buried SiO2 (BOX) layer
thicknesses for a fully depleted device should be in the range of 10 to
16 nm and 2 to 4 nm by 2006, respectively. A key issue for
fully-depleted CMOS transistors is control of such ultrathin layer
thicknesses and their uniformity along with other parameters such as
surface and interface roughness. This poses a challenge to metrology
because the layer thicknesses must be determined with angstrom
precision. Spectroscopic ellipsometry (SE) is an optical and
non-destructive technique for determining thin film thickness and
material optical properties. Because ellipsometry measures the change
in the polarization state of light as a function of the amplitude of p to
s polarizations, and in the phase retardation, it provides a precise way
to characterize such ultrathin SOI stacks. Comprehensive
characterization results for a number of thin and ultrathin SOI stacks
with different device structures will be presented together with
measurement repeatability results relevant to the film thickness
process tolerances. In addition, characterization results for advanced
device applications such as strained silicon-on-insulator (SSOI) will also be shown, demonstrating the use and capability of
spectroscopic ellipsometry for precise determination of layer thickness,
material composition, interfacial layers, etc. Principles and advantages
of the technique will also be discussed in the presentation.

**E6.10**
AlN Thin Films Formed by ECR Plasma Oxidation for
High-k Gate Insulator Application. Go Yamazaki, Tokuharu
Uchikawa, Shun-ichiro Ohtani and Tetsutaro Saito. Department
of Information Processing, Interdisciplinary Graduate School of
Science and Engineering, Tokyo Institute of Technology, Yokohama,
Kanagawa, Japan.

AlN thin films formed by the electron cyclotron resonance (ECR)
plasma oxidation of the AlN layer deposited on Si(100) by ECR
sputtering and magnetron sputtering methods will be presented with
application. AlN films (3.4 nm) were deposited on p/p+ Si(100) by
ECR sputtering at room temperature, and then the deposited AlN
films were oxidized by Ar/O2 ECR plasma for 15-120 s to form AlON
films after an annealing process at 600-1000 °C for 1 minute. Rapid thermal annealing (RTA) was performed for 1 min 400-1000 °C
in flowing N2 ambient. Finally Al/AlN/TiN was deposited as a top
electrode. It is well known that Al2O3 deposited on Si usually shows
fine-structure of valence band due to the existence of the negative fixed
charge, while the AlON thin films show the excellent electrical
characteristics with negligible fixed-band voltage shift. The leakage
current density was found to be decreased with the ECR plasma
oxidation. The equivalent oxide thickness (EOT) of 1.6 nm with the
leakage current of 1.1 x 10^-3 A/cm² was obtained for the film after
120 s ECR plasma oxidation. The surface roughness was also
improved from 0.3 nm (15 s oxidation) to 0.16 nm (120 s oxidation)
with ECR plasma oxidation. Next, the effect of post-deposition
annealing on the leakage current was studied. The leakage current
was found to be decreased without increase of EOT after the 1000 °C RTA, while the leakage current was increased after the 400 °C RTA. The negative fixed-band voltage shift was observed at 750 °C and was kept even after 1000 °C RTA. From the XPS measurement, the SiO2 peak at the interface was found to be weaker after 400 °C RTA, while the peak became strong after 1000 °C RTA probably because of the interfacial layer formation such as Al2O3 with relatively higher
dielectric constant compared to that of SiO2. It was found that the
surface and the interface after 400 °C RTA became rough compared to
the film without the RTA process, while those became smooth, the
interfacial layer formation was clearly observed after 1000 °C RTA with
relatively higher dielectric constant compared to that of SiO2. It was found that the excellent
uniformity of the film led to lower leakage current density without
increase of EOT. EOT of 2.0 nm with the leakage current of 7 x 10^-5
A/cm² was obtained for the AlON film formed by the 120 s ECR
plasma oxidation with 1000 °C RTA.

**E6.11**
AtOMIC simulations of the dynamics of amorphous
semiconductors. Sebastian von Althoff, Antti Kurasen and Kimmo
Kaski. Laboratory of Computational Engineering, Helsinki University
of Technology, Espoo, Finland.

We have developed computational methods to study crystallization
and phase separation in amorphous solids on atomic level. The basic
simulation technique is a Monte Carlo (MC) method originally
developed by Wooten, Wiener and Weaire (WWW). In the WWW
method the structure of the material is described by the topology of
the bonds connecting the atoms. The system is allowed to evolve by
dynamical moves that change the bond topology. Using this method we are able to directly model the development of the
structure of the material. We have improved the WWW method by
deriving an algorithm that allows simulation of the NPT ensemble
counter to previous versions which were limited to the NVT ensemble.
Various computational optimizations which speed up the simulations
significantly are also implemented. These methods are used to
study the formation of silicon nanocrystals in SOI. This problem has
practical applications since it offers possibility for creating active light emitting devices made of silicon is based on small clusters of crystalline silicon embedded in amorphous SiO2. We have also used it to study the structure and dynamics of twist grain boundaries and amorphous clusters embedded in a crystalline lattice.

**E6.12**
Substrate/Oxide Interface Interaction In LaAlO3/Si:
Structural, Roderick A. De Groot1, 2, Tassos V. Kuzmenko3,
Joseph Fourier, Grenoble, France; 3Air Force Research Laboratory,
Kirtland Air Force Base, Albuquerque, New Mexico.

Amorphous lanthanum aluminate films (LaAlO3) were deposited on
Si(100) and Si(111) substrates at room temperature using Rf
sputtering in pure Ar or an Ar/O2 mixture with an stoichiometric target.
The film composition was analyzed using XPS and EDX. Samples were annealed either in a tube furnace or in rapid thermal system at 900, 950 and 1000 °C for between 1 to 10 minutes. The annealed atmosphere was N2, N2:H2 or O2. Typical thicknesses of deposited samples were of the order of 155 nm after sputtering for 120 minutes reducing to 130 nm following an anneal at 950 °C for 1 min. The refractive index at 632.8 nm increased from 1.7 (as-deposited) to 2.1 after annealing at 1000 °C for 1 minute. FTIR analysis showed only one peak centered at 747 cm⁻¹ with a FWHM of 185 cm⁻¹ for the annealed samples indicating that oxygen diffusion in the LaAlO3 structure is limited. Following short time annealing at 1000 °C a broad band at 905 cm⁻¹ appeared indicating the formation of a layer ~14 nm thick rich in
Si-O-La bonds. Nitrification of the substrate before oxide deposition
only allowed the formation of the layer, it did not suppress it. X-ray
diffraction analysis of the films indicated the existence of an amorphous
crystalline structure, yet unidentified, whose direction depends upon the
orientation of the Si substrate. The dielectric constant in both the
annealed and as-deposited films was measured to be less than 14, the
leakage current density was measured to be less than 10^-11 A/cm².
Some metallic-like behavior was detected. This dielectric constant is substantially less than the value ~ 25 anticipated from bulk single crystal measurements. Reasons for
this discrepancy will be discussed.

**E6.13**
Al Surface Segregation in Atomic Layer Deposited
ZrO2/Al2O3/Si(100) stacks. Giampaolo Sciacca1, 2, Sandro Ferrari1,
Mirella Fondelli1, Vieri Lebedevski1, 2 and Andrey Zenkevich1, 2
1Materials, Laboratorio MDM-INFM, Agrigento, Brinni, Milano, Italy;
2Moscow Engineering Physics Institute, Moscow, Russian Federation.

Aluminum surface segregation in the Al2O3 film form and monolayer
thickness through the ZrO2 layer (~200 nm thick) is observed to occur in
atomic layer deposited (ALD) ZrO2/Al2O3/Si(100) stacks grown on H
terminated Si(100) substrates at 300°C. The stacks are of interest as
substrates of SiO2 in dielectric gates for CMOS devices. The ZrO2
layers were grown using CrCl3 and H2O as precursors on top of an
Al2O3 buffer layer, several monolayers thick, grown from Al(CH3)3
and H2O. Aluminum surface segregation is observed while profiling
the Al depth distribution with x-ray photoelectron spectroscopy (XPS)
and time of flight secondary ion mass spectrometry (ToF-SIMS).
Unlike established Si diffusion to the surface through a metal oxide layer, further annealing up to 1000°C does not change the Al distribution found in the film. Similarly, morphologies of the ALD
layers with similar thickness grown on Si(100) with reactive pulsed
laser deposition (PLD) technique and annealed in oxygen at 850°C do not exhibit any Al at the surface. To explain the aluminum segregation at the surface a density functional model based on a stoke-effect of Al atoms during the exchange reactions.
E6.14 Structural and electrical properties of HfO2 films grown by atomic layer deposition on Si, Ge, GaAs, and GaN.

| Macro Facciolli, Giovanni Scarel, Sabina Spiga, Grazia Tallarida and Claudio Wiemer, Laboratorio MDM, INFN, Agraniti Brianza (MI), Italy |

The scaling down of modern micro-electronic devices, based on a MOS structure, has motivated an intense activity on high-k dielectrics [1]. Although a large number of materials have been investigated, suitable candidates have not been identified yet. A possible intrinsic problem could be also related to the reduction of the effective electron mobility in the inversion layer of the Si substrate due to remote phonon scattering [2]. Having sacrificed SiO2, the possibility of using different substrates, with a higher carrier mobility, does not look too exotic. Indeed some preliminary work has been already reported on growth and characterization of different materials like Ge [3], GaAs [4], and GaN [5]. In this work we report on the structural and electrical characterization of HfO2 films grown by atomic layer deposition (ALD) on Si, Ge, GaAs, and GaN substrates. The HfO2 films were grown at 375 °C using a novel precursor scheme where Hf(OH)4 and Hf(OR)4 (R = mp)  were used as metal and oxygen sources respectively. Due to their low oxidizing power, alkoxides, used as oxygen sources, should assure the reduction of the SiO2 interlayer film [6], typical of the ALD growth with H2O [7] or O3. Spectral X-ray reflectivity reveals similar properties such as surface and interface roughness, thickness, and electronic density on all the samples. The surface morphology has been also investigated by atomic force microscopy. Grazing incidence X-ray diffraction shows that, irrespective of the substrate, the films are polycrystalline with a strong monoclinic component. This result is also confirmed by far infrared reflectance spectrum. The presence of interface states of HfO2, as well as the presence of surface will be discussed. Good quality MIS capacitors incorporating HfO2 films were successfully fabricated on the different substrates. The diode present density and leakage current were determined for the HfO2 films grown on Si, as reference sample, and on Ge, GaAs, and GaN. The results indicate that the properties of the HfO2 films grown by ALD on alternative substrates are promising for applications in high speed devices, though more work needs to be done on the optimization of the interface properties [1] G. D. Wilk, R. M. Wallace and J. M. Anthony, J. Appl. Phys. 89, 5243 (2001), [2] M. V. Fischetti, D. A. Neuman, and E. A. Carter, J. Appl. Phys. 90, 3587 (2001), [3] C. O. Chu et al., IEEE Elec. Device Lett. 23, 472 (2002), [4] D. J. Pu et al., Appl. Phys. Lett. 80, 446 (2002), [5] Ager et al., Science 303, 219 (2004). [7] G. Scarel, C. Wiemer, S. Ferrari, G. Tallarida, and M. Facciolli, to be published in the Proceedings of the Estonian Academy of Sciences.

E6.15 Silicate interface formation during the deposition of Y2O3 on Si by PE-MOCVD. Christophe Durand1, Christophe Vallee2, Catherine Daubourdieu2,1, Marceline Bonvalot, Olivier Jobez2 and Eric Gausthers1,1LMIC-CNRS, Grenoble, France; 2LMIC, UMR-CNRS, Grenoble, France; 3LMIC-CNRS, Grenoble, France; 4LMIC-CNRS, Grenoble, France.

The control of the interface during the deposition process of a high-k material is a key issue for any potential application in high-k based devices. The challenge is not only to limit the interface formation but also to understand its formation in view of its growth rates, thickness and composition. In the case of many high-k materials the silicate appears to be more stable with silicon than with the oxide. Zirconium and hafnium silicates have been demonstrated as potential high-k gate dielectrics with an amorphous microstructure after annealing. Yttrium silicate also possesses desirable properties. Previous studies have shown the formation of yttrium silicate by the oxidation of yttrium on silicon in dry air at 500-700°C. This work is focused on the yttrium silicate formation during the deposition by plasma enhanced metalorganic chemical vapor deposition (PE-MOCVD) of Y2O3 on Si and Si/SiO2 substrates. Y2O3 films are obtained by a MOCVD process, which combines plasma assistance and a pulsed liquid precursor supply set-up. Plasma assistance enables the lowering of the deposition temperature. The liquid supply system used is based on the sequential injection of micro-amounts of precursors inside an evaporator. The precursor V[J/m produces] is dissolved in an azeotrope (cyclohexane) and is maintained at room temperature in a closed vessel under a 2 bar inert atmosphere [N2]. The yttrium silicate formation was studied as a function of the injection frequency and reagent concentrations. It is shown that the silicate formation can be limited by increasing the injection frequency and based on X-ray photoelectron Spectroscopy analysis performed at different take-off angles as well as Transmission Electron Microscopy and Electron Energy Loss Spectroscopy analyses. The first stages of the growth are determined by the injection frequency. The growth of the amorphous or crystalline SiO2 bonding environments in the grown material and at the interface was also carried out using absorbance Temperature Attenuated Total Reflection (ATR) spectroscopy in p-polarization. The O2 plasma influence on the silicate formation will also be discussed.

E6.16 Atomic Layer Deposition of HfO2/Al2O3 and ZrO2/Al2O3 Films for Gate Dielectric Applications. Jeehyung Ko and Hyeongjae Jeon, Division of Materials Science and Engineering, Hanyang University, Seoul, South Korea.

The high dielectric materials of Al2O3, HfO2-based oxide films, and ZrO2-based oxide films have been widely investigated mainly due to their large band gap, good thermal stability, and relatively higher dielectric constant compared to SiO2. In this study, we investigated the composition characteristics of HfO2/Al2O3 and ZrO2/Al2O3 films as well as their physical, chemical and electrical properties for gate dielectric applications. HfO2/Al2O3 and ZrO2/Al2O3 films were successfully deposited by atomic layer deposition (ALD) method using trimethylaluminum (TMA) and ZrCl4 in Aluminum, Hafnium and Zirconium precursors, respectively. The electrical properties including equivalent oxide thickness, hysteresis, leakage current and dielectric constant were calculated and analyzed by using capacitance-voltage (CV) and current density-voltage (J-V) measurements. For the evaluation of the physical and chemical characteristics of HfO2/Al2O3 and ZrO2/Al2O3, these films were analyzed by cross-sectional transmission electron microscope (XTEM), Auger electron spectroscopy (AES), Medium energy ion scattering spectroscopy (MEIS) and X-ray photoelectron spectroscopy (XPS). In these results, the amount of carbon impurity of Al2O3, HfO2, ZrO2, HfO2/Al2O3 and ZrO2/Al2O3 films deposited by ALD were below 3 x 1018 cm⁻³. Films showed good adhesion without having an interfacial layer. However, HfO2 and ZrO2 films showed highly oriented polycrystalline structure. This paper will discuss the systematic analysis of HfO2/Al2O3 and ZrO2/Al2O3 films deposited by ALD method for gate dielectric applications.


As the gate oxide thickness of metal-oxide-semiconductor (MOS) devices is scaled down to the sub-10nm, tunneling leakage current through gate dielectrics and reliability become serious problems. Thus, the high-k gate dielectrics become one of the solutions in providing increased capacitance and reduced leakage currents without significantly increasing the actual equivalent oxide thickness (EOT) of gate dielectrics. Among the high-k materials, Al2O3 thin film is one of the high-k materials that alternate SiO2 gate dielectric due to high dielectric constant, large band gap and low leakage current and excellent surface properties. In this paper we will present the results of ALD grown Al2O3 films with varying different reactants. Al2O3 films were deposited on n-type (100) substrate using trimethylalumimium (TMA), (CH3)3Al or dimethyl-aluminum-isocoproxide [DMAP,(CH3)2AlCH3(CH3)2] precursor with various oxidants of O2, H2O and N2O. We also compared the results with plasma-assisted and non-plasma assisted films. The physical and chemical properties were analyzed by cross-sectional transmission electron microscope (XTEM), Auger electron spectroscopy (AES) and X-ray photoelectron spectroscopy (XPS). Also, electrical characteristics, including equivalent oxide thickness (EOT), hysteresis, leakage current were analyzed by I-V and C-V measurements. The results of these studies showed clean amorphous and stoichiometric Al2O3 films with low carbon concentration, low leakage current and high dielectric constant. In this paper, we will present the Al2O3 films as gate dielectric and compare the characteristics of Al2O3 grown by PEALD and MOALD.

E6.18 Characterization of the amorphous high-k oxide In203. Maurizio Zacchetti and Vincenzo Fiorenzi, Dept. of Physics, University of Cagliari, Monserrato, Italy.

High-k oxides are currently under scrutiny as possible candidates to replace silicon in Si CMOS gates. We investigated the structure of the amorphous phase of X203 rich-composite (X = La, Lu, Eu), whose crystalline phase is cubic bixbyite. Amorphization is effected by melt quenching using constant-pressure molecular dynamics with shell-model interatomic potentials, at various cooling rates (from 0.1 to 7 K/ps, with 7 K/ps corresponding to 10% per 10 ps). Configurational entropy is estimated by information-theoretic methods. Using ab initio DFT techniques, the amorphous configuration is further optimized in volume and internal structure. The amorphous structure resembles the crystalline structure of the parent crystalline structure in the Voronoi tessellation and the radial.
angular, and first-neighbor-count distribution functions. All the
named indicators show that in the amorphous phase the
Cr6+ /Cr3+ ion migration is not internally more compact and on average
more widely separated than in the crystal, leading to both an increased
density and a reduced dielectric constant.

E6.19 An Original Method To Detect Interaction Between
Poly-Si /Hi-K Dielectrics. Huaing Zhuo, John Kloth, Matthew
Bunyanoski, Wayne Wu, Joceng Jaron, Xi Xiang, Furaid Aramian, Bob
Choe-Phillips. Technology Development, Advanced
Micro Devices, Sunnyvale, California.

Possible interface interaction between poly-Si and high dielectric
constant (Hi-K) dielectrics is of great importance in CMOSFET device
performance using Hi-K films as gate dielectrics. Conventional
detection techniques such as TEM or by electrical characterization
from MOSFET are expensive and time-consuming. In this paper, an
original method is used to detect possible interface interaction between
poly-silicon / Hi-K dielectrics by using mercury-probe station
Capacitance-Voltage (CV) and Current-Voltage (IV) measurement for
blank films. The Hi-K dielectric film was ~30nm nitrided Hf-silicates
(HfSiON) prepared by MOCVD technique on p-type silicon substrate.
After dielectric film deposition, a 20nm poly-Si was deposited on
HiK film at 570°C, 400torr without doping. Film stack with
poly-Si/SiON on Si was used as a reference. CV and IV measurement
was done on blank film stack using mercury probe station before and
after poly-Si deposition. Before poly-Si deposition, the electrical
equivalent oxide thickness for HfSiON and SiON was 11.9 and 17.2A,
respectively. After poly-Si deposition, the poly-Si/HfSiON had EOT
~77A while poly/Si/SiON stack ~81A, which clearly showed that poly-Si
was working as dielectric with dielectric constant ~12. Significant
deployment region capacitance increase for CV curves of poly-Si/Hi-K
stack compared to poly-Si/SiON stack was observed. This indicated
possible electric interaction between poly-Si and Hi-K dielectric
introduced by poly-Si deposition. The possible mechanism was that
Hafnium-Oxygen bonding within HfSiON was decomposed by high
crystallization active atomic Hf species thus enabled Hf ions diffusing
into silicon substrate during high-temperature poly-silicon deposition.
In order to stop possible Hi diffusion, SiON dielectric layer between
HfSiON and Si substrate with thickness varying from 5A to 17A was
used instead of HfSiON. A thick interlayer was found that the
interlayer thickness was ~6A. This indicated Hi diffusion into Si in
contrast, Si3N4 with thickness up to 20A was not effective to stop
possible Hi diffusion.

E6.20 High thermal stable (HfO2)1-x (Al2O3) x gate dielectrics
for application in 50-nm generation devices. Qin Li1, S J Wang 2, P
C Lim3, A C H Hum4 5 and C K Ong6. 1Department of Physics,
National University of Singapore, Singapore, Singapore, 2Institute of
Materials Research & Engineering, Singapore, Singapore.

The silicon dioxide gate dielectric is approaching its application limit due
to the expected increase in tunneling and hence reliability concerns as the device scales to sub-100 nm dimensions.
One solution is to find suitable materials of higher dielectric constants (k) to replace silicon dioxide (SiO2). For silicon-based technology, SiO2 is used as the insulating layer and the semiconductor industry is comfortable with this approach. In contrast, very few high-k metal oxide materials possess resistance to crystallization as displayed by SiO2. Therefore, the ability to fabricate high thermal stability amorphous metal oxides is still sought after for the application of such oxides in semiconductor technology. In this report, the high thermal stable amorphous thin films of (HfO2)1-x (Al2O3) x were fabricated by a novel pulsed laser deposition technique on p-type Si (100). The rapid thermal annealing (RTA) effect on the microstructural and electrical properties of the films were studied. It was found the films with more than 80% HfO2 content still retain their amorphous structure after the RTA process. The TEM and electrical measurements yield a dielectric constant of about 13 for the films. However, SIMS and XPS studies suggest that Hf atoms have diffused into the silicon substrate, forming silicide bonds after the RTA process. Under optimized condition, ultra-thin films with equivalent oxide thickness 0.3 nm have been obtained. At high voltage of 1 V, the leakage current density is about 3.9 x 10^-12 A/μm². The results demonstrate that the ultra-thin (HfO2)1-x (Al2O3) x film is sufficiently stable against crystallization during rapid thermal annealing, and show promise as a gate dielectrics in future silicon-based devices.

E6.21 Phase Stability Study of HfO2 and HfO2-Al2O3 Alloy Thin Films. Kang Keon Lee 1, Zexing Shen 1, Andrew T S Wee1, Chen
Ching Yeow2, Byung Jin Cho3, Thomas Ospovice1 and Jiachen
Zheng4. 1Physics, National University of Singapore, Singapore, Singapore, 2Electrical and Computer Engineering, National University of
Singapore, Singapore, Singapore.

Due to its high dielectric constant, HfO2 (κ≈20) is a potential candidate for gate oxide replacement. However, as HfO2 is thermally stable and crystallizes at about 400 C, alloy materials that incorporate SiO2 and Al2O3 have been recently studied. In this study, we investigate the crystallization phases of HfO2 and HfO2-Al2O3 thin films (κ≈25) prepared by MOCVD. SiN films were deposited on p-type Si (100) substrates at 300 C. Characterization techniques used include FTIR, RBS, XPS and glancing incidence XRD (GLXRD). Samples were annealed using RTP up to a temperature of 1800 C. GLXRD results show that HfO2 thin films are amorphous with a small degree of crystallization. After annealing at 400 C, mixed monoclinic and tetragonal phases are observed. Complete transformation of HfO2 thin films from tetragonal to monoclinic phase occurs after annealing at 1000 C. HfO2-Al2O3 thin films remain amorphous up to an annealing temperature of 800 C. At 1000 C, crystallization occurs for films with greater than nominal 40% HfO2, and the effect of suppressed crystallization was more pronounced in HfO2-Al2O3 thin films than in HfO2 thin films. It was observed that the diffraction peaks of HfO2-Al2O3 films shift towards higher diffraction angle when compared to HfO2 thin films as a result of reduced bond length. In addition, the HfO2-Al2O3 thin films crystallize in the tetragonal phase in high Al2O3 matrix and it crystallizes in the monoclinic phase otherwise.

E6.22 A Study of MOCVD-Grown HfO2 Thin films Using A Novel Precursor. M. S. Dharmarajakumar 1, G. C. Deepk 2, Nwokonta Bhe 2, and S. A. Shivashankar1. 1Materials Research Center, India Institute of Science, BANGALORE, Karnataka, India; 2Devices Lab, ECE
Department, Indian Institute of Science, BANGALORE, Karnataka, India.

A novel metalorganic complex, N,N,N,N-tetraethyl-3,5,5,7,9-pentaoxydecyl-1-hafnium(V), HF(thd)1-xNO3, has been synthesized and characterized by IR, NMR,
MS spectroscopic techniques and elemental analysis. The crystal
structure of the complex has been confirmed by single crystal XRD.
The thermal characteristics of this complex have been studied by
TG/DTA. The metalorganic complex is volatile, starts sublimating at
about 150°C, with the weight loss amounting to about 6% of the initial
weight sample at 100°C. Thin films of hafnium dioxide (HfO2) are
deposited by low pressure MOCVD using this complex as the precursor,
on various substrates such as Si (100), fused silica, glass and polycrystalline aluminum, in a horizontal hot wall reactor built in
house. The deposition temperature and pressure were in the range of
400-700°C and 1-10 torr respectively. The HfO2 thin films are
characterized by XRD, SEM and FTIR. The dielectric characteristics of
as deposited films and the films annealed at different temperatures
(oxygen/argon ambient) are studied by HFCV and IV measurements.
The HFCV hysteretic and leakage current reduced in the annealed
samples. The dielectric constant calculated from the experimental
data is found to be in the range of 3-13.

E6.23 Annealing Behaviors of Void-type Defects in SiO2/SiC
Probed by Slow positron Beam. Min Gong 1, Hengjun Liu 1, Haiyun Wang 2, Huiming Weng 2 and Wen Yang 2. 1Department of
Physics, Simon University, Chengdu, Sichuan, China, 2Department of
Modern Physics, University of Science and Technology of China, HeFei, Anhui, China.

Silicon carbide has been realized to be one of the powerful
semiconductors. Various kinds of devices, including Schottky diodes,
bipolar transistors, MOSFETS and some 1C units with good
properties, have been manufactured using SiC. In these devices, SiO2 films play important roles. However, since the existence of carbon atoms, qualities of thermal oxidation formed SiO2 films on SiC wafers were far from as good as those on Si. The effects of impurities on the C/V characteristics of SiO2/SiC have been investigated by using atomic sensitive probes in the secondary ion mass spectrometry (SIMS) and the x-ray photoelectron spectroscopy (XPS). These
analyzing techniques are not adequate for full understanding of
characteristics of SiO2/SiC interface and structure of SiC film since
a large of void-type defects will form during thermal oxidation and
post-annealing due to removal of C atoms and CO molecules. In this work, the technique of Doppler broadening of
positron annihilation spectroscopy (PAS) has been used to reveal
information on void-type defects of SiO2/SiC system. Variable-energy positron beam makes positrons to different depth in the sample. The value of the S-parameter, which reflects the number of positrons annihilated with low-momentum electrons, increases since the reduced electron density at open volume decreases with more carbon atoms and CO molecules in the material. Therefore, the electron density at open volume decreases with more carbon atoms and CO molecules in the material. Therefore, the electron density at open volume decreases with more carbon atoms and CO molecules in the material. Therefore, the electron density at open volume decreases with more carbon atoms and CO molecules in the material.
Post-annealing were done at 1100°C in nitrogen gas. The thickness of the SiO2 film was about 0.6 nm measured by ellipsometry. Variable temperature [0.3-2000 K] measurements have been made on the samples at different annealing temperatures. The measurement results show that the SiO2/Si system has a narrow activation energy for oxygen diffusion. The activation energy decreases with increasing temperature.

E6.24 Stoichiometric control of ZrO2/SiO2 films using atomic layer deposition. Lijun Zhao1, Fang Chen1, Stephen A Campbell2 and Wayne I. Glaedtler3, 1Dept. Chem Eng & Mat Sci, University of Minnesota, Minneapolis, Minnesota, 2Dept. Elec & Comp Eng, University of Minnesota, Minneapolis, Minnesota, 3Dept. Chemistry, University of Minnesota, Minneapolis, Minnesota.

The atomic layer deposition (ALD) of triethoxysilane (TEOS) and zirconium acetylacetonate (Zr(acac)4) on Si (100) substrates at a low temperature (162°C) results in a film of high-quality ZrSiO4. The growth rate is controlled by the deposition sequence, resulting in a high rate of 2.5 Å per cycle. The film composition (Zr/Si = 1:1) is achieved at a low substrate temperature of 162°C.

E6.25 Improved structural properties of sputtered hafnium dioxide on silicon and silicon oxide for semiconductor and sensor applications. Heinrich Grueger, Christian Kunath, Eberhard Kurfürst, Stephan Sorge and Wolfsum Toll; Sensors Division, Fraunhofer IPMS, Dresden, Saxony, Germany.

Hafnium dioxide (HfO2) is a candidate with promising properties for semiconductor industries as well as for optical and sensorial applications. Chemical etching of HfO2 films in an HF:O2:Ar plasma results in highly crystalline and stoichiometric films. The high aspect ratio of the deposited layers allows for the fabrication of high-performance micromechanical devices.

E6.26 Abstract Withdrawn

conductivity (~1.43 S/cm) was measured by a four-probe method. K-doping using K-trioxidate to make Cu₂ZrSnS₂K₀.₂ is being investigated to increase the dielectric constant and other electrical properties of this material.

**E6.30**
**Transparent Transistors Based on Semiconducting Oxides.** Yongsheng Kwon¹, Y. Li², W.Y. Heo³, M. Jones⁴, V. R. Varadan⁵, B.S. Jeong¹, J. Zhou¹, S. Li⁵, H. Paul⁵, and D. P. Norton⁶

The synthesis and properties of transparent thin film transistors (TFTs) is reported using pulsed laser deposition. The field effect transistors are made with ZnO and SrCeO₄ as the channel material. Low leakage current density is achieved with amorphous (CeOₓ)Ga₂O₃ (CTMA) acting as the gate oxide, whose dielectric strength is measured to be 5MV/cm for structures fabricated on IndiaKinline (ITO) substrates. Capacitance-voltage properties show that n-type active layers are realized with undoped ZnO. Little hysteresis effects are observed when gate voltage is swept from accumulation to depletion. Charge densities in undoped ZnO are measured to 10⁻¹⁰ to 10⁻⁹ F/cm², using Hall measurement and CV plots. Current-voltage measurements for TFT operation are reported. Channel materials with thickness ranging from 20 to 2000 nm on patterned substrates show high conductance and modulation of channel conductance. CV measurements with MOS structure using doped Zn, Mg, and Sr and CeO₂ will also be described. The properties of depletion mode TFTs fabricated with doped and undoped oxide channel will be discussed in detail.

**E6.31**
**Effects of Ge on Thermal Decomposition of Ultrathin Silicon Oxides/Insulators.** Luqiang Zhang¹, Bin Yang¹, Paul Rughesop⁵, Feng Liu⁵ and Max G. Lagosky¹
¹University of Wisconsin-Madison, Madison, Wisconsin; ²University of Utah, Salt Lake City, Utah.

Silicon-on-insulator (SOI) substrates have attracted much attention because they greatly enhance the performance and reduce the power consumption of CMOS transistors. As the Si template layer thickness in SOI is reduced, the device is more and more thermally unstable, decomposing another islands at temperatures approaching processing temperatures [1, 2]. We have studied the effect of Ge deposition on the thermal decomposition of thin SOI. The thermal decomposition temperature of ultrathin SOI decreases with increasing Ge coverage. The temperature ordering of 3D Si islands seen in the decomposition of SOI is gradually lost with increasing Ge coverage. This observation can be understood in terms of the strain and surface energy anisotropy. As the Ge coverage increases, the strained Si island is covered more completely by Ge. It should then decompose more easily. Furthermore, the surface energy anisotropy between [111] and [110] facets on SiGe islands is smaller than that for the same facets on Si islands. Consequently, SiGe islands are not strongly faceted. The driving force for ordering along [110] directions is the hallmark of decomposition on SOI is therefore absent when Ge is deposited on SOI, and the 3D SiGe islands are randomly distributed. The lowering of the decomposition temperature of SOI that can be observed on the Si template layer suggests that the allowable processing temperatures or the thinness of SOGOI that can be used may be limited. [1] B. Legrand, V. Agnese, J. P. Nys, V. Senez, and D. Stievendi, Appl. Phys. Lett. 82, 2277, 2003; [2] R. Naryada, Y. Ishikawa, and M. Take Appl. Surf. Sci. 159, 121, 2000. Research supported by DARPA and DOE.

**E6.32**
**Study of work function of CVD WSix thin film on high K dielectric.** Sylvain Magrin¹, Stephane Allegret², Frederic Filloux³, Thierry Fierjo², Francois Martin², Bernard Guillaumot² and Gerard Passemard²
¹CEA-LETI, Grenoble, France; ²STMicroelectronics, Crolles, France; ³STMicroelectronics, Grenoble, France.

To meet requirements of MOS circuits at sub 65nm scale, gate oxide thickness shall decrease. Thus high K materials are needed as dielectric gate. In this setting, due to gate depletion effect, metal material should be used as an alternative to polysilicon gate. Moreover, specifications on threshold voltage require modulation of gate material work function with respect to NMOS or PMOS transistor. Work function is known to be sensitive to material stoichiometry. In this work, WSix thin films with x between 2.2 and 2.5 are evaluated as metal gate on HfO₂ and SiO₂ dielectric. Film chemical characteristics are correlated with work function measurements. Thin films are deposited using WEP and doped using 20nm Si wafer industrial chamber. Thermal treatments are applied to sample in order to recrystallize the film and confirm it.

stability. MOS Capacitors are processed. Electrical characteristics (capacitance vs voltage) are used to extract work function with respect to PMOS and NMOS. The electrical characteristics of the film are obtained from a 4-terminal measurement using x-ray emission from hexagonal to tetragonal after thermal annealing is observed using X-ray diffraction. Nevertheless, no strong morphological and compositional changes are detected after annealing using AFM, SEM observations, RBS and SIMS measurements. This indicates that films are stable up to 800° C anneal. Nominal film stoichiometry is evaluated by RBS. Using these characteristics and SIMS data, concentration profiles are obtained. A W/Si gradient is observed between dielectric/film interface and film surface. At dielectric/film interface, Si/W ratio is constant whatever the nominal stoichiometry. These results are in agreement with work function measurements.

**E6.33**
**Oxide Reduction in Advanced Metal Stacks for Microelectronic Applications.** Wentao Qin¹, Alex Volinsky, Dennis Werho and David Theodore
¹Process and Materials Characterization Lab, Motorola, Tempe, Arizona.

Aluminum and copper are widely used for microelectronic interconnect applications. Interfacial oxides can cause device performance degradation and failure by significantly increasing electrical resistance. Interfacial oxide layers found in Al/Ta and Ta/Cu metal stacks were studied with Transmission Electron Microscopy (TEM) combined with Energy Dispersive Spectroscopy (EDS) and Parallel Electron Energy Loss Spectroscopy (PEELS). The analysis indicates that the observed interfacial oxide layers, Al₂O₃ and Ta₂O₅, result from spontaneous reductions of Ta oxide and Cu oxide, respectively. Classical thermodynamics enables interpretation of the results.

**E6.34**
**Thickness Effect of C40 TiSi₂ to C54 TiSi₂ Transformation.** Ze Xiong Shen¹, Sheng Cui¹, Yaping Zhang¹ and Alex See²
¹Physics, National University of Singapore, Singapore, Singapore; ²Chuanter Cell Semiconductor Manufacturing, Singapore, Singapore.

TiSi₂, C40 is widely used as a low-resistivity contact in CMOS devices. C54 is normally formed by thermal annealing of the TiSi₂ C49 phase between 750-850 °C. However, due to the so-called narrow line effect, the C49 to C54 transformation on narrow poly-silicon lines requires very high annealing temperature, which could result in severe process punch through and aggressive edge effects and even complete failure. Recently, significant breakthroughs have been made such that the C54 phase is formed from a TiS₀₄ C40 template, completely bypassing the C40 phase and allowing direct formation of C54 at a low temperature of around 700 °C. The thin C40 film itself can also be transformed to C54 easily at a relatively low temperature, making it a real possibility to extend the application of TiSi₂ for sub-quarter-micron devices. The promotional template effect of C40 phase on the formation of C54 phase has been discussed extensively, which is due primarily to the similarity between the bernal planes of C40 and C54 where the C40 has an ABCABC arrangement while C54 has an ABCDEABC arrangement. However, the C40 transforms to C54 is much less clear as the two phases are very different and it is difficult to understand the low temperature needed to transform C40 to C54. In this presentation, we discuss the thickness effect of pure C40 TiSi₂ induced by different types of pulsed lasers - Nd:YAG and excimer laser - Nd:YAG laser (~70 nm) is thicker than the C54 TiSi₂ induced by excimer laser (~15 nm). While the thinner C40 requires only RTP at 780 °C for 60 s (corresponding to an activation energy Eₐ = 2.5 eV) to transform to C54, the thicker C40 TiSil₂ requires a very high temperature of around 1000 °C for 60 s (Eₐ = 6.5 eV) to transform to C54, which is even higher than the activation energy for C49 to C54 transformation in the range of Eₐ = 3.5-6 eV. It is worth noting that the activation energy Eₐ increases with increase in C40 TiSil₂ layer thickness, reflecting the fact that the C54 phase nucleates at the triple grain boundaries of the C49 grains. However, the activation energy Eₐ decreases with increase in C40 TiSil₂ layer thickness, demonstrating that the C40 to C54 transition is via a different mechanism.

**SESSION E7**
**Epitaxial Oxides on Semiconductors**

**Chairs:** Suprakash Guha and Gerd Nunner

**Wednesday, December 3, 2003**

Room 207 (Hynes)

**8:30 AM E7.1**
**Epitaxial SrTiO₃ Films on Silicon: Medium Energy Ion Scattering Studies.** Lyudmila Goncharova¹, Dimitri Starodub⁴, Eric Gutfleisch¹, Yang Guo⁵, Virginia Vlasov⁵ and Darrell Scholl⁵. ¹Physics Department, Rutgers University, Piscataway, New Jersey; ²Chemistry Department, Rutgers University, Piscataway, New Jersey; ³Department of Materials Science and Engineering, Penn State University, University Park, Pennsylvania.
Perovskite metal oxide films, such as SrTiO$_3$ (STO), have become a technologically important class of materials due to their unique electronic, optical, and magnetic properties. They have significant potential to enable a variety of new applications, such as novel active materials, or as thin buffer layers enabling other integrated heterostructures to be built on semiconductor substrates. For epitaxial films it is usually assumed critical to achieve structural matching of the two phases that meet at the interface while retaining chemical phase separation. Therefore it is necessary to eliminate or at least partially remove or compensate for the lattice mismatch between the layers (epitaxial STO and Si, in our case) by controlling the deposition conditions and the specific growth sequence used in the experiments. We have used high-resolution medium energy (4–10 keV) ion scattering (MEIS) to investigate the composition as a function of depth at (≤5nm) crystalline SrTiO$_3$ films on Si (100). This technique allows us to get quantitative information about the films buildup and about the substrate interface structure. The thin SrTiO$_3$ films we have investigated were deposited on Si (100) at low temperatures in an excess of oxygen and then recrystallized through solid phase epitaxy by heating the films in vacuum. Our MEIS results show that films grown by this method have Asite (SrO) termination. Submonolayer amounts of strontium silicide, used in the initial stages of growth, are fully replaced with a crystalline silicate at the interface after growth is completed. In addition, Ti film was grown. MEIS results indicate that the SrTiO$_3$/Si interface is crystalline; however the geometrical structure deviates significantly both from the bulk epitaxial film and from the substrate. Resulting interfacial composition is determined by mechanisms for Ti, Sr, and Si diffusion in the interface region will be discussed.

8:45 AM ET 2
Characterization of the Interface between Epitaxial SrTiO$_3$ and Silicon, S. J. Wang, 1,2 A. C. Haas, 3 W. Tian, X. Q. Pan, V. Vaitheeswaran, 4 D. G. Schlom, 5 T. Gustafsson 6 and E. Garfunkel. 7
1Institute of Materials Research & Engineering, Singapore, Singapore; 2Department of Materials Science and Engineering, The University of Michigan, Ann Arbor, Michigan; 3Department of Materials Science and Engineering, Penn State University, University Park, Pennsylvania; 4Chemistry and Physics Dept, Rutgers University, Piscataway, New Jersey.

Epitaxial oxides on semiconductors need to have excellent physical properties and chemical stability for a variety of potential applications including gate dielectrics, ferroelectric random access memories, and buffer layers for the integration of functional oxides for hybrid microelectronic devices. The atomic-level structure of the interface between the epitaxial oxide and semiconductor is vital to the functionality of such heterostructures. This interfacial structure depends on the materials involved and, very importantly, on the details of the deposition process. In this work we have studied the epitaxial interface between epitaxial SrTiO$_3$ films grown on 100 Si. The films were grown by molecular beam epitaxy (MBE). Several different heterostructures are investigated in this work including SrTiO$_3$/Si, including silicate at the crystalline interface, silicate at the disordered interface, and reduced silicon oxide at both the crystalline and amorphous interfaces. In this work, we report a crystalline silicidenated structure in the SrTiO$_3$/Si interface through a combination of high-resolution transmission electron microscopy (HRTEM), x-ray photoelectron spectroscopy (XPS), and theoretical modeling. The HRTEM images show that the interface is well crystallized and free of an amorphous layer. A crystalline Sr$_2$Si$_2$O$_7$ layer is identified from XPS depth profiling, which is different from the disordered silicate structure previously reported at such interfaces. The results show that the Sr$_2$Si$_2$O$_7$ layer has high thermal stability, is lattice matched with silicon, and can be used as an interfacial template for the growth of other epitaxial oxide layers. The effect of rapid thermal annealing on the microstructure and the electrical properties of the SrTiO$_3$/Si heterostructures has also been studied using SIMS, XPS, TEM, and electrical measurements.

9:00 AM ET 2.5
Stability of alkaline earth barrier layers during epitaxial growth of (Ba, Sr)O on Si(100), Gerd J. Norga, 1 Alexandre Guiller, 1 Jean-Pierre Loos, 2 Heinz Siegle, 3 David Halley, 4 Christophe Rossel, 5 Chiara Marchiori, 3 and J. W. Seo, 1 Science and Technology, IBM Zurich Research Lab, P.O. Box CH-8803, Rüschlikon, Switzerland; 2Laboratory MDM, INFN, Agnese Brusina, Italy.

High-temperature alkaline earth barrier layers play a crucial role for achieving interfacial oxide-free epitaxial oxides on silicon (100). The stoichiometry and detailed atomic structure of these barrier layers remain the subject of intensive debate among theoreticians and experimentalists. In this paper, we present a new approach to probe the structure of the interface between the epitaxial oxide layer and silicon. Our method is based on the measurement of phase shifts in the HHIEED oscillation signal, collected during epitaxial growth of [Ba,Sr]O on top of the incumbent oxide-free class of materials, such as SrTiO$_3$, electronic, optical, and magnetic properties. They have significant potential to enable a variety of new applications, such as novel active materials, or as thin buffer layers enabling other integrated heterostructures to be built on semiconductor substrates. For epitaxial films it is usually assumed critical to achieve structural matching of the two phases that meet at the interface while retaining chemical phase separation. Therefore it is necessary to eliminate or at least partially remove or compensate for the lattice mismatch between the layers (epitaxial STO and Si, in our case) by controlling the deposition conditions and the specific growth sequence used in the experiments. We have used high-resolution medium energy (4–10 keV) ion scattering (MEIS) to investigate the composition as a function of depth at (≤5nm) crystalline SrTiO$_3$ films on Si (100). This technique allows us to get quantitative information about the films buildup and about the substrate interface structure. The thin SrTiO$_3$ films we have investigated were deposited on Si (100) at low temperatures in an excess of oxygen and then recrystallized through solid phase epitaxy by heating the films in vacuum. Our MEIS results show that films grown by this method have Asite (SrO) termination. Submonolayer amounts of strontium silicide, used in the initial stages of growth, are fully replaced with a crystalline silicate at the interface after growth is completed. In addition, Ti film was grown. MEIS results indicate that the SrTiO$_3$/Si interface is crystalline; however the geometrical structure deviates significantly both from the bulk epitaxial film and from the substrate. Resulting interfacial composition is determined by mechanisms for Ti, Sr, and Si diffusion in the interface region will be discussed.

10:00 AM ET 7.4
The Oxides/Semiconductors Interface: Experimental Characterization and Theoretical Calculations, A. Hauser 1, 2 and S. J. Wang 1, 2 1Institute of Materials Research & Engineering, Singapore, Singapore; 2Department of Physics, National University of Singapore, Singapore, Singapore.

The interfaces between oxides and semiconductors are very critical for the application of oxide thin films, including gate dielectrics and ferroelectric transistors. Much research has focused on understanding and exploiting the properties of novel oxide/semiconductor interfaces to fulfill the stringent requirements for these and other applications. In this work, we will use a combination of characterization tools to determine the nature of the oxide/semiconductor interface, including high resolution transmission electron microscopy (HRTEM), X-ray photoelectron spectroscopy (XPS) and secondary ion mass spectroscopy (SIMS), in conjunction with first-principles calculation to understand the interface properties. Three different oxide films, Yttrium-stabilized ZrO$_2$, HfO$_2$ and Y$_2$O$_3$ have been fabricated on silicon and SiGe substrates using pulsed laser deposition technique. The appearance of an amorphous interfacial layer can be controlled by varying the growth process. HRTEM images show atomically sharp interfaces, while several different interfacial bonding structures have been observed between oxide and silicon, including silicate at the crystalline interface, silicate at the ordered or disordered interfaces and silicate oxide at an amorphous interface. The interfacial atomic structures are confirmed by HRTEM image simulation and first-principles calculation with good agreement between experimental and theoretical results. The dynamic growth mechanism of epitaxial oxides on semiconductors and the electrical properties are also discussed in the report.

10:15 AM ET 7.5
Structural and Dielectric Characterization of Epitaxial Rare-earth Scandate Thin Films, Juergen Schubert 1, Ying Jia 1, 2, 3 M.D. Bierega 1, 2, O. Brueckner 1, S. Trolle-Makrina 1, 2 and D.G. Schlom 2, 1TSG I-FI, Forschungszentrum Jülich GmbH, Jülich, Germany; 2Department of Materials Science and Engineering, Penn State University, University Park, 16802, Pennsylvania.

The rare-earth scandates (Re$_2$O$_5$), where Re is a rare earth element) were initially proposed for application as SrTiO$_3$ and SrTiO$_3$/Si MOSFETs in either amorphous or epitaxial form. That rare-earth scandates are promising for this application was based on measurements on single crystals of three different rare-earth scandates: Dy$_2$O$_3$, Gd$_2$O$_3$, and Sm$_2$O$_3$. All showed relatively high dielectric constants (K), high optical band gap energies, and stability in direct contact with silicon. In this work we investigate the dielectric properties and structural perfection of epitaxial Re$_2$O$_5$ thin films, including compositions identical to those whose properties have been studied as single crystals (i.e., Dy$_2$O$_3$ and Gd$_2$O$_3$) as well as a new composition whose high melting temperature prevented it from being measured studied as a single crystal (i.e., La$_2$O$_5$ with T$_m$ ~ 2900°C). The Re$_2$O$_5$ have been grown as a structure (space group Pbnm) with lattice parameters fitting nicely to the lattice parameter of Si(100). To verify that the dielectric properties of Re$_2$O$_5$ single crystals apply to epitaxial Re$_2$O$_5$ thin films and to investigate the properties of new rare-earth scandates, we have prepared Gd$_2$O$_3$, Dy$_2$O$_3$, and La$_2$O$_5$ epitaxial thin films using pulsed laser deposition. The films were grown on SrTiO$_3$(100) and SrTiO$_3$(100) covered with an epitaxial SrTiO$_3$ layer [4×4 nm with a thickness of 1 µm]. Dehydration treatment was performed at a pressure of 10⁻³ Torr using a mixture of O$_2$ and N$_2$. The thin film was annealed at a temperature ranging from 500°C to 1000°C. The thin film growth was performed at a temperature of 450°C. The films were analyzed using X-ray diffraction measurements and four-circle x-ray diffraction measurements. All of the materials showed epitaxial growth on SrTiO$_3$(100). Channelling minimum yield values ($\chi_{min}$) as low as 0.3% and rocking curve widths as narrow as 0.16° indicate the good
crystalline quality of these epitaxial layers. Electrical measurements were performed to determine the K-values of the different materials in thin film form. For La2O3, K-values of 26 were obtained.

10:30 AM E7.6

Projected transistor scaling trends require one to think about ways of making ultrathin silicon and germanium layers on buried insulators. One way of doing this is via epitaxial growth of crystalline oxides on semiconductors followed by the epitaxy of semiconductors on these oxide surfaces. The most recent trend is to use the same semiconductor-on-semiconductor epitaxy that we have been using to over the past 30 years, controlling oxide-semiconductor layers and interfaces is a considerable challenge given that we are trying to bring together materials with quite different valence, ionization, and bonding. Though microstructurally an oxide on silicon may have seemingly “perfect” registry of atoms across the oxide-semiconductor interface – it is unclear entirely what that buys us since the electrical consequences of such chemically dissimilar interfaces remain. While there has been a quite a bit of activity in growing epilaxial oxides on silicon the past decade, the epitaxy of semiconductors on these oxides is a further challenge made difficult by surface energy considerations that drive a Volmer Weber initial growth mode. We will address these issues in reporting on our results in growing epitaxially matched lanthanum yttrium oxide insulating films on silicon and then growing silicon grains by epitaxial growth. The oxide structures epitaxially on top of these oxides.

11:00 AM E7.7
Electrical Characteristics of Metal - (La2O3)x(Y2O3)yO - Silicon Capacitors. Edward Presler, Nestor Bojarczuk and Suprganik Gula; IBM T. J. Watson Research Center, Yorktown Heights, New York.

An investigation of metal-insulator-semiconductor capacitors, utilizing single crystal (La2O3)x(Y2O3)yO as the insulator is presented. Crystalline insulators are of interest because of the possibilities of obtaining an atomically flat interface and entirely eliminating the presence of dangling bonds at the interface. Capacitance – voltage measurements performed on MIS capacitors demonstrate a dielectric constant of 15 and suggest the absence of any interfacial oxide layer. The equivalent oxide thickness of the sample with the thickest dielectric layer is 13.5 Å. The flat-band voltage shift in as-grown samples scales linearly with the insulator thickness, indicating that fixed charge is isolated close to the semiconductor interface, or perhaps that a dipole layer forms at the interface between the silicon and the insulator. Interface state densities were found to be in the mid 10^12 cm^-2 electron/volt range and did not vary significantly after post-metallization annealing.

11:15 AM E7.8
Epitaxial and amorphous La2Hf2O7 on silicon for high-k gates. Athanasios Dimoulas1, George Vellianitis2, George Apostolopoulou1, Georgios Mavrou1, Anastasios Travlos1, J.C. Hooker3 and Z.M. Hittmenn1; NCSR DEMOKRITOS, ATHENS, Greece,4Philips Research, Leuven, Belgium.

Ultimate device scaling with equivalent oxide thickness (EOT) below 0.5 nm requires gate dielectrics with permittivity k higher than 20, grown on silicon or with novel materials. Up to now, perovskite SrTiO3 was the only known oxide with sufficient electrical quality on silicon. In this work, we show that other materials like the lattice matched perovskite La2Hf2O7 can be grown epitaxially on silicon with no interfacial layers using atomic oxygen beams from an RF plasma source in a MBE system. At 770 °C, this material grows in a cubic-cube on cubic mode on silicon such that La2Hf2O7(001) // Si(001) and La2Hf2O7(110) // Si(110) with clean, commensurate interfaces, although atomic morphology is rough due to the generation of large thermal strain. At lower temperatures around 700 °C, the material changes epitaxial orientation such that La2Hf2O7(111) // Si(111) while at even lower temperatures, the oxide is amorphous on silicon, up to 10-210°C. A fcc 9 11V accumulation were obtained in a sample with a total physical thickness of 3.3 nm and an interfacial layer of 1 nm. Despite the medium k value, the material could be a promising candidate provided the epitaxial films with no interfacial layers and with post deposition annealing can be obtained. [1] McKee et al., Phys. Rev. Lett. 81, 3014 (1998).
Depletion mode GaN MOSFETs have shown superior high temperature device performance compared to conventional GaN MOSFETs. Fabrication of the higher electric-field mode MOSFETs on GaN will require a more complete understanding of the oxide/nitride interface for further reduction of interfacial traps. However, GaN-based HEMTs are more highly developed and are now being fabricated in commercial bulk GaN substrates. Therefore, the problem is greatly reduced by the addition of a dielectric on the top surface of the fabricated HEMT, which acts as an oxidation layer to reduce the surface recombination. This will discuss the effects of substrate surface preparation of GaN, both in situ and ex situ, and the subsequent gas-source MBE growth of Sc$_2$O$_3$ and MgO. Surface preparation techniques have been used using RHEED, AES, SIMS, and XPS measurements to produce films of low interface trap density. L$_{2211}$-eV$^{-2}$cm$^{-2}$. A small volume of the as-fabricated HEMT surface was carried out to carry a cleaning procedure prior to dielectric passivation. The post-deposition treatment is included AES and XPS, as well as pulse and isolation current measurements for the passivated HEMT devices. From this study, the relationship between the surface structure and chemistry and the quality of the oxide/nitride electrical interface has been determined. This has led to the near-elimination of the current collapse phenomenon. In addition, the results of oxide/nitride interface quality have allowed for the first demonstration of inversion in GaN.

Metal oxides possess a wide range of novel electronic, optical, magnetic, and chemical properties that make them uniquely suitable for a number of potential technologies. Integration of crystalline oxides with semiconductors provides an opportunity through which the functional properties of oxides and mixture technology of semiconductors can be exploited simultaneously. The integration of the interface lies in chemical and structural similarities at an oxide/semiconductor interface. In this paper, we will show that using interface engineering, integrated systems with desired properties can be attained. We will first show that using a Ti pre-layer, epitaxial perovskite oxides such as SrTiO$_3$ can be grown on GaN. The chemical and electronic effective of the Ti layer will be discussed. Initial results of SrTiO$_3$ growth, band offsets and band bending at SrTiO$_3$/GaAs interface, and interfacial structural properties have been examined by photoemission, RHEED, STM, and TEM, and the results will be presented at the meeting. In addition to GaAs, we will discuss growth of perovskite oxides on Si. We will focus on modification of surface structure and interface energy upon formation of a Sr$_x$Ti$_{1-x}$O$_3$ layer on Si. Using several surface techniques, we have examined effects of Sr on Si dimer structures and dimer-derived states, and changes of surface electronic structures upon Sr deposition on Si. Different values of Sr coverages were examined in the atomic scale, and the Sr$_x$Ti$_{1-x}$O$_3$ layer on heteroepitaxy of crystalline SrTiO$_3$ on Si.

A ferroelectric oxide-semiconductor heterostructure (Pb$_2$Zr$_{1-x}$Ti$_x$O$_3$ or PZT (30/70))/GaAs and a metal-ferroelectric oxide-semiconductor heterostructure (Pb$_2$Zr$_{1-x}$Ti$_x$O$_3$ or PZT) have been fabricated, and the nanostructure and nanomechanical properties characterized by different methods. The nanostructure analysis confirmed a stoichiometric, phase-pure perovskite PZT films with (111) out-of-plane orientation. The ferroelectric character at 100 kHz estimated from the capacitance in accumulation was 200 but decreased to 45 with decreasing thickness. Using Pb$_2$Zr$_{1-x}$Ti$_x$O$_3$ as the ferroelectric layer the ferroelectric hysteresis loops were asymmetrical with lower polarization values compared to metal-ferroelectric-metal (M-F-PZT-Ru/GaAs/Sapphire or MFM) configuration. However, a well-defined and a nearly square hysteresis loop, $2P_c \approx 30 \mu$mC/cm$^2$ and $E_r \approx 76$ kV/cm, was observed for PZT films on GaAs.
Ru/GaN/Sapphire. The observed electrical properties are discussed in the light of MFS and MFM configurations, and depolarization fields.


We have fabricated a p-n junction, consisting of hole doped (p type) manganese and electron doped (n type) ZnO layers grown on sapphire substrate. These junctions exhibit good electrical rectifying behavior over the temperature range 200-1000K. Electrical characteristics of La$_x$Sr$_{1-x}$MnO$_3$ (LSMO) films by using the built-in electric field of the junction. It has been found that in the case of a 5 nm thick LSMO film, depletion region extends over entire film under zero biasing condition. By applying the external bias voltage, the thickness of the depletion layer and hence the electrical and magnetic characteristics of LSMO film can be modified. Precise control over the electrical and magnetic characteristics of giant magnetoresistive (GMR) LSMO films by using the built-in electric field of the LSMO/ZnO junction is an important step in the fast emerging magnetic industry. It also provides an opportunity to integrate various novel magnetic and magnetoelectronic properties of magnetic with nonlinear optical and optoelectronic applications of ZnO.

SESSION E9: Joint Session with C9: Gate Dielectrics and Functional Oxides on Silicon
Chair: Yashihuan Fajzulis Thursday Morning, December 4, 2003 Room 201 Eynus

8:30 AM E9.1 Lanthanum Oxide Thin Films for Advanced Gate Dielectrics, Bichek Vincenzo1, Claude-Christophe, Bernard Agnés1, Michel Trouilloud1 and Vincent Le Gaccon2, 2 Research & Development, STMicroelectronics, Crolles, France; 3Plastem Matériaux, LJPQ, Orsay, France.

For the past two years, the researches on advanced gate dielectrics have gained considerable attention since the technology roadmaps predict the need of a sub-30nm gate dielectric for sub-113nm MOSFET devices in 2002. The thinning of the gate dielectric required by scaling rules, currently between 2 and 2.5nm in fabrication, will give origin to unacceptably high gate current arising from electron tunneling through SiO$_2$ films. One possible solution is to use an alternative material to SiO$_2$ with dielectric constant (K) much higher than 3.9. Due to its high permittivity (K=38), La$_2$O$_3$ appears to be a good candidate. La$_2$O$_3$ films are deposited on Si substrates by rf magnetron sputtering of a La$_2$O$_3$ target in an argon atmosphere. This film properties are studied as a function of deposition (r/f power density, gas pressure) and thermal annealing parameters (temperature, time). One of the most important steps in our searching of La$_2$O$_3$ film properties is to correlate the physical properties of the material (composition, density) determined by Rutherford Backscattering Spectroscopy (RBS), Nuclear Reaction Analysis (NRA) and X-ray diffraction with the plasma characteristics investigated by optical diagnostics (Optical Emission and Absorption Spectroscopy). Whatever the deposition conditions, the film composition is O/La=1.3 ± 0.1 and its density is 7 ± 0.7 g/cm$^3$ (slab=6.5 g/cm$^3$). We have performed high frequency (1MHz, 10kHz, 1kHz) capacitance-voltage (C-V) measurements on Ra$_2$O$_3$/La$_2$O$_3$/Si MIS structure. With the device biased in accumulation regime, an insulating layer of 30 nm was deduced. The C-V curves exhibit well defined hump, depletion and inversion regimes which indicate a low interface state density.

9:00 AM E9.2 Liquid Injection MOCVD of Rare-earth Oxides Using New Alkoxide Precursors, Paul Andrew Williams, 1 Anthony C. Jones, 2 Helen C Aspinall, 2 Jeffrey M Gaskell, 2 Paul R. Chalker, 2 Paul A Marshall, 2 John L. Roberge 2 and Lesley M Smith 3; 1Epichem Limited, Bromborough, Wirral, United Kingdom; 2Chemistry, University of Liverpool, Liverpool, Merseyside, United Kingdom; 3Materials Science and Engineering, University of Liverpool, Liverpool, Merseyside, United Kingdom.

Thin films of rare earth oxides such as La$_2$O$_3$, Pr$_2$O$_3$, Gd$_2$O$_3$ and Nd$_2$O$_3$ have potential applications as all-dielectric layers in silicon-based field effect transistors. MOCVD is an attractive technique for the deposition of these materials, but growth has been restricted due to lack of suitable precursors. There are some reports on the use of metal-dialkoxy precursors, but these often require high growth temperatures and carbon contamination is a potential problem. Although metal alkoxides have been widely used in MOCVD, there have previously been no reports in the literature on the use of rare-earth alkoxide precursors in MOCVD. This is because the large ionic radius of the highly positively charged lanthanide (III) ions leads to the formation of bridging intermetallic-metal-oxo-bonds, resulting in many of the simple alkoxide complexes being polymeric or oligomeric, with a corresponding low volatility. However, the sterically hindered donor functionalised alkoxide ligand 1-Methoxy-1-Phenyl-2-Propanone, OMe$_2$CH$_2$OMe (mpmp), favours the formation of the volatile metal alkoxide complexes [M(mpmp)$_3$] (M = La, Pr, Gd etc). In this paper the synthesis of a number of these new complexes is described together with their use in liquid injection MOCVD.


Thin films comprising group-V metal oxides are likely candidates for replacing SiO$_2$ in high-performance low power Si electronics where the effective electrical thickness of the gate oxide must be less than the equivalent of 1.0 nm of SiO$_2$. Elemental oxides such as ZrO$_2$ and HfO$_2$ have dielectric constants that are in the suitable range, e=28-30, but crystalize readily under standard process conditions (1000°C for 5-20 seconds) required to activate ion-implanted dopants. It is known that crystallization can be suppressed by alloying with a main-group oxide such as SiO$_2$ or Al$_2$O$_3$, although these oxides have a much smaller dielectric constant and therefore strongly decrease the dielectric constant of the mixture. We have investigated the onset of crystallization of various transition-metal/main-group oxides using a composition-graded approach. This technique allowed us to determine that the mole fraction of main group oxide in the Zr-Si-O, Zr-Al-O, and Hf-Si-O systems must be greater than 10%, 65%, and 78%, respectively, in order to avoid crystallization. The kinetics of transformation suggest that this conclusion is not sensitive to the anneal time, though it is quite sensitive to the peak temperature. Evaluation of the dielectric constant in the same systems leads us to conclude that the useful dielectric constant is therefore limited to e < 6.9, 12.7, and 6.6, respectively. We conclude that the silicate systems are not likely to be useful replacements for SiO$_2$ while aluminates are more promising.

9:30 AM E9.4 Epitaxial thick film heterostructures of Pb(Mg$_{1/3}$Ni$_{2/3}$)$_2$O$_{3-3x}$-Pt/TiO$_2$ relaxor ferroelectric films on silicon for high performance electronics and MEMS, Dong Min Kim, Sung Don Bu, Chang Beom Eom, Vahnuor Nigaranj, Jun Ouyang, Ramamoorthy Ramesh, Venu Vithayathil, Susan Trotter-McKinnstry, Darrell G. Schrom, W. Tian and Xinqiao Pan; 1Materials Science and Engineering, University of Wisconsin-Madison, Wisconsin, 2Materials and Nuclear Engineering, University of Maryland, College Park, Maryland; 3Materials Science and Engineering, The Pennsylvania State University, University Park, Pennsylvania; 4Materials Science and Engineering, University of Michigan, Ann Arbor, Michigan.

Pb(Mg$_{1/3}$Ni$_{2/3}$)$_2$O$_{3-3x}$-Pt/TiO$_2$ (PMN-PT) single crystal relaxor ferroelectrics yield significantly higher electromechanical coupling coefficient than conventional polycrystalline ferroelectric materials. A major challenge is to fabricate epitaxial PMN-PT thick films between epitaxial metallic oxides and integrate them into micro-electromechanical systems on silicon wafer. We have created epitaxial thin films with the highest longitudinal piezoelectric tensor coefficient ever realized on silicon substrates by (1) using Pb(Mg$_{1/3}$Ni$_{2/3}$)$_2$O$_{3-3x}$-Pt/TiO$_2$ (PMN-PT), the material which in single crystal form is known for its giant piezoelectric response, (2) using epitaxial growth to optimize it optimally, and (3) nanostructuring it to reduce the constraint imposed by the underlying silicon substrate. When subdued by focused ion beam processing to reduce mechanical contrains, a 4 µm thick film shows a low-field d33 of 425 pm/V that increases to over 740 pm/V upon anneal of the sample in a mixture of nitrogen and hydrogen at 850°C for 30 min, higher than the highest strain achieved in Pb(Zr:Ti)0.3 thin films on silicon. These heteroepitaxial heterostructures can be used for multilayered MEMS devices with high strain and low driving voltage for miniature devices, high frequency ultrasound transducers for medical imaging, tunable dielectrics, and capacitors for charge and energy storage. We will discuss the effect of substrate constraint and thermal strain on the piezoelectric responses in heteroepitaxial PMN-PT thick films on silicon.

9:45 AM E9.5 c-axis oriented Epitaxial BaTiO$_3$ Films on (001) Si, Venugopala Vithayathil, James Lettieri, Darrell G. Schrom, 1
We have been investigating the epitaxial growth of c-axis oriented BaTiO$_3$ on [001] Si for a novel quantum computing architecture in which an epitaxial ferroelectric film in close proximity to silicon is desired. Subsequently, because of the weak inter-bilayer coupling for electrons and relatively long transverse decoherence time. The ferroelectric must be oriented such that its switching results in an electric field effect to confine the electrons laterally in the underlying silicon. The 4.55 lattice mismatch between BaTiO$_3$ and [001] Si at a typical growth temperature of 600 C, coupled with the much smaller thermal expansion coefficient of silicon than BaTiO$_3$, has until now prevented the growth of c-axis oriented epitaxial BaTiO$_3$ films on [001] Si. This work reports on the lattice constant of the BaTiO$_3$ film to its bulk cubic lattice constant at the elevated growth temperature. As such a relaxed BaTiO$_3$ film is cooled from its growth temperature, it experiences biaxial tension due to the larger thermal expansion coefficient of the BaTiO$_3$ film compared to the silicon substrate. When the film cools through the Curie temperature of the BaTiO$_3$, the c-axis of the BaTiO$_3$ aligns in the plane of the substrate (a-axis oriented BaTiO$_3$) to reduce the biaxial tension. To achieve the desired c-axis oriented epitaxial BaTiO$_3$ film on [001] Si for our application, a buffer layer of relaxed Sr$_2$TiO$_3$ is introduced between the Si and BaTiO$_3$ and the BaTiO$_3$ film has maintained the c-axis. The henceforth strained to the underlying relaxed Sr$_2$TiO$_3$ buffer layer. The films are grown by reactive MBE. In situ characterization of the films by XRD and RHEED characterization by XRD shows that the epitaxial c-axis oriented Sr$_2$TiO$_3$ films with rocking curve widths (FWHM in ) as narrow as 0.4°. The orientation relationship between flat substrate and Sr$_2$TiO$_3$ film is [001] // [001] and Sr$_2$TiO$_3$, [001] // [001]. By applying a voltage between a conductive AFM tip and the silicon substrate, domains with up and down polarization have been written in the films at locations specified by the user. Piezo-response AFM has been used to observe the written domains, which have lateral extent down to ~100 nm. J. Levy, Phys. Rev. A 6, 012320 (2010).

10:30 AM #E0.6 Long Retention Performance of a MFIS Device Achieved by Introducing High-k Al$_2$O$_3$/Si$_3$N$_4$/Si Buffer Layer. Yoshishin Fukijsaki, Kunie Ikeda, Hiroshi Ishiwana, Frontier Collaborative Research Center, Tokyo Institute of Technology, Yokohama, Japan; “Research and Development Association for Future Electronic Devices, Tokyo, Japan.

We introduced high-k Al$_2$O$_3$/Si$_3$N$_4$/Si buffer layer in MFIS (Metal-Ferroelectric-Insulator-Semiconductor) devices to realize long retention. We succeeded in increasing the electrically written data retention time longer than 2x10$^9$ sec. This long retention time is mainly due to the high insulating property of the buffer layer by reducing the loss of retained charges with minimizing the leakage current. We prepared thin (0.1) bilayered Al$_2$O$_3$/Si$_3$N$_4$/Si buffer layer by directly nitriding Al$_2$O$_3$ buffer layer at high temperature (300 °C). We could anneal the film to eliminate the defects in the film. The post oxidation was performed at 1000 °C for 30 sec in 5% O$_2$/5% N$_2$ ambient. On this stacked buffer layer, we deposited 150 nm-thick Bi$_2$La$_{5-x}$Ti$_{2+}$O$_{9+y}$ (BLT) ferroelectric films using LASMCD (Liquid Source Misted Chemical Deposition) technique. The BLT film were crystallized at 800 °C in oxygen ambient. The deposited BLT films oriented mainly along the c-axis of BLT crystal lattice normal in Al$_2$O$_3$/Si$_3$N$_4$/Si substrate. Since our buffer layer is highly dense, it prevents the underlying Si substrate from being oxidized during the post oxidation of Al$_2$O$_3$ film and the crystallization of BLT film. Therefore, the stacked Al$_2$O$_3$ /Si$_3$N$_4$/Si buffer layer can have high capacitance density and low leakage current even after highly oxidizing thermal treatments. The interface state density between the AlD:Al$_2$O$_3$/Radical-Si$_3$N$_4$ stacked insulator and n substrate is as low as 10$^{11}$ cm$^{-2}$ eV$^{-1}$. The current density less than 10$^{-6}$ A/cm$^2$ is realized under the 1V bias condition by application using films with the capacitance density of 128 F/μm$^2$. The memory window larger than 3V was realized in CV characteristics with ± 0.5 V voltage sweep. With this MFIS diode, we found that more than 1000% charge retention for 12 years. This excellent retention character is attributable to the high insulating property of the AlD:Al$_2$O$_3$/Radical-Si$_3$N$_4$ stacked insulator and also attributable to the perfect elimination of defects at the interfaces in the MFIS structure. This work was done under the R&D Projects in Cooperation with Academic Institutions (Next-Generation Ferroelectric Memory), supported by the New Energy and Industrial Technology Development Organization (NEDO), and managed by the R&D Center for Future Devices (RCFD) consisting of Hokkaido University, Tohoku University, the University of Electro-Communications, and Fukuoka University.

11:00 AM #E0.7 Investigation of Retention Properties for Y$_2$MnO$_3$ Based Ferroelectric/Insulator/Semiconductor (FIS) Capacitors. Takashi Yabuchi, Daisuke Ito, Hirokuni Sakata, Norimitsu Sugezumi, Kojiro Hara, and Norifumi Fujimura, Graduate School of Engineering, University of Michigan, Ann Arbor, Michigan.

Ferroelectric gate field-effect transistors (FETs) have been investigated for the applications to nonvolatile memory devices due to the nondestructive read operation and the advantages of decreasing memory cell size. Because of the difficulty to obtain the excellent ferroelectric-semiconductor interface, ferroelectric gate FETs with a metalf-ferroelectric-(metal)-insulator-semiconductor (MFIS) structure have been widely studied. We have investigated Y$_2$MnO$_3$ films for MFIS type ferroelectric gate FET, because Y$_2$MnO$_3$ has suitable properties for this application such as small spontaneous polarization and low permittivity. We have succeeded in fabricating Y$_2$MnO$_3$ epitaxial films with 2_0 of 3.4 µC/cm$^2$ on [111] Pt/n-Si substrates and epitaxially grown [0001]Y$_2$MnO$_3$/[111] Y$_2$O$_3$/[111] Si capacitors with ferroelectric type C-V hysteresis loops. In this study, we investigated the memory retention time of the Pt/Y$_2$MnO$_3$/Y$_2$O$_3$/Si capacitors are discussed using the leakage current analysis and the pseudo isothermal capacitance transient spectrum (pseud ICTS) and others. Although the retention time of the capacitors is better than 10$^9$ sec, we can improve the retention time by increasing the stacking current density was reduced from 4x10$^{-8}$ A/cm$^2$ to 2x10$^{-9}$ A/cm$^2$ by annealing under N$_2$ ambience. For the leakage current of the Pt/Y$_2$MnO$_3$/Y$_2$O$_3$/Si capacitors, we revealed that the oxidation emission was essential for memory retention state. However, Poole-Frenkel emission occurred when high voltage was applied. Since the activation energy of the Poole-Frenkel emission of the Pt/Y$_2$MnO$_3$/Y$_2$O$_3$/Si capacitors agreed with that of Pt/Y$_2$MnO$_3$/Pt capacitors, the origin of the Poole-Frenkel emission existed in the Y$_2$O$_3$ layer. It was also found that this leakage voltage with unnecessarily long time to polarization the ferroelectric gate layer generated the Poole-Frenkel defects in the ferroelectric layer and that the amount of the defects greatly affected the memory retention time. These results suggest that the Poole-Frenkel defects work as traps sites of the charge and that the charge injection to the Poole-Frenkel defects occurs gradually until it neutralizes the remnant polarization of the Pt/Y$_2$MnO$_3$/Y$_2$O$_3$/Si capacitors.

11:15 AM #E0.8 Characterization of Metal-Ferroelectric-Metal-Insulator-Semiconductor (MFMS) FEUTs using (Sr$_2$Sm)$_3$Bi$_2$Ta$_2$O$_9$ (SSBT) Thin Films. Hirotsugu Sadak and Eiwa Kojima, University of Tsukuba, Japan; “Koizumi Laboratory, Tokyo Institute of Technology, Yokohama, Kanagawa, Japan; RIEC, IT-21, Tohoku University, Sendai, Miyagi, Japan.

Metal-ferroelectric-metal-insulator-semiconductor (MFMS) structure has attracted considerable attention for ferroelectric-gate transistor application. MFMS structures have a merit that the current can be controlled in the area of an FM capacitor (Sr$_2$Sm$_3$Bi$_2$Ta$_2$O$_9$) and that of an MIS diode (Sr$_2$Sm$_3$Bi$_2$Ta$_2$O$_9$) independently. To match the ferroelectric polarization with the charge of FET channel, a large area ratio (S/S$_F$) is usually used in MFMS-FETs. However, S/S$_F$ is desirable for large-scale integration. We previously reported that S/S$_F$=1, Sr$_2$Sm$_3$Bi$_2$Ta$_2$O$_9$ (SSBT) thin film has small remnant polarization and large coercive field, which are suitable for MFMS structures. In this work, we fabricated metal and insulator bilayers for SSBT buffer layer and crystallization of SSBT film. Therefore, the stacked Al$_2$O$_3$ /Si$_3$N$_4$/Si buffer layer can have high capacitance density and low leakage current even after highly oxidizing thermal treatments. The interface state density between the AlD:Al$_2$O$_3$/Radical-Si$_3$N$_4$ stacked insulator and n substrate is as low as 10$^{11}$ cm$^{-2}$ eV$^{-1}$. The current density less than 10$^{-6}$ A/cm$^2$ is realized under the 1V bias condition by application using films with the capacitance density of 128 F/μm$^2$. The memory window larger than 3V was realized in CV characteristics with ± 0.5 V voltage sweep. With this MFIS diode, we found that more than 1000% charge retention for 12 years. This excellent retention character is attributable to the high insulating property of the AlD:Al$_2$O$_3$/Radical-Si$_3$N$_4$ stacked insulator and also attributable to the perfect elimination of defects at the interfaces in the MFIS structure. This work was done under the R&D Projects in Cooperation with Academic Institutions (Next-Generation Ferroelectric Memory), supported by NEDO and managed by FED.
Selective Deposition Of C-Axis Oriented Pb5Ge3O11 On Patterned Hi-K Gate Oxide By MOCVD Processes.
Tingting Li, Bruce Ulrich, Dave Evans and Sheng Teng Hsu; PTL, Sharp Labs. of America, Inc., Camas, Washington.

MFIS (Metal/Ferroelectrics/Insulator/Silicon) transistor ferroelectric memory devices have been fabricated. C-axis oriented Pb5Ge3O11 (PGO) thin films showed very good ferroelectric and electrical properties for IT-memory device applications. Extremely high c-axis oriented PGO thin films can be deposited on high k gate oxide, and functional IT-memory devices with PGO MFIS memory cell have been fabricated. The integration process induces damage such as etching damage that degrades the properties of FRAM devices and high surface roughness resulted in difficulty for alignment. In order to solve this problem, selective deposition processes have been developed to simplify integration processes and improve the properties of MFIS transistor ferroelectric memory devices. Based on different deposition rates of ferroelectric materials on high-k oxide and silicon dioxide, we selective deposited a c-axis oriented PGO film on patterned high-k oxide such as ZrOx (x=β-2), HfOx (x=β-2), TiO2, etc. and their mixtures other than on SiO2. By patterning the high-k dielectric, the PGO deposition is limited to just the preferred pattern area. SEM, EDX and x-ray measurements further confirmed that c-axis oriented PGO thin films selectively deposited on high-k gate oxide other than on field SiO2. Sometimes during annealing of the PGO, cracking of the field oxide occurs. This can be eliminated by not depositing PGO in the field area. The morphology of the PGO film can be very rough which can cause subsequent alignments to be very difficult if not impossible. Again by confining the PGO deposition to just the patterned area will also eliminate the roughness problem for alignments. Also etching damage is eliminated since there is no need to etch the PGO film, which improved the properties of FeRAM devices.