SYMPOSIUM D
Materials and Processes for Nonvolatile Memories

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* Invited paper
8:30 AM **D1.1** Future Direction of Non-Volatile Memory Technologies. Albert Fazio, Intel Corporation, Santa Clara, California.

This paper reviews the future direction of nonvolatile memory technologies. Moore’s law will continue to drive transistor-based memory technology scaling but technology complexity will be increasing. New memory concepts, not based on transistors, a basis of the memory cell, provide new opportunities for future low cost memories. Several of these new concepts will be summarized and contrasted with the mainstream transistor-based flash memory technologies. The task of introducing any new memory technology is very large. History has shown us that even successful new memory approaches take several years in research labs prior to attaining viable initial products and then several generations further are required for manufacturing learning on the new approach before it can displace the established incumbent in the marketplace, for cost, performance and scalability. It is therefore expected that for many years to come, the majority of the nonvolatile memories shipped will be based on current mainstream flash technologies, which utilize transistor-based charge storage memory cells and multi-level-cell concepts, for storing more than one logic bit in a single physical cell. In order to meet technology scaling, the mainstream transistor-based flash memories will need to evolve to incorporate material and structural innovations. Dielectric scaling in non-volatile memories is approaching the point where new approaches will be required to meet the scaling requirements, while simultaneously meeting the reliability and performance requirements of future products. For both the tunnel oxide and the inter-poly dielectric (IPD), high k materials are being explored as possible candidates to replace the traditional SiO2 and ONO (Oxide/Nitride/Oxide) films used today. The unique requirements of non-volatile memories, like the unique high-k material solutions from those being explored for traditional CMOS logic transistor scaling. Likewise, planar based memory cell scaling is approaching the point where physical space constraints force exploration of new materials and non-planar 3D scaling alternatives. Flash memory has historically utilized some 3D aspects, such as 3D wrapping of the floating gate for improved capacitive coupling. Both physical space limitations and transistor-based electrical limitations, in the gate, will need to drive the need for more complex 3D scaling in the future. This paper will review the current status and discuss the approaches being explored to provide scaling solutions for future transistor-based non-volatile memory products. Based on the introduction of material innovations, it is expected that the planar transistor-based flash memory cell can scale into the 32nm node. Further, more complex, structural innovations will be required to maintain further scaling.

9:00 AM **D1.2** Non-Volatile Memory Technology: Floating Gate Cell Concept Evolution. Cesare Clementi and Roberto Bec; CRD, ST Microelectronics, Agrate Brianza, Italy.

In the recent years the NVM market has experienced a fast growth thanks to the appearance of new memory technology particularly suitable for mobile applications. It is expected that in the next future portable systems will ask even more NVM both with high density and very high writing throughput for data storage applications, and with fast random access time for code execution in place. Nowadays two types of Flash architectures are considered as the industry standard: the common ground NOR, which is addressing both the code and data storage segments due to its versatility, and the NAND, optimized for the data storage market. Both of them are stacked gate cells, based on the concept of floating-gate (FG). Considering the evolution of the Flash, the technology scaling is one of the most important requirements that must be fulfilled to satisfy the strong market demand for lower cost memories. Till now the Flash scaling and the FG concept demonstrated to be really possible and to succeed in following the Moore’s law down to the 90nm technology node. The Flash technology is considered solid enough to sustain in the next few years the scaling down to the 45nm node. The Flash scaling to an even smaller beyond the 45nm node will face instead new issues, mainly related to the cell gate channel length and to the tunnel oxide thickness, which could affect the cell functionality and reliability. Hence the possibility to extend further the FG cell concept is strictly based on the opportunity to introduce new material and integration solutions. They must be able to solve the problems related to the active (W and L of the cell) and to the passive (FG, FG-active, active decoder elements of the cell) high value could be fundamental to reduce the gate L either as composite dielectric for tunneling (crested barrier) or as inter-gate dielectric for coupling. Other materials, like W or NiSi2, can be crucial to obtain a thin control gate with a low resistivity. Another possibility for the scaling path consists in substituting into the Flash structure the FG with discrete traps, formed by nano-crystals, or different technological processes. Extensive efforts of AMRAM or PCM are all trying to introduce in the basic CMOS process new materials, like perovskite, magnetic or chalcogenide to overcome the limits of the FG structure. All of them are anyway facing the issue of achieving scalability with the standard elements of the mainstream Flash process. The maturity of these technologies is still low and the pace of their learning curve is fundamental to carry on the fight with the scaling of the floating-gate cell, which will remain the reference technology till the end of this decade.

9:30 AM **D1.3** Lateral Distribution of Electrons Trapped in Nitride Layers. Marina Lorenzing1, Maarten Roosen1,2, Laurent Breuil1, Luc Haesebroug1, Jan Van Houdt1 and Kristin De Meyer, IMEC, Leuven, Belgium; 1Katholike Universiteit Leuven, Leuven, Belgium.

Recently, nitride-based trapping storage non-volatile memory concepts have received an increasing interest due to their smaller cell size, simpler fabrication process and double density. In these devices, the two-bit storage capability is achieved by storing the charge locally in the nitride layer in the vicinity of the source/drain junctions. A reverse read scheme allows for the detection of each single bit, provided the charge distributions are sufficiently spaced apart. Therefore, the characterization of the lateral distribution of the trapped charge is fundamental in understanding the scalability and retention properties of these concepts. In this work, the amplitude-sweep charge-pumping technique is applied to both the investigation of the electron distribution in the nitride under different injecting conditions and to the analysis of the charge distribution at high temperature. The lateral charge profile above the channel region is directly extracted from the measurements using a deconvolution-based procedure. The devices investigated consisted of a conventional n-channel MOSFET, manufactured using a 0.13 μm fabrication technology, which incorporates an oxide-nitride-oxide dielectric stack, consisting of a 7 nm thick thermally grown bottom oxide, a 10 nm nitride layer and a 8 nm thick deposited blocking oxide. Drained gate lengths ranging from 0.18 μm to 0.4 μm are considered, with effective channel lengths about 50 μm shorter. To investigate the effect of different injecting conditions, virgin samples have been programmed by channel-hot-electron injection changing the voltage and width of the gate pulse. Deviations from a steep rising edge shape of the charge-pumping signal are clearly sensed, which are indicative of localized trapped charge. Also, a marginal increase in the maximum charge-pumping current has been observed, indicating little to no creation of additional interface states. The trapped charge has been found confined in about 60 nm in the vicinity of the drain junction, while the peak of the distribution as well as its width increases with increasing programming pulse height and width. Electrons can diffuse from the initial trapping site under the influence of the concentration gradient and internal electric field. While no significant redistribution has been detected at room temperature over a period of a few weeks, a high-temperature bake enhances the lateral spread of the electron distribution. As the shape of the charge distribution changes, the charge-pumping signal modifies accordingly its rising edge. In principle, electrons can also leak away through the bottom or top oxide. However, their number, obtained by integration of the lateral distribution over the channel area, has been found practically constant during bakes up to 250°C, so that the sensed threshold voltage shifts appear to be solely determined by the lateral redistribution of the electrons in the nitride.
between the ONO defects and the back silicon interface through a thin tunneling oxide by either hot-carrier injection or Fowler-Nordheim tunneling. Leakage currents to the nitride and the substrate. We have developed a modified 'smart-cut' process to achieve the intended substrate: a single crystal silicon layer (10-15nm) formed on the silicon substrate by the hydrogen implantation. In SOI devices where the buried dielectric layer is of the order of a few hundreds of nanometers, the quality of the bonding interface may not be critical. However, in back-side tunneling memory devices, the channel width is varied from several microns to achieve the intended substrate: a thin single crystal silicon layer. [1] H. Silva and S. T. Wisan, "A nano-scale memory and transistor based on back-side trapping", Transactions on Nanotechnology, 3, 2 (2004).

10:30 AM *DL1.3 Integration and Performance Improvements of Silicon Nanocrystal Memories, Toshiro Hiramoto, II-Gweon Kim, Masumi Saitoh and Kousuke Yagadaira, Institute of Industrial Science, University of Tokyo, Tokyo, Japan.

Silicon nanocrystal memories are very promising for future non-volatile, high-density memory that can replace conventional floating gate memories. Although many research works have been reported previously on silicon nanocrystal memory, much more improvements of integration level, performance, and reliability will be achieved by proper optimizations of process and device structures. In this presentation, we will report (1) full process integration of silicon nanocrystal memory cells using advanced memory technology and (2) performance improvements of memory characteristics using ultra-small nano-scale SOI channel. Silicon nanocrystal memory cells with 4.6 F/cm² cell size on NOR type are successfully integrated. The cell size is 0.077 μm² using the 130 nm memory technology. This small cell size is achieved by the self-aligned contact process using landing plug polysilicon contact and direct tungsten hotline. Successful two-bit-per-cell operation is also achieved by local hot carrier injection into source/drain regions, that reduce with different threshold voltages. The reliability issues are significantly improved by properly fluorinated effect during the process. We have also investigated the dependence of memory characteristics on SOI channel structure. Tunneling oxide channel size and device with ultra-narrow channel, double-gate SOI channel, and single-gate ultra-thin body SOI channel are fabricated. In the ultra-narrow channel devices, the channel width is varied from several microns down to 5 nm. In the double-gate and single-gate devices, the channel thickness is varied from 2 to 4 nm. It is found that the threshold voltage shift, writing speed, and retention time are drastically improved when the SOI channel size (channel width in ultra-narrow devices and channel thickness in double/single-gate devices) becomes smaller. These results confirm that the silicon nanocrystal memories are scalable and promising for high-density memories.

11:00 AM DL1.6 Optimisation and Simulation of an Alternative Nano-flash Memory: The SASEM Device, Christophe Krezeminsky¹, Emmanuel Dubuc², Xiaohui Tang², Nicolas Reckinger², Andre Crayhay and Vincent Bauoy², 1ISEN, IEMN, Villeneuve d’Ascq, France, ²DICE, Université Catholique de Louvain, Louvain-la-Neuve, Belgium.

Since the conventional floating gate device is believed to be hardly scalable below the 65-nm technology node, alternative storage structures for nonvolatile memories are strongly needed. The feasibility to make a silicon-on-insulator nano flash memory device based on the nanocrystal memory concept from silicon nanocrystals in the arsenic doping concentration has previously been reported. The key processes involved in the fabrication are arsenic implantation, lithography and wet oxidation. The resulting device is a triangular MOSFET with a nanocrystal floating gate embedded in the gate oxide. Our objective is to improve the reliability of the process and to ensure the presence of the memory dot for various conditions. Furthermore, a clear understanding of the dot formation mechanisms and the degradation and failure effects or behavior under stress should be undertaken. We investigate the wet oxidation step in details using the generalised stress-dependent Deal and Grove approach. The various geometrical parameters (e.g dot surface, dot-channel distance...) of the nano-device have been simulated as a function of the oxidation temperature and the duration of this oxidation step. The time of oxidation is critical for the process reliability. We have shown that the dot shape and size is reduced by increasing the oxidation temperature. Furthermore, the impact of the oxidation temperature is different for different dot sizes. The study of the oxidation step is therefore a critical step to optimize the device performance. The oxidation temperature is used to control the size of the memory dot and the total thickness of the dielectric stack. The Simulation of the scaling issues and the impact on the various process parameters are the next priorities.

11:15 AM DL1.7 Formation of Ni Nanocrystals Embedded in HfO₂ and SiO₂ and Process Integration for Application in Nonvolatile Memories, Zelindia Y. L. Tan, S. K. Kumar Samanta, Won Jong Yoo and Sangjoo Lee; Electrical and Computer Engineering, National University of Singapore, Singapore, Singapore.

Flash memory using nanocrystals (NCs) as floating gate has received considerable attention because of its excellent electrical performance. Ni, despite its high work function (4.9 eV), high density of state and increasing popularity in CMOS processes, has not been studied for non-volatile memory applications. For higher programming efficiency and reduced charge loss, physically thick high-k materials with lower tunneling barriers have been proposed as an attractive alternative to conventional SiO₂. In this work, Ni nanocrystals were successfully formed on HfO₂ deposited by chemical vapor deposition and thermally grown SiO₂ using spincoating and rapid thermal anneal. Uniform and well separated Ni-NCs formed on both SiO₂ and HfO₂ were observed from Scanning electron microscopy (SEM) and X-ray photoelectron spectroscopy (AES). We found that the size and density of Ni-NCs on SiO₂ and HfO₂ can be controlled by the initial film thickness and annealing temperature. The size of the Ni-NCs is increased as the initial film thickness decreases. The smallest NC size (10nm) and highest NC density (2x10¹⁰ cm⁻²) was achieved at 600°C with 5nm initial thickness. At higher temperatures, NCs size is increased and density is decreased. During annealing, the elastic energy caused by the stress in the thin Ni film is relieved causing the film to rupture into islands on the dielectric surface. The dewetting of thin Ni films may also be attributed to the reaction of the metal absorbs to the oxygen in the substrate. The weaker bond enthalpy of Ni-Si (382 kJ mol⁻¹) compared to Hf-O (802 kJ mol⁻¹) and Si-O (799 kJ mol⁻¹), not only drives the three dimensional agglomeration of the Ni-NCs but also helps to ensure the chemical stability of Ni on HfO₂ and SiO₂. However, analysis of Ni-NCs mass loss on HfO₂ by AFM and X-ray photoelectron spectroscopy (XPS) shows that Ni diffuses into HfO₂ after anneal. This is detrimental to the device performance. By annealing in NH₃ ambient for dot formation, XPS analysis shows that the nitrogen content in HfO₂ is increased and the mass loss of Ni-NCs is reduced, implying that H₂N bonds block Ni diffusion in HfO₂ effectively. Nonvolatile memory devices using Ni-NC floating gate embedded in SiO₂ or HfO₂ were fabricated on p-type silicon substrates with 6nm tunnel oxide and 12nm control oxide with HfO₂ tunneling oxide, a 1V memory window was obtained with a 5V CV sweep compared to the control sample without Ni-NCs. Devices with Ni-NCs embedded in SiO₂, however, required a 10-12V CV sweep to achieve the same memory window. This is due to the lower tunneling barrier of 1.5eV compared to 3.5eV and improved coupling of the Ni-NCs to the channel due to the lower effective oxide thickness of HfO₂ (1.3nm) compared to SiO₂ (6nm). These results demonstrate the successfull integration of Ni-NCs for nonvolatile memory applications.
Germanium and SiO₂ interactions are important to a host of next generation electronics devices such as single electron transistors, optical waveguides, and flash memories. For flash memory devices, germanium passivation on insulator substrates is now being extensively studied as the charge storage elements because of higher carrier mobility and lower band edge when compared to Si particles. Many reports on the oxidation of Ge substrates and Si₁₋ₓGeₓ films have been published in the literature but remarkably few studies have been made on the interactions of Ge atoms or Ge films with insulator surfaces. In this work, a hot filament is used to thermally crack GeH₄ and deposit 0.5-20 ML Ge onto SiO₂ substrates. The substrates are 2-0.0 nm tunneling oxide SiO₂/Si(Si010) which are held at temperatures of 300-570 K during deposition. GeO₂ and GeO₂ desorptions are studied through temperature programmed desorption (TPD) experiments at 300-1100 K. Ge desorption spectra are complex exhibiting multiple desorption features. Low temperature features are attributed to GeO. No GeO₂ desorption features are observed. GeO formation results from Ge etching of the substrate as evidenced by monitoring the X-ray photoelectron spectroscopy (XPS) Si 2p peak area during exposure to a beam of Ge atoms at substrate temperatures above the Ge desorption peaks identified through TPD experiments. Guided by TPD peak temperatures, Ge bonding changes are also studied during annealing sets with XPS. These results explain why Ge nanoparticle growth is not observed after conventional low pressure chemical vapor deposition (LPCVD) on oxide substrates. Methods to modify the conventional LPCVD process and allow deposition of Ge on oxide substrates are discussed. Our findings could also be helpful in considering a number of other studies involving agglomeration of Si₁₋ₓGeₓ films on oxide materials.

11:45 AM D1.9
Low Voltage and High Speed Silicon Nanocrystal Memories.
Josep Carreras, B. Garrido, J. Arbiol and J. R. Morante; Electronics, University of Barcelona, Barcelona, Barcelona, Spain.

Si nanocrystals (Si-nc) used as charge storage nodes have demonstrated potential for both high speed and non-volatile memory applications. We have studied a set of MOS structures ion-implanted with Si at high doses (10, 15 and 20 atomic %) at projected range (25 nm) in which Si-nc has been precipitated by annealing at 1100 °C. The structural information of the device has been obtained by EFTEM, revealing the presence of a central layer of Si-nc, distributed with a mean size of about 2.65 Å ± 0.05 nm, a control oxide completely free of Si-nc of 12.5 nm, and a tunnel oxide of about 2.5 nm. This small tunnel oxide distance enables the direct tunnel mechanism, which is desired for high speed applications and reliability considerations, but also causes the stored charge to back-tunnel to the p-type substrate. This can lead to a zero gate leakage, typical retention times ranging from few hours to several months, depending on the concentration of Si-nc (Si excess). For developing low voltage memories we have focused on the highest Si excess sample, which shows long retention times (hours of microseconds) at very low gate fields (±2 MV/cm or ±6V). The onset of Fowler-Nordheim conduction has been estimated to be about ±0.6 MV/cm by J-V measurements, which means that the structure works in a direct tunnel regime, which is a must for reliable devices (no hot electrons). In order to increase the retention time, which diminish upon increasing the concentration of Si-nc (increasing Si excess) we have realized an additional annealing step in O₂ ambient for 16 and 32 minutes, resulting in a dramatic increase in the retention times, which is attributed to the growth of a high quality thin (1 and 1.7 nm respectively) tunnel oxide totally free of nanocrystals or Si clusters, Si excess and defects at the Si-SiO₂ interface. This additional oxidation step produces a decrease in the tunnel oxide thickness and an increase of the average distance between the nanocrystals and the Si substrate leads to a decrease of the tunneling current, which depends strongly on the thickness of the tunnel oxide. The increase in the retention time beyond the 10 years limit (in compliance with the current non-volatility standards) without compromising too much the writing speed, can be traded-off by increasing slightly the program voltage up to ±2.7 MV/cm. We have also demonstrated a Si-nc MOS cell, suitable for applications in which high speed and low voltages are specially required, with retention characteristics optimized to comply with the non-volatility standard definition.

SESSION D2: Ferroelectric Memories
Chairs: Hongsk Jeong and Tsu-Jae King
Tuesday Afternoon, November 30, 2004
Back Bay B (Sheraton)

11:30 AM D1.8
Influence of Thermal Treatments on the Chemistry and Self-Assembly of Nanoparticle Substrates
Scott K. Stanley, Shawn S. Coffee and John G. Ekerdt; Department of Chemical Engineering, The University of Texas at Austin, Austin, Texas.

Nonvolatile ferroelectric random access memories (FeRAMs) have received great attention in recent years because their writing speeds are much higher than those of Flash memories and their power consumption is much lower than those of other non-volatile memories. 1, 2 LSIs as large as 8MB have already been demonstrated and memories with Mbyte scale integration are now in production. These devices have the cell structure composed of one ferroelectric capacitor and one transistor that is similar to the DRAM cells. However, we can propose a structure that is a 3T type FeRAM cell, which is a candidate for nonvolatile FeRAM is the ferroelectric gate insulator. In this memory, the cell formed by the tunneling oxide is incorporated into a FeRAM technology.

2:00 PM D2.3
Step Coverage and Composition of Pb(Zr,Ti)O₃ Capacitors Prepared on Sub-Micron Three-Dimensional Trench Structure by Metalorganic Chemical Vapor Deposition.

For high-density integration of ferroelectric random access memory (FeRAM), three-dimensional (3-D) capacitor structures should be realized. Metalorganic chemical vapor deposition (MOCVD) is one of the most suitable techniques for conformal deposition of the films on the 3-D structures. There have been numerous reports on MOCVD films for FeRAM application. However, not much work of MOCVD study has been reported on the sub-micron trench structures, which are widely accepted as the most feasible structures for high density FeRAM. In the present study, Pb(Zr,Ti)O₃ films, a promising material for high-density FeRAM, were deposited into narrow trenches by MOCVD. Polycrystalline PZT films were deposited directly on SiO₂/TiAIN/Ti/Si substrates having a trench structure. In general, the standard reaction conditions of Pb(Zr,Ti)O₃ by MOCVD with high liquid delivery rates and low film growth rates were used. Pb(DPM)₄, Zr(MMP)₄ and Ti(MMP)₄ were used as Pb, Zr and Ti source materials, respectively. Ethylcyclohexane and O₂ gas was also used as a solvent and an oxidant, respectively. The liquid sources were vaporized at individual vaporizers and mixed before introduced into a cold-wall flow reactor. The coverage properties of the PZT films in SiO₂ trenches were observed by scanning electron microscopy (SEM) and transmission electron microscopy (TEM). Composition distribution of the PZT films was also investigated by energy dispersive x-ray spectroscopy (EDS) attached to TEM. In this study, the composition of the PZT films in the SiO₂ trenches was monitored along the interface. The PZT films were fabricated on the 3-D structured PZT capacitors. In this study, the composition of the PZT films in the SiO₂ trenches was monitored along the interface.
Ru films was achieved as high as 90 %. This result implies that Ru-based films can be adopted not only as the bottom electrode but also as an interlayer between the bottom and middle electrode layers of PZT films with higher aspect ratio. When 35 nm-thick PZT films were deposited at 450 °C directly on SiO₂ trenches with the aspect ratio of 1.8:1 (the opening width and depth were 250 and 440 nm, respectively), the leakage current was low with leakage current density of 7.6-7.5 × 10⁻⁵ A/cm². In addition, a significant change of EDS peak intensity of PZT constituent elements was not observed along the depth direction at the sidewall of the SiO₂ trench. Almost the same values of the effective step height could be obtained from the deposited Ru films.

These results suggest that uniformity of film thickness can be obtained within a wide deposition temperature region from this source materials combination.

2:15 PM D2.3
δ-Nb-doping Effect to the Interface Between IrO₂ Top Electrode and Pb(Zr,Ti)O₃ by Metal Organic Chemical Vapor Deposition (MOCVD)
Tatsuo Matsushita1, Masami Nakabayashi2, Yoshimasa Horii2 and Yoshihiro Sugiyama1,2, Fujitsu Laboratories Ltd., Atsugi, Japan; 2Fujitsu Limited, Atsugi, Japan.

Ferroelectric Random Access Memory (FRAM) has advantage of high speed and low power consumption nonvolatile RAM, suitable for embedded memory, mobile use with high security. Considering larger-capacity memory, metal organic chemical vapor deposition (MOCVD) method should be necessary to form 3-dimensional ferroelectric capacitors, because low film porosity, thinner film controllability and good step coverage can be expected. Interface control between electrodes and ferroelectrics is essential role for the issues of leakage current (Pr), low leakage current density, high endurance to thermal imprint and fatigue free behavior. In this study, we investigate Nb-doping effect on electric characteristics using uniformly Nb-doped Pb(Zr,Ti)O₃ (Undoped-PZT) and δ-Nb-doped PZT (DND-PZT) on IrO₂/PZT by low pressure MOCVD. We used precursor of Pb(DMP)₂, Zr(DMHD)₄, Ti(OPR)₂(DMP)₂, Nb(DMP)₃ diluted with THF. The source gases were regulated by liquid delivery system using vaporizer. The substrate temperature was set at 620°C. Highly oriented PZT was deposited on Ir/Ti/SiO₂/Si and had good ferroelectric characteristics as well as high endurance for imprint [1]. The PZT showed (111) preferred orientation measured by XRD. The composition of PZT was controlled at the Pb/Zr/Ti ratio of 40/56/4/0. Nb concentration (Nb/(Zr+Ti+Nb)) was 0 to 5 × 10⁻². The total thickness of PZT was controlled to 120nm including 0-20nm of DND-PZT. First, we investigated the Undoped-PZT capacitors to reveal the influence of Nb-doping. Increasing the Nb concentration, hysteretic curve shifted positively and a leakage current density decreased by one or two order at lower bias (≤1.8V). The shift suggests the existence of negative charge that increases the potential barrier for electron. The Pr decreased as increasing Nb concentration, which is caused by the decrease of the degree of tetragonal crystal as perovskite structure. Secondly, we investigated the ferroelectric capacitors with a DND-PZT. This capacitor structure also suppressed the leakage current by about one order as compared to undoped PZT capacitor and decreased Pr slightly. Thirdly, δ-Nb-doping to the top IrO₂ electrode/PZT interface is effective to decrease the leakage current without decreasing Pr. Increasing Nb concentration, the leakage current with negative higher bias region (≤2V) increased. This asymmetrical behavior increased with increasing fraction of Nb-doping region. Since this behavior was also observed with UND-PZT, asymmetrical potential profile along growth direction can exist, which can be caused by defects related to PZT constituents. In summary, δ-Nb-doping at the interface between IrO₂ top electrode and PZT is effective to decrease the leakage current maintaining almost the same Pr for nondoped PZT. [1] Y. Horii et al., IEDM2002, p.539

2:30 PM D2.4
Quantifying the Role of Electronic Charge Trap States on Imprinting Behavior in Ferroelectric Poly(pentadieene fluoro-trifluoroethylene) (P(VDF-TrFE)) Thin Films.
Connie Lew and Michael O. Thompson; Materials Science and Engineering, Cornell University, Ithaca, New York.

P(VDF-TrFE) ferroelectric thin films are a promising material for non-volatile memories. Fatigue, the loss of polarization with switching cycles, and imprint, the time-dependent tendency to resist polarization re-inversion, are key limitations that must be understood and minimized. Based on experimental measurements of the time and temperature dependence of imprint, we have investigated possible scenarios that link imprint, and potentially fatigue, to electronic charge trap states in the polymer. To quantify and characterize the density and dynamics of these traps, we have developed a fast-ramp thermally stimulated current (TSC) measurement technique suitable for monitoring the trap state dynamics within the seconds-time frame. Thin films of P(VDF-TrFE) with metal electrodes were fabricated on oxidized Si substrates. Following controlled polarization, fatigue, and imprint initialization, trap states were thermally filled/emptied through temperature cycling between 20-120°C with heating and cooling rates of 1-5°C/min. The density of trap states was then determined during thermal cycling, the final polarization state of the thin films was also determined. Imprint-induced filling of trap states has been verified from the TSC in the 1-1000 second time-frame. Similarly, thermally induced trap filling has been directly correlated with post-cycling imprint conditions. In addition, results show a significant asymmetry with field orientation (top versus bottom electrodes), suggesting that the trap density and characteristics are directly related to processing conditions and electrical dipoles within the films.

3:15 PM D2.5
Ferroelectric 1-T Memory Device – Will it be Viable for Nonvolatile Memory Application? Jin-Ping Han,1 Semiconductor Electronics Division, NIST, Gaithersburg, Maryland; 2IBM T.J. Watson Research Center, Yorktown Heights, New York.

The quest for a nonvolatile memory FET based on the metal-ferroelectric-semiconductor(MFS) or metal-ferroelectric-Insulator-semiconductor(MFIS) gate stack has greatly intensified in recent years because of the successful demonstration of ferroelectric thin films that can be integrated with Si-based CMOS technology. In principle, such a memory device could be building block for an ideal memory technology that offers random access, high speed, low power, high density and non-volatility. In practice, however, so far none of the reported ferroelectric memory transistors has achieved a memory retention time of more than a few days, a far cry from the 10-year retention time requirement for non-volatile memory devices. A close look at the device operation reveals two major causes of the short retention. (1) depolarization fields; (2) finite gate leakage current and its associated charge trapping. The origin of these problems can be understood from the semi-quantitative results of these analysis should help to illustrate the practical difficulties in attempting to realize a non-volatile 1-T memory device based on ferroelectrics. It will be revealed that grain size, surface roughness, thickness variation, interfacial properties, and crystallinity of the annealed ferroelectric SrBi₂Ta₂O₉ (SBT) films have a strong impact on the size of the memory window, as does the choice of the buffer layer material. The aspects of the use of SiN as a buffer layer sandwiched between the SBT and the Si substrate will be discussed; it’s interesting to note that the switching of polarization of the ferroelectric SBT plays a key role for both the ferroelectric nonvolatile memory dominated and the trapping dominated memory windows. Two possible solutions have been proposed to circumvent problems associated with the finite retention time in ferroelectric FET-type memories: (1) Refresh it as FEDRAM cell, (2) Single-crystallize the ferroelectric film. Acknowledgements The author would like to thank NIST office of Microelectronics Programs for financial support and Drs. E. Vogel, C.A. Richter, S-M. Koo at NIST for their insights and discussion. Part of the work was done at Yale University. The author would also like to thank Profs T.P. Ma, C.C. Badroide, K-H. Kim, Tomin Y. J. Zhu, Z.J. Luo, Mr. Y.X. Liu, Mr.C.J. Xie for their help and support.

3:45 PM D2.6
Non-volatile thin film transistors using ferroelectric/ITO structures. Eisuke Yokumitsu and Masanori Senoo; Precision and Intelligence Lab., Tokyo Institute of Technology, Yokohama, Japan.

In this presentation, we report ferroelectric-gate thin film transistors (TFTs) using indium tin oxide (ITO) as a channel material. Ferroelectric-gate field-effect-transistors (FETs) are promising for future nonvolatile memory applications. However, it is difficult to fabricate ferroelectric-gate FE FETs because ferroelectric and electrical properties of silicon substrates because of the interaction between silicon and ferroelectric materials. In addition, mismatch between ferroelectric polarization and channel charge of silicon-based FE FETs makes it more difficult to obtain good electrical properties. On the other hand, the ferroelectric-gate TFTs using conductive oxides as channel materials were already reported. However, the reported drain current on/off ratios is usually very small. In this work, we report nonvolatile memory operations of ferroelectric-gate TFTs using ferroelectric/ITO structures which have the drain current on/off ratio of more than 10³. Bottom-gate structure TFTs have been fabricated using ferroelectric Bi(4-x)LaₓSi(3)O(12) (BLT) or Pb(Zr,Ti)O(3) (PZT) films, and ITO channel. Ferroelectric and ITO layers were formed by the sol-gel technique and RF sputtering, respectively. The channel length of the fabricated devices was varied from 40 to 120um. Drain current-drain voltage (ID-VD) characteristics of both BLT/ITO and PZT/ITO ferroelectric-gate TFTs exhibited a good n-channel operation with clear current saturation. On-current as large as 1mA can be obtained for the BLT/ITO TFT when the applied gate voltage is 8V. Furthermore, drain current-gate voltage (ID- VG) characteristics demonstrate clear counterclockwise hysteresis loop due to the
ferroelectric gate insulator. The obtained memory windows are 4V and 2V for BLT/ITO and PZT/ITO structure devices, respectively. The on/off current ratio is more than 1000 for both BLT/ITO and PZT/ITO devices, which indicates that the ITO channel is sufficiently depleted by the ferroelectric polarization.

4:00 PM D2.7
Solution-Processed Polymeric Ferroelectric Field Effect Transistors. Ronald Naber1, Paul Blom1, Gerwin Gelink2, Alwin Marsman1 and Dago de Leeuw2; 1Materials Science Centre, University of Groningen, Groningen, Netherlands, 2Philips Research Laboratories, Eindhoven, Netherlands.

Field-effect transistors (FETs) with ferroelectric gate insulators are attractive for use as non-volatile memory elements. Their application has been strongly hampered by a relatively low on/off modulation (<100) and short retention (few days). In a recent all-organic ferroelectric FET with evaporated pentacene as semiconductor an on/off modulation of 50 has been achieved, with a retention time of a few hours (Ambrosius et al., 2007). In the present study we demonstrate polymeric ferroelectric FETs with all the active layers deposited by spin coating. In these devices the ferroelectric poly(vinylidene fluoride/ trifluoroethylene) is combined with a bisalloy-substituted poly(phenylene vinylene) as semiconductor. The polymeric ferroelectric FETs have modulation ratios > 104, exceeding the state-of-the-art (both organic and inorganic) with two orders of magnitude. Furthermore, initial studies demonstrate that this high modulation ratio is unaffected after 24 hrs. Combined with a read/write operation within 1 ms these devices are a major step forward towards applications as memory elements in low-cost electronic circuits for electronic barcodes or display driver logic.

4:15 PM D2.8
Selection of ferroelectric/high-k gate stack combination for optimized FeFET performance. Shen Xu1, Matteo Viapiana1,2, Matteo Viapiana1,2,

For the possible application of ferroelectric field-effect transistor (FeFET) type memories in embedded RAM applications, the scaling possibility towards future CMOS generation is a crucial property. One target is to obtain sufficient memory window at low operation voltage. Optimization of the gate stack material properties (dielectric constant and thicknesses) is needed to get proper voltage division over the ferroelectric layer. We have studied different gate stack combinations of SBT (SrBi2Ta2O9) and BLT (Bi (4-x) La4Ti3O12) films on Al2O3/SiO2, HfO2/SiO2 or SiO2 insulator in Metal-Ferroelectric-Insulator-Silicon (MFIS) test structures. We have investigated Bi-layered perovskite films for the ferroelectric films as they have lower dielectric constant than e.g. PZT (Pt/(x)La2O3(x)SiO2) and as the highest polarization charge is not desired in FeFET application. The use of the high-k layer can be beneficial both as material diffusion barrier and by offering a lower total equivalent oxide thickness (EOT) that could be obtained by SiO2 or SiO2+HfO2. Therefore, as high ferroelectric charge switching at the ferroelectric/insulator interface may induce breakdown for too thin SiO2 films. We evaluated Al2O3/SiO2, HfO2/SiO2 as these are the gate stacks currently in development for the scaled CMOS devices. 6 nm HfO2 or 6nm Al2O3 is deposited by ALD on top of a 0.5 nm wet chemical SiO2, and 1 nm Rapid Thermal Oxidation SiO2, resulting in a total EOT of 2 nm to 5 nm after the ferroelectric film crystallization anneal. The ferroelectric films were deposited by MOCVD (SBT) or spin-on (SBT, BLT) techniques, and different crystallization treatments (700-780°C) as well as film thicknesses (120-240 nm) were explored. The evaluation was based on both conventional high-frequency CV and pulsed-CV techniques to clarify the relative roles of trapping and true ferroelectric response. It was found that using the Al2O3/SiO2 insulator, strong trapping phenomena inhibit proper operation, while good ferroelectric performance is obtained on HfO2/SiO2. The relevant material properties, Pr and EOT of high-k/SiO2 are calculated from the electrical response and used in a simulation model to predict the optimal stack configuration for low-voltage operation. Optimized stack performance will be presented.

4:30 PM D2.9
Effect of Ferroelectric/HfO2/Si Structures on Electrical Properties of Ferroelectric-gate FETs. Koji Aizawa1, Byung-Eun Park2, Yoshikito Kawashima2, Kazuhito Takahashi and Hiroshi Ishiwara1; 1Precision & Intelligence Laboratory, Tokyo Institute of Technology, Yokohama, Japan; 2Department of Electrical and Computer Engineering, University of Seoul, Seoul, South Korea; 3Interdisciplinary Graduate School of Science and Engineering, Tokyo Institute of Technology, Yokohama, Japan.

Electrical properties of the p-channel metal-ferroelectric-insulator-silicon field effect transistors (MFIS FETs) using Pt/SrBi2Ta2O9(SBT)/HfO2/Si and Pt/(Bi0.5La0.5)TiO3(BLT)/HfO2/Si gate structures were investigated. An HfO2 film as a buffer layer was deposited by a modified electron-beam evaporation method, and then annealed at 800°C in an oxygen ambient. The physical thickness of HfO2 film is presumed to be approximately 10nm. 400-nm-thick SBT and BLT films were deposited on an HfO2 buffer layer by sol-gel method. The channel width and channel length of the fabricated MFIS FETs were 50μm and 5μm, respectively. Typical drain current vs. gate voltage characteristics of the fabricated MFIS FETs with SBT/HfO2 and BLT/HfO2 structures showed a single hysteresis curve and ferroelectric polarization reversal of the ferroelectric films. The memory window (the width of the hysteresis loop) was approximately 1.0V in the SBT/HfO2 structures and it was approximately 0.5V in the BLT/HfO2 structures, when the gate voltage was swept between -5V and +5V. The data retention characteristics of the MFIS FETs with the SBT/HfO2 and BLT/HfO2 structures were measured after applying the single "write" pulse of either +10V or -10V in amplitude and 1μs in width. The current on/off modulation ratio is unaffected after 24 hrs. Combined with a read/write operation within 1 ms these devices are a major step forward towards applications as memory elements in low-cost electronic circuits for electronic barcodes or display driver logic.

4:45 PM D2.10
Device Structures and Characterization of One Transistor Ferroelectric Memory Devices. Tingkai Li, Sheng Teng Hsu, Bruce Ulrich and David Evans; PTI, Sharp Labs. of America, Inc., Camas, Washington.

For the possible application of ferroelectric field-effect transistor (FeFET) type memories in embedded RAM applications, the scaling possibility towards future CMOS generation is a crucial property. One target is to obtain sufficient memory window at low operation voltage. Optimization of the gate stack material properties (dielectric constant and thicknesses) is needed to get proper voltage division over the ferroelectric layer. We have studied different gate stack combinations of SBT (SrBi2Ta2O9) and BLT (Bi (4-x) La4Ti3O12) films on Al2O3/SiO2, HfO2/SiO2 or SiO2 insulator in Metal-Ferroelectric-Insulator-Silicon (MFIS) test structures. We have investigated Bi-layered perovskite films for the ferroelectric films as they have lower dielectric constant than e.g. PZT (Pt/(x)La2O3(x)SiO2) and as the highest polarization charge is not desired in FeFET application. The use of the high-k layer can be beneficial both as material diffusion barrier and by offering a lower total equivalent oxide thickness (EOT) that could be obtained by SiO2 or SiO2+HfO2. Therefore, as high ferroelectric charge switching at the ferroelectric/insulator interface may induce breakdown for too thin SiO2 films. We evaluated Al2O3/SiO2, HfO2/SiO2 as these are the gate stacks currently in development for the scaled CMOS devices. 6 nm HfO2 or 6nm Al2O3 is deposited by ALD on top of a 0.5 nm wet chemical SiO2, and 1 nm Rapid Thermal Oxidation SiO2, resulting in a total EOT of 2 nm to 5 nm after the ferroelectric film crystallization anneal. The ferroelectric films were deposited by MOCVD (SBT) or spin-on (SBT, BLT) techniques, and different crystallization treatments (700-780°C) as well as film thicknesses (120-240 nm) were explored. The evaluation was based on both conventional high-frequency CV and pulsed-CV techniques to clarify the relative roles of trapping and true ferroelectric response. It was found that using the Al2O3/SiO2 insulator, strong trapping phenomena inhibit proper operation, while good ferroelectric performance is obtained on HfO2/SiO2. The relevant material properties, Pr and EOT of high-k/SiO2 are calculated from the electrical response and used in a simulation model to predict the optimal stack configuration for low-voltage operation. Optimized stack performance will be presented.

SESSION D3: Poster Session: Ferroelectric II

Chairs: Yoshihisa Fujisaki and Jon Slaughter
Tuesday, November 30, 2004
8:00 PM
Exhibition Hall D (Hynes)

D3.1
Improvement of Ferroelectric and Electrical properties of Sol-Gel Deposited BiTiO3 Thin Films by Multiple Rapid Thermal Annealing Techniques. Hua Wang, Department of Information Material Science and Engineering, Guilin University of Electronic Technology, Guilin, Guangxi Province, China.

Ferroelectric Bi4Ti3O12 (BIT) thin films were fabricated by sol-gel method and multiple rapid thermal annealing (MRTA) techniques on Pt/Ti/SiO2/p-Si substrates. The effects of annealing temperature and time on the crystallinity, the ferroelectric and electrical properties of Bi4Ti3O12 films derived by MRTA and by normal RTA were investigated. BIT films were polycrystalline and their x-ray diffraction
patterns exhibited peaks corresponding to the (117), (004), (008), and (111) reflections of the perovskite phase of BIT. The grain size and the roughness of surface increase with the annealing temperature, but the maximal remnant polarization of Bi4Ti3O12 films come forth when the annealing temperature is 650°C. The perovskite-phase of BIT thin films were formed at lower annealing temperature and smaller grain size were obtained in the BIT thin films prepared by MRTA compared with that by normal RTA. The typical values of remnant polarization of Bi4Ti3O12 films derived by MRTA was 11 μC/cm², which was higher than that derived by conventional RTA about 15%. While the leakage current density was 8.9 x 10⁻⁸ A/cm² by MRTA, which was lower than that by normal RTA about 90%.

D3.3 Characterization of MFMS and MFIS Structures for Non-volatile Memory Applications. Morisui, R., Aoba, Y., Koda, T., Uchida, H., Nakaki, H., Funakubo, H., Yamaji, S., and Nishikawa, Y., 1Department of Chemistry, Sophia University, Tokyo, Japan; 2Department of Innovative and Engineered Materials, Tokyo Institute of Technology, Yokohama, Japan.

To eliminate the interface reaction problems in MFMS (metal-ferroelectric-semiconductor) and MFIS (metal-ferroelectric-insulator-semiconductor) structures, a gate layer sandwich of the MFIS structure consisting of Pt-SBT-Pt-ZrO2-SiO2-Si stacks. In the MFMIS structures, since the fabricated devices have access to the floating capacitor through a metal as inter diffusion barrier. Therefore, the MIS capacitor with SiO2 and ZrO2 as an insulator with excellent performance of the switching polarization (Pc) down to 15°.

D3.3.3 Improvement of Ferroelectric Properties of Lead Zirconate Titanate Thin Films by Ion-substitution Using Various Rare-earth Cations. Hiroshi Nakaki1, Hiroshi Uchida1, Shoji Okamoto2, Shinataro Yokoyama3, Hiroshi Funakubo4, and Seiichiro Koda5, 1Department of Chemistry, Sophia University, Tokyo, Japan; 2Department of Innovative and Engineered Materials, Tokyo Institute of Technology, Yokohama, Japan.

Authors attempted the improvement of ferroelectric properties of PZT films by promoting the anisotropy of simple-perovskite crystal. Crystal anisotropy of PZT was controlled by the species and occupying site of substituent cation. B-site substitution using rare-earth cations whose ionic radii locate on bigger part of its series (such as Y³⁺, Gd³⁺, Dy³⁺, Yb³⁺, etc.) can promote the anisotropy of PZT crystal, i.e., the ratio of PZT lattice parameters (c/a), whereas inverse phenomenon occurs in the case of A-site substitution using rare-earth cations whose ionic radii locate on larger parts of its series (such as La³⁺, Nd³⁺, etc.). In this study, authors investigated the influences of the B-site substitution using some rare-earth cations on the properties of PZT films in order to confirm whether controlling the crystal anisotropy using rare-earth cation is effective for improving the ferroelectric properties. PZT-based films were fabricated by a chemical solution deposition. Spin-coating solutions with chemical compositions of Pb₁₋₅La₂ₓ(ZrxTi₁₋ₓ)O₃ were prepared by lead acetate, zirconium iso-propoxide, rare-earth (Ln: Y, Gd, Dy and Yb) nitrates and Pb₂⁺, Ti⁴⁺, so that the Pb₂⁺-deficiency and lower-valent cation doping respectively. We propose a simple model to describe two major microscopic scenarios for the suppression of the switching polarization (Pc) in Pb(Zr,Ti)O₃ films.

Yb³⁺-substituted PZT films (y = 5 x 10⁻⁵ - 5 x 10⁻⁴ A/cm²) were larger than those of Y³⁺, Gd³⁺ and non-substituted PZT films (y = 10⁻⁴ A/cm²). The degradation of ferroelectric properties at Gd³⁺ and Yb³⁺-substituted PZT films in the leakage current densities derived from Pb⁺⁺-deficiency and lower-valent cation doping respectively. We concluded that ion substitution using some rare-earth cations such as Yb³⁺ and Dy³⁺ is one of promising technology for improving the ferroelectric properties of PZT thin film.
concluded than in spite of the good performance due to the favorable environment for the growth of Pt system provided by the textured LSCO, higher interface energy and a better control of composition it is necessary to improve its fatigue behavior.

D3.8 Excimer (XeCl) Laser Annealing of PbZr0.52Ti0.48O3 Thin Film at Low Temperature for TFT FRAM Application. Wenwu Xianyu1, Takashi Noguchi1,2, Hans Cho3, Jangyeon Kwon1 and Huoxing Yin1,1, Samsung Advanced Institute of Technology, Suwon, Gyunggi-Do, South Korea; 2Samsungkyun University, Suwon, Gyunggi-Do, South Korea.

SoG (system on glass) technology is being developed to integrate multiple electronic functions onto glass substrates, with the final applications being mirror-type displays and sheet-like computers. For these mobile internet-capable SoG applications, the key requirements are nonvolatile functionality, low power consumption, minimal added process complexity and compatibility with LTPS (low-temperature poly-silicon) technology. Ferro-electric random-access memory (FRAM) is a promising candidate for SoG memory devices because of its high access speed, low power consumption and simple two-mask process. In this study, we successfully produced PbZr0.52Ti0.48O3 (PZT) thin films with high crystallinity and high remanant polarization at low process temperatures using pulsed excimer laser (XeCl) irradiation. We also propose a new technology for fabrication of thin film transistor (TFT)-driven FRAM devices. In our experiments, amorphous PZT films were prepared on Pt/Ti/SiO2/Si substrates by a sol-gel method. A two-step process was used to crystallize the amorphous thin films; the films were then laser annealed at 550 oC for 5 minutes. Laser annealing is necessary to transform the PZT perovskite phase and then annealed with a XeCl excimer laser at 400 oC in a 120 Torr nitrogen gas atmosphere. Laser energy density was varied from 100 to 600 mJ/cm2 per pulse (pulse laser with a width of 180 fs). It was confirmed that laser-annealing drastically improved the crystallinity of the PZT film, crystallizing it into the perovskite phase and not the pyrochlore phase. SEM photographs show that the PZT thin film has uniform-sized crystal grains. The ferroelectric properties were found to depend on the laser energy density, shot number, and gas pressure. Before the laser annealing, the films show hysteresis loops with low remanent polarization (Pr) and the loops do not saturate. After laser annealing, the films show saturated hysteresis loops, with the Pr increasing from 2.2 µC/cm2 to 23.9 µC/cm2.

D3.9 Optimization of the ferroelectric film for application in scaled FeFET. Matteo Viapiana1,2, Zhen Xu1, Ludovic Guox1, Ben Kaczer1, Guido Groeseneken1,2 and Dirk Wouters3, 1SPOT, IMEC, Leuven, Belgium; 2ESAT-INSYS, KULeuven, Leuven, Belgium.

For the proper operation of a ferroelectric field-effect transistor (FeFET), both the electrical and structural properties of the ferroelectric film are of crucial importance. Relevant material properties are remanent polarization (Pr), remanent polarization evaluated to be 130 mC/m2, coercive field and the dielectric constant. As the ferroelectric materials are crystalline and the remanent polarization is a function of the crystal orientation and size, distribution are important parameters especially towards further technology scaling. In this work, we characterized SBT (SrBi2Ta2O9) and BLT (Bi1-xLa1xTi3O12) films deposited on Al2O3/SiO2 and HfO2/SiO2 insulator stacks or directly on SiO2 insulator, for their application in the Metal-Ferroelectric-Insulator-Si (MFIS) gate stack of a FeFET-based memory. The SBT and BLT films are deposited by spin-on followed by low temperature heat treatments for drying and pyrolysis, and is repeated for making thicker films. The final crystallization is done using a rapid thermal anneal (RTA) system. The electrical performance of the films was derived from high-frequency C-V evaluation of MFIS capacitor structures, and compared with that of Pt/FeFET/FePt-metal-insulator-metal (MIM) capacitor structures using the same FE deposition process. It was found that good electrical properties of the MFIS structures could only be obtained at the higher crystallization temperature (~780°C), compared to~450°C for FE films directly deposited on Pt substrates, pointing to a more difficult nucleation on the metal oxide films. On the other hand, the value of the remnant polarization (Pr) as indirectly derived from the C-V measurements is much lower (~20% compared to that obtained on MIM capacitors. Also, the MFES structure on Al2O3 showed strong trapping behavior that may indicate a poor interface with the ferroelectric layer. The full electrical and structural characterization of the FE film is the current status and will be reported, and the results of SBT and BLT will be compared.

D3.10 Improvements in Electrical Properties of Hydrogen-Treated Ferroelectric Capacitors with PtOx Top Electrode for Memory Applications. Chun Kai Huang and T'ai-Bor Wu, Material Science Engineering, Material Science Engineering, Hsinchu, Taiwan.

The electrical properties of reactive sputtered PtOx were characterized by forming gas annealing at 700°C. PtOx/PEO/Pt film structure was formed using a high vacuum deposition without thermal decomposition. The structures, molecular orientation and surface morphology depend on the deposition parameters (substrate temperature, substrate species). The relative dielectric constant of the central oriented VDF oligomer films was estimated to be about 2.0 in the frequency range from 0.1 Hz to 1 MHz in room temperature. A rectangular polarization hysteresis loop was observed in well-ordered VDF oligomer thin films, and the remnant polarization evaluated to be 130 mC/m2, which is the largest value among organic molecules. Fatigues of polarization-field hysteresis loop along with an increase of leakage current density were observed from Pt to PtOx top electrode. The leakage current of the degraded capacitors was measured to be 0.05 µA/cm2 after 60s bias annealing, resulting in the barrier height reduction. The secondary ion mass spectroscopy and elastic recoil detection analysis reveal that the high density defects were created by the catalytic reaction on the Pt surface and originated mainly at the interface of PtOx and Pt electrodes. Pitting between domains and defect sites due to charged defects is suspected to dominate the initial stage of the degradation. The relationship between the defect density and barrier height is in good quantitative agreement with the Schottky barrier height model.

D3.11 Complex Oxide Nanostructures by Pulsed Laser Deposition through Nanostencils. Cristiano Victor Cojocaru, Catalin Harnagea, Federico Rosei and Alain Pignolet; INRS-EMT, Universite du Quebec, Varennes, Quebec, Canada.

A flexible method for simultaneous nanoscale structures fabrication and patterning is described, using a combination of stencil mask and pulsed-laser deposition (PLD) techniques [1, 2]. A miniature shadow-mask with nano-apertures in a very thin microfabricated membrane (nanostencil) was first manufactured and then, mechanically attached to the substrate of choice. To create free-standing membranes with arrays of apertures of different shapes and dimensions below 500 nm, a combination of advanced lithography and high precision ion milling by focused-ion-beam (FIB) and silicon micromachining techniques was used. Using PLD, complex oxides such as BaTiO3 and BiFeO3 were deposited directly through the stencil’s holes onto various substrates (Si, Pt, SrTiO3 and SrRuO3). Ordered arrays of nanomachined apertures were used to create a stencil deposition step, which replicate the aperture pattern in the stencil membrane. The morphology and composition of these nanostructures were characterized by scanning electron microscopy (SEM), atomic force microscopy (AFM) and X-ray photoelectron spectroscopy analysis. The ferroelectric properties of the patterned structures of different sizes were investigated by AFM piezoresponse method in order to...
study size effects in ferroelectrics. Pulsed laser deposition parameters as well as the geometrical attachment of the stencil onto the substrate are important factors that must be tuned during the process in order to increase the steepness of the structures. Several other issues related with the deposition process such as large scale uniformity and periodicity of deposited nanostructures across the substrate and the substrate's life must be investigated and discussed. This approach offers a simple, reliable, parallel method for growing, patterning and positioning ferroelectric functional nanostructures on various substrates, which is of wide interest for applications in electronics, for information storage applications in Ferroelectric Random Access Memories (FeRAM). It also represents a promising "tool" for local deposition of multiple geometries and high-purity nanostructures under high-vacuum or ultra-high vacuum conditions, in laboratories without expensive lithography equipment. [1] Jürgen Brügger et al. Microelectronic Engineering 53 (2000) 403 [2] Emiel A. Speets et al. Nano Letters, vol.4, no.5 (2004) 841-844

D3.11 Leakage Current and Ferroelectric Response of Bi1-xNdxTiO312 Thin Films. Maharaj S. Toman1, R. E. Melgarro2, R. P. Guzman3, Subhasish Basu Majumder4 and R. S. Katsyay5; 1Department of Physics, University of Puerto Rico, Mayaguez, Mayaguez, Puerto Rico.; 2Physics Department, University of Puerto Rico, San Juan, San Juan, Puerto Rico.

In the past few years, Nd substituted bismuth titanate spin coated films have shown large free giant ferroelectric response, but there is a lack of information on their leakage current response. Bi1-xNdx TiO312 films were prepared by sol-gel process and thin films were deposited by spin coating on Pt (Pt/TiO2/SiO2/Si) substrate. Top Pt electrode was evaporated and the room temperature leakage current was measured on the films with compositions x = 0.00, 0.06, 0.36, 0.56, and 0.75 in Pt/film/Pt capacitor configuration. Films were prepared under similar conditions and in each case the film thickness was 0.75 μm. The measured leakage current in pure Bi1TiO312 film (x = 0.00) was much lower in comparison with Nd substituted films. The lowest leakage current (less than 10-10 A) was observed in the film with composition x = 0.75. The leakage current behavior could be explained by defect density and grain size. Ferroelectric response presented for different composition shows the highest polarization for the composition x = 0.56. These results indicate the potential application of Nd substituted bismuth titanate films in non-volatile ferroelectric memories. [This work is supported by DoD-ONR Grant No. N00014-02-1-0215, and is gratefully acknowledged.]

D3.12 Dielectric and Fatigue Properties of PZT Thin Films Prepared From Oxide Precursors Method. Silvia T. Subbattula-Kagesawa1, Cristiano A. Gunary1, Eudes B. Araujo2 and Nobuo Oki1; 1Engenharia Elétrica, Universidade Estadual Paulista, Ilha Solteira, SP, Brazil; 2Física e Química, Universidade Estadual Paulista, Ilha Solteira, SP, Brazil.

Fatigue is a serious problem for a ferroelectric film to overcome for non-volatile memory applications. Fatigue, the remnant polarization and coercive field properties degrade with cycles increasing on hysteresis loops. The reasons have been attributed to different mechanisms such as a large voltage applied on ferroelectric film at high temperature in Ferroelectric Random Access Memory (FeRAM) or memories for digital storage in computer, grain size effects and others. The aim of this work is to investigate the influence of the crystallization kinetics on dielectric and ferroelectric properties of the P(x)zr012, (x)Ti03, (y)ZrO2 (PZT) thin films prepared by an alternative chemical method denominated Oxide Precursor Method. Films were crystallized air atmosphere on Pt/TiO2/SiO2/Si substrates at 700°C for 1 hour, using a conventional furnace, and at 700°C for 15 min, using a rapid thermal annealing (RTA) process. Final films were crack free and presented 1 μm in thickness in average. Dielectric properties were studied as a function of frequency from 100 Hz to 1 MHz. Films crystallized from RTA shows a dielectric dispersion at low frequency but PZT film crystallized in conventional furnace this dispersion disappear. Ferroelectric properties were measured from hysteresis loops at 10 kHz. The obtained remanent polarization (Pr) and coercive field (Ec) were 3.2 μC/m2 and 53 kV/cm film crystallized in conventional furnace and in films crystallized from RTA these parameters were respectively around 3.7 μC/m2 and 55 kV/cm. In the fatigue process, the Pr value decreased up to 16% from initial value after 1.3 x 108 switching cycles, for film crystallized in conventional furnace prepared from RTA Pr decreased up to 48% from initial value after 1.7 x 109 switching cycles.

D3.13 Characteristics of MMISFET with Pt/SrBi2Ta2O9/Pt/Y2O3/Si Gate Structure. Sun II Shim1,2, Young Suk Kwon3, Ik Soo Kim1, Seong-II Kim4, Yong Tae Kim5 and Jung Ho Park6; 1Electronics Engineering, Korea University, Seoul, South Korea; 2System Technology Division, Korea Institute of Science and Technology, Seoul, South Korea.

The metal-ferroelectric-semiconductor and metal-ferroelectric-insulator-semiconductor (MFS and MFIS) gate structures for the single tunnel field effect transistor (TFT) are promising devices for memory applications in non-volatile solid state memory, such as ferroelectric random access memory (FeRAM) have inherent weak points in short retention time and high operating voltage in spite of their advantages in non-destructive read operation and small cell size. For this reason, saturation of the ferroelectric film is obtained by the insulator with high dielectric constant is required. The alternative solution is metal-ferroelectric-metal-insulator-semiconductor (MFMIS) gate structure with different area ratio. The induced voltage to the ferroelectric film by using a buffer insulating layer in the MFIS gate structure. The Y2O3 film with thickness of 280 nm was deposited by rf sputtering of yttrium target in the reactive oxygen ambient and crystalized at 800°C for 30 min in the oxygen ambient. Bi2Sr2Ta2O9 (SBT) film with the thickness of 80 nm was deposited by rf sputtering of Tb metal target in the reactive oxygen ambient and crystallized at 600°C for 30 min in the oxygen ambient. The MFMSFET was fabricated and the electrical characteristics were investigated. It showed well-behaved counter clockwise drain current curve versus gate voltage characteristics and more than three orders of drain current difference between the programmed on and erase off state at 5 V operation.

D3.14 Nano electromechanics of Ferroelectric Lithography and Near-Atomic Density Data Storage by Piezoresponse Force Microscopy. Sergei V. Kulmin1, J. Shin1,2, Arthur P. Baddorf1, M. Kachanov3, E. Karapetian4 and A. Gruverman5; 1Condensed Matter Sciences Division, Oak Ridge National Laboratory, Oak Ridge, Tennessee; 2Department of Physics and Astronomy, The University of Tennessee, Knoxville, Tennessee; 3Department of Mechanical Engineering, Tufts University, Medford, Massachusetts; 4Department of Materials Science and Engineering, North Carolina State University, Raleigh, North Carolina.

The ability of ferroelectric materials to form stable sub-10 nm domains makes them one of the most promising materials for information storage applications. In the last several years, domain patterning using scanning probe technology was demonstrated to yield 40 nm domains, corresponding to 0.5 Tbit/in2 recording density. At the same time, Piezoresponse Force Microscopy (PFM) is routinely demonstrated to provide readout with 3-5 nm resolution, i.e., two orders of magnitudes higher recording density. To increase the achievable recording density, an understanding of the tip-induced polarization switching process is crucial. Here we analyze the tip-induced polarization switching in ferroelectric materials by PFM using exact solutions for electrostatic and coupled electroelastic fields below the tip. The solution of the coupled electroelastic problem for piezoelectric indentation is derived and used to obtain the tip-induced electric field and strain distribution in the ferroelectric material. This establishes a complete continuum mechanics description of the PFM imaging mechanism. The structure of tip-induced electroelastic fields is combined with the Landauer approach to provide a quantitative description of tip-induced polarization switching. It is proposed that the tip-induced domain switching can be mapped on the Landau theory of phase transitions with the domain size as an order parameter. For a point-charge interacting with a ferroelectric surface, switching of both first and second order is possible depending on the charge-separation surface. For a realistic tip shape, the domain nucleation process is first order in charge magnitude and polarization averaging occurs only above a critical tip radius. In using ferroelectric or ferroelastic switching, the late stages of the switching process can be described using a point charge/force model and arbitrarily large domains can be created; however, the description of the early stages of the nucleation process when the domain size is comparable with the tip radius of curvature requires the exact field structure to be taken into account. Optimal conditions for tip-induced polarization switching are determined and used to obtain the tip-induced electric field and strain distribution in the ferroelectric material. This establishes a complete continuum mechanics description of the PFM imaging mechanism. The structure of tip-induced electroelastic fields is combined with the Landauer approach to provide a quantitative description of tip-induced polarization switching. It is proposed that the tip-induced domain switching can be mapped on the Landau theory of phase transitions with the domain size as an order parameter. For a point-charge interacting with a ferroelectric surface, switching of both first and second order is possible depending on the charge-separation surface. For a realistic tip shape, the domain nucleation process is first order in charge magnitude and polarization averaging occurs only above a critical tip radius. In using ferroelectric or ferroelastic switching, the late stages of the switching process can be described using a point charge/force model and arbitrarily large domains can be created; however, the description of the early stages of the nucleation process when the domain size is comparable with the tip radius of curvature requires the exact field structure to be taken into account. Optimal conditions for tip-induced polarization switching are determined and used to obtain the tip-induced electric field and strain distribution in the ferroelectric material.

D3.15 Combinatorial Search of (Bi,LaCo)4Ti3O12 and (Bi,La,Ce)4Ti3O12 Prepared by Liquid Source Misted
Chemical Deposition (LSMCD) and Multi-Target Sputtering System. Seong Ihl Woo1,2,3, Ki Woong Kim1,4, Min Ku Jeon4,1, Kwang Seok Oh2,3, Tai Suk Kim1,4, and Yong Ki Park1,3; 1Chemical and Biointerface Engineering, Korea Advanced Institute of Science and Technology, Daejeon, South Korea; 2Korea Research Institute of Chemical Technology, Daejeon, South Korea. 3Center for Ultramicrochemical Process Systems (CUPS), Daejeon, South Korea.

We used the multi-target sputtering system equipped with movable mask to fabricate the Bi4+CeXTiO312 (BCT, 0 < x < 4) from Bi2O3 /CeO2 /TiO2 multi-layers. Here, the movable mask gives the variance of Bi/Ce over the substrate. To improve the solid-state intermixing, the deposition process was carried out at 300°C. We mapped the structural characteristics and ferroelectrical properties of BCT array as a function of Ce content, x. Microbeam XRD data showed that there were three phases: Bi-layered structure (x<0.8), Bi2TiO7 + CeO2 (0.8 < x < 2), and Bi2O3 + CeO2 (x>2). In addition, random spectra of BCT exhibited three characteristic peaks of TiO6 at 260, 5.4474 to 5.4353, 5.4217 and 5.4110 with increasing amount of Ce. These peaks showed the Bi2O2 layers, which were assigned to the Bi atoms in the perovskite units, became less observable with Ce substitution. The Ce content increased, these peaks were shifted to 205, 460, and 608 cm-1 relative to CeO2. To recognize the ferroelectric property, we deposited top electrode on the BCT array and then measured P-E hysteresis curve by using RT60A. In the Bi-rich region (x<0.8), the samples showed the ferroelectric property. The ferroelectric properties of BCT could be improved. On the basis of this conclusion, we fabricated other library of Bi3.75La0.25-xCexTi3O12 (BLCT) by liquid source misted chemical deposition (LSMCD) equipped with movable mask. Unlike the sputtering deposition, this deposition has an advantage that it could improve the homogeneity of library due to the liquid-liquid intermixing at R.T. Here, in the La-rich region (0.05 < Ce content, x <0.1), we observed that the intensity of (117) peak indicating the degree of TiO6 distortion was reduced, and especially, these samples exhibited good fatigue properties over 1010 cycles.

D3.18 UV-Assisted Rapid Thermal Processing of Strontium Bismuth Tantalate (SBT) Thin Films. Shane O’Brien1, Paul Hurley1, Gabriel O’Connor1, and Charles G. Wouters1; 1NMRC, Cork, Ireland; 2IMEC, Leuven, Belgium; 3STMicroelectronics, Catania, Italy.

Ferroelectric thin films of Strontium Bismuth Tantalate (SBT) have been found to have excellent fatigue resistance, even after 1012 cycles. Consequently, the SBT material system is attracting a lot of interest at present. One of the major challenges associated with the development of SBT based non-volatile memories is the integration of the ferroelectric films with established Si-based CMOS technologies. In particular, the thermal budget associated with the crystallisation of the SBT thin films (typically 700-800°C) can influence the performance of the underlying MOSFET, resulting in shifts in device parameters (e.g., Vt) and introducing the possibility of metallic contamination at the active device level. Consequently, it is of interest to develop processes which reduce the overall thermal budget necessary to achieve ferroelectric crystallisation and the required remnant polarisation (PR). The objective of this work is to present the results of an ultra violet (UV) assisted rapid thermal processing (UV-RTP) technique for SBT ferroelectric crystallisation. The SBT samples examined in this work were deposited by thermal MOCVD at 385°C on Pt/TiO2/SiO2/Si substrates. The SBT film was formed from three precursors: Bi(thd)3, for Bi, Sr(thd)2pmdeta for Sr, and Ta(O-ipr)4(thd) for Ta. The SBT film thickness was 120nm. The annealing of the samples was performed in a UV RTP system, with KrCl excimer lamps at 222 nm (5.8 eV). The anneals were performed in oxidizing atmosphere pressure O2 and the temperature ranged in the range 35-50°C. The crystallisation anneal is a two stage process, with a 300s period at the depostion temperature, and the second stage at the maximum anneal temperature (Tmax: 610-750°C). Experiments were performed with UV pre-exposure at 1000 mW/cm2, rapid thermal process. For selected samples, the second stage of the anneal was performed in a conventional furnace (700°C, O2, 60 minutes). The comparative measurements presented are based on SBT samples (3 cm x 3cm) taken from the same 200 mm wafer. FTIR absorbance data and electrical characterization data are presented for the SBT samples processed via the different irradiation strategies. Data were also obtained from samples where the second stage of the crystallisation anneal was performed in a conventional furnace (700°C, 60 minutes, O2). The effect of UV irradiation in UV-RTP annealing will be discussed in detail and optimum UV-assisted conditions for SBT crystallisation will be presented.

D3.19 Thin Ferroelectric Films between Double Schottky Barriers. Lyubin A. Delimova1, Igor V. Grekhov1, Dmitri V. Mashovets1, Sangmin Shin2, June-Mo Koo3, Suk-Pil Kim1 and Youngsoo Park1; 1Solid State Electronics Division, Ioffe Institute RAS, St.Petersburg, Russian Federation; 2Material and Devices Laboratory, Samsung Advanced Institute of technology, Suwon, South Korea; 3Processing Engineering Laboratory, Samsung Advanced Institute of technology, Suwon, South Korea.

A metal/ferroelectric/metal (M/F/M) capacitor structure is one of the key elements of modern nonvolatile memory manufacturing processes. The basic operations of a memory element are information writing, reading, and testing. These functions are executed by applying an external bias of different value and polarity to an M/F/M structure. Therefore, the ability to predict the behavior of M/F/M structure and...
find the distribution of the electric field $E(x)$, potential $\Phi(x)$ and polarization $P(x)$ in thin ferroelectric film as functions of bias $V$ is of great importance to the field of ferroelectronics. We write $E(x)$ definition is complicated. So, a standard way to find the $E(x)$, $\Phi(x)$, and $P(x)$ distributions across the film thickness as a function of bias and the film electrical history. We consider each Schottky barrier as an independent source of the electric field, therefore field in a thin film is produced each Schottky barrier. To avoid a self-consistent solution of equations, we use an external expedient: virtually enlarge the film thickness to a value which equals the total space charge region (SCR) as defined by Schottky barriers. We set the origin in the middle of the ferroelectric at the edge of the SCRs, where $E(x=0) = 0$, and select these values as the boundary conditions. Numerically integrating the Poisson equation on both sides of the point of origin, we find $E(x)$ and $\Phi(x)$, from the current-voltage characteristics and hysteresis loops. We use this model to describe a M/F/M structure showing a non-symmetrical hysteresis loop (HL). For this, we fulfilled calculations for different values of ferroelectric parameters and showed that the experimental HL agrees reasonably with the upper part of one calculated HL and the lower part of the other calculated HL. It confirms the possibility of the model to describe the studied structure. The non-symmetrical HL indicates a presence of a non-compensated charge within the ferroelectric. Using a transient current measurement, we can select the contribution of interface traps to the non-compensated charge.

D3.20
Layered Tunnel Barrier Lowering in Multilayer High-k Heterostructures using Bias-dependent Internal Photovemission

Damon B. Farmer1, Roy G. Gordon2, and Harry A. Atwater3; 1Jet Propulsion Laboratory, Pasadena, California; 2Thomas J. Watson Laboratory of Applied Physics, California Institute of Technology, Pasadena, California; 3Division of Engineering and Applied Sciences, Harvard University, Cambridge, Massachusetts.

Layered tunnel barriers have been proposed as replacements for SiO$_2$ for use as injection barriers in nanocrystal floating-gate memories. Due to the predicted larger change in conductance as a function of injection voltage, such barriers are expected to enable nanosecond programming and data retention times with high-speed operation. We have utilized internal photoemission (IPE) spectroscopy to study barrier height lowering of Al$_2$O$_3$/HIO$_2$/SiO$_2$/Si layered tunnel barrier structures over a wide range of applied biases. Dielectric stacks of Al$_2$O$_3$ and HIO$_2$ are grown on n-type silicon substrates by atomic-layer deposition (ALD). Individual layers were nominally 15 nm thick, with actual thicknesses determined by transmission electron microscopy. In addition, an interfacial layer is observed between the high-$k$ layers and the Si substrate; this layer is attributed to SiO$_2$ formed during the UV ozone clean and is common at high-$k$/Si interfaces. In these experiments, the unintentionally grown SiO$_2$ interfacial layer acts as another dielectric layer and in fact contributes to barrier lowering under bias. The IPE results are analyzed using a simple electrostatic model to yield effective barrier heights and overall band alignments across the entire voltage range. This treatment includes transport of carriers from both the silicon substrate and the aluminum gate contact. Using this technique we demonstrate substantial barrier lowering (0.75 eV) for Si-compatible dielectric heterostructures, and we discuss the application of these barriers to improved speed and reliability of floating gate nonvolatile memory devices.

D3.21
Electron Tunneling through Ultra Thin Ferroelectric Films.

Adrian Lin Pinyuen1, Nicholas K. Pertsin2, Rene Meyer3, Valanac Nagaprasak3, Andrew C. Krebs3, Juegen Schob3, Chuen Lin Jia1, Ulrich Poppe2, Hermann H. Kohlstedt1 and Rainer Waser2; 1Institut fuer Festkoerperforschung and CNI, Forschungszentrum Juelich GmbH, Juelich, Germany; 2Institut fuer Schichten- und Grenzflaechen and CNI, Forschungszentrum Juelich GmbH, Juelich, Germany; 3A. F. Ioffe Physico-Technical Institute, St. Petersburg, Russian Federation; 4EPFL, Lausanne, Switzerland.

Recent theoretical and experimental work showed that ferroelectricity exists down to a few unit cells thick epitaxial films under appropriate boundary conditions. In this work we present the relevance of electron tunneling through ultrathin ferroelectric films. We present our development of so-called ferroelectric tunnel junctions with the following layer sequence: SrTiO$_3$(substrate)/SrRuO$_2$(electrode)/BaTiO$_3$ or PbZr$_{0.52}$Ti$_{0.48}$O$_3$(as ferro-electric)/SrRuO$_2$ or Pt top electrode. The aim of our work is to study fundamental aspects of electron tunneling and electron transport through a ferroelectric material and the influence of the transport current on the ferroelectric polarization state of the barrier material. For thicknesses ranging between 240 nm and 8 nm common ferroelectric hysteresis loops were observed. For thinner barriers with the thickness ranging from 6 nm to 4 nm, the $I-V$ characteristics shown switching events with two resistive states. We will present a theoretical and experimental approach on the basis of the deformation potential model to combine the tunneling transfer matrix element with the strain state of the barrier. In addition the influence of the polarization state and the structure at the bottom and top interfaces will be discussed with respect to the tunnel barrier. The observed switching events will be discussed from the point of symmetry with the measured $I-V$ characteristics. Investigations on ultra thin PbZr$_{0.52}$Ti$_{0.48}$O$_3$ films are in progress, for film thicknesses in the range of 4 nm - 2 nm. Small area arrays have been fabricated using a Si$_3$N$_4$ stencil mask technique. $I-V$ measurements were performed in the temperature range of 180 K - 300 K by a conductive AFM technique.

SESSION D4/17: Joint Session: Magnetoresistive Random Access Memory


Magnetoresistive random access memory (MRAM) employs a magnetoresistive device integrated with standard silicon-based microelectronics, resulting in a combination of qualities not found in other memory technologies: MRAM is non-volatile, has unlimited read and write endurance, and has demonstrated high-speed read and write operations. Recent technology developments at MRAM are to develop a Magnetic Tunnel Junction (MTJ) device. The properties of our unique toggle-switching MRAM bit is discussed and compared to those of the conventional switching approach. For the first time a comprehensive review of the reliability of the MTJ tunneling dielectric and the current carrying write lines will be presented. Scaling of these results to operating conditions demonstrates the reliability of our 4Mb MRAM chip.

9:00 AM *D4.2/17.2 Spin-Transfer Switching In Nanometer-Sized Magnetic Tunnel Junctions For MRAM Application, Vinning Huang, R. D. Department, Grandis Inc., Pasadena, California.

Spin-polarized current induced magnetization switching has stimulated considerable interest in recent years due to its rich fundamental physics and great potential for new magnetoelectronic applications. Low switching current density and high read signal are required for the application of the spin transfer switching to non-volatile magnetic memory (MRAM). We present here a study of spin transfer switching in nanometer-sized magnetic tunnel junctions (MTJs) with low resistance-area product (RA) ranged from 1-10 $\Omega$m$^2$ and TMR$=30\%$. Bottom PtMn and IrMn exchange-biased MTJ films were deposited in a magnetron sputtering cluster system. A thin tunneling barrier was formed by natural oxidation of the pre-deposited thin Al layer. MTJ films were subsequently patterned into nanometer ellipse shaped pillars using both deep UV lithography (combined with resist tranding) and e-beam lithography. Spin-transfer switching has been consistently observed in MTJs with dimensions down to 0.2x0.2 $\mu$m$^2$. Low switching current density $Jc=10^7$ A/cm$^2$ has been achieved using low moment free layer CoFeB. High TMR values about 30% were obtained in spin-transfer induced switching and attributed to homogenous and continues Al$_2$O$_3$ barrier grown on smooth bottom lead with a roughness (RMS) of 2-3 A. These results could have potential applications for a spin transfer based MRAM.

During the last decade considerable attention has been devoted to the fabrication and characterization of thin film magnets with sub-micron lateral dimensions (nanomagnets). Nanometer-sized magnets can be engineered to exhibit large resistance changes depending on the relative orientation of the magnetization within each of the magnetic layers comprising the structure. This in turn allows for bits of information to be stored by controlling the magnetic configurations exhibited by these small elements. Present magnetic random access memory (MRAM) designs use large arrays of elongated nanomagnets which can be read and written using conductor lines [1]. Ring-shaped nanomagnets have been proposed as alternative MRAM cells [2], in part due to the existence of a range of stable magnetic configurations which could allow for high-density MRAM devices storing more than one bit per nanomagnet. The magnetotransport properties of ring-shaped single-magnetic-layer structures with widths of 200 nm and diameters exceeding 1 μm have previously been investigated [3]. In this contribution we report on the magnetic and magnetotransport properties of sub-micron diameter elliptical-ring magnets with diameters of 30 nm and above. The rings are fabricated using single layer NiFe or Co, or NiFe (6 nm)/Cu (3-6 nm)/Co (4 nm) pseudo-spin-valve thin film structures. A multilevel lithography process involving electron-beam lithography and lift-off processing was used to fabricate the rings with different structures. Magnetization measurements show that single layer rings transform between onion (bidomain) and vortex (flux-closed) states, at switching fields which increase with decreasing ring diameter and ring width. For example, 360 nm diameter, 160 nm thick rings have an onion transition at 150 Oe and a vortex-reverse onion transition at 850 Oe, while the corresponding values for a 110 nm wide ring are 240 Oe and 1900 Oe. Resistance changes resulting from anisotropic magnetoresistance of the material. In the case of multilayer rings, more complex magnetic behavior occurs because each layer has different switching fields, and magnetotransport effects originate from giant magnetoresistance in the structure. The magnetotransport properties reflect the different states within each magnetic layer, as well as the exchange and magnetostatic coupling between layers. In particular, the effects of varying the width of the rings and the thickness of the Cu spacer layer on the magnetic and magnetotransport behavior will be discussed. [1] Duram et al. IEDM technical Digest 2004, session 34, paper #6. [2] J.G. Zhu et al. J. Appl. Phys. 87 6688 (2000). [3] M. Klaui et al. Phys. Rev. Lett. 90, Art. No.097202 (2003).

Size Dependent Properties of Current-Confined CPP Spin Valve Device. Hao Meng, Jianguo Wang, Yunfei Ding and Jian-Ping Valve; Electrical and Computer Engineering, University of Minnesota, Minneapolis, Minnesota.

Current-perpendicular-to-plane (CPP) spin valve device has the potential to replace the current-in-plane (CIP) device for high density magnetic recording head and other spintronics applications. In order to achieve its intrinsic high magnetoresistance (MR) ratio, the resistance coming from the active layers of CPP spin valve has to be increased [1]. Several approaches such as dual spin valve structure, nano-oxide layer, and new materials have been investigated by many groups. Another effective approach to increase the resistance is to reduce the current crossing area. In this work, size effects on the CPP spin valve were investigated. A series of samples with small pillar area (75x130 nm², 150x217 nm² and 184x415 nm² with ellipse shape) were fabricated in our lab. The processes include thin film sputtering, electron-beam lithography, ion milling etching and magnetic annealing. Nano-oxide-layers (NOL) were also introduced in the present work and functioning as current confine to further reduce the effective area for current passing through. With dot size decreasing, higher MR and MR ratio were achieved, which indicates that device is approaching to its intrinsic MR ratio with size decreasing. However, the results show a non-linear relationship between dot area and MR ratio. This is because that the conducting lead contact resistance in the MR measurement is still too high to be neglected, thus the spin valve active layer resistance couldn’t dominate the measurement result, which caused MR ratio lower than the intrinsic value. Detailed results will be presented in full paper. 1. Atsushi Tanaka, Yoshikoh Seyann, Arata Jogo, Hirota Oshima, Reiko Kondo, Hiroshi Kishi, Chikayoshi Kumata, Yutaka Shimizu, Shin Eguchi, and Kazuaki Sabot, "Readout Performance of Confined-Current-Path Current-Perpendicular-to-Plane Heads", IEEE Trans. Magn., 40, 203, (2004) Corresponding Author Email: jpwang@ece.umn.edu

SESSION D5: Nanoparticle Memories

Chairs: Alain Claverie and Dimitris Tsolakidas
Wednesday Afternoon, December 1, 2004
Back Bay B (Sheraton)

1:30 PM D5.1


To overcome the limitations of the current nonvolatile semiconductor memory (NVM) technologies and successfully respond to new market opportunities (e.g. portable devices) several novel fabrication routes are being actively investigated. These technological alternatives face tough requirements including low-power consumption, low-voltage operation, high-density and high-speed information storage. To meet these requirements, metal-oxide-semiconductor transistors using a high-density (10^12 cm^-2) of laterally uncoupled nanocrystal dots with diameters of 5nm and below embedded in the gate dielectric have been proposed. As the optimum mean size of the NCs is below the current lithography resolution, an attractive approach to fabricate nanocrystals is through self-assembling process. Among the different processing routes explored during the last few years the ion beam synthesis (IBS) technique has received substantial attention because of its flexibility and its manufacturing advantages. The potential of IBS for nanocrystals memory applications has recently enhanced through the synthesis in the ultra-low-energy (ULE) regime (typically 1keV) of single silicon nanocrystals layers in thin SiO2 films. In terms of structural possibilities, a combination of ULE-IBS conditions and oxide thickness allows for the provision of nanocrystal dots at a location from the SiO2/Si interface that can be tailored for DRAM-like or EEPROM-like applications. Despite these attractive technological options, many fabrication issues remain to be solved before establishing a reliable process leading to reproducible memory devices. Charge neutralization, energy and impurity contamination during implantation, the effect of the post-implantation cleaning process, and the implantation-related oxide and SiO2/Si interface damage are significant issues that will be outlined through an analysis of electrical data and their linkage to structural parameters. The overcoming of concerns pertaining to the aforementioned issues allows for the fabrication of competitive and reliable memory structures, as it will be demonstrated for the case of laboratory prototype NC-FG MOSFETs. Particular emphasis will be placed on our recent research development for integrating the ULE-IBS technique in a conventional 0.13um flash memory technology. Finally, advantages and disadvantages of ULE-IBS relative to other synthesis techniques will be discussed.

2:00 PM D5.2

Manipulation of 2D-Arrays of Si Nanocrystals Embedded in a Thin SiO2 Layer by Low Energy Implantation. Caroline Bonafos1, Gerard Benassayag1, Sylvie Schamm1, Hubert Coffin1, Nikolay Cherkashin1, Alain Claverie1, Pascal Normand2, Panagiotis Dimitrakis2, Michel Nicaise3, Marie-Michèle Mueller4, Karl Heinz Heising4, Tence Marcel3 and Christian Collieux4.

1 CEMES/CNRS, Toulouse, France; 2 Institute of Microelectronics NCSR Demokritos, Aghia Paraskevi, Greece; 3 MEMS/INFAM, Aghate, Italy; 4 FZI Rosendorf, Dresden, Germany; 5 LPS, Paris Sud University, Orsay, France.

Silicon nanocrystal-based memories could potentially become an evolutionary replacement for the polymer-based flash memory technology in a small size, low-power flash memory. Silicon nanocrystal based metal-oxide-semiconductor (MOS) memory structures a fine control of the Si nanocrystals (ncs) location in the gate oxide is required for optimal device architectures. In this work, we show how to manipulate and control the depth-position, size and surface density of two dimensional (2D) arrays of Si nc's embedded in thin (<10 nm) SiO2 layers, fabricated by ultra-low-energy (typically 1 keV) ion implantation. Specific experimental methods have been developed to characterize these populations of nc's. They include Frensel imaging for the measurement of the injection distance between the channel and the nc's and spatially resolved Electron Energy Loss Spectroscopy (EELS) using the spectrum-imaging mode of a Scanning Transmission Electron Microscope (STEM) to measure the size distribution and density of the nc population and Time-Of-Flight Secondary Ion Mass Spectrometry (ToF-SIMS) to measure the depth distribution of excess silicon in the gate oxide. We have used all these techniques to study the influence of implantation and annealing conditions and oxide thickness on the characteristics of the nc populations and understand
how they affect the charge storage properties of associated devices (capacitors and transistors). Finally, we show that the injection distance between the band and the band gap can be tuned from 10 to 2 nm by a judicious combination of ion beam energy and initial SiO2 thickness. This trade-off is the result of a competition between ion implantation, sputtering and interfacial mixing. The density of the ncs can be varied between 10^11 and 2x10^12/cm2. Annealing under slightly oxidizing ambient has been found essential for the optimization of the memory properties of the devices. During such oxidations, the oxide integrity is restored, the ncs are passivated and a significant amount of the ncs is crosslinked to a further increase of the ncs density and a decrease of their mean size. Both EEPROM-like and NVRAM-like transistors have been fabricated following this route. Their characteristics will be discussed in relation with the characteristics of the 2D arrays of ncs on which they rely. These devices show comparable data retention and endurance characteristics than the actual SONOS-like structures and appear very attractive in the future for deep submicron CMOS technology.

2:15 PM D5.3 Chemical Vapor Deposition of Ge Nanocrystals on HfO2 for Nonvolatile Memory Device Application. Ying Qian Wang, Jing Hao Chen, Won Jong Yoo and Yee-Chia Yeo; Electrical and Computer Engineering, National University of Singapore, Singapore, Singapore.

Flash memory devices employing nanocrystals (NCs) have drawn considerable attention as one of the most promising candidates for future nonvolatile, high density, and low power memory IC application. By using a high-k dielectric in place of the conventional SiO2 based dielectric, NCs flash memory can achieve significantly improved programming/erasing efficiency and endurance. However, there is limited work on the integration of high-k dielectric materials with NCs, especially Ge nanocrystals embedded in HfO2. In this study, chemical vapor deposition (CVD) of germanium nanocrystals using GeH4 gas directly on hafnium oxide is investigated. Atomic force microscopy (AFM), X-ray diffraction (XRD), and X-ray photoelectron spectroscopy (XPS), and second electron microscopy (SEM) were utilized to characterize the Ge nanocrystals. The dependence of the Ge nanocrystal size and density on deposition temperature (1100 °C), deposition time (10 s to 40 s), and flow rate (60 sccm to 120 sccm) was explored. It was found that the formation of Ge nanocrystals on HfO2 does not substantially occur at temperatures below 550°C, but becomes significant at 600°C, where a maximum NC density is achieved. The tradeoff between amount of available gas reagent and gas residence time results in a maximum NC density at a flow rate of 80 sccm. In this experiment, the largest Ge NC density achieved is 10^11/cm², with a mean NC diameter of about 16nm. A MOS capacitor with CVD Ge NCs embedded in HfO2 was fabricated. For comparison, a control capacitor with HfO2 dielectrics but without Ge NCs was also fabricated. Capacitance-voltage characteristics of the capacitors were measured. The NC formation was confirmed by XTEM. The tunnel oxide is not completely free of Si-nc or clusters, as observed by AFM, and the Si-nc are completely free of Si-nc and thick enough (11 nm) to prevent tunnelling from/to the gate electrode. The Si-nc are located around the projected range and they show a mean size of 2.6 ± 0.2 nm. The tunnel oxide is not completely free of Si-nc or clusters, as observed by XTEM, but there is a trade-off between deposition temperature and density when approaching the p-type substrate. We believe that these small Si-nc or clusters in the tunnel oxide play an outstanding role in improving the performance of the devices. For charging (writing) when a gate bias is applied to the structure, these clusters assist traps when tunnelling to the central region. On the contrary, when the Si-nc are already charged, these nanoclusters do not contribute to the charge discharge process as they have larger band-gaps (due to quantum confinement) than the bigger Si-nc in the center of the layer, thus not being energetically favourable for the stored charge to back-tunnel. This simple model, based on the correlation of the most important electrical and structural parameters and the information, has helped us to understand the importance of the implantation dose as a technological parameter when a trade-off between write and retention times is required. For our samples, this dot size about 14% Si excess and low number fluctuations in the gate area, has prevented, showing a completely flat and stable programming window after 10^7 Write/Erase programming pulses.

2:30 PM D5.4 Characterization of Number Fluctuations in Gate-last Metal Nanocrystal Nonvolatile Memory Array Beyond 90nm CMOS Technology. Chung Ho Lee, Udayan Ganguly and Edwin C. Kan; Electrical and Computer Engineering, Cornell University, Ithaca, New York.

Fluctuation on number of nanocrystals in a small MOS gate area poses one of the main bottlenecks for the scalability of nanocrystal-based nonvolatile memories [1-3] beyond 90nm CMOS technology. If the nanocrystal formation or dot self-assembly is done before the gate stack patterning in a self-aligned source/drain process, there needs to be at least 100 nanocrystals within the effective gate area to control the number fluctuation below 10%. Based on typical nanocrystal diameter of 3-4nm, the effective gate area will be larger than 80nm by 80nm to satisfy the parametric yield requirements. This number fluctuation problem in gate area scaling can be addressed in the gate-last integration process [4]. When a nanocrystal self-assembly is performed after the gate patterning, Self-alignment of source and drain can still be achieved through a dummy gate replacement. Due to the additional surfaces at the side-walls and the high quality of the effective gate electrodes, the nanocrystal dots can be even smaller than 1nm. Atomic force microscopy and X-ray photoelectron spectroscopy will be used to characterize the nanocrystal dots and the correlation of the size and density in gate patterns with various feature sizes from 30nm to 250nm. The dummy gate regions with 50nm oxide wall are defined by e-beam lithography and RIE (ReactIon Etching). Metal nanocrystals of Au, Ag, and Pt are formed on 25nm tunneling oxide by direct-deposit self-assembly (i.e., evaporation and post-annealing) in the gate stack. Annealing under slightly oxidizing ambient has been found essential for optimization of the memory properties of the devices. Due to the additional surfaces at the side-walls and the high quality of the effective gate electrodes, the nanocrystal dots can be even smaller than 1nm. Atomic force microscopy and X-ray photoelectron spectroscopy were utilized to characterize the Ge nanocrystals. The dependence of the 2D arrays of ncs on which they rely. These devices show comparable data retention and endurance characteristics than the actual SONOS-like structures and appear very attractive in the future for deep submicron CMOS technology.


We report in this work a Si-nanocrystal (Si-nc) MOS memory which shows, at the same time, fast writing times and long charge retention. This has been achieved by optimizing a structure reported previously that exhibited excellent retention characteristics. For the new structure, 15 keV Si ions have been implanted in a 40 nm thick oxide at 1100 °C in order to create excess Si at the tunnel oxide. There is a Si excess compromise (density depth profile of Si-nc) in which write times are improved to less than 3 orders of magnitude (in the submilliseconds range) while still maintaining a virtually infinite retention time. Such behaviour has been correlated with the structural characteristic by EFTEM, which reveals a control oxide completely free of Si-nc and thick enough (11 nm) to prevent tunnelling from/to the gate electrode. The Si-nc are located around the projected range and they show a mean size of 2.6 ± 0.2 nm. The tunnel oxide is not completely free of Si-nc or clusters, as observed by XTEM, but there is a trade-off between deposition temperature and density when approaching the p-type substrate. We believe that these small Si-nc or clusters in the tunnel oxide play an outstanding role in improving the performance of the devices. For charging (writing) when a gate bias is applied to the structure, these clusters assist traps when tunnelling to the central region. On the contrary, when the Si-nc are already charged, these nanoclusters do not contribute to the charge discharge process as they have larger band-gaps (due to quantum confinement) than the bigger Si-nc in the center of the layer, thus not being energetically favourable for the stored charge to back-tunnel. This simple model, based on the correlation of the most important electrical and structural parameters and the information, has helped us to understand the importance of the implantation dose as a technological parameter when a trade-off between write and retention times is required. For our samples, this dot size about 13% Si excess and low number fluctuations in the gate area, has prevented, showing a completely flat and stable programming window after 10^7 Write/Erase programming pulses.

3:30 PM D5.6 Local Self-Order Observed During Chemical Vapor Deposition of Silicon Quantum Dots for Application in Nanocrystal Memories. Rosaria A. Puglisi¹, Salvatore Lombardo¹, Giuseppe Nicolet¹, Corrado Spinella¹, Cosimo Gerard², Barbara De Salvo³, Luca Perioli¹, and Giuseppe Grandi²²; Istituto per la Microelettronica e i Microsistemi, Consiglio Nazionale delle Ricerche, Catania, Italy; ²STMicroelectronics, Catania, Italy; ³CEA-LETI, Grenoble, France; ⁴Universita' di Pisa, Pisa, Italy.

Si quantum dots have been obtained by chemical vapor deposition of silane on silicon dioxide and implanted in a flash-like memory device. The dot formation process has been studied in the regime of the sub-monolayer depositions and of surface coverages of about 20-30%. Several substrate temperatures, post-deposition annealing temperatures, and substrate preparation conditions have been studied. Energy filtered transmission electron microscopy with very high spatial and chemical resolution is adopted to obtain the dot size and inter-dot distance distributions. It is shown that the nucleation process, though continuous under typical deposition conditions, is not a random process. The dots appear separated by Si-free denuded zones, due to the silicon adatom capture mechanism. The dot size is shown to scale with the size of its own capture zone.
Si nanocrystals can be produced in non-volatile memory devices to reduce susceptibility to charge loss via tunnel oxide defects, allowing scaling to smaller sizes than possible with conventional Flash memory technology. In order to optimize device performance, it is desirable to maintain sufficient inter-crystallite separation to limit electron tunneling between adjacent crystallites. Ideally, crystallite densities in excess of $10^{12}/\text{cm}^2$ with relatively narrow particle size distributions must be achieved, posing a significant challenge for process development and control. In order to facilitate development of such a process, a rate-expression-based model has been developed for the nucleation and growth of silicon nanocrystals on SiO$_2$ in a CVD process. The model addresses the phenomena of nucleation, growth, and coalescence and includes the effects of exclusion zones surrounding the growing nuclei. The model uses a phenomenological expression to describe the nucleation rate, which assumes that the following nucleation, crystallite growth is dominated by gas-phase deposition processes, analogous to CVD of polycrystalline silicon. The model-predicted time-evolutions of crystallite densities and crystallite size distributions are consistent with experimental distributions as measured by Scanning Electron Microscopy (SEM). By coupling the model to a reactor-scale model of polysilicon CVD, it is possible to predict variations in the crystallite size distributions at various locations across a wafer as a function of reactor settings (temperature, pressure, flow rates, etc.). This in turn can be used for process control and optimization in order to ensure uniform deposition of nanocrystals in a large-scale manufacturing environment.

**0400 PM D5.8**

Monte Carlo Simulations of Silicon Nanocrystals in an Insulator Matrix. George Hadjisavvas and Pantelis C. Kelires; Physics Department, University of Crete, Heraklion, Crete, Greece.

Si nanocrystals (nc) embedded in an insulator matrix, usually a-SiO$_2$, have been extensively studied in recent years because of their photoluminescence and nonvolatile memory properties. Possible sources of light emission are proposed to be the quantum confinement and localized surface states. The latter are also believed to be a key factor for the memory properties. However, some important issues remain unclear. For example, the confinement is lost if the size and density of the nanocrystals; it is essential to know their stability in the amorphous matrix as they become smaller. Also, the atomic structure of the interface, i.e., kind and proportion of bonds, is a crucial parameter, yet it is not well known. We present here results of Monte Carlo simulations which shed light on these issues. We consider Si nanocrystals in amorphous silicon dioxide. In our approach, the generation of the embedding a-SiO$_2$ structure is achieved via a modified Wooten-Winer-Wenner method. Starting from crystalline beta-cristobalite, the network is amorphized through bond-breaking and switching moves. The Si nc is positioned at the center of the cell. The energies are calculated using the Keating potential. We introduce novel bond-breaking moves of the type Si-Si to Si-O-Si, apposite to a-Si-Si to Si-O-Si, apposite to a-Si-Si to Si-O-Si, or a-Si-Si to Si-O-Si. This allows us to study interdiffusion in the system. We find a significant proportion of Si-O-Si bridge bonds at the interface, not considered previously. A penetration of oxygen into the nc, limited to few Angstroms, is observed. The interface is a non-uniform region. From an oxidation-number analysis, it comes out that its width is about seven Angstroms. The energetics show that this region is highly strained, and that the stability of the ncs increases as their size increases and when they approach each other (formation of a dense array.) We found a critical diameter of 1.5 nm, below which the nc's are unstable. This is accompanied by heavy deformation and oxidation of the core of the nc. Spherical and faceted ncs of the same size have also been considered. We are currently examining the nanocrystal nucleation process in the amorphous matrix.

**0415 PM D5.9**

Characterization of Electronic Charged States of Silicon Nanocrystals as a Floating Gate in MOS Structures. Seichi Miyazaki$^1$, Taku Shibaguchi$^1$ and Mitsuhashi Ikeda$^2$; $^1$Graduate School of Advanced Sciences of Materials, Hiroshima University, Higashi-Hiroshima, Japan; $^2$Research Center for Nanodevices and Systems, Hiroshima University, Higashi-Hiroshima, Japan.

Discrete charged states in Si quantum dots (QDs) embedded in SiO$_2$ is a crucial factor for nonvolatile memory operations of Si-QDs floating gate MOS devices. We have studied capacitance-voltage and transient current-voltage characteristics of MOS capacitors with Si-QDs floating gate in dark and under visible light illumination at room temperature to gain a better understanding of the electronic properties of the Si-QDs floating gate. A 3 nm-thick SiO$_2$ as a tunnel oxide layer was first grown on p-type and n-type Si(100) at 1000°C in 2%O$_2$ diluted with N$_2$. Hemispherical Si nanocrystals as QDs were self-assembled on the tunnel oxide by LPCVD using SiH$_4$ at 575°C. A 2%O$_2$ and the average dot height were controlled at 5.5x10$^4$ cm$^{-2}$ and 8nm, respectively. After the dot surface oxidation at 800°C in 2%O$_2$ diluted with N$_2$, a 7.5nm-thick control oxide was formed using conformal deposition of a 3.5nm-thick SiO$_2$ layer by LPCVD using 10% SiH$_4$ diluted with He at 440°C and complete oxidation of the Si layer at 1000°C in 2%O$_2$ diluted with N$_2$. Al-gates with a size of 1mm in diameter were formed for MOS capacitors. Capacitance-voltage (C-V) characteristics of Al-gate MOS capacitors on p-type and n-type Si(100) show unique hystereses due to the charging and discharging of the Si-QDs floating gate with a symmetric pattern reflecting the Fermi level of the substrate. This confirms that the undoped Si-QDs floating gate acts as a storage node for both electrons and holes. Namely, the contribution of traps with a specific energy state to the observed C-V hystereses can be ruled out. For each of high-frequency C-V curves measured in dark, a single capacitance peak appears only around a flat-band voltage condition, which is attributed to the quick flat-band voltage shift caused by the collective emission of charges (electrons in the MOS capacitors on p-Si(100) or holes in the MOS capacitor on n-Si(100)) retaining in the Si-QDs floating gate as confirmed from the corresponding transient current peak. Under visible light illumination, another capacitance peak due to collective injection of charges (electrons in the MOS capacitors on p-Si(100) or holes in the MOS capacitor on n-Si(100)) to the electrical neutral Si-QDs floating gate becomes observable in a weak-inversion condition as a result of photogenerated carriers (electrons in p-Si(100) or holes in n-Si(100)) in the vicinity of the area masked with the Al gate flow into beneath the gate oxide. This work was supported in part by Grant-in-Aid for scientific research of priority area (A) and for the 21st Century COE program on NanoElectronics for Tera-bit Information Processing from the Ministry of Education, Science, Sports and Culture of Japan.
has been shown that low pressure chemical vapor deposition (LPCVD) of nanocrystals is feasible in a batch reactor but with a large size dispersion in SiGe layers. To improve the size dispersion of the nanocrystals, a novel 2-step process with silane was introduced. In the conventional 1-step process, the oxide surface is exposed to silane at the same partial pressure and temperature during both nucleation and growth steps. In the new 2-step process, the surface is first exposed briefly to silane at higher temperature (580-600°C) and then to the temperature is lowered to allow selective growth on the existing silicon nuclei over the oxide surface. With this approach, the nucleation step can be separated from the growth step and consequently the size dispersion can be improved by a factor of 2. These nanocrystals have been incorporated into device wafers and the electrical data will be collected and presented, along with the SEM and ellipsometry results.

D6.2 Ge Nanocrystals in MOS-Memory Structures Processed by Molecular-Beam Epitaxy and Rapid-Thermal Processing.

Arne Nylandsted Larsen1, A. Kanjilal3, John L. Hansen1, Peter Gaduk1, Pascal Normand2, Panagiotis Dimitrakis1, Dimitris Tsoukalas3, Nikolay Cherksihn and Alain Claverie2; 1Institute of Physics and Astronomy, University of Aarhus, Aarhus, Denmark; 2Institute of Microelectronics, NCSR Demokritos, Athens, Greece; 3CEMES/CNRS, Toulouse, France.

A considerable attention is presently focused on semiconductor nanocrystals embedded into the silicon oxide of a MOSFET device for future high speed and low power consuming logic and memory devices, and a variety of fabrication procedures and structures are being tested. We have developed a new method of forming Ge nanocrystals in a SOI layer based on molecular beam epitaxy (MBE) and rapid thermal processing (RTP)1-3. The method is, among other things, distinguished by giving sharp distributions of nanocrystal sizes in the oxides and the growth. The method has the advantage of the very high precision by which a very thin Ge layer can be deposited on this Ge layer is first deposited by MBE on a thermally grown SiO2 layer on a (001) Si wafer, followed by MBE deposition of a Si capping layer. The structure is subsequently oxidized by RTP in an oxygen ambient followed by a reduction process at elevated temperature in a nitrogen ambient. With proper choice of process parameters the nanocrystal size can be varied between 3 and 7 nm and the density of the binary structure is between approximately 1x1011 and 1x1012 dots/cm2. The tunneling oxide thickness is determined by the thickness of the thermally grown SiO2 layer, and is typically 4 nm. C-V measurements of MOS capacitors reveal hole and electron injection from the substrate into the nanocrystals. Memory windows of about 0.2 and 0.5 V for gate-voltage sweeps of 3 and 6 V, respectively, are achieved. 1 Structural and electrical properties of silicon dioxide layers with embedded germanium nanocrystals grown by molecular beam epitaxy (MBE) and rapid thermal processing (RTP): A. Kanjilal, J. Lundgaard Hansen, P.Gaduk, A Nylandsted Larsen, N.Cherkshin, A.Claverie, P.Normand, E.Kaplanakias, D.Skarlotos and T.Tsoukalas, Appl.Phys.Lett. 82, 1212 (2003) 2 Size and aerial density distributions of Ge nanocrystals in a SOI layer produced by molecular beam epitaxy and rapid thermal processing: A. Kanjilal, J. Lundgaard Hansen, P. Gaduk, A Nylandsted Larsen, P. Normand, P. Dimitrakis, D. Tsoukalas, N. Cherksihn and A. Claverie, to be published. 3 Method for formation of a memory structure with nanocrystals in dielectric layer: A.Nylandsted Larsen, J.Lundgaard Hansen, P.Gaduk, and K.-H Heing, PCT Request, 2003.

D6.3 Investigation of Programming Voltage Scaling in Memory Devices using SiGe Nanocrystals, Rohit Gupta1, S. K. Samanta1, Won Jong Yoo2, Ganesh Samudran1, Daniel Chan1, L. K. Berna1 and N. Balsubramanian1; 1Electrical and Computer Engineering, National University of Singapore, Singapore, Singapore; 2Institute of Microelectronics, Singapore, Singapore.

It is well understood that distributed floating gates of semiconductor devices can be an alternate solution for scaling of the conventional memory devices. Where SiO2 is being used as a tunneling barrier, which has a high barrier height, voltage scaling is difficult. However, high-k dielectrics as tunneling/control dielectrics ensure further reduction of the device footprint and improvement in the performance of the devices. Where SiO2 is being used as a tunneling barrier, which has a high barrier height, voltage scaling is difficult. However, high-k dielectrics as tunneling/control dielectrics ensure further reduction of the device footprint and improvement in the performance of the devices. In this research SiGe nanocrystals (NC) by LPCVD were used to fabricate memory transistors with HfO2 as well as SiO2 tunneling / control dielectrics. Nanocrystals in the SiO2 layer were produced by the MBE grown SiO2 and SiO2 characterized by atomic force microscopy (AFM). Auger electron spectroscopy (AES), x-ray photoelectron spectroscopy (XPS), cross-sectional TEM (X-TEM), and Raman spectroscopy methods. Recently it was found that at lower pressures (0.5 Torr) the properties of dielectric substrate do not seem to play a major role in SiGe NC deposition from the fact that the density, distribution, and minimum size are roughly the same. Meanwhile, material composition depends on the deposition pressure, deposition time, substrate temperature, and on underlying substrate material (nucleation site density) as measured by AES, AFM. The XPS analysis reveals that there are various states of Ge up to +4 but Si is found to have only zero oxidation state.

Multiple oxidation state of Ge(0+/+2) alloyed with Si9 can lead to various defects in NCs, which can be discrete charge storage nodes in memory devices. The cross-sectional TEM pictures show the presence of, partially crystalline and electrically isolated, SiGe NCs embedded in SiO2 and HfO2. Memory effects were clearly observed at room temperature from floating gate MOSFET devices: threshold voltage shift for electrical stress of about 0.8 V, with a retention time of about 1.8 V. Furthermore, we demonstrate using CHE is faster than that using FN. MOS memory devices containing semiconductor nanocrystals have drawn considerable attention recently, due to their advantages when compared to the conventional non-floating memories [1]. At the same time is only a little work done on memory devices containing metal nanocrystals [2,3]. Despite the fact that this would have given them many advantages in comparison with devices based on semiconductor nanocrystals. The main aim of these efforts is to increase the retention time of carriers within the nanocrystals, without increasing the power consumption of the device and without decreasing the time of write/erase process. By using metal nanocrystals we have in our disposal a large variety of work functions and it is easier to tradeoff between the speed of write/erase process and the charge retention time. In this work we describe the fabrication of a MOSFET device with embedded Pt nanoparticles in the SiO2/HfO2 interface of a MOS device. We chose to work with Pt nanocrystals due to the fact that they have a large work function. In addition, using as upper oxide a high-k oxide our device, has a great degree of scalability. On n-Si (100) wafers we deposited 3.5 nm of SiO2 (tunnel oxide) using Chemical Vapor Deposition. On top of this surface we deposited a very thin (1 nm) platinum (Pt) layer. Separate Pt nanoparticles of high density were formed. Then we evaporated HfO2 oxide with a second electron gun at 200 °C in a nitrogen rich ambient, so that this oxide becomes stoichiometric as possible. The above device shows a clear hysteresis behavior on C-V characteristics. No hysteresis was observed in similar samples that did not contain nanocrystals. References: 1) S. Tiwari et al., Small silicon memories-confinement, single-electron, and interface state considerations, Appl. Phys. A, Vol. 71, p.403-414 (2000) 2) Z. Liu et al., Metal nanocrystals memories. Part I: Device, design and fabrication, IEEE transactions on electron devices, vol. 49 (9),p.1695-1613, September 2002 3) Q. Wang et al., Synthesis and electron storage characteristics of isolated silver nanodots on/ embedded in Al2O3 gate dielectric, article in press Applied surface Science (2004).

D6.5 Zn Nanocrystal Formation by Photo-MOCVD Method.

Kyoungkang Sung1, Sanggu Kim, Seungyong Myong and Jeongwon Kim2; 1Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea; 2Institute of materials Science, National Centre for Research "Demokritos", Ag. Parnasli Attikis, Athens, Greece.

Recent research on nanocrystal memories employing discrete traps as a charge storage medium has attracted a lot of research attention as the promising candidates to replace conventional DRAMs or Flash memories. Until now, for nanocrystal floating gate memory fabrication, most researches are focused on Si or Ge nanocrystal memories. However, in order to minimize the good read disturb characteristics in Si or Ge nanocrystal memories, the programming voltages cannot be scaled down easily. Interface and dopant fluctuations at the Si/Ge nanocrystal interface also cause device design difficulty. On the other hand, metal nanocrystals have many advantages over the semiconductor counterparts including high density of states around the Fermi level, stronger coupling with the conduction channel, it is easier to get desirable transfer functions, and smaller energy perturbation due to carrier confinement. Metal nanocrystals also provide a great degree of scalability for the nanocrystals size. However, most researches to fabricate metal nanocrystals are concentrated on evaporation or sputtering method,
followed by thermal annealing. These methods are complicated and time-consuming. In this paper, a new method for metal nanocrystal fabrication is presented, which is based on photo-MOCVD (Metal-Organic-Chemical Vapor Deposition) method. Photo-MOCVD is based on photo-chemical process involving photo-dissociation. The photon wavelengths emitted from the mercury light source are 184nm and 254nm. In this work, a diethylzinc (DEZ) source was used to fabricate Zn nanocrystal and decomposed by the UV source. DEZ source is heated in the thermostat to 20 °C and carried from source cylinder to the reactant chamber by Ar carrier gas. The system was evacuated to 10-6 Torr, then passivated with a monolayer of DEZ by UV source. AFM (Atomic Force Microscope) and SEM (Scanning Electron Microscope) were used to identify the Zn nanocrystal. As a result, dense Zn nanocrystals were obtained when the chamber pressure was 2 Torr, the substrate temperature was set to 150 °C; flow rate of carrier gas was set to 30 sccm, and the process time was 1 min. Dense Zn nanocrystals fabricated by photo-MOCVD can be easily applied to the Zn nanocrystal memory.

D6.6 Oxidation of Si nanocrystals obtained by low energy ion implantation in a thin SiO2 layer. Hubert Coffin1, Caroline Bonafos1, Nikolay Cherkasshin1, Sylvie Schamman1, Gerard Ben Assayag1, Gerald Zanchi1, Panagiotis Dimitrakis1, Pascal Normand2, Marc Tracqui3, Alain Chaverrier1

Fundamentally it is not physical vapor deposition but chemical vapor deposition method. Hence, there are several parameters to adjust for optimal condition such as chamber pressure, flow rate of carrier gas and substrate temperature. In the experiment, DEZ was set to 20 °C and the chamber pressure was set to 150 °C, and the flow rate of carrier gas was changed from 20 sccm to 50 sccm. Thereafter, Zn nanocrystal shape was investigated with the process time varied. AFM (Atomic Force Microscope) and SEM (Scanning Electron Microscope) were used to identify the Zn nanocrystal. As a result, dense Zn nanocrystals were obtained when the chamber pressure was 2 Torr, the substrate temperature was set to 150 °C; flow rate of carrier gas was set to 30 sccm, and the process time was 1 min. Dense Zn nanocrystals fabricated by photo-MOCVD can be easily applied to the Zn nanocrystal memory.


D6.9 The Effect of Composition and Annealing Environment on Fabrication of Nonvolatile Memory using E-beam Deposition of Silicon-rich Silicon Oxide. Daigil Cha1, Jung H. Shin1, Soo-Hwan Jeong2, Young Kwan Cha2 and In K. Yoo2

Physics, KAIST, Daejeon, South Korea; 2U-team, Samsung Advanced Institute of Technology, Suwon, South Korea.

Nanocrystal Si (nc-Si) based nonvolatile memory devices have received much attention recently as a promising alternative to conventional poly-Si based floating gate memory devices, with promises of low-voltage programming with a faster programming speed and improved retention time. In fabricating such nc-Si memory, easy, manufacture-friendly formation of a dense, uniform layer of small nc-Si with controlled separation from the channel is the key. In this paper, we report on fabricating such nc-Si memory with a 3 nm sized nc-Si with electron-cyclotron resonance plasma enhanced chemical vapor deposition (ECR-PECVD). 3 nm thick SiOx (x=2) layer was deposited on a p-type Si substrate with 4 am thick thermal oxide by ECR-PECVD using SiH4 and O2. After deposition of the SiOx layer, a 7 nm thick gate oxide of stoichiometric SiO2 layer was deposited by reducing the SiOx layer, thus producing the entire non-Si memory structure in one simple deposition step. After deposition, nc-Si was precipitated inside the SiO2 layer and anneal at 960°C. High-resolution transmission electron microscopy revealed formation of a single layer of a dense array of nc-Si, and confirmed that the diameter and location of the nc-Si were controlled by the thickness of the original SiO2 layer and the thermal oxide layer.
respectively. High-frequency capacitance - voltage (CV) measurements show clear charge-trap and memory effects due to the nc-Si with flat band shift of 2.8 V, corresponding to electron/hole trap density of (4 × 10^{12} / 3 × 10^{12} cm^{-2}), and negligible distillation of stored charge even after 48 hrs. Interestingly, such memory effects were observed only when the sample was annealed in oxidizing environment (9/5 mixture of N_{2} and O_{2}) and not during the anodization in inert environment (Ar). Furthermore, formation of nc-Si in 3 nm thin SiO_{x} layer required a much higher excess Si content than that necessary for a thick SiO_{x} film. These results indicate that precipitation kinetics of nc-Si-Si layers may be significantly different from that of SiO_{x} layers, and that in - situ oxidation of the SiO_{x} layer plays an important role in determining the precipitation kinetics. A more detailed analysis of the oxidation and precipitation kinetics and memory effects will be presented.

D6.10 Abstract Withdrawn

D6.11 Abstract Withdrawn

D6.12 Small Magnetic Clusters of Ga and In with As and V. Liudmila A. Pozhar', Alan T. Yeates', Frank Szmulowicz and William C. Mitchell. 1Chemistry, Western Kentucky University, Bowling Green, Kentucky; 2Polymer Materials Branch, Materials and Manufacturing Directorate, Air Force Research Lab, Wright-Patterson Air Force Base, Ohio; 3Sensor Materials Branch, Materials and Manufacturing Directorate, Air Force Research Lab, Wright-Patterson Air Force Base, Ohio.

GaAs and InAs molecules, and the smallest pre-designed clusters of Ga and In with As have been recently studied \cite{1} in detail by means of the Hartree-Fock-based, multi-configurational self-consistent field (MCSCF) method. The data so obtained proved that manipulations with the cluster structure, stoichiometry and form can lead to changes up to an order of magnitude in clusters' electronic energy level patterns and direct optical transition energies. In this work the above studies have been extended to include several small, pre-designed magnetic clusters of Ga and In with As atoms some of which are replaced by V atoms. With magnetic semiconductors element clusters, a prediction that experimentally developed clusters may be more functional if grown in confinement, can be of utmost importance. The major reason is that the density of magnetic memory elements confined in sub-nanoscale pores arrays provided by alumina and silica membranes (pore width of several atomic diameters) can be increased by several orders of magnitude as compared to that existing at present. At the same time, the confinement may reduce significantly spin-disordering temperature effects, thus preserving desirable ferromagnetic properties of such confined magnetic semiconductor clusters or wires. The pre-designed small pyramidal clusters of Ga-As-V and In-As-V atoms have been studied by means of the Hartree-Fock-based, MCSCF method. Their electronic energy level patterns and optical transition energies were compared to those specific to "pure" small Ga-As and In-As clusters of the same structure and numbers of Ga and In atoms studied earlier. This comparison allows elucidation of the effects of inclusion of magnetic semiconducting properties of magnetic semiconductor element clusters. 11.1 A. Pozhar, A.T. Yeates, F. Szmulowicz and W.C. Mitchell, Small Atomic Clusters: Templates for Sub-Nanoscale Heterostructure Units with Pre-Designed Charge, Transport Properties, Phys. Rev. Lett. (2004, in press); L.A. Pozhar, A.T. Yeates, F. Szmulowicz and W.C. Mitchell, Virtual Synthesis of Sub-Nanoscale Materials with Prescribed Physical Properties, 2003 Fall Meet. Proc. Sym. L. Continuous Nanophase and Nanostructured Materials, Eds. S. Komarneni, J.C. Parker and J.J. Watkins, December 1-5, Boston, MA (6 p), in: MRS Proceedings, 788, LI1.40 (6p) (2004); L.A. Pozhar, A.T. Yeates, F. Szmulowicz and W.C. Mitchell, Virtual Fabrication of Electronic Materials of Prescribed Physical Properties, Proc. 2003 Ann. AICHE Meet., November 16-20, 2003, San Francisco, CA (10 p).


Chalcogenide semiconductors have attracted much attention because of their interesting electrical, optical and thermal properties. For example, Ge_{2}Sb_{2}Te_{5} material can be used in the phase-change rewritable optical disk and nonvolatile memory due to its different electrical and optical properties at amorphous and crystalline states. Our group has studied Ge_{2}Sb_{2}Te_{5} films in order to improve the phase-change process and the phase-change was taken place by laser irradiation or pulse current heating. In this paper, we studied Ge_{2}Sb_{2}Te_{5} films at different temperatures and showed some interesting results observed. A KrF excimer laser was used as the external energy source. The phase-change Ge_{2}Sb_{2}Te_{5} target mounted at 45 degree with respect to the laser beam. Single-crystal Al2O3 and Si substrates were mounted on a stainless steel holder by silver paste with a distance of 5 cm from the facing target. A background pressure of 10-6 Torr was achieved with a turbomolecular pump. The films were deposited at laser fluence of 2 J/cm² and a repetition rate of 10 Hz. After film growth, substrates were cool down to room temperature at the same pressure. Six groups of Ge_{2}Sb_{2}Te_{5} films were prepared at the different growth temperatures. Another two groups of samples grown at room temperature were annealed for ten minutes at high temperatures. We found that no films were grown on the substrates at 340 °C or above. At 300 °C or below, films can be obtained on the substrates. This indicates the critical growth temperature of Ge_{2}Sb_{2}Te_{5} films is between 300 and 340 °C. The electrical and optical properties as well as crystal structures of thin films at different growth temperatures were analyzed by four-probe measurement, Hall effects, Ellipsometer and XRD. It was found that resistivity, carrier density and n & k of thin films strongly depend on the growth temperature.


Fusion de nouveau ferromagnetic insulator (FI) thin films is important in order to observe the spin-filter effect as FI tunnel barriers can form the basis for the realization of quantum computer devices \cite{1}. In general, ferromagnetic insulators (FI) are not common because in most insulating solids spins tend to order antiferromagnetically. A few ferromagnetic insulators belonging to the Europia-chalcogenide family are known, however the corresponding Curie temperatures are far below room temperature \cite{2}. In a recent work, we have observed giant moment and above room temperature ferromagnetism in Co-doped Hafnia films \cite{3}. Hafnia (HfO_{2}) thin films have the potential to replace SiO_{2} layers in MOS devices due to their low-leakage current rates. We report in this work the observation of interesting magnetic properties of dilutely Co-doped (5 mol%) high-k dielectric HfO_{2}, and other systems viz., CeO_{2} (CEO), Sm_{2}O_{3} (STO) and In_{2}O_{3} (INO). Above room temperature ferromagnetism is observed in all the systems in their epitaxial thin film form. Giant magnetic moment (6.8 B/Co) is observed in HfO_{2}:Co thin films grown by PLD and the moment varies for other thin film systems (CEO, STO and INO) for the same amount of Co-doping. Recently a great deal of interest has been generated worldwide in the search for ferromagnetism in doped magnetic systems \cite{4,5}. However, all such systems are either conducting or semiconducting in contrast to the current case of highly insulating matrix. Co-doping in Hafnia stabilizes the monoclinic phase at low growth temperature (750°C). Magnetic moment observed as a function of time was quite stable and was fitted to an equation of the type M_{2} = M_{0} exp (-t/τ), where M_{0} and M_{2} are the initial (starting) and final time of the measurement. The value of t = 106 s which indicates a robust ferromagnetism. TEM results do not show the formation of clusters and Co-valence state observed from EELS study is +2. Rutherford backscattering (RBS) studies indicate the stabilization of the monoclinic phase. Our preliminary results also show magnetism in room temperature grown Co-doped Hafnia thin films on Si-substrate. Magnetism in HfO_{2}:Co thin films can have prospective applications in devices. The relationship between the dielectric constant and magnetic moment will be discussed in the context of a vacancy (defect) model. 1. D. P. DiVincenzo, J. Appl. Phys. 83, 4785 (1995). 2. L. Esaki, P.J. Stiles, and S. von Molnar, Phys. Rev. Lett. 19, 852 (1967). 3. M.S.R. Rao et al. Phys.Lett. (submitted) 4. J.K. Furdyna, J. Appl. Phys. 64, R29-R64 (1988). 5. S.B. Ogale et al. Phys. Rev. Lett. 51, 4720 (2003). The authors acknowledge the support received from DARPA (grant # N000142010992) and NSF-MBSEC (# DMR-00-80098).

D6.14 Growth Temperature and Properties of GeSb/Te Films. Wendi Cong, Lu Ping Shi, Xianghao Miao, Xiang Hu, Rong Zhao and Joon Fatt Chong; Data Storage Institute, Singapore, Singapore.

Chalcogenide semiconductors have attracted much attention because of their interesting electrical, optical and thermal properties. For example, Ge_{2}Sb_{2}Te_{5} material can be used in the phase-change rewritable optical disk and nonvolatile memory due to its different electrical and optical properties at amorphous and crystalline states. Usually, Ge_{2}Sb_{2}Te_{5} films are prepared at the room temperature. The phase-change was taken place by laser irradiation or pulse current heating. In this paper, we studied Ge_{2}Sb_{2}Te_{5} films at different temperatures and showed some interesting results observed. A KrF excimer laser was used as the external energy source. The phase-change Ge_{2}Sb_{2}Te_{5} target mounted at 45 degree with respect to the laser beam. Single-crystal Al2O3 and Si substrates were mounted on a stainless steel holder by silver paste with a distance of 5 cm from the facing target. A background pressure of 10-6 Torr was achieved with a turbomolecular pump. The films were deposited at laser fluence of 2 J/cm² and a repetition rate of 10 Hz. After film growth, substrates were cool down to room temperature at the same pressure. Six groups of Ge_{2}Sb_{2}Te_{5} films were prepared at the different growth temperatures. Another two groups of samples grown at room temperature were annealed for ten minutes at high temperatures. We found that no films were grown on the substrates at 340 °C or above. At 300 °C or below, films can be obtained on the substrates. This indicates the critical growth temperature of Ge_{2}Sb_{2}Te_{5} films is between 300 and 340 °C. The electrical and optical properties as well as crystal structures of thin films at different growth temperatures were analyzed by four-probe measurement, Hall effects, Ellipsometer and XRD. It was found that resistivity, carrier density and n & k of thin films strongly depend on the growth temperature.
Understanding polarization switching behaviors in ferroelectric (FE) films is of great importance in both scientific interests and practical applications. Multiferroic materials are expected to be widely used in a variety of electronic devices and sensors. Therefore, the basic understanding of polarization switching behaviors has been of great importance.

In thin films of Bi_xO_y Sr_y Ta_z O_{(y+z)} and Sr_y Bi_{y+1} Ta_z O_{(y+z)} (SBT) were deposited by metalorganic chemical vapor deposition (MOCVD) on 150 mm silicon (100) wafers that were pre-treated with Pt or Ir electrodes. The substrate temperature and the deposition pressure were varied from 300 to 650 C and from 0.35 to 7 mbar, respectively. Translational bisulphate (Bi(III) or triphenylbisulphide (Bi(III)) and strontium bisperchloroethylenoxide tantalate (Sr(III)O(III)Ta(III)Cl(II)O(II)Me(III)) were used as Bi precursor and as Sr-Ta precursor, respectively. A liquid delivery system was used to supply and to vaporize the precursor into the reactor. X-ray photoelectron spectroscopy (XPS), ellipsometry, and chemical bonding measurements were carried out to characterize the film properties. The growth rate of the MOCVD of Bi_xO_y and Sr_y Bi_{y+1} Ta_z O_{(y+z)} was compared to the growth rate of SBT to obtain information about mutual interactions between the precursors. The growth rate of bismuth oxide thin films deposited from triethylbismuth was low (10 nm/h at 0.35 mbar) and did virtually not depend on the temperature. On the contrary, the growth rate of strontium tantalate films decreased strongly on the substrate temperature. The deposition rate of SBT films was similar to rate of the bismuth oxide film deposition, which slightly increased with increasing substrate temperature. However, the deposition rate of SBT was always lower than the deposition rate of the single precursors. The growth rate significantly depended on the deposition pressure. A decrease of the deposition pressure in the reactor chamber reduced the deposition rate of Bi_xO_y, Sr_y Ta_z O_{(y+z)} and SBT on the other hand, it improved the uniformity of the film thickness. The XPS measurements showed a deficit of bismuth in the SBT films even though the concentration of the Bi precursor was several times higher compared to the other precursors. The XPS depth-profiling by Ar+ ion sputtering indicated differences in bond characteristics of Ti, Sr, and Bi before and after ion beam bombardment.

A new phase change memory cell using resistance transition between two crystalline phases of (Ge_xSb_yTe_z)_{(x+y+z)} alloy is proposed in this study. Sn Bi_2Te_4 of 20 mole% not only accelerates the crystallization of Ge_xSb_yTe_z through forming a complete solid solution alloy but also changes the basic concept of binary phase transition memory element which has amorphous and crystalline (fcc) states. In this new phase change memory device, phase change material has no amorphous phase but the data is stored in different forms of crystalline phases. Transition of cell resistance from low conducting crystalline state (fcc) to high conducting crystalline state (hcp) and vice-versa is very abrupt and fast (<70 ns), and also each cell resistance values correspond the resistivity of each phases of (Ge_xSb_yTe_z)_{(x+y+z)} alloy. This is a strong advantage for the low power circuit which is needed for direct observation of fast fcc to hcp transformation by electrical stress, however this phenomenon will increase the cyclability of the device since it reduces the volume change between two phases.

All-organic single-transistor permanent memory device.

**D6.16**

**Material Characteristics Change in Ge_xSb_yTe_z Film through its Patterning Processes for Phase-Change Random Access Memory Integration.** Byung-Ok Cho, Suk-Hoo Jou, Kyung-Rae Byun, Jong-Chan Shin, Hee-Seok Kim, U-In Chung, and Jong-Tae Moon; Process Development Team, Memory Division, Samsung Electronics Co., Ltd., Yongin-City, Gyeonggi-Do, South Korea.

PRAM (Phase-Change Random Access Memory) is a non-volatile memory device based on the drastic resistivity change between amorphous and crystalline phases of its core material, i.e., chalcogenide film such as GST (Ge_xSb_yTe_z). Though dry etch and ashing for the patterning of GST film are key processes to the PRAM high-density or high-speed memories, few researches have been reported on the impact of the processes on the material characteristics and the electrical behaviors of the film. In this article, we investigated the effect of process conditions on the crystallization of GST pattern, the film surface composition and chemical bonding, and the film structure. We chose a combination of etch gases as basic dry etch chemistry for the GST patterning based on a thermodinamic analysis.

We prepared p-type Si wafers on which silicon oxide bottom layer, N-doped GST, TiN top electrode, and silicon oxide hard mask were sequentially deposited and finally photo-patterned as test samples. We obtained an optimal process window for the best etch profile considering the sidewall undercut and the bottom residues. We observed plasma gas phase by OES (optical emission spectroscopy) and found that Ge atomic peak at 305 nm best represented the GST etch process in the plasma so the peak was set as the main EPD (end point detection) signal. We analyzed the surface atomic compositions and chemical bonding of GST film changing from their as-deposited to post-etch and post-ashing states by XPS (X-ray photoelectron spectroscopy). We also used TEM (Transmission electron microscopy) and EDX (Energy Dispersive X-ray Spectroscopy) for the change in the structure and compositions through patterning of real PRAM devices.

Finally, we investigated potential device issues that can be related to the changes in material characteristics mentioned above.

**D6.17**

Preparation of Strontium Bismuth Tantalate Thin Films by Liquid-Delivery Metalorganic Chemical Vapor Deposition. Masaaki Sugimoto, Takahiro Omata; Matsuyama University, Matsuyama, Japan; 1Kalkoen, Tatiana Hur'eva; 1Bernd Garke 2and Edmund Burtle; 1Institute of Micro and Sensor Systems, Otto von Guericke University Magdeburg, Magdeburg, Germany; 2Institute of Theoretical Physics, Otto von Guericke University Magdeburg, Magdeburg, Germany.

Thin films of Bi_xO_y Sr_y Ta_z O_{(y+z)} and Sr_y Bi_{y+1} Ta_z O_{(y+z)} (SBT) were deposited by metalorganic chemical vapor deposition (MOCVD) on 150 mm silicon (100) wafers that were pre-treated with Pt or Ir electrodes. The substrate temperature and the deposition pressure were varied from 300 to 650 C and from 0.35 to 7 mbar, respectively. Translational bisulphate (Bi(III) or triphenylbisulphide (Bi(III)) and strontium bisperchloroethylenoxide tantalate (Sr(III)O(III)Ta(III)Cl(II)O(II)Me(III)) were used as Bi precursor and as Sr-Ta precursor, respectively. A liquid delivery system was used to supply and to vaporize the precursor into the reactor. X-ray photoelectron spectroscopy (XPS), ellipsometry, and chemical bonding measurements were carried out to characterize the film properties. The growth rate of the MOCVD of Bi_xO_y and Sr_y Bi_{y+1} Ta_z O_{(y+z)} was compared to the growth rate of SBT to obtain information about mutual interactions between the precursors. The growth rate of bismuth oxide thin films deposited from triethylbismuth was low (10 nm/h at 0.35 mbar) and did virtually not depend on the temperature. On the contrary, the growth rate of strontium tantalate films decreased strongly on the substrate temperature. The deposition rate of SBT films was similar to rate of the bismuth oxide film deposition, which slightly increased with increasing substrate temperature. However, the deposition rate of SBT was always lower than the deposition rate of the single precursors. The growth rate significantly depended on the deposition pressure. A decrease of the deposition pressure in the reactor chamber reduced the deposition rate of Bi_xO_y, Sr_y Ta_z O_{(y+z)} and SBT on the other hand, it improved the uniformity of the film thickness. The XPS measurements showed a deficit of bismuth in the SBT films even though the concentration of the Bi precursor was several times higher compared to the other precursors. The XPS depth-profiling by Ar+ ion sputtering indicated differences in bond characteristics of Ti, Sr, and Bi before and after ion beam bombardment.
orders of magnitudes better than regular transistor/capacitor memory cells. The device operates flawlessly in air. The FerroFET, therefore, is a new type of memory similar to ferroelectric memories, but can be manufactured at a very small fraction of the cost and at ambient temperatures. Therefore, we anticipate that the FerroFET will be the choice of memory for organic transistors, as it is an inherently built-in ferroelectric memory transistor technology, exhibits excellent characteristics, and conserves energy in mobile modules due to the high memory retention.

D6-20
Contribution of α-Domain on the Ferroelectric Property of (100)/(001)-Oriented Epitaxial PZT Films, Hiroshi Funakubo 1, Hitoshi Moroioka 1, Risaue Ueno 1, Shintaro Yokoyama 1, Keisuke Saito 1, 2Tokyo Institute of Technology, Yokohama, Japan, 2PA, Nalysychev, Tokyo, Japan.

Epitaxially grown (100)/(001)-oriented epitaxial PZT films have been thoroughly investigated to understand the characteristics of the PZT because of the lack of the single crystal data. However, the systematic research for the films by changing the volume fraction of (001) orientation, has been hardly reported. We have already succeeded in growing perfectly polar-axis-, (001)-oriented Pb(Zr0.52Ti0.48)O3 films by MOCVD and succeeded in obtaining the large spontaneous polarization value up to 90 μC/cm2. In the present study, we grew the (100)/(001)-oriented epitaxial PZT films with α(001) and investigated the change of the electrical property of the films with α(001). Epitaxial Pb(Zr0.52Ti0.48)O3 films with α(001) from 6 to 100% were grown on (100)SrRuO3/(100)SrTiO3 substrates by changing the deposition temperature and the film thickness. α(001) decreased with decreasing the deposition temperature and the film thickness. α(001) was not detected. This shows that the obvious contribution of (001) orientation, α(001), has been detected within the limit of the present study.

D6-21
Enhanced Spontaneous Polarization of Dysprosium-substituted Lead Zirconate Titanate Thin Films by a Chemical Solution Deposition Method, Hiroshi Uchida 1, Hiroshi Nakaki 2, Shoji Okamoto 2, Shintaro Yokoyama 2, Hiroshi Funakubo 2, Seiichiro Koda 1, 1Department of Chemistry, Sophia University, Tokyo, Japan; 2Department of Innovative and Engineering Materials, Tokyo Institute of Technology, Yokohama, Japan.

Enhancing the ferroelectric properties of lead zirconate titanate (Pb(Zr,Ti)O3; PZT) film is required for developing the integration of nonvolatile, high speed and inexpensive memory devices. We attempted the improvement of ferroelectric properties of PZT films by promoting the anisotropy of simple-perovskite crystal. Crystal anisotropy of PZT was controlled by the species and occupying site of substituent cation; B-site substitution using rare-earth cations whose ionic radii locate on larger parts of its series (such as La3+, Gd3+, Dy3+, Yb3+, etc.) can promote the anisotropy of PZT crystal, i.e., the ratio of PZT lattice parameters (c/a), whereas inverse phenomenon occurs in the case of A-site substitution using rare-earth cations whose ionic radii locate on larger parts of its series (such as La3+, Nd3+, etc.). In this study, authors especially focused on the dysprosium (Dy3+) ion as a substituent cation for improving the ferroelectric properties of PZT films because Dy3+ ion has relatively larger ionic radius in the group of rare-earth cations that are to occupy B-site in PZT crystal. The influences of the ion substitution using Dy3+ ion on the ferroelectric properties of PZT films were investigated. PZT-based films were fabricated by a chemical solution deposition method. Spin-coating solutions with chemical compositions of Pb1-x/2Nd1/2(Dy2/3(0.33)Zr4/3(0.66)Ti0.33)O3 and Pb1-x/2La1/2(Zr0.46Ti0.54)O3 (denoted A-PDZT and B-PDZT respectively) were prepared using lead acetate, zirconium iso-propoxide, dysprosium-butoxide, niobium pentoxide, nitrate and 2-methoxyethanol as starting materials. These solutions were spin-coated on (111)Pt/ Ti/SiO2/Si(100) and (111)SrRuO3/(111)Pt/(100)YSZ/100)Si substrates. The film thicknesses of the films were measured by a white light interferometer. The spontaneous polarization and dielectric constant of the films were measured in the range of 0.1-100 GHz. The films were also characterized using X-ray diffraction, X-ray photoelectron spectroscopy (XPS), atomic force microscopy and scanning electron microscopy. Based on these results, accompanying with these results, we will propose a model of microscopic phenomena.

8:30 AM PT7.1
Organic Thin Film Nonvolatile Memory Devices, Yang Yang Materials Sci. & Eng., UCLA, Los Angeles, California.

Organic functional thin films and related devices, with emphasis on LEDs, transistors, and solar cells, have attracted strong attention in the past decade. On the other hand, organic memory devices have only been demonstrated for the most important electronic devices, was left untouched until recently when a high performance organic bistable and memory was reported. (Appl. Phys. Lett. 82, 1419, (2003)) The UCLA organic memory devices take the advantages of the nano technology incorporated nano-particles into the organic matrix system. The performance of the devices makes them attractive for memory cell type of applications. The two states, the 0 and 1 states, of the devices differ in their electrical conductivity by several orders in magnitude and show remarkable stability, i.e., once the device reaches either state, it tends to remain in that state for a prolonged period of time. More importantly, the high and low conductivity states of our memory devices can be precisely controlled by the application of a positive voltage pulse (to write) or a negative voltage pulse (to erase), respectively. These organic memory devices can be formed by either large-area vacuum coating technology or by wet polymer coating processing, are promising for forming two-voltage write-read memory devices having low-cost and high-performance advantages.

9:00 AM PT7.2
Organic Memory Devices Using C60 and Polymer, Aokik Kawal, Shashi Paul and Manish Chhowalla, Ceramics and Materials Engineering, Rutgers University, Piscataway, New Jersey.

The ease of fabrication and use of inexpensive substrates has generated tremendous interest in organic electronics [1] while molecular electronics offers the potential of miniaturization down to a few atoms. However, unlike organic electronic devices, molecular devices are extremely difficult to assemble making mass production impossible with the existing technology. Although several types of single molecule devices have been demonstrated, the integration of the most important electronic devices, was left untouched until recently when a high performance organic bistable and memory was reported. (Appl. Phys. Lett. 82, 1419, (2003)) The UCLA organic memory devices take the advantages of the nano technology incorporated nano-particles into the organic matrix system. The performance of the devices makes them attractive for memory cell type of applications. The two states, the 0 and 1 states, of the devices differ in their electrical conductivity by several orders in magnitude and show remarkable stability, i.e., once the device reaches either state, it tends to remain in that state for a prolonged period of time. More importantly, the high and low conductivity states of our memory devices can be precisely controlled by the application of a positive voltage pulse (to write) or a negative voltage pulse (to erase), respectively. These organic memory devices can be formed by either large-area vacuum coating technology or by wet polymer coating processing, are promising for forming two-voltage write-read memory devices having low-cost and high-performance advantages.

SESSION D7: Organic and Resistive Memories

Chairs: Shashi Paul and Dimitris Tsoukalas
Thursday Morning, December 2, 2004
Back Bay B (Sheraton)
fabricate high density two terminal voltage-switchable memory states can also be achieved. Device’s properties, Von, Voff, Vthreshold shape (i.e. with a negative differential resistance region). Multistable 9:30 AM D7.4 9:45 AM D7.5...
phase-change memory. Unlike the conventional single phase change layer, the SLL recording layer consists of alternating thin layers with two different phase change materials, i.e. GeTe and Sb2Te3. Although neither GeTe nor Sb2Te3 could be used as a phase change layer material, present experimental results have shown that the phase change memory with the SLL structure demonstrate a much better recordability that could match practical application requirements. The devices demonstrated remarkable performance of fast speed and small current. Different parameters of SLL phase change memory cell, such as thickness of elemental layer, ratio of GeTe to Sb2Te3, and total thickness of SLL layer, were varied and the properties were compared in order to get optimized structure. The mechanism and issues encountered was investigated by means of simulation and experiments. The issued encountered in designing the recording stacks are also discussed.

11:15 AM D7.8
Investigation of Resistive Switching in Cr-Doped SrZrO3 Perovskite Structures, Hwan-Soo Lee1, Sukwon Choi2, Paul A. Salvador2 and James A. Bain1,2,3. 1Electrical and Computer Engineering, Carnegie Mellon University, Pittsburgh, Pennsylvania; 2Materials Science and Engineering, Carnegie Mellon University, Pittsburgh, Pennsylvania; 3Data Storage Systems Center, Carnegie Mellon University, Pittsburgh, Pennsylvania.

We have prepared capacitor-like epitaxial thin film stacks of perovskite materials on SrTiO3 substrates having the following structures: substrate/SrRuO3/Cr (0.2 at.%)-doped SrZrO3/Ti/Au. These structures are similar to the reported by others [1], and were prepared by pulsed laser deposition (PLD). The SrRuO3 film as a bottom electrode was epitaxially grown on SrTiO3 (001) substrates. Half of the area of these electrodes was then masked off prior to the deposition of each SrZrO3 film. Both films were deposited at 700 °C and O2 pressure ranging from 50 mTorr to 150 mTorr. Electrodes of Ti/Au with diameter of 250 µm were sputter-deposited on top of the SrZrO3 film as well as on the exposed SrRuO3 film, using a second shadow mask. The epitaxy of the films was checked by x-ray diffraction (XRD) and transmission electron microscopy (TEM). The XRD spectra of the SrZrO3 films on SrTiO3 substrates showed strong (001) and (002) peaks at angles of 21.6° and 44.0°, respectively, in #29 scanning, with no other peaks in the range of 26° ± 20°. Well-defined fourfold symmetry in in-plane orientation was observed through a scan of the (111) peak of the SrTiO3 substrate. This suggests a good epitaxial growth along the (001) orientations. The lattice mismatch between the SrZrO3 films and the SrTiO3 (001) substrate is about 5.3%, calculated from the XRD spectra. In this study, we have focused on hysteretic behavior in resistance, which may permit their use in two terminal non-volatile memory devices. Electrical transport measurements with current perpendicular to the plane were carried out using a Keithley 2400 source meter in current-controlled mode. By sweeping the current (I) negative and subsequently to positive values (with respect to the bottom SrRuO3 electrode), a reversible and reproducible transition in junction resistance could be observed. Typical I-V characteristics of a 220-nm-thick SrZrO3 film showed resistance changes of a factor of approximately 10 between the high (as deposited) and low-resistance states, after accounting for the series resistance of the SrRuO3 electrode. Total measured resistances (junction plus contacts and electrodes) were in the range of 15 kOhms for the high resistance state and 3 kOhms for low resistance state, with approximately half of the latter value being electrode series resistance. Switching currents showed a variation of about ±30% in their values in for repeated cycling through the switching event. In this study, we further discuss process parameters such as oxygen pressure during growth and cooling, and their effects on hysteretic properties and switching behavior. References [2] A. Beck et al., "Reproducible switching effect in thin oxide films for memory applications," Appl. Phys. Lett., 77, 139 (2000).

11:30 AM D7.9
Effect of the Bottom Electrode Contact (BEC) on the Phase Transformation of N2 doped Ge2Sb2Te5 (NGST) in a Phase-Change Random Access Memory, Siyoun Lee1, Y. J. Song1, Y. N. Hwang1, S. H. Lee1, J. H. Park1, K. C. Ryu1, S. J. Ahn1, C. W. Jeong2, J. H. Oh3, J. M. Shin3, F. Yeung4, W. C. Jeong1, Y. T. Kim1, J. B. Park3, K. H. Koh4, G. T. Jeong4, H. S. Jeong5 and Kinam Kim6; 1Advanced Technology Development Team, Samsung Electronics, Yongin, South Korea; 2CAE Team, Samsung Electronics Co. Ltd, Yongin-City, South Korea; 3AE Lab, Samsung Advanced Institute of Technology, Yongin-City, South Korea.

With respect to the operation of a Phase-Change Random Access Memory (PRAM or PCM), we studied the dependence of the phase transformation of the N2 doped Ge2Sb2Te5 (NGST) on the electrical and thermal resistance of the BEC. The high resistive BEC was made by oxidizing the high conductive metallic BEC and the resistance was controlled with the extent of oxidation. We found that the needed current (Ireset) to amorphize that material was highly reduced with the increase of the temperature. This result was qualitatively consistent with the calculation of temperature profile using the heat transport equation in that material. In addition, we characterized a junction between NGST and BEC in the frame of the metal-amorphous semiconductor (M/a-Sm) junction and investigated the effect of the estimated junction parameters on the operation of a PRAM. Finally, the prospects of a high density PRAM using high resistive BEC will be addressed.