SYMPOSIUM H

Silicon Carbide–Materials, Processing, and Devices

November 27 – 29, 2000

Chairs

Anant K. Agarwal
Cree Research Inc
Durham, NC 27703
919-313-5539

James Cooper, Jr.
School of ECE
Purdue Univ
1285 EE Bldg
West Lafayette, IN 47907-1285
765-494-3514

Erik Janzen
Dept of Physics & Measurement Tech
Linkoping Univ
Linkoping, S-58183 SWEDEN
46-13-281797

Marek Skowronski
Dept of MS&E
Carnegie Mellon Univ
Pittsburgh, PA 15213
412-268-2710

Symposium Support
†Cree Inc.
II-VI, Inc.
†MMR Technologies, Inc.
Sterling Semiconductor, Inc.
†2000 Fall Exhibitor

**Proceedings published as Volume 640
of the Materials Research Society
Symposium Proceedings Series.**

* Invited paper

SESSION H1: SiC BULK GROWTH
Chairs: Erik Janzen and Shigehiro Nishino
Monday Morning, November 27, 2000
Room 202 (Hynes)

9:00 AM *H1.1
SiC CRYSTAL GROWTH FROM THE VAPOR AND LIQUID PHASE. Dieter Hofmann, Matthias Bickermann, Boris Epelbaum, Thomas Straubinger, Roland Weingaertner, Peter Wellmann, Albrecht Winnacker, University of Erlangen-Nuernberg, Dept of Materials Science 6, Erlangen, GERMANY; Lev Kadinski, Markus Selder, Dept of Fluid Mechanics, University of Erlangen-Nuernberg, Erlangen, GERMANY.

Recent advances of SiC based innovative devices in high power/high temperature electronics and production of group III-nitride optoelectronics are pushing both commercial SiC wafer suppliers and related resarch institutions to improve crystal quality for future industrial needs and understanding of the SiC bulk growth process, respectively. Although a considerable decrease of defect densities in 4H- and 6H-SiC wafers and increase of crystal diameter have been accomplished actually, micropipe elimination, reduction of dislocation density and stress, increase of yield and improvement of dopant non-uniformity are of permanent relevance in research and development. In this paper at first SiC crystal growth by physical vapor transport (PVT) is addressed. Characterization results of n- and p-type 4H- and 6H-SiC boules are presented with regard to crystalline defect density and distribution (micropipes, macrodefects, dislocations, stress fields, parasitic polytypes) and lateral/longitudinal dopant variations. The impact of PVT process conditions is analyzed with the support of numerical modelling. The simulation tools include heat transfer, mass transport, chemical processes and stress generation. The influence of thermal and constitutional fields are discussed concerning both crystalline defect formation and dopant incorporation. The status of the development of SiC liquid phase growth at our laboratory is introduced. Experimental results on achievable growth rates, crystal geometry and crystalline defect densities are shown. Of special interest is the evident discrepancy of micropipe propagation in SiC vapor and liquid phase growth. During PVT crystallization micropipes are propagating generally along the c-axis through the whole crystal whereas this defect can be closed during liquid phase processing. Finally experimental facts and models for the actual understanding of filamentory void formation (micropipes, macrodefects) and elimination during vapor and liquid phase growth, respectively will be presented.

9:30 AM *H1.2
HTCVD GROWTH OF SEMI-INSULATING 4H-SiC CRYSTALS WITH LOW DEFECT DENSITY. A. Ellison, C. Hemmingsson, Okmetic AB, SWEDEN; L. Storasta, B. Magnusson, A. Henry, Q. Wahab, N.T. Son and E. Janzén, Dept of Physics and Meas. Technology, Linköping University, SWEDEN.

The development of a novel SiC crystal growth technique, generically described as High Temperature Chemical Vapor Deposition (HTCVD) is reviewed. The structural, optical and electrical properties of 4H-SiC wafer demonstrators are investigated with the aim of developing high-frequency device quality semi-insulating SiC substrates.
Carried out at temperatures above 2100°C, the HTCVD technique uses, as in CVD, gas precursors (silane and a hydrocarbon diluted in a carrier gas) as source material. The growth process can, however be described as "Gas Fed Sublimation" and is shown to proceed by the gas phase nucleation of Si_x-C_y clusters, followed by their sublimation into active species that are condensed on a seed crystal. 4H and 6H-SiC crystals with diameters up to 40 mm have been obtained with growth rates of 0.5 to 0.7 mm/h.
Owing to the purity of the source material used in the HTCVD technique, 4H wafers prepared from undoped crystals (with vanadium concentration lower than 5×10^{14} cm^{-3}) exhibit semi-insulating behaviour with a bulk resistivity higher than 5×10^{9} Ω·cm at room temperature. The temperature dependence of the resistivity shows that the compensation mechanism is either dominated by a single deep-level (1.1 eV) or by two levels (~0.5 and 1.1 eV) in 4H-SiC. The possible origin of these levels is investigated, together with their thermal stability. The structural quality of high-resistivity wafers and mechanisms controlling micropipe defects formation are investigated. Specific process steps such as in-situ seed surface preparation and micropipe closing have in particular enabled growth of semi-insulating crystals with micropipe densities lower than 30 cm^{-2}.

10:30 AM H1.3
THE EFFECT OF MECHANICAL AND CHEMO-MECHANICAL SEED SURFACE PREPARATION ON THE DISLOCATION DENSITIES OF PVT GROWN SiC. E.K. Sanchez, M. Skowronski, Dept. of Materials Science and Engineering, Carneige Mellon University, Pittsburgh, PA; W. Vetter, M. Dudley, Dept. Materials Science and Engineering, SUNY Stony Brook, Stony Brook, NY; W.C. Mitchel, AFRL Wright Patterson AFB, OH.

Mechanical damage of seed surfaces due to cutting, lapping and polishing has been known to result in increased dislocation densities in single crystals. The standard process for SiC epitaxy includes an in situ HCl or hydrogen etch design to remove the damage. It is difficult, however, to incorporate such an etching step into the sublimation growth process. The effect of SiC seed surface preparation on dislocation densities in SiC overgrowth has been assessed by KOH etching, x-ray topography, and Atomic Force Microscopy. Lely platelets with very low dislocation densities have been used as seeds. Growth surfaces have been prepared by either mechanical polishing with diamond paste (one um grit size), chemo-mechanical polishing (CMP) with colloidal silica, and/or given an ex-situ high temperature hydrogen etch. PVT grown material on seeds finished with mechanical polishing exhibited a screw dislocation density on the order of $10^6/cm^2$ and an edge dislocation density on the order of $10^7/cm^2$. Screw dislocations with opposite sign Burgers vectors were arranged in pairs along scratches left behind by the mechanical polishing. Edge dislocations align along irregular shaped boundaries. Growth on CMP seeds resulted in screw dislocation densities on the order of $10^3/cm^2$ and edge dislocation densities of $10^5/cm^2$. However in between scratches these densities were one to two orders of magnitude lower. Hydrogen etching resulted in a monotonic decrease of dislocation densities with the amount of material removed. For on-orientation seeds the best samples exhibited screw dislocation densities of $10^2/cm^2$. The edge dislocations were arranged in pairs with densities on the order of $10^5/cm^2$. The depth of damage was estimated at 400-600 A. Platelets that were polished below the growth layer and into the Lely seed exhibited very low dislocation densities. This indicates that the dislocations are not created by plastic deformation. Hence, both screw and edge dislocations are created by nucleation at the initial stages of growth.

10:45 AM H1.4
HEAT AND MASS TRANSFER SIMULATION OF SiC BOULE GROWTH BY SUBLIMATION. Michel Pons, Michail Anikin, Jean-Marc Dedulle, Bernard Pelissier, Alexandre Pisch, Elisabeth Blanquet, Roland Madar, Etienne Pernot, Claude Bernard, Institut National Polytechnique de Grenoble, FRANCE; Cecile Moulin, Philippe Grosse, Christian Faure, LETI-CEA Grenoble, FRANCE.

The silicon carbide SiC semiconductor material is proving today, from intense scientific and industrial development, its potential to replace and outperform silicon in several or all electronic devices for high power, high frequency and high temperature applications. The potential of this material has been known since the fifties. The main reason for its late emergence is the difficulty to growth large electronic grade SiC single crystals. The continuing improvement observed so far is mainly the result of extensive experimental work. However, different computational tools have allowed to obtain important additional information to the wide experimental knowledge. The phenomena involved in the sublimation growth process are quite complex, they include heat transfer by electromagnetic heating, radiation, conduction and convection, multicomponent species transport and gas/surface chemistry. In particular, there is a strong need of a better control through simulation of the temperature field inside the growth chamber. This first step has proved its efficiency for the optimization of the local temperature field but its does not allow the direct determination of the growth rate and shape of the growing ingot. For this purpose, heat transfer must be coupled with gaseous species transport. In this presentation, the different models and databases will be first described. The standard geometry for the fabrication of SiC boules and the experimental verification of the computations will be presented. Secondly, the influence of some design modifications on heat transfer will be discussed. Thirdly, tentative simulations of the relations between process parameters, crystal shape, defect appearance and crack propagation will be proposed with more or less generic computations. Experimental results of our recent SiC bulk growth process development will complete the presentation and are included all along in order to verify experimentally the validity of the models.

11:00 AM H1.5
NEW CRUCIBLE DESIGN FOR SiC SINGLE CRYSTAL GROWTH BY SUBLIMATION. Shin-Ichi Nishizawa, Hirotaka Yamaguchi, Tomohisa Kato, M. Nasir Khan, Kazuo Arai, Upr, Electrotechnical Laboratory, Tsukuba, JAPAN; Naoki Oyanagi, Yasuo Kitou, Wook Bahng, Upr, R&D Association for Future Electron Devices, Tsukuba, JAPAN.

SiC bulk single crystal growth by sublimation was investigated numerically. Electromagnetic and temperature fields inside a growth furnace with various crucible designs were analyzed by finite element method. Results of calculation were compared to growth experiments in order to discuss the correlation between temperature distribution in a growth cavity and grown crystal shape. It was pointed out that grown crystal shape strongly depends on the temperature distribution

in a growth cavity. In addition, crystal growth rate has also strongly connection with temperature distribution and its gradient in a growth cavity. It is possible to control the grown crystal shape by modifying the temperature distribution inside a growth cavity. From these points of view, new crucible design, which is a double-crucible with inner-cone tube, for SiC bulk single crystal growth by sublimation was proposed, and its effect was confirmed by experiments. With this type of double-crucible, the uniformity of temperature distribution on the growing surface was so improved that a growing surface shape became flat in comparison with a case of standard crucible which grown surface was convex toward a growth cavity. Furthermore, in case of a double-crucible, temperature distribution inside a SiC source powder became more parallel to horizontal axis than in a case of standard crucible. Then SiC source sublimated uniformly for time and space. It deduced that a crystal growth rate kept constant. On the other hand, in case of standard crucible, crystal growth rate changed by time because temperature distribution and its gradient changed during the growth.

11:15 AM H1.6
INVERSE-COMPUTATION DESIGN OF LARGE-DIAMETER SiC BULK CRYSTAL GROWTH SYSTEM. Alexey V. Kulik, Svetlana E. Demina, Sergey K. Kochuguev, Dmitry Kh. Ofengeim, Sergey Yu. Karpov, Soft-Impact Ltd., St. Petersburg, RUSSIA; Mark S. Ramm, Alexander I. Zhmakin, A.F. Ioffe Physical-Technical Inst, St. Petersburg, RUSSIA; Anna A. Alonso, Sergey G. Gurevich, High Frequency Current Inst, St. Petersburg, RUSSIA; Yuri N. Makarov, Fluid Mechanics Dept, Univ of Erlangen-Nuernberg, Erlangen, GERMANY.

The studies of the last decade has clearly shown that sublimation growth of SiC bulk crystals as well as the properties of the grown material are entirely controlled by a particular temperature distribution in the growth system. Normally, direct modeling is used to optimize the thermal field in a growth system. For this purpose, coupled heat and mass transport are simulated for chosen geometries of the growth system to be designed. In fact, such a trial-and-error approach is based mainly on tentative considerations and experience of growth engineers. Direct modeling is, therefore, time consuming, rather expensive and likely ineffective in multi-factor optimization. In this paper we employ the inverse-problem modeling for optimization of SiC bulk crystal growth systems. This approach allows one to minimize handwork in the computations, to redesign quickly the system geometry for the solution of a particular growth problem by simple modification of a target function only. Upscaling of the growth system to get the crystal of a larger diameter becomes much more easy. The results reported provide a family of the growth systems optimal in terms of prescribed temperatures in the reference points, temperature gradients in the growth cavity and SiC powder, etc. A sensitivity of optimal configurations to variation of the material properties and to choice of target function and bound constrains is analyzed. A concept of multi-factor optimization is discussed. As the optimization target not only the temperature profiles but also some other factors can be considered, for instance, absence of undesirable poly-SiC deposits near the seed.

11:30 AM H1.7
6H-SiC BULK CRYSTAL GROWTH BY NOVEL SOLID PHASE EPITAXY. M. Hiramoto[1], Y. Asaoka[2], Tanino[1], Y. Yamada[1], N. Sano[2], T. Kaneko[2], [1]Nippon Pillar Packing CO., Hyogo, JAPAN; [2]Kwansei Gakuin University, Dept of Physics, Hyogo, JAPAN.

Silicon carbide is a material of great technological interest for high power, high frequency and high temperature device applications. The bulk SiC crystals have been grown mainly by sublimation method. However, the improvement of the crystal quality still remains a critical issue in terms of the reduction in micropipes and the enlargement in substrate size. In this research, we propose a novel growth method which is based on solid phase epitaxy to achieve micropipe-free 6H-SiC surface on a seed substrate. The experiments were conducted in a high temperature atmospheric annealing chamber employing a simple material configuration. The materials used were a CVD-grown poly-crystalline 3C-SiC(111) wafer as a "source" to be recrystallized and a 6H-SiC(0001) seed substrate wafer. Those wafers were simply aligned in pile vertically followed by mirror-polishing and chemical treatment. By increasing the process temperature up to 2300°C, the recrystallization of 3C-SiC(111) to 6H-SiC occurred at the interface where a small temperature gradient was inserted to maintain the substrate at lower temperature. The maximum growth rate exhibited 300um/h. The most notable phenomenan during this growth is the blockade of the propagation of the micropipes into the grown layer. The growth process was characterized by transmission electron microscopy as well as optical microscopy and Raman spectroscopy. We will discuss this novel growth mechanism in detail. This work was supported by the grant Advanced Technology Initiative for New Industry.

11:45 AM H1.8
INVESTIGATION OF SILICON CARBIDE GROWTH ON THE C-TERMINATED FACE OF 6H SEEDS BY PHYSICAL VAPOUR TRANSPORT. Detlev Schulz, Jürgen Doerschel, Institut für Kristallzüchtung, Berlin, GERMANY.

SiC epitaxial layers and crystals were grown by the modified Lely method. The C-terminated faces of 6H-SiC have been used as seeds. As-grown surfaces and axial cuts of crystals were examined by atomic force microscopy (AFM), optical microscopy (OM) as well as cathodoluminescence (CL). Early studies of Stein et al. claimed, that regardless of the seed polytype the 4H polytype had always been obtained using the C-terminated face during sublimation growth [1]. Kanaya et al. concluded from a detailed study that 4H crystal growth on C-terminated 6H seeds is favoured at lower temperatures, higher source-seed temperature difference and lower argon pressure as compared to 6H crystals [2]. Koga et al. investigated the polytype stability on both polar faces of 6H seeds by variing the temperature and the pressure reduction rate [3]. In contrast to [1] 4H crystals were only obtained on the C-terminated face at high temperatures. To shed more light on these contradictory results, polytype changes have been examined dependent on the growth conditions. There is a strong influence of the seed orientation on surface morphology. Using off-oriented substrates different step arrangements are visible for $< 11-20 >$ and $< 1-100 >$ off-direction. For the on-oriented case growth proceeds via the coalescence of individual islands, which are nearly flat. While growing crystals on both kinds of seeds the 6H polytype is maintained under low supersaturation. Instead of obtaining 4H crystals, inclusions of 15R are occasionally observed. In order to force the change from 6H to the 4H polytype the supersaturation has been increased. Especially during initial growth stages the 4H appearance is very sensitive to the growth pressure. During the evacuation period for the growth start the 4H polytype formation is favoured at low system pressures. Nevertheless, the induced polytype changes result in the deterioration of the crystalline quality. A lot of micropipes can by seen in such regions. [1] R.A. Stein, P. Lanig, S. Leibenzeder, Mater. Sci. Engineer. B11 (1992) 69-71 [2] M. Kanaya, J. Takahashi, Yu. Fujiwara, A. Moritani, Appl. Phys. Lett. 58 (1991) 56-58 [3] K. Koga, T. Yamaguchi, Prog. Crystal Growth Character. 23 (1991) 127-151

SESSION H2: SiC EPITAXY
Chairs: Hiroyuki Matsunami and Alexandre E. Ellison
Monday Afternoon, November 27, 2000
Room 202 (Hynes)

1:30 PM H2.1
DEFECT EVOLUTION IN 4H-SiC SUBLIMATION EPITAXY LAYERS GROWN ON LPE BUFFERS WITH REDUCED MICROPIPE DENSITY. Rositza Yakimova, Mikael Syväjärvi, Henrik Jacobsson, Anelia Kakanakova-Georgieva, Erik Janzén, Linköping Univ, Dept of Physics and Measurement Technology, Linköping, SWEDEN; Svetlana Rendakova, Vladimir Dmitriev, TDI Inc, Gaithersburg, MD.

A critical issue in SiC crystal growth technology is the formation of micropipes. During epitaxial growth for device structures, micropipes propagate into the epitaxial layer, thus becoming detrimental obstacles for large-area applications. We have previously shown that by using LPE on Si-terminated 4H-SiC substrates, micropipes can be cured and they do not evolve in the subsequently grown sublimation epitaxy layer. In this work we study defect evolution in similar structures by including results from growth on C-terminated surfaces with the aim to find optimal characteristics for buffer layers reducing the micropipes and thus giving device quality top layers. The results were analyzed using optical microscopy, SEM images, and synchrotron topography in back reflection mode. Laue patterns from large-area topographs were taken as well. The results show that nearly all (90%) of the micropipes in the substrate are terminated in the LPE layer while changes in the threading dislocation density can not be clearly resolved. We have observed dislocation networks uniformly distributed over the sample, which are not seen in the top layer grown by sublimation epitaxy. However this layer exhibits rough surface reflecting the roughness of the LPE layer, with morphological features characteristic of anisotropic step bunching and facet related defects. The dislocation appearance is different from that of the substrate with the buffer layer, although the etch pits dislocation density is slightly lower. We have found small size "new-born" micropipes pointing out the growth direction and shell-like etch pits. We relate these imperfections to growth disturbances on the rough buffer layer surface. The experimental findings are discussed in respect to the optimal buffer layer thickness, and the formation mechanism of micropipes originating in the top layer. The interpretations are in agreement with the earlier suggested model for micropipe healing. A relation between the LPE layer thickness, micropipe size and healing efficiency is proposed.

1:45 PM H2.2
HOLLOW DEFECT ELIMINATION DURING SOLUTION GROWTH OF SiC. B.M. Epelbaum, D. Hofmann, M. Müller and A. Winnacker, University of Erlangen-Nurnberg, Dept of Materials Science 6, Erlangen, GERMANY.

SiC solution growth was shown to be a promising technique to close micropipes and macrodefects in SiC wafers prepared by the PVT technique [1]. Using the top-seeded solution growth method we investigated systematically hollow defect elimination during 6H SiC solution growth over a wide temperature range from 1500°C to 2100°C. High-temperature experiments at 1800-2100°C were performed under pressurized argon atmosphere (100-130 bar) in order to prevent silicon melt evaporation [2]. Effective control of supersaturation was achieved by accurate adjustment of temperature gradients in the crucible and by forced melt convection. In the report comparative analysis of two different growth approaches will be given: epitaxial (LPE) growth of thick 50-100 μm layers on PVT grown substrates containing micropipes and macrodefects (a) and growth of bulk SiC crystals using point seeds cut from hollow-defect-free Lely platelets (b). LPE experiments were accomplished on (0001) 6H wafers grown in our laboratory. Grown samples were investigated using optical microscopy, AFM and SEM. (a) During LPE growth all hollow defects existing in a substrate show an evident tendency to act as growth centers and after an adequate period of liquid phase treatment they are overgrown. Growth morphologies observed in epilayer in the vicinity of hollow defects are rather different depending on defect type (mainly on dislocation content), substrate polarity and growth rate/supersaturation. Classification of hollow defects based on these observations will be presented, corresponding closing mechanisms will be discussed. (b) Crystals grown using a point seed are similar in morphology to those grown by the Lely method, but exhibit a more rough surface because of pronounced step-bunching. Typical defects of these crystals are flat silicon inclusions. Number of inclusions and their size are strongly dependent on forced melt convection. [1] M. Syvajarvi, R. Yakimova, H.H. Radamson et. al., J. Cryst. Growth, 197 (1999) 147 [2] D. Hofmann, M. Müller, A. Materials Science & Engineering B61-62 (1999) 29

2:00 PM H2.3
GROWTH OF MESFET STRUCTURES BY HOT-WALL CHEMICAL VAPOUR DEPOSITION. U. Forsberg[1], M.K. Linnarsson[2], A. Henry[1], and E. Janzén[1]; [1]Dept of Physics and Measurement Technology, Linköping University, Linköping, SWEDEN; [2]Solid State Electronics, Royal Institute of Technology, Stockholm, SWEDEN.

The hot-wall SiC CVD reactor was developed in our group several years ago to be able to grow thick low-doped layers with good morphology for power devices. The aim of the present study is to find out whether the use of hot-wall reactors compared to cold-wall reactors will improve the performance of high frequency devices as much as for high-voltage devices.
We will here report doping and abruptness of MESFET structures grown in a hot-wall CVD reactor with a SiC coated susceptor on both semi insulating and n-type 4H-SiC substrates. The growth parameters have been optimised for grow of thin (<200 nm) layers with good doping and thickness uniformity. By using relatively low growth rate (<4 μm/h), very abrupt doping profiles have been obtained for both p- and n-type layers.
SIMS measurements have been performed of both nitrogen and aluminium concentrations in a MESFET structure with a cap layer (n-type, 150 nm), a channel layer (n-type, 350 nm) and a buffer layer (p-type, 1000 nm). We observe a transient behaviour of the aluminium concentration at the interface substrate/buffer (over 100 nm) which could be due to an initial reaction between TMA and oxygen in the beginning of the growth. The nitrogen interface between the channel/cap layer does not show any tendency of transient behaviour and is very abrupt.
Commercially available structures have shown concentration peaks at the interfaces of the nitrogen containing layers. These peaks have been up to one order of magnitude higher in doping than the layer itself. The peaks may cause an accumulation of charges that could affect the performance of the device. The structures we have grown in the hot-wall CVD reactor do not show any tendency to concentration peaks and exhibit excellent thickness profile and doping uniformity.

2:15 PM H2.4
INVESTIGATION OF LO-HI-LO AND DELTA-DOPED SILICON CARBIDE STRUCTURES. A.O. Konstantinov, S. Karlsson, C. Adas and C.I. Harris, ACREO AB, Stockholm, SWEDEN.

Lo-hi-lo doping is a useful tool in semiconductor device technology. This technique is used in high efficiency MESFETs and IMPATT devices. Silicon carbide devices could potentially benefit from using the lo-hi-lo doping. However, thin doped layers with high precision doping control have traditionally been a problem in silicon carbide technology. Epitaxial growth was used in this work as one technique of obtaining lo-hi-lo profiles. Growth was performed in the hot-wall CVD reactor manufactured by EPIGRESS. Doping profiles were controlled using capacitance-voltages techniques. Steep and almost exponential doping transients were obtained using nitrogen donors. A peak width of around 25 nm can be achieved. Aluminum doping profiles are somewhat more complicated, however the peak widths achieved were comparable to that of nitrogen. An alternate way to form lo-hi-lo structures is a shallow dopant implantation with subsequent regrowth. This technique was found to result in deactivation of deep portions of low-doped epitaxial layers underneath the implanted region, even for nitrogen implants. Deactivated regions can be can be up to 2 micron deep. Multifrequency capacitance-voltage plots indicates conversion of these regions into p-type. Investigation of avalanche breakdown has been performed. The results demonstrate that lo-hi-lo structures are easier to terminate than conventional p-n junctions. This facilitates investigation of the material imperfections responsible for early breakdown of silicon carbide devices.

2:30 PM H2.5
ELECTRONIC PROPERTIES OF NITROGEN DELTA-DOPED SILICON CARBIDE LAYERS. Toshiya Yokogawa, Kunimasa Takahashi, Takeshi Uenoyama, Osamu Kusumoto, Masao Uchida and Makoto Kitabatake, Matsushita Electric Ind. Co., Ltd., Advanced Technology Research Laboratories, Kyoto, JAPAN.

We demonstrate, for the first time, a nitrogen delta-doped silicon carbide (SiC) by chemical vapor deposition (CVD). We report on electronic properties of delta-doped SiC and propose the application for field-effect transistor (FET). Doping distributions with high peak concentrations and narrow distribution widths were advantageous for a high mobility and high breakdown voltage. Delta-doping in CVD was performed by a pulse doping method using a pulse valve. The valve can open and close within very short period less than 10 μs. The nitrogen gas as n-type dopant was injected into the reactor through the pulse valve. The capacitance-voltage measurements were carried out. The doping distribution profile of the delta-doped SiC had strikingly narrow width of 10 nm. The peak concentration was in the high 1×10^{18} cm^{-3} range. By Hall-effect of the delta-doped SiC, the temperature dependence of a Hall mobility and a carrier concentration was investigated. The mobility enhancement was observed for the delta-doped structure over the corresponding uniformly doped SiC. The enhancement factor of 2 to 3 was obtained for the delta-doped SiC. The self-consistent calculation by the coupled sets of Poisson and Schrödinger equation suggests that the high mobility is related to the overlap of the electron wave-function of the delta-doped layer with high purity SiC layers. The high mobility attracts considerable interest in FET having the delta-doped channel. Delta-doped channel MES-FET was fabricated. The FET structure employs an n^+ cap layer on top of the delta-doped channel to decrease ohmic contact resistance. The recess gate was formed by etching the n^+ cap layer using reactive ion etching. The device had large drain-gate break down voltage of 120 V, high drain current capability and easy control of the threshold voltage with a good pinch-off characteristics.

2:45 PM H2.6
A NEW SUBLIMATION ETCHING FOR REPRODUCIBLE GROWTH OF EPITAXIAL LAYERS OF SiC ON SiC SUBSTRATES IN A CVD SYSTEM. Rongjun Wang, Paul Chow and Ishwara Bhat, ECSE Department, Rensselaer Polytechnic Institute, Troy, NY.

A horizontal water-cooled cold-wall reactor for SiC epitaxial growth was recently installed at RPI. In-situ H_2 etching studies and epitaxial growth of SiC on both 6H-SiC and 4H-SiC substrates have been carried out in this system. Epitaxial layers with excellent surface morphology and thickness up to 12 μm were grown reproducibly on both 4H- and 6H-SiC, 1.375" diameter substrates using metalcarbide-coated graphite susceptor. N-type layers are obtained using nitrogen as the dopant. The surface morphology of H_2-etched and epitaxially grown SiC was atomically smooth (rms. roughness less than 0.2nm over 2μmX2μm) examined by atomic force microscopy (AFM). The films are characterized using SIMS and C-V measurements. Films with background concentration less than 10^{15}cm^{-3} can be obtained using this new system. Excellent layers with reproducible growth were possible due to a new susceptor cleaning method we developed, which is based on the principle of sublimation etching. This method is found to be much more effective than pure hydrogen etching. The deposition on a metalcarbide-coated graphite susceptor formed during a three-hour epitaxial growth can be completely removed in less than 30 minutes at temperatures less than 1540°C. By using this method prior to each growth run, we were able to make the epitaxial growth more reproducible and also were able to extend the lifetime of the susceptor.

3:30 PM H2.7
CRYSTALLOGRAPHIC CHARACTERIZATION OF SiC EPITAXIAL LAYERS GROWN ON POROUS SiC SUBSTRATES.

G. Melnychuk, S.E. Saddow, Emerging Materials Research Laboratory, Dept. of ECE, Mississippi State, MS; M. Mynbaeva, I. Nikitina, Ioffe Institute, St. Petersburg, RUSSIA; W.M. Vetter, L. Jin, M. Dudley, Dept. of Materials Science, SUNY-Stony Brook, Stony Brook, NY; M. Shamsuzzoha, Dept. of Metallurgical Engr. and School of Mines Energy Development, University of Alabama, Tuscaloosa, AL; V. Dmitriev, TDI, Inc, Gaithersburg, MD; C.E.C. Wood, Office of Naval Research, Arlington, VA.

The presence of micropipes and dislocations in SiC wafers used as substrates for SiC epitaxial growth may cause formation of lattice defects in the epilayers. The objective of this research was to develop a CVD growth process on porous SiC substrates in order to reduce the concentration of structural defects in SiC epilayers. We have reported on the growth and crystal quality of CVD epitaxial layers grown on porous SiC (PSC) substrates [1]. A layer of porous SiC was fabricated by surface anodization of commercial 4H and 6H-SiC (0001)Si face off-axis wafers. The 4H and 6H-SiC epilayers were grown on porous SiC (PSC) substrates using atmospheric pressure CVD at 1580°C and a Si to C ratio of 0.3. Results of X-ray diffraction, RHEED, SEM and AFM characterization demonstrated good surface quality of the films grown on porous material. PL data indicates a greatly improved defect structure in the epi layers grown on PSC as compared to control samples [1]. TEM investigation on cross-sectional specimens of the CVD epitaxial layers thus grown revealed that the presence of pores in the substrate does not lead to the formation of any micropipe in the epitaxial layer. The investigation also failed to detect a more than usual dislocation density on the basal plane of the epitaxial layer. Based upon the results of various analytical techniques applied to the CVD deposit we propose that the density of screw dislocations in the epitaxial layer is less than $5x10^4$ cm$-$3. It should be noted that the density of similar types of dislocations in the initial substrate as determined by the TEM was $\sim 10^6$ cm^{-3}, so this preliminary investigation indicates that the epitaxial layer grown on PSC may have a reduction in dislocation density of more than an order of magnitude over those grown on conventional SiC substrates that are not porous. In this paper we will present characterization data from X-ray and TEM experiments performed on this material where we have further characterized not only the epitaxial layer but the PSC/epi layer interface.
[1] G. Melnychuk, M. Mynbaeva, S. Rendakova, V. Dmitriev, and S.E. Saddow, Spring 2000 MRS Symposium, San Francisco, CA, April 2000.

3:45 PM H2.8
APPLICATIONS OF THE REGROWTH OF SILICON CARBIDE ON POROUS SILICON CARBIDE SUBSTRATES. Jonathan E. Spanier[a], Irving P. Herman[a], Greg T. Dunne[b], and Larry B. Rowland[b]. [a]Department of Applied Physics, Columbia University, New York, NY; [b]Sterling Semiconductor, Inc., Sterling, VA.

We report on new developments in the study of SiC vapor-phase epitaxy on porous silicon carbide (PSC) substrates formed by electrochemical anodization of both *n*-type and *p*-type 6H-SiC. The effects of PSC preparation conditions on the properties and material quality of the epitaxy are presented. Polarized micro-Raman scattering is shown to be an effective probe of the epitaxy, and indicates that the regrown films are of the 6H polytype and are of high quality [1]. Several potential applications of epitaxial 6H-SiC on porous 6H-SiC pertaining to isolation, microfabrication and epitaxial lift-off are discussed.
[1] Jonathan E. Spanier, Greg T. Dunne, Larry B. Rowland and Irving P. Herman, Appl. Phys. Lett. **76**, (2000).

4:00 PM H2.9
GROWTH OF SINGLE CRYSTALLINE CUBIC SiC ON Si USING POROUS Si AS A COMPLIANT SEED CRYSTAL. A. Faik, D. Purser, D. Lieu, F. Vaccaro, and M.-A. Hasan, and M.R. Sardela Jr.[a], C.C. Cameron Applied Research Center & The Department of Electrical and Computer Engineering, University of North Carolina, Charlotte, NC; [a]Materials Research Laboratory, University of Illinois, Urbana IL.

Single crystalline 3C-SiC layers were grown on a porous Si seed using a single gas source, trimethylsilane. The method is environmentally friendly, utilizes a non-toxic gas, and is economical. Conversion of porous Si into SiC was also attempted using methane but the process did not lead to the formation of continuous layers. The porous Si layers were made by anodizing p-type Si(100) wafers in a mixture of hydrofluoric acid and ethanol. The SiC was grown in a UHV system that was converted into a low pressure CVD reactor and was fitted with a resistive heating stage capable of heating the samples up to 1250°C. The formation of stoichiometric SiC was confirmed by secondary ion mass-spectrometry (SIMS) and Fourier transform infra-red spectroscopy (FTIR) while the crystal structure was examined by transmission electron microscopy (TEM) and X-ray diffraction. FTIR showed a strong peak at 800 cm^{-1} which corresponds to the Si-C vibrational mode. Atomic force microscopy (AFM) showed the formation of rough surfaces for thin SiC layers and large flat terraces for thick SiC layers. TEM selected area diffraction (up to 20μm on several areas on the sample) indicates the formation of fully relaxed single crystalline 3C-SiC(100) on Si(100) wafers. However, large area X-ray diffraction suggests the presence of other crystal orientations within the dominating SiC(100) layer. Hetero-junction Si/SiC diodes were fabricated, which displayed a soft breakdown voltage as high as 375V.

4:15 PM H2.10
SURFACE MORPHOLOGY OF 6H-SiC ON VARIOUS A-PLANE USING Si_2Cl_6 $C_3H_8H_2$ BY CHEMICAL VAPOR DEPOSITION. Shigehiro Nishino, Yasuichi Masuda, Satoru Ohshima and Chacko Jaciob, Department of Electronics and Information Science, Faculty of Engineering and Design, Kyoto Institute of Technology Matsugasaki, Sakyo-ku, Kyoto, JAPAN.

To realize the devices, it is important to know the morphological dependence of the epilayer on various orientation of the substrates. Most of the homoepitaxial growth is carried out on the 6H-SiC (0001) Si basal plane off cut toward $< 11-20 >$ direction. Recently epilayer on a-plane (11-20) is also focused because of high channel mobility of MOSFET was achieved [1]. We already reported morphological dependence of epilayer on a-planes prepared by Si_2H_6 C_2H_2-H_2 system [2]. In this presentation, we show the morphological dependence of epilayer on two different substrates such as a-planes (11-20), (1-100) using Si_2Cl_6 C_3H_8 H_2 system. Crystal growth was carried out at a substrate temperature of 1500°C using Si_2Cl_6 C_2H_8 H_2 by atmospheric CVD. The CVD system in this study was made from a horizontal quartz-tube with water cooling jacket. The substrates were placed on SiC coated graphite susceptor. Typical growth condition was as follows: flow rate of Si_2Cl_6=0.45 sccm, C/Si=10, H_2=3 slm, growth period=2h. The growth rate=3 μm/h. The growth rate was mainly limited by flow rate of Si_2Cl_6 and independent of flow rate of C_3H_8. When we choose appropriate parameter, very smooth surfaces appeared on the epilayer of (11-20) plane. Rather smooth surface epilayer appeared on (1-100) plane, however, a parallel fringe pattern was observed along $< 11-20 >$ direction. Buffer layer effect will be presented in detail. Polytypes of the epilayer was characterized by PL and Raman spectroscopy. [1] T. Kimoto et al. Proc. ICSCRM99. [2] S. Nishino et al. in "Amorphous and Crystalline silicon Carbide 3", (1992). Springer-Verlag. p. 363.

4:30 PM H2.11
MODELING OF EPITAXIAL GROWTH AND DEPOSITION CHARACTERISTICS OF SiC LAYER. Gang Zhou, Wei Ji, Christer Hallin and Peter Lofgren, ABB Corporate Research, Västeras, SWEDEN.

A comprehensive chemical vapour deposition model, including gas-phase and surface chemistry coupled with reactor fluid dynamics and heat transfer, has been used to predict the growth rate and the morphology of epitaxially grown silicon carbide (SiC) in a Si-C-H(Ar) system. Hydrogen and hydrogen slightly diluted with argon are used as carrier gases. The precursors are silane (SiH_4) and propane (C_3H_8). A local "etching" model, taking care of the reversible surface adsorption at higher temperatures (>1300°C), has been added to the interactive gas phase and surface chemistry model, which resulted in a significant improvement between predicted growth rate and experimental data. The deposition characteristics of SiC film growth has been predicted using a sequential coupled local thermodynamic equilibrium model. The equilibrium calculation has been carried out at near adjacency of the surface, based on the steady-state simulation solution of heat and mass transfer coupled gas-phase and surface chemistry in a SiC chemical vapour deposition process. The simulated deposition of SiC, both growth rate and morphology, is corresponding well to our experimental measurements at relatively low temperatures. Several simulation results corresponding to different carrier gases, organosilicon compounds, reactor geometry, and operating conditions will be reported and discussed in this presentation.

4:45 PM H2.12
GROWTH OF THICK 4H-SiC EPILAYERS IN A VERTICAL RADIANT-HEATING REACTOR. Hidekazu Tsuchida, Isaho Kamata, Tamotsu Jikimoto, Kunikazu Izumi, Central Research Institute of Electric Power Industry, Yokosuka Research Laboratory, Kanagawa, JAPAN.

We report on growth of very thick 4H-SiC epilayers in a vertical radiant-heating reactor. The reactor consists of a vertical hot-wall and an inner susceptor. We used a V-shaped susceptor with upward gas stream. In this reactor, induction current flows only in the hot-wall, so that the susceptor and substrates are heated by radiation from the hot-wall. This heating method achieves an inverse temperature gradient, as the substrate temperature is slightly higher than the susceptor temperature. The temperature gradient prevents a backside

deposition during thick epitaxial growth. The typical growth temperature is around 1550°C at the susceptor top, whereas the hot-wall temperature is considerably higher than the measured susceptor temperature. Epitaxial growth was performed at 10-18 μm/hr under a reduced pressure as low as around 50 Torr. A 150 μm-thick epilayer has been grown and characterized by atomic force microscopy (AFM) and low temperature photoluminescence (PL) measurements. The layer has a specular surface, and the AFM image showed a regular step structure without macro step bunching indicating a stable step-flow growth. The RMS surface roughness of the epilayer was as low as 0.2 nm for a 10 μm × 10 μm area. The PL spectra taken from the layer showed strong free excitons and comparatively small nitrogen bound excitons. Aluminum and boron bound excitons were almost negligible. Titanium-related lines and boron-related DAP recombination were also very weak.

SESSION H3: SiO_2/SiC INTERFACES
Chairs: Carl-Mikael G. Zetterling and
Heinz Lendenmann
Tuesday Morning, November 28, 2000
Room 202 (Hynes)

8:30 AM *H3.1
CHALLENGES AND STATE-OF-THE-ART OF OXIDES ON SiC. Lori Lipkin, Mrinal Das and John Palmour, Cree Research, Durham, NC.

The material characteristics of SiC make this semiconductor an outstanding choice for power devices that carry high current, control high voltages or amplify at high frequencies. In addition, devices that operate at high (350°C) temperatures are possible. However, any semiconductor device must be passivated. SiC devices remain limited by the lack of good passivation. Although various materials have been investigated, no insulator other than silicon dioxide (SiO_2) appears to have a band-gap wide enough to passivate SiC directly. Evaluating a metal-oxide-SiC capacitor or MOSFET has challenges that are not present for such Si devices. Progress has been made towards understanding the nature of the SiC:SiO_2 interface, but control of this interface remains elusive. The current consensus is the inversion mobility of n-channel MOSFETs is controlled by interface states near the conduction band. These states are almost an order of magnitude higher for 4H-SiC than for 6H SiC, which corresponds to the almost order of magnitude lower mobility of 4H-SiC. Reduction of the near-conduction band interface states has been accomplished via multi-layer dielectrics and post oxidation anneals. However, the density of interface states near the band edges remain quite high. While not an ideal solution, some success has been achieved by implanting the channel to lower the doping or to create a buried channel. In addition to the high density of electrically active states, other concerns exist for device passivation and/or gate insulation. Breakdown field strength, long-term reliability, reliability at high temperatures, and gate leakage have been investigated and in some instances improved with some of the processing solutions implemented for reduced interface state densities. A general overview and history of oxides and insulators on SiC will be presented along with current trends in processing and measurement techniques.

9:00 AM *H3.2
TRAPS AT THE SiC/SiO_2 - INTERFACE. Gerhard Pensl, Michael Bassler, Florin Ciobanu, University of Erlangen-Nuernberg, Institute of Applied Physics, GERMANY; Valery Afanas'ev, KU Leuven, Laboratory for Semiconductor Physics, BELGIUM; Hiroshi Yano, Tsunenobu Kimoto, Hiroyuki Matsunami, Kyoto University, Department of Electronic Science and Engineering, JAPAN.

The progress in the development of SiC-based devices is due to the huge improvement of the crystal quality of SiC-substrates and to the favorable factor that device processing can be partially taken from the silicon technology, e.g. the formation of thin insulating SiO_2–films by thermal oxidation. In comparison with Si/SiO_2-MOS structures, the trap density at SiC/SiO_2–interfaces (D_{it}) is enhanced in the whole band gap by at least two orders of magnitude. This enhancement of D_{it} is assumed to originate from carbon precipitates at the interface, which are formed during the oxidation process. Moreover, it is experimentally demonstrated that Dit close to the conduction band edge of the 4H-SiC polytype increases much steeper than in the 6H- or 15R-SiC polytype. This increase of D_{it} is probably responsible for the low channel mobility in 4H-SiC MOS devices. We have experimental evidence that these energetically shallow traps are caused by near interface traps located in the oxide close to the interface. Because of the larger band gap of the 4H-SiC polytype, the energy positions of these shallow traps are within the band gap of this polytype; there they can capture free electrons and can, in addition, reduce the channel current by Coulomb scattering.
In this talk, we review the progress on understanding the role of interface traps in different SiC polytypes (4H-, 6H- and 15R-SiC) and report on the effect of hydrogen on interface states. We further discuss the open question whether operation at temperatures above 600K leads to a degradation of 6H/4H-SiC-MOS capacitors.

9:30 AM *H3.3
BONDING, DEFECTS, AND DEFECT DYNAMICS IN THE SiC-SiO_2 SYSTEM. S.T. Pantelides, R. Buczko, G. Duscher, S.J. Pennycook, L.C. Feldman, Vanderbilt University, Nashville, TN and Oak Ridge National Laboratory, Oak Ridge, TN; M. Di Ventra, S. Wang, S. Kim, K. McDonald, R.K. Chanana, R.A. Weller, Vanderbilt University, Nashville, TN; G.Y. Chung, C.C. Tin, T. Isaacs-Smith, J.R. Williams, Auburn University, Auburn, AL.

Interface defects at the SiC-SiO_2 interface reduce carrier mobility and act as carrier traps, limiting the potential usefulness of SiC for power devices. This talk will report comprehensive first-principles atomic-scale calculations, atomic-resolution Z-contrast TEM images electron energy-loss spectra that provide microscopic understanding of the SiC-SiO_2 system and account for the observed passivation of interface defects by N. The atomic-scale processes that underlie the oxidation of SiC and possible interface defect structures, including C clusters, are identified. The results elucidate the mechanisms by which C is removed as CO. C clusters can be passivated by both H and N.CO molecules can be trapped in the oxide in the form of defect complexes and can subsequenctly be dissolved. Investigations of the global bonding of the SiC-SiO_2 suggest that a mixed-phase transition layer is required at the interface. Atomic-resolution Z-contrast images show an abrupt termination of crystalline SiC, but EELS reveals a mixed-phase transition region that contains C and is quite extended in as-oxidized samples, but is reduced to 1-2 monolayers in reoxidized samples. The work was supported in part by a joint grant from DARPA and EPRI.

10:30 AM *H3.4
EPITAXIAL GROWTH OF SiC ON NON-TYPICAL ORIENTATIONS AND MOS INTERFACES. Hiroyuki Matsunami, Tsunenobu Kimoto, Hiroshi Yano, Dept of Electronic Science and Engineering, Kyoto University, Kyoto, JAPAN.

Epitaxial growth of 4H- and 6H-SiC on (0001)Si planes with off- angle has been extensively carried out owing to availability of substrates. Drawbacks of this plane, however, include micropipe penetration from substrates and probable inclusion of 3C-SiC. Growth on SiC $(11\bar{2}0)$ planes, perpendicular to (0001) planes, has advantages of perfect replication of SiC polytypes and possible absence of micropipes. The authors have succeeded to grow high-quality homoepitaxial layers on SiC $(11\bar{2}0)$ planes and investigated device fabrication systematically. In this paper, details of epitaxial growth and impurity doping are described. The physical properties of epitaxial layers and MOS (metal-oxide-semiconductor) interfaces on both $(11\bar{2}0)$ and (0001)Si planes are elucidated. Epitaxial growth was carried out using atmospheric-pressure CVD in a SiH_4-C_3H_8-H_2 system at around 1500°C. The growth rate on $(11\bar{2}0)$ planes (2.5μm/h) was similar to that on (0001)Si planes. Surface morphology examined by an optical microscope and an AFM profiler is described together with crystal quality analyzed by X-ray diffraction. Doping characteristics and Schottky-barrier performances are discussed based on electrical measurements. The most striking results on the performance of MOS interfaces are focussed on in the presentation. N-channel planar MOS field effect transistors were fabricated on p-type epilayers grown on $(11\bar{2}0)$ and (0001)Si planes of 4H- and 6H-SiC. Wet oxidation was performed to fabricate MOS interfaces with an oxide thickness of 40nm on both planes. Dramatic increase of inversion channel mobility (from 5.59cm^2/Vs for (0001)Si planes to 95.9cm^2/Vs for $(11\bar{2}0)$ planes) is explained together with the temperature dependencies of inversion channel mobility and threshold voltage. The reason for the dramatic increase will be discussed in detail related with interface states.

11:00 AM *H3.5
NITROGEN PASSIVATION OF INTERFACE STATES NEAR THE CONDUCTION BAND IN SILICON CARBIDE. G.Y. Chung, C.C. Tin, T. Issacs-Smith and J.R. Williams, Physics Department, Auburn University, Auburn, AL; K. McDonald, M. Di Ventra, S.T. Pantelides[1] and L.C. Feldman[1], Department of Physics and Astronomy, Vanderbilt University, Nashville, TN [[1]Also at Oak Ridge National Laboratory, Oak Ridge, TN]; R.A. Weller, Department of Electrical Engineering and Computer Science, Vanderbilt University, Nashville, TN; O.W. Holland, Solid State Division, Oak Ridge National Laboratory, Oak Ridge, TN.

Two significant problems appear to hinder the development of silicon carbide inversion mode metal - oxide - semiconductor field effect transistors: (1) epilayer surface roughness introduced prior to oxidation by high temperature activation anneals of implanted source / drain regions, and (2) a large, broad density of interface

states that exists at about 2.9eV above the valence band edge in all the hexagonal polytypes. These problems adversely affect the silicon dioxide / silicon carbide interface and limit the channel mobility that can be achieved for inversion mode devices. Our paper is concerned with the second of these problems. The interface density near the conduction band is much higher for 4H silicon carbide compared to 6H, and this situation is now considered a primary reason for the lower channel mobilities that are reported for 4H devices. These interface states have been observed and characterized in several laboratories since they were first described by Schorner, et al [1]. Interface state densities near the conduction band are studied using n-silicon carbide under the assumption that p-type material has a similar distribution of states. Over the past year, much attention has been focused on finding methods by which these states can be passivated. We will describe a nitrogen-based passivation process that is performed using post-oxidation, high temperature anneals in either nitric oxide or ammonia [2]. This process reduces the interface state density near the conduction band in n-4H silicon carbide by almost one order of magnitude - from $>10^{13}$ to approximately $2x10^{12}cm^{-2}eV^{-1}$. Initial measurements for passivated n-channel inversion mode devices have yielded channel mobilities of approximately $50cm^2/V$-s. This result represents a significant improvement compared to the single digit mobilities often reported for 4H inversion mode devices. We believe that it may be possible to achieve 4H channel mobilities in the range of 75 to $100cm^2/V$-s using an optimized passivation process together with improved implantation / activation procedures that minimize epilayer surface roughness. [1] R. Schorner, P. Friedrichs, D. Peters and D. Stephani, IEEE Electron Device Lett. 20 (1999) 241. [2] G.Y. Chung, C.C. Tin, J.R. Williams, K. McDonald, M. Di Ventra, S.T. Pantelides, L.C. Feldman and R.A. Weller, Appl. Phys. Lett. 76(13) (2000) 1713.

11:30 AM H3.6
NITROGEN INCORPORATION IN SiO_2/4H-SiC by NO AND NH_3 ANNEALS. Kyle McDonald, R.K. Chanana, R.A. Weller, L.C. Feldman, Vanderbilt University, Nashville, TN; G.Y. Chung, C.C. Tin, J.R. Williams, Auburn University, Auburn, AL.

Although 4H-SiC has a higher bulk electron mobility than other polytypes, metal-oxide-semiconductor (MOS) devices made from 4H-SiC exhibit a large density of interface trap states (D_{it}) near the conduction band and poor channel mobility. Recently, annealing 4H-SiC MOS capacitors in NO or NH_3 has been shown to substantially reduce D_{it} near the conduction band, promising higher mobility[1]. Using nuclear reaction analysis (NRA), Rutherford backscattering spectrometry (RBS), and secondary ion mass spectrometry (SIMS), we have made a quantitative determination of the nitrogen profile in SiO_2/4H-SiC incorporated by NO and NH_3 anneals. We also show the relationship between D_{it} and nitrogen content. Although the D_{it} results are similar for both NO and NH_3, the location and amount of nitrogen for similar anneal conditions are completely different.
[1]G.Y. Chung, C.C. Tin, J.R. Williams, K. McDonald, M. Di Ventura, S.T. Pantelides, L.C. Feldman, R.A. Weller, Appl. Phys. Lett. **76**,1713 (2000).

11:45 AM H3.7
PROFILING OF THE SiO_2 - SiC INTERFACE USING X-RAY PHOTOELECTRON SPECTROSCOPY. R.N. Ghosh, S. Ezhilvalavan and B. Golding, Center for Sensor Materials, Michigan State Univ., E. Lansing, MI; S.M. Mukhopadhyay, N. Mahadev and P. Joshi, Mechanical & Materials Engineering, Wright State Univ., Dayton, OH; M.K. Das, Cree Research Inc., Durham, NC; J.A. Cooper, Jr., School of Electrical & Computer Engineering, Purdue Univ., W. Lafayette, IN.

Recent advances in silicon carbide device technology have enabled the implementation of SiC based sensors and electronics for operation in harsh, high temperature environments. Understanding the properties of the SiO_2 - SiC interface is crucial for field effect devices. Using x-ray photoelectron spectroscopy (XPS) we have studied both the abruptness of the interface as indicated by sub-oxide species and the possible presence of carbon at the interface in the form of oxy-carbides or even discrete clusters. Samples consist of device-quality thermally grown 50nm oxides on both 4H and 6H SiC substrates with electrically measured interface state densities near mid gap and fixed oxide charge densities below $1E11/eV/cm^2$ and $1E12/cm^2$, respectively. A very shallow wedge (angle < 0.01rad) was mechanically polished to expose the oxide-SiC interface. An AXIS Ultra scanning XPS system was used to obtain C1s, O1s and Si2p photoelectron spectra of the SiC substrate and the full oxide layer. The Si2p signal showed distinct chemical shifts in the SiC and SiO_2 regions. An oxide species, possibly a thin native oxide, was observed on the nominally bare SiC surface and some C was present as an impurity on the oxide surface. We also obtained spatially resolved photoelectron images of the sample surface. We shall discuss these spectroscopic images of the wedge region in terms of variations in composition and chemical state as a function of distance from the interface. Comparison of XPS images of samples with different electrically active defect densities should yield information on the microscopic origin of interface mobility reduction in the SiO_2 - SiC system.

SESSION H4: SiC DEVICES
Chairs: Anant K. Agarwal and James A. Cooper, Jr.
Tuesday Afternoon, November 28, 2000
Room 202 (Hynes)

1:30 PM *H4.1
PERFORMANCE AND RELIABILITY OF HIGH POWER 4.5kV DIODES. Heinz Lendenmann, PerAke Nilsson, Fanny Dahlquist, J. Peder Bergman, ABB Corporate Research, Vaesteraas, SWEDEN.

SiC devices with 10-fold breakdown strength compared to Si are expected to improve power electronic systems such as HVDC transmission. Good basic device properties such as forward voltage (3.4V), low leakage currents (1e-6Acm^{-2}) and high current switching (400A, 1250V) for large area ($20mm^2$ and $40mm^2$) PiN diodes for the 2.5kV range as well as near theoretical performance for $1mm^2$ 2.0-2.8kV JBS diodes are reported. Moreover, the PiN diodes were successfully scaled to 4.5kV blocking voltage. These diodes with implanted anodes were fabricated on 4H SiC wafers, with low $10^{15}cm^{-3}$ n-type doped hot-wall CVD Epi layers of 30 - 50um thickness. For voltage termination an implanted JTE with an oxide surface passivation layer is used. Blocking reliability testing (1000h) at high-temperature (125C), showed stable leakage currents in the range of 10^{-5} to $10^{-4}A/cm^2$. However, continuous converter operation revealed a new drift phenomenon of the forward voltage drop in bipolar diodes. Drifting diodes may increase in V_f from ~0mV to several 100mV (or more under severe conditions). Diodes with a fast drift (hours-days), coexist with slow- and non-drifting diodes (>2000h) on the same wafer. The increase in forward voltage is accompanied by a reduction in the electrical minority carrier lifetime and by regions with reduced photoluminescence. These areas are also related to changes in the crystal matrix. It was found, that the substrate material as well as process uniformity can make marked differences in the occurrence of this phenomenon. In contrast to bipolar PiN diodes, the unipolar JBS type diodes do not exhibit this phenomenon. In the summary known crystal imperfections are juxtaposed to a detailed analysis of minor and major non-ideal device properties. Most device non-idealities (forward and reverse) can be explained in terms of the local substrate quality causing Epi defects.

2:00 PM *H4.2
SILICON CARBIDE BIPOLAR POWER DEVICES - POTENTIALS AND LIMITS. Ranbir Singh, John W. Palmour, Cree Inc., Durham, NC.

To exploit the tremendous advantages offered by SiC for bipolar power devices, it is important to understand the relevant voltage/current range, fundamental limits and technological challenges in order to develop this technology commercially. The opportunity of operating a device at a high current density (>300 A/cm^2) to increase total current with reasonable yield, the poor reliability of MOS at high temperatures, and the relatively low channel mobilities obtained in 4H-SiC MOSFETs may make certain bipolar devices more attractive even as low as 1700 V. Depending on the operating conditions, the maximum limit on the on-state current density may arise from one of the three factors: (a) the heat dissipation limit of the package (commercial packages limit the continuous current density to about 400 A/cm^2 at VF=4.5 V; (b) the contact resistance of anode or cathode, especially if one of these contacts is p-type; and (c) the heat dissipation limit of SiC, arising only in very high pulsed current ($>10^5$ A/cm^2) applications. Bipolar devices made with SiC offer 20-50X lower switching losses as compared to conventional semiconductors. Another very significant property of SiC bipolar devices is their lower differential on-state voltage drop than similarly rated Si bipolar device, even with an order of magnitude smaller carrier lifetimes in the drift region. This property allows high voltage (>20 kV) to be far more reliable and thermally stable as compared to those made with Silicon. The switching losses and the temperature stability of bipolar power devices depends on the physics of operation of the device. The two major categories of bipolar power devices are: (a) single injecting junction devices (for example BJT and IGBT); and (b) double injecting junction devices (like Thyristor-based GTO/MTO/JCT/ FCT and PIN diodes). Detailed analysis of these devices will be presented at the conference. Detailed measurements on devices with record breaking voltage and current ratings will be presented at the conference. These include 4H-SiC 8.6 kV PIN diodes, 605 V/1 A buried gate FCT and >1 A p-channel IGBTs.

2:30 PM *H4.3
MICROMACHINING TECHNIQUES FOR SiC MEMS.

Mehran Mehregany, Christian A. Zorman, Case Western Reserve University, Department of Electrical Engineering and Computer Science, Cleveland, OH.

SiC is well known for its excellent mechanical, electrical, and chemical properties; making it a leading material for microfabricated sensors and actuators designed for environments too harsh for Si-based devices. However, the very properties that make SiC attractive for harsh environments, make it a challenging material to micromachine. Bulk micromachining of SiC is particularly difficult, since anisotropic wet-chemical etching has not been demonstrated and deep reactive ion etching is still in its infancy. In the area of surface micromachining, recent advances in SiC deposition and patterning techniques have led to the development of processes that yield both single and two-layer devices. To date, however, a fabrication process with capabilities and design rules comparable to the well-known four polysilicon layer MUMPs process has not been demonstrated in SiC, in part because SiC dry etching processes exhibit poor selectivity to silicon and silicon dioxide sacrificial layers. This paper details the development of molding-based bulk and surface micromachining processes for SiC MEMS devices. For SiC bulk micromachining, SiC deposition, mechanical polishing, and Si wet chemical etching are used to fabricate free standing polycrystalline SiC (poly-SiC) components from Si molds fabricated by deep reactive ion etching. A similar concept is used for SiC surface micromachining, where polysilicon and silicon dioxide thin films are deposited onto sacrificial layers, patterned into micromolds by reactive ion etching, filled with poly-SiC, planarized by mechanical polishing, and eventually dissolved and released in selective wet chemical etchants. We are using the micromolding technique as the basis for a four-layer, poly-SiC surface micromachining process analogous to the MUMPs process that we call the MUSiC (Multi-User SiC) process. The extended paper will detail each micromachining process, discuss the issues related to molding-based patterning, and highlight several examples of fabricated devices.

3:30 PM H4.4
INFLUENCE OF INTERFACE STATES ON THE OUTPUT CHARACTERISTICS OF 4H-SiC MESFETs ON SI SUBSTRATES. Nabil Sghaier, Abdelkader Souifi, Jean-Marie Bluet, Gerard Guillot, Institut National des Sciences Appliquees de Lyon, Laboratoire de Physique de la Matiere, Villeurbanne, FRANCE; Olivier Noblanc, Christian Brylinski, THOMSON-CSF, Laboratoire Central de Recherches, Orsay, FRANCE.

The development of 4H-SiC MESFETs for power amplification in L and/or S band requires the use of SI substrates in order to reduce parasitic losses. Unfortunately, the structural quality of SI substrates is still poor in comparison with conductive ones leading to limitation in the power densities in comparison to the expected values. Improvement in the devices performance is then strongly linked to the optimization of the buffer layer. Toward this end, a clear understanding of the impact of defects laying at the SI substrate/ buffer layer or buffer layer/active layer is strongly needed. In this study we discuss the correlation between "abnormal behaviors" observed on DC output characteristics and trapping/detrapping phenomena. The transistors have different geometry (gate length ranging from 1 μm to 32 μm and peripheries between 200 μm and 4 mm), and were realized directly on SI substrates or using n or p type buffers. The Id-Vd characteristics have been recorded at various temperatures (300 K- 600 K). For each temperature the measurements have been done either by increasing or decreasing the gate bias. At 300K, a strong hysteresis effect is observed for devices without buffer. Indeed, a decrease of the drain current is obtained when the gate voltage (Vg) is swept from high to low values. This behavior can be due to negatively charged interface traps acting as a parasitic gate near the substrate. The hysteresis effect disappears progressively for increasing temperatures in agreement with a thermal ionization of the electron traps. To confirm the presence of deep traps, Random Telegraph Signal measurements have been performed and show that a discrete current fluctuation is possible only for high gate voltages (i.e. when the current flows near the interface). The parasitic phenomena described above are drastically reduced when n or p-type buffer layers are used.

3:45 PM H4.5
DESIGN AND PROCESS ISSUES FOR SILICON CARBIDE POWER DIMOSFETS. Sei-Hyung Ryu, Anant K. Agarwal and John W. Palmour, Cree, Inc., Durham, NC.

High voltage power DiMOSFETs (Double implanted MOSFETs) in silicon carbide (SiC) are very attractive because they have potentials to match silicon IGBTs in on-state drop, but offer superior switching speed and higher operating temperatures. In SiC power DiMOSFETs, the peak electric field in the blocking region is designed to be approximately 10X higher than that of a Si device with equivalent blocking voltage. This can be detrimental to gate oxide if adequate shielding of electric field is not provided. In this paper, SiC DiMOSFETs with JFET gaps ranging from 1 μm to 6 μm is studied using a 2D device simulator, so that the optimal compromises between gate oxide protection and JFET resistance are found for 1200V (6H) and 2000V (4H) devices. Measurement data from DiMOSFETs with JFET gaps ranging from 1 μm to 6 μm fabricated in both 6H- and 4H- SiC are presented to compare with the simulation results. Another important issue for SiC DiMOSFETs is extremely low surface channel mobility, especially in 4H-SiC. Several methods, such as channel implantations and different anneals for gate dielectric have been suggested to improve MOS channel mobility. These methods were successful for simple devices built in lightly doped p-type epilayers. However, high channel mobilities on an implanted p-well, which is more practical for power MOSFETs, have yet to be demonstrated. In this paper, MOSFET results for several different channel implantation doses and gate oxide anneals are obtained for devices in implanted p-wells, and characteristics of power DiMOSFETs fabricated using these techniques are presented.

4:00 PM H4.6
SHORT-CHANNEL EFFECT SUPPRESSION IN SILICON CARBIDE MESFETS. A.O. Konstantinov, A.-M. Saroukhan, S. Karlsson, C.I. Harris, ACREO AB, Stockholm, SWEDEN and A. Litwin, Ericsson Microelectronics AB, Stockholm, SWEDEN.

Short-channel effects are an important performance limitation for GaAs-based microwave power devices. For wide bandgap materials such effects might be even more significant in view of much higher electric fields. Some wide bandgap device characteristics published in literature have pronounced short-channel effects, however no dedicated studies of these effects in SiC or GaN microwave FETs have been reported to date. We report on a study of short-channel effects in silicon carbide power MESFETs on conductive substrates, which utilize thick buffer layers. Such buffer layers should preferably be doped as low as possible in order to minimize RF losses. However, the decrease of acceptor doping in the buffer layer dramatically increases problems with the drain-induced channel modulation and with the source-to-drain punchthrough. Devices with low-doped buffer layers require long gates to be pinched off with a reasonable gate bias. This, in turn, deteriorates high frequency performance. One solution found in the course of simulations is to incorporate a relatively thin p-type layer with elevated doping close to the channel region. Layer thickness and doping are selected so as to ensure complete depletion of the additional p-buffer underneath the drain, at least for the voltages above the knee. The additional p-buffer considerably increases the punchthrough voltage. Correct choice of active layer thickness is, nevertheless, critical for achieving the desired operation voltage. Semiconductor structures with composite p-buffers have been grown using the CVD technique. Devices were processed to form airbridged MESFETs. Comparative study of MESFETs with varied gate length has been done, which clearly supports the simulation results. In the talk we will also compare between short channel effects in the MESFETs of ACREO manufacture with those in commercially available silicon carbide devices.

4:15 PM H4.7
STACKING FAULTS IN 4H SiC PN-DIODES CREATED DURING FORWARD VOLTAGE OPERATING CONDITIONS. J.P. Bergman, H. Lendenamnn, ABB Corporate Research, Västeras, SWEDEN; H. Jakobsson, E. Janzen, Linköping University, Department of Physics and Measurement Technology, Linköping, SWEDEN; T. Tuomi, Helsinki University of Technology, Optoelectronics Laboratory, Espoo, FINLAND.

One of the main applications for SiC devices is in high power systems as voltage source converters, which has very high demand on the device regarding high blocking voltage, low switching losses and high current levels. This makes properties such as reliability and long term stability important. In this work we have observed and studied the creation of crystal defects after long term controlled operation reflecting continuos converter conditions. The PN-diodes were made on 30um thick 4H epitaxial layers, with a doping of 10E15 cm^{-3}, using a standard diode process. The static forward voltage drop at 100A/cm^2 was originally in the order of 3.4 V, and a measurable (50-100 meV) increase was observed after testing. The top metal layer was removed on selected diodes and the remaining epitaxial material was studied using synchrotron white beam x-ray topography (SWBXT), cathode luminescence (CL), and by optically measuring room temperature minority carrier lifetimes. The SWBXT showed that crystal defects were created in the epitaxial material on tested diodes. These crystal defects are observed as triangular features and interpreted as stacking faults in the (0001) basal plane propagating through the entire epi-layer from the substrate/epilayer interface to the surface. These are directly correlated to similar optical features observed in the CL maps of the diodes cathode luminescence at low temperatures, showing dark triangular shaped regions with reduced emission efficiency. Spatially high resolution optical measurements of

the minority carrier lifetime revealed a local reduction, from about 400ns to below 200ns, in the regions of stressed diodes, correlated to the crystal defects observed in CL and SWBXT. This indicates that the created crystals defects, or defects connected to these, are electrically and optically active. The electrically observed increase in forward voltage drop in these diodes can partly be related to the reduction of minority carrier lifetime.

4:30 PM H4.8
ELECTROLUMINESCENCE FROM 4H-SiC SCHOTTKY DIODES.
Fredrik H.C. Carlsson, Quamar ul-Wahab, Peder J. Bergman, Erik Janzén, Linköping Univ, Dept of Physics and Measurement Technology, Linköping, SWEDEN.

Electroluminescence are normally not observed from Schottky diodes, since minority carrier are not injected, but can be possible under certain conditions such as at low doping levels and with high barrier heights. Under these conditions an inversion layer is formed under the Schottky contact and an accumulation of minority carriers are formed close to the contact. To study the electroluminescence from Schottky diodes provides an easy and additional technique for defect characterization of epitaxial layers. In this work we report the result from spectral and time resolved electroluminescence measurement a from 4H Schottky diodes in the temperature range from 2K to 300K. We compare this with corresponding measurements of photoluminescence on the same material. The diodes were n-type epilayers with a doping of low 10^{15} cm^{-3} with Ni or Au as Schottky contacts. Electroluminescence was observed from the edge of the sample under a relatively high current density in the order of 100 A/cm^2. The spectra in the bandgap region are at lower temperatures dominated by the luminescence from the nitrogen bound excitons and free exciton, where the latter dominates at higher temperatures, together with their respective phonon replicas. The donor-acceptor pair emission involving Al and N are also clearly seen in the spectra. In addition we also observe a broad emission with its maximum around 5200 $\AA$. This emission are not seen in the low temperature photoluminescence of the same material, but have previously been observed in electroluminescence of pn-diodes. At low temperatures we can also observe the D1spectra with a higher relative intensity than in the corresponding photoluminescence measurements of the same material. The increase of the relative intensity for the D1 as well as for the Al-related emissions are most likely related to the higher injection density in the case of electroluminescence compared to photoluminescence.

4:45 PM H4.9
CHARACTERIZATION OF LIGHT EMISSION FROM 4H AND 6H SiC MOSFETs. P.J. Macfarlane, R.E. Stahlbush, Naval Research Laboratory, Washington, DC.

While SiC devices are an attractive alternative to Si in high power applications, interface trap densities measured in SiC MOSFETs are significantly larger than in Si ones. Here, we study SiC MOSFETs using a measurement technique that is based on imaging light emission produced by alternately driving the channel between accumulation and inversion. Emission is due to interface state and bulk electron-hole recombination. The flow of electrons into the channel can be imaged by adjusting the time the channel is cycled into inversion, t_{inv}. For small t_{inv}, only interface traps in the regions around the source and drain emit. Increasing t_{inv} enlarges the emitting areas until light is observed from under the entire gate. Due to lower mobility and higher interface state densities in 4H devices, the electron flow in 4H MOSFETs is 100 to 1000 times slower than that in 6H transistors. We will discuss a model for electron diffusion that is characterized by a travelling electron front, which progresses into the channel by first filling interface traps along a sharp boundary create by the front edge. These results provide an estimate for the interface trap density in the MOSFETs. This imaging technique is also useful for identifying extended defects such as 3C inclusions and the effects the inclusions have on the electron flow in the channel. In addition, we will report on the energy dependence of bulk and interface state emission for both 4H and 6H devices. While the energy dependence of the interface trap emission is the same in 4H and 6H MOSFETs, bulk recombination emission spectra of the two polytypes differ. Sources of the emission peaks will be discussed. We thank J.A. Cooper and M.K. Das for providing the SiC MOSFETs. This work is supported by the ONR Power Electronics Program.

SESSION H5: POSTER SESSION
SiC MATERIALS, CHARACTERIZATION, AND DEVICES
Tuesday Evening, November 28, 2000
8:00 PM
Exhibition Hall D (Hynes)

H5.1
DEPENDENCE OF PVT SiC BULK GROWTH CONDITIONS ON THE TEMPERATURE DISTRIBUTION IN THE CRUCIBLE.
R.V. Drachev, C.A. Rhodes, D.I. Cherednichenko, I.I. Khlebnikov, T.S. Sudarshan, Department of Electrical Engineering, University of South Carolina, Columbia, SC.

Using FIDAP 8.0, the temperature distribution in the bulk crystal growth reactor has been numerically simulated for different stages of the growth process. From the simulation data the characteristic temperatures determining the growth dynamics have been found: T_V - the temperature of sublimative evaporation at the front of source material and T_S - the temperature of the growth front. The following analytical relationship for the rate of growth as a function of these characteristic temperatures is suggested $V=C_V \bullet U \bullet (1-\exp[(-W/R \bullet T_V) \bullet \Delta T/T_S] \bullet T_V S/T_S) \bullet \epsilon/4$. Here C_V is the concentration of the carbon species, which is the limiting component in the vapor; U is the thermal velocity of chemical species in the vapor; W is the molar sublimation energy of SiC; $\Delta T = (T_V - T_S)$. Factor $\epsilon=4X_S{}^2 \bullet n_1 \bullet \phi$ is the sticking parameter, which includes the collision factor $4X_S{}^2$, the effective concentration of chemical species at the front of growth in the adsorbed state n_1, and the probability of chemical reaction between the colliding atoms collisions ϕ. As a result of our analysis the numerical criteria for Si liquid phase formation, which significantly alters the conditions of the growth, as a function of ΔT, has been formulated. Physical aspects of the linear (micropipe) and planar defect generation have also been considered. Performed estimations show that the dislocations present in the substrate can affect only the initial stage of the micropipe formation and the planar defects are not to appear as a second phase from the solute of point defects even in case of their high concentration in the lattice.

H5.2
NOVEL TECHNIQUES FOR THE GROWTH AND CHARACTERIZATION OF SILICON CARBIDE SUBSTRATES.
A. Gupta, M. Yoganathan, J. Burton, F. Long, J. Whitlock, N. Thomas, T. Anderson, Litton Airtron, Morris Plains, NJ.

Affordable, high quality SiC wafers are very desirable for a variety of new technologies including GaN based lighting, RF, and high-power electronics based on wide band gap materials. At Litton-Airtron we have a major effort in the growth and characterization of SiC. We will present data on 35, 50 and 75 mm diameter crystals. We are growing both n-type and semi-insulating 4H and 6H material. Improved growth techniques have allowed for the production of exceptionally long crystals. Longer crystals grown at rapid growth rates with high transport efficiencies will allow for the reduction of the price of SiC wafers. A variety of characterization techniques are being used at Litton-Airtron to determine wafer quality. These include Raman microscopy, KOH etching of wafers for counting micro-pipe density, and crossed polarizer images. Raman spectroscopy is an excellent probe of polytype and carrier concentration for n-type materials; in addition it can be done at room temperature and is sufficiently fast that it can be used in an industrial environment. The use of digital photography allows for the collection of images that can be quantitatively analyzed and archived. We will also discuss some of the issues involved with micro-pipe counting. This work was partially supported by the DoD Title III program contract F33615-99-C-5318 and DUAP contract number F33615-98-2-5434.

H5.3
ONE OF MANY SOURCES OF DEFECT GENERATION IN SiC.
Igor Khlebnikov, Univ of South Carolina, Dept of Electrical Engineering, Columbia, SC; Yuri Khlebnikov, Bandgap Technologies Inc., Columbia, SC; Colin Wood, Office of Naval Research, Arlington, VA; Tangali S. Sudarshan, Univ of South Carolina, Dept of Electrical Engineering, Columbia, SC.

Silicon carbide is a unique material for the study of process of defect generation and crystallization. In this paper, for the first time, we report the observation of the entrapment of whiskers and dendrites (tree-like defects) within the volume of the growing monocrystalline SiC. The encapsulation of the tree-like defects in the volume of the grown crystal leads to solid state polytype transformation. According to Oswald rule, the most probable tranformation sequence is as follows: 2H $\rightarrow$ 3C? $\rightarrow$ nR? $\rightarrow$ 4H, 6H ... until a stable phase is established for the given conditions of crystal growth. We observe that the entrapment of tree-like defects are the source of SiC defects such as micropipes and planar defects. It is very likely that the above process is also the source of dislocations. Practically, every branch of the tree-like structure generates the above mentioned defects (micropipes, planar defects, etc.). Our investigation (by EDAX) shows that the chemical composition of the tree-like defect is the same as that of bulk SiC. In this paper, we will present the mechanism of the entrapment of the tree-like defects in the bulk crystal.

H5.4
DISLOCATION CONTENT OF ETCH PITS IN HEXAGONAL SILICON CARBIDE. Igor Khlebnikov, Mohsen Banizaman-Lari, Robert T. Bondokov, Tangali S. Sudarshan, Univ of South Carolina, Dept of Electrical Engineering, Columbia, SC.

6H- and 4H- SiC crystals grown on the Si-face were chemically etched on the as-grown (virgin) surface and the C-face (sliced side). The etching of both of the surfaces revealed a strong relationship between a variety of etch pits and the morphological features of the grown boule surface. Several types of etch patterns were revealed. On the Si face, we observed small, medium, and large hexagonal shaped pits and a linear array of small etch pits. However, the C face contained only small pits and a linear array of small pits. We observed individual or group of dislocations that were connected from the Si face to the opposite C face of the wafer. Also, etch pit lines oriented along specific crystallographic directions were seen. Our experimental observations have provided a physical basis to explain the generation of defects in SiC. An analysis of our observations shows that a correlation exists between the distribution of different size etch pits and the condition of the crystal growth process.

H5.5
SUBLIMATION GROWTH OF 6H-SiC Bulk ON VARIOUS A-PLANE SUBSTRATES. Shigehiro Nishino, Taro Nishiguchi, Tomoaki Furusho, Toshiyuki Shimizu and Makoto Sasaki, Department of Electronics and Information Science, Faculty of Engineering and Design, Kyoto Institute of Technology, Matsugasaki, Sakyo-ku, Kyoto, JAPAN.

Recently SiC epilayer on (11-20) plane is focused because high channel mobility of MOSFET was reported [1]. However, bulk growth of a-plane is limited. We already reported the preliminary result of a-plane growth [2]. In this presentation, we focus to grow 6H-SiC bulk on (11-20) and (1-100) planes. We already established the bulk growth by sublimation method and found optimum condition to 2 inch bulk. In this time, seed crystal was cut perpendicul to the growth direction, $< 0001 >$, from the bulk SiC grown on (0001) basal plane. Cross sections of the the substrates were carefully examined by X-ray diffraction and two a-planes, (11-20) and (1-100), were selected as the substrates. The crucible was set in the water cooled quartz tube and it was heated by rf induction. Sublimation growth was carried out following conditions; source temperature: 2400°C, substrate temperature: 2200°C, and inner argon pressure: 150 Torr. Growth rate was about 0.6 mm/h. The grown layer on (11-20) was a roof-shape and top of the roof directed to $< 11-20 >$ direction.The grown layer on (1-100) was almost flat. Growth rate of the bulk on (11-20) substrates was a bit faster than the (1-100) substrate. X-ray rocking curve was measured for the substrate cut from the substrate to top of the bulk. Better crystallinity was obtained on the top of the bulk. Enlargement of the bulk was not enhanced even though long run. Crystal defects were characterized by molten KOH and Raman spectroscopy. Electrical properties is also presented. [1] T. Kimoto et al. Proc. ICSCRM99. [2] S.Nishino et al. in "Amorphous and Crystalline silicon Carbide 3", (1992). Springer-Verlag. p.15.

H5.6
HEAT AND MASS TRANSFER MODELING FOR A BETTER KNOWLEDGE OF THE LARGE-AREA GROWTH OF HOMOEPITAXIAL SiC BY CVD. Jerome Meziere, Stephane Wan, Tang Kuan, Michel Pons, Elisabeth Blanquet, Roland Madar, Institut National Polytechnique de Grenoble, FRANCE; Eric Neyret, Pierre Ferret, Lea Di Coccio, LETI-CEA Grenoble, FRANCE.

In view of its excellent thermal, mechanical and electronic properties, silicon carbide is the semiconductor material of reference for high temperature, high frequency and high power devices. The 4H-SiC polytype is considered as the most attractive for the fabrication of such devices. The resulting applications have made tremendous progress primarily because of the commercial availability of SiC substrates of ever increasing diameter and quality. The growth of thick epitaxial layers with low defect density is an essential technique and the next step. Recently, hot wall reactors using silane and propane diluted in hydrogen were commercially available (Epigress - Sweden). The typical growth temperature range is 1800-2000 K and total pressure range 10-100 kPa. The resulting epilayers were grown at 10-15 μm/h. They exhibit low background doping, low defect density and good uniformity over 30 mm, the size of the typical wafers. The main problem is that it is difficult with this first generation of reactors to ensure a constant temperature over larger wafer dimensions (50 mm and the forthcoming 75 mm wafers). A 3D simulation approach of heat and mass transfer was used with three objectives. The first one is to have a visualization of the flow, temperature and gaseous species fields in the standard reactor. The second one is to propose solutions for the optimal control of the temperature field and the subsequent uniformity of the epilayers over large dimensions. The third one is to improve the kinetic databases in this temperature range which has been very little investigated. The combination of our recent experimental and modeling results remains the main objective of the presentation.

H5.7
CHARACTERIZATION OF SiC GROWN ON Ge MODIFIED SILICON SUBSTRATES. Jörg Pezoldt, Thomas Stauden, Plamen Maslarski, TU Ilmenau, Institut für Festkörperelektronik, Ilmenau, GERMANY; Pierre Masri, Universite de Montpellier, Groupe deEtude des Semiconducteurs, Montepellier, FRANCE.

The silicon carbide layers grown on silicon suffer from the high lattice and thermal lattice mismatch between these two materials leading to high residual stress and lattice defect densities in the grown silicon carbide layers. These lead to insufficient electrical properties of the grown silicon carbide layer and the heterojunction. The properties of the SiC layer can be improved by using one of the following methods: (1) SiC growth on SOI substrates, (2) SiC growth on porous Si, (3) growth of SiC on modified Si substrates. Only the last method is applicable if the electrical properties of the heterojunction are of interest. We used Ge predeposition on (111)Si surfaces by using a solid source molecular beam equipment to modify the properties of the SiC-Si heterojunction. This modified surfaces were then transformed into a thin SiC layer by using a carbonization step. Subsequently a SiC layer was grown. The grown layers were investigated by in situ RHEED, spectroscopic ellipsometry, ex situ AFM, XPS, XRD and FTIR. For electrical characterization a simple diode was prepared. It will be shown that Ge predeposition and incorporation into the heterointerface lead to and improved crystallinity of the grown layers. Furthermore the carried out U-I measurements showed a decrease of the reverse current of the SiC-Si heterojunction.

H5.8
FORMATION OF THE INTERFACIAL BUFFER LAYER USING MONOMETHYL SILANE FOR 3C-SiC/Si HETEROEPITAXY. Hideki Nakazawa, Maki Suemitsu, Tohoku University, Research Institute of Electrical Communication, Sendai, JAPAN.

Heteroepitaxy of 3C-SiC on Si wafers allows us deposition of large area single crystal 3C-SiC for electronic device applications. To form high-quality SiC films on Si wafers, it is crucially important to atomically control the surface morphology of the SiC/Si interfacial buffer layer to remove stacking faults. Since high-temperature processes cause surface degradation of the buffer layer, lowering the formation temperature of the buffer layer is of the highest priority. While the carbonization method using reactions between hydrocarbon gases and the Si substrate has been common, the high temperatures (typically T>900°C) required to decompose the hydrocarbon gases cause Si-voids in the Si substrate during the formation of the Si-C bonds. In this study, we have successfully formed the buffer layer at as low as $T \leq 650$°C by using monomethylsilane (H_3Si-CH_3; MMS) gas, and have obtained qualified 3C-SiC films onto the buffer layer using the MMS-gas-source MBE at 900°C [1]. Reflection-high-energy-electron-diffraction observation indicated a formation of a uniform single-crystalline SiC buffer layer over the Si substrate. We relate this success to the presence of a Si-C bond in the MMS molecule, which may play a great role in suppressing the Si out-diffusion during the buffer layer formation. The TO-phonon absorption from the film grown onto the buffer layer presented a sharp peak at 795 cm^{-1}, indicating that the film is fully relaxed. The shape is more symmetrical than that from the film grown directly onto the Si substrate. AFM evaluation indicated a RMS-roughness of ~3 nm. These observations clearly indicate that qualified 3C-SiC films with good surface morphology can be grown using the buffer layer by MMS, for which we named organo-silane method. [1] H. Nakazawa *et al.*, Thin Solid Films (2000), in print.

H5.9
STRUCTURAL PROPERTIES OF SiC LAYERS GROWN ON Si SUBSTRATES BY ELECTRON CYCLOTRON CVD TECHNIQUE. C.F. Pirri, G. Cicero, S. Ferrero, F. Giorgis, P. Mandracci, Polytechnic of Torino, ITALY; R. Reitano, P. Musumeci, L. Calcagno, G. Foti, University of Catania, ITALY; G. Barucca, University of Ancona, ITALY.

SiC is a wide bandgap semiconductor very interesting for high-power, high-frequency and high-temperature devices, due to its high breakdown field, high electron saturated drift velocity and good thermal conductivity. The cubic 3C polytype in SiC is interesting since, unlike other polytypes, it can be grown on Si substrates. Electron Cyclotron Resonance CVD is a plasma-assisted deposition technique, which allows a higher degree of ionisation respect to standard r.f. Plasma Enhanced-CVD, leading to a more efficient dissociation of the growing species. A new ECR-CVD deposition system which allows to join the advantages of the highly ionised ECR plasma with the possibility to reach a substrate temperature up to

2000°C, was aimed to growth epitaxial SiC films at a temperature lower than that required by thermal CVD. Several films of polycrystalline 3C-SiC were deposited on (100)-Si and (111)-Si wafers by the ECR-CVD technique, using SiH4 and CH4 as gas precursors at different flow rates, temperatures and microwave powers. The films were characterised by X-ray diffraction, transmission-electron-microscopy, stationary photoluminescence and micro-Raman spectroscopy to verify the internal structure, while Fourier-transform infrared absorption and Rutherford back-scattering spectrometry were applied in order to evaluate the chemical composition of the films. All the samples showed a polycrystalline structure, with columnar structure and lateral dimensions of the 3C-SiC grains in the range of 30nm-200nm, which strongly depend on film composition and growth history, showing in optimized conditions a preferential orientation close to that of Si substrate. A correlation between film structure and deposition conditions (included substrate surface preparation) is presented and discussed.

H5.10
EPITAXIAL GROWTH OF SiC ON AlN/ SAPPHIRE USING HEXAMETHYLDISILANE BY MOVPE. Kasif Teker, Ki Hoon Lee, Pirouz Pirouz, Case Western Reserve Univ, Dept of Materials Science and Engineering, Cleveland, OH; Chacko Jacob, Shigehiro Nishino, Kyoto Institute of Technology, Dept of Electronics and Information Science, Kyoto, JAPAN.

High quality SiC and AlN films allow the fabrication of metal/AlN/SiC MIS structures and SiC/AlN heterostructures that require a low lattice mismatch and excellent thermal stability. Epitaxial SiC on AlN/sapphire was grown using hexamethyldisilane (HMDS) by MOVPE. 2H-AlN is epitaxially grown on sapphire by MOVPE, and subsequently SiC is deposited on it. The growth of high quality SiC was achieved by one step process without any nucleation step using dilute hydrogen (12% H_2+Ar) as a carrier gas, which is less explosive than pure H_2. The effect of growth temperature, thickness of AlN, concentration of source precursor on the SiC crystal quality and the surface smoothness were studied. All films were analyzed using reflection high energy electron diffraction (RHEED), Nomarski differential interference contrast microscopy (NDIC), X-ray diffraction (XRD), and atomic force microscopy (AFM). Optimum temperature for SiC growth was between 1300°C and 1350°C. At temperatures between 1300°C and 1350°C, the films show strong epitaxial relationship with AlN and very smooth surface (RMS ~0.1-0.75 nm). Below 1300°C, the film becomes polycrystalline. At 1400°C, it was highly textured, observed by XRD. In the RHEED, however, weak rings appear superimposed on the spot pattern, which implies the films are highly textured but polycrystalline. In order to evaluate the effect of AlN on the SiC film, AlN layers with various thicknesses (50, 200, 400 nm) have been used at 1350°C. The SiC film on a 50 nm thick AlN layer shows very smooth surface (RMS ~0.1 nm) compared to the SiC film on a 400 nm AlN layer (RMS ~0.75 nm). This seems to be caused by the increasing roughness of AlN, as it becomes thicker. However, all the films show highly epitaxial growth features, which imply 50 nm is sufficient to relieve the mismatch strain of the underlying AlN/sapphire.

H5.11
EFFECT OF TMG ADDITION ON THE EPITAXIAL GROWTH OF 3C-SiC ON Si(100) AND Si(111) USING HMDS BY MOVPE. Ki Hoon Lee, Kasif Teker, Juyong Chung and Pirouz Pirouz, Dept. of Materials Science and Eng., Case Western Reserve University, Cleveland, OH.

Epitaxial and crack-free 3C-SiC film was successfully grown on Si(100) and (111) by one step without any nucleation or carbonization step at a low temperature of 1200°C by MOVPE. The growth was achieved by using hexamethyldisilane (HMDS) with the addition of a small amount of trimethylgallium (TMG) with dilute hydrogen (12% H_2 + Ar) as a carrier gas. Without the addition of TMG during growth, epitaxial growth of SiC on Si was only possible at temperatures above 1300°C with a nucleation step at 1250°C. After growth, all the films were analyzed by cross-sectional transmission electron microscopy (TEM), X-ray diffraction (XRD), atomic force microscopy (AFM) and X-ray photoelectron spectroscopy (XPS). It is observed by XPS that only a small amount of Ga is contained in the SiC film, which means Ga component of TMG is not incorporated much in SiC film, in spite of the relatively high ratio of TMG/HMDS. To investigate the effect of TMG flow rate, various amount of TMG (0.5 ~ 5sccm, 10sec ~ 30min.) was added during SiC deposition. Below 0.5 sccm of TMG flow rate, the SiC film shows epitaxial growth, as observed by TEM and XRD. However, above 1 sccm, the XRD peak of 3C-SiC becomes smaller and broadened, as the flow rate of TMG increase. This result implies that the SiC lattice is being strained gradually with the TMG addition. It is also observed by AFM that at the initial stage of growth, nucleation is much facilitated with the addition of TMG. The deposition rate with the addition of TMG at 1200°C is 500 nm/hr, which is much larger than the rate without TMG addition (300 nm/hr). Thus, it is believed that TMG addition make a positive effect on the nucleation and HMDS decomposition during deposition.

H5.12
OPTIMIZATION OF THE CARBONIZED BUFFER LAYER FOR THE GROWTH OF VERY HIGH QUALITY SINGLE CRYSTAL SiC ON Si. T. Cloitre, N. Moreaud, P. Vicente[a], M. Sadowski, M. Moret and R.L. Aulombard, Groupe d'Etudes des Semicon- ducteurs, Université Montpellier II, FRANCE. [a]NOVASIC, Plombières, Moutier, FRANCE.

Carbonized buffer layers were formed on Si (100) nominally oriented and 2° off substrates with propane diluted in palladium purified hydrogen, using different processes, in a cold wall vertical reactor. Subsequent SiC layers were grown using silane and propane at atmospheric pressure with growth temperature ranging from 1150°C to 1350°C. The layers obtained were characterized by LT photoluminescence, IR transmission and reflectivity, X-ray diffraction, micro-raman on clived edges, AFM, MEB and optical microscopy. We have focused our study on the reduction of etch pits density, the minimization of the residual strain on both sides of the Si/SiC heterointerface and the suppression of interfacial voids. Drastic influence on the layer surface morphology was evidenced depending on the transition step between the carbonization and the SiC epitaxial growth. We have also paid particular attention to the graphite susceptor condition by regularly reconditioning its surface, using an outgassing process and in-situ SiC coating. As a result, we have developed a two steps carbonization process leading to very high quality SiC films grown at 1200°C.

H5.13
INTERACTION OF OXYGEN WITH 4H- AND 6H- SILICON CARBIDE. Y. Song and F.W. Smith, Dept. of Physics, City College of New York, Graduate Center, City University of New York, NY.

The ability to grow passivating SiO_2 surface coatings on SiC is an important advantage of this material in both electronic and ceramic applications. The SiC O_2 reaction leading to the formation of SiO_2 is complicated, however, by the presence of carbon. A thermochemical model describing the interaction of O_2 with SiC will be used to predict the possible vapor and solid phase components formed and their locations in a CVD phase diagram. At high T and low O_2 pressures, $P(O_2)$, the SiC surfaces is etched, with the volatile SiO and CO species being formed. At intermediate T and $P(O_2)$ the products are solid SiO_2 and CO, while at low T and high $P(O_2)$ only solid products are predicted to be formed, i.e. SiO_2 and C. The unexpected prediction that solid C is a thermodynamically-stable product of the interaction of oxygen with SiC at low temperatures and high O_2 pressures will be analyzed and its implications for the growth of passivating SiO_2 films on SiC will be discussed. The results of experimental investigations of the interactions of oxygen with the Si- and C-terminated (0001) surfaces of 4H- and 6H-SiC will also be presented. It has been found that the C-terminated surface not only oxidized faster but also etchs more rapidly than the Si-terminated surface. Oxide decomposition via the reaction $2SiO_2+SiC \rightarrow 3SiO+CO$ has also been observed, with interesting differences found for the 4H- and 6H-SiC substrates studies.

H5.14
STRUCTURAL AND ELECTRICAL CHARACTERIZATIONS OF OXYNITRIDE FILMS ON SOLID PHASE EPITAXIALLY GROWN SILICON CARBIDE. L.K. Bera, W.K. Choi, Microelectronics Laboratory, Department of Electrical and Computer Engineering, National University of Singapore, SINGAPORE; D. McNeill, Department of Electronics and Electrical Engineering, The Queen's University of Belfast, Belfast, UNITED KINGDOM; S.K. Ray, Department of Physics and Meteorology, Indian Institute of Technology, Kharagpur, INDIA; S. Chatterjee, and C.K. Maiti, Department of Electronics and Electrical Communication Engineering, Indian Institute of Technology, Kharagpur, INDIA.

The potential applications of silicon carbide (SiC) films in high temperature, high power and high frequency MOSFET devices require high-quality dielectric. We present here structural and electrical results of as-prepared and rapid thermal oxynitride films on C^+ implanted solid phase epitaxially grown SiC. The oxynitride was grown using N_2O. The C concentration of the samples was estimated to be 1, 2 and 5 at. %. From the infrared spectra, samples with 1 and 2 at. % carbon showed an absorption peak at 615 cm^{-1} which indicates that the carbon is substitutionally incorporated into the silicon. No precipitation of SiC was detected as no peak was observed at around 794 cm^{-1}. However, for the 5 at. % C sample, some precipitation was observed as indicated by a broad peak at ~800 cm^{-1}. The oxynitride films showed the Si-O-Si stretching mode at 1070-1100 cm^{-1} and the bending mode at 450 cm^{-1}. The shoulder at 1067-981 cm^{-1} is due to the O-Si-N bond. The peak at 830 cm^{-1} is due the Si-N and Si-C bonds and C-O complex vibrational mode was

also observed at 663 cm^{-1}. The refractive indices of the oxynitride films with 1, 2 and 5 at. % C substrate were found to be 2.12, 2.18 and 2.40, respectively. Electrical characterization of the oxynitride films was carried out using the MOS capacitor structure. The interface state density was found to range between 5-8$\times 10^{12}$ $cm^{-2}eV^{-1}$ and increases with an increase in the C concentration. The electrical breakdown field was found to be in the range of 5-7 MV cm^{-1} and reduces with an increase in C concentration. All the samples showed electron-trapping characteristic with the trap generation rate higher for lower C content samples. The charge-to-breakdown value was measured as 5-20 mC cm^{-2} and decreases with an increase in C concentration.

H5.15
OXIDATION STUDY OF HYDROGENATED AMORPHOUS SILICON CARBIDE FILMS. W.K. Choi and L.P. Lee, Microelectronics Laboratory, Department of Electrical and Computer Engineering, National University of Singapore, SINGAPORE.

Hydrogenated amorphous silicon carbide (a-$Si_{1-x}C_x$:H) films have attracted significant research interests due to their potential applications in optoelectronic devices. We present here results of an oxidation study of a-$Si_{1-x}C_x$:H films prepared by the plasma enhanced chemical vapor deposition of silane and acetylene. The composition (i.e. x) of the samples was determined by the flow rates of silane and acetylene. Oxidation was carried out at 400 to 600°C in dry oxygen ambient. IR spectra of the as-prepared films showed the intensity of the Si-C peak decreases and the Si-CH_3 peak increases as x increases. The Si-H peak shifts to higher frequency as x increases. Note that the incorporation of CH_3 radicals in a-$Si_{1-x}C_x$:H films has shown to introduce voids and increased the porosity of the films. The IR spectra of the oxidized samples showed clear Si-O stretching and rocking/wagging modes for a-$Si_{0.2}C_{0.8}$:H and an absent of such modes for a-$Si_{0.5}C_{0.5}$:H and a-$Si_{0.7}C_{0.3}$:H films. We suggest that the growth of oxide on a-$Si_{0.2}C_{0.8}$:H is a result of voids that facilitate the diffusion of oxidants into the film. For sample oxidized at 400°C, we observed a super linear and a parabolic regime in the oxide thickness versus oxidation time plot. For sample oxidized at 500 and 600°C, only the parabolic regime was observed. The Si-O stretching peak of oxidized films were found to be at 1056-1071 cm^{-1} for films oxidized at 400 and 500°C. This shows that the oxides are rather porous and slightly oxygen deficient, i.e. $SiO_{1.7}$ and $SiO_{1.9}$ for the 400 and 500°C oxidized samples. The capacitance versus voltage curves of the Al-oxide-silicon capacitors fabricated from oxidizing the a-$Si_{0.2}C_{0.8}$:H films at 400-600°C showed a large flatband shift (>10V) and big hysterisis (10-15V). This indicates the oxide contained large amount of trapped charge.

H5.16
QUALITY OF THERMALLY GROWN OXIDE IN 4H-SiC OVER NITROGEN AND PHOSPHORUS IMPLANTED REGIONS. I.A. Khan, B. Um, M. Matin, M.A. Capano and J.A. Cooper Jr., Purdue University, Department of Electrical and Computer Engineering, West Lafayette, IN.

Recent studies of the dielectric strenght of thermally grown oxides reported in the literature have been over non-implanted epilayers [1]. The oxide breakdown strength was measured to be about 10MV/cm at room temperature [1]. The electrical characteristics of oxides specifically over implanted regions, however, have not been investigated as extensively. Oxide quality over implanted regions is important for SiC metal-oxide-field-effect-transistors (MOSFET) that have a gate electrode which overlaps the implanted source/drain regions. For n-channel MOSFETs, phosphorus and nitrogen are the preferred species for source/drain impantation. The quality of oxides over these regions can potentially affect the performance of the device. Low dielectric strength of the oxide can cause excessive gate leakage currents in the on-state, resulting in either total failure of the device or poor device transfer characteistics. Furthermore, excessive injection of carriers in these regions can significantly reduce the life of the device by creating a short between the source/drain and the gate. In this talk, we present the results obtained from the electrical characterization of capacitors formed on thermally grown oxides over implanted regions in 4H-SiC. The implanted samples were annealed at 1200°C for 30 min in argon. The oxide over these regions has a much lower breakdown field as compared to the non-implanted regions. For nitrogen implanted capacitors, catastrophic breakdown of the oxide at room temperature occured at about 7MV/cm, and for phosphorus capacitors it occured at about 2.5MV/cm. The results are compared with a control sample from the same wafer that is processed along with the above samples, but does not go through the implantation step. This sample had a breakdown field close to 9MV/cm. Additional measurements of the oxide leakage current taken at 100-200°C will be reported. The implications of these results on the performance of NMOSFETs will also be discussed.
[1] Anant K. Agarwal, Suresh Seshadri, and Larry B. Rowland, "Temperature Dependence of Fowler-Nordheim Current in 6H- and 4H- SiC MOS Capacitors," IEEE Electron Device Letters, Vol. 18, No. 12, December 1997.

H5.17
ATOMIC SCALE OXIDATION OF SILICON CARBIDE AND ABRUPT SiO_2/SiC INTERFACE FORMATION. F. Amy, H. Enriquez, P. Soukiassian, Commissariat a l'Energie Atomique, Saclay and Universite de Paris-Sud, Orsay, FRANCE; Yeu-kuang Hwu, Academia Sinica, Taipei, TAIWAN; F. Semond, CNRS-CRHEA, Sophia Antipolis, FRANCE; A. Mayne, G. Dujardin, CNRS-LPPM, Universite de Paris-Sud, Orsay, FRANCE; C. Brylinski, Thomson-CSF, Orsay, FRANCE.

Surface passivation is a central issue in successful SiC device applications. Thanks to the exceptional properties of silicon dioxide, the most promising passivation is expected to be achieved by surface oxidation. However, the latter might result in mixed Si and C oxides products for SiC due to the presence of a binary compound. We investigate the oxidation of the Si-rich 6H-SiC(1000)3x3 and 3C-SiC(100) surfaces by core level and valence band photoemission spectroscopies using synchrotron radiation and by atom-resolved scanning tunneling microscopy (STM). At the atomic scale, the STM study of oxygen interaction with the cubic 3C-SiC(100)3x2 surface is found to be significantly anisotropic with a propagation faster along dimer rows. Initial oxygen atoms interact with surface defects leading to the formation of other defects having the same nature. The latter defects become active sites upon further oxygen deposition leading to a self-propagating oxidation process. For hexagonal 6H-SiC(1000)3x3 surface, the STM study indicates an isotropic propagation of the oxidation in contrast to the cubic 3C-SiC(1000)3x2 surface behavior. The oxide growth is performed by oxygen exposures at surface temperatures from 300 K to 900 K. Unlike silicon surfaces, 6H-SiC(1000)3x3 oxidation is taking place already at very low oxygen exposures. The oxidation rate is significantly enhanced at increasing surface temperatures. The results also indicate that the direct oxidation of the 6H-SiC(0001)3x3 surface leads to SiO_2 formation at low temperatures (800 K) with a non abrupt interface having significant amounts of mixed (Si-O-C) and intermediate (Si 3, Si 2, Si) oxidation products. In contrast, C-free and abrupt SiO_2/6H-SiC(0001) interface formation is achieved when pre-deposited Si overlayer is thermally oxidized at low oxygen exposures and low temperatures (800 K).

H5.18
AB INITIO STUDY OF SiC/METAL POLAR INTERFACES: RELATION BETWEEN INTERFACE STRUCTURE AND SCHOTTKY-BARRIER HEIGHT. Shingo Tanaka (SWING), Masanori Kohyama, Osaka National Research Institute, Dept of Material Physics, Osaka, JAPAN.

Ab initio study of the SiC/metal polar interfaces has been performed based on a pseudopotential and a supercell method using the technique of the first-principles molecular dynamics method. SiC is very important for high-performance electronic and optelectronic devices. For such applications, it is essential to fabricate SiC/metal interface with good electronic property. Recently, our group has performed *ab initio* calculations for such interfaces as the SiC/Al and SiC/Ti system and obtained great interesting results, especially the difference of interface dipole and Schottky-barrier hight(SBH) for different terminated atoms pair. SBH is sensitive for atomic and electronic structures at the reactive interface and is difficult to discuss some traditional-simplified models. In present work, we carefully discuss the SBH with the calculated work functions for both the SiC-slab and metal-slab. Stable atomic configurations, charge distributions, local density of states and SBH are presented for the 3C-SiC(001)/Al, 3C-SiC(001)/Ti and 3C-SiC(111)/Ti polar interfaces, both the Si-terminated and C-terminated are dealt with. Results show that the C-terminated interfaces have strong covalent (partially ionic) bonding and large adhesive energies and small SBH. We thus say a good candidate for terminated atom in SiC devices with Al or Ti contacts is the carbon.

H5.19
ALUMINUM/NICKEL AND ALUMINUM/TITANIUM OHMIC CONTACTS TO P-TYPE SILICON CARBIDE DIFFUSED LAYER. Xaiobin Wang, Stanislav Soloviev, Ying Gao, Tangali Sudarshan, Univ. of South Carolina, Dept. of Electrical Engineering, Columbia, SC; John R. Williams, Auburn Univ, Leach Nuclear Science Center, Auburn, AL; John Crofton, Physics Department, Murray State University, Murray, KY.

The outstanding physical properties of silicon carbide allow utilizing this material for high temperature, high power, high frequency electronics devices. To achieve the highest performance of these devices stable ohmic contacts with as low as possible specific resistance are necessary. In this report we present a study of the contact resistance of 6H-SiC material with a diffused p-type layer.

The p-type layer was fabricated by diffusion from vapor phase into both p-type and n-type substrates. Surface concentration of holes in the diffused samples was about 10^{19} cm^{-3}. Metal contacts to p-type substrate (doping concentration is $1.2\times$ 10^{18} cm^{-3}) without diffused layer were formed as well. Two types of metal structures (Al/Ni and Al/Ti) with thermally evaporated aluminum and sputtered nickel and titanium have been studied. Before placement in deposition chamber samples were cleaned by standard RCA process. Annealing of the samples was realized either by an electron beam in vacuum or in a tube furnace with argon atmosphere at 1100°C. The values of specific resistance for p-type substrate with and without diffused layer were estimated by using a two terminal resistor structure (Cox and Strack method), while the values of specific resistance for n-type substrate with p-type diffused layer were measured using the transmission line method (TLM). To implement the Cox and Strack method an array of metal dots of diameter varying from 20 to 240 μm was fabricated on the top of a wafer and bottom side of the substrate was fully metallized. The influence of annealing conditions for each metal structure on the values of specific contact resistance is discussed in this report.

H5.20
LOW TEMPERATURE OHMIC CONTACT FORMATION OF Ni_2Si ON N-TYPE 4H-SiC AND 6H-SiC. A.M. Elsamadicy, D. Ila, R. Zimmerman, C. Muntele, L. Evelyn, I. Muntele, Center for Irradiation of Materials, Alabama A&M University, Normal, AL; D.B. Poker, D. Hensley, Solid State Division, Oak Ridge National Laboratory, Oak Ridge, TN; J.K. Hirvonen, J.D. Demaree, WMRD, U.S. Army Research Lab, APG, MD; M.A. George, University of Alabama in Huntsville, Huntsville, AL.

Nickel Silicide (Ni_2Si) is investigated as possible Ohmic contact to heavily nitrogen doped n-type 4H-SiC and 6H-SiC. Nickel Silicide was deposited with various thicknesses on both Si and C faces of the SiC substrates. The Ni_2Si contacts were formed at room temperature as well as at elevated temperatures (400K to 1000K). Contact resistivities and I-V characteristics were measured at temperatures between 100°C to 700°C. To investigate the electric properties, I-V characteristics were studied and the Transmission Line Method (TLM) was used to determine the specific contact resistance for each sample at each annealing temperature. Both Rutherford Backscattering Spectroscopy (RBS) and Auger Electron Spectroscopy (AES) were used for depth profiling of the Ni_2Si, Si, and C. X-ray Photoemission Spectroscopy (XPS) was used to study the chemical structure of the Ni_2Si/SiC interface. Acknowledgment Research sponsored in part by the NASA - Alabama Space Grant Consortium, Ctr. For Irradiation of Materials of Alabama A&M University and by the U.S. Department of Energy under contract DE-AC05-00OR22725 with the Oak Ridge National Laboratory, managed by UT-Battelle, LLC.

H5.21
COMPARISON OF CURRENT-VOLTAGE CHARACTERISTICS OF N AND P TYPE SiC SCHOTTKY DIODES. Qingchun Zhang, Vipin Madangarli, and Tangli S. Sudarshan, University of South Carolina, Dept. of Electrical Engineering, Columbia, SC.

Current - voltage (I-V) characteristics of N and P type SiC Schottky diodes with different Schottky contact diameters are compared in a temperature range of room temperature to 400°C. While the room temperature I-V characteristics of the N type Schottky diode after turn-on is more or less linear upto $\sim$100 A/cm^2, indicating a fairly constant on-state resistance, the I-V characteristics of the P type Schottky diode shows a non-linear behavior even after turn-on, indicating a variation in the on-state resistance with increase in forward current. The reduction in the on-state resistance of the P type Schottky diode, resulting in a non-linear increase in the forward current, is attributed to the activation of un-ionized acceptors with increase in temperature due to high current density. Though the voltage drop across the P type Schottky diode is initially higher than that across the N type Schottky diode, for the first time it is shown that at high current densities (>125 A/cm^2) the forward voltage drop across P type Schottky diodes is lower than that across N type Schottky diodes. Further, high temperature measurements clearly indicate that while the on-state resistance of N type Schottky diodes increases with increase in temperature, the on-state resistance of P type Schottky diodes decreases with increase in temperature until a 'knee temperature', above which the resistance increases as in the case of N type Schottky diodes. The knee temperature was found to be strongly dependent on the Schottky contact diameter, decreasing with decrease in contact diameter. Techniques such as 'current spreading dots' to reduce the threshold voltage of P type SiC Schottky diodes so as to exploit the observed negative resistance behavior will be discussed in detail in the paper.

H5.22
LOW TEMPERATURE FORMATION OF $NiSi_2$ CONTACTS TO SiC. A.H. Heuer, C.W. Deeb, H. Kahn, Case Western Reserve University, Dept. of MS&E, Cleveland, OH.

Thermodynamically stable, low specific contact resistance electrical contacts to SiC are essential to the application of such devices in high power or high temperature applications. Nickel disilicide ($NiSi_2$) is very useful for this application, as contacts can be formed on SiC by reacting a sacrificial layer of amorphous silicon (a-Si) with a layer of sputtered nickel at 300°C. Using sacrificial a-Si, $NiSi_2$ forms directly; this is not the case when Ni reacted with single crystal Si or with polysilicon, where more Ni-rich silicides initially form. Thin film resistivity and specific contact resistance have been measured using circular TLM devices. This SiC-$NiSi_2$ interface has also been characterized using high resolution TEM.

H5.23
OPTICAL ABSORPTION OF DOPED AND UNDOPED BULK SiC. K. Miller, J. Dunn, H.X. Zhang, M.O. Manasreh, Department of Electrical and Computer Engineering, University of New Mexico, Albuquerque, NM; Z.C. Feng, Institute of Materials Research & Engineering, SINGAPORE; I. Ferguson, EMCORE Corporation, Somerset, NJ.

Optical absorption spectra of undoped, n-type, and semi-insulating 6H and 4H bulk SiC were obtained in the spectral region of 200 - 3200 nm (6.20 - 0.3875 eV). Several features were observed in the absorption spectra collected for various samples. A sharp peak below the band gap was observed in 4H SiC. The intensity of this peak was observed to increase in samples that exhibit larger absorption due to free carriers, which leads us to conclude that the defect responsible for this peak is also the source of the free carriers in the materials. Additionally, a series of optical absorption peaks separated by approximately 21 meV were observed around 0.9185 eV (1350 nm). Based on preliminary analysis, these peaks may be due to s - p transitions in VSi - related defect. The optical absorption near the band edge was observed to be sample dependent. The optical absorption measurements of the band gap show that 4H SiC has larger band gap as compared to 6H SiC. In all doped samples, the band gap is decreased as the dopant density is increased. The variation of the band gap as a function of temperature is also observed to be sample dependent. In certain samples, the band gap was found to be approximately independent of temperature in the entire range of 10 - 300 K.

H5.24
ORDINARY AND EXTRA-ORDINARY DIELECTRIC FUNCTIONS OF 4H-SiC AND 6H-SiC IN THE 0.7 - 9 eV SPECTRAL RANGE. O.P.A Lindquist, K. Järrendahl, Dept of Physics and Measurement Technology, Linköping University, SWEDEN; D.E. Aspnes, Dept of Physics, NC State University, Raleigh, NC; S. Peters, SENTECH Instruments GmbH, Berlin, GERMANY; J.-T. Zettler, C. Cobet, Institut für Festkörperphysik, Technische Universität Berlin, GERMANY; A. Henry, H. Arwin, and N.V. Edwards, Dept of Physics and Measurement Technology, Linköping University, SWEDEN.

We present the first ellipsometric measurements of both the ordinary ($\epsilon \perp$ c-axis) and extra-ordinary ($\epsilon \parallel$ c-axis) dielectric functions of 4H- and 6H-SiC in the spectral range from 0.7 to 9.0 eV. Two sets of samples were measured for each polytype; material oriented (i) with the [11-20]-direction and (ii) with the [10-10]-direction normal to the surface. Optical axes were determined by reflectance difference spectroscopy and samples were aligned during subsequent ellipsometric measurements such that a 90° rotation of the [10-10]-oriented sample yielded spectra equaling that obtained for the [11-20]-oriented sample and vice versa. Results indicated that parallel components of ϵ differ most dramatically from perpendicular components at energies above 5 eV and that this difference is greater for 4H- that for 6H-SiC, consistent with expectations based on the physical structure of the polytypes and with current theoretical predictions. E.g., we observed that the effects of polytypism are more pronounced in the parallel vs. perpendicular components of ϵ; that this effect is more pronounced in the imaginary parts of $\epsilon \parallel$ c-axis; and that there is a relative decrease in the number of well-defined peak structures in $\epsilon_2 \parallel$ c-axis for 6H relative to 4H, as expected. We will discuss these and other differences in the context of the observed spectral features and their relationship to SiC bandstructure. E.g., preliminary results from both real and reciprocal space analysis of ellipsometric lineshapes indicates that the controversial shoulder observed near 5.5 eV in $\epsilon \perp$ c for 4H-SiC is indeed a critical point Eg=(5.47±0.05) eV with Γ=240 meV, with the E_1 peak of the same spectra located at Eg=(6.937±0.01) eV with Γ=179 meV.

H5.25
CALCULATION OF POSITRON CHARACTERISTICS IN SILICON CARBIDE. Bernardo Barbiellini, Northeastern Univ, Dept of Physics, Boston, MA; Jan Kuriplach, Charles Univ, Dept of Low Temperature Physics, Prague, CZECH REPUBLIC; Wolfgang Anwand, Gerhard Brauer, Research Center Rossendorf, Institute of Ion Beam Physics

and Materials Research, Dresden, GERMANY.

Positron affinity calculations performed by a first-principles approach based on density functional theory reveal, contrary to many other semiconductors, that free positrons and positronium can escape from SiC. It is found that the treatment of the electron-positron interaction plays a crucial role when calculating the annihilation characteristics. These characteristics originating from both valence and core electrons, combined with the corresponding measurements, yield a very useful tool for surface studies and point defect identification in the bulk. Calculations will be compared with experimental data obtained for positron annihilation in dislocations and the Si-C-divacancy which were created by ion implantation and subsequent annealing.

H5.26
THEORETICAL INVESTIGATION OF INTRINSIC DEFECT COMPLEXES IN α-SiC. Eva Rauls, Zoltán Hajnal, Thomas Frauenheim, University of Paderborn, Theoretical Physics, GERMANY; Ádám Gali, Péter Deák, Budapest University of Technology and Economics, Dept of Atomic Physics, HUNGARY.

Properties of isolated intrinsic defects in SiC are widely studied and their atomic and electronic structure is already known. Although further experimental evidence shows the presence of defect complexes, only a few of them could be clearly identified up to now. In binary semiconductors antisite pairs play a special role. In SiC it is expected to be a defect with high formation energy, however, it is likely to be created during irradiation, or non–equilibrium growth. The properties and role of these defects in diffusion, in growth as well as their interaction with other defects deserves consideration. Therefore, we describe first the atomic structure and properties of selected vacancy–antisite complexes calculated within a selfconsistent–charge density functional based tight binding scheme (*SCC-DFTB*). Since antisite pair formation in the perfect lattice is very unlikely to occur, we then systematically investigate the lowering of its formation energy and barrier in the presence of other intrinsic defects. Besides carbon vacancies, we find V_C-C_{Si} complexes to particularly promote formation of an antisite-pair. Its formation energy and barrier are reduced by over 1.0 and 4.5 eV, respectively. Since the calculated absolute energies are still too high to be relevant for thermal processes, further work is in progress to identify energetically more favourable routes.

H5.27
STUDY OF Ga IMPLANTED p-TYPE 6H-SiC FOR OHMIC CONTACT METALLIZATIONS. M.D. Prenatt, A.A. Iliadis, University of Maryland, Dept of Electrical and Computer Engineering, College Park, MD; M.C. Wood, M. Derenge, B. Geil, and K.A. Jones, Army Research Laboratory, Adelphi, MD.

The development of high quality ohmic metallizations on p-type SiC is of critical importance to the performance of high temperature/high power SiC devices. Our previous work indicated that the use of Ga focused ion beam (FIB) technology reduced contact resistance in p-type SiC significantly (1). During the application of the focused ion beam surface modification, Ga was found to be incorporated within the top 30 nm of the surface. In the present work, we have employed broad area implantation techniques to perform shallow (30 nm) Ga implantations on p-type 6H-SiC, and examined the physical and electrical properties of the system upon high temperature annealing. The implantations were carried out at an energy of 70 KeV and doses ranging between 10E15 and 10E16 per square cm. Samples were annealed between 1000 and 1600 C. SIMS annalysis was employed to verify the implanted profiles and identify the changes in the distribution of the elements, while AFM surveys were performed to identify morphological changes of the surface prior to and after treatment. An AlN layer of approximately 50 nm was also deposited by pulsed laser deposition (PLD) on the surface of the samples, in order to serve as a capping layer during annealing. The analysis showed that significant outdifusion of Si and redistribution of Ga still occured through the AlN layer at 1500°C. As-implanted and annealed samples were elactrically evaluated for contact resistance by the TLM method. The electrical and physical evaluation of the Pt-Ga-SiC metallization system will be reported and the implications of the incorporation of Ga into the SiC lattice will be discussed. (1) A.A. Iliadis et al, JEM Vol. 28, No 3, pp 136-140,1999

H5.28
STRUCTURAL, CHEMICAL AND ELECTRICAL CHARACTERIZATION OF 6H-SiC IMPLANTED BY MeV IONS AT 300°C AND ANNEALED AT 1700°C. R. Nipoti, M. Bianconi CNR-LAMEL, Bologna, ITALY; G. Mattei, CNR-IMAI, Roma, ITALY; A. Carnera, INFM and Universita degli Studi di Padova, Padova, ITALY.

6H-SiC on-axis and off-axis wafers were implanted at 300°C by N or Al ions at different energies between 300 keV and 3 MeV and different fluence values so to produce 1 mm thick doped layers with a doping concentration modulated across the value 5 x 10^{19} cm^{-3}. Peaks and valleys were intentionally produced in this box shape profile. All the samples were annealed at 1700°C for 30 min. The structural characterisation of the as-implanted and annealed samples was done by Rutherford Back-Scattering spectrometry (RBS-C) in the $< 0001 >$ channeling geometry and by confocal micro-Raman spectrometry (m-R) (Ar laser 514.5 nm). Only micro-Raman allow us to estimate the thickness of the damaged layer by taking into account both the integrated intensities of the 789 cm^{-1} band and of the broad bands due to crystal disorder as a function of the laser beam focusing distance from the sample surface. After the annealing the crystalline quality was restored as measured by RBS-C and m-R and no material loss was detected as shown by the comparison of the doping profiles in the as implanted and annealed samples as measured by Secondary Ion Mass Spectrometry (SIMS). m-R cross measurements of the annealed samples allowed us to study the behaviour of LO phonon-plasmon mode from which information on the depth distribution of the free carrier density was extracted.

H5.29
DIFFERENCE IN SECONDARY DEFECTS BETWEEN HIGH ENERGY B^+ AND Al^+ IMPLANTED 4H-SiC. Toshiyuki Ohno, Ultra-Low-Loss Power Device Technology Research Body (UPR)/R&D Association for Future Electron Devices (FED), Tsukuba, Ibaraki, JAPAN; Naoto Kobayashi, UPR/Electrotechnical Laboratory, Tsukuba, Ibaraki, JAPAN.

B^+ implanted pn junction has small reverse leakage current than that in Al^+ implanted one. This result has some relation with the residual defects in implanted layers but detailed reason is not clear. In this paper, we report on the cross-sectional TEM observations in high-energy B^+ or Al^+ implanted 4H-SiC and show the difference in the size, structure and distribution of secondary defects between the two implanted layers. For the similar dopant concentration, B^+ implanted samples have larger size of secondary defects compared to Al^+ implanted ones. For example, when the dopant concentration is 2-4×$10^{18}$$cm^{-3}$ (dose of 7×$10^{14}$$cm^{-2}$ for 2.0-0.5MeV B^+ implantation and dose of 2.6×$10^{14}$$cm^{-2}$ for 2.0-0.5MeV Al^+ implantation) and annealing temperature is 1700°C, the defect size in B^+ implanted sample is 4-20nm and that in Al^+ implanted one is 2-7nm. In B^+ implanted sample, the structure of the defects larger than 12nm is dislocation loop with an extra Si-C bilayer parallel to {0001} (type-A) and those smaller than 12nm have no extra plane and show strained contrast (type-B). On the contrary, defects in Al^+ implanted sample re all type-B. When Al^+ dose is increased to 2.6×$10^{15}$$cm^{-2}$, the size of defects grows 3-15nm. In this sample, the defects with the size larger than 12nm are type-A and others are type-B. Secondary defects in implanted layers of 4H-SiC are probably formed by agglomeration of interstitials, generated by implantation and when enough amount of them are inserted on the basal plane, type-A defects are formed. Above mentioned results suggest that agglomerating kinetics of interstitials are different between B^+ and Al^+ implanted layers and interstitials can cluster easier in B^+ implanted ones. This work was performed under the management of FED as a part of the MITINSS Program (R&D of Ultra-Low-Loss Power Device Technologies) supported by NEDO.

H5.30
PHYSICAL AND ELECTRICAL CHARACTERIZATION OF RESIDUAL IMPLANT DAMAGE IN 4H-SiC DOUBLE IMPLANTED BIPOLAR TECHNOLOGY. N.G. Wright, C.M. Johnson, S. Ortolland, A.B. Horsfall, K. Adachi, A.G. O'Neill, Dept of Electrical Engineering, University of Newcastle, UNITED KINGDOM; P.G. Coleman, Dept. of Physics, University of Bath, UNITED KINGDOM; A.P. Knights, Dept of Electrical Engineering, University of Surrey, UNITED KINGDOM.

The effects of post-implant anneal conditions on the level of residual damage resulting from nitrogen and boron implants after different anneal processes are investigated using the PAS and RBS techniques. It is shown that after implantation there is a substantial defect concentration significantly below the range of the implants. However such damage is almost completely recovered after anneal in contrast with the damage close to the implant range point. Such residual damage has a strong effect on the electrical characteristics of double implanted bipolar transistors - principally though reduction in carrier mobility and lifetime. It is shown that the precise implant and anneal conditions play a strong role in the electrical characteristics of such devices and a methodology for optimising such conditions is suggested.

H5.31
IMPURITY ACTIVATION IN N^+ ION-IMPLANTED 6H-SiC WITH PULSED LASER ANNEALING METHOD. O. Eryu, K. Aoyama, K. Abe and K. Nakashima, Dept. of Electrical and Computer Engineering, Nagoya Institute of Technology, Nagoya, JAPAN.

We have succeeded in pulsed laser annealing of N^+ ion-implanted 6H-SiC, which induces little redistribution of implanted impurities after annealing. By repeated laser irradiation at low energy density without melting the surface region, the ion-implanted impurities was electrically activated. SiC substrates with impurity concentration of $7.6 \times 10^{17}/cm^3$ were implanted with 30 keV N^+ ions with dose of $4.8 \times 10^{13}/cm^2$ (N concentration at the Rp was $1 \times 10^{19}/cm^3$). After pulsed laser annealing, a contact resistance was measured to be $5.7 \times 10^{-5}\Omega cm^2$ using Al electrodes deposited on the N^+-implanted layer. Using the time resolved optical reflectivity measurements, we have obtained the transient information during laser annealing. The vibration of the reflectivity was observed during the laser annealing on samples which were amorphized by ion-implantation. We consider that this oscillations should be caused by interference with optical reflections from both the surface of the substrate and that of the self propagating liquid layer, moving in the amorphous SiC towards the interface between the amorphouse layer and the crystalline substrate. In the case of laser irradiation on the sample implanted with such a low dose of ions as that dose not induce an amorphous layer, the change of the reflectivity was slight, and the vibration of the reflectivity was not observed. Present results show that the impurity-doped layer with a high carrier concentration can be formed by both ion-implantation and pulsed laser annealing methods at the room temperature.

H5.32

EFFECT OF C/B SEQUENTIAL IMPLANTATION ON THE B ACCEPTORS IN 4H-SiC. Yoshitaka Nakano, Tetsu Kachi, Hiroshi Tadano, Toyota Central R&D Labs., Inc., Aichi, JAPAN; Rajesh Kumar Malhan, Denso Corp, Aichi, JAPAN.

Ion implantation technique is important as a selective area doping process in SiC electronic devices. Boron (B) is one of the promising group-IIIA acceptor impurities for SiC and forms shallow acceptor level and deep level. B-related deep defect can lead to the degradation of the device electrical characteristics in long terms; therefore, a suitable process is needed to suppress the deep defect level, known as D-center. Troffer et al. have demonstrated that the sequential implantation of C/B can suppress the formation of the D-centers based on a site-competition effect. In this study, using thermal admittance spectroscopy (TAS) and deep level transient spectroscopy (DLTS), we have systematically investigated the effect of sequentially co-implanted C on the formation of shallow and deep levels introduced by the C/B sequential implantation. (0001)-oriented 4H-SiC P^-/P^+ epitaxial wafers were used. The background Al impurity concentration and thickness of the epitaxial layer were $1x10^{16}cm^{-3}$ and $5\mu m$, respectively. Multiple step C and B implantation with suitable ion energies was performed at 1000°C (depth=$0.75\mu m$). The mean B concentration in the implanted region was $1x10^{18}cm^{-3}$. The C concentration was varied from $1x10^{16}$ to $1x10^{20}cm^{-3}$. The samples were annealed at 1700°C in Ar to activate the dopants. Finally, TAS and DLTS measurements were performed on fabricated Schottky diodes. The density of D-centers was found to start decreasing with increasing concentration of co-implanted C and to be completely suppressed for the C and B ratio of 1:1. However, a new deep level defect shows up at about 450meV for the C and B ratio of 10:1, i.e., C-rich condition. The C-V results also indicate a decrease in the free hole concentration under the C-rich condition. As a result, the concentration of co-implanted C is found to be very sensitive to the formation of B acceptors and deep levels.

H5.33

PULSED LASER PROCESSING ON SiC SUBSTRATES AND ITS APPLICATION TO UV SENSORS. Kenshiro Nakashima, Osamu Eryu and Yuichi Nishikuni, Nagoya Institute of Technology, Dept. of Electrical and Computer Engineering, Nagoya, JAPAN; Masanori Watanabe, Ion Engineering Institute Corporation, Osaka, JAPAN.

Silicon Carbide (SiC) devices are expected for use in high temperature environments under high power and low loss conditions. Several sensor applications such as ultraviolet sensitive diodes (UV sensors) and gas sensors are other fields of targets for SiC devices under the high temperature environment. Although SiC diodes are suitable for detecting UV emissions around 300nm because of the wide band gap energy of the material, they need shallow junction depth less than about 100nm for optimum detection of the UV emission. Additional refinements of impurity-doped layers are necessary for fabricating such a shallow junction except usual procedures such as ion implantation and subsequent annealing. In addition, ohmic electrodes prepared with the high temperature annealing procedure easily penetrate the thin junction region to destroy the diode characteristics. For further development of such SiC devices, we need both to improve impurity-doping techniques and to lower the device processing temperature. This paper describes results on controlling Al doping-profiles in n-type 6H-SiC with the pulsed laser processing using a KrF excimer pulsed laser and a gas source containing Al. Acceptor properties of Al impurities in the as-doped state are confirmed with both Hall effect measurements and photoluminescence bands due to the electron transition from the conduction band to Al-acceptor level at $E_v 0.239$ eV. A shallow p-n junction obtained by the present process is applied to fabricate UV sensor diodes. The laser processing techniques have made it also possible to fabricate Ti/Al ohmic contacts with a narrow contact transition region on the Al-doped thin layer. Together with Al-doping and contact fabrication techniques, UV-sensitive p-n junction diodes are realized with a spectral response in the investigated range from 300 nm to 430 nm. Preliminary external quantum efficiency is estimated to be 40% at 340 nm without surface passivation.

H5.34

OPTICAL PROPERTIES AND MICROSTRUCTURE OF ION-IMPLANTED SiC. F.W. Smith and Y. Song, Dept. of Physics, City College of New York, NY.

Ion implantation is the preferred method of introducing dopants into SiC. Depending on the level of implantation, the resulting damage can lead to the amorphization of this material and the loss of chemical order. Chemical ordering in SiC corresponds to a high concentration of Si-C bonds and is observed in deposited amorphous SiC films. When ion implantation of SiC occurs at low T, however, the disordered region may not be able to reach a relaxed amorphous state of lower free energy. As a result, significant concentrations of like-atom bonds, i.e. Si-Si, C-C, and C=C, are likely to be present. The presence of these bonds can be detected optically since Si-Si and C=C bonds absorb below the optical energy gap of SiC. Measurement of the optical dielectric function ϵ of the implanted region can serve as a useful probe of the microstructure of the disordered material and also its evolution with the degree of implantation and annealing. Effective medium models have been used to describe the dependence of the optical response of the damaged SiC on its microstructure. Such a model based on a homogeneous mixture of four components (amorphous Si with Si-Si bonds, amorphous C with C-C and C=C bonds, amorphous SiC with Si-C bonds, and void regions) will be used to determine whether the local bonding is random, chemically-ordered, or phase-separated. The predictions of this model will be presented and compared with existing experimental results to determine how the volume fractions of these four components vary with the level of ion implantation and with annealing.

H5.35

HIGH HOLE LIFETIME ($3.8\mu s$) IN 4H-SiC DIODES WITH 5.5 kV BLOCKING VOLTAGE. Pavel A. Ivanov, Michael E. Levinshtein, Sergey L. Rumyantsev, Ioffe Inst of Russian Acad of Sci, Solid State Electronics Division, St. Petersburg, RUSSIA; Kenneth G. Irvine, Olle Kordina, John W. Palmour, Ranbir Singh, Cree Inc, Durham, NC.

Pulse current-voltage characteristics and minority carrier lifetime at high injection level have been measured in 4H-SiC $p^+ - n$ diodes with 5.5 kV blocking voltage. The voltage-blocking n-layer (base) W_n was $50\,\mu m$ thick and had a donor doping concentration $N_d - N_a = 6 \times 10^{14}\,\mathrm{cm}^{-3}$. The doping level in the p^+- emitter directly above the junction was $3 \times 10^{18}\,\mathrm{cm}^{-3}$. The structure diameter was $500\,\mu m$. To estimate the effectiveness of base modulation by minority carriers, isothermal forward current-voltage characteristics of the diodes were measured in the temperature range from 293 to 550 K up to current densities j of about $400\,\mathrm{A/cm}^2$. At $j = 400\,\mathrm{A/cm}^2$, the diode differential resistance was found to be $4 \times 10^{-3}\,\Omega\mathrm{cm}^2$. Meanwhile, the ohmic resistance of non-modulated base is $R_\Omega = W_n/e\mu_n n_0 \approx 6 \times 10^{-2}\,\Omega\mathrm{cm}^2$, i.e. 15 times higher than the experimentally observed value, provided that $\mu_n = 800\,\mathrm{cm}^2/\mathrm{Vs}$ and $n_0 = N_d - N_a = 6 \times 10^{14}\,\mathrm{cm}^{-3}$. Hence, the current-voltage characteristics demonstrate directly the high level of base resistance modulation. Hole lifetime τ_p in the n-base of the diodes has been measured in the temperature range from 293 K to 550 K using Open Circuit Voltage Decay technique. The τ_p increases monotonically from $\sim 0.6\,\mu s$ at 300 K to $\sim 4\,\mu s$ at 550 K. To the best of our knowledge, the above values of τ_p are the highest reported for 4H-SiC.

H5.36

FABRICATION OF 2.4KV HIGH VOLTAGE N-TYPE 4H-SiC SCHOTTKY BARRIER DIODES USING THICK EPITAXIAL LAYERS. Takashi Tsuji, Hiroyuki Fujisawa, Shinji Ogino, Fuji Electric Corp. R&D Ltd., Yokosuka, JAPAN; Hidekazu Tsuchida, Isaho Kamata, Tamotsu Jikimoto, Kunikazu Izumi, Central Research Institute of Electric Power Industry, Yokosuka, JAPAN.

Fabrication and characterization of n-type 4H-SiC Schottky barrier diodes using $27\mu m$ thick epitaxial layers with the carrier concentration of $2 \times 10^{15}cm^{-3}$ grown by low pressure chemical vapor deposition are presented. These Schottky barrier diodes have the guard rings of $100\mu m$ width and $0.5\mu m$ depth, which were made by boron ion implantation followed by the 30 minute annealing at 1700°C. The Schottky barrier diodes with the diameter of 4mm showed the breakdown voltages more than 800V and the leakage

currents of 1×10^{-3}A/cm^2 at -600V. Breakdown voltage 2.4kV, which was 55% of the ideal parallel plane breakdown voltage, was obtained in 1mm diameter Schottky barrier diode. It showed Schottky barrier height of 1.61eV with an ideality facter of 1.01. The on-resistance was 12.7mΩcm^2, which was a little higher than that of the substrate is 9.7mΩcm^2. Optical beam induced current analysis was done to clarify the origin of the high leakage current over the wide range from 1×10^{-7}A/cm^2 to more than 1×10^{-1}A/cm^2. Many bright spots were recognized in the high leakage current SBDs.

H5.37
TEMPERATURE DEPENDENCE OF CHANNEL MOBILITY IN 4H-SiC MOSFETS. Shinsuke Harada[1,3], Ryoji Kosugi[1,3], Jyunji Senzaki[1,3], Seiji Suzuki[1,2], Won-Ju Cho[1,3], Kenji Fukuda[1,3], Kazuo Arai[1,3]. [1]Ultra-Low-Loss Power Device Technology Research Body, [2]R&D Association for Future Electron Devices, [3]Electrotechnical Laboratory, Ibaraki, JAPAN.

4H-SiC metal-oxide-semiconductor field effect transistor (MOSFET) is a promising candidate for high power electronic devices due to excellent physical properties of 4H-SiC. However, some problems still exist to achieve the high quality 4H-SiC MOSFETs. The most important is the low channel mobility of electrons in the surface inversion layers. 4H-SiC MOSFETs with a thermally grown gate oxide have a channel mobility less than 10 cm^2/Vs, which is much lower than that of bulk 4H-SiC (~800 cm^2/Vs). Recently, Schörner et al. have analyzed the temperature dependence of the channel mobility in p-type 6H-SiC MOSFETs, and proposed that interface states near the conduction band edge has a great influence on the low channel mobility. In this study, we have investigated a thermal activation process for the channel mobility in order to clarify the origin of low channel mobility in 4H-SiC MOSFETs. These MOSFETs were fabricated on p-type 4H-SiC (0001) wafers. A gate oxide was grown by thermal oxidation in a wet and dry O_2 atmosphere, resulting in a thickness of ~40 nm. Electrical characterizations of the samples were performed by current-voltage and capacitance-voltage measurements at temperatures up to 250°C. Channel mobility and threshold voltages were determined from $I_d{}^{1/2}$-V_g plots using a V_d in the saturation region. The channel mobilities in both dry and wet oxidized samples were less than 10 cm^2/Vs at room temperature, and increased with increasing temperature. On the other hands, threshold voltage decreased drastically as temperature is increased because the negative charges decreased at the SiO_2/SiC interface. The measured activation energies for the channel mobilities were less than 0.1 eV. This suggests that the observed increasing in the channel mobility with temperature is originated from the reduction of Coulomb scattering due to the activation of electrons from the interface state traps within 0.1 eV from the conduction band edge.

H5.38
INTERFACE EFFECTS ON THE RAMAN SPECTRA OF Si/3C-SiC SUPERLATTICES. E.F. Bezerra, A.G. Souza Filho, J. Mendes Filho, V. Lemos, V.N. Freire, Departamento de Física, Universidade Federal do Ceará, Fortaleza, BRAZIL; Y. Ikoma, T. Endo, F. Watanabe, and T. Motooka, Dept Materials Science and Engineering, Kyushu University, Fukuoka, JAPAN.

Among the several polytypes, only the cubic 3C-SiC can be grown epitaxially on Si(100) substrate. The inverse heteroepitaxial grpwth of SiC on 3C-SiC was recently demonstrated by the use of a pulsed supersonic free jets technique, thus making it possible to obtain multilayer structures, whose interfacial regions were observed to have nanometric thickness by high-resolution transmission electron microscopy measurements [1]. Here, we present calculations of the Raman spectra of $(3C\text{-}SiC)_{8-\delta}/(3C\text{-}SiC)_{0.5}Si_{0.5}/Si_{8-\delta}/((3C\text{-}SiC)_{0.5}Si_{0.5})_{\delta}$ superlattices for several values of interface thickness, δ, (in units of monolayers). The dispersion relations were obtained using a linear chain model with the alloyed interface considered in the virtual crystal approximation. A modified bond-polarizability model was used to calculate the Raman spectra. The analysis of the corresponding atomic displacements for the ideal superlattice allowed us to describe all the acoustic modes as extended through the whole superlattice. The optical modes, however, were seen to be extended only for frequencies ω below 518cm^{-1}. Two optical modes, accidentally degenerated at ω = 518cm^{-1} are quasi-confined in the Si-layers. The modes occurring in the frequency 518–620 cm^{-1} are quasi-confined in the 3C-SiC-layers. Completely confined modes in 3C-SiC-layers occur in the 800–1000 cm^{-1} range. In the Raman spectrum of $\delta = 0$ superlattices the two dominant peaks are at ω = 518cm^{-1} and ω = 969cm^{-1} corresponding to the Si-quasi-confined and the 3C-SiC-confined modes, respectively. Only very weak structures are present in between. By considering the existence of an interface region, however, several new peaks arise in this region, with increased intensity as the interface becomes thicker. For an interface thickness $\delta = 3$ some of these peaks have intensity comparable with those of the abrupt superlattice. The appearance of the new peaks can be interpreted as due to modes confined in the interfacial transition regions, mainly.
Y. Ikoma, T. Endo, F. Watanabe, and T. Motooka, Appl. Phys. Lett. **75**, 2977 (1999).

H5.39
RAMAN SCATTERING AND DEPTH PROFILING ON EPITAXIAL SILICON CARBIDE STRUCTURES. Z.C. Feng, Institute of Materials Research & Engineering, SINGAPORE; L.T. Hiang, G. Karunasiri, S.J. Chua, National Univ of Singapore, Centre for Optoelectronics; K.P.J. Williams, G.D. Pitt, Renishaw plc, UNITED KINGDOM.

In recent years, research and development on SiC have been greatly enhanced. Commercial 6H and 4H SiC bulk and epitaxial wafers are available. To meet various electronic and optoelectronic applications, it is needed to non-destructively assess the quality and properties of these structural wafers. In particular it is challenging how to evaluate the variation along the growth direction without damaging the materials. In this report, we are applying and developing the Raman scattering depth profile technique for its application in 4H-/4H- and 6H-/6H-SiC homo-epitaxial structures. By computer-automate-adjusting the sample stage, the laser focusing plan can be changed to obtain the Raman spectra at different depth in the normal direction of the sample in the micrometer scale. The Raman scattering depth profiles of un-doped and n-doped SiC films of 4H- and 6H- grown on homo-type substrate are acquired. Strong transverse and longitudinal optical (LO) phonon as well as the LO-plasma coupling modes are shown. Features from the heavily doped substrate and lightly doped epitaxial layer can be distinguished through the shape, frequency and intensity of the A1 symmetry LO mode. Through the theoretical modeling and fitting of the line shape of the LO-plasma coupling modes, the free carrier concentration can be determined at different depths. The doping variation in the film normal direction, therefore, can be obtained non-destructively. We have performed the Raman depth profile measurements on a series of 6H-/6H- and 4H-/4H-SiC samples and obtained their free carrier concentration and doping levels in the order of 10th power of 18 to 19 per cubic centimeters for substrate and 10th power of 16 to 17 for epi-layer. These are consistent with the results measured by other methods. Further efforts are pursuing to raise the accuracy of this measurement technology.

H5.40
CHEMOMECHANICAL POLISHING AND RAPID THERMAL ANNEALING OF SiC: RAMAN SPECTROSCOPY AND ESCA (XPS) STUDIES. Bahram Roughani, Uma Ramabadran, Diana Phillips, Science and Mathematics Department, Kettering University, Flint, MI; W.C. Mitchel, and C.L. Nelsen, Air Force Research Laboratory, Materials and Manufacturing Directorate, Wright Patterson AFB, OH.

Raman scattering and ESCA (XPS) studies on Nitrogen doped SiC samples revealed changes due to mechanical, chemomechanical polishing (CMP) and rapid thermal annealing (RTA) on surface and bulk properties of our samples. The SiC wafers were standard commercial grade 4H-SiC grown by the physical vapor transport process with no epitaxial layers, and nitrogen dopant at around 5x18 cm^{-3}. A SiC wafer was divided, so two sets of samples were prepared for these studies. The first set was mechanically polished and subsequently treated by RTA at 600-1100°C temperature range. The second set of samples was CMP and subsequently treated by RTA at the exact same temperature as the first set of samples. Phonon peaks do not show any significant changes due to the polishing and RTA treatment for two sets of samples. However, Raman scattering investigation shows certain changes in the coupled plasmon-LO phonon (CP-LOP) modes. For CMP samples with RTA treatment only samples with annealing temperature of above 1000°C show an increase in the peak position of the CP-LOP mode. However, for the mechanically polished samples, the CP-LOP modes shift with temperature for 600-1100°C. The shift in this coupled mode indicates a change in the free carrier concentration. Our ESCA (Electron Scattering for Chemical Analysis, also known as XPS) analysis of SiC samples shows differences in the Si, C, N, and O peaks. Observed changes in the binding energies show a trend with the annealing temperature and surface polishing process. Similar to the Raman studies, the most noticeable changes in the ESCA spectra were observed for annealing temperatures above 1000°C. The correlation between the ESCA and changes in the Raman spectra will be discussed.

H5.41
RESISTLESS ETCHING OF SiC WITH PHOTO OXIDATION REACTION BY USING EXCIMER LASER. Masahiro Toda, Jie Yang, Masataka Murahara, Tokai Univ, Dept of Electrical Engineering, Kanagawa, JAPAN.

We developed new etching method of SiC, using Photo Chemical reactions by excimer laser. SiC is expecting as a Semi-conductor

material of next generation. And SiC is called environment free semi-conductor material (heats, radiation, chemical and abrasion resistance). But, on manufacturing point of view, SiC is very tough material. Because, SiC has characteristics of very high physical hardness, and quite high chemical stability, it seems very tough to make micro-lithography onto SiC substrate. We use to reported several etching methods of SiC and showed possibility of micro-photolithography, by photochemical reactions of ClF_3 or NF_3 gases. But, it is very difficult to handle those reaction gases. We developed a photo etching method of SiC, which is using hydrogen peroxide (H_2O_2) and hydrogen fluoride water solution (HF) as activated species, to run etching process easily and safely. Put small mount of mixed solution of hydrogen peroxide and hydrogen fluoride on SiC substrate then put sapphire window onto solution to make thin liquid layer above the SiC surface. KrF eximer laser beam was projected through patterned photo mask, vertically. The area where the laser beam was projected, activated oxygen was produced by photolysis of hydrogen peroxide. And also, SiC surface was excited by UV light, which penetrated thin liquid layer. Then activated oxygen was oxidized Si and C of excited SiC surface producing SiO_2 and CO_2. CO_2 was released to the Air as gas, but SiO_2 was left on substrate. This produced SiO_2 was etched by hydrogen fluoride, which exists in mixed solution. For example of our experiments, when 10,000 shots of KrF Laser, energy density was 600mJ/cm^2 and mixture rate of solution was 10:1 (H_2O_2 : HF), etch depth was 40nm.

H5.42
REACTIVE ION ETCHING OF SiC USING C_2F_6/O_2 INDUCTIVELY COUPLED PLASMA. Sung-Min Kong, Byung-Teak Lee, Chonnam National Univ, Dept of Metallurgical Engineering, Kwangju, KOREA.

Etching characteristics of n-type 6H-SiC and 4H-SiC using C_2F_6/O_2 inductively coupled plasma have been investigated as a function of ICP coil power (600 $\sim$ 900W), substrate bias power (0 $\sim$ 300W), and O_2 concentration(0$\sim$70%). The etch rate increased rapidly with rf bias power and O_2 concentration resulting in 260nm/min etching rate at the optimum condition of 800W (ICP coil power), 200W (bias power), 4mTorr and 60% O_2 concentration. The etching profile is highly anisotropic and the etched surface of SiC was clean. Root-mean-square (RMS) roughness were 2 $\sim$ 10 nm for etched SiC over wide range of etching conditions. Micromasking effect and trenching effect were observed in the case of high bias power conditions. Recents at the I-V test and AES analysis will be also discussed in the presentation.

H5.43
SURFACE CHARACTERIZATION OF 3C-SiC FILMS GROWN BY CVD ON Si(001) AND (211) SUBSTRATES. B.A. Grayson, M.K. Graves, and J.T. Wolan, Dave C. Swalm School of Chemical Engineering, Mississippi State University, Mississippi State, MS; M.R. Bledsoe and S.E. Saddow, Emerging Materials Research Laboratory, Department of Electrical & Computer Engineering, Mississippi State, MS.

In this study the outermost atomic layer, near-surface region, and film/substrate interface of air-exposed thin 3C-SiC films grown on a 50-mm (2-in.) diameter Si(001) and 2 cm square Si(211) substrates have been investigated. Two sets of 3C-SiC films were investigated. First a carbonization process was used to create the film in a RF induction-heated horizontal atmospheric-pressure chemical-vapor-deposition (APCVD) reactor utilized a propane-hydrogen mix (3% C3H8 in ultra-high purity hydrogen) with a hydrogen carrier gas [1]. The second set of films studied was identical to the first with additional growth performed whereby a silane-hydrogen mix (3% SiH4 in ultra-high purity hydrogen) was added to the carbonnized layer to effect a 3C-SiC film via standard silane-propane 3C-SiC growth methods [1]. Angle-resolved X-ray photoelectron spectroscopy (ARXPS), Auger electron spectroscopy (AES) and ion scattering spectroscopy (ISS) were performed on the four films. Chemical-state identification, in-depth elemental distribution profiles and outermost atomic layer compositions of the thin-films are presented. Several structure sensitive techniques including atomic force microscopy (AFM), x-ray diffraction (XRD) in T-22 and T-rocking curve measurements as well as low temperature photoluminescence (PL) and scanning electron microscopy (SEM) to examine crystal structure, surface morphology and film thickness where performed and will be presented. [1] S.E. Saddow, M.E. Okhuysen, M.S. Mazzola, M. Dudley, X.R. Huang, W. Huang and M. Shamsuzzoha, Proceedings of the Materials Research Society, Boston, MA, Nov. 1998.

H5.44
IRAS ANALYSIS OF THE EARLY STAGE OF THERMAL OXIDATION ON A SiC SURFACE. Tamotsu Jikimoto, Hidekazu Tsuchida, Isaho Kamata, Kunikazu Izumi, Central Research Institute of Electric Power Industry, Yokosuka Research Laboratory, Kanagawa, JAPAN.

To control the electrical properties of SiO_2 film on SiC, it is important to understand the relationship between the structure of the SiO_2/SiC interface and the electrical properties. In this study, we investigated the early stage of thermal oxidation of the SiC surface using infrared reflection absorption spectroscopy (IRAS). Experiments were carried out in the UHV system with IRAS equipment. The base pressure was below 5 $\times$ 10^{-8} Pa, and the dew point of oxygen used was -108°C. We compared IRAS spectra of oxide film formed on 6H-SiC(0001) and Si(100). The varying thickness of the oxide layer was obtained by adjusting the oxidation time. In the case of oxide films on 6H-SiC(0001), the LO mode ($\approx$ 1250 cm^{-1}) of Si-O-Si stretch vibration is almost constant with increasing oxide thickness from 0.5 nm to 2 nm. On the other hand, the LO mode for the oxide layer on a Si(100) surface became lower with decreasing oxide thickness. These results indicate that there is considerable difference in the optical constant near the interface between a thermally grown oxide layer formed on SiC and one formed on Si.

H5.45
CHEMICAL AND ELECTRICAL ANALYSIS AT THE SILICON DIOXIDE - SILICON CARBIDE INTERFACE. K.C. Chang, L.M. Porter, Carnegie Mellon University, Department of Materials Science and Engineering, Pittsburgh, PA; Q. Wahab, Linköping University, Department of Physics, Linköping, SWEDEN.

The ability to grow stoichiometric SiO_2 on SiC by thermal oxidation is an important advantage for the development of metal-oxide-semiconductor field effect transistors (MOSFETs), which are important devices for high power and high frequency applications. However, high interface state densities are believed to be associated with the low channel mobilities in these devices. Thermal oxides were grown on n-type 6H-SiC(0001) at 1100°C in a wet oxygen ambient for 4 hrs after cleaning the substrates using the complete RCA cleaning process. High carbon concentrations at distinct regions at several thermally-grown SiO_2/6H-SiC(0001) interfaces have been detected by electron energy loss spectroscopy (EELS). The interface state density (D_{it}) in metal-oxide-SiC diodes (with thermally-grown SiO_2) was 7*10^{11} cm^{-2}eV^{-1}. In contrast, carbon rich regions were not detected from EELS analysis of thermally-grown SiO_2/Si interfaces nor of plasma CVD-deposited SiO_2/SiC interfaces. Moreover, layers adjacent to the thermally-grown SiO_2/SiC interface were found to be silicon-rich by EELS. The C-rich regions and the change in stoichiometry may be associated with the higher than desirable interface state densities and the low channel mobilities in SiC-based MOSFETs. Different processing conditions, including chemical and plasma cleaning of the SiC surface, have been investigated. The effect of these conditions on the composition and electrical properties of the interface will also be presented.

SESSION H6: IMPLANTATION/RADIATION DAMAGE

Chairs: Marek Skowronski and Rositza Yakimova
Wednesday Morning, November 29, 2000
Room 202 (Hynes)

8:30 AM *H6.1
ION IMPLANTATION FOR SILICON CARBIDE ELECTRONIC DEVICES. Michael A. Capano, Purdue University, School of Electrical and Computer Engineering, West Lafayette, IN.

As the demands on electronic systems intended for high temperature, high power or high frequency operation increase, silicon-based electronics are being pushed to their fundamental material limits. Consequently, continued improvement in system level performance for these applications requires new semiconductor materials. Silicon carbide (SiC) is a candidate material for the applications listed above, but considerable materials, processing, and device research are still needed. This presentation concentrates on ion implantation processing of SiC, and attempts to illustrate specific problems associated with ion implantation and how they may be solved. Data from a series of experiments relevant to SiC MOSFETs are presented for this purpose. Ion implants into SiC are discussed first to show how a strategy for improving the acceptor activation ratio from less than 1% to nearly 100% is developed. The annealing temperatures (>1600°C) needed to attain high activation ratios lead to severely roughened surfaces. Results from experiments designed to preserve high-quality surfaces have been encouraging from a purely materials perspective. Atomic force microscopy data to be presented will demonstrate low surface roughness following high temperature annealing. However, these solutions have not translated into improved transport characteristics for SiC MOSFETs. An investigation of inversion layer mobility in 4H-SiC MOSFETs will be presented to illustrate this point and close out the talk.

9:00 AM H6.2
STRUCTURAL DEFECTS IN ION IMPLANTED SiC. Per O. Persson, Lars Hultman, Thin Film Physics Division, Dept of Physics, Linköping University, Linköping, SWEDEN.

For the purpose of producing SiC planar devices, selective area doping is necessary. The choice of technique today is mainly ion implantation. The implantation process damages the crystal by inducing vacancies and interstitials from collisions between the implanted ions and the lattice. The as-implanted ions predominantly occupy interstitial lattice sites where they are electrically inactive. To activate these and to restore the implantation induced damage, the sample is subject to thermal annealing. Studies show that annealed SiC samples, irradiated by a dose of ions slightly lower than the amorphisation threshold, contain crystal structural defects. It is the intention of this paper to present results on studies of the evolution of these defects after high temperature annealing. In the present study samples were prepared by implanting 4H SiC with Al, C and Si respectively, at energies ranging from 100-200 keV. Most samples were subject to annealing studies, in which the annealing time and temperature was varied. The samples were studied by EELS, cross sectional and Plan-view TEM. At low temperature implantations, the entire volume affected by the implantation contains dislocation loops. However, after implantation at elevated temperatures only the volume in which the dopant concentration is above a threshold level ($\approx$1e18) contain loops. It was concluded that the dislocation loops contain self-interstitials. These originate from a supersaturation of excess interstitial atoms, which are created in a process where an implanted ion occupy a substitutional site, after having kicked out a native atom and thereby forming a self-interstitial, according to the 1 model. It is shown that when an implanted sample is annealed the excess interstitials start to cluster. As soon as equilibrium between point defects and nucleated loops has been established, coarsening of defects occur according to the Ostwald ripening theory for planar precipitates, with an activation energy of 5.7 eV.

9:15 AM H6.3
MULTI-AXIAL CHANNELING STUDY OF DISORDER IN GOLD IMPLANTED 6H-SiC. W. Jiang, W.J. Weber, S. Thevuthasan, V. Shutthanandan, Pacific Northwest National Laboratory, Richland, WA.

A single-crystal wafer of 6H-SiC has been implanted in different areas with 2.0 MeV Au^2 ions to low fluences of 0.05, 0.1 and 0.2 ions/nm^2 at room temperature. This experimental condition was selected in order to produce low-level disorder, thus avoiding significant lattice strains from occurring in the implanted crystal. The disorder on both the Si and C sublattices has been analyzed using in-situ Rutherford backscattering spectrometry combined with nuclear reaction analysis along $< 0001 >$, $<10\bar{1}1>$ and $<1\bar{1}02>$ axial channeling directions. Depth profiles of the implantation-induced disorder, as measured along the three axes, will be quantitatively compared and possible mechanisms for the different defect concentrations will be suggested. Thermal annealing experiments at 570 K (20 min) for the implanted sample show different recovery rates, as viewed along the different axes. A comparable minimum yield for the Si and C sublattices in both the as-implanted and post-annealed specimen has been observed along $< 0001 >$, while a higher value on the C sublattice has been observed along $<1\bar{1}02>$. In addition, the half widths of the angular profiles around the three axes appear to become smaller as a result of the Au^2 implantation. These results along with detailed analyses will be presented and discussed.

9:30 AM H6.4
DEFECT STRUCTURES IN NEUTRON IRRADIATED 6H-SiC STUDIED BY X-RAY DIFFRACTION LINE PROFILE ANALYSIS. Christoph Seitz, Andreas Magerl, Kristallographie und Strukturphysik, Univ of Erlangen-Nuremberg, Erlangen, GERMANY; Hans Heissenstein, Reinhard Helbig, Angewandte Physik, Univ of Erlangen-Nuremberg, Erlangen, GERMANY.

Nuclear transmutation by neutron irradiation can be applied to dope SiC by phosphorous. This method is useful to achieve a homogeneous doping in large crystal volumes. As a disadvantage, however, radiation induced defects occur, mainly by high energy neutrons. We have investigated in detail the peak shape of several Bragg reflections in irradiated 6H-SiC samples by high resolution x-ray diffraction. The effects of different neutron fluences, neutron spectra and annealing treatments have been studied. A detailed line profile analysis demonstrates a clear correlation of the defect densities of second kind with the neutron fluences and the annealing procedures. We are able to determine quantitatively the defect densities and to elucidate a change of the character of the defects upon annealing. Further qualitative information on crystal damage is obtained from x-ray diffuse scattering and from Bragg scans along the hexagonal crystal axis We find that the pronounced diffuse scattering in irradiated samples becomes largely reduced and that 001 Bragg peaks may be split after high temperature annealing cycles.

9:45 AM H6.5
ELECTRON IRRADIATION OF 4H SiC BY TEM: AN OPTICAL STUDY. S.G. Sridhara, P.O.Å. Persson, J.P. Bergman, E. Janzén, Department of Physics and Measurement Technology, Linköping University, Linköping, SWEDEN; Geraint Evans, J.W. Steeds, Department of Physics, University of Bristol, Bristol, UNITED KINGDOM.

We present an optical study of the defects created by low energy electron irradiation from a TEM, using photoluminescence (PL) and time-resolved measurement techniques. The motivation for this work is to obtain a better understanding of the defect spectra, seen immediately after irradiation and even ion-implantation. Recently, a report [Ref.1: T. Egilsson et. al., Phys. Rev. B **59**, 8008 (1999).] on PL of 4H SiC irradiated with 2MeV electrons, showed multiple series of lines (approx. 12 series) which were proposed to be due to excitons recombining at isoelectronic centers related to silicon vacancies. By using a 200KeV TEM as the irradiation source in our study, we aimed to displace only the atoms in the carbon sublattice. A low doped 4H SiC epilayer was irradiated for 8hrs with the TEM instrument resulting in an electron dose of about 10^{18} cm^{-2}, which is the same dose as was used in ref.1. Low temperature PL measurements show the presence of at least seven series of lines. The luminescence decay times were measured at 2K for all the series of lines and varied from a 0.5 to 625 micro-seconds for the lines identified with transitions from the ground states of the bound excitons and from 0.3 to 0.7 micro-seconds for the lines associated with excited states, in ref.1. Such a long lifetime is indicative of recombination at isoelectronic centers. In addition, the observation of excited states with relatively long lifetimes, indicates a slow relaxation process between the excited states and the ground states. Interestingly, spectral lines in the infra-red, associated with the silicon vacancy are not observed in our epilayer which supports our assumption of displacement of atoms in only the carbon sublattice. Results on epilayers irradiated with different electron energies along with the annealing behavior of these defects will be presented.

10:30 AM H6.6
UNDERSTANDING AND CONTROL OF RADIATION DAMAGE OF 4H AND 6H SiC. John Steeds, Francesca Carosella, Geraint Evans, Mudhahir Ismail, Wolfgang Voegeli, Physics Department, University of Bristol, Bristol, UNITED KINGDOM.

We have used a 300kV transmission electron microscope to carry out small area, voltage controlled, temperature controlled, near-threshold, electron displacement damage of 3C, 4H, 6H and 15R SiC. After irradiation the samples were examined by low temperature photoluminescence microscopy employing 325 nm and 488 nm lasers to arrive at a new understanding of the radiation damage processes that occur in these materials. Studies have included both n and p doped materials, epilayers and substrates from a number of different sources. Carbon displacements have been distinguished from silicon displacements by choice of the accelerating voltage used. At voltages above 180 kV silicon atoms are displaced while carbon atoms are displaced at accelerating voltages down to 90kV. Diffusion of the point defects, created during irradiation, out of the irradiated regions has been measured by photoluminescence imaging using Renishaw micro-Raman systems fitted with Oxford Instruments cryogenic stages. Annealing characteristics have been studied independently for the two different sub-lattice elements. Regions of polytype non-uniformity in 4H and 6H SiC have been mapped out and other inhomogeneities have been identified. Some of the samples studied had been implanted with high energy nitrogen ions and annealed at high temperatures. These exhibited the well-known D_I luminescence. By appropriate subsequent electron irradiation of these implanted samples a procedure has been worked out to eliminate the D_I luminescence.

10:45 AM H6.7
DEFECTS IN 6H-SiC AND 4H-SiC INDUCED BY HIGH ENERGY HELIUM IMPLANTATION. Erwan Oliviero, Marie France Beaufort, Alain Declémy, Jean Franáois Barbot, Laboratoire de Métallurgie Physique, UMR 6630, Futuroscope-Chasseneuil, FRANCE; Esidor Ntsoenzok, Gilbert Blondiaux, CERI CNRS, Orléans, FRANCE.

Convergent Beam Electron Diffraction (CBED), conventional electron diffraction and X-ray diffraction have been used to study the defect formation in crystalline n-type 6H-SiC implanted at room temperature with helium at a dose of $2x10^{16}$ cm^{-2} at 1.6 MeV, following by an annealing at 800°C for 30min. In contrary to what was observed in silicon, the damage layer do not show any bubble formation but consists in a discontinued layer of prismatic loops of 10 nm in diameter. This layer is surrounded by a strong contrasted zone which is impossible to solve using conventional microscopy (TEM). A

run of CBED patterns from the surface toward the bulk along the [0001] direction followed by the analysis of the distortion of the Holz lines contrast show that the perturbed zone is between 3.5 and 4.4 μm. By X-ray diffraction experiments (q,dq), a shoulder is present in the low angle side, which result to the dilatation of about 1% of the c-axis lattice. These results are discussed and compared to the defect formation in crystalline n-type 4H-SiC implanted with helium at a dose of $10^{17}cm^{-2}$ at 1.6 MeV. In that last case a continuous damage layer of 765nm width is observed which can be divided in three different regions. With the central band consisting of an amorphous area and a lot of small bubbles (1-2 nm in diameter). The study is still in progress

11:00 AM H6.8
CHARACTERIZATION AND MODELING OF p-TYPE 6H-SiC IMPLANTED SURFACES. Yu Zeng, Warren Welch, Marvin H. White, Lehigh University, Sherman Fairchild Center, Bethlehem, PA.

In recent years, a considerable amount of work has been performed on Silicon Carbide (SiC) MOS devices; however, much of this work has focused on the characterization of epitaxial SiC layers. Since MOS devices, such as DMOS and IGBTs, employ implanted regions, an understanding of the implanted, p-type, SiC surface is imperative. The purpose of this work is to examine the influence of ion implantation and high-temperature activation anneals on SiC surfaces. Lightly-doped, p-type epitaxial layers on p 6H-SiC substrates have been implanted with aluminum to form shallow, highly doped, p layers, which are annealed at temperatures ranging from 1100C to 1400C. These implanted p layers are characteristic of substrate regions, where inversion channels exist in DMOS and IGBT devices. Reduced temperatures are employed to minimize 'step bunching' on the SiC surface. In order to establish surface equilibrium over a portion of the voltage sweep in capacitance-voltage (C-V) and conductance (G-V) measure-ments, a supply of inversion layer electrons is provided with an implanted N grid. C-V and G-V measurements are used to determine activation percentage and interface trap densities.

11:15 AM H6.9
SELECTIVE DOPING OF 4H-SiC BY ALUMINUM/BORON CO-DIFFUSION. Ying Gao, Stanislav Soloviev, Xiaobin Wang, Vipin Madangarli, Tangali Sudarshan, Univ of South Carolina, Dept of Electrical Engineering, Columbia, SC.

Selective doping plays a significant role in semiconductor device fabrication. Due to the lack of a suitable protective mask for thermal diffusion, selective doping is currently realized by ion implantation followed by high temperature annealing to reduce the lattice damage and obtain reasonable percentage of electrical activation of impurities. However, the inherent drawbacks of ion implantation limit the potential features offered by SiC. Using a high temperature mask developed in our laboratory we have successfully fabricated pn diodes based on selective boron diffusion. The good rectification characteristics confirmed the feasibility of this process except that the forward voltage drop is poor mainly due to the high ionization energy (340 mV) of boron acceptor. On the other hand, Al has lower ionization energy (200meV) and diffusion coefficient compared to B. That is why in this work we have attempted to carry out selective co-diffusion of boron and aluminum in order to form a shallow p^+ layer (Al) and a deep linearly graded p^- layer (B) simultaneously. A vertical double wall water-cooled quartz chamber with inductive heating was used to realize the diffusion process. The diffusion temperature was varied from 1800 to 2100°C. Graphite film was deposited on the sample surface as protection mask to provide selectivity of the doping process. A mixture of elemental boron, aluminum and silicon carbide powder was used as the source of dopants. Cathodoluminescence and photoluminescence measurements were done to identify the local doped regions. Anodic oxidation technique combined with the Hall measurement as well as SIMS were employed to analyze the impurity concentration profiles. The existence of the intrinsic layer due to boron compensation is confirmed. I-V characteristics of the pn diodes based on both only B diffusion and Al/B co-diffusion are compared.

SESSION H7:
METALLIZATION/CHARACTERIZATION
Chairs: Michael A. Capano and Gerhard Pensl
Wednesday Afternoon, November 29, 2000
Room 202 (Hynes)

1:30 PM *H7.1
MECHANISMS FOR OHMIC CONTACT FORMATION TO SILICON CARBIDE. Lisa M. Porter, Taehoon Jang, Carnegie Mellon University, Dept of MS&E, Pittsburgh, PA.

The fabrication of reproducible ohmic contacts with low contact resistivities to p-type SiC is a critical problem for many devices. The traditional approach consists of annealing an Al-based contact (e.g., TiAl) on highly-doped SiC at 900-1000°C. Another approach employs one or more Si layers along with a transition metal to react with the Si and C in the substrate in equal ratios. We have investigated thin ($\sim$100 Å) Si interlayers and metal overlayers with microstructural, chemical and electrical characterizations. Both the structure and resulting chemical phases formed with the metal overlayer depend on the deposition and annealing temperature, and these in turn affect the quality of the ohmic contacts. Because the homogeneity of the interface affects the reproducibility of the contacts, it is important to control the interfacial morphology and the extent of chemical reaction. In this study the deposition temperatures varied from R.T. to 500°C and annealing temperatures from R.T. to 1000°C. The electrical behavior ranged from strongly rectifying to ohmic, while the microstructure ranged from amorphous to crystalline as a function of the deposition and annealing temperatures. The interfacial homogeneity also depended strongly on the processing conditions. The correlations observed among the electrical, microstructural and reaction characteristics will be presented along with the implications for fabricating reproducible ohmic contacts to SiC.

2:00 PM H7.2
TITANIUM TUNGSTEN (TiW) METALS FOR OHMIC CONTACTS TO P-TYPE 4H-SiC. S.-K. Lee, C.-M. Zetterling and M. Ostling, KTH, Royal Institute of Technology, Department of Electronics, Kista, SWEDEN.

Metal-semiconductor contacts have many considerable interests in developing devices for high power, high temperature, and high frequency applications using a wide bandgap silicon carbide. For p-type contacts, very few works have been reported for both Schottky and Ohmic contacts to 4H-SiC. Recently, we have successfully reported and proved that both n- and p-type TiW Schottky contacts had excellent rectifying characteristics after annealing at 500°C with a thermally stable ideality factor of 1.08 and the Schottky barrier height of 1.22 and 1.93 in the range of 24-300°C using IV and CV characteristics (n- and p-type respectively, J. Appl. Phys. vol. 87, p 8039, 2000). In this work, we extensively investigated sputtered titanium tungsten (TiW) contacts for both Schottky and Ohmic contacts to p-type 4H-SiC. We achieved an average contact resistivity(ρ_c) of 4×10^{-5} $\Omega\cdot cm^2$ and sheet resistance (R_s) of 1.35 kΩ/sq. from the linear TLM measurements after 980°C 60s RTA. Epitaxial layers with a doping concentration of 1.3×10^{19} and 6×10^{18} cm^{-3} were used, as well as Al ion implanted samples (700°C implant, 1700°C anneal) with a dose of 3×10^{14} cm^{-2} and an energy of 180keV. We found some variation of the specific contact resistance and the sheet resistance from our TLM measurement. We will discuss this variation behavior with the measurement of SIMS. RBS measurement was also performed to analyze Ti and W composition, thickness of TiW, and reaction at the interface for as-deposited and 980°C annealed contacts.

2:15 PM H7.3
ENGINEERING THE Al-Ti OHMIC CONTACT TO p-SiC FOR OPTIMAL PERFORMANCE. Je-Yi Lin, S.E. Mohney, The Pennsylvania State University, Department of Materials Science and Engineering, University Park, PA; J. Crofton, Murray State University, Department of Physics and Engineering Physics, KY; J.R. Williams, T. Isaacs-Smith, Auburn University, Department of Physics, Auburn, AL.

Al-Ti alloys are widely used as ohmic contacts to p-type SiC. Until our study was performed, however, little was known about the performance of these contacts as a function of composition. We have examined alloy compositions with 90, 70, 60, and 19 weight% Al. Only the compositions with 90 and 70% Al provided ohmic contacts to p-SiC ($p = 7\times10^{18}$ cm^{-3}) after annealing at 1000°C. Interestingly, the Al-Ti phase diagram shows that only the compositions that provided ohmic contacts had Al present as a liquid phase during annealing. The Al present in the more Ti-rich contacts was in high melting point titanium aluminides. Upon removing the annealed contacts with a chemical etchant and examining the exposed SiC surface with scanning electron and atomic force microscopies, we found that the ohmic contacts had non-uniform metal/semiconductor interfaces. On the other hand, the non-ohmic contacts with 60% Al had much smoother interfaces. Explanations for these observations will be presented. From the point of view of reproducibility, we further found that the alloy with 70% Al is the best. Finally, in past work we have observed that the composition of the contact changes during annealing due to evaporation of Al. To slow the evaporation of Al, we have explored the use of a conductive chromium boride cap during annealing. Electrical and materials characterization of the Al-Ti contacts annealed with the caps will also be presented.

2:30 PM H7.4
INVESTIGATION OF FACTORS LIMITING THE HIGH TEMPERATURE STABILITY OF W/WC/TaC/SiC OHMIC CONTACTS TO N-TYPE 6H-SiC. T. Jang and L.M. Porter, Dept of Materials Science and Engineering, Carnegie Mellon University, Pittsburgh, PA; B. Odekirk, 3C Semiconductor Corporation, Portland, OR.

Based on its thermodynamic compatibility and other properties, TaC with one or more metallic overlayers was investigated as a thermally-stable, ohmic contact to n-type 6H-SiC. As expected, high resolution transmission electron microscopy (TEM) analyses revealed no reaction between TaC and SiC after annealing at 1000°C for 15 min. to form an ohmic contact. After annealing at this temperature, the average specific contact resistivity (SCR) of TaC contacts with W/WC overlayers was 6.5×10^{-5} Ωcm^2 on 7.5×10^{18} cm^{-3} doping level. The SCR of these samples remained constant within the experimental error after annealing at 600°C for 1000h. Significant increases in the SCR were not observed until the samples were annealed at 1000°C for a few hundred hours. Electrical measurements were correlated with microstructural and chemical analyses of the W/WC/TaC/SiC contacts to understand the conditions associated with both the stability and degradation. The stability of the contacts at elevated operating temperatures (to 1000°C) was also measured. Changes in the electrical characteristics coincided with decomposition of the WC layer as a result of annealing at 1000°C for 600 h. Investigation of the W/WC/TaC/SiC interface by conventional and high resolution TEM with electron energy loss spectroscopy (EELS) indicated that a reaction between the layers had occurred. Little reaction of the film with the SiC substrate was observed; however, atomic-scale reactions appeared to be concentrated adjacent to grain boundaries in the reacted film. From Auger and SIMS depth profiles, it was also found that incorporation of O (as a function of annealing conditions) affected the electrical properties of the TaC-based contacts. These findings have important implications on the current operating limits for SiC high temperature devices. Distinctions between the two main stability factors will be presented through correlations of the electrical measurements with the reactions and oxygen incorporation in the films.

2:45 PM H7.5
THERMOCHEMICAL CONSIDERATIONS FOR THERMALLY STABLE CONTACT METALLIZATION ON CRYSTALLINE SiC. Robert S. Okojie[1], Dorothy Lukco[2], Carl Salupo[3], David Spry[3], and Jeff Krotine[3]; [1]NASA Glenn Research Center, Instrumentation and Controls Division, Cleveland OH; [2]AYT Corporation; [3]Akima Corporation, Fairview Park, OH.

In high temperature and extreme vibration environments, which are typical in aeronautical propulsion systems, the device contact metallizations undergo irreversible microstructural changes that eventually lead to severe degradation and catastrophic failure. These failure mechanisms include inter-diffusion between different metal layers, contact oxidation, and thermomechanically induced phase transformations. Excellent thermal stability of contact metallization becomes a fundamental requirement. The thrust of this work is to develop an in-depth understanding of thermochemical issues in high temperature contact mettalization schemes being developed at NASA-Glenn. As a result of this effort we have developed a thermally stable Ti (1000Å)/$TaSi_2$ (2000Å)/Pt (3000Å) high temperature metallization on both 4H and 6H-SiC. The diffusion barrier mechanisms allow specific contact resistance values of (10^{-4}-10^{-6}) Ω-cm^{-2} and Schottky barrier heights (SBH) to remain practically constant after heat treatment in air at 600°C for over 500 hours. Scanning electron microscopy (SEM) used to evaluate the surface morphology of the contact metallization revealed a network of two-dimensional oxidation growth patterns as function of time at temperature. Auger electron spectroscopy (AES) enabled identification of three diffusion barrier mechanisms. One is the decomposition of $TaSi_2$ and subsequent outward migration of silicon during annealing at 600°C in nitrogen for 30 minutes, forming a silicide of platinum, which provides critical protection against oxygen transport. The second is the formation of titanium silicide adjacent to the decomposed $TaSi_2$. The third is the formation of quasi-epitaxial titanium carbide as the new interface with silicon carbide after the initial nitrogen anneal, as revealed by High-resolution transmission electron microscopy (HRTEM), similar to that observed in [1]. Theoretical analyses of the thermochemical reactions at both the free surface and the metal/SiC interface indicate that diffusion-limited mechanisms prevail, thereby implying parabolic growth rates. Using the Deal-Grove [2] and Nicolet-Bartur [3] approximations at the free surface and metal/SiC interface respectively, parabolic reaction rates after fifty hours at 600°C for silicide oxidation ($3.19\times10^{-10}cm^2$-s^{-1}, titanium silicide ($4.07\times10^{-15}cm^2$-s^{-1}), and titanium carbide ($1.78\times10^{-20}cm^2$-s^{-1}) formation are obtained. The theoretical model appears to correlate well with experiment. Detailed results will be presented. 1. L.M. Porter and R.F. Davis, J. Mater. Res., 10, No. 3, 668-679 (1995). 2. B.E. Deal and A.S. Grove, J. Appl. Phys., 36, 3770 (1975). 3. M.-A. Nicolet and M. Bartur, J. Vac. Sci. Tech. 19, 786 (1981).

3:30 PM H7.6
A NOVEL DIRECT PULSE LASER DEPOSITED NICKEL SILICIDE OHMIC CONTACT TO n-SiC. M.W. Cole, P.C. Joshi, C.W. Hubbard, E. Ngo, J.D. Demaree, J.K. Hirvonen, M.H. Ervin, M.C. Wood, U.S. Army Research Laboratory, Weapons and Materials Research Directorate, Aberdeen Proving Ground, MD.

SiC is a promising semiconductor material for high power and high temperature device applications. It has been reported that most SiC based electronic devices which can not sustain a long-term operation at an elevated temperature and/or power level suffered deterioration of their metal/SiC contacts. Thus, formation of low resistance Ohmic contacts with good thermal, chemical, and mechanical properties is important for realization of reliable SiC devices. Ni Ohmic contacts to n-SiC are widely used and have been deemed the industry standard due to their reproducible low specific contact resistance. Fabrication of Ni Ohmic contacts requires a post deposition high temperature anneal in order to form Ni_2Si and achieve Ohmic behavior. Unfortunately, the annealing process causes carbon accumulation at the metal-SiC interface and throughout the metallization layer, contact broadening, poor interface morphology laden with Kirkendall voids, and substantial roughening of the contact surface. These features are detrimental to device reliability and will ultimately lead to device failure after exposure to long term high power and high temperature device operational stresses. In order to retain the low specific contact resistance and suppress the undesirable characteristics of Ni Ohmic contacts we have directly deposited Ni_2Si, the thermodynamically stable interface phase between Ni and SiC, onto (0001) 4H n-SiC. The material properties of the as-deposited and annealed Ni_2Si-SiC contacts were quantitatively assessed via AFM, FESEM, AES, RBS, and TEM. The reliability of this contact metallization in response to palpitated high power switching, was assessed via acute pulsed thermal fatigue testing. Our results demonstrated that the as-deposited and 700°C annealed contacts were non-Ohmic, while the 950°C annealed contact exhibited excellent Ohmic behavior. All samples possessed smooth surfaces morphologies and abrupt metal-SiC interfaces. The electrical, compositional and structural integrity of the contact-SiC interface suffered minimal degradation after exposure to pulsed thermal fatigue testing. Details of the aspects of contact formation and the results of the palpitated thermal fatigue testing will be presented and discussed.

3:45 PM H7.7
COMPARISON OF F_2 PLASMA CHEMISTRIES FOR DEEP ETCHING OF SiC. K.P. Lee, Univ of Florida, Dept of MS&E, Gainesville, FL; P. Leerungnawarat, Bell Labs, Lucent Technologies, Reading, PA; S.J. Pearton, Univ of Florida, Dept of MS&E, Gainesville, FL; F. Ren, Univ of Florida, Dept of Chemical Engineering, Gainesville, FL; S.N.G. Chu, Bell Labs, Lucent Technologies, Murray Hill, NJ; C.-M. Zetterling, Royal Institute of Tech (KTH), Dept of Electronics, Kita, SWEDEN. [a]Current address is Lucent Technologies, Reading, PA.

A number of F_2-based plasma chemistries (NF_3, SF_6, PF_5 and BF_3) were investigated for high rate etching of SiC. The most advantageous of these is SF_6, based on the high rate (0.6 μm• min^-1) it achieves and its relatively low cost compared to NF_3. The changes in electrical properties of the near-surface region are relatively minor when the incident ion energy is kept below approximately 75 eV. At a process pressure of 5 mTorr, the SiC etch rate falls-off by ~15 % in 30 μm diameter via holes compared to larger diameter holes ($\geq$60 μm diameter) or open areas on the mask.

4:00 PM H7.8
STRUCTURE AND DYNAMICS OF SILICON CARBIDE SURFACES FROM FIRST PRINCIPLES SIMULATIONS. Giulia Galli, Lawrence Livemore National Laboratory, CA; Alessandra Catellani, MASPEC, Parma, ITALY; F. Gygi, Lawrence Livermore National Laboratory, CA.

Using first principles molecular dynamics, we have studied the structural and electronic properties of cubic SiC(001) surfaces [1-5] at zero and finite temperature. In particular, we have investigated different reconstructions of Si-terminated [2-4] and C-terminated [1,5] SiC(001), focussing on how the presence of stress and defects can influence the surface structure. Furthermore we have studied the deposition of nitrogen on SiC(001), to investigate the early stages of nitride growth on silicon carbide [6], and we have simulated the structural properties of an amorphous silicon carbide surface [7], both at zero and finite temperature. A review of our results will be presented, with focus on the comparison between ab-initio calculations and recent photoemission and STM experiments.

[1] A. Catellani, G. Galli, F. Gygi, Phys. Rev. Lett. 77, 5090 (1996).
[2] A. Catellani, G. Galli, F. Gygi, F. Pellacini, Phys. Rev. B 57, 12255 (1998).
[3] A. Catellani, G. Galli, F. Gygi, Appl. Phys. Lett. 72, 1902 (1998).
[4] L. Pizzagalli, A. Catellani, G. Galli, F. Gygi and A. Baratoff, Phys. Rev. 60, R5129 (1999).
[5] A. Catellani, G. Galli, P.L. Rigolli, Phys. Rev. B (submitted).
[6] G. Galli, A. Catellani and F. Gygi, Phys. Rev. Lett. 83, 2006 (1999).
[7] G. Galli, F. Gygi and A. Catellani, Phys. Rev. Lett. 82, 3476 (1999).

4:15 PM H7.9
OPTICAL ANISOTROPY OF THE SiC(001) SURFACE: EVIDENCE FOR THE TWO-ADLAYER ASYMMETRIC-DIMER MODEL. Wenchang Lu, E.L. Briggs, and J. Bernholc, North Carolina State University, Dept of Physics, Raleigh, NC; W.G. Schmidt, Institut für Festkörpertheorie und Theoretische Optik, Friedrich-Schiller-Universität, Jena, GERMANY.

Much attention has recently been focused on the properties of SiC growth planes, for both fundamental reasons and due to their technological importance. The β-SiC(001) surface, exhibiting three major surface phases, $c(2\times2)$, (2×1), and (3×2), serves as a prototype in that respect. It has been intensively investigated by both experiment and theory. However, despite considerable efforts, the atomic structures of these surface phases are still not clear. This holds in particular for the Si-rich (3×2) reconstruction, which results from Si adsorption on the Si-terminated SiC substrate. To our knowledge no less than four reconstruction models have been suggested, namely the single dimer row model (SDRM), the alternate dimer row model (ADRM), the double dimer row model (DDRM), and the two-adlayer asymmetric dimer model (TAADM). First-principles calculations of the energetics of this surface give contradicting results and no experiment thus far could either prove or disprove any of the above models. The present work aims at resolving these controversies by computing the reflectance anisotropy spectra from first principles and comparing the calculated results with experimental data. All of the four candidate models were considered. The results for the TAADM give two main peaks and one dip in the experimental energy window, which is in very good agreement with experimental data. The other three models, SDRM, ADRM, and DDRM, lead to negative features in the anisotropy spectra that are not observed in experiments. The surface structures that dominate the optical anisotropy signal have been identified in each case, providing a detailed picture of the origin of optical anisotropy for this surface. The present results show that a combination of optical anisotropy measurements and calculations can be used to determine the atomic reconstruction patterns for complex, severely reconstructed surfaces.

4:30 PM H7.10
BEHAVIOUR OF ALUMINIUM AND NITROGEN IN COMPENSATED 4H-SiC EPITAXIAL LAYERS. M. Syväjärvi, R. Yakimova, A. Henry, A. Kakanakova-Georgieva, M. Linnarsson, E. Janzèn.

Silicon carbide (SiC) is a recognized wide bandgap semiconductor for high-power, high-frequency and high-temperature electronics. For p-type layers aluminium is used as dopant since it gives a shallow acceptor level. In growth of n-type layers aluminium may be unintentionally introduced from the growth environment. Nitrogen is always present to some extent and creates a shallow donor level. Compensation makes the property control more complicated. We have studied epilayers containing aluminium and nitrogen. The aluminium concentration was in the range 1E15 to 1E18 atoms/cm^3 and nitrogen was in E16 order. Impurity concentrations were determined by secondary ion mass spectroscopy. Electrical, low-temperature photoluminescence, and cathodoluminescence techniques have been used for studying the epilayers. The samples were grown by sublimation epitaxy with growth rates from 50 to 100 μm/h in the temperature range of 1750 to 1800°C. We report a comparative study on the influence of compensation on luminescence of bound excitons and Al-N donor-acceptor pairs in n- and p-type 4H-SiC. In photoluminescence measurements the luminescence from nitrogen bound excitons is sensitive to the aluminium concentration in the epilayers. The intensity of nitrogen bound excitons decreases with increasing aluminium concentration while the intensity of aluminium bound excitons increases. The ratio of the N bound exciton zero phonon lines to the aluminium bound exciton lines shows a proportional dependence to the aluminium concentration. This is more clear in n-type samples. The compensation level was evaluated from C-V measurements and knowledge of acceptor and donor concentrations. Cathodoluminescence was used to analyze donor-acceptor pair emission around 420 nm which is commonly related to the presence of aluminium and nitrogen in SiC. An effect of compensation on the optical properties of 4H-SiC epilayers is demonstrated. The results from the characterization techniques are combined for further understanding the complex interplay of aluminium, nitrogen and boron in compensated material.

4:45 PM H7.11
DEEP-LEVEL LUMINESCENCE AT 1.0 eV IN 6H SiC.
B. Magnusson, A. Ellison, N.T. Son, and E. Janzén, Department of Physics and Measurement Technology, Linköping University, Linköping, SWEDEN.

We have studied the infrared luminescence around 1.0 eV from an unidentified defect center, which we label UD-1, found in our as-grown high-temperature CVD 6H SiC samples. The grown material is transparent and usually has high resistivity, even when it is not intentionally doped with vanadium. The UD-1 luminescence has a similar intensity as the vanadium-related luminescence at 0.75-0.95 eV. Some other sharp luminescence lines (UD-2 at 1.1 eV, UD-3 at 1.35 eV) are usually also observed in the infrared region but not so strong as the UD-1 and vanadium. We tentatively ascribe the high resistivity of the material as due to the UD-1 defect.
The luminescence of the UD-1 consists of three sharp no-phonon lines at 0.994, 1.000 and 1.001 eV. The line width is less than 0.5 meV. In this report we will present the optical properties in more detail together with the electronic structure of the center. The results are to a large extent based on Zeeman measurements in the range from 0 to 5 T and on photoluminescence (PL) measurements using below bandgap excitation. The measurements allow us to make a rough estimate of the ground-state level of the center in the bandgap by varying the excitation energy.
The UD-1 center is never observed in our systematic annealing studies of electron irradiated pure CVD layers. However in commercial substrates the UD-1 center is present before but not after irradiation unless the substrates are annealed (>750°C). This behavior suggests that the UD-1 center is related to impurities rather than to intrinsic defects.