SYMPOSIUM A

Materials Issues in Novel Si-Based Technology

November 26 – 28, 2001

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* Invited paper

SESSION A1: GROUP IV ALLOY AND STRAINED MATERIALS AND DEVICES
Chair: James C. Sturm
Monday Morning, November 26, 2001
Room 202 (Hynes)

8:30 AM *A1.1
STRAINED SILICON/SILICON GERMANIUM MATERIALS AND DEVICES. Judy L. Hoyt, Microsystems Technology Laboratory, Dept. of EECS, Massachusetts Institute of Technology, Cambridge, MA.

MOSFETs fabricated on tensile strained Si layers grown on relaxed SiGe exhibit significant enhancements in electron and hole mobility, and current drive, at a given channel length. Such devices are promising candidates as a means of extending the performance limits of silicon MOSFET technology, for both digital and analog applications. However, challenging materials and process integration issues remain, including those associated with the relaxed SiGe layer itself. Several groups have recently pursued the formation of relaxed SiGe on insulator, which has the potential to provide all the device advantages associated with silicon on insulator (e.g. reduced capacitance), while simultaneously improving integration issues associated with the thick relaxed SiGe layer. Simplified device isolation and reduced junction leakage currents are expected for strained Si MOSFETs fabricated on relaxed SiGe on insulator. After a brief review of strained Si MOSFETs, the formation of relaxed SiGe on insulator by bonding and H delamination, and etch back techniques will be discussed. Preliminary results indicate that the electron mobility in strained Si MOSFETs fabricated on such material matches that obtained for devices fabricated on thick relaxed SiGe layers. Key device processing issues associated with strained Si MOSFETs, such as the diffusion of dopants in relaxed SiGe structures, and silicide formation will also be discussed.

9:00 AM A1.2
THERMAL STABILITY OF STRAINED Si ON RELAXED $Si_{1-x}Ge_x$ BUFFER LAYERS. P.M. Mooney, S.J. Koester, J.A. Ott, J.O. Chu, and J.L. Jordan-Sweet, IBM Research Division, T.J. Watson Research Center, Yorktown Heights, NY.

Strained Si/SiGe is of interest for future generations of CMOS technology, since both electron and hole mobility is enhanced in Si under biaxial tensile strain. The thermal stability of strained Si layers grown epitaxially on relaxed SiGe buffer layers was investigated using high resolution x-ray diffraction, microRaman spectroscopy and planar view transmission electron microscopy (TEM). The samples, consisting of step-graded relaxed $Si_{1-x}Ge_x$ buffer layers, where $0.19<x<0.30$, with a strained Si cap layer 10-30 nm-thick, were grown on Si(001) by UHV/CVD at temperatures in the range 500-550°C. They were subsequently annealed at 1000°C for times as long as 300 sec. The x-ray measurements were performed at beamline X20 at NSLS* using a triple-axis configuration with an 8 keV incident beam. The large dynamic range of the synchrotron enabled the diffraction peak of the strained Si cap layer to be observed in addition to the relaxed SiGe buffer layer peaks. MicroRaman spectra taken using 488 nm incident radiation show a strong peak corresponding to the relaxed SiGe buffer layer and a less intense peak (or shoulder at low x) corresponding to the strained Si cap layer. Both the x-ray and microRaman measurements show that the thickness of the strained Si cap layer decreases with increasing annealing time, a result that we attribute to interdiffusion at the Si/SiGe interface. However, no significant relaxation of the strain in the Si cap layer was detected by either method. This latter result is confirmed by TEM which shows a negligible misfit dislocation density at the Si/SiGe interface after annealing. *The National Synchrotron Light Source at Brookhaven National Laboratory is supported by the US Department of Energy, Division of Materials Sciences and Division of Chemical Sciences.

9:15 AM *A1.3
STRAINED-Si-ON-INSULATOR (STRAINED-SOI) MOSFETS - CONCEPT, STRUCTURES AND DEVICE CHARACTERISTICS. Shin-ichi Takagi, Tsutomu Tezuka, Tomohisa Mizuno, Naoharu Sugiyama, Atushi Kurobe, Advanced LSI Technology Laboratory, Toshiba Corp, Kawasaki, JAPAN.

Attention is being paid to MOSFETs with high mobility channel, in order to relax several fundamental limitations of CMOS scaling. Strained-Si CMOS is an attractive device structure among them, because of high electron and hole mobility and compatibility with Si CMOS processing. This paper proposes a new device structure using the strained-Si channel, strained-Si-on-Insulator (strained-SOI) MOSFET, applicable to sub-100 nm Si CMOS technology nodes. This device includes thin strained-Si/relaxed SiGe layers formed on buried oxides. The device structure and the advantages of strained-SOI MOSFETs and strained-SOI CMOS are presented. The combination of the SIMOX technology and re-growth technique of strained Si films realizes this device structure. It is demonstrated that strained-SOI n- and p-MOSFETs with Ge content of 10-13% have mobility of 1.6 and 1.3 times as high as the universal mobility, respectively. Furthermore, we also propose a novel technique to fabricate ultra-thin SiGe-on-Insulator (SGOI) virtual substrates with higher Ge content, which is mandatory to realize fully-depleted SOI MOSFETs with higher mobility. This fabrication technique is based on the enrichment of Ge content in SiGe films by oxidizing SGOI substrate with lower Ge content or SOI substrates with SiGe top layer. The rejection of Ge atoms from oxidized layer into remaining SiGe films and the block against Ge diffusion into Si substrate by buried oxide enable to realize ultrathin SGOI films with higher Ge content. A 10 nm-order SGOI substrate with Ge content larger than 50% are successfully fabricated by this technique. Using this substrate, strained-SOI structure with total SOI thickness of 21 nm, which is applicable to sub-100 nm fully-depleted strained-SOI CMOS, is accomplished.

9:45 AM A1.4
FOURIER-TRANSFORM INFRARED INVESTIGATIONS OF $Si_{1-y}C_y$ STRUCTURES FOR HBT APPLICATIONS. D. Gruber, M. Mühlberger, T. Fromherz, F. Schäffler, Inst. Halbleiterphysik, Univ Linz, AUSTRIA; M. Schatzmayr, Austria Mikrosysteme Int., Unterpremstätten, AUSTRIA.

With the rapid proliferation of commercial SiGe HBT (hetero bipolar transistor) devices, incompatibilities with mainstream integration technologies become an important issue. A common problem in device processing is transient enhanced diffusion (TED) of boron out of the base region due to poly-emitter implantation and annealing. It has been shown that co-doping of the $Si_{1-x}Ge_x$ base with C can very efficiently suppress TED of B. This is mainly caused by the much more efficient TED of C, which oversaturates the interstitial diffusion paths for B. Hence, C co-doping leads inherently to a broad C distribution throughout the active device. Moreover, the required C concentrations are beyond the solid solubility of C in Si, and are thus metastable against SiC formation. It is therefore essential to characterize the structural and electronic behavior of C co-doping under realistic process conditions. For this purpose we combined Fourier Transform Infrared spectroscopy (FTIR), x-ray diffraction and SIMS experiments to investigated in which form C is present after thermal treatment of $Si_{1-y}C_y$ layers with and without ion-implanted poly-Si emitter. The FTIR technique is sensitive to substitutional C, coherent and incoherent SiC precipitates and some C-containing complexes via their characteristic local vibration modes. With this technique we followed the evolution of SiC precipitate formation upon annealing at typical process temperatures between 750 and 1050°C, and correlated these results with strain relaxation in the $Si_{1-y}C_y$ layers. The results suggest that low thermal budgets are an essential precondition for employing C containing epitaxial layers in device structures.

10:30 AM A1.5
SILICON-GERMANIUM ON INSULATOR (SGOI). Zhi-Yuan Cheng, Matthew T. Currie, Chris W. Leitz, Gianni Taraschi, Arthur Pitera, Minjoo L. Lee, Thomas A. Langdo, Judy L. Hoyt[a], Dimitri. A. Antoniadis[a], Eugene A. Fitzgerald, MIT, Department of Materials Science and Engineering, Cambridge, MA; [a]MIT, Department of Electrical Engineering and Computer Science, Cambridge, MA.

Relaxed SiGe-on-insulator (SGOI) is a very promising technology as it combines the benefits of two advanced technologies: the conventional SOI technology and the disruptive SiGe technology. The SOI configuration offers various advantages associated with the insulating substrate, namely reduced parasitic capacitances, improved isolation, reduced short-channel-effect, etc. High mobility strained-Si or strained-SiGe or strained-Ge MOS devices can be made on SGOI substrates. Other III-V optoelectronic devices can also be integrated into the SGOI substrate by matching the lattice constants of III-V materials and the relaxed SiGe. SGOI may serve as an ultimate platform for high speed, low power electronic and optoelectronic applications. We have fabricated high quality SGOI substrates and demonstrated high mobility enhancement in strained-Si MOSFET's fabricated on relaxed SGOI substrates with a high Ge content of 25%. The substrates were fabricated by wafer bonding. The initial relaxed SiGe layers were grown on Si donor substrates by a graded epitaxial growth technology using UHVCVD. Two different bonding approaches were investigated: SiGe-handle wafer direct bonding and SiGe/oxide-handle wafer bonding. Two different ways to thin down the bonded pair were developed: etch-back utilizing a 20% Ge layer as a natural etch stop and "smart-cut" process using hydrogen implantation. Bonding conditions were optimized for strong bond energy. The resultant SiGe film quality was compared among the different approaches. Large-area strained-Si MOSFET's were then fabricated on the SGOI substrates. Epitaxial regrowth was used to produce the upper portion of the relaxed SiGe and the surface strained Si layer. The measured electron mobility shows significant enhancement over both the universal mobility and that of co-processed bulk-Si MOSFET's. This SGOI process has a low thermal budget and thus is compatible with a wide range of Ge contents in SiGe layer.

10:45 AM A1.6
RELAXATION PHENOMENA IN $Si_{1-x}Ge_x$- BUFFER LAYERS ON Si(001) BY He^+ ION IMPLANTATION. S.H. Christiansen, P.M. Mooney, J.O. Chu, A. Grill, IBM Research Division, T.J. Watson Research Center, Yorktown Heights, NY.

Transmission electron microscopy (TEM) in planar view and cross section and x-ray diffraction have been applied to study the relaxation characteristics of relaxed (>80%) thin (≈100nm) SiGe buffer layers with a Ge content of 15%. The relaxed buffer layers have been obtained through a 3-step process: I) a pseudomorphic SiGe layer was deposited on a Si(001) substrate using ultra high vacuum chemical vapor deposition (UHVCVD); II) He^+ was implanted into the substrate; III) the sample was annealed at elevated temperatures. As a result of this process, 3-dimensional defects that act as internal interfaces for dislocation half-loop nucleation are formed. The different defects have been evaluated with regard to their shape, size and spacing and their potential for dislocation nucleation. It was found that the dislocation half-loops glide towards the layer/substrate interface where they deposit 60°-misfit dislocation segments along the < 110 > directions and thereby govern the relaxation of the strained SiGe layer. Various dislocation reactions have been evaluated and some were found to differ from those observed in the commonly used step graded buffer layers. We found the formation of non-glissile 90° < 110 > dislocations from two close, nearly parallel 60° misfit dislocations. These have previously not been reported in SiGe/Si. Dislocation blocking at bundles of dislocations that frequently occurs in step graded buffer layers was observed only rarely. On the other hand, we frequently observed dislocation splitting reactions that occur when intersecting dislocations have parallel Burgers vectors. The different relaxation mechanisms in step-graded and implanted buffer layers are discussed.

11:00 AM A1.7
BEHAVIOR OF ION-IMPLANTED N-TYPE DOPANTS IN SILICON GERMANIUM. Satoshi Eguchi, Judy L. Hoyt, Massachusetts Institute of Technology, Microsystems Technology Lab, Cambridge, MA; Christopher W. Leitz, Eugene A. Fitzgerald, Massachusetts Institute of Technology, Dept of Materials Science and Engineering, Cambridge, MA.

An understanding of the behavior of ion implanted n-type dopants in SiGe is essential for the development of novel silicon-based technologies, such as strained Si on relaxed SiGe CMOS. In this work, the diffusivities of ion-implanted n-type dopants, phosphorus and arsenic are observed to be enhanced in relaxed $Si_{0.8}Ge_{0.2}$ compared to Si, in contrast to the diffusion of boron, which is known to be retarded in SiGe relative to diffusion in Si. We discuss the effective diffusivities of phosphorus and arsenic under long time annealing conditions. We also report arsenic diffusion under transient conditions in SiGe, and compare to diffusion measured in similarly processed Si samples. SIMS data is compared to TSUPREM-4 simulations. Simulation profiles are calculated using the interface trap model, which is required to account for the observed pile-up of dopant at the oxide/Si and oxide/SiGe interface. Under long-time annealing conditions, the extracted effective diffusivity enhancement factor (measured relative to the extracted dopant diffusivity in silicon) for phosphorus is about three, while the effective diffusivity enhancement factor for arsenic is roughly 10. The diffusivity of arsenic in SiGe is enhanced more than that of phosphorus in SiGe. However, the absolute diffusivity value of phosphorus is still roughly 4 times higher than that of arsenic in SiGe. Under transient annealing conditions at 900°C, arsenic diffusion in SiGe is comparable to that in Si, suggesting that using arsenic, short-time annealing may be used to obtain similar junction depths in ion implanted Si and SiGe.

11:15 AM A1.8
ELECTRICAL PROPERTIES OF $Si_{1-y}C_y$ FILMS GROWN BY PLASMA-CVD AT A LOW SUBSTRATE TEMPERATURE. Shuhei Yagi, Katsuya Abe, Takashi Okabayashi, Akira Yamada, Makoto Konagai, Tokyo Inst of Tech, Dept of Physical Electronics, Tokyo, JAPAN.

We have successfully grown $Si_{1-y}C_y$ films and widely investigated on their electrical properties. Epitaxial $Si_{1-y}C_y$ films were grown on Si(001) by the plasma-CVD using a gas mixture of SiH_4, H_2 and $SiH_2(CH_3)_3$. PH_3 was used as doping gas. The substrate temperature and the growth pressure were maintained at 210°C and 0.5 Torr, respectively. The n-type $Si_{1-y}C_y$ films were obtained and electron concentration could be linearly controlled up to 1×10^{19} cm^{-3} by varying the doping ratio of PH_3/SiH_4. In the as-grown films, the electron concentration of C-added film (C 1%) was the half value of the Si film at the same doping ratio (PH_3/SiH_4), while the values were almost one order of magnitude lower than that of the Si film when the C concentration was higher than 1%. On the other hand, after annealing at 700°C, the electron concentration of both Si and $Si_{0.99}C_{0.01}$ showed the same value. However, the values of the $Si_{1-y}C_y$ films whose C concentration was higher than 1% were still one order of magnitude smaller than that of Si film. In our previous work, we found that almost all C atoms located at the Si substitutional site in the annealed sample with total C composition of lower than 1% at the annealing temperature of 700°C. On the contrary, the interstitial C content was increased with increasing the total C composition higher than 1% after annealing. Thus, the behavior of the electron concentration following annealing could be explained as follows: The interstitial C atoms form the defect complex with P atoms and suppress the dopant activation, resulting in the reduction of the electron concentration.

11:30 AM A1.9
STRAINED-GERMANIUM CHANNEL *p*-TYPE MOSFETS FABRICATED ON $Si_{1-x}Ge_x$/Si VIRTUAL SUBSTRATES. Minjoo L. Lee, Christopher Leitz, Arthur Pitera, Gianni Taraschi, Eugene Fitzgerald, MIT, Dept of Materials Science and Engineering, Cambridge, MA; Dimitri Antoniadis, MIT, Dept of Electrical Engineering and Computer Science, Cambridge, MA.

Low defect density relaxed SiGe alloys on Si have created a new platform for high mobility electronic devices as well as integration of optoelectronics on Si. Strained silicon *n*- and *p*-type MOSFETs on relaxed $Si_{1-x}Ge_x$/Si virtual substrates exhibit mobility enhancements of 1.25 to 2 times that of bulk devices. But just as in bulk Si, the *p*-MOS mobility lags the *n*-MOS considerably. Compressively strained $Si_{1-y}Ge_y$ channels on $Si_{1-x}Ge_x$ (y>x) have thus been used to attain even higher hole mobilities. However, the highest hole mobility should be realized with a compressively strained, pure germanium channel due to reduced intervalley scattering and the lack of alloy scattering. Strained-Ge layers on $Si_{1-x}Ge_x$ have previously been used to fabricate high mobility and high transconductance MODFETs, but all of these devices utilized Schottky gates. Germanium oxide's hygroscopic nature and the high interface state density which results when SiO_2 is deposited onto Ge surfaces have historically prevented the development of germanium MOS technology. To circumvent this, the Ge channel in our devices is capped with a thin epitaxial silicon layer. Despite the lattice mismatch of over 2.8% and great relaxation, our optimized growth process yields a top Si layer with fully planar morphology. This Si layer protects the Ge-rich heterostructure from standard etching processes and also provides a high quality interface with the gate SiO_2. Our Ge MOSFETs show a mobility enhancement of more than 7 times that of coprocessed bulk Si devices with a peak effective mobility of 1160 cm^2/V-s. At sufficiently high vertical fields, the top Si layer was shown to conduct as a parallel hole channel, resulting in slightly degraded mobility enhancement. But since the compressive Ge channel strongly confines holes, minimizing the top Si thickness allowed the mobility enhancement to be maintained at fields as high as 0.6 MV/cm.

SESSION A2: ADVANCED CMOS: SOI AND VERTICAL DEVICES
Chair: Erin C. Jones
Monday Afternoon, November 26, 2001
Room 202 (Hynes)

1:30 PM *A2.1
PROCESS CHALLENGES FOR FUTURE SOI CMOS DEVICES. Scott Crowder, Semiconductor Research & Development Center, IBM, Hopewell Junction, NY.

There are several important technical challenges to overcome in the fabrication of future SOI CMOS transistors. This talk will focus on the processing issues related to scaling today's SOI transistors into the 0.07 micrometer generation and beyond. Topics will include the challenges in reducing silicon film thickness, creating trench isolation in SOI, integrating DRAM into SOI logic and building novel devices that offer advantages over the current device structure.

2:00 PM *A2.2
MATERIALS REQUIREMENTS FOR FUTURE THIN-BODY SOI CMOSFETS. Tsu-Jae King, Department of Electrical Engineering and Computer Sciences, University of California at Berkeley, Berkeley, CA.

As the MOSFET is scaled down to gate lengths below 30nm to achieve continued improvements in cost and performance, alternative transistor structures such as thin-body FETs will eventually be needed in order to adequately control sub-threshold leakage current and short-channel effects. Existing technological challenges for single-gate and double-gate fully-depleted SOI CMOS transistors must be overcome before they can be used in the manufacture of high-density integrated circuits, however. This paper will describe the materials requirements for control and enhancement of thin-body SOI FET performance in future CMOS technologies.

2:30 PM A2.3
THE STUDY ON THE FORMATION OF THIN SOI STRUCTURE BY SIMOX WITH WATER PLASMA. Jing Chen, Meng Chen, Xiang Wang, Yemin Dong, Zhihong Zheng, Xi Wang, Ion Beam Laboratory, Shanghai Institute of Metallurgy, Chinese Academy of Sciences, CHINA.

The biggest drawback of the widely application of SOI material is high cost which mainly due to the long implantation time by conventional beamline implanter. An implanter without ion mass analyzer is used to fabricate SOI materials by water ions implantation using water plasma based on the consideration that the masses of the three ions of H_2O^+, HO^+ and O^+ are quite close, their depth profiles in as-implanted wafers will not disperse much, that makes it possible for the formation of single buried oxide layer by choosing appropriate implantation energy and dose. The process provides shorter implantation time, lower cost and preferential potential for large size wafers. Single crystal silicon wafer was implanted with 50-90 keV water ions (H_2O^+, HO^+, and O^+) at the dose ranged from 1×10^{17} to 7×10^{17} cm^{-2} at 680°C. Capped with 500 nm SiO_2 layers by LPCVD, the samples were annealed over 1300°C for 5 hours in a flowing 99%Ar 0.5%O_2 ambient. The structure of as-implanted and annealed samples was investigated by XTEM, HRTEM, SIMS, and RBS, respectively. The results show that it exits a dose window at fixed implantation energy to form desirable thin or even ultra-thin SOI structure with the buried oxide layer free of silicon islands and smooth interfaces. Compared to conventional SIMOX fabrications, the samples implanted at the same dose and energy have thicker BOX layers, which may be caused by the hydrogen-induced defects, for there are two hydrogen enrichment peaks around both sides of the projected range (R_p) of oxygen in the as-implanted wafers by SIMS measurements. The hydrogen effect in the formation process will be discussed.

2:45 PM A2.4
A PATTERNED SOI BY MASKED ANNEAL FOR SYSTEM-ON-CHIP APPLICATIONS. G.M. Cohen and D.K. Sadana, IBM T.J. Watson Research Center, Yorktown Heights, NY.

System on a chip (SoC) requires the integration of logic and memory circuits on the same chip. While for logic circuits the driving force is primarily speed, for memories, and in particular dynamic random access memories (DRAM), it is the circuit density. Logic circuits implemented with silicon-on-insulator (SOI) technology exhibit a significant improvement in the device speed due to the reduction in the junction capacitance. High density DRAM is built using deep trench capacitors, which are not compatible with SOI technology, and are implemented with conventional bulk Si wafers. Combining logic and memory on the same chip would therefore require a mixed SOI and bulk Si wafer technology.
In a recent work [R. Hannon, et. al, 2000 Symposium on VLSI Technology, p. 66, 2000] a 64 MB DRAM and logic circuits were integrated on a patterned SOI wafer which was fabricated by the patterned SIMOX (separation by implantation of oxygen) process. In the case where a high dose of oxygen was used a considerable amount of defects were observed near the mask edge. The defect density was reduced, but not completely eliminated, even by lowering the oxygen dose and forming a thinner BOX.
We present an alternative method to reduce the defects at the SOI-bulk boundary in a patterned SOI. The fabrication steps consist of: a blanket oxygen implant, deposition and patterning of a hard mask followed by high temperature annealing in an inert ambient mixed with oxygen. The internal thermal oxidation (ITOX) during annealing plays an important role in the BOX formation. A patterned SOI structure is created when the implanted oxygen dose is low enough such that the BOX forms only where ITOX occurs, (i.e., in an open mask region where the oxygen supply from the ambient is not blocked by the hard mask) and no BOX forms under the mask region where no ITOX occurs. When the implanted dose is high the patterned SOI contains a thick BOX under the unmasked region and thin BOX under the masked region.

3:30 PM *A2.5
INTEGRATION CHALLENGES FOR DOUBLE-GATE MOSFET TECHNOLOGIES. Witek P. Maszara, AMD, Sunnyvale, CA.

Device modeling data and some early experiments suggests that fully-depleted MOSFET devices where channel is controlled by two opposing gates or one gate that surrounds most or the entire channel, will provide better scaling than the classic devices with one gate on one side of the channel. However, formation of such devices requires complex, non-conventional and sometimes exotic geometry and processing, ranging from wafer bonding to selective lateral "tunnel" epitaxy, to selectively wet-etched channels with triangular cross-section. Classic single-gate transistors have been recently demonstrated with reasonable performance at 20 nm of physical gate length. Double-gate transistors with their process integration complexity will likely become a viable alternative for smaller geometries. This paper will discuss various approaches to realization of those multi-gate fully-depleted devices and their process integration challenges for sub-20 nm gates.

4:00 PM A2.6
WAFER BONDING OF DIAMOND FILMS TO SILICON FOR SILICON-ON-INSULATOR TECHNOLOGY. Gleb N. Yushin, Scott D. Walter, Alex Kvit, Zlatko Sitar, North Carolina State Univ, Dept of Material Science, Raleigh, NC; John T. Prater, Army Research Office, Research Triangle Park, NC; B.R. Stoner, MCNC, Material and Electronic Technologies Division, Research Triangle Park, NC.

At present, the fabrication of silicon-on-insulator (SOI) devices by wafer bonding (WB) is a well established procedure. WB offers reduced defects in the SOI layer, which leads to better electrical characteristics. Conventional SOI technique employs silicon dioxide as a buried insulator. However its low thermal conductivity limits the performance of the high power devices due to the resulting self-heating. Diamond is considered to be a promising material as a buried insulator due to its high thermal conductivity combined with low resistivity and high breakdown electrical field. A study of hydrophobic and hydrophilic WB of diamond films to silicon was performed. Polycrystalline diamond films polished to an RMS roughness of 15 nm were bonded to (100) silicon in a dedicated ultrahigh vacuum bonding chamber. Bonding under a uniaxial mechanical stress of 32 MPa was observed at temperatures as low as 950°C. The bonded interface was examined by plane-view infrared and acoustic imaging techniques. The results indicated that bonding across the whole wafer area could be achieved at temperatures above 1150°C for both hydrophilic and hydrophobic type of bonding. This paper will discuss in detail process parameters and results of different characterizations, including interfacial studies of the bonded interface by cross-sectional transmission electron microscopy.

4:15 PM *A2.7
THE VERTICAL REPLACEMENT-GATE (VRG) MOSFET: A HIGH-PERFORMANCE VERTICAL MOSFET WITH LITHOGRAPHY-INDEPENDENT CRITICAL DIMENSIONS. J.M. Hergenrother, Sang-Hyun Oh, T. Nigam, D. Monroe, F.P. Klemens, A. Kornblit, Agere Systems, Murray Hill, NJ.

We have demonstrated the Vertical Replacement-Gate (VRG) MOSFET, the first MOSFET ever built in which 1) all critical transistor dimensions are controlled precisely without lithography, 2) the gate length is defined by a deposited film thickness, independently of lithography and etch, and 3) a high-quality gate oxide is grown on a single-crystal Si channel. In addition to this unique combination, the VRG-MOSFET includes self-aligned source/drain extensions formed by solid source diffusion (SSD), small parasitic capacitances, and a replacement-gate approach to enable alternative gate stacks. All of this is achieved using current manufacturing methods and tools, and high-performance devices with 50 nm gate lengths have been demonstrated with precise gate length control without advanced lithography. In the VRG process, a stack containing a sacrificial gate layer sandwiched by two dopant source layers is deposited. A trench is etched through this stack and it is filled with single-crystal Si to form the device body. Shallow, self-aligned source/drain extensions are formed by SSD from the dopant sources. The sacrificial gate layer is removed, a gate oxide is grown on the exposed Si, and the gate is deposited in place of the sacrificial layer. This replacement-gate approach allows for the fabrication of high-quality gate oxides on a vertical {100} Si surface whose length is defined by a film thickness. This flow is mechanically scalable to sub-30 nm gate lengths with excellent control. Since both sides of the device drive in parallel, the VRG drive current can far exceed that of advanced planar MOSFETs. Our 100 nm VRG-pMOSFETs with 25 Å gate oxides drive 80% more current than specified in the 1999 ITRS Roadmap. Our 50 nm VRG-pMOSFETs with 25 Å gate oxides approach the 1.0 V roadmap drive current target of 350 $\mu A/\mu m$ without the need for a hyperthin (< 20 Å) gate oxide.

4:45 PM A2.8
ENHANCED MOBILITY IN 100 NM STRAINED SiGe VERTICAL P-MOSFETS FABRICATED BY UHVCVD. Sanjay Banerjee, Sankaran Jayanarayanan, Freek Prins, Xiangdong Chen, University of Texas, Austin, TX.

Recently, strained silicon-germanium MOSFETs are receiving considerable attention due to the enhancement of in-plane hole mobility, as well as out-of-plane electron and hole mobilities over conventional silicon MOSFETs. In the direction normal to the growth plane of strained SiGe, both electron and hole mobilities are improved from predictions of theoretical bandstructure calculations. Strained SiGe vertical PMOSFETs have been fabricated with a channel length of 100 nm without sophisticated lithography and the whole process is compatible with a regular CMOS process. The SiGe source, channel and drain layers were grown by ultrahigh vacuum chemical vapor

deposition (UHVCVD) at 500°C using Si_2H_6 and GeH_4. PH_3 and B_2H_6 were used for in situ doping. X-ray diffraction (XRD) rocking curves of the Si (004) plane demonstrate that the SiGe layers do result in compressive strain. The germanium profile, with a mole-fraction of about 15%, is uniform over the entire device. Atomic force microscopy (AFM) of the SiGe and silicon sample surfaces shows the RMS roughness to be 0.18 nm. Reactive ion etch was used to define the mesa of the vertical MOSFET. A 10 nm silicon cap layer was grown by UHVCVD before growing a 4 nm gate oxide by wet oxidation at 750°C. The drive current for the vertical SiGe PMOSFET was found to be enhanced by as much as 70% as compared with the silicon control device, in both the forward and reverse modes of operation. The drain induced barrier lowering (DIBL) for the SiGe device was observed to be higher than the silicon device, since silicon-germanium has a lower bandgap than that of silicon. The sub-threshold slopes of the silicon and silicon-germanium devices were 105 and 180 mV/decade, respectively.

SESSION A3: POSTER SESSION
SILICON-BASED SUBSTRATES AND DEVICE PROCESSING
Chair: Tsu-Jae King
Monday Evening, November 26, 2001
8:00 PM
Exhibition Hall D (Hynes)

A3.1
EXPERIMENTAL STUDY OF THE ROLE OF HYDROGEN IN THE BREAKDOWN OF LOW-TEMPERATURE Si EPITAXY. J. Platen-Schwarzkopf, W. Bohne, W. Fuhs, K. Lips, J. Röhrich, B. Selle, and I. Sieber, Hahn-Meitner-Institut, Silizium-Photovoltaik and Ionenstrahl-Labor, Berlin, GERMANY.

We report on a study of homoepitaxial Si layer growth performed by Electron-Cyclotron Resonance Plasma-Enhanced Chemical Vapor Deposition (ECR PECVD) on Si(100) from a gas mixture of SiH_4, H_2 and Ar at temperatures between 325 and 500°C. The transition from epitaxial to disordered growth at a critical thickness was investigated at various growth conditions by changing the growth temperature, the gas flow rates and the substrate bias voltage. The depth profiles of the Si disorder and of the impurity concentrations (H, O, N, C and Ar) were studied by 1.4 MeV ^{4}He Rutherford Backscattering Spectrometry (RBS) in channeling mode, by Heavy-Ion Elastic Recoil Detection Analysis (HI-ERDA) using 230 MeV ^{129}Xe ions, and by Secondary Ion Mass Spectroscopy (SIMS). In addition, the films were analyzed by Raman spectroscopy and Scanning Electron Microscopy (SEM). - A striking similarity was found between the Si disorder profiles evaluated from the RBS channeling spectra and the impurity profiles determined by HI-ERDA and SIMS. Concurrent with the breakdown of the epitaxial growth a strong increase of the hydrogen concentration is found at the same depth position. Raman spectra and SEM cross-section images show that at this limiting thickness of epitaxial growth conically shaped precipitates of amorphous Si:H are being nucleated. The dependence of the critical thickness on the growth parameters can be understood within the framework of a model recently proposed by Thiesen et al. [1]. The model predicts the critical thickness due to a hydrogen supersaturation of the growth surface which is balanced by the incident hydrogen flux and the diffusive transport of hydrogen into the substrate. In accordance with this model we observe a significant concentration of hydrogen that has diffused into the Si substrate. [1] J. Thiesen, H.M. Branz, R.S. Crandall, Appl. Phys. Lett. 77, 3589 (2000).

A3.2
FABRICATION OF HIGH INTEGRITY THIN BURIED OXIDE LAYER FROM GOOD MATCHES OF DOSE-ENERGY COMBINATION. Chen Meng, Chen Jing, Wang Xiang, Dong Yeming, Liu Xianghua, Yu Yuehui and Wang Xi, Chinese Academy of Sciences, Shanghai, PR CHINA.

It is of great interest in low-dose (dose$<1.0\times10^{18}$ cm^{-2}) Separation of implanted oxygen (SIMOX), because the thin BOX SIMOX has been shown to improve wafer quality in all aspects as discussed for the full dose SIMOX wafers due to the lowered oxygen dose by reducing the implantation time. However, the low dose SIMOX materials usually have higher density of Si islands and pinholes in BOX layer, which have been reported to be responsible for increased electrical leakage current through the BOX, or in extreme cases, its dielectric breakdown. In this paper, we report directly formation of device grade low dose SIMOX materials at an energy of 45 - 160 keV with a dose of 1.8 - 13.5×10^{17} cm^{-2}. The materials were characterized by RBS, SIMS, TEM, HRTEM, SECCO, Cu-plating and MOS capacitance. The results reveal a series of good matches of dose-energy combination for formation of device-grade low-dose SIMOX materials with high crystal quality of top silicon layer, low silicon islands density and pinhole density in BOX layer. Minimal yields X_{min} from RBS measurement are 3.82 - 4.47%, which are comparable with that of virgin silicon. TEM reveals high integrity BOX layer is likely to be formed at a good match of dose-energy combination. HRTEM reveals a strong dependence of upper interface on dose-energy match. SECCO characterization indicates that samples fabricated at optimum dose-energy matches have a threading dislocation density lower 10^4 cm^{-2}. Cu-plating reveals that the samples implanted at optimum dose-energy matches have a pinhole density lower 3 cm^{-2} which is much lower than those implanted outside of optimum dose-energy match. Breakdown field determined from MOS capacitance is about 6 MV/cm[1]. Furthermore, the higher the oxygen dose, the higher the implanted energy required for the formation of Si-island free BOX. The effect of dose-energy match is due to the oxygen profile in as-implanted wafers, which is corrected with dose-energy match. This work also indicates a possibility to synchronous control the thickness of both SOI and BOX layer by choosing an optimum match of energy-dose combination. Furthermore, it can be used to fabricate ultra-SIMOX materials by optimizing low energy-dose implantation that will meet the requirements of fully depleted CMOS circuits and system-on-chip on SOI wafers, easily realize the patterned SOI structure, and improve the throughput capacity in the SIMOX wafer manufacture without additional products cost.

A3.3
A SELF-ALIGNED SILICIDE PROCESS FOR THIN SILICON-ON-INSULATOR MOSFETs AND BULK MOSFETs WITH SHALLOW JUNCTIONS. G.M. Cohen, C. Cabral Jr., C. Lavoie, P.M. Solomon, K.W. Guarini, K.K. Chan, R.A. Roy, IBM T.J. Watson Research Center, Yorktown Heights, NY.

Self-aligned silicide (salicide) is a process that converts the surface portions of the source, drain and gate silicon regions of CMOS devises into a low resistance silicide contact. The silicide film must be contained within the source and drain junction otherwise it would form a leakage path to the substrate. Scaling the gate length of a MOSFET requires shallow junctions to suppress short channel effects (SCE). The junction depth is expected to become comparable or even thinner than the silicide film thickness.
Scaling of the silicon-on-insulator (SOI) MOSFET leads to similar constraints on the salicide process. In the case of SOI, reducing the channel thickness (t_{si}) was found to have an important role in suppressing SCE for both single and double-gate MOSFETs. The use of the conventional salicide process with devices having a very thin SOI channel leads to the following problems: There may not be enough silicon in the source/drain regions to complete the silicide formation. Furthermore, even a consumption of more than 80% of the silicon film would actually increase the series resistance due to a reduction in the contact area.
A new salicide process flow with reduced silicon consumption was proposed and experimentally tested: A blanket film consisting of a Co and Si mixture (with 20% Si) was deposited and annealed to form the metal rich silicide phase (Co_2Si). Annealing was carried out with a TiN cap to prevent cobalt oxidation. The unreacted $Co_{0.8}Si_{0.2}$ mixture was etched selectively followed by a blanket Si cap deposition. The 2nd anneal formed the disilicide phase ($CoSi_2$) by consuming silicon from the underlying SOI and the overlaying silicon cap. Thus, the silicon consumption from the SOI layer is reduced by half during the second anneal. Since half of the silicon required to form the metal rich phase was present in the $Co_{0.8}Si_{0.2}$ mixture, the overall reduction in silicon consumption is 50% as compared to the conventional process. The unreacted portion of the silicon cap was etched selectively by TMAH. The $CoSi_2$ sheet resistance obtained on bulk silicon formed with the new process was 18 $\mu\Omega$-cm, and was the same as that obtained with the conventional salicide process. The process uses the same thermal cycles as the conventional salicide process and results in a raised source/drain structure.

A3.4
Abstract Withdrawn.

A3.5
ELECTRICAL PROPERTIES OF ULTRA SHALLOW P JUNCTION ON N TYPE Si WAFER USING DECABORANE ION IMPLANTATION. Jae-Hoon Song, Won-Kook Choi, Korea Insititute of Science and Technology, Thin Film Technology Research Center, Seoul, KOREA; Duck-Kyun Choi, Hanyang Univ, Dept of Inorganic Materials Engineering, Seoul, KOREA.

The junction depth should be less than 0.05 μm to fabricate sub 0.1 μm devices, which requires less than 1 keV ion implantation energy. However in this case, it takes so much time to implant ions due to low ion beam current. In addition, boron as a p type dopant for PMOSFET has high diffusivity and thus easily diffuses into Si wafer even in rapid thermal processing. To manipulate this problem on boron implantation, decaborane ($B_{10}H_{14}$) for low energy ion source was implanted to make p /n junction on n-type Si wafer. Ionized decarborane by thermo-electron bombardment was accelerated at 1-15

kV and implanted up to doses from $1\times10^{12}/cm^2$ to $5\times10^{13}/cm^2$. Afterward, B implanted Si wafers were post-annealed for 10 sec at 800°C, 900°, and 1000°, respectively. Through RBS channeling of as-implanted n-type Si wafer at 5kV, it was observed there are amorphous Si layers with 4 nm in depth and boron ions are implanted up to 1-5 nm in depth from SIMS analysis. These p /n junctions showed 127-130 Ω/sq. of sheet resistance, and I-V characteristics of 0.3V turn-on voltage and -1.1 V breakdown voltage. From above results, ultra shallow junction below than 10 nm can be assembled by this technique.

A3.6
GROWTH AND CHARACTERIZATION OF UHV-CVD SiGe STRAINED-LAYER SUPERLATTICES ON BULK CRYSTAL SiGe SUBSTRATES. Shuran Sheng, Institute for Microstructural Sciences, National Research Council of Canada, Ottawa, ON, CANADA; Michel Dion, SiGe Semiconductor Inc., Ottawa, ON, CANADA; Sean P. McAlister, Institute for Microstructural Sciences, National Research Council of Canada, Ottawa, ON, CANADA.

The development of advanced Si-based electronic and optical devices and thermoelectric generators incorporating Ge, would be enhanced by the availability of high-quality, low defect density substrates with an adjustable lattice parameter and band gap between Si and Ge. Such substrates would permit the growth of tensile-strained Si or SiGe layers, giving rise to a type II band alignment required for developing SiGe/Si devices based on electron confinement. Single crystal SiGe would be an advantage as the lattice-matched substrate material, instead of Si for SiGe epitaxial growth. Here, we report the first growth of high-quality UHV-CVD Si/SiGe strained-layer superlattices at 525°C on commercially available low defect density ($\sim10^4$ cm^{-2}) bulk crystal SiGe substrates grown using a modified Czochralski technique by Virginia Semiconductor Inc., rather than using thick virtual substrates. These strained-layer superlattices were characterized by high-resolution x-ray diffraction (XRD), Auger electron spectroscopy (AES), atomic force microscopy (AFM), cross-sectional transmission electron microscopy (TEM) and photoluminescence (PL) spectroscopy. XRD rocking curve analyses show uniform layer thickness and alloy composition across superlattices of 5 periods, in good agreement with Auger profile analysis. The Ge concentration determined by both XRD and AES is nearly the same as that for SiGe substrates. Neither strain relaxation nor threading dislocations were observed by XRD. AFM images show similar RMS roughness of much less 1nm for both the top layer surface and the substrate surface, indicating very smooth surfaces. Details of this work along with the data of interfacial abruptness, dislocations and defects will be presented. This study demonstrates that the use of bulk crystal SiGe substrates, combined with low temperature epitaxy, leads to high-quality strained-layer Si/SiGe superlattices, and may open up many new device applications.

A3.7
Abstract Withdrawn.

A3.8
POLY-SiGe TFTs FABRICATED BY LOW-TEMPERATURE CHEMICAL VAPOR DEPOSITION AT 450°C. Kousaku Shimizu, Jianjun Zhang, Jeong-woo Lee and Jun-ichi Hanna, Imaging Science and Engineering Laboratory, Tokyo Institute of Technology.

Low temperature growth of poly-SiGe has been investigated by reactive thermal chemical vapor deposition (RTCVD) method, which is a newly developed technique for preparing poly-SiGe by using redox reactions in a set of source materials, i.e., disilane (Si_2H_6) and germanium tetrafluoride (GeF_4). The technique gives quite uniform films as well as no polymeric silane particles, which can be applied to large-area electronic devices such as TFT arrays for flat-panel display devices and solar cells. This is because the source gases are activated thermally at the vicinity of the substrate surface and reacts each other, resulting in film growth on the substrate as is the case of the thermal CVDs. Moreover, in this CVD, germanium tertrafluoride plays an important role to crystal growth at a low temperature of 450°C. In order to prepare Si-rich poly-SiGe (Si >96 atm%), total pressure, gas flow ratio and residence time were optimized. The typical condition is as followed: the gas flow rate of $Si_2H_6/GeF_4/He$=5/0.5/1000(sccm), the reaction pressure of 5.0 Torr and substrate temperature of 450°C. In this condition, the film uniformity (>90%) and reproducibility was well established. Bottom gate type of n-channel TFTs have been fabricated with 200nm thick films of poly-SiGe with various grain sizes on the glass substrates. The TFTs were treated with atomic hydrogen after fabrication by using hot wire technique. The TFTs of L/W=50μm/50μm exhibit the field effect mobility of 5-30 cm^2/Vs with an increase in the grain size of 500-900nm. Threshold Voltage (Vt) is around 2±0.5V, and On/Off ratio is more than 10^4.

A3.9
IN-SITU X-RAY STUDIES OF SILICON SURFACES UNDERGOING ION SPUTTERING. C.R. Eddy, Jr., K.F. Ludwig, Jr., R. Singh, Depts. of Electrical Engineering and Physics, Boston University, Boston, MA; O. Malis, R. Headrick, CHESS, Cornell University, Ithaca, NY.

Plasma etching of silicon plays a critical process role in the fabrication of a wide range of devices from microelectromechanical systems to integrated circuits. As such, plasma etching has been the subject of much characterization and simulation in an effort to perfect the patterning of surfaces while imparting minimal damage. In-situ surface x-ray diffraction offers a unique tool for the study of surface structural evolution during processing. As a first step toward realizing this capability, we have examined the evolution of silicon surfaces undergoing the purely physical component of such processes - ion sputtering. Using synchrotron x-ray radiation, we have examined silicon (100) and (111) surfaces undergoing Ar^+ ion bombardment as a function of ion energy (100 to 500 eV) and temperature (50 to 450°C). Grazing-incidence small-angle x-ray scattering (GISAXS) shows that the surface morphology evolution varies significantly with ion energy in this range. In some parameter ranges, a single roughness length scale apparently dominates the surface morphology while in others at least two separate length scales appear. The results of the in-situ characterizations are supplemented by ex-situ atomic force microscopy (AFM) of the processed surfaces. Feature sizes observed by AFM on the processed surfaces agree well with the length scales determined by the in-situ measurements.

A3.10
OPTIMIZED HETEROSTRUCTURES FOR SiGe-BASED CMOS APPLICATIONS. C.W. Leitz[a], M.T. Currie[a], M.L. Lee[a], Z. Cheng[a], D.A. Antoniadis[b], E.A. Fitzgerald[a]; [a]Department of Materials Science and Engineering, MIT Cambridge, MA; [b]Department of Electrical Engineering and Computer Science, MIT Cambridge, MA.

Strained Si- and SiGe-based heterostructure MOSFETs grown on relaxed SiGe virtual substrates exhibit dramatic electron and hole mobility enhancements over bulk Si, making them promising candidates for next generation CMOS devices. The most heavily investigated heterostructures consist of a single strained Si layer grown upon a relaxed SiGe substrate. While this configuration offers significant pMOS and nMOS performance gains, hole mobility is still much lower than electron mobility. By contrast, the combination of buried compressively strained SiGe layers and tensile strained Si surface layers grown on relaxed SiGe, hereafter referred to as dual channel heterostructures, offers nearly symmetric electron and hole mobilities without compromising nMOS device performance. To investigate these heterostructures, we study the effects of alloy scattering, channel thickness, and surface morphology on channel mobility in long channel MOSFETs. In these experiments, MOSFETs are fabricated by a novel short flow process utilizing a deposited gate dielectric and only one lithography step. This type of device allows us to measure effective mobility at vertical fields approaching 1 MV/cm, thereby enabling us to quickly explore the impact of materials parameters on channel mobility at fields approaching those of state-of-the-art MOSFETs. With this approach, we have achieved hole mobility enhancement factors over bulk Si of 5.15 for dual channel heterostructure devices. By employing different virtual substrate compositions, we can decouple the effects of strain and alloy scattering in both tensile surface channels and compressive buried channels. Direct measurements of the impact of alloy scattering on channel mobility in both of these layers will be presented. Mobility enhancements in hole channels will also be correlated to changes in channel morphology resulting from large compressive strain levels. We will demonstrate that dual channel heterostructures provide excellent performance gains for both pMOS and nMOS devices and explore the useful design space of these structures.

SESSION A4: MILC MATERIALS GROWTH FOR CMOS AND TFT
Chair: Mansun J. Chan
Tuesday Morning, November 27, 2001
Room 202 (Hynes)

8:45 AM A4.1
GRAIN QUALITY ENHANCEMENT OF NICKEL-CRYSTALLIZED POLYSILICON FILM IN QUANTUM-WIRE-LIKE STRUCTURES. W.M. Cheung, Hongmei Wang, Singh Jagar, C.F. Cheng, M.C. Poon, Mansun Chan, Dept of Electrical & Electronic Engineering, Hong Kong University of Science & Technology, Sai Kung, HONG KONG.

Methods for forming high quality recrystallizing polysilicon films are being actively studied due to their ability to provide significant improvement to polysilicon Thin-Film-Transistors (TFT). Recently, a simple Metal-Induced-Lateral-Crystallization (MILC) method with

nickel, together with high temperature annealing, can result in single crystal like polysilicon film [1]. TFTs fabricated on this so-called Large-grain Silicon-On-Insulator (LPSOI) can achieve SOI MOSFET performance especially at small dimension. This paper reports that the silicon grain quality can be further enhanced by crystallizing the polysilicon film into the shape of long-wire. The crystallization procedure starts with a regular MILC process at 560°C as described in [1]. The film is then etched into narrow wires parallel to the direction of nickel propagation. The second anneal at 850-900°C is then performed on these silicon wire. Through surface energy anisotropy stimulated grain expansion in the post-MILC annealing, enhanced grain quality beyond that on planar polysilicon film. Transistor fabricated on these wire is similar to gate-all-around structure as that of FinFET [2]. Much better scalability to the deep submicron region is observed for these wire transistors than regular planar TFTs formed on the same MILC film. Experiment results show that a wide transistor formed by the parallel combination of the wire transistors give 400% more current drive than a TFT on the same MILC film with equivalent width. [1] S. Jagar, M. Chan, M.C. Poon, H. Wang, M. Qin, P.K. Ko, and Y. Wang, "Single Grain Thin-Film-Transistor (TFT) with SOI CMOS Performance Formed by Metal-Induced-Lateral-Crystallization", 1999 IEEE International Electron Device Meeting (IEDM) Technical Digest, pp. 293-296, Dec. 5-8, 1999, Washington, DC. [2] X. Huang, W.-C. Lee, C. Kuo, D. Hisamoto, L. Chang, J. Kedzierski, E. Anderson, H. Takeuchi, Y.-K. Choi, K. Asano, V. Subramanian, T.-J. King, J. Bokor, and C. Hu, "Sub 50-nm FinFET: PMOS", 1999 IEEE International Electron Device Meeting (IEDM) Technical Digest, pp. 67-70, Dec. 5-8, 1999, Washington, DC.

9:00 AM A4.2
ENHANCEMENT OF METAL-INDUCED LATERAL CRYSTALLIZATION RATE BY SCAN-TYPE RAPID THERMAL ANNEALING. Hye-Hyang Park, Yeo-Geon Yoon, Gi-Bum Kim, Seung-Ki Joo, School of Materials Science and Engineering, College of Eng., Seoul National University, Seoul, KOREA.

It has been known that amorphous silicon (a-Si) can be crystallized below 500°C by metal-induced lateral crystallization (MILC) phenomenon. In this study, a-Si was crystallized by conventional rapid thermal annealing (RTA) and scan-type RTA, and compared each other. MILC growth length of scan-type RTA was calculated from the temperature profile and activation energy of MILC, and then which was compared with the experimental length. The experimental value of scan-type RTA was several times larger than calculated value, while that of conventional RTA was almost same to the calculated value. As a result, we found that scan-type RTA was more favorable in term of growth rate than the conventional RTA. We also performed experiments about the temperature gradient effects on the crystallization of a-Si. The growth rate of the crystallization of the a-Si with positive temperature gradient was faster than that of negative temperature gradient. It has been found that temperature gradient helps catalytic transformation in MILC, which results in the MILC rate by the order of magnitude.

9:15 AM A4.3
EFFECTS OF PROCESS CONDITIONS ON THE PERFORMANCE OF LARGE GRAIN POLY-SILICON ON INSULATOR (LPSOI) MOSFET FOR ADVANCED CMOS APPLICATIONS. C.F. Cheng, S. Shivani, M.C. Poon and Mansun Chan, Department of Electrical and Electronic Engineering, Hong Kong University of Science and Technology, Kowloon, HONG KONG.

With the increasing demand for higher packing densities of VLSI, there has been much attention to Silicon-On-Insulator (SOI) devices. SOI devices possess the considerable advantages of high packing density, easy isolation, simple process as well as the possibility to be used in 3-D integration. To achieve maximum flexibility make available from SOI technology, a method to form high quality silicon film on oxide and other insulating substrate is required. We have previously demonstrated that with the combination of MILC and high temperature annealing on amorphous film, very large grain can be achieved. However, the conditions of grain enlargement needs to be optimised and requires a well-established process. The effects of process conditions (temperature, time, thermal budget etc.) on the performance of LPSOI MOSFET are studied. A method of ramp annealing with the combination of MILC is proposed and the effect of temperature and time was studied in detail and optimized. It has been found that the grain size after ramp annealing is remarkably enhanced and can reach of the order of several ten's of microns. The velocity of MILC with ramp annealing is two to three times faster than that of MILC with isothermal annealing Finally, TFTs were fabricated and characterized at different MILC annealing temperatures with and without subsequent high temperature compatible with conventional CMOS process with only one extra mask added. The mobility of the TFTs fabricated using ramp annealing was found to be two times more than those fabricated using isothermal annealing. It was found that the thin film transistors fabricated by the proposed method showed considerably improvement in the electrical characteristics, which directly reflect the quality of polycrystalline silicon active layer. It is believed that super TFTs with SOI CMOS performance and good uniformity can be obtained through the reduction in channel dimensions and optimized process conditions.

9:30 AM A4.4
EFFECTS OF DOPANTS ON METAL INDUCED LATERAL CRYSTALLIZATION RATE. Gi-Bum Kim, Yeo-Geon Yoon, Ji-Soo Ahn, Hye-Hyang Park, Min-Sun Kim, Joo-Wook Park, Seung-Ki Joo, School of Materials Science and Engineering, Seoul National Univ., Seoul, KOREA.

Polycrystalline silicon thin film transistors (poly-Si TFTs) technology is very attractive for the applications of active matrix liquid crystal devices (AM-LCDs) with integrated peripheral driver circuits fabricated on glass substrates. So many works have been concentrated on lowering the crystallization temperature of a-Si films. Metal induced lateral crystallization (MILC) process has been previously introduced, by which the amorphous silicon thin films can be crystallized below 500°C. In this works, the effects of dopants on the rate and behavior of MILC were investigated. When a-Si was doped with boron, MILC rate has increased to about twice of intrinsic a-Si and the front edge of crystallized silicon became rugged. But the a-Si doped with boron quantity of below 1E14/cm^2 did not show the any improvement in MILC rate. On the contrary, in case of phosphorus doped a-Si, MILC rate was decreased about 75% and there are still some a-Si islands in the crystallized silicon region. The role of dopants in MILC rate, specially the mechanism of the accelerated MILC rate of boron doped a-Si, will be discussed in terms of activation energy for crystallization of a-Si and microstructure.

9:45 AM A4.5
LATERAL EPITAXIAL OVERGROWTH OF Si AND SiGe ON SiO_2 USING BURIED LOW-TEMPERATURE (T_s <500°C) SOLID-METAL-MEDIATED EPITAXY. T.J. LaFave, N. Lakshminarayana, and M.-A. Hasan. C.C. Cameron, Applied Research Center & The Department of Electrical and Computer Engineering, University of North Carolina, Charlotte, NC.

Buried lateral epitaxial overgrowth of Si on thin SiO_2 layers (<100 nm) using a thick solid Al layer as growth mediator was demonstrated using a newly developed solid-metal-mediated epitaxy (SMME) method. The experiments were carried out at growth temperatures T_s <500°C using electron beam evaporation for Si and thermal evaporation of Al from an effusion cell. Si(100) wafers were thermally oxidized and patterned to provide seed/oxide strips ranging from 2/2 to 50/500 microns. Each seed/oxide strip was repeated within an area of ~1.25x2.00 cm^2 and all patterns were placed on the same wafer. The wafers were then thermally etched at T_s = 900°C under UHV conditions to desorb the remnant native oxide from the seed areas followed by deposition of Al at room temperature. Si was then deposited on the resulting structure at T_s <500°C re-grew epitaxially at the buried Al/Si interface and growth was extended laterally over the oxide layer. Initial TEM results demonstrated lateral growth of single crystalline Si over the oxide layer. This SOI method described above is based on SMME. In SMME, silicon grows epitaxially at a buried Al/Si interface during thermal evaporation of Si. Si atoms diffuse through the Al overlayer to the interface where low-energy atomic Si sites act as sinks for the diffusing Si atoms. This process is fundamentally different from surfactant assisted growth in which a small concentration of a metal (typically a fraction of a monolayer) is used to enhance epitaxial growth. In SMME, the Al layer can be thousands of monolayers thick (solid). The new findings may lead to new silicon-on-oxide fabrication method. Also, it provides a procedure for combined metallization and heavy p-type doping, e.g. in MOS device structure. Applications of this method in device fabrication will be discussed.

SESSION A5: NANOCRYSTAL MEMORIES
Chair: Sandip Tiwari
Tuesday Morning, November 27, 2001
Room 202 (Hynes)

10:30 AM *A5.1
NANOCRYSTAL MEMORIES AS ELECTRONIC AND PHOTONIC DEVICES. Harry A. Atwater, Caltech, Pasadena, CA.

Si nanocrystal memories in which a dense Si nanoparticle array comprises the floating gate of a nonvolatile field effect device have potential for pervasive application in electronics and photonics. In this talk, I will describe recent work on different approaches to nanocrystal memory fabrication, and also about efforts to enhance the read/write performance through the use of heterostructure layered tunneling barriers to achieve nanosecond program/erase times with

archival retention times. Further we are currently investigating optical reading and writing of nanocrystal memories as a tool to understand the physics of these devices and to assess the potential for optical nanocrystal memories to function as optically addressable nonvolatile devices.

11:00 AM *A5.2
FUTURE SILICON NANOCRYSTAL NONVOLATILE MEMORY TECHNOLOGY. Michele L. Ostraat, Jan De Blauwe, Agere Systems, Murray Hill, NJ.

A great deal of research interest is being invested in the fabrication and characterization of nanocrystal structures as charge storage memory devices. In these flash memory devices, it is possible to measure threshold voltage shifts due to charge storage of only a few electrons per nanocrystal at room temperature. Although a variety of methods exist to fabricate nanocrystals and to incorporate them into device layers, control over the critical nanocrystal dimensions, tunnel oxide thickness, and interparticle separation and isolation remains difficult to achieve. This control is vital to produce reliable and consistent devices over large wafer areas. To address these control issues, we have developed a novel two-stage ultra clean reactor in which the Si nanocrystals are generated as single crystal, nonagglomerated, spherical aerosol particles from silane decomposition at 950°C at concentrations exceeding 10^8 cm^{-3} at sizes below 10 nm. Using existing aerosol instrumentation, it is possible to control the particle size to approximately 10% on diameter. Particles are passivated with a high quality oxide layer with shell thickness controllable from 0.7 to 2.0 nm. The two-stage aerosol reactor is integrated to a 200 mm wafer deposition chamber such that controlled particle densities can be deposited thermophoretically. With nanocrystal deposits of 10^{13} cm^{-2}, contamination of transition metals and other elements can be controlled to less than 10^{10} atoms cm^{-2}. We have fabricated 0.2 μm channel length aerosol nanocrystal floating gate memory devices using conventional MOS ULSI processing on 200 mm wafers. The aerosol nanocrystal memory devices exhibit normal transistor characteristics with drive current 30 $\mu A/\mu m$, subthreshold slope 200 mV/dec, and drain induced barrier lowering 100 mV/V, typical values for thick gate dielectric high substrate doped nonvolatile memory devices. Uniform Fowler-Nordheim tunneling is used to program and erase these memory devices. Despite 5 nm tunnel oxides, threshold voltage shifts >2 V have been achieved with microsecond program and millisecond erase times at moderate operating voltages. The aerosol devices also exhibit excellent endurance cyclability with no window closure observed after 10^5 cycles. Furthermore, reasonable disturb times and long nonvolatility are obtained, illustrating the inherent advantage of discrete nanocrystal charge storage. No drain disturb was detected even at drain biases of 4V, indicating that little or no charge conduction occurs in the nanocrystal layer. We have demonstrated promise for aerosol nanocrystal memory devices. However, numerous issues exist for the future of nanocrystal devices. These technology issues and challenges will be discussed as directions for future work.

11:30 AM A5.3
ELUDING METAL CONTAMINATION IN CMOS FRONT-END FABRICATION BY NANOCRYSTAL SELF ASSEMBLY. Zengtao Liu, Chungho Lee, Gen Pei, Venkat Narayanan and Edwin C. Kan, School of Electrical and Computer Engineering, Cornell University, Ithaca, NY.

Use of metals in nano-scale CMOS structures offers many attractive device features. Metal gate is void of poly depletion or dopant penetration, and provides the design choice of work function to alleviate threshold adjustment by channel doping [1]. Nondegenerate doping in nano-scale devices may suffer from position/number fluctuations and insensitivity for fully depleted SOI. Metal nanocrystal floating gate EEPROM cells are much less subject to interface fluctuation and offer lower voltage/longer retention operations than Si/Ge nanocrystal ones [2]. Metal source/drain contacts by thin-films [3] or nanocrystals [4] can eliminate the need of doping entirely in CMOS and reduce the sheet/contact resistance [5]. However, metals are conventionally forbidden in the front-end fabrication before the relatively thick CVD oxide (>100nm) is deposited over poly gate layers, especially for short-channel and shallow-junction devices. Metals can contaminate oxide and Si by junction spiking, grain boundary worming, mismatched expansion and deep diffusion during later thermal cycles, which can cause serious hazard to channel mobility, minority lifetime, interface states and oxide quality [6]. We have demonstrated that metal contamination can be virtually eliminated by the surface energy minimization step in RTA (also called nanocrystal self assembly or ripening). If nanocrystal formation dominates over the other processes during RTA, later thermal cycles including source/drain dopant activation will not cause metal nanocrystals to decompose. This assumption is corroborated by monitoring MOSC deep depletion holding time (for minority lifetime), accumulation-to-inversion transition (for interface states), gate leakage current (for oxide traps), and MOSFET channel universal mobility (for Si traps) for structures containing metals (Au, Ag, Pt, and W) on thin gate oxide (5-7nm). This newly observed phenomenon has provided an effective integration option for using metals in the front-end process. Thicker continuous metal films can also potentially be achieved by stitching thin metal layers or nanocrystals.

11:45 AM A5.4
CAPACITANCE-VOLTAGE HYSTERESIS IN THE METAL-OXIDE-SEMICONDUCTOR CAPACITOR WITH Si NANOCRYSTALS DEPOSITED BY THE GAS EVAPORATION TECHNIQUE. Puspashree Mishra, Shinji Nozaki, Ryuta Sakura, Hiroshi Morisaki, Hiroshi Ono, Kazuo Uchida, Department of Electronic Engineering, The University of Electro-Communications, Tokyo, JAPAN.

Capacitance-voltage (C-V) hysteresis was observed in the metal-oxide-semiconductor (MOS) capacitor with silicon nanocrystals. The MOS capacitor was fabricated by thermal oxidation of Si nanocrystals, which were deposited on an ultra-thin thermal oxide grown previously on a p-type Si substrate. The Si nanocrystals were deposited by the gas evaporation technique with a supersonic jet nozzle. This technique has been developed to deposit Si nanocrystals at the supersonic speed resulting from the differential pressure between the evaporation and the deposition chamber. The size of nanocrystals is precisely controlled by the gas pressure and the distance of the nozzle from the evaporation boat. The size uniformity and crystallinity of the Si nanocrystals are found to be better than those fabricated by the conventional gas evaporation technique. The MOS capacitor consists of 2 nm tunnel oxide and 15 nm control oxide with 3 - 5 nm nanocrystals and exhibits hysteresis loops in the C-V characteristics. In contrast, the MOS capacitors without the nanocrystals do not show any hysteresis. The hysteresis is attributed to electron charging and discharging of the nanocrystals, which function as a charge storage. Both charging and discharging are achieved at small gate voltages in the direct tunneling regime. The flat band shift depends on the size and density of the nanocrystals and the gate voltage. Higher positive gate voltage leads to greater flat band shift, indicating storage of more number of electrons in the nanocrystals. The retention characteristic of the above structure has been also studied. The MOS structure with Si nanocrystals deposited by the gas-evaporation technique has proved to be a good candidate for nanocrystal memories.

SESSION A6: GROWTH OF NANOSTRUCTURED MATERIALS
Chair: Michele L. Ostraat
Tuesday Afternoon, November 27, 2001
Room 202 (Hynes)

1:30 PM A6.1
LOW PRESSURE CHEMICAL VAPOR DEPOSITION OF Si NANOCRYSTALS FOR NON-VOLATILE MEMORIES. R. Rao, K. Scheer, G. Malyavanatham, R. Muralidhar, M. Rossow, B-Y, Nguyen and B. White, Materials and Structures Labs, Motorola SPS, Austin, TX.

Si nanocrystal based non-volatile memories are increasingly attracting more research effort due to their low voltage operation, long retention and fast write times. A critical technology issue in the fabrication of these devices is the uniform deposition of a high density (of the order of $10^{12}/cm^2$) of Si nanocrystals without inducing coalescence. Such a high density of Si nanocrystals is not easily achieved on SiO_2 substrates. Numerous efforts have focussed on obtaining a high density of nanocrystals through a variety of deposition techniques including aerosol technique, sol-gel technique, ion-implantation, low pressure chemical vapor deposition (LPCVD), molecular beam epitaxy and cluster beam evaporation. We have grown Si nanocrystals on SiO_2 and Si_3N_4 substrates by LPCVD and characterized the size and density of these nanocrystals using atomic force microscopy, scanning electron microscopy and transmission electron microscopy. This paper will explore the nucleation and growth mechanisms of Si nanocrsytals deposited by LPCVD on dielectric surfaces. Specifically, the nucleation curves from incubation to coalescence will be compared on different substrate surfaces. The influence of precursor gas partial pressure and substrate temperature on the nucleation and growth characteristics will be investigated in terms of the size and density of the Si nanocrystals. Furthermore, the use of different precursor and carrier gases will also be compared.

1:45 PM A6.2
GROWTH OF Si NANOCRYSTALS VIA PHYSICAL AND CHEMICAL VAPOR DEPOSITION. T. Leach, G. Malyavanatham, Jianhong Zhu and D. Ekerdt, Department of Chemical Engineering, University of Texas, Austin, TX; R. Rao, K Scheer, R. Muralidhar, B. Nguyen, B. White, M. Rossow, Materials and Structures Labs,

Motorola SPS, Austin, TX.

The control of silicon nanocrystal density and size is crucial in silicon nanocrystal based electron devices such as single electron transistors and nanocrystal floating gate memories. The atomistic nucleation and growth of Si nanocrystals on structureless substrates like silicon dioxide and silicon nitride occurs via a Volmer/Weber island growth mechanism that exhibits a) an incubation phase where the adatom concentration in surface builds up, b) a rapid nucleation phase where stable clusters are formed, c) a saturation phase where the density of nanocrystals remains constant but increase of size occurs and d) a coalescence phase where growing nanocrystals begin to touch each other. In this paper, we focus on the first two stages via physical vapor deposition (PVD) achieved via cracking of reactant to form silicon and UHVCVD/LPCVD with the objective of understanding the roles of gas phase transport, surface reaction and surface diffusion of adatoms. In physical vapor deposition, the nanocrystal density is dependent on two time scales, a) arrival of Si atoms on the surface and b) surface diffusion. In chemical vapor deposition, there can be three timescales: a) arrival of chemisorbing species on the surface, b) surface reaction including by-product desorption and c) surface diffusion of Si adatoms. This is particularly so when incoming adsorption sites potentially block the chemisorbing species. Experimental results as a function of reactant type and reactant partial pressure, surface temperature and type of adsorbing surface will be used to delineate the differences between PVD and CVD methods. A first principles model accounting for adatom formation, surface diffusion and clustering will be used to interpret the results. This work attempts to delineate for the first time the differences between PVD and CVD on saturation density of nanocrystals.

2:00 PM A6.3
SILICON QUANTUM DOTS ON DIELECTRICS: ELUCIDATING KINETICS OF ADATOM FORMATION, NUCLEATION AND DOT GROWTH. W. Thomas Leach, Jian-hong Zhu, John G. Ekerdt, The University of Texas at Austin, Dept of Chemical Engineering, Austin, TX.

Routes to high density and uniform size Si quantum dots on SiO_2/ and Si_3N_4/Si(100) substrates for use in quantum dot flash memory applications are presented. The kinetics of adatom formation, nucleation and dot growth are studied by depositing Si adatoms onto the substrates through conventional thermal chemical vapor deposition (CVD) with disilane and by physical vapor deposition from a hot wire over which disilane is cracked. A computer simulation is presented that predicts dot density and size distributions based on growth conditions, and correlation with our and other published data is demonstrated. Finally, we describe theoretically how to fabricate high-density dots of uniform size by controlling the adatom flux onto the substrate and the diffusion length. Dots grown according to these principles are presented with densities as high as 9×10^{11} dots/cm^2.

2:15 PM A6.4
LPCVD DEPOSITION TECHNIQUES FOR NANOGRAIN SUB-10NM POLYSILICON ULTRA-THIN FILMS. Serge Ecoffey, Didier Bouvet, Adrian M. Ionescu, Pierre Fazan, Swiss Federal Institute of Technology, Electronic Laboratories, Lausanne, SWITZERLAND.

This work evaluates the limits of three different approaches to achieve the deposition of a nanograin ultra-thin (< 10nm) polysilicon film for Single-Electron Devices (SED): (i) Direct polysilicon (poly-Si) deposition - Because of the high deposition rate of poly-Si around 620°C, films become porous for thickness below 30nm, though grain sizes between 20nm and 30nm are achievable. A good option to reduce porosity is to dilute the silane in hydrogen, helium or nitrogen to decrease the growth rate, a tuning of the deposition temperature allowing a good control of the grain size. (ii) Hemispherical Silicon Grain (HSG) deposition - The size and density of the HSG are influenced by pressure, temperature and time during deposition and in-situ annealing of the film. The paper demonstrates the feasibility of HSG with sizes around 50nm and the potential extension of the proposed method for sizes less than 10nm. (iii) Amorphous silicon (a-Si) deposition followed by a crystallization anneal - The key factor to obtain an uniform layer with the a-Si/crystallization process lies in a good control of the nucleation phase at the early stage of deposition. At 500°C, with a silane pressure of 150mT, the film appears to be porous for a 10nm thick layer. Hence, we identified three different ways to raise the density of nuclei: replace the SiO_2 tunnel oxide by Si_3N_4, increase the pressure of silane, or dip the wafer into a HF solution before deposition. With these methods we have succeeded in the deposition of uniform poly-Si layer ranging from 6nm to 10nm with equivalent grain sizes. As a conclusion, it is worth noting that the deposition of nanograin, ultra-thin polysilicon films involves process innovation in both nucleation and annealing phases. It was found that the a-Si/crystallization process seems to be the best candidate for polysilicon films and grain sizes less than 10nm.

2:30 PM A6.5
Si/SiGe NANOSTRUCTURES FABRICATED BY ATOMIC FORCE MICROSCOPY OXIDATION. Xiang-Zheng Bo, Leonid Rokhinson, Haizhou Yin, D.C. Tsui, J.C. Sturm, Center for Photonics and Optoelectronic Materials, Department of Electrical Engineering, Princeton University, Princeton, NJ.

There is a great interest in the ability to pattern Si/SiGe structures with small features using processes which do not cause radiation or etching damage. Recently, silicon has been locally oxidized by atomic force microscopy (AFM) writing in air with feature size down to 10-30 nm. In this work, we have extended this method of AFM oxidation to strained SiGe alloys using a controlled humidity environment. The writing creates a raised surface feature because of the volume expansion associated with oxidation. The effects of oxidation parameters, such as, bias voltage on the microscope tip, tip writing speed, and tip tapping amplitude on the line-width and oxide height on SiGe have been investigated, and compared with that of local oxidation on silicon. It was found that when bias voltage increases, and/or when the tip writing speed decreases, or/and when tapping amplitude decreases, the oxidation height of silicon germanium increases. Minimum line widths of 25 nm were achieved both in the oxide feature and in the SiGe after the oxide was removed by wet etching. Typical writing speed are about 0.1-10 micron per second. In contrast to conventional thermal oxidation, the oxide height on SiGe alloys is slightly less than that on Si. Finally, this method was used to successfully cut SiGe quantum well lines with high resolution and confirmed electrically, which demonstrated the first use of AFM writing to pattern Si/SiGe device structures. This work was supported by ARO-MURI DAA655-98-1-0270.

2:45 PM A6.6
WIRE-LIKE SILICON NANO-HETEROSTRUCTURE GROWN BY SELF-ORGANIZING PROCESSES. A. Klimovskaya, I. Prokopenko, A. Efremov, A. Sarikov, P. Lytvyn, S. Kostyukevich, Institute of Semiconductor Physics NAS, Kyiv, UKRAINE; I. Ostrovskii, State Univ "Lviska Polytechnika", Lviv, UKRAINE; A. Gutovskii, Yu. Nastaushev, A. Aseev, Institute of Semiconductor Physics SD RAS, Novosibirsk, RUSSIA.

Using several self-organizing processes we grow the smallest Si-based heterostructures currently known. They consist of a cylinder-like c-Si core and nanoporous Si-based envelope. A morphology of the envelope as well its crystalline structure are controlled by changing growth conditions such as a growth temperature, rate of Si-atoms flux, etc. The heterostructures were characterized by different high-resolution instruments (CM 200UT Philips, EM4000EX Jeol, IMS 4F Fiber, PHI 660 Perkin-Elmer, etc.) and reveal a high stability of their physical properties.

SESSION A7: NANO-SCALE DEVICES
Chair: Harry A. Atwater
Tuesday Afternoon, November 27, 2001
Room 202 (Hynes)

3:30 PM *A7.1
SILICON SINGLE-ELECTRON TRANSISTORS AND SINGLE-ELECTRON CCD. Yasuo Takahashi, Akira Fujiwara, Yukinori Ono, Hiroshi Inokawa, and Kenji Yamazaki, NTT Basic Research Laboratories, Atsugi-shi, JAPAN.

Single-electron transistors (SETs) are advantageous for future large-scale integration because of their ultralow power-consumption and small size. The most difficult issue in fabricating SETs is to make a nanometer-scale island sandwiched between tunnel capacitors at both ends. We have developed a method called PADOX (PAttern-Dependent Oxidation) [1,2], that exploits a special phenomenon that occurs when a Si nanostructure is thermally oxidized. PADOX converts a small one-dimensional Si wire to a tiny SET in a self-aligned manner. The basic mechanism of this conversion is that the oxidation causes huge stress to accumulate in the middle of the wire. This produces a potential dip in the middle of the wire since strain due to the stress reduces the band-gap energy. In addition, the quantum size effect in the whole wire increases the effective bad gap there. These result in a potential profile for a SET. We have demonstrated the integration of SETs to embody various circuits, such as a half-adder and multiple-valued logic circuits.
We have also developed another device that enables us to manipulate a single electron without attaching tunnel capacitors [3]. The device utilizes small Si wire MOSFETs connected in series, and an elemental charge can be transferred like in a CCD. In addition, we can sense the existence of the elemental charge (single hole) by using electron current since the device employs the electron-hole-coexistence system where electrons and holes are separated in space by large electric

fields.
These devices will provide single-electron LSIs with highly sophisticated functions. [1] Y. Takahashi et al., Electron. Lett. **31**, 136 (1995).
[2] Y. Ono et al., IEEE Trans. Electron Devices **47**, 147 (2000).
[3] A. Fujiwara et al., Nature **410**, 560 (2001).

4:00 PM A7.2
EPITAXIAL $CoSi_2$/Si-NANOSTRUCTURES AND THEIR USE FOR ADVANCED MOSFET-DEVICE STRUCTURES. P. Kluth, Q.-T. Zhao, S. Winnerl, E. Rije, S.M. Hogg, S. Lenk, and S. Mantl, Forschungszentrum Jülich, Institut für Schichten und Grenzflächen (ISG-IT), Jülich, GERMANY.

We developed a novel patterning technique for ultra-thin, single-crystalline $CoSi_2$-layers to produce functional silicide/Si structures. The method, involving only conventional optical lithography and standard silicon processing steps, uses controllable stress effects during local oxidation of the silicide to generate uniform gaps in the silicide layer with dimensions down to 40 nm and $CoSi_2$-nanowires with diameters down to 50 nm. The structures are generated along the edges of an oxidation mask consisting of 20 nm SiO_2 and 300 nm Si_3N_4 patterned with conventional optical lithography and dry etching. This mask induces a strain field into the underlying layers causing anisotropic diffusion of the Co atoms during rapid thermal oxidation. The diffusion behavior, combined with different mask geometries and etching steps to shift or modify the stress conditions leads to the above mentioned nanostructures. This technique was successfully applied to 20-30 nm thick $CoSi_2$-layers grown on Si(100) and ultra-thin silicon on insulator (SOI) substrates using molecular beam allotaxy (MBA). Commercial SOI layers were thinned down by furnace oxidation and wet etching. High quality, thermally stable single-crystalline silicide layers were produced on both types of substrates. The silicide/silicon interface of these layers is atomically abrupt and they form excellent Schottky contacts on moderately doped p- and n-type silicon. The nanogaps were used to fabricate planar short-channel Schottky-Barrier MOSFETs. These transistors can be driven as both p-channel and n-channel devices without complementary substrate doping. The nanowires can be used as building blocks for vertical nano-MOSFETs, where they can be used as an etching mask for narrow silicon lines as well as a top contact on the silicon ridge. Structural and electrical properties of these wire/ridge-structures are investigated before and after performance of shallow implants.

4:15 PM A7.3
HETEROGENEOUS ELECTRICAL PROPERTIES OF SiGe NANOSTRUCTURES DETERMINED BY ELECTRIC FORCE MICROSCOPY. E.R. Tevaarwerk, P. Rugheimer, D.E. Savage, M.G. Lagally, M.A. Eriksson, University of Wisconsin-Madison, Madison, WI.

Future integrated circuits may exploit nanostructured materials in place of conventional materials in CMOS devices. Arrays of electrically isolated SiGe self-assembled 3D quantum dots (QDs) could provide exceptionally thin and well-controlled nanostructured gates. Thinned silicon top layers on SOI wafers can enable electrical isolation of neighboring QDs from each other. Electric force microscopy (EFM) allows measurements of electric field gradients, providing a powerful method for investigating the nanoscale electrical properties of SiGe QDs. We have patterned thinned SOI (5 nm silicon) into mesas with widths ranging from 5 to 20 mm. When germanium is deposited on these mesas, the resulting QDs grow in concentric rings beginning at the edge of the mesas; the QDs vary in size across the mesas, with the largest QDs found near the edge. Atomic force microscopy and transmission electron microscopy measurements indicate that QDs in the outer rings are separated from each other by oxide, whereas QDs toward the center of the mesa may be connected by a thin silicon layer. EFM measurements support this interpretation, indicating that the outer rings of QDs are significantly different from the QDs in the inner rings. In comparison, QDs grown on patterned bulk silicon display a uniform EFM signal. This work supported by NSF.

4:30 PM A7.4
LAYERED TUNNEL BARRIERS FOR SILICON BASED NONVOLATILE MEMORY APPLICATIONS. Julie D. Casperson, Harry A. Atwater, California Institute of Technology, Watson Laboratory of Applied Physics, Pasadena, CA; L. Douglas Bell, Jet Propulsion Laboratory, Pasadena, CA; Brett W. Busch, Lalita Manchanda, Martin L. Green, Agere Systems, Murray Hill, NJ.

Among the main performance limitations of floating gate nonvolatile memory devices, such as flash memories and nanocrystal memories, are the long program time ($\sim$1 μs) and erase time ($\sim$1 ms) achievable via a Fowler-Nordheim tunneling mechanism for charging of the floating gate through a homogeneous tunnel barrier. An interesting alternative to homogeneous dielectric tunnel barriers is a silicon compatible layered tunnel barrier, which enables a large drop in the barrier height with applied voltage.
To assess the performance of layered tunnel barriers, we have performed simulations and experiments with heterostructure amorphous dielectrics on Si(100). Tunneling probability simulations for layered tunnel barriers have been performed using an effective-mass model. By numerically integrating over all angles and energies, we naturally include a wide range of possible transport mechanisms such as thermionic emission, Fowler-Nordheim tunneling, and tunneling through the Schottky barrier of the silicon. Within this model, transmission is calculated exactly using numerical methods allowing for analysis of resonant tunneling effects and localized charge densities in potential minima.
Using this model we have calculated the current-voltage (I-V) characteristics so that we can optimize the layered tunnel structure. Ideally we would like the ratio of the current density at some maximum voltage to the current density at some minimum voltage to be at least as large as 10^{18} to correspond to a device with a retention time of at least 30 years and a programming time of about 1 nanosecond. Using this model we have investigated the different transport mechanisms as a function of layer thickness in order to optimize the tunnel barrier structure for a thin middle barrier we expect an appreciable direct tunneling current, and for a thicker structure we expect thermionic emission to dominate.
Several specific layer barrier structures have been investigated including Si_3N_4 / Al_2O_3 / Si_3N_4 and $ZrSiO_4$ / Al_2O_3 / $ZrSiO_4$. We have performed calculations on a 6 nm Si_3N_4 / 6 nm Al_2O_3 / 6 nm Si_3N_4 / n-Si dielectric heterostructure with assumed conduction band offsets with respect to the Si conduction band of 2.4 eV and 2.8 eV for the Si_3N_4 and Al_2O_3 layers, respectively. We have also modeled an identical structure on p-type silicon where the valence band offsets are 1.8 eV and 4.9 eV respectively. For these structures, the tunneling probability varies much more rapidly with applied bias than for a homogeneous barrier that is dominated by Fowler-Nordheim tunneling. For example, a change in applied bias for the described 3-layer structure from 0 eV to 2.5 eV on p-type silicon yields a theoretical change in tunneling probability by 19 orders of magnitude compared with only 8 orders of magnitude obtainable with a single 6 nm Al_2O_3 layer.
We have fabricated the layered barrier structures Si_3N_4 / Al_2O_3 / Si_3N_4. The Si_3N_4 was made by low-pressure chemical vapor deposition, and the Al_2O_3 was made by physical vapor deposition and atomic layer deposition. We have also fabricated single-layer barriers of Al_2O_3 and double barriers of Si_3N_4 / Al_2O_3. A comparison of the current-voltage and capacitance-voltage characteristics of these two structures will be discussed as well as the structural characterization.

SESSION A8: POSTER SESSION
NANOSTRUCTURES
Chair: Yasuo Takahashi
Tuesday Evening, November 27, 2001
8:00 PM
Exhibition Hall D (Hynes)

A8.1
Abstract Withdrawn.

A8.2
Abstract Withdrawn.

A8.3
WHITE LIGHT LUMINESCENCE FROM ZnS DOPED POROUS SILICON. K.W. Cheah[a], Ling Xu[a,b] and Xinfan Huang[b], [a]Department of Physics, Hong Kong Baptist University, Kowloon Tong, HONG KONG; [b]State Key Laboratory of Solid State Microstructure and Department of Physics, Nanjing University, Nanjing, CHINA.

Nano-ZnS was deposited into porous silicon. By varying the concentration of the nano-ZnS solution, the deposition rate can be controlled. The doped porous silicon exhibited a distinct shift in its photoluminescence spectrum. With appropriate deposition, it is possible to shift the photoluminescence spectrum from red to blue, and at an optimum doping, white light photoluminescence was obtained. Photoluminescence excitation spectrum showed that there was a clear excitation band due to ZnS existed in the ultra-violet region. Luminescence lifetimes of undoped porous silicon, nano-ZnS, and doped porous silicon were measured. The luminescence lifetime showed that radiative recombination center of nano-ZnS dominated decay at near ultra violet, whereas decay in the red region was still dominated by porous silicon. Nevertheless, the porous silicon surface radiative recombination was effective quenched by the deposition, and no longer active in the doped porous silicon. The result demonstrates that luminescence color tuning is possible using nano-ZnS doped into porous silicon.

A8.4
MATERIALS ISSUES IN Si/SiGe QUANTUM CASCADE STRUCTURES. T. Roch, M. Meduna, J. Stangl, T. Fromherz, G. Bauer, Physics Dept., University of Linz, AUSTRIA; G. Dehlinger, L. Diehl, U. Gennser, D. Gruetzmacher, LMN-PSI, SWITZERLAND.

Si/SiGe based quantum cascade (QC) emission structures exhibiting well resolved electroluminescence at about 125 meV involving heavy hole intersubband transitions have been reported recently (Dehlinger et al. Science 290,2277 (2001)). In order to improve their emission properties we have designed, grown and studied several quantum cascade structures with overall thicknesses of about 900 nm and Ge contents in the SiGe wells of more than 40%. In the SiGe QC emission devices the active region consists of an injector, the active quantum wells and the collector, which is repeated four times and forms one QC block. The entire structure consists of four such QC blocks. Graded SiGe layers and 1000$\AA$ thick Si spacer layers were introduced to reduce the average Ge content to about 10% to avoid plastic reelaxation. Using x-ray diffraction (XRD) scans and reciprocal space maps we show that such structures can be grown completely pseudomorphic on (001) Si at 350°C. With XRD maps we probe the entire layer stack and a sample area of several mm^2 is illuminated. Our results prove together with TEM investigations the absence of extended defects. From specular x-ray reflectivity scans (dynamic range >8 orders of magnitude) and reflectivity reciprocal space maps we determine that the entire system of QC stacks exhibits negligible thickness fluctuations, an rms interface rouhgness which increases from $2\AA$ at the first interface only to $2.8\AA$ the top of the entire cascade structure. From the resonant diffuse scattering in the reflectivity reciprocal space maps and their simulation we deduce that the interface morphologies within one cascade block are vertically correlated.

A8.5
SIZE AND SURFACE-DEPENDENT ELECTRICAL TRANSPORT IN SILICON NANOWIRES. Lincoln J. Lauhon, Yi Cui, Charles M. Lieber, Harvard University, Department of Chemistry and Chemical Biology, Cambridge, MA.

The future of electronics continues to lie in miniaturization, and semiconductor nanowires are emerging as a viable technology for nanoscale interconnects and devices. A key concern of nanoscale devices, regardless of fabrication method, is the increasing dominance of interfacial over bulk properties in determining device performance. In particular, the potentially deleterious consequences of surface scattering and interfacial trapping need to be addressed. We have studied the size dependence of the field effect mobility in n and p-type silicon nanowires grown by nanoparticle-catalyzed chemical vapor deposition. We have measured mobilities comparable to and even exceeding bulk values for wire diameters as small as 5 nm. These findings demonstrate the viability of using ultrasmall silicon nanowires as interconnects. In addition, the wire conductance is found to be highly sensitive to the state of the surface oxide. Chemical functionalization of this oxide may therefore be used to (1) mitigate environmental effects for utilization as interconnects; (2) rationally tailor the response to build environmental sensor functionality into the wire itself. The ultimate sensitivity limits of the smallest nanowire sensors will be discussed.

A8.6
PHOTOLUMINESCENCE OF Si-SiC HETEROSTRUCTURES AND QUANTUM DOTS. E. Ribeiro, Laboratorio Nacional de Luz Sincrotron, Campinas, SP, BRAZIL; E.F. da Silva Jr., Departamento de Fisica, Universidade Federal de Pernambuco, Recife, PE, BRAZIL; V.N. Freire, V. Lemos, Departamento de Fisica, Universidade Federal de Fortaleza, Fortaleza - CE, BRAZIL; Y. Ikoma, F. Watanabe, T. Motooka, Department of Materials Science and Engineering, Kyushu University, Hakozaki, Fukuoka, JAPAN.

SiC is an important semiconductor material for the fabrication of high-power electronic devices, designed to work at elevated temperatures and pressures. The cubic silicon carbide, 3C-SiC, was found to be the only polytype which can be epitaxially grown on Si (001) substrate. Several studies report on the growth of 3C-SiC on Si substrates but just a few have successfully achieved the reverse epitaxial growth of Si on 3C-SiC. This makes it possible to fabricate Si-based quantum devices, such as tunneling diodes, using very thin 3C-SiC films as electron barriers [1]. Due to the lattice mismatch between 3C-SiC and Si, it is possible to obtain Si quantum dots embedded into 3C-SiC, which could be useful for developing light-emitters devices and Si-based lasers. We present low-temperature photoluminescence (PL) of a thin film of 3C-SiC grown on Si (100) substrate, capped with Si (sample 1), and of Si quantum dots embedded in 3C-SiC (sample 2). The 3C-SiC layer was grown by the pulsed supersonic free jets method [1]. PL emission of sample 1 is shifted to lower energies compared to the bulk 3C-SiC, due to the tensile strain. Considering the experimental values for the bulk 3C-SiC exciton and for its elastic constants, together with theoretical predictions for the deformation potentials, we determined the residual tensile strain in the 3C-SiC layer to be 2.7% (strongly relaxed). For sample 2, the PL peak is broader and also shifted to lower energies, again indicating the presence of a tensile strain. To evaluate the strain in this situation, it would be necessary to develop a model considering the shape of the 3C-SiC capping layer, and how the film under the dots respond to this effect. [1] Y. Ikoma, T. Endo, F. Watanabe and T. Motooka, Appl. Phys. Lett. 75, 3977 (1999).

A8.7
QUANTUM CONFINEMENT ON THE VIBRATIONAL PROPERTIES OF SILICON NANOWIRES. C.K.A. Adu, S. Bhattacharyya, and P.C. Eklund, Dept. of Physics, Pennsylvania State University, University Park, PA; J.E. Fischer, Department of Material Science and Engineering and Laboratory for Research on the Structure of Matter, University of Pennsylvania.

We present results of Raman spectroscopy (RS) and Photo-luminescence (PL) on silicon nanowires prepared by pulse laser vaporization of hot targets in an inert atmosphere. Targets of Si:1% Au, Si:1%Fe and Si:1%Ni were used to produce crystalline Si nanowires in the diameter range 5-15 nm and with lengths exceeding 10μm. The materials were observed to be highly crystalline via the observation of well defined, periodic HRTEM fringes extending over long distances. A large redshift, up to 25 cm^{-1}, of the first order Raman-active transverse optical phonon compared to bulk silicon has been observed along with an increase of line width of $\sim$30 cm^{-1}. The asymmetric lineshape is analyzed in terms of the TO phonon branch dispersion and the range of allowed q vectors activated by quantum confinement. This signature of strong phonon confinement in the wires is supported by our PL emission data in the red region (1.61 eV) where, a blue shift is observed relative to buck Si. This work was supported by NSF MRSEC (UPenn)

A8.8
C-V AND G-V MEASUREMENTS SHOWING SINGLE ELECTRON TRAPPING IN NANOCRYSTALLINE SILICON DOT EMBEDDED IN MOS MEMORY STRUCTURE. Shaoyun Huang, Souri Banerjee, Shunri Oda, Tokyo Institute of Technology, Research Center for Quantum Effect Electronics, Tokyo, JAPAN.

The mechanism of single electron trapping in nanocrystalline silicon (nc-Si) dot has recently attracted great interest for further understanding the single electron memory (SEM) device performance [1]. Fast write/erase and long charge retention time, which are strongly influenced by the barrier and interface states, are major concerns. Capacitance-Voltage (C-V) and Conductance-Voltage (G-V) measurements are useful tools to study semiconductor interfaces and charge trap mechanism as well as the charge storage behavior in nanostructures. The SiO_2/nc-Si/SiO_2 sandwich Metal-Oxide-Semiconductor (MOS) diode has been prepared on $<100>$ n-type silicon wafer with an ultra-thin SiO_2 layer of 2 nm in thickness. The remote PECVD method is employed to fabricate nc-Si dots of 8 nm in diameter [2]. The dots thus prepared have a narrow spread and a density of about 10^{11} cm^{-2}. A comparatively thicker upper oxide was deposited by TEOS PECVD technique. The C-V and G-V characteristics were obtained by sweeping the voltage up and down between inversion and accumulation region. Clockwise hysteresis in both C-V and G-V characteristics were observed. Notable in the G-V curve is the presence of a peak, close to the flat band voltage, in each forward and backward measurement, indicating that a trap event has occurred. In contrast, neither any obvious hysteresis in C-V nor a peak in G-V characteristics was observed in the samples without dots. The results of C-V associated with G-V indicate a single electron trapping per nc-Si dot leading to a clear memory effect. In the time dependent capacitance measurement, a memory retention time exceeding 10^3 s was confirmed in this memory device. The charge storage mechanism in such a memory device will be discussed in detail. [1]. B.J. Hinds et. al. Mater. Res. Soc., 2000 Fall Mtg. F2.2, Proceedings 638 in press [2]. T. Ifuku et. al. Jan. J. Appl. Phys. 36 (1997) 4031.

A8.9
ELECTRICAL CHARACTERIZATION OF CARRIER CONFINEMENT AND THERMALIZATION IN Si/SiGe NANOSTRUCTURES. F.S. Flack, D.E. Savage, P. Rugheimer, K.A. Slinker, M.A. Eriksson, M.G. Lagally, University of Wisconsin-Madison, Madison, WI; Y. Zhao, Keithley Instruments, Cleveland, OH.

Semiconductor quantum dots have been studied intensely because of their potential for nanoelectronic or optoelectronic devices. In particular, understanding of the transport properties of SiGe-based quantum dots is increasingly vital, as applications are seen in devices such as integrated electronic memories and IR detectors. To design these structures, fundamental quantities, such as the carrier energy

levels, band offsets, and Coulomb charging effects, are needed. We report here the results of space charge spectroscopy of ensembles of SiGe quantum dots grown using UHV-CVD. The quantum dot ensembles were grown, with densities ranging from 10^9 to 10^{11} cm^{-2} and lateral sizes from 15 nm to 70 nm, in the neutral region of Schottky diodes on highly p-doped wafers. Admittance spectroscopy was performed at frequencies ranging from 10 kHz to 1 MHz and temperatures from 20K to 300K. Changing the applied bias sweeps the Fermi level through the dot's energy levels, allowing direct modification of the diode's conductance. Energy levels within the dots are then calculated using the equivalent parallel circuit model. We compare these results to carrier emission from regions of lateral confinement created by local stressors on a SiGe quantum well. We use a buried ensemble of quantum dots as the stressors. By varying the thickness of the Si spacer layer separating the dots and the well, we can controllably adjust the "depth" of the strain-induced quantum dots (SIQDs) while maintaining the precise control of thickness and compostion in the quantum well. Research supported by AFOSR and NSF

SESSION A9: ADVANCED CMOS GATE STACKS AND METALLIZATION
Chair: William G. En
Wednesday Morning, November 28, 2001
Room 202 (Hynes)

8:45 AM A9.1
EVALUATION OF CANDIDATE METALS FOR DUAL-METAL GATE CMOS USING HIGH-K GATE DIELECTRICS.
Srikanth B. Samvedam, J.K. Schaeffer, D.C. Gilmer, P.J. Tobin, J. Mogab, B. Cheng, K.G. Reid, B.-Y. Nguyen, M.V. Raymond, R.S. Rai, O. Adetutu, Z.-X. Jiang, L.B. La and J.A. Smith, Motorola, Digital DNA Laboratories, Austin, TX; R.B. Gregory, Motorola, Digital DNA Laboratories, Mesa, AZ; S. Dakshinamurthy, AMD-Motorola Alliance, Austin, TX.

As the MOSFET gate lengths are scaled down to 50 nm or below, the expected increase in gate leakage will be countered by the use of a high dielectric constant (high K) material. The series capacitance from polysilicon gate electrode depletion becomes a significant fraction of the actual capacitance from the gate dielectric as the dielectric thickness is scaled down to 15 $\AA$ equivalent oxide thickness (EOT) or below. Metal gates promise to solve this problem and address other issues like boron penetration and increased gate resistance that will have increased focus as the polysilicon gate electrode dimensions are scaled down further. Extensive simulations have shown that the optimal gate work-functions for the sub-50 nm channel lengths should be 0.2 eV below (above) the conduction (valence) band edge of silicon for n-MOSFETs (p-MOSFETs). In addition to the work-function requirements, the metal gate and the high-k gate dielectric should be mutually compatible and not inter-diffuse or react at the MOSFET thermal budget. This study summarizes the evaluations of TiN, TaSiN, WN and TaN as candidate metals for dual-metal gate CMOS using HfO_2 as the gate dielectric. The gate work-functions and fixed charge induced was determined by fabricating MOS capacitors with varying dielectric thicknesses. The metal-dielectric compatibility and thermal stability was studied by annealing the capacitors at different temperatures. The gate stacks were characterized using TEM, SIMS and X-ray diffraction. Of the metals evaluated, TaSiN shows most promise as a candidate gate electrode for HfO_2 n-MOSFETs. None of metals studied have work-functions suitable for HfO_2 p-MOSFETs.

9:00 AM A9.2
INITIAL GROWTH OF SILICON GERMANIUM FILMS ON ZIRCONIUM OXIDE.
Dong-Won Kim, Freek E. Prins, Choong-Hoo Lee, Kil-Soo Ko, Dim-Lee Kwong and Sanjay Banerjee, Microelectronics Research Center, The University of Texas at Austin, Austin, TX.

Recent efforts on scaling silicon dioxide in standard complementary metal-oxide-semiconductor (CMOS) technology have focused on alternate gate dielectric materials themselves. However, most high-K dielectric materials are not thermally stable in direct contact with silicon. An interface layer between the high-K dielectric materials, Si substrate and Si poly gate is necessary to prevent the interface reaction. Therefore the investigation of alternative gate electrode materials is desirable. Polycrystalline silicon-germanium (poly-SiGe) has recently been shown to be a potential alternative to polycrystalline silicon (poly-Si) for advanced submicron devices. The advantages of poly-SiGe over poly-Si include low process temperature, low activation energy of dopant, more appropriate gate work function and high carrier mobility. However, the initial stages of the SiGe film formation and nucleation which are known to control the film structure and hence film properties are not clearly understand. In this study, the initial growth characteristics of a SiGe film realized by ultrahigh-vacuum chemical vapor deposition (UHV CVD) using GeH_4 and disilane on high-K gate oxide, ZrO_2, has been investigated within the temperature range from 475°C to 550°C. The influence of the surface reaction on growth characteristics such as the incubation of growth, roughness distribution of SiGe, and the interface reaction of the SiGe film with ZrO_2 are specially focused on. For this purpose, atomic force microscopy (AFM), Auger electron spectroscopy (AES), X-ray photoelectron spectroscopy (XPS) and transmission electron microscopy (TEM) were used. From our analysis we conclude that ZrO_2 reacts with Si and forms zirconium silicide in the temperature range between 500°C and 550°C. The surface roughness of amorphous SiGe layers increase from 0.5nm to 1.5nm with increasing Ge content from 0.1 to 0.3. A further increase of surface roughness is observed from less than 1nm to 5nm as SiGe layer transition from amorphous to poly crystalline layer.

9:15 AM A9.3
STRUCTURE AND STABILITY OF ALTERNATIVE HIGH-K DIELECTRICS ON SILICON.
S. Stemmer, Department of Mechanical Engineering and Materials Science, Rice University, Houston, TX; D. Wicaksana, J.-P. Maria and A.I. Kingon, Department of Materials Science and Engineering, North Carolina State University, Raleigh, NC.

Technology roadmaps predict that continued scaling of complementary metal-oxide-semiconductor devices would eventually require a gate dielectric with a capacitance equivalent to that of SiO_2 of less than 1.5 nm thickness, a thickness regime where tunneling currents become unacceptably high for many applications. Replacing SiO_2 with a material with a higher dielectric constant (k) would allow physically thicker films to achieve the required capacitance values. Two important issues are the thermal stability of the alternative gate dielectric on silicon and the electrical quality of the interface. To investigate these issues a microstructural characterization method is required that not only images gate stacks but that can also analyze the composition and electronic structure with atomic spatial resolution. Here we use electron energy-loss spectroscopy (EELS) in transmission electron microscopy with a sub 0.2 nm probe. We have investigated $La_2O_3/SiO_2/Si$ and $ZrO_2/SiO_2/Si$ structures with well-characterized electrical and dielectric properties before and after rapid thermal annealing (RTA) at different temperatures and oxygen partial pressures. Results show that after RTA at 600°C, a La_2O_3 layer on a thermal SiO_2 remained amorphous. After 800°C RTA, crystallites appeared in the original La_2O_3 layer, and the total oxide layer thickness increased by 17%, most likely due to oxygen diffusion and reaction at the Si/SiO_2 interface. EELS showed that RTA at 600°C did not cause significant La diffusion into the SiO_2 layer, whereas some intermixing was observed at 800°C. Equivalent oxide thicknesses (EOT) estimated from the microstructures are found to closely correspond to results from capacitance-voltage measurements. For example, a La_2O_3 layer grown on a chemical SiO2 and subjected to RTA at 1000°C showed an EOT of 1.8 nm. We investigate the interfacial composition of $ZrO_2/SiO_2/Si$ structures, and quantify the amount of interfacial SiO_2-ZrO_2-silicate of samples annealed under four different annealing atmospheres. Results of EELS fine-structure analysis of interfaces will be presented and provide an understanding of the electrical and dielectric behavior of the films.

9:30 AM A9.4
STOICHIOMETRY OF SILICON NITRIDE FILMS: A COMPARISON OF UV/VIS SPECTROMETRY WITH SPECTROSCOPIC ELLIPSOMETRY AND RUTHERFORD BACKSCATTERING SPECTROSCOPY.
C.S. Cook, N.V. Edwards, Stefan Zollner, R.B. Gregory, Erika Duda, Dennis Werho, H.G. Tompkins, Motorola Process and Materials Characterization Lab, Mesa, AZ.

Silicon nitrides are commonly used in microelectronic applications where achieving a targeted stoichiometry is crucial for successful operation of the device. For example, antireflective coatings in photolithography, gate dielectrics, and final passivation require either silicon rich, nitrogen rich, or stoichiometric SiN films. Stoichiometry is primarily determined by Rutherford Backscattering Spectroscopy (RBS), because it requires no standard. However, RBS is not a viable option for quick, in-line measurements. This work focuses on the film stoichiometry determined by spectroscopic ellipsometry (SE), a nondestructive and suitable in-line technique, in which the Tauc Gap (E_T) is related to composition. Measurements were performed on a set of films whose nitrogen ratios range from 38% to 56%, as determined by RBS. Ellipsometric angles ψ and Δ were obtained from 190 to 1600 nm on a J.A. Woollam variable angle spectroscopic ellipsometer (VASE) with a compensator. The data was modeled with a Tauc-Lorentz oscillator model and the optical properties n and k were calculated from the fitted data. Determining n and k from SE allows us to calculate the cutoff wavelength where α=3679 cm^{-1}, which was correlated by Rand and Wonsidler to the Si/N ratio determined by electron microprobe measurements. We compare the

cutoff wavelengths determined by a commercial Hewlett-Packard UV/VIS spectrometer and our ellipsometer. We also compare the stoichiometry determined from (1) the cut-off wavelength, (2) directly measured by our RBS analysis, and (3) the Tauc gap using Jellison's correlation between the Tauc gap and the stoichiometry.

9:45 AM A9.5
INTERFACIAL DIFFUSION STUDIES OF Hf AND Zr INTO Si FROM THERMALLY ANNEALED Hf AND Zr SILICATES.
M. Quevedo-Lopez, M. El-Bouanani, S. Addepalli, B.E. Gnade and R.M. Wallace, Department of Materials Science, University of North Texas, Denton, TX; L. Colombo, M. Bevan, M. Douglas, and M. Visokay, Si Technology Research, Texas Instruments Incorporated, Dallas, TX.

Thermal stability of alternate high-κ gate dielectrics on silicon is an important issue for future CMOS devices due to the fact that the dielectric must withstand the very short, but relatively high (~5-30 s @ 900-1100°C) dopant activation anneal temperatures. This high temperature annealing can result in undesirable properties including: interfacial layer growth, microstructural changes in the film, and possible metal outdiffusion from the gate dielectric into silicon[1]. $HfSi_xO_y$ and $ZrSi_xO_y$ are two of the promising high-k gate dielectric candidates which are expected to meet the requirements of the SIA technology roadmap[2-5] especially the need of less than 2.0 nm SiO_2 gate dielectric for sub-0.13 μm scaled silicon CMOS. However, the stability of the ([1] $HfSi_xO_y$, $ZrSi_xO_y$)/silicon interface following dopant activation annealing remains one of the most important issues to be solved. Any Zr or Hf metal diffusion into the channel is critical because impurity diffusion from the gate dielectric into the channel region would likely in deleterious effects on carrier mobility. Diffusion studies of Hf and Zr from high-k gate dielectric thin films (4-5 nm) candidates[1] $HfSi_xO_y$ and $ZrSi_xO_y$ into Si will be presented. Gate dielectric samples were subjected either to rapid thermal processing (RTP) or standard furnace annealing in an N_2 atmosphere. After annealing, the dielectric films were chemically etched prior to depth profiling using both ToF-SIMS and a combination of Heavy Ion Rutherford Backscattering Spectrometry (HI-RBS) UV-ozone oxidation/etching cycles. As-deposited and annealed films were studied using monochromatic X-ray Photoelectron Spectroscopy (XPS), High resolution TEM was used to determine any structural changes or growth of interfacial layers. Film deposition, chemical etching and characterization issues will be discussed. No significant Hf diffusion into Si was observed for both RTP and furnace-annealed films. The Zr diffusion into Si was more pronounced in both cases, when compared to Hf. Implications for high-κ gate dielectric applications are also discussed. This work was supported by the Texas Advanced Technology Program, the Semiconductor Research Corporation, and DARPA.
REFERENCES
[1] G.D. Wilk, R.M. Wallace and J.M. Anthony, J. Appl. Phys. 89, 5243 (2001) [2] G.D. Wilk and R.M. Wallace, Appl. Phys. Lett. 74, 2854 (1999). [3] G.D. Wilk and R.M. Wallace, Appl. Phys. Lett. 76, 112 (2000). [4] W.-J. Qi, R. Nieh, E. Dharmarajan, B.H. Lee, Y. Jeon, L. Kang, K. Onishi, and J.C. Lee, Appl. Phys. Lett. 77, 1704 (2000). [5] Semiconductor Industry Association roadmap 1999

10:30 AM A9.6
NEAR-ZERO-THICKNESS SELF-ASSEMBLED LAYERS FOR INTERFACIAL ISOLATION IN FUTURE DEVICE STRUCTURES.
G. Ramanath, M. Stukowski, G. Cui, and X. Guo, Rensselaer Polytechnic Institute, Dept of Materials Sci & Eng, Troy, NY; S. Nitta, IBM, Hopewell Junction, NY.

Tailoring ultrathin layers to inhibit interfacial interdiffusion and phase formation will be a critical factor in the fabrication of future Si-based microdevices, micro electromechanical systems (MEMS), and nanodevices. For instance, < 5-nm-thick diffusion barriers that can conformally coat sub-100-nm-diameter vias are necessary to fully realize the full potential of Cu-interconnect technology. In this talk, we demonstrate the use of <2 nm-thick self-assembled molecular layers (SAMs) as effective barriers to Cu diffusion into SiO_2 between 100-300°C in a 2 $MVcm^{-1}$ electrical field. Capacitance-voltage and current-voltage measurements of MOS capacitors with SAMs having aromatic terminal groups consistently show as much as *5 orders of magnitude lower leakage currents and a factor of 4 higher mean-time-to-failure* when compared with the corresponding values measured from uncoated samples. SAMs with short tail lengths or aliphatic terminal groups are ineffective in hindering Cu diffusion, suggesting that molecular length and chemical configuration are key factors in determining the efficacy of SAMs as barriers. We will also address the temperature dependence of the barrier properties, and preliminary results pertaining to their deposition and behavior on SiLK. The results will be discussed in the context of microelectronics device processing and integration, to evaluate the utility of ultrathin molecular layers in future microdevices and MEMS.

10:45 AM A9.7
POSITRON ANNIHILATION LIFETIME SPECTROSCOPY (PALS) APPLICATION IN METAL BARRIER LAYER INTEGRITY FOR POROUS LOW-K MATERIALS.
Simon Lin, Jia-Ning Sun[a], David W. Gidley[a], Jeffrey T. Wetzel, K.A. Monnig, Simon Jang[b], Douglas Yu[b] and M.S. Liang[b], International SEMATECH, Austin, TX; [a] Department of Physics, University of Michigan, Ann Arbor, MI; [b] Taiwan Semiconductor Manufacturing Co, HsinChu, TAIWAN, ROC.

Cu and low-k dielectric are both applied in the damascene integration in order to reduce RC delay so as to increase the device speed. As dielectric constant (k) is needed less than 2.2 for the 0.1 mm technology as shown in the ITRS roadmap, porous instead of dense low-k is the only way to achieve the goal from the present suppliers. Application of porous low-k into integration introduces the problems of metal barrier integrity on trench sidewall, which is never been encountered from dense low-k before. As the dimension shrinks, the barrier layer thickness needs reduction as shown in the ITRS roadmap, which also complicates the barrier integrity problems. In this paper, PALS is introduced to evaluate barrier layer integrity in the early stage. The correlation between PALS screening and single damascene integration for various Silica-based low-k results is presented. The criterion to achieve good barrier integrity between the barrier thickness and the pore sizes is also discussed. The paper demonstrates that PALS is a useful tool to pre-screen metal barrier integrity for porous low-k dielectrics. Large scale meso-porous (> 50A) low-k will encounter Cu diffusion problems when using SEMATECH in-house PVD Ta 250A as barrier layer for trench dimension smaller than 0.25 mm. Positronium (Ps) leakage is correlative to bridge current leakage in the electrical tests and pin-holes in the barrier layer. For small scale meso- (20 - 50A) and micro-porous (< 20A) low-k, no Cu diffusion was observed even with Ta 50A as the barrier layer, which is contributed from sidewall densification to close up pores after etch and ash. No Ps leakage from pattern wafer by PALS is also correlated to electrical data and cross section images. Therefore, smaller pore size of porous low-k (< 50A) will be preferential for future technology.

11:00 AM A9.8
DIFFUSION CHARACTERISTICS OF COPPER IN TiN THIN FILMS.
Abhishek Gupta, Alex V. Kvit, T.K. Nath and J. Narayan, NSF Center for Advanced Materials and Smart Structures Department of Materials Science and Engineering, NCSU, Raleigh, NC.

We have investigated the diffusion characteristics of copper in nanocrystalline, polycrystalline and single crystal TiN thin films, which is being used as a diffusion barrier for sub-quarter-micron metallization. These films were synthesized on Si < 100 > substrate by first ablating amorphous TiN and then ablating amorphous copper targets using Pulse Laser Deposition. The three different crystal structures of TiN were achieved by growing the films at different substrate temperatures, where higher temperatures (~650°C) leads towards epitaxy. Then a uniform thin layer of copper was deposited at room temperature for all the three depositions above. Each sample is annealed at three different temperatures (400°C, 500°C and 600°C) to study the diffusion barrier characteristics of TiN. Study of diffusion profile and the copper concentration measurement were performed using Scanning Transmission Electron Microscopy-Z contrast (0.16nm resolution), Secondary Ion Mass Spectroscopy, Electron Energy Loss Spectroscopy and Rutherford Backscattering Spectroscopy techniques. These data were used to plot the measured concentration of copper with respect to the temperatures for the three crystal structures of TiN to calculate the diffusion coefficients and were compared to study the effect of microstructure of TiN thin film on the diffusion of copper after annealing.

11:15 AM A9.9
Mg EFFECTS ON AGGLOMERATION, ADHESION, RESISTIVITY OF Ag(Mg)/SiO_2/Si MULTILAYERS.
Bongjoo Kang, Yeonkyu Ko, Heejung Yang, Jaegab Lee, Kookmin Univ, School of Metallurgical and Materials Engineering, Seoul, KOREA; ChangOh Jeong, Samsung Electronics Ltd, AMLCD Division, KOREA.

Ag has received attentions as a potential interconnection in ultra-large scale integration and large area TFT/LCDs because it shows the lowest resistivity among metals and high electromigration resistance. However, several issues such as agglomeration, poor adhesion to SiO_2 have to be addressed to implement Ag metallizations into integrated circuits and TFT/LCDs as well. The effects of Mg in Ag(Mg)/SiO_2/Si multilayers on adhesion, passivation, and resistivity after annealing in an vacuum at 200°C to 500°C have been investigated. Heating Ag(Mg)/SiO_2/Si multilayer films above 300°C produced surface and interfacial MgO layers, resulting in MgO/Ag/MgO/SiO_2/Si structure. The presence of surface MgO improved the mechanical properties such as higher strength, better resistance to diffusional flow and also provided the passivation layer against air, thus leading to the significant enhanced resistance to agglomeration. In addition, adhesion was remarkably improved due to

the formation of interfacial MgO resulting from the reaction of Mg with SiO_2. However, the interfacial reaction proceeded to a limited extent because free silicon generated from the reaction has the negligible solubility into Ag. This limited interfacial reaction between Mg and SiO_2 in Ag(Mg)/SiO_2 is contrasted with the unlimited interfacial reaction occurring in Cu(Mg)/SiO_2. The resistivity of Ag(4.5at.% Mg) continued to decrease with increasing the temperature and was 2.6 $\mu\Omega$·cm after heating at 500°C.

11:30 AM A9.10
TEXTURE DEVELOPMENT IN Ti-Ta ALLOY DISILICIDE FILMS. A.S. Ozcan, K.F. Ludwig, Jr., Boston University, Dept. of Physics, Boston, MA; C. Lavoie, C. Cabral, Jr., J.M.E. Harper, IBM Research Division, Yorktown Heights, NY.

The development of texture in blanket Ti-Ta(0-6 at.%) disilicide films has been studied both in-situ and ex-situ with x-ray diffraction. For pure Ti films on Si(001) substrates, the C49 TiSi2 phase develops with (131) poles primarily in the film plane. The final C54 TiSi2 texture is dominated by orientations with C54(110) and C54(-110) parallel to Si(111). This suggests that ledging (local facetting) on Si(111) planes may play an important role in the C54 formation. The addition of Ta causes a change in textures with C54(010) becoming the dominant orientation normal to the substrate. This texture change becomes complete with the addition of 6 at.% Ta, which is an effective alloy composition for the reduction of the C54 formation temperature. On Si(001) substrates, there is also an in-plane preferential orientation with C54(011) || Si(110). In-situ studies show that the C54 texture can evolve during the C54 formation process, possibly because those grains with the most favorable orientation relative to the substrate have the highest growth velocity. This work has been partially supported by NSF-ECS 9515181.

SESSION A10: POSTER SESSION
ADVANCED CMOS GATE STACKS AND METALLIZATION
Wednesday Evening, November 28, 2001
8:00 PM
Exhibition Hall D (Hynes)

A10.1
Abstract Withdrawn.

A10.2
SYNTHESIS OF TITANIUM SILICATE ($Ti_xSi_yO_2$) AS A HIGH-k DIELECTRIC MATERIAL BY O_2 IMPLANTATION INTO TITANIUM SILICIDE ($TiSi_2$) FILM. D.K. Sarkar, E. Desbiens, R.W. Paynter and B.L. Stansfield, INRS-Materials and Energy, Varennes, Quebec, CANADA.

Recently, a great deal of attention has been paid to finding an alternative gate dielectric material as a substitute for SiO_2 in future MOSFET devices due to the expected leakage current through an ultra-thin SiO_2 layer. The dielectric constant of SiO_2 is 3.9, which is very low, while that of TiO_2 is 80 which is too high for future applications. We have attempted to synthesize titanium silicate, which should have a dielectric constant between that of SiO_2 and TiO_2, by implanting O_2 into titanium silicide. The titanium silicide film was grown on a crystalline Si(100) substrate by rapid thermal annealing (RTA) of a 20 nm Ti film at 800°C. The sheet resistance of the silicide film is 0.98 Ω/□. An XPS depth profile shows that the stoichiometry of the film is $TiSi_2$. O_2 was implanted in the silicide film by means of a plasma ion implanter with an energy of 15 keV and a dose of $\sim 5\times10^{17}$ ions/cm^2. An XPS depth profile has also been obtained from the O_2 implanted silicide film. The surface of the O_2-implanted silicide film is contaminated with TiO_2 and SiO_2 as confirmed by the binding energy of the Ti $2p_{3/2}$ peak (459.0 eV), Si 2p (103.5 eV) and O 1s (530.4 and 532.2 eV). After sputtering for 300 seconds (~5 nm), a Ti $2p_{3/2}$ peak appears at 459.6 eV, a Si 2p component at 102 eV and a O 1s peak appears at 531 eV. The binding energy of the Ti $2p_{3/2}$ peak therefore increases while that of Si 2p is reduced in the O_2-implanted silicide as compared to their oxide states; this is characteristic of silicate materials. The dielectric constant of the O_2 implanted silicide film is estimated by measuring the I-V characteristics and fitting the data using the Schottky emission model; and the value obtained is about 30.

A10.3
BOROPHOSPHOSILICATE GLASSES FOR SILICON DEVICES: SOL-GEL SYNTHESIS AND SPECTROSCOPIC CHARACTERIZATION. Carmen Canevali, Franca Morazzoni, Roberto Scotti, Anna Vedda, Giorgio Spinolo, Universitá di Milano-Bicocca, Dipartimento di Scienza dei Materiali, Milano, ITALY.

Borophosphosilicate glasses (BPSG) thin films are used in semiconductor manufacturing for insulation between metal interconnections and silicide gate structures because of their low flow temperature and strong ability to getter Na^+ impurities. These glass film properties depend on the elemental composition. In order to understand the dependence of glass properties on composition, the preparation of BPSG monoliths at different B and P concentrations has been pursued by the sol-gel method. The sol-gel method allows to prepare glasses with a high degree of homogeneity and purity. BPSG have been prepared so far as powders [1] or as monoliths from aerogels [2], but this is the first time that bulk transparent glasses free of cracks were obtained from xerogels. Xerogels were prepared by hydrolysis and condensation in water/methanol of $Si(OCH_3)_4$, $B(OCH_3)_3$ and $P(OCH_3)_3$. Boron and phosphorous contents in the range 0-12 molar percentage were considered. The densification of xerogels to glasses was performed by a thermal treatment at 973 K in flowing oxygen alternated to reduced oxygen pressure in order to burn residual carbon, to eliminate solvents and to avoid glass cracking. Glass formation was followed by infrared and Raman spectroscopies. Radiation-induced point defects were investigated by optical absorption and electron paramagnetic resonance (EPR) spectroscopy. Phosphorous-oxygen-hole centers (POHC) [3], boron-oxygen-hole centers (BOHC) [4] and Si-E′ centers were identified, to be correlated with the Na^+ getting ability. [1] J.Y. Kim and P.N. Kumta, J. Phys. Chem. B, 102 (1998) 5744-5753. [2] T. Woignier, J. Phalippou and J. Zarzycki, J. Non-Crystalline Solids, 63 (1984) 117-130. [3] D.L. Griscom et al., J. Appl. Phys., 54 (1983) 3743-3761. [4] W.L. Warren et al., Appl. Phys. Lett., 67 (1995) 995-997.

A10.4
PROCESS - STRUCTURE - FUNCTION RELATIONSHIPS OF NITRIDED OXIDES AND OXYNITRIDES. Anindya Dasgupta and Christos G. Takoudis, University of Illinois at Chicago, Department of Chemical Engineering, Chicago, IL.

Thermally grown Si_3N_4 films in NH_3 are known to have a higher dielectric constant and a higher N concentration than silicon oxides/oxynitrides, but they incorporate H atoms that induce hot electron carriers during subsequent high temperature processing. Further, silicon nitride is difficult to grow over 6 nm thick, due to self-limiting growth. One alternative is SiO_2 and SiN_yO_z films post-nitrided with NH_3.
In this work we study the different bonding states in nitrided oxide and oxynitride films with X-ray photoelectron spectroscopy (XPS) and Fourier transform infrared (FTIR) spectroscopy as well as process-structure relationships in ambient containing NO, N_2O or O_2 at 1000°C. Critical parameters of interest also include the N and O concentration profiles in nano-scale novel dielectric films and how those profiles change in different processing environments. Experimental data suggests that the presence of N at different positions within the dielectric films imparts distinct advantages like retarding Boron penetration when present near the dielectric surface or better strain relaxation when present near the dielectric/substrate interface.
The detailed concentration profiles of N, O and Si within the dielectric layer with different sputtering times obtained by secondary ion mass spectrometry coupled with the binding energies and bonding states at different depths through our FTIR and XP Spectroscopic studies will be shown to be essential in designing nano-dielectrics with desired N concentration profiles and in understanding related process-structure-function relationships.

A10.5
FILM PROPERTIES OF HIGH-PERFORMANCE FSG FILMS. Takashi Yoda, Hideshi Miyajima, Keiji Fujita, Renpei Nakata, Yukio Nishiyama, Toshiba Corporation, Tokyo, JAPAN.

FSG films are widely used not only Al based Technology but also Cu/Damascene devices. Numerous FSG film studies describe the film quality deposited by the SiH_4 based PE-CVD and HDP-CVD, which the k-value of these studies is about 3.6-3.8. Nevertheless the requirement to improve circuit performance cannot satisfy these k-values. The k-value is linearly related to the in-film fluorine concentration. However excess fluorine atoms can attack Al and Cu wiring to cause resistance changes, poor adhesion to SiN and TaN, and also reliability problems. FSG film which meets the k-requirement ($k<3.5$) and pass these stability test is viable. In this study, we developed the advanced FSG film (k=3.4),which shows excellent film properties. The feature of new PE-CVD tool is as follows. Basically the chamber consists of parallel plate electrode, and the RF power is applied from the upper and lower electrode, 60MHz and 2MHz respectively. Furthermore FSG processes require a well controlled wafer temperature. The heating platen with ESC can easily control the wafer temperature during deposition. The advanced FSG film appears to be superior to the HDP-FSG film by a wide margin in the following tests. The moisture absorption test by TDS (after 4 days of air exposure); about 10X less. The hardness; 1.8X more. The hydroscopicity (after 1 hr. boiling); 3X less. These differences are

mainly due to the good water penetration resistance of the advanced FSG film. The results of RBS measurement show that Si-OH peak is about 4X less than HDP-CVD FSG film. These properties supposed to depend on the local structure of FSG films. Further investigations such as EXAFS spectra studies are in progress.

A10.6
Abstract Withdrawn.

A10.7
ALUMINUM OXIDE BASED THIN HIGH-K DIELECTRICS. Pallavi Katiyar, Alex V. Kvit, D. Kumar, J. Narayan, NSF Center for Advanced Materials and Smart Structures, NC A&T and N.C. State University, Burlington Labs, Raleigh, NC.

Conventional scaling of the SiO_2 gate oxide thickness, has enabled MOS gate dimensions to be reduced to 100 nm or less. We have successfully deposited stoichiometric aluminum oxide between room temperature and 500°C using a pulsed laser deposition technique. The thickness of the deposited oxide was varied from 1-100 nm. Microstructural as well as electrical measurements of aluminum oxide thin film was done in order to study the dielectric properties. The quality of the film was found to strongly depend on the laser and substrate parameters. The high- resolution transmission electron microscopy (HRTEM) and electron energy-loss spectroscopy (with a resolution of 0.16nm) was done to study the interfacial structure of the film. The HRTEM studies showed a sharp and uniform interface between Al_2O_3 thin film and the silicon (100) substrate. The electron energy-loss spectroscopy (EELS) studies showed the absence of any interposing SiO_2 layer. The high and low frequency Capacitance-Voltage (C-V) and current-voltage (I-V) measurements revealed low leakage current. These results show that Al_2O_3 films are suitable for high-k dielectrics to replace the conventional SiO_2 gate oxide.

A10.8
STRUCTURE AND CRYSTALLIZATION OF ULTRATHIN ZrO_2 AND Zr SILICATE FILMS. Debra L. Kaiser, Igor Levin, Charles Bouldin, Mark D. Vaudin, NIST, Ceramics Division, Gaithersburg, MD.

ZrO_2 and Zr silicate are leading materials for the replacement of SiO_2 gate dielectrics. We have studied the crystallization behavior, structure, and compositional homogeneity of Zr oxide and Zr silicate thin films using high resolution TEM, extended x-ray absorption fine structure (EXAFS) and grazing incidence x-ray diffraction. The films for these studies were fabricated in-house by a metalorganic spin coating technique and had thicknesses in the range 2.5 nm to 5 nm. The onset of crystallization in the ZrO_2 films occurred at about 500°C; the EXAFS results suggest the presence of two crystalline ZrO_2 phases above 500°C.

A10.9
THEORETICAL INVESTIGATION OF THE TUNNELING THROUGH A 1 NM MOS AND A DOUBLE BARRIER SiO_2-Si-SiO_2 STRUCTURES. A.A. Demkov and Xiaodong Zhang Physical Sciences Research Labs, Motorola, Inc., Tempe AZ.

We describe a consistent methodology to create structural models of the Si-dielectric interface with a realistic atomic geometry. To construct a Si-SiO_2 interface we use a direct quantum molecular dynamics oxidation of the Si (001) surface [1]. A similar approach is used to investigate the initial decomposition of NO on the Si surface. The resulting structures show the interfacial sub-oxide region that amounts to about 0.4 nm. We have constructed several structural models with the dielectric thickness ranging from 0.6 to 0.15 nm. These structures are similar to those of ultra small transistors described in a recent report from Bell Laboratories. In addition, we investigate silicon oxynitrides SiO_xN_y which are often observed in the interfacial regions e.g. between the oxide and the nitride. The International Technology Road Map for Semiconductors states that the scaling of CMOS devices will stop about the year 2012. The main reason for this is the leakage through the silicon dioxide gate with a thickness below 4 nm. The modification of the oxide layer to improve the dielectric constant coupled with the understanding of the microscopic nature of the leakage may extend the current materials technology for a few device generations, before we will ultimately have to switch to a high-k gate dielectric. We investigate the leakage current in ultra thin MOS structures and tunneling through SiO_2-Si-SiO_2 double barrier structures constructed using the interface models described above. The Landauer ballistic transport theory is used to model the conductance. We employ a t-matrix approach that does not use the effective mass approximation and is essentially exact within the LCAO formalism chosen here. In addition, we investigate the effects of the local atomic structure changes, caused by the presence of nitrogen at the interface, on the electric properties of this fundamental element of the CMOS technology. In summary, we are able to build atomistic models of the interfaces, capacitors and double barrier structures and go all the "way up" to estimate their transport properties. This is an example of the "bottom up" engineering, where a combination of the materials and quantum transport theories can make a real impact. 1. A.A. Demkov and O.F. Sankey, Physical Review Letters 83, 2038.

A10.10
A COMPARATIVE STUDY OF GADOLINIUM OXIDE, GALLIUM OXIDE AND YTTRIUM OXIDE AS HIGH-K GATE DIELECTRICS ON SiGe. S. Pal, S.K. Ray, Department of Physics and Meteorology, I.I.T Kharagpur, INDIA; B.R. Chakrabarti, National Physical Laboratory, New Delhi, INDIA; S.K. Lahiri, Department of Electronics and Electrical Communication Engineering, I.I.T Kharagpur, INDIA; D.N. Bose, Advanced Technology Center, I.I.T Kharagpur, INDIA.

Enhanced hole mobility and the compatibility of the strained SiGe material system with silicon have attracted considerable attention for applications in complementary metal-oxide-semiconductor (CMOS) technology. Conventional high temperature (>700°C) thermal oxidation for the growth of gate oxide is not suitable for strained $Si_{1-x}Ge_x$ layers as it causes strain relaxation and Ge segregation at the oxide-semiconductor interface. Thus the search for a suitable CMOS gate dielectric continues. We report here a comparative study of the electrical properties of some novel oxides e.g. Gd_2O_3, $Ga_2O_3(Gd_2O_3)$ deposited from GGG, Y_2O_3 and Ga_2O_3 as gate dielectrics for strained $Si_{1-x}Ge_x$ CMOS devices. Experiments were carried out on epitaxial layers of strained $Si_{0.74}Ge_{0.26}$($\sim$300$\AA$ thick) grown by ultra high vacuum chemical vapor deposition (UHVCVD) on an epitaxial Si-buffer layer (500 $\AA$) at 550°C on (100) p-Si (7-10Ω·cm) substrates using SiH_4 and GeH_4. The layers were boron doped in-situ at 1 - 2 $\times 10^{17}$ /cm^3. Secondary Ion Mass Spectrometry (SIMS) of the Ga_2O_3 (Gd_2O_3) / SiGe sample showed significant amount of GaO and GdO along with Ga and Gd signals.The depth profile taken for O, Si, SiO, Ga, Ge, Gd & GdO showed a sharp interface at about 20 nm. C-V and G-V measurements showed that though Gd_2O_3 and Y_2O_3 had highest resistivity and breakdown strength, Ga_2O_3 (Gd_2O_3) was found to be most effective for surface passivation of SiGe giving lowest interface state density. Pure Ga_2O_3 on the other hand was found to be incapable of passivating the SiGe surface. The positive fixed oxide charge and interface state density for $Ga_2O_3(Gd_2O_3)$ film were found to be 8.4 $\times 10^{10}$/cm^2 and 4.8 $\times 10^{11}$/eVcm^2 respectively which are the lowest among all the oxide films. Constant current stressing experiments showed all the oxides exhibited hole trapping during current injection through the gate.

A10.11
MODULATION OF THE AMORPHOUS STRUCTURE OF SiO_2 OVER Si(001). W. Donner, M. Castro-Colin, S.C. Moss, Dept of Physics, Houston, TX; R.J. Nemanich, Dept of Physics, North Carolina State, Raleigh, NC; Z. Islam, S.K. Sinha, APS ANL, Argonne, IL.

Using grazing incidence x-ray diffraction (GID), we find a fourfold modulation of the first sharp diffraction peak (FSDP) of the amorphous structure factor of SiO_2 over Si(001) in a 100 Å film grown by furnace oxidation. We propose a model for the SiO_2/Si interfacial structure in which the SiO_4 tetrahedra, which form the building blocks of the amorphous network, are locked into the diagonal of the Si surface unit mesh. The model is supported by X-ray Reflectivity measurements which reveal an intermediate interfacial layer with an enhanced density, which is confirmed by the radial position of the FSDP. In-plane measurements at reflections of the underlying Si lattice also show distinct effects of the SiO_2 layer, and the strain accompanying it. Research supported by the DOE on DE-FG03-87ER. We also wish to thank Hubert Zajonz at the NSLS, beamline X22C, for assistance with preliminary GID and reflectivity measurements on this sample. One of us (W.D.) is supported by a Feodor Lynen-Fellowship of the Alexander von Humboldt-Foundation.