SYMPOSIUM E

E: Fundamentals of Novel Oxide/Semiconductor Interfaces

December 1 - 4, 2003

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SESSION E1: Characterization of Novel Oxides on Silicon
Chair: Matt Copel
Monday Morning, December 1, 2003
Room 207 (Hynes)

8:30 AM *E1.1
Inelastic Electron Tunneling Spectroscopy (IETS) Study of HfO2/Si and HfAlO/Si. T.P. Ma and Wei He; Electrical Engineering, Yale University, New Haven, Connecticut.

High-K dielectrics must resolve many issues, such as thermal instability, high densities of oxide charge and traps, and interface traps, before any of them can replace SiO2 as the gate dielectric for future CMOS technology. It is very important to be able to have effective characterization techniques to probe the underlying mechanisms behind these challenging issues. A promising technique is Inelastic Electron Tunneling Spectroscopy (IETS), which probes the MOS structure by detecting the interaction between the tunneling electrons and the energy-loss modes caused by lattice vibrations (phonons), impurities, and defects in the gate dielectrics. The principle of the IETS technique is based on the fact that, as the bias voltage brings the Fermi level of the injecting electrode to reach the characteristic energy of an energy-loss mode in the tunnel barrier, an inelastic interaction of tunneling electrons with this energy-loss mode opens up an additional tunneling channel on top of the elastic tunneling current background, and the current-voltage (I-V) curve will increase its slope at that bias voltage. By taking the second derivative of the I-V curve, a peak shows up where the slope changes in the I-V curve. Thus the IETS technique basically takes the 2nd derivative of the I-V characteristic to reveal inelastic interactions between tunneling electrons and the various energy-loss modes in the tunnel barrier. The energy where a peak occurs corresponds to the characteristic energy of that particular mode, whether it is due to a phonon, an impurity, or a particular defect, and the area of the peak is directly related to the strength of the interaction. In this paper, we will report some IETS spectra that contain a wealth of information on the chemical bonding and composition of ultra-thin HfO2 and aluminum doped HfO2 (HfAlO) as high-k gate dielectrics in MOS capacitor structures. We will also show the effects of traps on IETS spectra, and the use of IETS to study the trap-assisted current transport mechanisms, the creation of traps by electrical stress, as well as the microscopic origins of stress-induced-leakage-current (SILC) .

9:00 AM E1.2
Point defects in thin $HfAlO_x$ films probed by monoenergetic positron beams. Akira Uedono[1], R. Mitsuhashi[2], A. Horiuchi[2], K. Torii[2], M. Goto[1], K. Yamabe[1], K. Yamada[3], R. Suzuki[4], T. Ohdaira[4] and T. Mikado[4]; [1]Institute of Applied Physics, University of Tsukuba, Tsukuba, Ibaraki 305-8573, Japan; [2]Semiconductor Leading Edge Technologies, Inc., Tsukuba, Ibaraki 305-8501, Japan; [3]Nano Technology Research Laboratory, Waseda University, 513, Waseda-Tsurumaki, Shinjuku, Tokyo, Japan; [4]National Institute of Advanced Industrial Science and Technology, Tsukuba, Ibaraki 305-8568, Japan.

Hafnia (HfO_2) and its related alloys such as $HfAlO_x$ are possible replacements for silicon dioxide as the gate dielectric materials for CMOS transistors. Since the electric properties of such "high-k" materials are expected to relate the presence of point defects, knowledge about behaviors of the defects in high-k materials is crucial. The positron annihilation technique is an established means of studying point defects in materials. When a positron is implanted into solids, it annihilates with an electron, and emits γ quanta. The motion of the positron-electron pair causes a Doppler shift in the energy of the quanta. A positron may be localized in a vacancy-type defect due to Coulomb repulsion from ion cores. Since the momentum distribution of the electrons in such defects is different from that in the bulk, one can detect the defects through measurements of Doppler broadening spectra of γ quanta. The change in the spectrum is characterized by the S parameter, which mainly characterizes the fraction of the annihilation of positron-electron pairs having a low momentum distribution. The value of S differs depending on the specific type of defects. Information useful for identifying vacancy-type defects can also be obtained by measuring the lifetime spectra of positrons. The present study used monoenergetic positron beams to investigate defects in $HfAlO_x$ films. The samples were 7-nm thick $HfAlO_x$ films deposited on Si substrates by atomic layer deposition technique. Trimethylaluminum and hafnium tetrachloride were used as precursors, and water vapor was used as an oxidizing agent. After the deposition, the samples were annealed at 1050°C (1 s) in O_2/N_2 atmosphere. For the as-deposited film, the annihilation modes of positrons were found to be two, and their lifetimes were obtained to be 281 ps and 524 ps (58%), respectively. Since those lifetimes were longer than the typical lifetime of positrons annihilated from the free-state in metal oxides, it can be concluded that two different kinds of open spaces were present in the as-deposited film. After annealing in 0.02%-O_2 atmosphere, the value of S for $HfAlO_x$ film decreased, and its annihilation mode became one; the positron lifetime was 412 ps. These results can be attributed to the shrinkage of the mean open spaces due to the change in the matrix structure of $HfAlO_x$ during annealing. We observed a clear correlation between the mean size of vacancy-type defects and the amount of oxygen in annealing atmosphere. From the detailed analysis of the S-E relationships, negatively charged defects near the $HfAlO_x$ film was also detected. The present results show that a monoenergetic positron beam can be used to study behaviors of defects in thin high-k films deposited on Si substrates. In particular, the potential of positron annihilation for detecting vacancy-type defects in the high-k films makes it a powerful tool for the development of the high quality high-k materials.

9:15 AM E1.3
Probing the electronic structure and bonding in gate oxide stacks. David William McComb[1], Alan J Craven[2], David A Hamilton[2,3] and Maureen MacKenzie[2]; [1]Materials, Imperial College London, London, United Kingdom; [2]Physics and Astronomy, University of Glasgow, Glasgow, United Kingdom; [3]Chemistry, University of Glasgow, Glasgow, United Kingdom.

Electron energy-loss spectroscopy (EELS) is a powerful probe of the local chemistry, electronic structure and bonding in a range of materials via analysis of the fine structure, energy loss near-edge structure (ELNES), present on the ionisation edges. Moreover the technique can be used to analyse samples on a sub-nanometre length scale when carried out in a suitable scanning transmission electron microscope. In this paper we will summarise the results of our experimental investigations of the oxygen K-edge ELNES in HfO2, ZrO2, HfSiO4, ZrSiO4 and SiO2. By utilising sol-gel chemistry as well as co-deposition methods for the formation of these standards we can investigate the influence of semi-amorphous or nanocrystalline structures on the observed ELNES. In order to fully interpret the data obtained we have utilised band structure methods to model the experimental edges. Building on the results of our fundamental study on these bulk standards, we will report the results of EELS spectrum imaging experiments carried out on a range HfO2 layers grown on silicon using both MOCVD and ALD. We will demonstrate that variations in the local electronic structure and bonding can be detected using ELNES and that these can be directly related to chemical and physical changes that occur within the layers and at the interfaces during processing.

10:00 AM *E1.4
Electron Spin Resonance Characterization of Defects at Interfaces in Stacks of Ultrathin High-k Dielectric Layers on Silicon. Andre Stesmans and Valery V Afanas'ev; Physics, University of Leuven, Leuven, Belgium.

The scaling of metal-oxide-silicon (MOS) based devices in integrated circuit technology, entering the 100-nm technology node, drives materials and technological requirements to ever new extremes. A most challenging issue concerns the intended replacement of the traditional SiO2 gate dielectric by one of substantially higher dielectric constant k, which, as projected, would need to be introduced in devices by1 2005. Various potential alternative dielectrics, such as the binary metal oxides Al2O3, ZrO2, TiO2, HfO2, and La2O3, have been or still are intensely studied. The exposed research efforts are impressive; multiple top analyzing techniques are combined to explore compositional and structural characterization. Incorporated in MOS structures and devices, electrical probing methods reveal the occurrence of defects and charge traps2-4 which detrimentally affect the electrical merit of the new high-k layers. Interface traps also appear to play a prominent role.5 The current work reports on the application of the electron spin resonance technique (ESR), a key physical atomic-scale identification tool of point defects in solids5. It is applied here to the investigation of (100)Si/insulator structures with ultrathin high-k layers, including stacks of nm-thin SiOx and layers of ZrO2, Al2O3, and HfO2, grown by various chemical vapor deposition methods. Results will be overviewed with particular emphasis on occurring interface defects and charge traps. Generally, after hydrogen photodesorption, prominent trivalent-Si interface defects (Pbo, Pb1 Si dangling bond type centers) are observed at the (100)Si/dielectric interfaces. This Pbo, Pb1 fingerprint, generally unique for the thermal (100)Si/SiO2 interface, indicates that the as-deposited (100)Si/metal oxide interfaces are basically Si/SiO2-like. Comparison of three different preparation methods of the (100)Si/HfO2 structure shows the Pb-type defect signature, and hence the interface, to be sensitive to the kind of deposition process. The Pb-type defects may serve as atomic probes utmost sensitive to the strain state of the interface, which will be discussed. Also is addressed the influence of post-deposition thermal treatment. This will include, among others, the effect of annealing in H2 on the interface defects (passivation efficiency) and on the multilayer structure in general. Parallel electrical analysis reveals the correlation of Pb-type defects and fast interface traps. A general

conclusion is that ESR may provide specific (atomic) information on the attained interface quality. 1 International Technology Roadmap for Semiconductors (SIA, 2001) 2 M. Houssa et al., J. Appl. Phys. 87, 8615 (2000 3 J. Chavez et al., J. Appl. Phys. 90, 4284 (2001)) 4 L. A. Ragnarsson et al., J. Appl. Phys. 93, 3912 (2003) 5 A. Stesmans and V. V. Afanas'ev, Appl. Phys. Lett. 1957 (2002)

10:30 AM E1.5
Thermal Transformation of Yttrium, Lanthanum and Aluminum Mixed Oxide Films Deposited By Chemical Solution Deposition. Deborah Ann Neumayer, IBM, yorktown heights, New York.

The thermal stability, and microstructure of ytrrium aluminum oxide (YAO) and lanthanum aluminum oxide (LAO) mixed oxides were evaluated. The films were prepared by chemical solution deposition (CSD) using a solution prepared from yttrium, or lanthanum butoxyethoxide, and aluminum butoxyethoxide dissolved in butoxyethanol. The films were spun onto SiOxNy coated Si wafers and furnace annealed at temperatures from 500-1200 ^{o}C in oxygen for 30 minutes. The microstructure and electrical properties of YAO and LAO films were examined as a function of Y/Al and LA/Al ratio and annealing temperature. The films were characterized by X-ray diffraction, FTIR, RBS and AES. At low (<25%) Y or La concentrations at anneal temperatures less than 800 ^{o}C, an amorphous γ-alumina like material was observed in the YAO and LAO films. Crystallization of $YAlO_3$ and $LaAlO_3$ in YAO and LAO films was observed at higher Y or La concentrations and at anneal temperatures > 800 ^{o}C. The YAO and LAO films were observed to react with the underlying silicon at the interface to form silicates. Lanthanum silicate was observed to form more readily than yttrium silicate. Dielectric Constant was observed to be dependent on Y and La concentrations.

10:45 AM E1.6
Influence of nitrogen bonds on electrical properties of HfAlON films fabricated through LL-D&A process using NH_3 annealing. Kunihiko Iwamoto[1], Koji Tominaga[1], Tomoaki Nishimura[2], Tetsuji Yasuda[2], Koji Kimoto[3], Toshihide Nabatame[1] and Akira Toriumi[4,2]; [1]MIRAI -ASET, Tsukuba, Japan; [2]MIRAI -ASRC, AIST, Tsukuba, Japan; [3]AML-NIMS, Tsukuba, Japan; [4]The University of Tokyo, Tokyo, Japan.

We have developed a Layer-by-Layer Deposition and Annealing (LL-D&A) process for growing $HfAlO_x$ as high-k gate dielectrics [1]. This process features that RTA treatments are inserted during ALD cycles and effective to remove residual impurities in the high-k/buffer layer interface. Also, this process can control the extent of nitrogen incorporation in the $HfAlO_x$ layer by using an optional NH_3 annealing. In this paper, we report on the nitrogen bonding features in HfAlON films prepared by LL-D&A process using RTA in NH_3 ambient, which were analyzed by SIMS, XPS, and TEM-EELS measurements. Poly-Si gate HfAlON MOS capacitors and nMOSFETs were fabricated to reveal the influence of nitrogen incorporation on the electrical properties. HfAlON films were prepared by the LL-D&A process, in which a sequence of 0.8nm-thick HfAlOx film growth by ALD and subsequent NH_3 annealing was repeated. NH_3 annealing was carried out at three different temperatures of 650, 850 , and 950°C. It was shown that the nitrogen concentration of HfAlON films prepared by 850 and 950°C is about one order of magnitude higher than the case of 650°C samples as confirmed by SIMS measurements. The XPS data indicated that the Hf4f peak of both 850 and 950°C samples is shifted to lower binding energy by $0.3 - 1.0$ eV as compared to the 650°C samples. The $Hf4f_{7/2}$ and $4f_{5/2}$ components are clearly split for the 650°C sample, while their splitting disappears for both 850 and 950°C cases. The results suggest that Hf-N bonds were formed in HfAlON network when annealed at 850 and 950°C by using NH_3 ambient. It is preliminary shown that excessive incorporation of nitrogen results in a significant increase in the leakage current through HfAlON films. This work was supported by NEDO. [1] T. Nabatame et al., VLSI Symp. Tech. Dig., p 25 (2003)

11:00 AM E1.7
Nano-scale Evaluation of the Topography and Surface Potentials of HfO_2 Layers on Si(100). Rudolf Ludeke and E. P. Gusev; IBM T. J. Watson Research Center, Yorktown Heights, New York.

The known crystallization transition of amorphous, atomic-layer-deposited (ALD) HfO_2 layers annealed above 600°C has led to concerns for surface roughening and associated increases in the inhomogeneous variations of the surface potentials (work function), which could affect the carrier mobility in the underlying channel through additional scattering. We have investigated the topography and surface potential variations of 3 nm thick ALD grown HfO_2 films in the as-deposited (grown at 300°C) and annealed state (650°C and 750°C). We have used a JEOL 4500A AFM microscope operating in the non-contact mode in ultra high vacuum (UHV), which permits the simultaneous acquisition of the topography and the surface potential map (Kelvin image) with lateral resolution of <2 nm and height resolution of <0.1 nm. The first significant observation is the strikingly smooth topography of the as-grown HfO_2 layers, which exhibited a local peak-to-valley roughness in the 0.2-0.4 nm range. The topography consists of laterally extended hillocks of dimensions in the 20-50 nm range that in turn are composed of a nodular substructure of lateral dimensions in the 5-10 nm range. For comparison, SiO_2 thermal oxides and particularly RTO oxides of similar effective thickness exhibited a somewhat grainier morphology with a local roughness that was somewhat larger than that of the HfO_2 layers. Subsequent anneals of the HfO_2 layers to first 650°C and then to 750°C in UHV did not alter the surface roughness, nor its morphology in a significantly measurable way. Pin holes or abnormal, charge sensitive defects were not observed. The surface potential images show some correlation with the topography, more so with the broader features than the smaller substructure. The topography is more sensitive to oxide charge, which in turn is controlled by the bias applied between the substrate and the conductive AFM cantilever tip. In contrast, contact potential profiles, obtained from cuts through the Kelvin images, are essentially independent of the bias over a comparable bias range. Such profiles do not replicate the fine structure of the corresponding profiles in the topography, but rather exhibit long range fluctuations of the order of 50 nm in extent and peak-to-valley values (workfunction variations) of 0.2 V. Over a typical image of 200x200 nm^2, contact potential difference (CPD) extrema are about twice this value. As with the topography, annealing the layers did not alter the magnitude of contact potential fluctuations, although the average values (DC level) increased by about 0.2 V between the 650°C and 750°C anneals.

11:15 AM E1.8
Structure and Stability of Hafnium Silicate Films. Susanne Stemmer[1], Youli Li[1], Yan Yang[1], Brendan Foran[2], Patrick Lysaght[2], Stephen Streiffer[3] and Paul Fuoss[3]; [1]Materials, University of California Santa Barbara, Santa Barbara, California; [2]International Sematech, Austin, Texas; [3]Argonne National Laboratory, Argonne, Illinois.

Grazing-incidence small-angle X-ray scattering (GISAXS) and high-resolution transmission electron microscopy (HRTEM) were used to investigate phase separation in hafnium silicate films after rapid thermal annealing between 700 and 1000 °C. 4 nm thick Hf-silicate films with 80 mol% and 40 mol% HfO2, respectively, were prepared by metal organic vapor deposition. Films of the two compositions showed distinctly different phase-separated microstructures, consistent with two limiting cases of microstructural evolution: nucleation/growth and spinodal decomposition. Films with 40 mol% HfO2 phase separated in the amorphous by spinodal decomposition and exhibited a characteristic wavelength in the plane of the film. Decomposition with a wavelength of $\sim$ 3 nm could be detected at 800 °C. At 1000 °C the films rapidly demixed with a wavelength of 5 nm. This is consistent with the theory of spinodal decomposition, which predicts that the characteristic wavelength increases with increasing temperature. In contrast, films with 80 mol% HfO2 phase separated by nucleation and growth of crystallites, and showed a more random microstructure. We also present calculations of the metastable extensions of the miscibility gap and spinodal for the ZrO2-SiO2 system. The calculations predict that SiO2-rich compositions, investigated for gate dielectric applications, will show spinodal decomposition if they contain less than $\sim$ 90 mol% SiO2 at the typical device processing temperature of 1000 °C. The factors determining specific film morphologies and phase separation kinetics are discussed. With respect to the films properties, a laterally phase separated film structure will cause large fluctuations of the electric field along the Si channel. The wavelengths of the composition fluctuations are a significant in comparison with current gate lengths. This may lead to device performance and reliability problems.

11:30 AM E1.9
Characterization of the Electronic Structure and Optical Properties of for Al2O3, ZrO2, and SrTiO3 from Analysis of Reflection Electron Energy Loss Spectroscopy in the Valence Region. Guolong Tan[1], Lin K. Denoyer[2], Roger H. French[1,3], Ana Ramos[4], Martine Gautier-Soyer[5] and Yet Ming Chiang[4]; [1]Dept. of Materials Science and Engineering, University of Pennsylvania, Philadelphia, Pennsylvania; [2]Deconvolution and Entropy Consulting, Ithaca, New York; [3]Experimental Station, DuPont Corporation Central Research, Wilmington, Delaware; [4]Dept. of Mat. Sci .& Eng.,, Massachusetts Institute of Technology, Cambridge, Massachusetts; [5]Service de Physique et Chimie des Surfaces et Interfaces, CEA Saclay, France.

Characterization of thin surficial films of oxides has become the focus of increased interest due to their applications in microelectronics. The ability to experimentally determine the electronic structure and

optical properties of oxide materials permits the direct study of the interband transitions from the valence to the conduction band states. In the past years there has been much progress in the quantitative analysis of transmission electron energy loss spectroscopy in the electron microscope and we are extending this work for analysis of thin oxide films on semiconductors. Here we employed reflection electron energy loss function (REELS) as well as vacuum ultraviolet (VUV) spectroscopy to determine the optical properties and electronic structure of oxide materials, i.e. Al2O3, ZrO2 and SrTiO3. The surface and bulk plasmon resonances for these oxide materials have been determined from VUV and REELS, along with the influence of primary electron energy on the REELS results. Once the multiple scattering has been removed from the REELS spectra we have used Kramers-Kronig dispersion transforms to determine the complex optical properties. The relative contribution of surface and bulk plasmon oscillation in REELS has been investigated. Comparison with VUV results and existing TEELS results indicate that Kramers-Kronig analysis can also be applied to REELS spectra and the corresponding conjugate optical properties can be obtained. Quantitative studies of the electronic structure and optical properties of thin Surficial films using VUV and REELS or TEELS, represent a new avenue to determine the properties of these increasingly important films. This work was partially funded by NSF Award DMR-0010062 in cooperation with EU Commission Contract G5RD-CT-2001-00586.

11:45 AM E1.10
Process dependant band structure changes of transition-metal (Ti, Zr, Hf) oxides on Si (100). C. C. Fulton[2], G Lucovsky[1] and R J Nemanich[1]; [1]Physics, North Carolina State University, Raleigh, North Carolina; [2]Materials Science & Engineering, North Carolina State University, Raleigh, North Carolina.

In this study we have deposited Ti, Zr and Hf oxides on ultra-thin (~0.5 nm) SiO_2 buffer layers and have identified metastable states which give rise to large changes in their band alignments with respect to the Si substrate. The high-k oxides were formed by electron beam evaporation of a transition metal followed by remote plasma oxidation. These films were then characterized by x-ray and ultraviolet photoemission spectroscopy (XPS and UPS), which provided information about band bending, chemical bonding and valance band maxima. We observed a potential across the interfacial SiO_2 layer, significant band bending and large shifts in the high-k valence band. The magnitude of the shifts differed for the three materials where ZrO_2 showed the largest shift, HfO_2 was intermediate, and TiO_2 showed the smallest shift. We have also observed that the magnitude of the shift was inversely related to the thickness of the buffer layer. With increased buffer layer thickness the resulting electronic shift decreased. We propose a model in which excess oxygen accumulates near the high-k – SiO_2 interface providing electronic states, which are available to electrons that tunnel from the substrate. Research supported by SRC.

SESSION E2: High-K Oxides on Silicon
Chairs: Evgeni Gusev and T.P. Ma
Monday Afternoon, December 1, 2003
Room 207 (Hynes)

1:30 PM *E2.1
Formation and Stability of Metal Oxide/Si and Silicate/Si Interfaces. Matthew Copel, M. Reuter, N. Bojarczuk, S. Guha, E. Gusev, P. Jamison, V. Narayanan and D. Neumayer; ibm, Yorktown Hts, New York.

Interface formation is critical to integration of alternative gate dielectrics for Si-based CMOS. This talk will describe medium energy ion scattering studies of high-k/silicon structures. Typically, metal oxide stacks rely on a thin SiO2 or SiOxNy buffer layer to passivate the Si surface. Once created, the survival of the interfacial oxide is far from certain. Numerous mechanisms have been found to destabilize this barrier, such as silicate formation, growth-induced reduction and high temperature reduction. Silicate formation is highly dependent on metal species, with Y and La oxides undergoing a facile reaction compared to Hf and Zr oxides. In the extreme case of yttrium, buffer layers can be entirely consumed by silicate formation during UHV high temperature annealing. For HfO2, we see little evidence of silicate formation, but we do observe interactions with SiO2. Deposition of HfO2 under MBE conditions can cause rapid reduction of SiO2, even with a high oxygen overpressure. Detailed kinetic studies suggest that oxygen vacancies generated during growth are responsible. Understanding the stability of buffer layers is critical to successful integration of stacked dielectrics. Alternatively, removing interfacial oxide may provide a route to higher capacitance structures, but this will only prove viable in the unlikely event that we can learn how to passivate and integrate these fragile structures.

2:00 PM E2.2
Properties of Ultra-Thin Silicon Nitride Barriers.
Katherine Buchheit, Hideki Takeuchi and Tsu-Jae King; Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, Oakland, California.

Metal oxides such as HfO_2 and ZrO_2 are known to form interfacial layers at the Si interface, resulting in an undesirable increase of EOT (effective oxide thickness). It has been reported that NH_3 pre-treatment is effective for suppressing the EOT increase. However, detailed properties of the silicon nitride layer are not well understood. In this study, properties of 0.8 - 1.3 nm Si_3N_4 formed by RTN (rapid thermal nitridation) were investigated. First, interface properties of the nitride layer were characterized by surface charge analysis, which can extract interface state densities, fixed charge densities, and near-interface trap densities without suffering from high leakage. It was found that high temperature annealing (900-1100°C) of the nitride layer in an inert ambient reduces trap densities by at least a factor of two ($\sim 5x10^{11} cm^{-2} eV^{-1}$). In addition, only electron traps and negative fixed charges were observed for the nitride, whereas only hole traps and positive fixed charges were observed for ultra-thin SiO_2 films. Next, immunity to boron penetration from p+ poly-Si was characterized. After a high thermal budget anneal in varied ambient gases, the resulting doping profiles measured by spreading resistance analysis showed that a nitride film annealed in N_2 kept the additional junction depth caused by annealing to only 24% of that of a control sample with no nitride. Finally, application of the nitride layer to ultra-shallow junction formation was proposed. I-V characteristics of the p+ poly-Si gated MIS capacitor showed leakage current of the same order of magnitude as that of the diodes with no nitride, indicating that boron diffusion can be suppressed without degrading forward diode current.

2:15 PM E2.3
Material Science and Integration of A New Hybrid $Ti_xAL_{1-x}O_y$ Layer As An Alternative Gate Oxide For Sub-100 nm CMOS Devices. Orlando Auciello[1], Wei Fan[1,2], Bernd Kabius[1], John M. Hiller[1], Sanjib Saha[1], John A. Carlisle[1], Shuyou Y. Li[2], Vinayak P. Dravid[2], Robert P.H. Chang[2], Cirillo Lopez[3], Eugene A. Irene[3], Raul A. Baragiola[4] and Charles A. Dukes[4]; [1]Materials Science, Argonne National Laboratory, Argonne, Illinois; [2]Materials Science, Northwestern University, Evanston, Illinois; [3]Chemistry, University of North Carolina, Chapel Hill, North Carolina; [4]Materials Science, University of Virginia, Charlottesville, Virginia.

A new $Ti_xAl_{1-x}O_y$ (TAO) oxide layer developed in our laboratory, produced by sputter-deposition, exhibit the combination of properties required for the next generation of integrated circuit gate oxides, namely: (a) a dielectric constant k ~ 30 (higher than that of current leading amorphous gate oxides); (b) thermodynamic stability when integrated with Si (a SiO_2 interface layer < 1 nm thick, depending on the oxidation temperature in the range of room temperature to 500 °C, is formed between TAO and Si); (c) bandgap ~ 3.9 - 4 eV (may be higher when optimized); (d) leakage current ~ 10^{-5} A/cm ^{2} at 1 V for a TAO layer with equivalent oxide thickness (EOT) ~ 1.7 nm and ~ 4.2 A/cm ^{2} for TAO with EOT of 0.8 nm; and (e) relatively low density of electrically active defects at the oxide/Si interface (not optimized yet). Chemical analysis via x-ray photoelectron spectroscopy and near-edge synchrotron x-ray absorption spectroscopy, respectively, reveals a delicate equilibrium in oxygen binding to Ti and Al atoms, as well as Ti-Al bonding, resulting in a fully oxidized amorphous TAO structure that inhibits a strong reaction of oxygen with Si that is characteristic of other gate materials currently under investigation. Cross-sectional high-resolution transmission electron microscopy and spectroscopic ellipsometry provide evidence for an atomically sharp TAO/Si interface. Oxidation via atomic oxygen at room temperature enables a TAO layer with a negligible SiO_2 interface. The amorphous microstructure of the TAO layer plus its chemical state results in the excellent electrical properties revealed by C vs. V, leakage current, interface state measurements. * This work was supported by the US Department of Energy, BES-Materials Sciences, under Contract W-13-109-ENG-38; NSF/ONR under Contract N00014-89-J1178 (UNC-CH).

3:00 PM *E2.4
Stability of Nitrogen in High-k Dielectrics. I. J. R. Baumvol, Universidade Federal do Rio Grande do Sul - UFRGS, Porto Alegre, RS, Brazil.

The use of metal oxide and silicate films on Si as a high-k replacement for silicon oxide and oxynitride gate dielectrics in advanced VLSI technology presents several difficulties concerning interface density of states, chemical and structural stability in further processing steps following high-k deposition, oxidation of the Si substrate, and migration of metallic species into the active semiconductor region, as well as transport of Si into the high-k film. Recent investigations

indicated that incorporation of nitrogen into the metal oxide and silicate films provided substantial improvements in the direction of overcoming the above mentioned difficulties. However, since N is mainly incorporated into metastable configurations in these oxide and silicate films, the integration of nitrided high-k dielectrics into the fabrication process relies on the stability of N in these materials during further processing steps. We report here on N, O, Si, Al, and Hf atomic transport and exchange processes during thermal processing of nitrided aluminum oxide and hafnium silicate films on Si. The profiles of the light elements were determined, before and after thermal processing, by narrow nuclear resonant reaction profiling with sub-nanometric depth resolution. Strong N removal and redistribution of the remaining N were observed following thermal processing, the major mechanism responsible for N removal being N-O exchange. N redistribution, on the other hand, seems to be the result of a complex reaction-diffusion mechanism which will be discussed. Oxygen migration and amounts of oxidation and nitridation of the Si substrate during different thermal processing routines were also accessed by profiling.

3:30 PM *E2.5

Study of HfAlOx Films Deposited by Layer-by-Layer Growth for CMOS High-k Gate Dielectrics. Akira Toriumi[1,2], Toshihide Nabatame[3] and Tsuyoshi Horikawa[2]; [1]Materials Science, The University of Tokyo, Tokyo, Japan; [2]AIST, Tsukuba, Japan; [3]ASET, Tsukuba, Japan.

We have investigated ternary metal oxides for possible high-k gate dielectrics by using layer-by-layer deposition & annealing method so as to keep the dielectric constant of the film high with no crystallization. In fact we have prepared HfAlOx films by alternating deposition of HfO2 and Al2O3 atomic layers. It is a key for controlling the film quality to understand the intermixing process between two layers by the thermal treatment. So, we first discuss the atomic diffusion and structural change of the HfO2/Al2O3 superlattices film as a function of annealing temperature by changing the Hf/Al composition ratio. In case of the film with Hf/Al=9A/3A cycle, the superlattice peak was observed below 750C by XRD. Above 850C, it disappeared, and then the orthorhombic or tetragonal structure was detected. These results indicate that the intermixing in HfO2/Al2O3 films occurs between 750 and 850C. The intermixing onset temperature increases with increasing Al content in Hf/Al ratio. Next, the MOS characteristics with HfAlOx films prepared by this method are discussed in terms of the quality improvement and the profile design inside the dielectric film. Finally, prospects of these oxides for CMOS high-k gate dielectrics are also addressed.

4:00 PM E2.6

Measurement of the Band Offset Between Amorphous Lanthanum Aluminate and Silicon. Lisa Friedman Edge[1], D G Schlom[1], S A Chambers[2], C Hinkle[3], G Lucovsky[3], Y Yang[4], S Stemmer[4] and M Copel[5]; [1]Materials Science and Engineering, Pennsylvania State University, University Park, Pennsylvania; [2]Fundamental Science Division, Pacific Northwest National Laboratory, Richland, Washington; [3]Department of Physics, North Carolina State University, Raleigh, North Carolina; [4]Materials Department, University of California, Santa Barbara, California; [5]IBM T.J. Watson Research Center, Yorktown Heights, New York.

$LaAlO_3$ is a promising alternative gate dielectric for the replacement of SiO_2 in silicon MOSFETs. Single crystalline $LaAlO_3$ is known to have a dielectric constant of 24 and an optical bandgap of 5.6 eV. It has also been shown that single crystalline $LaAlO_3$ is stable in contact with silicon under standard MOSFET processing conditions (1026 °C for 20 s). An important additional characteristic for alternative gate dielectric applications is knowledge of the band offsets between $LaAlO_3$ and Si. These have been predicted to be in the range 1.0 to 2.1 eV for electrons and 1.9 to 3.5 eV for holes.[1,2] By investigating the oxidation kinetics of Al and La, both individually and together (codeposition), to determine the minimum oxygen partial pressure required to achieve fully oxidized lanthanum aluminate, we have found a regime in which we can deposit amorphous lanthanum aluminate on Si without any interfacial SiO_2. These films are made by molecular beam deposition (MBD) in a low temperature / excess oxidant regime. AES, MEIS, and XPS analyses indicate that these amorphous lanthanum aluminate films as thin as 10 Å are fully oxidized and show no SiO_2 at the interface, even after prolonged exposure of the films to air. Using XPS we have measured the band offsets for these abrupt amorphous lanthanum aluminate films with Si. The measured band offsets are 1.35 ± 0.3 eV for electrons and 3.15 ± 0.1 eV for holes. The band offsets are independent of doping concentration in the Si substrate as well as the thickness of the amorphous lanthanum aluminate film. [1] J. Robertson, MRS Bull. **27**, 217 (2002). [2] P. W. Peacock and J. Robertson, J. Appl. Phys. **92**, 4712 (2002).

4:15 PM E2.7

Maximization of the Crystallization Temperature and Dielectric Constant for the Hafnia-Alumina-Gadolinia Ternary. Chad Robert Essary, Joshua M. Howard, Valentin Craciun and Rajiv K. Singh; Materials Sci & Eng, University of Florida, Gainesville, Florida.

Currently in the search for an alternative high-k dielectric material to replace silicon dioxide, hafnium oxide has shown promise due to its thermodynamic stability on silicon and higher dielectric constant. However, hafnia crystallizes at relatively low processing temperatures which results in leakage path formation at the grain boundaries. To increase the crystallization temperature hafnia was alloyed with alumina and gadolinia using a multi-target pulsed laser deposition technique. In this study, thin films of various compositions in the ternary were deposited, including the pure endpoint components, to compare band gaps, dielectric constant changes, and the effect on the crystallization temperature. Film stoichiometry and quality was assessed using x-ray photoelectron spectroscopy and Fourier transform infrared spectroscopy. Crystallization temperatures were determined by high-resolution x-ray diffraction with high temperature capabilities up to 900°C. Electrical properties of the films were compared using capacitance-voltage and current-voltage measurements with platinum electrodes. From these results, the optimal composition which maximized the dielectric constant and the crystallization in this ternary system was determined.

4:30 PM E2.8

Physico-chemical and electrical characterisation of HfO_2 layers deposited on strained SiGe by Atomic Layer Deposition. Jean-Francois Damlencourt[1], Olivier Weber[1,2], Jean-Michel Hartmann[1], Frederique Ducroquet[1,2] and Marie-Noelle Semeria[1]; [1]CEA -DRT, LETI/DTS, CEA/GRE, Grenoble cedex 9, France; [2]LPM, INSA-Lyon, Villeurbanne.

Recent results have shown that High-K materials, such as HfO_2, are very promising materials for the replacement of SiO_2 in the gate stack of MOS transistors, in order to achieve a lower leakage current for the same Equivalent Oxide Thickness (EOT). However, the use of HfO_2 on Si led to a strong mobility degradation. Enhanced hole mobility in $Si_{1-x}Ge_x$ under compressive strain has been reported and could be an alternative to the mobility degradation. This paper focuses on the growth of HfO_2 by Atomic Layer Deposition (ALD) at 350°C on pseudomorphic $Si_{1-x}Ge_x$ thin films (x=15 and 25%). Three different SiGe surface preparations (Chemical oxidation, HF-dip and HF-dip + in situ hot water pulses) have been investigated to obtain the best HfO_2 film quality with the thinnest interfacial layer. The start of the ALD growth on these different surfaces has been analysed by Total X-Ray Fluorescence. No nucleation retardation has been observed not even for HF dipped SiGe treated surfaces. We assume that this is due to the greater Ge oxidation potential. We have also seen, by X-Ray Photoelectron Spectroscopy, that HF-dipped SiGe surfaces were very convenient to obtain high quality HfO_2 films. The structure of the interfacial layer has been precisely analysed : it is made of a Ge/Si mixed oxide layer. The evolution of this interfacial layer has been studied as a function of subsequent annealing treatments. Thin HfO2 layers (2.5, 3.5, 5 and 8nm) deposited on HF-dipped $Si_{0.75}Ge_{0.25}$ strained layers were analysed by mercury probe. An EOT as low as 0.7 nm was obtained for a 2.5 nm as-deposited HfO_2 film. Results on the physico-chemical and electrical characterisation of HfO_2 layers deposited by ALD at 350°C directly on pure Ge layers will be also presented.

4:45 PM E2.9

Chemical and Electrical Characteristics of HfSixOy HfAlxOy Gate Dielectric MOSFETs. Choong-Ho Lee, Sundar Gopalan, Jeff Peterson, Jim Gutt, Hong-Jyh Li, Pat Lysaght and Mark Gardner; Advanced Gate Stack Project, SEMATECH, Austin, Texas.

Various high dielectric constant materials such as Ta2O5[1-2], Al2O3[3-4], TiO2[5], and SrTiO2[6] have been researched for gate dielectric application. Ta2O5 was shown to have interfacial reactions with Si substrate [7], while TiO2 and SrTiO2 were not thermally stable in direct contact with the silicon substrate. Al2O3 is compatible with the silicon substrate, but the overall dielectric constant is less than 10; therefore, achieving an equivalent oxide thickness (EOT) of less than 10A may not be feasible using Al2O3. Recently, HfO2 and HfSixOy have received industry attention due to their thermal stability on Si and moderately high dielectric constant (12 ~ 25).Also, they are believed to have a wide band gap of ~5.5eV with electron and hole barrier heights of 1.4eV and 3.3eV, respectively. However, the low crystallization temperature of HfO2 (<500C) creates a problem for conventional planar CMOS integration. There have been many attempts to improve the crystalline temperature of HfO2 by adding nitrogen, Si and aluminum [8-9], including a HfO2-Al2O3 laminate gate dielectric MOSFET with poly silicon gate, in which the laminated layers are intermixed after the source/ drain activation anneal [10]. Scaling below 14 ~15A EOT with HfSixOy and a poly-Si gate is extremely difficult, as leakage becomes considerably high. By

using HfAlxOy, the scalability can be improved with better leakage. However, mobility degradation with HfAlxOy is a serious concern. It has been reported that Al diffusion into the FET channel is a possible cause for mobility degradation in Al2O3 gated MOSFETs. This paper presents an investigation of HfAlxOy as a capping layer to improve EOT scalability for HfSixOy dielectric, with the intent that the HfSixOy may screen any mobility degredation associated with the HfAlxOy. We have found that using ALD HfAlxOy as a capping layer for HfSixOy gives superior EOT scaling over ALD HfO2 capping layers and will present data demonstrating the feasibility of EOT scaling below 10A using HfSixOy HfAlxOy gated MOSFETs. We also show that the mobility of HfSixOy HfAlxOy gated MOSFETs improve when the ALD HfAlxOy thickness is decreased. We propose that the mobility characteristics of the HfSixOy HfAlxOy gate MOSFET are dominated by remote charge scattering. [1]A. Chatterjee, et al., Tech. Dig. Int. Electron Device Meet. 1998, p.777 [2]D. Park, et al., Tech. Dig. Int. Electron Device Meet. 1998, p.381 [3] D. A. Buchanan, et al., Tech. Dig. Int. Electron Device Meet. 2000, p.223 [4]J. H. Lee, et al., Tech. Dig. Int. Electron Device Meet. 2000, p.645 [5]X. Guo, et al., Tech. Dig. Int. Electron Device Meet. 1999, p.137 [6]K. Eisenbeiser, et al., APPLIED PHYSICS LETTERS, Vol. 76, No. 10, p. 1324, (2000) [7] G. B. Alers, et al., APPLIED PHYSICS LETTERS, Vol. 73, No. 11, p. 1517, (1998) [8] C. Choi, et al, IEDM 2002, 34.3 [9] G. D. Wilk , et al., Symposium on VLSI Tech., 2002, p88 [10]J. H. Lee, et al., VLSI 2002, p84

SESSION E3: Poster Session: Fundamentals of Novel Oxide/Semiconductor Interfaces I
Chairs: Cammy Abernathy and Evgeni Gusev
Monday Evening, December 1, 2003
8:00 PM
Exhibition Hall D (Hynes)

E3.1
Scanning Tunneling Spectroscopy Characterization of Oxide/Silicon Interfaces. Louis Nemzer and Fredy R. Zypman; Physics, Yeshiva University, New York, New York.

We will present results on the effects of imperfections on performance of quantum multi-layered materials. More concretely, we have quantified the dependence of current-vs-voltage (I-V) curves on interface roughness and interface strain. Recently, a new type of quantum structure has been designed based on silicon and oxygen. These semiconductor-atom structures (SAS) are built by alternating layers of silicon and films of oxygen, thus creating structures similar to the traditional superlattices. These SAS have good optical electro- and photo-luminescence and may therefore form the basis of future all-Si integrated circuits with both electrons and photons. Due to their novelty, their I-V curves are only qualitatively satisfying. TEM images show that SAS have stacking faults and dislocations in substantial quantities as to affect response time and transmission. Substantial experimental work has been done to understand why in SAS, silicon may grow epitaxially after the oxygen barrier. This is never the case in Si/SiO2 interfaces. If, during growth, the oxygen valve is left open, a large number of defects is generated in bulk silicon. However, by controlling the oxygen rate supply, it is possible to produce silicon on both sides of the oxygen interface with defect densities below 109/cm2. Nevertheless, the oxygen layer itself is typically broken up in islands. What is clear is that it is technically possible to produce SAS with negligible bulk defects but that still present strain and disorder at the oxygen interface. We have studied the effect of interface disorder and strain on SAS current-voltage curves. Their quality factor is extremely sensitive to the presence of imperfections. We will present results for structures made of alternating layers of materials. The I-V curves will be calculated within Tight Binding (TB) Theory. As a spin-off of the TB calculations, we have extracted a value of an effective silicon-oxygen barrier height.

E3.2
Oxide-Semiconductor Interface Characterization Using Kelvin Probe-AFM In Combination With Corona-Charge Deposition. Bert Lagel, Maria Daniela Ayala, Elena Oborina, Andrew M Hoff and Rudy Schlaf; Electrical Engineering, University of South Florida, Tampa, Florida.

Corona charge deposition methods in combination with spatially resolved surface potential measurements have become a standard tool for Si oxide quality monitoring [1]. Based on this technique oxide-semiconductor interface parameters such as surface barrier height, oxide thickness and oxide charge density can now be monitored in-line with commercially available devices. The ongoing downscaling of integrated circuits into the sub-100 nm regime makes the development of high resolution oxide screening methods increasingly important. However, currently available commercial devices are limited in their spatial resolution since they employ the traditional vibrating Kelvin probe technique, restricting their lateral resolution to several μm [2]. In order to increase the lateral resolution of this measurement method we have combined the corona-charge deposition technique with Kelvin Probe AFM. We present initial results of this novel measurement technique and demonstrate its feasibility by measurements on lithographically prepared oxide patterns on Si wafers with different oxide thicknesses. [1] D.K. Schroder, Meas. Sci. Technol 12(3), R16 (2001). [2] L. Kronik. Y. Shapira, Surface Science Reports 37, 1 (1999).

E3.3
Field-induced Reactions of Water Molecules at Si-dielectric Interfaces. Leonidas Tsetseris[1], Xing Zhou[2], Ronald D Schrimpf[2], Daniel M Fleetwood[2] and Sokrates T Pantelides[1,3]; [1]Physics and Astronomy, Vanderbilt University, Nashville, Tennessee; [2]Electrical and Computer Engineering, Vanderbilt University, Nashville, Tennessee; [3]Solid State Division, Oak Ridge National Laboratory, Oak Ridge, Tennessee.

Water molecules are to a varying degree present in SiO_2 and other dielectrics and at Si-dielectric interfaces. Their presence, even in small concentrations, constitutes a critical reliability problem for present day ultrathin dielectrics. Here we present first-principles density functional calculations that probe the reactivity of water molecules at the Si-dielectric interface. Even though these molecules are generally non-reactive at room temperature, they become active in the presence of strong electric fields that produce a hole inversion layer, as in a p-channel MOSFET. We report results on different possible reaction pathways for water at the interface, including dissociation of water that can lead to the release of H^+ ions. The released protons can migrate away and depassivate dangling bonds. Results are also presented for the reaction of water with a number of defects, including a passivated bond, a suboxide bond, and a hydrogen migrating laterally along the interface. We thus obtain the atomic-scale mechanisms for the creation of interface traps and oxide trapped charge, the two features that give rise to negative bias temperature instability (NBTI), a well known reliability phenomenon that occurs in MOSFETs under normal operating and stress conditions.

E3.4
Kinetics of thermal oxidation at the Si(001)-SiO2 interface; Revisited from high-temperature. Hiroo Omi, Masashi Uematsu, Hiroyuki Kageshima and Toshio Ogino; Device Physics, NTT Basic Research Laboratories, Atsugi, Kanagawa, Japan.

An understanding of thermal silicon oxidation is essential for further advancements of semiconductor science and technology. It is particularly important to reveal the mechanism of morphological evolution between the growing thermal silicon oxide layers and Si(001) substrate during oxidation to obtain an abrupt interface on an atomic scale. Despite all of the work that has been done on the Si(001)/SiO2 interface formation, however, there is little quantitative understanding of the oxidation kinetics at the interface. In this presentation, we will show the first quantitative scaling analyses of the interface kinetics of thermal silicon oxidation at 1100 - 1380 degrees C. We systematically studied the morphological evolution of the Si(001)-SiO2 interface during oxidation in Ar atmosphere containing a small fraction of O2 using atomic force microscopy (AFM) as a function of oxidation time, O2 fraction, and substrate miscut angle. The interface morphology was observed by AFM after removal of the thermal silicon oxides in dilute HF solution. Scaling analyses on the interface evolution show that the interface width W(L,t) during oxidation scales as Lî.0 and tô.25 at 0.2% O2 atmosphere, and Lô and tô at 2% O2 atmosphere at 1200 degrees C, where L is length and t is oxidation time. The scaling laws we obtained tell us that the Si diffuses inside the growing silicon oxide during the oxidation. The diffusion coefficient derived from the emergence of step-terrace morphology at the interface is close to that of the Si self-diffusion in silicon oxide film. The above results are consistent with a model that involves diffusion of Si species emitted from the substrate and reaction with oxygen gases at the interface. We believe that these findings will help us to understand the kinetics of thermal silicon oxidation at the Si(001)/SiO2 interface below 1100 degrees C.

E3.5
The Oxidation of Si-Ge Alloys and Analyses of Sub-Bonded Si -Implication for Thin Film Oxidation of Si. Ralph Jaccodine[1] and Steve J. Kilpatrick[2]; [1]Lehigh Univ., Bethlehem, Pennsylvania; [2]U.S. Army Research Laboratory, Adelphi, Maryland.

An experimental study of the oxidation of Si-Ge alloys grown on Si.was undertaken to explore conditions under which oxides of mixed composition ie.SiO2-GeO2 occurs. Alloy composition spanned from 1.8% to 16.8% Ge.Dry oxidations were carried out in situ in a Scientia ESCA-300 system with partial pressure of oxygen varied by nine orders of magnitude and between 400 and 800 degrees C. In situ oxidations and analyses were done ranging from initial cleaning to

monolayer absorption to actual oxide formation.Films grown up to 10 nm were analyzed by angle resolved x-ray spectroscopy. These studies were used to explore the influence of alloy composition on sub-bonded states of Si.Mixed oxides were found to be poorer than the pure SiO2 grown on the same alloy. The implication of this work on early oxidation of Si will be suggested!!

E3.6

Nanoscale analysis of local leakage currents in stressed gate SiO2 films by conducting atomic force microscopy.

Hiroki Kondo[1], Akiyoshi Seko[1], Yukihiko Watanabe[3], Akira Sakai[1], Shigeaki Zaima[2] and Yukio Yausda[1]; [1]Department of Crystalline Materials Science, Graduate School of Engineering, Nagoya University, Nagoya, Aichi, Japan; [2]Center for Cooperative Research in Advanced Science & Technology, Nagoya University, Nagoya, Aichi, Japan; [3]Toyota Central R&D Labs., Inc, Nagakute, Aichi, Japan.

Reliability of thin gate dielectrics is one of serious problems in recent ULSI technologies. It is well-known that stress induced leakage current (SILC) occurs at an early stage of the dielectric fatigue caused by applying the high electric field. Although SILC and subsequent dielectric breakdown are considered to take place locally in the film, degradation mechanisms at each local site have not been well understood and only macroscopic measurements have been done so far. In this work, we have developed a nanometer scale observation method for local leakage currents induced in stressed gate SiO_2 films in metal-oxide-semiconductor (MOS) capacitors. Detecting local leakage sites with a nanometer scale area in current images by conducting atomic force microscopy (C-AFM), we studied leakage current properties at respective defect sites and their distributions in gate SiO_2 films. MOS capacitors with a structure of n^+-polysilicon gate electrode/gate SiO_2/n-Si substrate were used. Gate SiO_2 films with a thickness of 11.3 nm were thermally grown at 800°C in pyrogenic oxidation ambient. As a result of Fowler-Nordheim (FN) constant current stress with a current density of 100 mA/cm^2 and a stress time of 100 sec (gate bias was negative), SILC was observed in the current-voltage (I-V) characteristics of MOS capacitors. After the poly-Si gates were removed and the SiO_2 films were thinned chemically to be 5.2 nm thick, current images were observed with a negative substrate bias for both stressed and non-stressed gate SiO_2 films by C-AFM. Only for stressed SiO_2 films, nanometer scale leakage sites were clearly observed. No concavity was confirmed at corresponding positions in a concurrently-obtained morphological image and thus the observed leakage sites were not originated from the thickness fluctuation of SiO_2 but reflected locally-generated defects in the film by FN stress. As the scan for C-AFM observations was repeated at the same area with the same bias condition, average currents of the local leakage sites decreased gradually and, finally, the sites were no longer observed. Converting the number of scan into a current flow time (τ), the leakage current is found to decrease inversely proportional to τ. After the leakage sites disappeared, the C-AFM tip was scanned with a positive substrate bias at the same area. Interestingly, the disappeared leakage sites were detected again at the same positions in the current image. From a similarity to the macroscopically-measured leakage current property, the observed leakage sites are associated with a leakage current known as a transient-SILC. We deduce that appearance and disappearance of the leakage sites depending on the tip-substrate bias condition is due to the hole injection and emission which occur at stress-induced defect sites in the gate SiO_2 film.

E3.7

First-principles Investigation for Reacition of Oxygen at Ultrathin Si-oxide/Si Interface.

Toru Akiyama[1,2] and Hiroyuki Kageshima[1]; [1]NTT Basic Research Laboratories, NTT Corporation, Atsugi-shi, Kanagawa, Japan; [2]Dept. Physics Engineering, Mie University, Tsu-shi, Mie, Japan.

Silicon thermal oxidation is of great interest and importance as a key process in the fabrication of Si-based devices. Even if conventional gate oxides in metal-oxide-semiconductor field-effect transistors are replaced by oxynitride or high permittivity dielectrics, thin oxides might still play a role as a buffer layer in order to reduce defect levels at the interface. In dry oxidation, it is widely believed that silicon oxidation consists of a diffusion process of oxidant in the oxide and its reaction process at the interface. Therefore, a number of experimental studies have been intensively carried out for both the diffusion and the interfacial reaction processes, but theoretical investigations have been mainly focused on the diffusion process. The atom-scale mechanisms such as the reaction pathway and its energy barrier for oxygen insertion at the interface are still unclear. In this work, we performed total-energy electronic-structure calculation to clarify the reaction mechanism of oxygen atoms and molecules at the Si-oxide/Si(100) interface. It is found that in the oxide region of the interface oxygen molecules are more stable than O atoms with the energy gain of 1.0 eV. Moreover, the energy barriers for incorporation of oxygen molecules into the Si substrate are lower than those of O atoms. From these results, it is shown that oxygen molecules diffusing in the oxide directly react with the substrate, indicating that oxygen molecules are the dominant reaction species in dry oxidation. The present energy barriers of the oxygen molecule along and off the energetically lowest path agree well with experimentally reported activation energies for ultrathin oxide formation: The activation energy for very low oxygen gas pressure corresponds to the energy barrier along the energetically lowest path. Therefore, the difference of experimentally reported activation energies depending on the pressure seems to be related to the reaction pathways for oxygen incorporation. The present results also support high oxide-growth rate in ultrathin oxide, which is intuitively understood by the low activation energy compared with that evaluated from the oxide growth rate for oxide layer with 10-100 nm.

E3.8

Atomistic mechanism of B diffusion in gate Si-oxide.

Minoru Otani, Kenji Shiraishi and Atsushi Oshiyama; Institute of Physics, University of Tsukuba, Tsukuba, Japan.

Due to the recent nano-scale miniatualization of silicon devices, penetration of B dopants through ultra-thin gate oxide (SiO2) has become serious. Experimentally the diffusion of B atoms in SiO2 has been extensively studied [1], and several empirical recipes for suppression of B penetration have been proposed. However, the atomistic mechanism of B diffusion is still unclear, although Fair proposed a diffusion model in which the B atom diffuses in SiO2 via peroxy linkage defect (PLD), ≡Si-O-O-Si≡ [2]. Very recently, we have performed first-principles calculations and investigated the diffusion mechanism of a B impurity in perfect SiO2 [3]. We have found that the B atom takes a variety of stable and metastable geometries depending on its charge state and that it can diffuse by forming and breaking a bond configuration in SiO2 networks [3]. It is well known that the gate oxide contains intrinsic defects such as O vacancies and O interstitials, since it is formed by thermal oxidation. In this study, to clarify the role of the defects for the B impurity and its diffusion, we have performed first principle total-energy calculations of the B atom coupled with two types of defects in a-quartz: In one case, the B atom is bound with PLD (an O interstitial), and in another is bound that binds with an O vacancy. We have found that the B atom bound with the O vacancy is rather unstable than that in the perfect crystal or that with PLD. Our calculations have also shown that the B atom forms a bond with an interstitial O atom (B-O complex), becoming three-fold coordinated with surrounding O atoms. Contrary to the Fair's model, we have found that B-O complex diffuses along the bond networks of SiO2 and calculated activation energies are close to those for the B atom diffusion in perfect SiO2. [1] T. Aoyama, H. Tashiro, and K. Suzuki, (1999) J. Electrochem. Soc. 146, 1879 and references therein. [2] R.B. Fair, IEEE Electron Device Letters, 17 242 (1996) [3] M. Otani, K. Shiraishi, and A. Oshiyama, (2003) Phys. Rev. Lett. 90, 075901

E3.9

Ultra Shallow Incorporation of Nitrogen into Gate Dielectrics by Pulse Time Modulated Plasma.

Seiichi Fukuda[1], Yoshimune Suzuki[1], Tomoyuki Hirano[1], Takayoshi Kato[1], Akihide Kashiwagi[1], Masaki Saito[1], Shingo Kadomura[1], Youichi Minemura[2] and Seiji Samukawa[2]; [1]Micro Systems Network Company, Sony Corporation, Atsugi-shi, Kanagawa, Japan; [2]Tohoku University, Sendai-shi, Miyagi, Japan.

Pulse time modulated plasma was studied for formation of ultra thin silicon oxy-nitride for gate application. Pulse time modulated plasma which has been studied to provide a new plasma etching technology with low radiation damage has a potential to serve a new technology to incorporate nitrogen atoms into gate dielectrics such as silicon dioxide (SiO2) and high-k materials. In order to obtain a controllability in the nitrogen depth profile in the oxy-nitride gate dielectrics which has been known to have a strong effect on MOS reliability, micro second ordered pulse was used for the inductive coupled plasma source in our pulse time modulated plasma. The radio frequency (RF) of source plasma and pulse frequency were 12.56 MHz and 10 kHz (100 micro second), respectively. Pulse duty ratio was varied from 20 to 100%. 1.7nm thick thermal silicon dioxide films were subjected to the pulse time modulated plasma and analyzed by SIMS to see the depth profile of nitrogen. A new finding is that both the concentration and the peak position of nitrogen atoms in silicon dioxide films depend on the pulse duty ratio and plasma radiation time. In other words, we found, for the first time, that the nitrogen profile can be finely controlled by our pulse time modulated plasma. For example, a nitrogen peak position of 0.5 nm deep from the oxide surface can be obtained at any desirable peak concentrations with a high controllability by tuning the pulse duty ratio and RF power. This new technology is promising to form reliable gate dielectrics for 65 nm node and beyond where suppression of boron penetration and gate leakage current are the stringent requirements. In this paper, we will also describe extendibility of the new technology to application to

Hf silicate.

E3.10
First-principles study of behaviour of excess Si atoms around ultra-thin Si-oxide/Si interfaces. Hiroyuki Kageshima[1], Toru Akiyama[2], Kazuto Akagi[3], Masashi Uematsu[1], Kenji Shiraishi[4] and Shinji Tsuneyuki[3]; [1]NTT Basic Research Labs., NTT Corp., Atsugi, Kanagawa, Japan; [2]Dept. of Physics Engineering, Mie Univ., Tsu, Mie, Japan; [3]Dept. of Physics, Univ. of Tokyo, Bunkyo, Tokyo, Japan; [4]Dept. of Physics, Univ. of Tsukuba, Tsukuba, Ibaraki, Japan.

The atomic-scale behaviour of excess Si atoms in the bulk Si crystals, namely Si self-interstitials, has been investigated experimentally and theoretically from both scientific and engineering viewpoints and much information has been obtained. However, actual Si crystals have surfaces and interfaces. Since excess Si atoms flow in and out of the interfaces and across the surfaces, an understanding of their behaviour around these surfaces and interfaces is important. Especially, the recent progress of the silicon technology requires fine control of the quality of gate oxide layer and the oxide/substrate interface as well as that of the dopant distribution in the shallow junctions neighbouring to the gate oxide. In this contribution, we investigated the stability of excess Si atoms at the Si-oxide/Si interface using the first-principles calculation and a Si(100) substrate surface covered with a 2-molecular-layer Si-oxide. The results show that the excess Si atoms are more stable both in the oxide layer and at the substrate side of the interface than in the deep substrate. The excess Si atoms appear as the self-interstitials at the substrate side, but they can transform into much stable O-vacancies in the oxide layer. Such stability indicates high solubility of excess Si atoms at the substrate side and in the oxide layer and suggests that they segregate near the interface and flow into the oxide across the interfaces during thermal treatment. It is natural to consider that such excess Si flow into the oxide occurs across both the non-oxidizing and the oxidizing Si-oxide/Si interfaces regardlessly. Since O-vacancies are well-known stable defects in bulk Si-oxide and are often regarded as the source of charge traps, this suggests that the excess Si atom flow into the oxide layer causes degradation of gate oxide quality in case of the non-oxidizing interfaces. On the other hand, the O-vacancies are thought to disappear by reacting with the incoming oxydant in case of the oxidizing interfaces. Alternately, the flow into the oxide is thought not to be negligible and to modulate the growth rate of the oxide layer thickness, because the excess Si atoms are known to emit from the interfaces during the thermal oxidation.

E3.11
Degradation of Ultrathin SiO2 Films by Dynamic Stress — A Local Study by Scanning Probe Mircoscopy/Spectroscopy. Kun Xue, Jianbin Xu, Jian Chen and Jin An; Electronic Engineering, The Chinese University of Hong Kong, Hong Kong, Hong Kong.

The reliability of the insulating characteristic of gate oxide is a continuing concern in the development of semiconductor devices. Though much endeavor has been dedicated to address the mechanism of SiO2 films wear out and degradation, no definitive answers are available yet. Since most of devices in integrated circuits (ICs) are usually biased under variable timing conditions, the local study of ultrathin SiO2 degradation by dynamic stress may give a more realistic scenario of the degradation process. In the present work, we applied a continuous pulse voltage at the sample (ultrathin SiO2 film) to induce dynamic electrical stress. The pulse frequency is selected to be out of the response frequency of the scanning tunneling microscopy (STM) feedback loop. The ultrathin SiO2 films were prepared by in-situ thermal oxidation of silicon in ultra-high vacuum and ozone thermal oxidation in ambient. The local I-V characteristics of the SiO2 before and after the stress process were measured and compared. It shows that under the dynamic stress, the oxide degradation has a relaxation effect that could be explained by the hydrogen-related degradation model. Moreover, we have also studied the frequency dependence of the wear-out in the oxide by using STM and conducting atomic force microscopy (AFM). The result showed that the wear-out process had greatly prolonged after high frequency pulse stress.

E3.12
Conductance Transient Comparative Analysis of ECR-PECVD Deposited SiN_x, SiO_2/SiN_x and SiO_xN_y Dielectric Films On Silicon Substrates. Helena Castan[1], Salvador Duenas[1], Juan Barbolla[1], Alvaro del Prado[2], Enrique San Andres[2], Ignacio Martil[2] and German Gonzalez-Diaz[2]; [1]Electronica, Universidad de Valladolid, Valladolid, Valladolid, Spain; [2]Fisica Aplicada III, Universidad Complutense de Madrid, Madrid, Valladolid, Spain.

We present a study of MIS structures based on SiN_x, SiO_2/SiN_x and SiO_xN_y films deposited on silicon by electron cyclotron resonance plasma-enhanced chemical vapour deposition (ECR-PECVD). PECVD techniques use plasma to generate active precursors for low temperature deposition. ECR technique allows a very efficient activation of the precursors, reducing the ion bombardment damage. For $Al/SiN_x/Si$ and $Al/SiN_x/SiO_2/Si$ devices, we deposited a 90 Å layer of silicon dioxide over a half of the samples by using an Astex ECR plasma source on n-type Si substrates. After that, all the samples underwent an ECR-PECVD $SiN_{1.44}$ film deposition. Gases employed are N_2 and SiH_4. In this way, we obtained two kinds of samples: one with a silicon oxide film and another without it. As for $Al/SiO_xN_y/Si$ MIS structures, precursor gases are N_2, O_2 and SiH_4. We made a C-V and DLTS characterization of all devices. Room and low temperature C-V curves exhibit hysteresis phenomena for all the samples, thus indicating that interface state distribution fits to the Disordered-induced gap state (DIGS) model. When defects are not only located at the interface but they are spatially distributed into the insulator, are called DIGS or slow traps, and conductance transients are detected when driving MIS structures from deep to weak inversion. We observe that interface trap densities are higher for silicon oxynitride than for silicon nitride and oxide/nitride films. Surprisingly, the interface quality of Al/SiNx/SiO2/Si samples seems to be poorer than for $Al/SiN_x/Si$ devices. Conductance transients contribute to clarify this: $Al/SiN_x/Si$ devices exhibit the highest DIGS density, whereas the lowest one corresponds to $Al/SiN_x/SiO_2/Si$. Silicon oxynitride MIS capacitors show an intermediate behaviour. We detect that for $Al/SiN_x/SiO_2/Si$ samples there are DIGS defects up to depths of only 20 Å into the insulator bulk. The maximum DIGS density, located at 150 meV above the silicon conduction band edge, is around $2x10^{10}$ $cm^{-2}eV^{-1}$. However, for the $Al/SiN_x/Si$ devices the maximum DIGS density, located at the same energy, is about one order of magnitude higher ($1.2x10^{11}$ $cm^{-2}eV^{-1}$). Moreover, DIGS are reach depths of 35 Å into the dielectric bulk. An overall comparison of DLTS and G-t measurements allows us to conclude that defects in samples with a SiO_2 layer are preferentially located at the interface Si/SiO_2 interface, whereas in those with silicon nitride and silicon oxynitride films there are DIGS states spatially located farther away from the interface. Moreover, although $Al/SiO_xN_y/Si$ MIS show higher interfacial state density than $Al/SiN_x/Si$ devices, they exhibit lower DIGS density values, and, therefore, better interface quality. Thermal treatments applied to $Al/SiO_xN_y/Si$ samples reduce the DIGS density to values even lower than those corresponding to Al/SiNx/SiO2/Si devices.

E3.13
Ultrathin oxynitride films formed by using pulse-time-modulated nitrogen beams. Seiji Samukawa[1], Youichi Minemura[1] and Seiichi Fukuda[2]; [1]Institute of Fluid Science, Tohoku University, Sendai, Japan; [2]Sony Corporation, Kanagawa, Japan.

Ultra thin Si oxynitride (SiO_xN_y) films have been identified as leading candidates to replace conventional SiO_2 gate dielectrics for present and future ultra large-scale integrated circuits. Remote plasma processes for top surface nitridation of thermally grown oxides have been developed and applied in complementary MOS device applications. However, it is much difficult to control the concentration and position of nitrogen in ultrathin Si oxynitride film by using plasma processing and there are many serious problems, such as plasma radiation damage and increases in interface state density due to N penetrating the SiO_2-Si interface. We investigated how the N concentration profile in a thin SiO_2 film could be precisely controlled using a pulsed N_2 neutral beam. To inject N_2 into SiO2 films, a neutral energy beam of more than a few eV is indispensable. Under the pulsed N_2 beam, N_2 was only injected into the SiO_2 film during the pulsed plasma-on time. The N peak position strongly depended on the pulse-on time and the ICP source power, and the N peak concentration was determined by total beam flux. As a result, the N peak position and N peak concentration were independently controlled by using a pulse-time-modulated N_2 neutral beam of a few tens of μseconds. The substrate temperature was also important in determining the N concentration profile in the SiO_2 film. By combining the pulsed N_2 neutral beam and a high substrate temperature of 300 degrees, the N concentration profile in a thin 2-nm SiO_2 film could be precisely controlled. A neutral-beam generation system can also drastically minimize the radiation damage caused by ions and ultraviolet photons when nitridating the top surface of thermally grown oxides.

E3.14
Thermally Grown and Reoxidized Nitrides as Alternative Gate Dielectrics. Alexandra Katharina Ludsteck[1], Waltraud Dietl[2], Hinyiu Chung[2], Carolin Tolksdorf[1], Joerg Schulze[1], Zsolt Nenyei[2] and Ignaz Eisele[1]; [1]Institute of Physics EIT 9, University of the Bundeswehr Munich, Neubiberg, Germany; [2]Mattson Thermal Products GmbH, Dornstadt, Germany.

The use of high-k materials as gate dielectric still meets a lot of unsolved problems such as thermal instability during post deposition anneals resulting in the formation of interfacial oxide layers or bad process compatibility. As long as these requirements are not

accomplished alternative gate dielectrics have to be formed by oxynitrides or gate stacks build of oxynitrides and some high-k material. In order to achieve a low equivalent oxide thickness (EOT) it is necessary to grow homogeneously thin oxynitrides which are nitrogen-rich and which have a high interface quality. Therefore we have studied the growth of thin nitrides and oxynitrides (EOT = 1 - 2nm) formed by rapid thermal nitridation in NH_3 and wet reoxidation. By varying the partial pressure of NH_3 in the process gas ambient NH_3/Ar the nitride quality could be optimized: it was found that an optimized ratio of NH_3 and Ar during nitridation improves the electrical properties of the nitrides and oxynitrides significantly. Interface state densities as low as those of dry thermal oxides and leakage current densities reduced by four orders of magnitude compared to SiO_2 of the same thickness have been obtained. Due to the high incorporation of nitrogen into the oxynitride by rapid thermal nitridation and following reoxidation the leakage current densities are also lower than those of most oxynitrides reported in literature. In addition we present data concerning the suppression of boron diffusion from p^+ poly-Si electrodes. In summary the developed oxynitrides are suitable to bridge the gap between common SiO_2 and new alternative gate dielectrics or to form gate stacks in combination with high-k materials.

E3.15
Low-temperature growth of HfO2 dielectric layers by plasma assisted MOCVD. Giovanni Bruno[1], Marianna Luchena[1], Pio Capezzuto[1], Maria Losurdo[1], Maria Michela Giangregorio[1], Davide Barreca[2] and Eugenio Tondello[2]; [1]Chemistry, CNR-IMIP and INSTM, Bari, Italy; [2]Chemistry, ISTM-CNR and INSTM, University of Padova, Padova.

Alternative gate oxides are required to minimize leakage current while mantaining high capacitance for scaling down of MOS and sub-100 nm MOSFET devices. HfO2 is considered as one of the most reliable material to satisfy such requirements because of its high dielectric constant (>25), large band gap (~6 eV), and good interface stability with Si. In this contibution, we present data on the characterization and growth of HfO2 dielectric layer on p-type Si(100) by r.f. (13.56 MHz) plasma assisted metallorganic chemical vapor deposition conditions are used: tipically a pressure of 0.3 Torr, a r.f. power of 5-20 Watt and O2-Ar gas flow rate in the range 10-50 sccm with a hafnium-t-butoxide flux of few μmol/min. The main advantage of the O2 plasma is that it allows growth of HfO2 even at room temperature avoiding oxygen deficiencies into the layer. In the present study, the deposition temperature is investigated in the range RT-250C. We found that by lowering the deposition temperature the subcutaneous oxidation of the Si substrate is minimized. In particular, the effect of surface temperature and plasma power on the thickness of the interfacial SiO2 layer and on the microstucture of the HfO2 layer going from amorphous to microcrystalline film is investigated. Structural and optical properties of the HfO2 layers are investigated by spectroscopic ellipsometry (SE) in the photon energy range 0.75-6.5 eV. Particular attention is given to the interface between the Si subtrate and the HfO2 film using SE that is a reliable non-destructive technique for the investigation of the interface layers. SE data are corroborated by XPS, XRD, AFM and C-V characteristics. XPS and SE spectra clearly show that fully oxidized HfO2 layer are grown even at RT because of the high reactivity of O-atoms from the plasma that reduces by oxygen deficiency within the layer which contributes to the dielectric leakage. The optical functions of the HfO2 layer are parameterized as a function of microstructure and impact of microstructure on the high frequency dielectric constant are determined. In situ control of the plasma phase, i.e., oxygen atoms density, hafnium precursor fragmentation is carried out by optical emission spectroscopy and mass spectrometry allowing correlation between the precursor densities and films properties. Another key point of the present study in the discussion of spectroscopic ellipsometry data used to study in real time structural and optical modifications of the HfO2/Si interface reactivity upon "passivating" treatments of the Si surface with nitrogen-based plasmas yielding an increase stability and resistance to oxidation of Si.

E3.16
Characterization of Si/SiO_2 interfaces in silicon-on-insulator by soft-x-ray resonant scattering. Eric Wiedemann, Bryan M Barnes, Zhiwei Li, Don E Savage and Max G Lagally; Materials Science, University of Wisconsin - Madison, Stoughton, Wisconsin.

As the lateral size of Si devices decreases, the thickness of individual film layers must also decrease. The interfacial rms roughness of such films should correspondingly affect device performance. Although many techniques (e.g. scanning probe microscopy) characterize surface morphology, there are few methods for quantifying the roughness of buried interfaces. By tuning synchrotron-produced x-rays either away from or on the $K\alpha_1$ absorption line of oxygen, we may distinguish between the roughness of the Si template layer on silicon-on-insulator (SOI) and the silicon/buried-oxide interface in a nondestructive fashion. We calculate that for a 50 nm Si film on a semi-infinite SiO_2 layer, off-resonant scattering cannot adequately resolve the roughness of the buried interface. For on-resonant scattering, changes in either the surface or the interfacial roughness should yield distinguishable reflectivity profiles. We show initial results of resonant scattering on model SOI systems to determine the buried interface roughness. Supported by NSF and DARPA

E3.17
On the thermal re-oxidation of silicon oxynitride.
Arturo Morales-Acevedo and Francisco Perez-Sanchez; Electrical Engineering, CINVESTAV-IPN, Mexico, D. F. , Mexico.

Based on the classical Deal and Grove's oxidation model, we propose a simple two layer model for describing silicon oxide growth during the re-oxidation of silicon oxynitride (SiO2:N) previously deposited (in N2O). Using this two layer model, and our exoperimental results, we determine the activation energy for the diffusion coefficient of oxygen through the oxynitride layer, obtaining 3.67 eV which is much higher than for diffusion of oxygen in SiO2. We explain this high activation energy as due to the presence of nitrogen within the SiO2:N layer.

E3.18
On the Interface Quality of MIS Structures Fabricated from Atomic Layer Deposition of HfO_2-SiO_2, Ta_2O_5 AND Nb_2O_5-Ta_2O_5-Nb_2O_5 Dielectric Thin Films. Salvador Duenas[1], Helena Castan[1], Hector Garcia[1], Juan Barbolla[1], Kaupo Kukli[2,3], Mikko Ritala[2] and Markku Leskela[2]; [1]Electronica, Universidad de Valladolid, Valladolid, Valladolid, Spain; [2]Chemistry, University of Helsinki, Helsinki, Finland; [3]Institute of Experimental Physics and Technology, University of Tartu, Tartu, Estonia.

Atomic layer deposition (ALD) is one of the most promising techniques to obtain high quality high K dielectric thin films. This method allows very precise and convenient control of the film thickness. Gate dielectrics deposited by ALD show important leakage reduction with respect to conventional silicon dioxide. Among the candidates to substitute silicon dioxide, metal oxides with high band gap like HfO_2 and Ta_2O_5 have been widely considered. These dielectrics have relative dielectric constants of about 18-20 and 25-30, respectively. In this work we present a study of Metal-Insulator-Semiconductor (MIS) structures based on HfO_2, HfO_2-SiO_2, Ta_2O_5 and Nb_2O_5-Ta_2O_5-Nb_2O_5 dielectric thin films deposited on silicon substrates by ALD. We focus our attention on interface quality and defect density in the dielectric. Interface states limit the carrier mobility in the MOSFET channel, whereas defects in the dielectric cause leakage currents that degrade important features of MOS devices. The interface states as well as defects inside the insulator bulk were measured by using capacitance-voltage (CV), deep level transient spectroscopy (DLTS) and conductance transient (G-t) techniques. When defects are spatially distributed into the insulator, are called DIGS or slow traps, and conductance transients can be detected by driving MIS structures from deep to weak inversion. The dielectric films were grown in an F-120 ALD reactor onto p-type silicon substrates. Film thickness ranged from 4 to 10 nm. In the HfO_2/SiO_2, the Si wafer was covered by a chemically grown SiO_2 film prior to the ALD HfO_2 film deposition in which the precursor was hafnium tetrakisethylmethylamide and water. HfO2/Si samples were grown using $HfCl_4$ or HfI_4 and water. Ta_2O_5 layers were grown from tantalum pentaethoxide and water. And, finally, Nb_2O_5-Ta_2O_5-Nb_2O_5 consisted on a multilayer stack. The Nb_2O_5 precursor was niobium pentaethoxide. In the table we summarize some of our results. Nb_2O_5-Ta_2O_5-Nb_2O_5 has the highest interface state density, whereas the minimum is obtained for HfO_2. When we look at conductance transients, we observe that no DIGS states are detected in Al/HfO_2/SiO_2/Si stacks. We also observed that postmetallization annealing in forming gas diminishes the trap interface density at expenses of increasing DIGS. The highest values were obtained for HfO2 grown at 300 °C. As for Ta2O5, we obtain intermediate values of DIGS. We clearly see that the addition of Nb_2O_5 buffer layers degrades the structure. More experimental details and discussion will be presented during the conference.

E3.19
Crystallinity and Wet Etch Behavior of HfO2 Films Grown by MOCVD. Katherine Saenger, Cyril Cabral and Paul C Jamison; IBM T.J. Watson Research Center, Yorktown Heights, New York.

The crystallinity and wet etching behaviors of ultrathin (<10 nm) HfO2 films grown by metal organic chemical vapor deposition (MOCVD) were characterized as a function of growth temperature, deposited film thickness, and post-deposition annealing treatments. As-deposited films grown at 400-500 oC to a thickness of 3 nm were amorphous (as evidenced by the absence of x-ray diffraction peaks) and slowly etchable in aqueous HF. After a post-deposition anneal at 700 oC, these films became impervious to HF and showed weak x-ray diffraction peaks at the 111 reflection of monoclinic HfO2. In contrast,

thicker (7-10 nm) films deposited at the same growth temperatures were typically impervious to HF as-deposited and showed a moderate x-ray intensity at the 111 reflection that did not increase upon post-deposition annealing. Films produced by thinning these thicker films back to 3 nm had the same crystallinity and wet etch properties as films grown to 3 nm and annealed after deposition. Implications and mechanisms will be discussed.

E3.20

Determination of Nano and Sub-Nano Fluctuations in Surface Oxides of GaSb with Br-IBAE. Kannan Krishnaswami[1], B Krejca[1], S Vangala[1], M Ospina[2], L. P Allen[3], C Santeufemio[3], C Sung[2], K Vaccaro[4] and W. D Goodhue[1]; [1]Physics and Applied Physics, University of Massachusetts, Lowell, Massachusetts; [2]Center for Advanvced Materials, University of Massachusetts, Lowell, Massachusetts; [3]Epion Corporation, Billerica, Massachusetts; [4]Air Force Research Laboratory/SNHC, Hanscom AFB, Massachusetts.

High-quality substrates with thin uniform oxide layers are critical to the development of low-power epitaxy-based GaSb electronic and electro-optic devices. In this material system the thickness and elemental composition of the oxide layers are a strong function of the surface preparation method. Here, a way of determining the thickness variations and qualitative composition of an oxide layer on GaSb has been developed using bromine ion beam assisted etching (Br-IBAE). Initial measurements show that the etch rates of most oxides formed on GaSb are much slower than that of GaSb, on the order of 1:20. Hence, nano and sub-nano fluctuations of the oxide thickness due to the oxide surface and substrate/oxide interface, result in amplified roughness fluctuations in the etched GaSb substrate. Furthermore, the overall thickness and composition of the oxide determines the etch depth, given fixed etch times and Br-IBAE parameters. In two GaSb samples with identical oxides, atomic force microscopy (AFM) images show that both the 5 and 10 minute etched samples have nearly the same roughness (~7nm), indicating that the Br-IBAE process does not change the surface morphology as a function of etch depth. The oxide thickness fluctuations in these samples are calculated to be ~0.35nm. To demonstrate the effects of overall thickness and compositional variations, another sample was prepared with each half having a different oxide, with thicknesses of 11.3nm and 28.6nm respectively. After etching both regions for 10 minutes, the etch depth of the thinner 11.3nm oxide region was ~1.2μm deeper than the thicker 28.6nm region, indicating that the compositions of the oxides were vastly different. In this paper we develop the Br-IBAE etching technique as way of characterizing oxide layers on GaSb. This method can be extended to a number of material systems.

E3.21

Theoretical study of reaction mechanisms of $ZrCl_4$ with hydrated and hydroxlated Si(100) surfaces. Max Petersen, Accelrys, Inc., San Diego, California.

The ever increasing need of device integration in semiconductor technology has reached a stage were quantum mechanical tunneling across the widely used SiO_2 gate dielectrics becomes an issue. The most promising approach to overcome this limitation is to replace SiO_2 with materials with higher tunnel barriers - the so called high k materials. One of the candidates in this goup of materials is ZrO_2, typically grown by highly controlled growth mechanisms such as atomic layer deposition (ALD). In the ALD experiment the growing surface is exposed alternatingly with $ZrCl_4$ and H_2O. One of the technological challenges is to avoid the formation of SiO_2 at the interface to the Si(100) substrate. Therefore studying the reaction of $ZrCl_4$ with the Si(100) surfaces might be a first step to understand how this interface might form. Hydrated and hydroxlated Si substrates are studied in order to understand any deterioration of the Si-ZrO_2 interface due to formation of SiO_2. Particularly, a synchronous transit method combined with density functional theory is used to locate transition states of these reactions. The simulation results show that $ZrCl_4$ preferentially reacts at OH groups present of the substrate, whereas reactions at hydrated substrates is energetically clearly disfavored.

E3.22

High-k ZrO2 Gate Dielectric on Strained-Si.
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Fundamental limits to CMOS scaling are rapidly approaching as devices are scaled below 50 nm range. New methods and materials for CMOS fabrication must be investigated to allow continued device improvement [1]. Gate leakgae reduction in ultrathin gate dielectrics is the main motivation for the serach of high-k materials. ZrO2 is being considered as a potential candidate for the replacement of SiO2 due to its high dielectric constant and low leakage current. Recently, the use of strained-Si has attracted considerable attention for advanced CMOS devices beacuse of enhancement of in-plane mobility of both the electrons and holes compared to bulk-Si [2]. In this paper, we present the results of our study on the growth and structural characterization of UHV-compatible LPCVD grown strained-Si layers (on both step- and lineraly-graded relaxed SiGe virtual substrates) on which high-k ZrO2 ultrathin films have been deposited using microwave plasma CVD at a low temperature (150 deg C). The strained-Si layers have been charcterized using AFM, TEM and Raman spectroscopy. The layers are 20 nm in thickness and have been characterised with a strain of 3.55 GPa. The electrical properties of the deposited ZrO2 films are also presented. The C-V and G-V characteristics have been used to calculate the interface trap density, near the midgap energy, and the fixed charge density. These are found to be 2.24E12 per cm2ev and 1.45E11 per cm2, respectively. The ZrO2 films show a linear relationship between current density and the applied bias. The conduction mechanism is found to be dominated by the Poole-Frenkel mechanism. The computed dynamic permittivity of the ZrO2 films was found to be ~9.94. We have demonstrated the feasibility of integration of high-k ZrO2 gate dielectric with strained-Si for the first time, as a possible candidate for future strained-Si CMOS applications. [1] International Technology Roadmap for Semiconductors, 2002 Update. [2] C. K. Maiti et al., Solid-State Electron., vol. 41, 1997, p. 1863.

E3.23

Praseodymiun silicate formation by post-growth high temperrature annealing. Akira Sakai[1], Shinsuke Sakashita[1], Mitsuo Sakashita[1], Shigeaki Zaima[2], Yukio Yasuda[1] and Seiichi Miyazaki[3]; [1]Department of Crystalline Materials Science, Graduate School of Engineering, Nagoya University, Nagoya, Japan; [2]Center for Cooperative Research in Advanced Science and Technology, Nagoya University, Nagoya, Japan; [3]Department of Electrical Engineering, Graduate School of Advanced Sciences of Matter, Hiroshima University, Hiroshima, Japan.

Research on new high-k dielectric materials to replace SiO_2 gate dielectrics has been recently accelerated by continuous miniaturization of Si metal-oxide-semiconductor (MOS) devices. This is because the scaling to the diminished size of MOS structures requires simultaneous reduction of SiO_2 gate dielectric layer thickness, leading to an increase in tunneling leakage current and degraded dielectric reliabilty. In the regime of exploiting and developing new high-k materials compatible with the MOS device manufacturing, the stability of the high-k layers in contact with Si during high temperature annealing is one of crucial factors. It is generally reported that the thermal instability results in the growth of unwanted low-k interface layers, such as SiO_2 and silicate, and a noticable decrease in the effective capacitance is eventually obtained. Thus the preparation of thermally-robust high-k layers is an urgent issue to meet the stringent requirement for the next generation MOS device technology. In this work, we focus on praseodymiun silicate (Pr-silicate) which meets both requirements for having a high dielectric constant and high thermal stability. We present an approach to form Pr-silicate by using deposition of Pr_2O_3 layers on Si substrates and high temperature post-growth rapid thermal annealing (PORTA). In experiments, Pr_2O_3 films with a thickness ranging from 7 to 10 nm were deposited on hydrogen-passivated Si(111) substrates at a temperature between 300 and 700°C using a moelcular beam epitaxy system with a base pressure of 1×10^{-10} Torr. A powder-packed ceramic Pr_6O_{11} was used for electron beam evaporation. The pressure during deposition was in the range of 10^{-8} Torr and, in some case, an oxygen gas was intentionally introduced up to 5×10^{-7} Torr. The films were then subjected to PORTA at a temperature of 1000°C for 15 sec in an N_2 environment. It has been revealed by transmission electron microscopy that as-deposited films typically have a hexagonal or cubic Pr_2O_3 phase grown epitaxially on Si(111) with 0.5- to 2-nm-thick interface layers. Structural variation depending on the growth condition was also seen; lowering the temperature and the oxygen partial pressure during deposition promotes epitaxy. However, the films grown under the oxygen deficient conditions ferequently show high leakage currents in current-voltage characteristics. On the contrary,PORTA drastically alters the film structure into an amorphous phase. The obtained film was completely homogeneous and had no interface layers. We used X-ray photoelectron spectroscopy to measure chemical composition of the films and confirmed the intermixing of Si into Pr_2O_3 to form Pr-O_x-Si_y alloys (Pr-silicate). Preliminary results for a typical dielectric constant and a leakage current density for Pr-silicate grown under an optimal growth condition are 20 and 3×10^{-9} A/cm^2 at +1 V relative to flat band voltage for an equivalent oxide thickness of 1.8 nm, respectively.

E3.24

Analysis of N2, NH3 annealing effect on HfxAlyOz gate

dielectric films grown by chemical vapor deposition using a single molecular precursor. Suk Woo Lee, Jaehoo Park, Hong Bae Park, Moonju Cho and Cheol Seong Hwang; School of Materials Science & Engineering, Seoul National University, Seoul, South Korea.

HfxAlyOz gate dielectric films were deposited on SC1 and HF-cleaned Si wafers by chemical vapor deposition (CVD) method using Hf-Al single molecular precursor [HfAl(OC3H7)5(OC4H8OCH3)2]. HfxAlyOz was treated under N2 and NH3 atmospheres by rapid thermal annealing at 600, 700, 800, and 900c for 30 s, respectively. The as-deposited HfxAlyOz films were amorphous and crystalline at deposition temperatures of 380c and 430c, respectively. Hf and Al concentrations in the films were very uniform through the full depth range of the film. 380c deposited HfxAlyOz films showed small CET variations during N2 and NH3 rapid thermal annealing up to 800c but suddenly degrades at 900c. Flat band voltage slightly increased with the increasing annealing temperature. However, the flat-band voltage was remained at the ideal value at 600 and 700c rapid thermal annealing, and the hysteresis in the capacitance-voltage plots became very small as a result of the rapid thermal annealing. HfxAlyOz films showed feasibility as a high-k gate dielectric film.

E3.25
Silicide Formation at ZrO_2/Si and HfO_2/Si Interfaces Induced by Ar^+ Ion Bombardment. Yuri Lebedinskii[1], Andrei Zenkevich[1], Dmitrii Filatov[2], Dmitrii Antonov[2], Julia Gushina[2] and Georgii Maximov[2]; [1]Moscow Engineering Physics Institute, Moscow, Russian Federation; [2]University of Nizhny Novgorod, Nizhny Novgorod.

Ar^+ ion bombardment is used for etching of thin films in surface analysis techniques (XPS, AES, SIMS, etc.) widely for depth profiling of the elements concentration as well as for ion milling of samples in TEM. At the same time, it is known that ion etching may affect both elementary and chemical compositions of the surface layer. To detect possible effect of ion bombardment, in situ XPS investigation of the interface forming during the growth of high-k dielectric layer on Si(100) was performed and compared to that resulting from subsequent ion etching of the grown metal oxide layer. Reactive pulsed laser deposition of Zr and Hf in oxygen ambient was employed to grow step-by-step ultrathin ZrO_2 (HfO_2) layers up to the thickness ~7 nm. Zr^{4+} and Hf^{4+} were the only chemical states detected with XPS at high-k dielectric / Si interface. Subsequent etching of the grown layers with Ar^+ ions at the energy E=1.5÷3.5 keV resulted in the appearance of components in XPS spectra unambiguously attributed to Zr (Hf) in silicide form when metal oxide / Si interface was approached. The thickness of the forming silicide layer is estimated to be ~2 nm. It should be noted that no silicates were observed. *Exsitu* combined Scanning Tunneling Microscopy/Atomic Force Microscopy (STM/AFM) was used to monitor the surface morphology and the electronic properties of the ZrO_2/Si (HfO_2/Si) samples after ion etching. The tunneling spectra recorded on the etched surface with a conductive cantilever while the feedback was maintained by AFM corroborate the formation of silicide layer on Si. The work has been supported by Joint Russian American Program "Basic Research and Higher Education" (BRHE) sponsored in parity by US Civilian Research and Development Foundation (CRDF) and Russian Ministry of Education, Award # REC-NN-001.

E3.26
Laser Assisted Molecular Beam Deposition of Hafnium Oxide and Zirconium Oxide Thin Films for Gate Dielectrics Applications. James F. Garvey[1,3], Robert L DeLeon[3], Gary S. Tompa[3], Spyros Gallis[2], Richard Moore[2], Harry Efstathiadis[2] and Jean-Claude Fouere[4]; [1]Chemistry, SUNY/Buffalo, Buffalo, New York; [2]School of Nanoscience and NanoEngineering, University at Albany - SUNY, Albany, New York; [3]AMBP Tech Corp., Amherst, New York; [4]SOPRA Inc., Westford, Massachusetts.

High dielectric constant (k) hafnium oxide (HfO_2), and zirconium oxide (ZrO_2) thin films have successfully been deposited on silicon substrates by Laser Assisted Molecular Beam Deposition (LAMBD). The films were grown at the substrate temperature of 300 ^oC and at process pressure ~1 Torr. The LAMBD process uses a pulsed laser to create a hot plasma to ablate material from a rotating target rod. The target rod can be practically any material: metal or non-metal, a pure substance, or a layered composite. Oxygen was used as the carrier gas to entrain the ablated material in a cooling expansion process. The choice of carrier gas exerts considerable control over the process; it can control both the chemical composition and the temperature of the ablation plasma.. Depositions on silicon substrates yielded controlled thicknessess of 5 nm to 100 nm of stoichiometric HfO_2, and ZrO_2 films. Structural and chemical characterization of the films were performed by Auger electron spectroscopy (AES), Rutherford Back-scattering (RBS), x-ray diffraction (XRD) spectroscopy, and scanning electron microscopy (SEM). Optical characterization was performed by means of spectroscopic ellipsometry (SE) and x-ray reflectivity (XRR) measurements. In this work the film microstructure will be compared to the microstructure of films deposited by LAMBD at room temperature.

E3.27
Room Temperature Fabrication of $Al_2O_3/TiO_2(TiAlO_x)/Al_2O_3$ Nanolaminates for High-k Gate Dielectrics. Wei Fan[1,4], Sanjib Saha[1], Bernd Kabius[1], Jon M Hiller[1], John A Carlisle[1], Orlando Auciello[1], Lisa Edge[2], Darrell G Schlom[2], Jurgen Schubert[3,2], RPH Chang[4], Ciro M Lopez[5] and Eugene A Irene[5]; [1]Materials Science Division, Argonne National Laboratory, Argonne, Illinois; [2]Department of Materials Science and Engineering, Pennsylvania State University, University Park, Pennsylvania; [3]Institut fur Schichten und Grenzflachen ISG1-IT, Forschungszentrum Julich GmbH, Julich, Germany; [4]Department of Materials Science and Engineering, Northwestern University, Evanston, Illinois; [5]Chemistry Department, University of North Carolina, Chapel Hill, North Carolina.

The application of ultra-high k (ϵ_r>50) TiO_2 as a gate dielectric is hampered primarily by its high leakage current as the result of a close zero offset barrier to Si and its instability with Si and the poly-Si gate in CMOS. On the other hand, Al_2O_3 with low permittivity (ϵ_r=9) exhibits a large band gap (E_g=8.8 eV) and excellent thermal stability with Si. To take the advantages of the combined properties of Al_2O_3 and TiO_2, nanolaminate $Al_2O_3/TiO_2/Al_2O_3$ and $Al_2O_3/TiAlO_x/Al_2O_3$ multilayers were developed for a dielectric structure with high permittivity and good thermal stability. The layered dielectric stacks were fabricated by two distinct methods: a) post-deposition oxidation of sputter-deposited Al/Ti(TiAl)/Al metallic multilayers with atomic oxygen and b) oxidation during deposition by co-depositing O_2 and Al or Ti in an MBE system. For the first method, the top Al_2O_3 layer inhibits oxidation of the Al/Ti(TiAl)/Al metal stack by preventing oxygen diffusion, resulting in a leaky dielectric stack due to the incomplete oxidation of the central Ti layer. A modified two-step oxidation process, involving oxidation of the Ti(TiAl)/Al structure followed by deposition and oxidation of the top Al layer, was performed at low temperature to overcome the incomplete oxidation problem of the central TiO_2 layer, while preventing the formation of SiO_x at the Si interface. For the second method, molecular beam deposition (MBD), we investigated the minimum oxygen pressure needed to oxidize Al and Ti species and their combination (to avoid producing a SiO_2 interfacial layer), using a quartz crystal microbalance. Fully oxidized $Al_2O_3/TiO_2(TiAlO_x)/Al_2O_3$ gate dielectric layered structures with sub-1.0 nm EOT were achieved on Si at room temperature using both methods described above. A detailed comparison between the structural and dielectric properties of sputter- and MBD-deposited dielectric layers will be discussed. * This work was supported by the U.S. Department of Energy, BES-Materials Sciences, under Contract W-31-109-ENG-38.

E3.28
Characterization of Titanium-Aluminum Oxide Thin Films for New Generation of CMOS Gates via Spectroscopic Ellipsometry. Ciro M Lopez[1], N A Suvorova[1], W Fan[2], O Auciello[2] and E A Irene[1]; [1]Chemistry, University of North Carolina-Chapel Hill, Chapel Hill, North Carolina; [2]Materials Science Division, Argonne National Laboratory, Argonne, Illinois.

New Titanium-Aluminum oxide thin films were fabricated on Si(100) substrates by ion-beam sputter deposition of a Ti-Al alloy target and subsequent oxidation at temperatures ranging from R.T. to 500°C. These films are being investigated as candidates for the new generation of gate oxides, since they exhibit properties compatible with the requirements of next generation CMOS gates. A combination of Rutherford backscattering analysis to obtain film composition, and cross-sectional transmission electron microscopy to reveal thickness and the film stack structure were used to provide information, in order to construct an optical model for the material, based upon SE analysis. Spectroscopic ellipsometry on Ti-Al alloy oxide films with various thicknesses yielded the optical properties of these films. The optical properties were also modeled using Lorentz oscillators. Physical thickness of titanium-aluminum oxide and interfacial SiO_2 thickness was determined from the model and compared with values obtained from other analytical techniques. From a Tauc plot the band gap was estimated to be 3.8 eV. *- This work was supported by the US Department of Energy, BES-Materials Sciences, under Contract W-13-109-ENG-38; NSF/ONR under Contract N00014-89-J1178 (UNC-CH)

E3.29
High-k Dielectric Characterization by combined VUV Spectroscopic Ellipsometry and X-Ray Reflectometry. P Boher[2], P Evrard[2], C Defranoux[2], A Darragon[1], Lianchao Sun[1], J.C. Fouere[1], J.L. Stehle[2], E Bellandi[3] and H Bender[4]; [1]SOPRA Inc, Acton, Massachusetts; [2]SOPRA SA, Bois Colombes, Paris, France;

[3]STMicroelectronics, Agrate Brianza (MI), Italy; [4]IMEC, Leuven, Belgium.

At present, new high-k dielectric materials are being intensively investigated to replace the silicon dioxide as gate dielectric for the next generation of electronic devices. Several candidate materials (such as ZrO2, HfO2, Al2O3) and deposition processes are currently under investigation. Because the layer thickness which is required in the next generations of devices is of the order of few nanometers, a precise determination and control of layer thickness will be mandatory. Although spectroscopic ellipsometry (SE) is well established non-contact, non-destructive and precise technique for determining thickness and optical properties of thin films, it becomes more difficult to obtain this information unambiguously and simultaneously for ultra-thin films with traditional SE alone because of possible high correlations between film structure and optical properties. In this study, a complementary non-destructive Grazing X-ray reflectometry (GXR) was first used to extract the thickness of such ultra thin films. Then, the optical properties of the films were determined with Vacuum Ultra-Violet Spectroscopic Ellipsometry (VUV-SE), which covers a wide spectral range down to 140nm wavelength. Within the VUV range, all the high-k dielectrics under evaluation are no longer transparent. This enhances the capability of using SE for such high-k dielectric film characterization. HfO2, Al2O3 and HfAlOx films were deposited on silicon substrates with Atomic Layer Deposition (ALD) technique. HfCl4 and Al(CH3)3 mixing with H2O were used as precursors for HfO2 and Al2O3 respectively. Al concentration in HfAlOx was varied by changing the relative number of HfCl4 and Al(CH3)3 cycles (2:1, 1:1 and 1:2). The characterization results show a strong dependency between aluminum concentration and optical constants (refractive index and extinction coefficient) in VUV range. This proposes a way to quantatively determine Al concentration in HfAlOx films and their thickness.

E3.30
Strontium Titanate Thin Films on Thermally Oxidized and Bare Si Substrates. Natalya A. Suvorova[1], Ciro M. Lopez[1], Alexandra A. Suvorova[2], Martin Saunders[2] and Eugene A. Irene[1]; [1]Department of Chemistry, University of North Carolina-Chapel Hill, Chapel Hill, North Carolina; [2]Centre for Microscopy and Microanalysis, University of Western Australia, Crawley, Western Australia, Australia.

Among the choices for the high dielectric constant (K) materials for future generation MOSFET application, strontium titanate (STO) is one of the promising candidates for alternative gate oxide. Replacement of SiO_2 by high-K dielectrics poses several problems. The major one is a production of high level of interface states (D_{it}) compared to that of SiO_2 on Si. An insertion of a thin SiO_2 layer prior the growth of STO thin film is a simple solution that helps to limit reaction with Si substrate and attains a high quality interface. However, the combination of two thin films reduces the overall K of the dielectric stack. An optimization of the SiO_2 underlayer in order to maintain the interface quality yet minimize the effect on K is the focus of this work. The results from our study are presented with emphasis on the key process parameters that improve the dielectric film stack. For in-situ growth characterization of STO film grown on thermally oxidized Si substrates spectroscopic ellipsometry has been used. Studies of material properties have been complemented with analytical electron microscopy. Electrical characterization has been employed using the Pt/STO/Si structures. From conductance-voltage analysis, the interface trap density D_{it} was observed to significantly decrease for the capacitors grown on oxidized Si substrates and annealed in forming gas.

E3.31
Optical and Dielectrical Properties of Eu- and Y-Polytantalate Thin Films Grown by RF Sputtering on Si Substrates. Vladimir Vasilyev[1], Alvin Drehman[1], Helen Dauplaise[1], Lionel Bouthillette[1], Mark Roland[2], Alex Volinsky[3] and Stefan Zollner[3]; [1]Sensors Directorate, Air Force Research Laboratories, Hanscom AFB, Massachusetts; [2]Solid State Scientific Co., Hollis, New Hampshire; [3]Semiconductor Products Sector, Motorola, Inc., Tempe, Arizona.

We report further results of our study of one family of thin film rare-earth polytantalates, $RETa_7O_{19}$ (RE=Eu, Tb, Y, Tm, Nd), which exhibit highly efficient photo-luminescent characteristics. Earlier we have shown [1] that oriented polycrystalline thin films of stoichiometric Eu-Y polytantalates ($Eu_xY_{1-x}Ta_7O_{19}$, x=0-1.0) can be grown by RF magnetron sputtering on Si, fused silica and sapphire substrates. These films exhibited an intense red emission under UV excitation. Because Ta and rare-earth oxides are currently being considered as an alternative to silicon dioxide as high-k gate dielectrics for CMOS devices scaling below 0.1 μm, these films of rare-earth tantalates could be also of interest as new materials with high dielectric constant. This study is a first attempt to investigate basic physical properties of thin films of polytantalates containing Eu, Y, and their solid solutions. Films with the thicknesses of 30 to 500 nm were deposited on Si substrate at room temperature by RF magnetron sputtering in Ar atmosphere and post-annealed in oxygen at 900 to 1000 ^oC. Using x-ray diffractometry, AFM, SEM, HR-TEM, spectroscopic ellipsometry, and standard dielectric testing procedure, the values of thickness, surface roughness, band-gap, refractive index, low-frequency dielectric constant, and breakdown and leakage current were determined for the as deposited amorphous and post-annealed crystalline films. Also we have studied structural and morphological properties of deposited films and the Film/SiO_2/Si interface, and compared that to luminescent and dielectric measurements.
*supported by the Air Force Office of Scientific Research, through the National Research Council Associateship Program. 1.V.Vasilyev, A. Drehman and L. Bouthillette, Characterization of Eu- and Y-polytantalate Films Deposited by RF Diode Sputtering. MRS Symp. Proc., Vol. 749, W5.8.1.

E3.32
Characteristics of hetero structures composed of oxides and foreign compound materials on Si for the future novel devices. Yoo YoungZo[1], Song JeongHwan[1], Parhat Ahmet[1], Nakajima Kiyomi[1], Chikyow Toyohiro[1,2], Konishi Yoshinori[3] and Koinuma Hideomi[1,2,4]; [1]Nano-Material Assembly Group, National Institute for Materials Science, Tsukuba, Ibaraki, Japan; [2]CREST, JST, Japan; [3]Fuji Electric Corporate Research and Development., Yokosuka-city, Japan; [4]Materials and Structures laboratory, Tokyo Institute of Technology, Yokohama, Japan.

Over the last decades, there has been increasing interest in the development in functional oxide devices, such as ferroelectric memories and optoelectronics. One of the most fundamental but fascinating structures for device applications is heterojuction between oxides and foreign materials, where metals are involved. To fabricate such devices, selecting proper substrates is also crucial because it does not only affect the device performance, but also open new possibilities for realizing novel devices. In this respect, Si must be one of the highest potential substrates due to matured process technology. In this presentation, we demonstrate two types of heterostructures on Si, namely oxide/sulfide and metal/oxide hetero structures respectively. First, heterojuntion composed of SrTiO3 and wide bandgaps (4.5 eV) are fabricated on p-Si and their structural and electrical properties are investigated. The second, Heterostructures composed of metal alloy on ZnO are fabricated and their electrical properties are described. Combinatorial method is applied for the quick optimization and the systematic study of those obtained hetrostructures in both experiments.

E3.33
The adoption and nitridation of Al2O3 inter-layer for improving thermal stability and flat-band behavior of HfO2 gate dielectric films grown by atomic layer deposition. Hong Bae Park, Moonju Cho, Jaehoo Park, Suk Woo Lee and Cheol Seong Hwang; School of Materials Science and Engineering, Seoul National University, Seoul, South Korea.

HfO2/Al2O3 gate dielectric thin-film stacks were deposited on HF-cleaned Si wafers using an atomic-layer-deposition (ALD) technique. A 2.3-nm-thick Al2O3 inter-layer was grown at 450oC using Al(CH3)3 and O3, and 4 to 5-nm-thick HfO2 films were grown on Al2O3 at 400oC using HfCl4 and H2O as a precursor and an oxidant. The Al2O3 inter-layer was treated under a NH3 atmosphere at 790oC for 40 sec prior to HfO2 deposition with and without the rf-plasma. The plasma-nitridation increased the Al2O3 inter-layer thickness by approximately 0.9 nm and decreased the overall capacitance, whereas thermal-nitridation did not increase the Al2O3 inter-layer thickness, and the overall capacitance was the same as that of the non-treated HfO2/Al2O3 stack. The thermal stability of the capacitance density was also improved by the nitridation of the inter-layer. The flat-band voltage was controlled to the ideal value, and the hysteresis in the capacitance-voltage plots of the HfO2/Al2O3 stacks became very small as a result of thermal-nitridation. Furthermore, the interface trap density of the sample with the nitrided Al2O3 inter-layer decreased from that of the non-treated sample by almost one order of magnitude.

E3.34
First-principles study of ultra-thin SrO, TiO_2 and $SrTiO_3$ films on MgO(001). Petr Casek, Fabio Finocchi and Claudine Noguera; Groupe Physique des Solides, Universite Paris 6-7 and CNRS, Paris, France.

Thin oxide films exhibit many attractive properties such as colossal magneto-resistance, ferro-electricity, and superconductivity. $SrTiO_3$, in particular, has been suggested as a possible candidate to replace SiO_2 in electronic devices [1]. However, the strong interplay between the atomic and electronic degrees of freedom makes the control of the

microscopic structure of oxide-oxide interfaces an important challenge for practical applications. In this context, a detailed analysis of the first stage of the epitaxial growth of strontium titanate on the MgO(001) surface is performed [2], based on the density-functional theory. Several configurations for the ad-layers are considered. We show that the cube-on-cube TiO_2/MgO contact is favoured among all the stoichiometric interfacial configurations, because of the formation of quite strong interfacial bonds favouring stress relaxation. The SrO/TiO_2 ad-layer shows many analogies with much thicker adsorbed $SrTiO_3$ films. We also analyse the relevance of chemistry on the stability of the interface, considering the most frequent defects, such as O vacancies (on both sides of the interface) and stacking faults in the $SrTiO_3$ systems, better known as Ruddlesden-Popper phases $Sr_{n+1}Ti_nO_{3n+1}$ [3]. The electronic properties of these interfaces are in general strongly dependent on the local atomic environment. In order to understand such an interplay, the Local Density of States (LDOS), the charge transfers and the band lineup at the interface are studied systematically and interpreted in terms of the theory of Atoms-In-Molecules [3]. We find that the electronic structure is very sensitive to the actual interface stoichiometry, exhibiting electron localization phenomena and/or an open-shell character. The interfacial charge transfer is also deeply affected, which can play a role on the electron transport across the interface. [1] R.A. McKee, F. J. Walker, and M. F. Chisholm, Science 293, 468 (2001). [2] P.Casek, S.Bouette, F.Finocchi, and C. Noguera, submitted. [3] C. Noguera, Phil. Mag. Lett. 80, 173 (2000), and references therein. [4] R. F. W. Bader, "Atoms in Molecules, a quantum theory" (Clarendon Press, Oxford, 1990).

E3.35
High Temperature AlN Dielectrics for Passivation of SiC Power Devices. B Nagaraj[1], Shiva S Hullavarad[1], R D Vispute[1], T Venkatesan[1], D Hall[1], D Habersat[2], A Lelis[2], M Ervin[2], B Geil[2] and C J Scozzie[2]; [1]Center for Superconductivity Research, University of Maryland, College Park, Maryland; [2]US Army Research LAboratory, Adelphi, Maryland.

AlN has excellent properties of high breakdown strength, a thermal conductivity and dielectric constant. It grows epitaxially on 6H SiC as they have hexagonal crystal structure. In this work we report the passivation of SiC based devices by two main approaches. In first part, pulse laser deposition is used to deposit AlN from high purity AlN target pellet on SiC based devices. A novel technique of Off-Axis Rotation is utilized to cover the sidewalls to achieve the deposition of best quality AlN on side walls of device. In second approach, we use RF Sputtering of AlN from a high purity Al (99.99%) pellet in Ar and N2 atmosphere. The technique of sputtering provides sufficient coverage of sidewalls than the pulse laser deposition. A comparison is made between the crystalline quality of AlN films deposited by two techniques using X-ray diffraction. The morphology of the film, which is expected to cover the sidewalls uniformly, is monitored by scanning electron microscopy. The relative merits of the pulsed laser deposited and rf sputtered AlN films are investigated from the point of view of aspect ratio, leakage characteristics and interface properties.

SESSION E4: High-K Oxides, Metal Gates and Integration
Chairs: Andre Stesmans and Akira Toriumi
Tuesday Morning, December 2, 2003
Room 207 (Hynes)

8:30 AM E4.1
Thermal Stability and Electrical Properties of Ru Films by Selective MOCVD on ALD HfO_2 and ALD $LaAlO_3$.
Jaydeb Goswami[1], Diefeng Gu[1], Anirban Das[1], Wei Cao[1], Sandwip K. Dey[1], Steven Marcus[2], Henk de Waard[2] and Chris Werkhoven[2]; [1]Arizona State University, Tempe, Arizona; [2]ASM America, Inc., Phoenix, Arizona.

Selective deposition of Ruthenium (Ru) films was carried out on patterned HfO_2 and $LaAlO_3$ surfaces (deposited by atomic layer deposition or ALD) using a liquid-source metalorganic chemical vapor deposition (MOCVD) technique. The Ru films (30-200 nm) were deposited in the mass and kinetically controlled regimes at temperatures (T_{sub}) between 250 and 350 °C and a total pressure of 1 Torr. Note, oxygen-assisted pyrolysis was used to decompose the Bis (2,2,6,6-tetramethyl-3,5-heptanedionato)(1,5-cyclooctadiene) Ru (or $Ru(THD)_2COD$) precursor and to reduce the carbon contamination. In the kinetically controlled regime (250-270 °C), the activation energy was 136 kJ/mol, and Ru films deposited in this regime exhibited nearly 100% step coverage. The Ru films deposited at T_{sub} of 260 °C showed a highly dense and polycrystalline nanostructure (grain size: 2-15 nm) with amorphous grain-boundaries and an interfacial layer between Ru and HfO_2 surface; from RBS, XPS, HRTEM, and EELS, the amorphous layer was found to be RuO_x. However, the higher sticking coefficient of $Ru(THD)_2COD$ in the mass transport controlled regime at 350 °C resulted in poor step coverage of only 50%. Moreover, when T_{sub} was raised to 425 °C and a very high oxygen flow-rate of 500 sccm was used, phase-pure and polycrystalline RuO_2 was deposited on HfO_2. The electrical resistivity (ρ) for the as-deposited Ru films (75-160 nm) was ~15 $\mu\Omega$ cm, but it increased rapidly below 40 nm. The Ru films on HfO_2, annealed at 1050 °C in vacuum, showed a higher degree of (001) texture, stronger temperature dependence of ρ, and higher residual resistivity ratio (RRR = ρ_{293K}/ρ_{10K}) of ~13 compared to as-deposited films. The workfunctions of as-deposited Ru by selective MOCVD on HfO_2 and $LaAlO_3$ surfaces, determined from the capacitance-voltage measurements, were ~5.3 and ~4.9 eV, respectively. The variation of the workfunction after various annealing treatments will be presented and discussed.

8:45 AM E4.2
Schottky Barriers at Transition-metal/Strontium-titanate Contacts. Matous Mrovec[2,1] and Christian Elsaesser[1]; [1]Fraunhofer IWM, Freiburg, Germany; [2]IZBS, University of Karlsruhe, Karlsruhe, Germany.

Local electronic structures at coherent interfaces between cubic (001)-oriented $SrTiO_3$ substrates and transition-metal films have been studied by means of the density functional theory with the mixed-basis pseudopotential approach. The main focus of this work is to investigate the influences of the chemical composition, atomistic structure and externally applied electric fields on the Schottky barrier of the studied metal/ceramic contacts. The calculations have been performed for six transition metals from groups VI.A (Cr, Mo, W) and X.A (Ni, Pd, Pt) in order to analyse the effects of both varying atomic size and different electronic structure. Furthermore, in the cases of Ni and Cr the role of intermediate oxide monolayers is examined.

9:00 AM E4.3
First-Principles Calculation of the Work Function of Metals on High-K Metal Oxides. L. R. C. Fonseca[1], A. Knizhnik[2], I. Iskandarova[2], A. Bagatur'yants[2], A. A. Demkov[3], S. B. Samavedam[3], J. Schaeffer[3], B. White[3] and P. J. Tobin[3]; [1]Motorola Inc., Tempe, Arizona; [2]Kintech Technologies Ltd., Moscow, Russian Federation; [3]Motorola Inc., Austin, Texas.

The work functions of Mo, TiN, HfN, and TaN have been calculated on SiO_2, HfO_2, and vacuum using first principles techniques, and compared to experimental values. The electronic properties calculated for the model structures strongly depend on the atomic level structure of the model. Since the atomic structure in most cases cannot be determined by a direct experiment, the model structures need to be chosen with great care. We will show how total energy calculations and simple thermodynamic arguments can be used to make a reasonable selection. The impact of a bonding configuration on the metal work function will be discussed. We will also show how the bulk-derived Fermi level pinning parameters and the charge neutrality level for HfO_2 and SiO_2 compare with values extracted from the data and interface calculations. Finally, we will identify Fermi pinning properties that are intrinsic to the dielectric and those that are connected to the metal gate through comparison between different metals and from our previous results for PolySi/HfO_2 interfaces.

9:15 AM E4.4
Thermal Stability of PVD TaSiN with high-k gate dielectrics.
Michael Gribelyuk[1], Alessandro Callegari[2], Cyril Jr Cabral[2] and Vijay Narayanan[2]; [1]Semiconductor Resarch and Development Center, Microelectronics Division, IBM, Hopewell Junction, New York; [2]Semiconductor Research and Development Center, Research Division, T. J. Watson Research Center, IBM, Yorktown Heights, New York.

Gate stacks consisting of Si/High-k dielectric/TaSiN are shown to be thermally stable during high temperature annealing. The stacks have been analyzed by a combination of high resolution TEM and small probe electron energy loss spectroscopy (EELS). The high k dielectrics studied were ALD grown ZrO2, Al2O3 and HfO2. The TaSiN/dielectric interface was found to be rough due to damage incurred during PVD TaSiN deposition. As-deposited, TaSiN is predominantly amorphous with some small crystallites less than 2 nm in diameter. Stacks annealed at 1000C in nitrogen showed no sign of a TaSiN/dielectric interfacial reaction both by EELS and HRTEM, thus proving that the material is thermally stable on high-k oxide films. A workfunction of ~ 4.4eV was measured on capacitor structures produced from these stacks using the Vfb vs EOT measurement method. The data has also shown flat band shifts and wide hysterisis, which may be due to fixed charges formed during PVD TaSiN deposition, high-k film deposition or due to insufficient post metal anneals of a TaSiN/dielectric gate stack. To reduce damage during electrode deposition alternative deposition methods might have to be considered for successful implementation of TaSiN as potential gate material in future generations of CMOS devices

10:00 AM E4.5

Study of metal gate work function modulation using plasma and SiH4 treated TiN thin films. Fillot Frederic[1], Sylvain Maitrejean[1], Thierry Farjot[1], Bernard Guillaumot[2], Bernard Chenevier[3] and Gerard Passemard[2]; [1]DTS, CEA-LETI, Grenoble, isere, France; [2]STmicroelectronics, Crolles, isere, France; [3]UMR 5628, LMGP-CNRS, Grenoble, isere, France.

As gate oxide thickness decreases, the capacitance associated with the depleted layer in poly Silicon gate becomes significant, making it necessary to consider alternative gate electrodes. TiN films elaborated with TiCl4 precursor is widely studied as metal gate in semi conductor technology. In this work, a study of TiN metal gate deposited by MOCVD using TDMAT precursor is proposed. N2,H2 plasma application and SiH4 treatment after TiN thin film growth modify composition and microstructure. Consequently, they alter the physical properties of films. Such treatments may be a way to modulate work function and thus threshold voltage. A series of metal layers was deposited in a chamber using a commercial 8 inch wafer deposition tool. In this study, structural and compositional properties of TiN were correlated with work function measurements. Firstly, the evolution of the composition (Carbon content) was studied with spectroscopy (AES, SIMS) as a function of plasma and SiH4 treatments; details on the microstructure (XRR, XRD, AFM) will be also given. Secondly, MOS structures were processed on uniformly doped p-type wafers. C-V curves of capacitors are used to estimate the flat band voltage and permit to extract the work function, the effect of fixed charges in oxide and the density of interface states. It is shown that as-deposited amorphous films exhibit a work function of 4.4eV. Silicidation is shown to increase this work function. Thin films properties are not impacted by anneal treatments. Work function stability is tested at 450C, 900C and 1050C. Thermodynamic compatibility with gate oxide is verified thanks to experimental results and calculations.

10:15 AM E4.6

Mechanism of Self-Organized Decomposition of the Si Template Layer in Ultrathin Silicon-on-Insulator. Bin Yang[1], Pengpeng Zhang[1], Feng Liu[2] and Max G Lagally[1]; [1]University of Wisconsin-Madison, Madison, Wisconsin; [2]Unversity of Utah, Salt Lake city, Utah.

Silicon-on-insulator (SOI) is rapidly becoming a mainstream substrate in microelectronics fabrication. SOI technology greatly reduces the power consumption and improves the performance of CMOS transistors. The Si template layer on ultrathin SOI (001), which can be as thin as several nanometers, is thermally unstable and decomposes at high temperatures into 3D silicon islands that show a unique pattern [1,2]. We have used AFM, SEM, and low-energy electron microscopy (LEEM) observations of the decomposition of ultrathin SOI in real time to investigate the mechanisms of self-organized decomposition. The decomposition starts from defect sites, such as pinholes and sites where threading dislocations exit the film, and then expands outward first along the elastically soft directions, which should be the easiest directions to relax the stress associated with the defect sites. At later stages, Si islands form along <013> directions into a pattern with good long-range order. The 3D island diameter is on the order of one hundred nanometers, depending on the initial Si template layer thickness and the rate of decomposition. Real-time LEEM observation has revealed the detailed mechanisms and processes for such island formation and ordering. Si atoms first diffuse away or evaporate to form individual trenches with stable {131} side facets. Consequently, the trenches extend along <013> directions. As two adjacent trenches expand in width, a narrow ridge with {131} facets forms along the <013> direction. The ridge eventually breaks into isolated silicon islands due to the Rayleigh instability [3], leading to the final island patterns. [1] B. Legrand, V. Agache, J. P. Nys, V. Senez, and D. Stievenard, Appl. Phys. Lett. 76, 3271 (2000); [2] R. Nuryadi, Y. Ishikawa, and M. Tabe, Appl. Surf. Sci. 159, 121 (2000); [3] Lord Rayleigh, Lond. Math Soc. Proc., Ser 1, 10, 4 (1879). Supported by ONR, NSF, and DOE.

10:30 AM E4.7

Structural Comparisons of SiOx and Si/SiOx Formed by Passivation of Single-Crystal Silicon by Atomic and Molecular Oxygen. Maja Kisa[1], Judith C Yang[1] and Ray D Twesten[2]; [1]Materials Science and Engineering Department, University Of Pittsburgh, Pittsburgh, Pennsylvania; [2]Frederick Seitz Materials Research Laboratory, Center for Microanalysis of Materials, Urbana, Illinois.

The structural characteristics of a silica layer and Si/SiO_2 interface formed on Si single-crystal by oxidation in hyperthermal atomic oxygen (AO) and molecular oxygen (MO) at 493K were compared by High Resolution Transmission Electron Microscopy (HRTEM), Electron Energy Loss Spectroscopy (EELS), Atomic Force Microscopy (AFM), Rutherford Backscattering Spectrometry (RBS), Scanning Electron Microscopy (SEM) and X-ray Photoelectron Spectroscopy (XPS). The hyperthermal AO with kinetic energy of 5.1eV was created by the pulsed laser detonation of oxygen gas. We previously determined by RBS and HRTEM that AO forms an amorphous oxide on Si(100) and this oxide is nearly twice the thickness and approximately two times rougher surface as that formed by MO. Here we report that the silica layer formed on Si(111) by AO is also nearly twice the thickness and about seven times rougher surface when compared to the oxide created by MO. The oxide formed by AO and MO on both silicon orientations is amorphous as observed by HRTEM and selected area electron diffraction (SAED). However, the oxide formed by AO has a less random distribution of silicon and oxygen atoms as compared to the oxide formed by MO, as evidenced by the SAED pattern and EELS spectra. In contrast to MO formed silica, initial EELS results across the Si/SiO_2 interface revealed no region of sub-oxides exists near the interface in the AO formed silica. SEM and AFM experiments were performed at the MSE Department, University of Pittsburgh. HRTEM, EELS, XPS and RBS experiments were carried out in the Center for Microanalysis of Materials, University of Illinois, which is partially supported by the U.S. Department of Energy under grant DEFG02-91-ER45439.

10:45 AM E4.8

Electronic and Optical Carrier Injection in Layered High-k Heterostructures. Julie D. Casperson[1], L. Douglas Bell[2], Damon B. Farmer[3], Brett W. Busch[4], Mun Yee Ho[4], Martin L. Green[4], Roy G. Gordon[3] and Harry A. Atwater[1]; [1]Applied Physics, California Institute of Technology, Pasadena, California; [2]Jet Propulsion Laboratory, Pasadena, California; [3]Chemistry, Harvard University, Cambridge, Massachusetts; [4]Agere Systems, Murray Hill, New Jersey.

We have modeled and fabricated silicon-compatible layered high-dielectric constant structures that enable carrier injection from a silicon channel to a floating gate or contact electrode that can be modulated by an applied bias. We utilize an effective mass-based tunneling model to predict the current-voltage characteristics and carrier distributions in layered tunnel barrier structures under applied bias. Experimental characterization of tunneling and band offsets has been performed using current-voltage and capacitance-voltage measurements and internal photoemission spectroscopy measurements to obtain band offsets. We find from our simulations that some of the most promising structures for layered tunnel barriers consist of Al_2O_3 with Si_3N_4 or HfO_2 and we have fabricated such structures. The Si_3N_4 was made by low-pressure chemical vapor deposition, while the Al_2O_3 and HfO_2 were made by atomic layer deposition. We have fabricated and characterized the layered barrier structures Si_3N_4 / Al_2O_3 / Si_3N_4 and HfO_2 / Al_2O_3 / HfO_2 as well as single- and double-layered structures using these materials. These heterostructures are designed to enable carrier injection into floating gate structures with dramatically increased programming speeds in nonvolatile memory devices, such as flash memories and nanocrystal memories. Such silicon-compatible layered barrier heterostructures that enable a large drop in the barrier height with applied voltage are promising candidates to replace single dielectric films as the tunnel barriers for nonvolatile memories. Such voltage-dependent barrier lowering may also form the operating principle for a new class of photodetectors with electrically-tunable cutoff wavelengths. Internal photoemission spectroscopy measurements have been performed on metal-insulator-semiconductor structures with semi-transparent gates in order to directly measure the band offsets of layered tunneling barrier structures, using a chopped tunable arc-lamp source for illumination. Our measurements indicate band-offsets for SiO_2 and Al_2O_3 to be 3.5 eV and 3.1 eV, respectively. Our measurements for other single dielectrics and heterostructures will be presented.

11:00 AM E4.9

Nitrided Hafnium Silicate Film Formation by Sequential Process Using a Hot Wall Batch System and Its Application to MOS Transistor. Tomonori Aoyama, Kazuyoshi Torii, Riichirou Mitsuhashi, Takeshi Maeda, Satoshi Kamiyama, Atsushi Horiuchi, Hiroshi Kitajima and Tsunetoshi Arikado; Research Dept. 1, Semiconductor Leading Edge Technologies, Inc., Tsukuba, Japan.

We have developed the novel high-k gate dielectrics formation process. Si pre-oxidation (t_{ox}=0.5nm), $HfSiO_x$ MOCVD and post deposition annealing are sequentially performed using a hot wall batch-type LP-CVD system in order to suppress contamination between processes. $HfSiO_x$ MOCVD was carried out at 280°C employing a hafnium tetra-t-butoxide and disilane mixture. The post deposition annealing consists of oxidation and nitridation using O_3 and NH_3, respectively. O_3 oxidizes carbon remained in the $HfSiO_x$ film and NH_3 treatment incorporates nitrogen into the film to improve the thermal stability. Analyses using RBS and SIMS reveal that this film is $Hf_{0.6}Si_{0.4}O_xN_y$. Distribution of equivalent oxide thickness (EOT) and composition are uniform enough not only within a 300mm wafer but also within a batch. In addition to contamination suppression,

this sequential process has an ability to achieve high throughput from pre-oxidation to NH_3 treatment. These dielectrics (3nm HfSiON/0.5nm SiO_2) were applied to MOSFET. NMOS and PMOS were fabricated using the CMOS process except for the gate dielectrics. In order to accomplish higher reliability, the gate dielectrics should keep amorphous after activation of dopants (P and B) implanted into the Si substrate and the poly-Si gate. NH3 nitridation at 700°C for 10min improves thermal stability of $HfSiO_x$ so that the film keeps amorphous condition even after 1050°C / 1sec annealing. EOT of 1.47nm and low leakage current of 1.3mA/cm^2 at 1.1V could be accomplished. These values are lower than the expected target values for 65nm-node LSTP CMOS technology. In addition, high electron and hole mobility were obtained.

11:15 AM E4.10
Band Offsets at Ba- SrTiO3 / Si Interfaces.
Alan Shu-Chung Wan, Fabrice Amy and Antoine Kahn; Electrical Engineering, Princeton University, Princeton, New Jersey.

The continuous drive toward faster electronics and scaling down of MOSFET device dimensions requires alternatives to SiO2 for gate dielectrics. High-k dielectrics have therefore received considerable attention from industry and the scientific community. Crystalline perovstike oxides such as SrTiO3 and BaTiO3 are of special interest and offer several advantages. First, they can be MBE-grown lattice-matched to Si (or Ge) substrates with very low interface state density.1 Second, they can serve as a buffer layer for the growth of semiconductors, opening possibilities for integrating Si electronics and III-V optoelectronics. However, several issues concerning these materials remain to be fully addressed, among which band offsets with Si and other semiconductors. In this work, we use a SrTiO3(100 Å)/BaSrO(11 Å)/Si structure grown by MBE, and X-ray and UV photoemission spectroscopy to study core levels and valence band respectively. Depending on surface preparation, including ex-situ UV ozone, O2 or UHV annealing, the valence band maximum position shifts by more than 2 eV, whereas very little if any shift is observed on core levels. These findings indicate that surface composition and morphology are of paramount importance in the UPS determination of electronic structure, and may explain discrepancies between results reported in the literature. Our investigation of clean and stoichiometric SrTiO3 surface indicates that its conduction band minimum is located 0.4 eV (± 0.4) below the one of silicon. An in-depth investigation of the role of surface preparation is being pursued, and results on BaTiO3/SrTiO3/Si samples will be reported. 1 . R. A. McKee, F. J. Walker, and M. F. Chisholm, Phys. Rev. Lett. 293, 468 (2001)

11:30 AM E4.11
Abstract Withdrawn

11:45 AM E4.12
***Insitu* Investigation of Me_xO_y/Si (Me=Hf, Al, Yb) Interfaces with PLD-XPS.**
Andrei Zenkevich and Yuri Lebedinskii; Moscow Engineering Physics Institute, Moscow, Russian Federation.

SiO_2 as the gate dielectric material in Si-based CMOS technology is to be replaced eventually with a higher dielectric constant (high-k) material. Metal oxides considered as candidates would have ~5nm in thickness in real products. At such thickness of overlayer x-ray photoelectron spectroscopy is a technique allowing to monitor simultaneously chemical bonding in the growing oxide film and at metal oxide/silicon interface. Reactive pulsed laser deposition (PLD) by ablating metal in reduced oxygen atmosphere (10^{-2}-10^{-6} Torr) allows to vary metal/oxygen concentration ratio in the film, deposition rate and substrate T as independent parameters and to control the growing layer thickness with submonolayer accuracy. To investigate the initial stages of high-k dielectric/Si interface formation and its evloution during annealing both in vacuum and in oxygen, reactive PLD combined with *insitu* XPS analysis is advantageous. We present comparative XPS data on the chemical bonding at Me_xO_y/Si interface (Me=Hf, Al, Yb) during RT growth and upon further annealing in vacuum as well as in oxygen. Layer-by-layer growth during reactive PLD is established with XPS and confirmed with *exsitu* AFM. During HfO_2, Al_2O_3 and Yb_2O_3 growth at RT, Si-O bonding within one monolayer only is observed at the interface. The thickness of SiO_2 interlayer as a function of annealing T is presented. The conversion of interfacial SiO_2 into metal silicate is found to depend on the particular Me_xO_y/Si system and oxygen concentration in metal oxide layer.

SESSION E5: Theory of Novel Oxide/Semiconductor Interfaces
Chairs: Peter Bloechl and David Vanderbilt
Tuesday Afternoon, December 2, 2003
Room 207 (Hynes)

1:30 PM E5.1
Dielectric Permittivity of Atomic-layer Thick SiO_2 Films or Interlayers on Silicon Substrates.
Feliciano Giustino[1,2], Paolo Umari[1,2] and Alfredo Pasquarello[1,2]; [1]ITP (Institut des Theories des Phenomenes Physiques), EPFL (Ecole Polytechnique Federale de Lausanne), Lausanne, Switzerland; [2]IRRMA (Institut Romand pour la Recherche Numerique sur les Materiaux), Lausanne, Switzerland.

To address the dielectric effect of a thin silica interlayer between silicon and high-κ oxides, we investigated the dielectric permittivities of atomic-layer thick SiO_2 films on silicon using a density functional approach. We constructed several model structures of the Si/SiO_2 interface with oxide thickness varying between 3 and 12 Á, and for each of them we calculated both the static and high-frequency permittivities. We found that a classical three-layer model (including the silicon substrate, a 3 Á thick suboxide, and the pure SiO_2 oxide) reproduces to a high degree of accuracy the results obtained from first principles. This suggests that the evolution of the screening properties from Si to SiO_2 is rather abrupt, and essentially takes place within the suboxide region. To check the validity of this conclusion, we investigated the microscopic polarization induced at the interface by an external electric field. We found that the local polarization is approximately constant in the substrate and in the pure oxide, and that the transition essentially occurs within the suboxide. This result provides a truly microscopic justification for the classical three-layer model. Static and high-frequency permittivities of the suboxide layer were found to be significantly larger than the corresponding values of bulk SiO_2 (3.8 and 6.8 instead of 2.0 and 3.8, respectively). To interpret this enhanced screening, we analyzed the interface from a chemical point of view. Following the Berry-phase theory of polarization, we determined the maximally localized Wannier functions of the system, and assigned each of them to a specific chemical bond (Si-Si or Si-O). Then, we evaluated the effective polarizability for each Wannier function, and found that the screening provided by Si-Si and Si-O bonds is almost independent of their location with respect to the interface. As a consequence, the enhanced screening of the suboxide layer must arise from the chemical grading. Similar conclusions hold for the ionic screening. Metal-induced gap states are shown to contribute to the polarization of the suboxide, but their role in enhancing the SiO_2 permittivity in proximity of the substrate appears less prominent than previously suggested. The enhanced screening of the suboxide implies that the effect of a thin silica interlayer between silicon and a high-κ dielectric is less severe than expected on the basis of the bulk SiO_2 permittivity.

1:45 PM E5.2
Ab-initio study on the γ-Al_2O_3 surfaces and interfaces.
Henry Paul Pinto and Simon David Elliott; Physics, NMRC, University College, Cork, Cork, Ireland.

The controlled growth of alumina films by atomic layer deposition (ALD) is of great interest to the electronics industry, as high-k dielectrics are being sought for the next-generation MOSFETS [1]. Many aspects of the surface structure and reactivity of alumina are still unknown, but are amenable to computation. We present a theoretical study of the alumina polymorph γ-Al_2O_3. The calculations are based on density functional theory (DFT). The predicted bulk structure for γ-Al_2O_3 has the Al-vacancy sites widely separated, which is in agreement with other theoretical predictions [2]. We estimated the energy of several γ-Al_2O_3 surfaces namely: (111), (110) and (150). The atomic and electronic structure of the most stable (111) surface is discussed and compared with the α-Al_2O_3(0001). The presence of H_2O within the (111) surface is studied and contrasted with the results when the water is inside the bulk. Besides, the interaction of a H_2O onto the (111) surface is considered. Finally, a model for γ-Al_2O_3(111)/AlOOH-like interface is proposed and the atomic structure and the ideal work of adhesion are computed. In addition, we study the hydrogen diffusion and the water influence within the interface and these results are discussed in light of available experimental data. References. [1] G.D. Wilk, R. M. Wallace, J. M. Anthony, J. Appl. Phys. 89, 5243 (2001). [2] C. Wolverton, K. C. Hass, Phys. Rev. B 63, 024102 (2001)

2:00 PM *E5.3
Lattice Dielectric Properties of ZrO_2 and HfO_2.
David Vanderbilt[1] and Xinyuan Zhao[2]; [1]Physics and Astronomy, Rutgers University, Piscataway, New Jersey; [2]School of Physics, Georgia Institute of Technology, Atlanta, Georgia.

We have investigated the structural, electronic, and lattice dielectric properties of crystalline ZrO_2 and HfO_2. The calculations have been carried out within the local-density approximation using ultrasoft pseudopotentials and a plane-wave basis. Our calculations on cubic, tetragonal, monoclinic, and orthorhombic phases indicate a strong dependence of the lattice dielectric susceptibility and its anisotropy on the choice of crystal phase. For example, we find a large in-plane susceptibility for the tetragonal phase. Significant differences in the

electronic density of states and band gaps are also revealed. The calculated zone-center phonon frequencies yield good agreement with infrared and Raman measurements. Born effective charge tensors are also reported. Preliminary results on a model of amorphous ZrO_2 generated via melt-and-quench first-principles molecular dynamics reveal a distribution of coordination numbers for both Zr and O atoms. Implications for potential high-K applications of these materials will be discussed.

2:30 PM E5.4
Theoretical Analysis Of Oxygen Diffusion In Monoclinic HfO_2. Minoru Ikeda[1], Georg Kresse[2], Toshihide Nabatame[1] and Akira Toriumi[3,4]; [1]MIRAI, Association of Super-Advanced Electronics Technologies(ASET), Tsukuba, Ibaraki, Japan; [2]Institut fuer Materialphysik, Universitaet Wien, Sensengasse, Wien, Austria; [3]MIRAI, Advanced Semiconductor Research Center(ASRC), National Institute of Advanced Industrial Science and Technologies(AIST), Tsukuba, Ibaraki, Japan; [4]Department of Materials Science School of Engineering, University of Tokyo, Hongo, Bunkyo-ku, Tokyo, Japan.

Recently, HfO_2 (hafnia) grown on Si substrates is widely studied as a potential candidate for replacing silicon dioxide as the gate dielectrics in scaled CMOS. At the interface between Si and hafnia, the interfacial layer has been formed. And this layer thickness increases by the post deposition annealing [1]. This indicates that oxygen diffuses through hafnia. Foster et al. reported the interstitial oxygen diffusion in hafnia and concluded that the O^{2-} diffuses in the bulk HfO_2 [2]. In this report, we present the detailed analysis of the interstitial oxygen (O^{2+}, O^0, O^{2-}) diffusion in hafnia using the Projector Augmented Plane Wave method [3-5] with the Nudged Elastic Band theory [6]. The interstitial oxygen atom kicks out the oxygen atom at the 3-fold-site and occupies the 3-fold-site. And then the newly kicked-out interstitial oxygen atom jumps to the nearest neighbor site and couples again with the atoms at the crystal sites. This kick-out-mechanism is valid for all charge states of the interstitial oxygen in monoclinc HfO2. The interstitial O^{2+} forms a trimer with the two neighbor 3-fold-sites O atoms. And the neutral interstitial O^0 atom forms the dimer coupled with the one nearest neighbor 3-fold-site O atom. Contrary to these two cases, the O^{2-} forms new 3-fold site among Hf atoms. In hafnia, the interstitial oxygen atom can take 3 charge states depending on Ef. However, the O^{2-} does not contribute to the diffusion process in hafnia because of the pair annihilation process between O^{2-} and oxygen vacancy (V^{2+}) defect pair. We can simulate such a pair annihilation process in hafnia. In the higher range of E_f, O^0 might contribute. And for the lower range of E_f, we think that the actual experimental situation satisfies this condition, the O^{2+} only contributes to the diffusion process in hafnia. This work was supported by NEDO. References [1] T.Nabatame, T.Yasuda, M.Nishizawa, M.Ikeda, T.Horikawa and A.Toriumi, Extended Abstracts of SSDM 2002, p.64. [2] A.S.Foster, A.L.Shluger, and R.M.Nieminen, Phys.Rev.Lett. 89, 225901(2002) and A.S.Foster,F.L.Lopez Gejo, A.L.Shluger, and R.M.Nieminen, Phys.Rev.B65,174117(2002). [3] G.Kresse and J. Hafner,Phys.Rev.B47,558(1993) and G.Kresse, TUW,Thesis(1993). [4] P.E. Blochl, Phys. Rev. B 50, 17953 (1994). [5] G.Kresse and D.Joubert, Phys.Rev.B59,1758(1998). [6] G.Henkelman and H. Jonsson, J.C.P.,Vol 113,9978(2000).

2:45 PM E5.5
Bonding and Epitaxial Relationships at High-K Oxide:Si Interfaces. John Robertson and Paul W Peacock; Engineering, Cambridge University, Cambridge, United Kingdom.

High dielectric constant oxides are needed to replace silicon dioxide as the gate oxide in future CMOS devices. Also, functional oxides with ferroelectric, ferromagnetic, CMR, or superconducting properties are desired for future devices [1]. However, the interfaces between oxides and silicon are not easily described because of the change from ionic bonding in the oxide to covalent bonding in Si. We have studied the interfacial bonding at epitaxial interfaces of Si:ZrO2 and Si:SrTiO3 with Si for a wide variety of orientation and terminations see in experiment [1-4], using total energy calculations. The results can be explained within simple rules. The key requirement is for the interface to be insulating and have no interface gap states. We show that the oxide face must actually be polar, to satisfy the Si dangling bonds. Both oxygen-last or metal-last are possible. The oxygen-last interfaces tend to be insulating, if our stoichiometry rules are followed, whereas the metal-last interfaces often have interface gap states. Oxygen-last interfaces are constructed by saturating all the surface Si dangling bonds by oxygens, and then adding non-polar constructed surfaces for (100), (110) or (111) oxide. This gives a net oxygen-rich interface. For ZrO2, the bonding rules explain the epitaxial rules found by Yoshimoto [3] for fluorite on Si systems such as Si:ZrO2(100), Si(100):ZrO2(110) and the similar cases of (111) epitaxy in the bixbyite (Y,La)2O3 series. The band offsets are calculated for each case. For ZrO2, the band offset is found to be relatively independent of orientation and also to be close to the value determined from bulk charge neutrality levels [5]. 1. R A McKee, F J Walker, M F Chisholm, Science 293 468 (2001) 2. V Narayanan et al, J App Phys 93 251 (2003) 3. M Yoshimoto et al, Jap J App Phys 29 L1199 (1990) 4. X Hu, et al, App Phys Lett 82 203 (2003) 5. J Robertson, J Vac Sci Technol B 18 1785 (2000)

3:30 PM E5.6
High dielectric constant materials: a band line-up problem. Alex Demkov[1,3], Leonardo Fonseca[2], Otto F. Sankey[3] and John Tomfohr[3]; [1]Motorola, Inc., Austin, Texas; [2]Motorola, Inc., Tempe, Arizona; [3]Arizona State University, Tempe, Arizona.

To insure continuous downscaling of CMOS technology the semiconductor industry must make a transition from the Si-SiO2-poly-Si triad to a much more complex Si-dielectric-metal system. The higher than silicon dioxide dielectric constant of the new gate dielectric will allow maintaining the gate capacitance and therefore the drain-source saturation current without the thickness reduction of the oxide. The integration of this new stack into the current CMOS flow is one of the most urgent tasks of today's electronics. The oxide's gate action, among other factors, depends on the barrier height (same as band discontinuity) at the oxide-semiconductor and oxide-metal interfaces. The band alignment is often estimated within the so-called metal-induced gap states (MIGS) model. The MIGS model describes both Bardeen and Schottky limits and interpolates between the two in a linear fashion, provided that electron affinities, charge neutralities and the pinning factor are known. The theory was also successfully used to describe the band discontinuity in heterojunctions between covalent semiconductors. It is not obvious whether this approach should work for junctions between Si and high-k dielectrics. A consistent procedure to determine the charge neutrality level is also not clear. We use the complex band structure of several prospective gate dielectrics (SiO2, SrTiO3, HfO2, and Al2O3) to estimate their charge neutrality levels, and compute band offsets to Si and Pt. Results of these model calculations are then compared to those obtained with direct electronic structure methods and available experiment. It appears that charge neutrality levels thus obtained indeed provide a consistent picture. However, the uncertainty in the conduction band position inherent in the local density approximation may render the theory inadequate for the engineering support. Despite this limitation, linear scaling the charge neutrality levels based on the experimental band gaps has shown excellent agreement with experimental data.

3:45 PM E5.7
A View of Sr Adsorption on Si(001) from First Principles Calculations. Christopher R Ashman[1], Clemens J Foerst[2,1], Karlheinz Schwarz[2] and Peter E Bloechl[1]; [1]Institute for Theoretical Physics, Clausthal University of Technology, Clausthal-Zellerfeld, Germany; [2]Institute for Materials Chemistry, Vienna University of Technology, Vienna, Austria.

The initial stages of metal deposition on silicon are critical to understanding the growth of high-K oxides on silicon with abrupt interfaces. We performed state-of-the-art electronic structure calculations and ab-initio molecular dynamics simulations of the adsorption structures of Sr on Si(001). The atomic and the electronic structures and the energetics depending on the Sr-coverage will be discussed and compared with existing experimental information. The adsorption can be explained by a series of structural motifs which derive from the chemical binding.

4:00 PM *E5.8
Ab-initio Simulations on Initial Growth Steps of High-K Oxides on Silicon: $SrTiO_3$/Si(001). Peter E. Bloechl[1], Christopher R. Ashman[1], Clemens J. Foerst[1,2] and Karlheinz Schwarz[2]; [1]Institute for Theoretical Physics, Clausthal University of Technology, Clausthal-Zellerfeld, Germany; [2]Institute for Materials Chemistry, Vienna University of Technology, Vienna, Austria.

State-of-the-art electronic structure calculations and ab-initio molecular dynamics simulations have been performed to investigate the growth of $SrTiO_3$ on Si(001). I will briefly touch on the adsorption of Sr on Si(001). Then, I will explain the formation of the first SrO layers on silicon and describe the atomic and electronic structure of the $SrTiO_3$./Si(001) interface. The structural changes upon variation of the oxidation partial pressure have been investigated. Based on these results, a method to engineer the band offsets in order to obtain an acceptable injection barrier will be proposed.

4:30 PM E5.9
Structure and dielectric properties of the high-k oxides CeO2 and LaAlO3. Gianluca Gulleri[1,2] and Vincenzo Fiorentini[1]; [1]Dept. of Physics, University of Cagliari, Monserrato, Italy; [2]MDM-INFM Lab, Agrate, Italy.

We study the structural stability, effective charges, and ionic dielectric

constants of the high-k oxides CeO2 and LaAlO3 from ab initio density-functional and Berry phase polarization calculations. Ceria is a stable fluorite, not exhibiting the phonon instabilities of zirconia and hafnia; the stable structure of LaAlO3 is a rombohedral variant of a perovskite. Anomalous charges (~5) and large ionic dielectric constants (~20-25) are found in both cases. As for our previous calculations on zirconia and hafnia, models of interfaces with Si are currently being set up and evaluated in terms of energetics and band offsets.

4:45 PM E5.10
First-Principles Study of the $LaAlO_3$(001)/Si(001) Interface.
A. Knizhnik[2], I. Iskandarova[2], A. Bagatur'yants[2], B. Potapkin[2], L. R. C. Fonseca[1] and A. Korkin[1]; [1]Motorola Inc, Tempe, Arizona; [2]Kintech Technologies Ltd., Moscow, Russian Federation.

$LaAlO_3$ has been considered as a possible high-k dielectric candidate for the next generation of MOSFET devices but very little is known about its electronic attributes. We performed first-principles calculations of its bulk and surface properties, and studied the $LaAlO_3$(001)/Si(001) interface structure. We calculated a dielectric constant of ~30 for crystalline $LaAlO_3$, which is similar to hexagonal La_2O_3, and is in good agreement with experimental data. In the case of $LaAlO_3$(001) slabs, a net nonzero dipole moment arises as a result of non-identical surfaces. This problem was addressed and several ways of eliminating the net dipole moment are presented. We show that the migration of an oxygen anion is a favorable technique for compensating the $LaAlO_3$(001) surface dipole. The model structures of $LaAlO_3$(001) surfaces with compensated dipole moments were used to study $LaAlO_3$(001)/Si(001) interface properties. We investigated the stability of these interfaces and found that lanthanum-terminated $LaAlO_3$(001) cases are in general more stable than aluminum-terminated cases for both the oxidized and unoxidized Si(001) surfaces. Using density-of-states techniques we found that the O-rich interfaces result in a significant reduction of the $LaAlO_3$(001)/Si(001) valence band offset due to the creation of interface dipoles. The analysis of the interface states density showed that direct La-Si bonds forming at the $LaAlO_3$(001)/Si(001) interface do not create interface states in the silicon band gap, in contrast with Zr(Hf)-Si bonds studied previously in m-Zr(Hf)O_2/Si(001) model systems.

SESSION E6: Poster Session: Fundamentals of Novel Oxide/Semiconductor Interfaces II
Chairs: Darrell Schlom and Susanne Stemmer
Tuesday Evening, December 2, 2003
8:00 PM
Exhibition Hall D (Hynes)

E6.1
p-type in ZnO:N by codoping with Cr.
Eliana Kaminska[1], Anna Piotrowska[1], Jacek Kossut[2], Renata Butkute[2], Witold Dobrowolski[2], Ewa Ilczuk[2], Krystyna Golaszewska[1], Adam Barcz[1,2], Elzbieta Dynowska[2], Rafal Jakiela[2] and Dorota Wawer[1]; [1]Institute of Electron Technology, Warsaw, Poland; [2]Institute of Physics, PAS, Warsaw, Poland.

There is a growing interest in the use of transparent-oxide electronics with the potential advantages of invisible electronic circuits, high-temperature performance and radiation hardness. The majority of transparent conducting oxides (TCOs), however, are n-type semiconductors. Despite the considerable amount of work on the growth of p-type TCOs, relatively few results have been reported. As for ZnO, it is commonly accepted that fabrication of p-type material is a formidable technological challenge if possible at all [1]. With this fact in mind we have attempted to fabricate ZnO with p-type conductivity by oxidation of nitrogen-doped zinc metallic films and zinc nitride films. The starting materials were grown either by magnetron sputtering or by molecular beam deposition. Quartz, sapphire and thin GaN films on sapphire were used as substrates. We present results of secondary ion mass spectrometry and x-ray diffraction analyses of the oxidized layers, which indicate that formation of ZnO does take place. The layers of ZnO obtained by oxidation of metallic Zn so far were always found to be either highly resistive or showed n-type conduction. In contrast to that, oxidized layers obtained from zinc nitride were found to be p-type (the carrier concentration $\sim 5\times10^{14}cm^{-3}$ and mobility $\sim 50 cm^2/Vs$). The best results (with the hole concentration reaching $5\times10^{17}cm^{-3}$ and mobility being 5 cm^2/Vs at room temperature) were obtained when the starting material before oxidation was additionally doped with Cr. The transmittance of 320 nm thick ZnO:N:Cr films in the whole visible wavelength spectrum reached 60%. The energy gap, as inferred from transmission measurements, was 3.27eV. Work supported by grant from the European Commission NANOPHOS (contract IST-2001-39112) within the 5th Framework Programme and by grant from the State Committee for Scientific Research PBZ-KBN-044/P03/2001. [1] S.B. Zhang, S.-H. Wei, and A. Zunger, Phys. Rev. B 63, 075205 (2001)

E6.2
Microstructure and Electrical Properties of Zinc Oxide Thin Film Varistors Prepared by RF Sputtering.
Keng-ming Chang[1], Chuan-pu Liu[1] and Chon-ming Tsai[2]; [1]Department of Materials Science and Engineering, National Cheng Kung University, Tainan, Taiwan; [2]Besdon Technology Corporation, Taipei, Taiwan.

The thin film varistors of ZnO-Bi2O3 multilayer junctions were fabricated by RF sputtering. The nonlinear I-V characteristics and nonlinear coefficient, α, under the reverse bias were examined and they were effected by composition and structure of the multilayer varistors. The threshold voltage can be adjusted by altering the donor density in ZnO, which was achieved by varying doping concentration Al and sputtering conditions. In addition the structure and thickness of the Bi2O3 layer in thin film varistors determine the threshold voltage. The higher leakage current and lower nonlinear coefficient associated with the ZnO films doped with Al (ZnO:Al) can be improved by inserting another ZnO layer doped with selective transition metal impurities between ZnO:Al and Bi2O3 layers. The microstructure and defects of the multilayer were investigated in detail and related to the performance of the electrical properties. The interface states in the ZnO films were attemped by electron energy-loss spectrometry (EELS) in a transmission electron microscopy. The EELS data along with the doping concentration by Hall measurement were also used to explain the electrical properties.

E6.3
Properties of ZnO and aluminum doped ZnO thin films grown by pulsed electron deposition.
Ram Janay Choudhary[1], S. S. Hullavarad[1], R. D. Vispute[1], S. B. Ogale[1], S. R. Shinde[1], V. N. Kulkarni[1], T. Venkatesan[1], K. S. Harshvardhan[2] and Mikhail Strikovski[2]; [1]Center for Superconductivity Research, University of Maryland, College Park, Maryland; [2]Neocera Inc., Beltsville, Maryland.

The technique of pulsed electron deposition (PED), which is based on channel spark discharge and magnetically self-pinched pulsed electron beam, is applied to grow thin films of ZnO with and without Al doping on c-Al_2O_3 and Si (001). The films are deposited at a discharge voltage of 15 kV, repetition rate of ~5 Hz, and a background pressure of 6 mTorr of forming gas (95% Ar + 5% H_2). The film properties are investigated by various techniques such as Rutherford back scattering, ion channeling, x-ray diffraction, UV Spectroscopy, atomic force microscope, and four probe resistivity measurement. These films are c-axis oriented, electrically conducting, and optically transparent with transmittance close to 75% in the visible and IR region of the spectrum. The band gap is 3.4 eV. The overall quality of these films will be compared with that of the pulse laser deposited films. The structural, transport and optical properties of these films will be discussed in details. Work Supported by Maryland Industrial Partnership (MIPS) program.

E6.4
Electronic Structure of Zn(Mn)O - A Resonant Photoemission Study.
Elzbieta Guziewicz[1,2], Krzysztof Kopalko[2], Janusz Sadowski[3,4,2], Marek Guziewicz[5] and Zbigniew Golacki[2]; [1]MST-10, Los Alamos National Laboratory, Los Alamos, New Mexico; [2]Institute of Physics, Polish Academy of Sciences, Warszawa, Poland; [3]Niels Bohr Institute fAFG, Orsted Laboratory, University of Copenhagen, Copenhagen, Denmark; [4]MAX-lab, Lund University, Lund, Sweden; [5]Institute of Electron Technology, Warszawa, Poland.

Ferromagnetic properties of ZnO with 3d transition-metal impurities have been widely investigated in the past 3 years. Especially, incorporation of Mn into semiconducting ZnO attracts considerable attention because an antiferromagnetic ordering in n-Zn(Mn)O and a ferromagnetic ordering in p-Zn(Mn)O at room temperature has been predicted. In addition, a high solubility of Mn in ZnO has been confirmed. These features make Zn(Mn)O a good material for transparent magnets and for new applications in spintronics. We have investigated an electronic structure of Zn(Mn)O surface alloy by synchrotron radiation photoemission. Four of manganese monolayers were deposited on Zn(0001) single crystal and next Mn/ZnO system was annealed up to 5000C. The scanning Auger measurements taken after annealing show no metallic film and confirm that the Zn(Mn)O surface alloy of 20 Angstroms thickness has been created. Resonant photoemission spectra near the Mn3p-Mn3d absorption edge taken before and after annealing show resonant enhancement of Mn3d states within 10 eV of the Fermi edge. An experimentally obtained Mn3d partial density of states change considerably as a result of annealing. The relative intensity of satellite/main ratio decrease after annealing from 0.89 to 0.43 giving evidence of higher degree of hybridization between the Mn3d states and the ZnO valence band. The comparison

with previous resonant photemission results show that the hybridization effect in ZnMnO surface alloy is similar to that in ZnMnS ternary compound and much higher than in ZnMnSe and ZnMnTe. We have also measured photoemission from the Mn3p core level. Photoemission spectra show two Mn3d components separated by about 4 eV. The relative intensity of these two components is different before and after annealing. This suggests that two manganese states are observed in the Zn(Mn)O interface region.

E6.5
Fabrication of $SrRuO_3$ Epitaxial Thin Films on $YBa_2Cu_3O_x$ / CeO_2 / YSZ-buffered Si Substrates by Pulsed Laser Deposition. Takamitsu Higuchi, Koichi Morozumi, Setsuya Iwashita, Masaya Ishida and Tatsuya Shimoda; Technology Platform Research Center, SEIKO EPSON CORPORATION, Fujimi-machi, Nagano-ken, Japan.

Much attention has been paid to $SrRuO_3$ epitaxial thin film electrodes, because heteroepitaxial growth of perovskite-type ferroelectric or piezoelectric oxides on the $SrRuO_3$ epitaxial thin film electrodes would bring about an increase in remnant polarization or piezoelectric constant. However, it is quite difficult to fabricate $SrRuO_3$ epitaxial thin films directly on Si substrates due to the formation of a SiO_2 layer on the Si substrates. Therefore, metal oxide-buffered Si should be used as substrates. In general, however, the epitaxial growth of such metal oxides on Si has been realized at a low oxygen partial pressure (P_{O2}) and a high substrate temperature (T_s), where the SiO_2 layer on Si is easily removed. In the present study, epitaxial growth of a yttria-stabilized-zirconia (YSZ) buffer layer on a Si (100) substrate was demonstrated at a relatively high P_{O2} and a low T_s by pulsed laser deposition (PLD), and pseudocubic $SrRuO_3$ (100) epitaxial thin films was fabricated on a $YBa_2Cu_3O_x$ / CeO_2 / YSZ-buffered Si substrate by PLD. Reflection high energy electron diffraction (RHEED) revealed that the YSZ buffer layer with the thickness of 5 nm was epitaxially grown on a naturally oxidized Si substrate with the process conditions of a relatively high P_{O2} (= 5×10^{-5} Torr) and a relatively low T_s (= 700 °C) compared to previously reported data, and that an orientation relationship of YSZ (100) / Si (100) and YSZ <011> // Si <011> was established. Accounting for the Gibbs free energy change, the vapor pressure of SiO, and the growth rate for the thermally oxidized SiO_2 on the Si substrate surface, it is suggested that the epitaxial growth of YSZ on the naturally oxidized Si is caused by deoxidization of SiO_2 on Si by Zr with a rate larger than the growth rate of SiO_2, and by evaporation of Si as a SiO. The second deposition of the CeO_2 buffer layer with the thickness of 10 nm resulted in an orientation relationship of CeO_2 (100) / Si (100) and CeO_2 <011> // Si <011>. The third deposition of the $YBa_2Cu_3O_x$ buffer layer with the thickness of several nm played an important role to bring about a (100) orientation of a perovskite-type cubic unit cell. The last deposition of $SrRuO_3$ resulted in a pseudocubic (100) epitaxial thin film, exhibiting an orientation relationship of $SrRuO_3$ (100) / Si (100) and $SrRuO_3$ <010> // Si <011>, and good crystallinity with a full width at half maximum (FWHM) of 1.7 ° in the $SrRuO_3$ (200) rocking curve by X-ray diffraction (XRD).

E6.6
Surface Phase Transitions of Layered Perovskite $Ca_{2-x}Sr_xRuO_4$. Rob G. Moore[1], S. V. Kalinin[2], Ismail Ismail[1,2], Jiandi Zhang[3], A. P. Baddorf[2], R. Jin[2], D. G. Mandrus[1,2] and E. W. Plummer[1,2]; [1]Physics and Astronomy, University of Tennessee, Knoxville, Tennessee; [2]Oak Ridge National Laboratory, Oak Ridge, Tennessee; [3]Physics, Florida International University, Miami, Florida.

Strong coupling between electronic, lattice, orbital and spin degrees of freedom in transition metal oxides has attracted significant interest in exploiting their immense potential for oxide electronic devices with novel functionalities. Understanding the fundamental physics of reduced dimensionality involved in surface/interface properties is vital for the realization of such devices. Here we investigate the surface behavior of the layered calcium-strontium ruthenate crystals, $Ca_{2-x}Sr_xRuO_4$, grown using the optical floating zone technique by a combination of electron spectroscopy and scanning probe microscopy techniques. Sr_2RuO_4 is a layered metallic perovskite exhibiting p-wave superconductivity below ~1.5K, while the small size of Ca ions in Ca_2RuO_4 results in tilt and rotation of the RuO_6 octahedra giving rise to an antiferromagnetic insulating ground state. Electronic and structural properties of these surfaces are studied by variable temperature Scanning Tunneling Spectroscopy (STS) and Low Energy Electron Diffraction (LEED). It is found that broken symmetry on the Sr_2RuO_4 surface results in the rotation of RuO_4 octahedra relative to bulk positions along the c-axis, changing the relative in-plane Ru-O bond length and shifting the surface phonon energies. The substitution of Sr ions in Ca_2RuO_4 crystals results in a rotation plus a tilt of the RuO_6 octahedra creating a Mott-insulator phase. Particularly, $Ca_{1.9}Sr_{.1}RuO_4$ exhibits a metal to Mott-insulator transition below ~150K in bulk single crystals. However, with STS and High Resolution Electron Energy Loss Spectroscopy (HREELS), we observe a metal to Mott-insulator transition at the surface of single $Ca_{1.9}Sr_{.1}RuO_4$ crystals below ~120K, surprisingly lower than the transition temperature in the bulk. The lowering of transition temperature is intimately related to different lattice distortions at the surface, indicating a strong electron-phonon coupling in addition to electron-electron correlation. These results imply a coexistence of a metallic surface on a nonmetallic bulk. Understanding the coupling between various degrees of freedom on surfaces and interfaces is required to create materials with the desired transport properties necessary for the next generation of electronic devices.

E6.7
Elementary processes during the epitaxial growth of oxides: the case of MgO. Gregory Geneste[1], Joseph Morillo[1], Fabio Finocchi[2] and Marc Hayoun[3]; [1]CEMES, CNRS, TOULOUSE, France; [2]GPS, Univerity Paris 6-7 and CNRS, PARIS, France; [3]LSI/DRECAM/DSM, CEA, PALAISEAU, France.

Metal oxides are nowadays used in many applications (microelectronics, magnetic devices, etc). They may appear as epitaxially grown thin films on various substrates, substrates, or both of them. Due to the intense and rapidly varying microscopic electric field, their electronic properties are very sensitive to the atomic structure, such as the surface flatness and to the details of the interfaces with other materials. The understanding of the basic mechanisms (adsorption, diffusion, etc.) that govern the epitaxial growth is therefore important for technological applications. We focus on oxide on oxide growth studied by means of first-principles and empirical simulations. We performed an overall study of the elementary processes in the prototypical case of MgO homoepitaxy on the MgO(001) surface [1], considering as deposited species atoms (Mg,O) or small molecules (O2, MgO, MgO2) that may occur in molecular beam epitaxy or sputtering. We show that the local electronic and atomic structures play a crucial role in determining the energy landscape that is seen by the diffusing species, diffusion close to atomic steps can be qualitatively and quantitatively different from that on flat terraces: whereas onto the flat surface the diffusing species are the Mg adatom and MgO admolecule, the situation is reversed along the [001] step, the more mobile species being now the O adatom. Also we show that there is no Schoebel barrier accross the [001] step, which favors 2D growth. Moreover, the study of various charge-transfer reactions between the ad-molecules and/or the ad-atoms reveals that the actual surface stoichiometry results from a subtle interplay between their reactivity and diffusing behaviour. For example the O atom sticks to the surface on top of another O atom forming a very stable peroxo-bond. The Mg + O -> MgO reaction at the surface must then proceed with a strong local rearrangement. We show that this reaction (including charge transfer) occurs at very short distances but without any extra barrier than that for Mg diffusion. The computed core-level shifts of the ad-species can be compared to the outcome of X-ray photoemission spectra taken during the growth, thus permitting the identification of the ad-species on real samples. The atomic and electronic structures of small flat ad-clusters are also studied. Finally, we outline a possible scenario for large-scale homo-epitaxy and compare our simulations to available experimental data with particular emphasis on the perspectives of linking our atomic-scale calculations with the macroscopic models that are usually used to describe the crystal growth. In particular, we show that those models must be generalized to account for the larger complexity of the chemistry and the physics at oxide surfaces, compared to elemental metals. [1] G.Geneste et al, Appl. Surf. Sci., 188, (2002) 122-127 ; Surf. Sci., 532-535, (2003) 508-513 ; F. Finocchi et al, Nuovo Cimento, (2003) in press.

E6.8
Optical, Electronic and Interface Studies of ZrO_2 and HfO_2 Thin Films on Si and Amorphous SiO_2. Ciro M Lopez[1], N A Suvorova[1], A A Suvorova[2], M Saunders[2] and E A Irene[1]; [1]Chemistry, University of North Carolina-Chapel Hill, Chapel Hill, North Carolina; [2]Centre for Microscopy and Microanalysis, University of Western Australia, Crawley, Western Australia, Australia.

Zirconia, ZrO_2, and Hafnia, HfO_2, thin films were grown on single crystal MgO(100), Si(100), and amorphous SiO_2 by ion-beam sputter deposition of the parent metal and subsequent oxidation at various temperatures. The optical properties for the ZrO_2 and HfO_2 films as well as the sputter-deposited metals were determined by $in-situ$ spectroscopic ellipsometry(SE) in the photon energy range of 1.5-4.5eV. The nature and optical properties of the interface layers between the dielectric layer and substrate have also been determined. Time of flight mass spectrometry of recoiled ions (TOF-MSRI) and SE performed $in-situ$, along with analytical electron microscopy were used to investigate the material properties of all samples. The interface layer could be investigated separately by growing thin films that were all intermixed. A stacked structure was found where the Si was covered with a SiO_2 layer, an intermixed interface layer and a

pure dielectric layer. The growth dynamics for these layers was determined. Electrical measurements were performed on fabricated Pt/ZrO_2, HfO_2/Si capacitors prepared *invacuo*, in order to determine the fixed charge and dielectric constant for the overall film stack. Interface trap state density (D_{it}) was determined via the conductance method. Variation of D_{it} with various annealing procedures (viz. post-oxidation and post metallization anneals) was also studied.

E6.9
Precise Characterization of Silicon on Insulator (SOI) and Strained Silicon on Si1-xGex on Insulator (SSOI) Stack with Spectroscopic Ellipsometry. Lianchao Sun[1], J.C. Fouere[1], C. Defranoux[2], J.L. Stehle[2] and H.J. Hovel[3]; [1]SOPRA Inc, Westford, Massachusetts; [2]SOPRA SA, Bois Colombes, Paris, France; [3]T. J. Watson Research Center, IBM Corp., Yorktown Heights, New York.

Further improvements in CMOS circuit performance such as switching speed and power reduction will rely on the use of silicon on insulator (SOI) substrates with decreased functional layer thicknesses. According to the International Technology Roadmap for Semiconductors (ITRS), the silicon and buried SiO2 (BOX) layer thicknesses for a fully depleted device should be in the ranges of 10 to 16nm and 24 to 40nm by 2005, respectively. A key issue for fully-depleted CMOS transistors is control of such ultra-thin layer thicknesses and their uniformity along with other parameters such as surface and interface roughness. This poses a challenge to metrology because the layer thicknesses must be determined with angstrom precision. Spectroscopic ellipsometry (SE) is an optical and non destructive technique for determining thin film thickness and material optical properties. Because ellipsometry measures the change in the polarization state for both the amplitude ratio of the p to s polarizations, and in the phase retardation, it provides a precise way to characterize such ultra thin SOI stacks. Comprehensive characterization results for a number of thin and ultra thin SOI stacks with different thickness ranges will be presented together with measurement repeatability results relevant to the film thickness process tolerances. In addition, characterization results for advanced device applications such as strained silicon-on- Si1-xGex-on-insulator (SSOI) will also be shown, demonstrating the use and capability of spectroscopic ellipsometry for precise determination of layer thickness, material composition, interfacial layers, etc. Principles and advantages of the technique will also be discussed in the presentation.

E6.10
AlON Thin Films Formed by ECR Plasma Oxidation for High-k Gate Insulator Application. Go Yamanaka, Takafumi Uchikawa, Shun-ichiro Ohmi and Tetsushi Sakai; Department of Information Processing, Interdisciplinary Graduate School of Science and Engineering, Tokyo Institute of Technology, Yokohama, Kanagawa, Japan.

AlON thin films formed by the electron cyclotron resonance (ECR) plasma oxidation of the AlN layer deposited on Si(100) by ECR sputtering method was investigated for high-k gate insulator application. AlN films (3-4 nm) were deposited on p/p^+Si(100) by ECR sputtering at room temperature, and then the deposited AlN films were oxidized by Ar/O_2 ECR plasma for 15-120 s to form AlON films after the annealing in vacuum (10^{-4} Pa) at 600°C for 3 min. Rapid thermal annealing (RTA) was performed for 1 min 400-1000°C in flowing N_2 ambient. Finally Al or Al/TiN was deposited as a top electrode. It is well known that Al_2O_3 deposited on Si usually shows flat-band voltage shift because of the existence of the negative fixed charge, while the AlON thin films show the excellent electrical characteristics with negligible flat-band voltage shift. The leakage current density was found to be decreased with the ECR plasma oxidation. The equivalent oxide thickness (EOT) of 1.6 nm with the leakage current of 1.1×10^{-3} A/cm^2 was obtained for the film after 120 s ECR plasma oxidation. The surface roughness was also improved from 0.3 nm (15 s oxidation) to 0.16 nm (120 s oxidation) with ECR plasma oxidation. Next, the effect of post-deposition annealing was investigated. The leakage current was found to be decreased without increase of EOT after the 1000°C RTA, while the leakage current was increased after the 400°C RTA. The negative flat-band voltage shift was observed after 400-800°C RTA, while it was not observed after 1000°C RTA. From the XPS measurement, the SiON peak at the interface was found to be weaken after 400°C RTA, while the peak became strong after 1000°C RTA probably because of the interfacial layer formation such as AlSiON with relatively higher dielectric constant compared to that of SiO_2. It was found that the surface and the interface after 400°C RTA became rough compared to the film without the RTA process, while those became smooth, the interfacial layer was clearly observed and the amorphous phase was kept even after 1000°C RTA. It can be considered that the excellent uniformity of the film led to lower leakage current density without increase of EOT. EOT of 2.0 nm with the leakage current of 7×10^{-5} A/cm^2 was obtained for the AlON film formed by the 120 s ECR plasma oxidation with 1000°C RTA.

E6.11
Atomistic simulations of the dynamics of amorphous semiconductors. Sebastian von Alfthan, Antti Kuronen and Kimmo Kaski; Laboratory of Computational Engineering, Helsinki University of Technology, Espoo, Finland.

We have developed computational methods to study crystallization and phase separation in amorphous solids on atomic level. The basic simulation technique is a Monte Carlo (MC) method originally developed by Wooten Wiener and Weaire (WWW). In this WWW method the structure of the material is described by the topology of the bonds connecting the atoms. The system is allowed to evolve by doing trial moves that change the bonding topology. Using this method we are able to directly model the development of the structure of the material. We have improved the WWW method by deriving an algorithm that allows simulation of the NPT ensemble contrary to previous version which were limited to the NVT ensemble. Various computational optimizations which speed up the simulations significantly are also implemented. These methods are used to study the formation of silicon nanocrystals in SiO. This problem has practical applications since one possibility for creating active light emitting devices made of silicon is based on small clusters of crystalline silicon embedded in amorphous SiO_2. We have also used it to study the structure and dynamics of twist grain boundaries and amorphous clusters embedded in a crystalline lattice.

E6.12
Substrate/Oxide Interface Interaction In $LaAlO_3/Si$ Structures. Tito Busani[1,2] and Roderick A Devine[2]; [1]Universite Joseph Fourier, Grenoble, France; [2]Air Force Research Laboratory, Kirtland Air Force Base, Albuquerque, New Mexico.

Amorphous lanthanum aluminate films ($LaAlO_3$) were deposited on Si(100) and Si(111) substrates at room temperature using rf sputtering in pure Ar or an Ar/O_2 mixture with a stoichiometric target. The film composition was analyzed using XPS and EDX. Samples were annealed using either a tube furnace or a rapid thermal system at 900, 950 and 1000 $^\circ$C for between 1 to 10 minutes. The anneal atmosphere was N_2, N_2H_2 or O_2. Typical thicknesses of deposited samples were of the order of 165 nm after sputtering for 120 minutes reducing to 130 nm following an anneal at 950 $^\circ$C for 1 min. The refractive index at 632.8 nm increased from 1.7 (as-deposited) to 2.1 after annealing at 1000 $^\circ$C for 1 minute. FTIR analysis showed only one peak centered at 747 cm^{-1} with an FWHM of 185 cm^{-1} for as-deposited samples indicating an amorphous structure. Annealed samples showed very narrow absorptions at 607, 695-720 and 811 cm^{-1}. No evidence for SiO_2 peaks at $\sim$1060 cm^{-1} was observed indicating that oxygen diffusion in the $LaAlO_3$ structure is limited. Following short time annealing at 1000 $^\circ$C a broad band at 905 cm^{-1} appeared indicating the formation of a layer $\sim$14 nm thick rich in Si-O-La bonds. Nitridation of the substrate before oxide deposition only slowed the formation of the layer, it did not suppress it. X-ray diffraction analysis of the annealed films indicates a very oriented crystalline structure, yet unidentified, whose direction depends upon the orientation of the Si substrate. The dielectric constant in both annealed and as-deposited films was measured to be less then 14, the leakage current density was very low. Some mobile charge was detected. This dielectric constant is substantially less than the value $\sim$ 25 anticipated from bulk, single crystal measurements. Reasons for this discrepancy will be discussed.

E6.13
Al Surface Segregation in Atomic Layer Deposited $ZrO_2/Al_2O_3/Si(100)$ stacks. Giovanna Scarel[1], Sandro Ferrari[1], Marco Fanciulli[1], Yuri Lebedinskii[2] and Andrei Zenkevich[2]; [1]Materials, Laboratorio MDM-INFM, Agrate Brianza, Milano, Italy; [2]Moscow Engineering Physics Institute, Moscow, Russian Federation.

Aluminium surface segregation in the Al_2O_3 form and monolayer thickness through the ZrO_2 layer ($\approx$20 nm thick) is observed to occur in atomic layer deposited (ALD) ZrO_2/Al_2O_3 stacks grown on H terminated Si(100) substrates at 300°C. The stacks are of interest as substitutes of SiO_2 in dielectric gates for CMOS devices. The ZrO_2 layers were grown using $ZrCl_4$ and H_2O as precursors on top of an Al_2O_3 buffer layer, several monolayers thick, grown from $Al(CH_3)_3$ and H_2O. Aluminum surface segregation is observed while profiling the Al depth distribution with x-ray photoelectron spectroscopy (XPS) and time of flight seconday ion mass spectrometry (ToF-SIMS). Unlike well established Si diffusion to the surface through a metal oxide layer, further annealing up to 1000°C does not change Al distribution throughout the film. Stacked ZrO_2/Al_2O_3 layers with similar thickness grown on Si(100) with reactive pulsed laser deposition (PLD) technique and annealed in oxygen at 850°C do not exhibit any Al at the surface. To explain the aluminum segregation at the surface during ALD growth, we propose a model based on a "take-over" of Al atoms during the exchange reactions

involving $ZrCl_4$ and H_2O in the ALD process.

E6.14
Structural and electrical properties of HfO2 films grown by atomic layer deposition on Si, Ge, GaAs, and GaN.
Marco Fanciulli, Giovanna Scarel, Sabina Spiga, Grazia Tallarida and Claudia Wiemer; Laboratorio MDM, INFM, Agrate Brianza (MI), Italy.

The scaling down of modern nano-electronic devices, based on a MOS structure, has motivated an intense activity on high-k dielectrics [1]. Although a large number of materials have been investigated, suitable candidates have not been identified yet. A possible intrinsic problem could be also related to the reduction of the effective electron mobility in the inversion layer of the Si substrate due to remote phonon scattering [2]. Having sacrificed SiO2, the possibility of using different substrates, with a higher carrier mobility, does not look too exotic. Indeed some preliminary work has been already reported on the growth and characterization of different oxides on Ge [3], GaAs [4], and GaN [5]. In this work we report on the structural and electrical characterization of HfO2 films grown by atomic layer deposition (ALD) on Si, Ge, GaAs, and GaN substrates. The HfO2 films were grown at 375 C using a novel precursor scheme where HfCl4 and Hf(OtBu)2(mmp)2 were used as metal and oxygen sources respectively. Due to their low oxidizing power, alcoxides, used as oxygen sources, should assure the reduction of the SiOx interface layer [6], typical of the ALD growth with H2O [7] or O3. Specular x-ray reflectivity reveals similar properties such as surface and interface roughness, thickness, and electronic density on all the samples. The surface morphology was also investigated by atomic force microscopy. Grazing incidence x-ray diffraction shows that, irrespective of the substrate, the films are polycrystalline with a strong monoclinic component. This result is also confirmed by far infrared reflection spectra. The presence of metastable phases of HfO2, as well as the presence of texture will be discussed. Good quality MIS capacitors incorporating HfO2 films were successfully fabricated on the different substrates. The dielectric constant, interface state density, fixed charge density and leakage current were determined for the HfO2 films grown on Si, as reference sample, and on Ge, GaAs, and GaN. The results indicate that the properties of the HfO2 films grown by ALD on alternative substrates are promising for applications in MOSFET devices, although more work needs to be done on the optimization of the interface properties. [1] G. D. Wilk, R. M. Wallace and J. M. Anthony, J. Appl. Phys. 89, 5243 (2001). [2] M.V. Fischetti, D.A. Neumayer, and E.A. Cartier, J. Appl. Phys. 90, 4587 (2001). [3] C. O. Chui et al., IEEE Electr. Device Lett. 23, 473 (2002). [4] D. J. Fu et al., Appl. Phys. Lett. 80, 446 (2002). [5] Agere Systems White Paper, March 2003. [6] M. Ritala et al., Science 288, 219 (2000). [7] G. Scarel, C. Wiemer, S. Ferrari, G. Tallarida, and M. Fanciulli, to be published in the Proceedings of the Estonian Academy of Sciences.

E6.15
Silicate interface formation during the deposition of Y2O3 on Si by PE-MOCVD. Christophe Durand[1], Christophe Vallee[1], Catherine Dubourdieu[2], Marceline Bonvalot[1], Olivier Joubert[1] and Eric Gauthier[3]; [1]LTM, CNRS, Grenoble, France; [2]LMGP, UMR-CNRS, Grenoble, France; [3]IMN-CMC, Nantes, France.

The control of the interface during the deposition process of a high-k material is a key issue for any potential application in high-k -based devices. The challenge is not only to limit the interface formation but also to understand its formation in order to be able to control its thickness and composition. In the case of many high-k materials the silicate appears to be more stable with silicon than the oxide. Zirconium and hafnium silicates have been demonstrated as potential high-k gate dielectrics with an amorphous microstructure after annealing. Yttrium silicate also possesses desirable properties. Previous studies have shown the formation of yttrium silicate by the oxidation of yttrium on silicon in dry air at 500-700°C. This work is focused on the yttrium silicate formation during the deposition by plasma enhanced metalorganic chemical vapor deposition (PE-MOCVD) of Y2O3 on Si and Si/SiO2 substrates. Y2O3 films are obtained by a MOCVD process, which combines plasma assistance and a pulsed-liquid precursor supply set-up. Plasma assistance enables the lowering of the deposition temperature. The liquid supply system used is based on the sequential injection of micro-amounts of precursors inside an evaporator. The precursor Y(tmhd)3 is dissolved in a solvent (cyclohexane) and is maintained at room temperature in a closed vessel under a 2 bar inert atmosphere (N2). The yttrium silicate formation was studied as a function of the injection frequency of reactive species. It is shown that the silicate formation can be limited by increasing the injection frequency. This is discussed based on X-ray Photoelectron Spectroscvopy analyses performed at different take-off angles as well as Transmission Electron Microscopy and Electron Energy Loss Spectroscopy analyses. The first stages of the growth were investigated by atomic force microscopy. A study of the bonding environments in the grown material and at the interface was also carried out using absorbance Attenuated Total Reflection (ATR) spectroscopy in p-polarization. The O2 plasma influence on the silicate formation will also be discussed.

E6.16
Atomic Layer Deposition of HfO_2/Al_2O_3 and ZrO_2/Al_2O_3 Films for Gate Dielectric Applications. Jaehyoung Koo and Hyeongtag Jeon; Division of Materials Science and Engineering, Hanyang University, Seoul, South Korea.

The high dielectric materials of Al_2O_3, Hf-based oxide films, and Zr-based oxide films have been widely investigated mainly due to thier large band gap, good thermal stability, and relatively higher dielectric constant compared to SiO_2. In this study, we investigated the comparison characteristics of HfO_2/Al_2O_3 and ZrO_2/Al_2O_3 films as well as their physical, chemical and electrical properties for gate dielectric applications. HfO_2/Al_2O_3 and ZrO_2/Al_2O_3 films were successfully deposited by atomic layer deposition (ALD) method using tri-methyl aluminum (TMA), $HfCl_4$ and $ZrCl_4$ as Aluminum, Hafnium and Zirconium precursors, respectively. The electrical properties including equivalent oxide thickness, hysteresis, leakage current and dielectric constant were calculated and analyzed by using capacitance-voltage (C-V) and current density-voltage (J-V) measurements. For the evaluation of the physical and chemical characteristics of HfO_2/Al_2O_3 and ZrO_2/Al_2O_3, these films were analyzed by cross-sectional transmission electron microscope (XTEM), Auger electron spectroscopy (AES), Medium energy ion scattering spectroscopy (MEIS) and X-ray photoelectron spectroscopy (XPS). In these results, the amount of carbon impurity of Al_2O_3, HfO_2, ZrO_2, HfO_2/Al_2O_3 and ZrO_2/Al_2O_3 films deposited by ALD were below 3 at.%. Al_2O_3 films showed an amorphous structure without having an interfacial layer. However, HfO_2 and ZrO_2 films showed randomly oriented polycrystalline structure. This paper will discuss the systematic analysis of HfO_2/Al_2O_3 and ZrO_2/Al_2O_3 films deposited by ALD method for gate dielectric applications.

E6.17
Characteristics of Al_2O_3 Films Deposited by Atomic Layer Deposition Method Using Various Oxidants. Seungho Lee, Jaehyoung Koo and Hyeongtag Jeon; Division of materials Science and Engineering, Hanyang Univ., Seoul, South Korea.

As the gate oxide thickness of metal−oxide−semiconductor (MOS) devices is scaled down to the sub−100nm, tunneling leakage current through gate dielectrics and reliability become serious problems. Thus, the high−k gate dielectrics become one of the solutions in providing increased capacitance and reduced leakage currents without significantly increasing the actual equivalent oxide thickness(EOT) of gate dielectrics. Among the high−k materials, Al_2O_3 thin film is one of the high−k materials that alternate SiO_2 gate dielectric due to high dielectric constant, large band gap and low leakage current and excellent surface properties. In this paper we will present the results of ALD grown Al_2O_3 films with varying the different reactants. Al_2O_3 films were deposited on p−type Si (100) substrate using trimethyl−aluminum (TMA, $(CH_3)_3Al$) or dimethyl−aluminum−isopropoxide (DMAP,$(CH_3)_2AlOCH(CH_3)_2$) precusor with various oxidants of O_2, H_2O and N_2O. And we will also compare the results with plasma assisted Al_2O_3 films with non−plasma assisted films. The physical and chemical properties were analyzed by cross sectional transmission electron spectroscope (XTEM), Auger electron spectroscopy (AES) and X−ray photoelectron spectroscopy (XPS). Also, electrical characteristics, including equivalent oxide thickness (EOT), hysteresis, leakage current were analyzed by I−V and C−V measurements. The results of these study showed a clean amorphous and stoichiometric Al_2O_3 films with low carbon concentration, low leakage current and high dielectric constant. In this paper, we will present the Al_2O_3 films as a gate dielectric and compare the characteristics of Al_2O_3 grown by PEALD and MOALD.

E6.18
Characterization of the amorphous high-k oxide Lu2O3.
Maurizio Zaccheddu and Vincenzo Fiorentini; Dept. of Physics, University of Cagliari, Monserrato, Italy.

High-k oxides are currently under scrutiny as possible candidates to replace silica in Si CMOS gates. We investigated the structure of the amorphous phase of a representative X2O3 rare-earth oxide, lutetia (Lu2O3), whose crystalline phase is cubic bixbyite. Amorphization is effected by melt quench using constant-pressure molecular dynamics with shell-model interatomic potentials, at various cooling rates (down to 7 K/ps, with a rate-dependent density drop of over 30%). Configurational entropy is estimated by information-theoretic methods. Using ab initio DFT techniques, the amorphous configuration is further optimized in volume and internal structure. The amorphous structure carries significant reminders of the parent crystalline structure in the Voronoi tessellation and the radial,

angular, and first-neighbor-count distribution functions. All the named indicators show that in the amorphous phase the cation-oxygen units are internally more compact and on average more widely separated than in the crystal, leading to both an increased density and a reduced dielectric constant.

E6.19
An Original Method To Detect Interaction Between Poly-Si/Hi-K Dielectrics. Huicai Zhong, Jon Kluth, Matthew Buynoski, Wayne Wu, Joong Jeon, QI Xiang, Farzad Arasnia, Bob Clark-Phelps and Bob Ogle; Technology Development, Advanced Micro Devices, Sunnyvale, California.

Possible interface interaction between poly-Si and high dielectric constant (Hi-K) dielectrics has great impact on CMOSFET device performance using Hi-K films as gate dielectrics. Conventional detection techniques such as TEM or by electrical characterization from MOSFET are expensive and time-consuming. In this paper, an original method is proposed to detect possible interface interaction between poly-silicon/ Hi-K dielectrics by using mercury-probe station Capacitance-Voltage (CV) and Current-Voltage (IV) measurement for blank films. The Hi-K dielectric film was ~3nm nitrided Hf-silicates (HfSiON) prepared by MOCVD technique on P-type silicon substrate. After dielectric film deposition, a 20nm poly-Si was deposited on HfSiON film at 5750C, 40Torr without doping. Film stack with poly-Si/SiO2 on Si was used as a reference. CV and IV measurement was done on blank film stack using mercury probe station before and after poly-Si deposition. Before poly-Si deposition, the electrical equivalent oxide thickness for HfSiON and SiO2 was 11A and 17A, respectively. After poly-Si deposition, the poly-Si/Hi-K had EOT ~77A while poly/SiO2 stack ~81A, which clearly showed that poly-Si was working as dielectric with dielectric constant ~12. Significant depletion region capacitance increase for CV curves of poly-Si/Hi-K stack compared to poly-Si/SiO2 stack was observed. This indicated possible interface interaction between poly-Si and Hi-K dielectrics introduced by poly-Si deposition. The possible mechanism was that Hafnium-Oxygen bonding within HfSiON was decomposed by high concentration active atomic H species thus enabled Hf ions diffusing into silicon substrate during high-temperature poly-silicon deposition. In order to stop possible Hf diffusion, SiO2 dielectric layer between HfSiON and Si substrate with thickness varying from 5A to 17A was used as interfacial diffusion stop layer. It was found that 5A SiO2 interfacial layer was thick enough to prevent possible Hf diffusion into Si. In contrast, Si3N4 with thickness up to 20A was not effective to stop possible Hf diffusion.

E6.20
High thermal stable $(HfO_2)_{1-x}(Al_2O_3)_x$ gate dielectrics for application in 50-nm generation devices. Qin Li[1], S J Wang[2], P C Lim[2], A C H Huan[2,1] and C K Ong[1]; [1]Department of Physics, National University of Singapore, Singapore, Singapore; [2]Institute of Materials Research & Engineering, Singapore, Singapore.

The silicon dioxide gate dielectric is approaching its application limit due to the exponential increase in tunnelling current and intrinsic reliability concerns as the device scales to sub-100 nm dimensions. One solution is to find suitable materials of higher dielectric constants (k) to replace silicon dioxide (SiO_2). For silicon-based technology, SiO_2 is used as an amorphous layer and the semiconductor industry is comfortable with this approach. In contrast, very few high-k metal oxide materials possess resistance to crystallization as displayed by SiO_2. Therefore, the ability to fabricate high thermal stability amorphous metal oxides is still sought after for the application of such oxides in semiconductor technology. In this report, the high thermal stable amorphous thin films of $(HfO_2)_{1-x}(Al_2O_3)_x$ were fabricated by a novel pulsed laser deposition technique on p-type Si (100). The rapid thermal annealing (RTA) effect on the microstructrual and electrical properties of the films were studied. It was found the films with more than 80% HfO_2 content still retain their amorphous structure after the RTA process. The TEM and electrical measurements yield a dielectric constant of about 19 for the films. However, SIMS and XPS studies suggest that Hf atoms have diffused into the silicon substrate, forming silicide bonds after the RTA process. Under optimized condition, ultra-thin films with equivalent oxide thickness 0.9 nm have been obtained. At bias voltage of 1 V, the leakage current density is about $3.9x10^{-2}$ A/cm^2. The results demonstrate that the ultra-thin $(HfO_2)_{1-x}(Al_2O_3)_x$ film is sufficiently stable against crystallization during rapid thermal annealing, and show promise as a gate dielectrics in future silicon-based devices.

E6.21
Phase Stability Study of HfO_2 and HfO_2-Al_2O_3 Alloy Thin Films. Kwee Lee Tok[1], Zexiang Shen[1], Andrew T S Wee[1], Chia Ching Yeo[2], Byung-Jin Cho[2], Thomas Osipowizc[1] and Jiazhen Zheng[1]; [1]Physics, National University of Singapore, Singapore, Singapore; [2]Electrical and Computer Engineering, National University of Singapore, Singapore, Singapore.

Due to its high dielectric constant, HfO_2 (κ~20) is a potential candidate for gate oxide replacement. However, as HfO_2 is not thermally stable and crystallizes at about 400 C, alloy materials that incorporate SiO_2 and Al_2O_3 have been recently studied. In this study, we investigate the crystallization phases of HfO_2 and HfO_2-Al_2O_3 thin films (~20nm) prepared by ALCVD. Samples were deposited on p-type Si(100) substrates at 300 C. Characterization techniques used include FTIR, RBS, XPS and glancing incidence XRD (GI-XRD). Samples were annealed using RTP up to a temperature of 1000 C. GI-XRD results show that as-deposited HfO_2 thin films are amorphous with a small degree of crystallization. After annealing at 400 C, mixed monoclinic and tetragonal phases are observed. Complete transformation of HfO_2 thin films from tetragonal to monoclinic phase occurs after annealing at 1000 C. HfO_2-Al_2O_3 thin films remain amorphous up to an annealing temperature of 800 C. At 1000 C, crystallization occurs for films with greater than nominal 40% HfO_2. The effect of suppressed crystallization was more pronounced in HfO_2-Al_2O_3 thin films with higher Al_2O_3. In particular, we observed that the diffraction peaks of HfO_2-Al_2O_3 films shift towards higher diffraction angle when compared to HfO_2 thin films as a result of reduced bond length. In addition, the HfO_2-Al_2O_3 thin films crystallize in the tetragonal phase in high Al_2O_3 matrix and it crystallizes in the monoclinic phase otherwise.

E6.22
A Study of MOCVD-Grown HfO_2 Thin films Using a Novel Precursor. M. S. Dharmaprakash[1], G. C. Deepak[2], Navakanta Bhat[2] and S. A. Shivashankar[1]; [1]Materials Research Center, Indian Institute of Science, BANGALORE, Karnataka, India; [2]Devices Lab, ECE Department, Indian Institute of Science, BANGALORE, Karnataka, India.

A novel metalorganic complex, Nitratotris(2,2,6,6-tetramethyl-3,5-heptadionato)hafnium(IV), $Hf(thd)_3NO_3$, has been synthesized and characterized by IR, NMR, MS spectroscopic techniques and elemental analysis. The crystal structure of the complex has been confirmed by single crystal XRD. The thermal characteristics of this complex have been studied by TG/DTA. The metalorganic complex is volatile, starts subliming at about 150°C, with the weight loss amounting to about 6% of the initial sample weight at 160°C. Thin films of hafnium dioxide (HfO_2) are deposited by low-pressure MOCVD using this complex as precursor, on various substrates such as Si(100), fused silica, glass and, polycrystalline alumina, in a horizontal hot wall reactor built in house. The deposition temperature and pressure were in the range of 400-700°C and 2-10 torr respectively. The HfO_2 thin films are characterized by XRD, SEM and FTIR. The dielectric characteristics of as deposited films and the films annealed at different temperatures (oxygen/argon ambient) are studied by HFCV and IV measurements. The HFCV hysteresis and leakage current reduces in the annealed samples. The dielectric constant calculated from the experimental data is found to be in the range of 9-13.

E6.23
Annealing Behaviors of Void-type Defects in SiO2/SiC Probed by Slow positron Beam. Min Gong[1], Hongjun Liu[1], Haiyun Wang[2], Huiming Weng[2] and Wen Yang[1]; [1]Department of Physics, Sichuan University, Chengdu, Sichuan, China; [2]Department of Modern Physics, University of Science and Technology of China, Hefei, Anhui, China.

Silicon carbide has been realized to be one of the powerful semiconductors. Various kinds of devices, including Schottky diodes, bipolar-transistors, MOSFETs and some IC units with good properties, have been manufactured using SiC. In these devices, SiO2 films play important roles. However, since the existance of carbon atoms, qualities of thermal oxidation formed SiO2 films on SiC wafers were far from as good as those on Si. The effects of impurities on the C-V characteristics of SiO2/SiC have been investigated by using atoms sensitive probes such as the secondary ion mass spectrometry (SIMS) and the x-ray photoelectron spectroscopy (XPS). These analyzing techniques are not adequate for full understanding of characteristics of SiO2/SiC interface and structure of SiO2 film since a large of void-type defects will form during thermal oxidation and post-annealing due to the removal or escape of C atoms and CO molecules. In this work, the technique of Doppler broadening of positron annihilation spectroscopy (PAS) has been used to reveal information on void-type defects of SiO2/SiC system. Variable-energy positron beam makes positrons to different depth in the sample. The value of the S-parameter, which reflects the number of positrons annihilated with low-momentum electrons, increases since the reduced electron density at open volume defects narrows the momentum distribution. The SiC materials used in the experiments were obtained from Cree. The wafers were 6H-SiC (0001) having basic nitrogen and aluminum dopants of 1x10Î7cm-3 in n- and p-type samples, respectively. Dry oxidation was carried out at 1150C for 6 hours.

Post-annealing were done at 1100C in nitrogen gas. The thickness of the SiO2 film was about 0.6 nm measured by ellipsometry. Variable energy (0-20 keV) positron beam made the positrons stop and annihilate at different depth from the SiO2 surface to the SiC bulk. The measurement results obviously showed that the S-parameters in the range of SiO2 films have decreased after annealing. This indicated that a large of void-type defects have formed during the oxidation and its density reduced after post-annealing, which probably is one of the reasons of better C-V characteristics of SiO2/SiC MOS structures after annealing in nitrogen gas reported in the previous works. That the results could been observed in all the n- and p-type samples means that the defects in either kind of samples have similar charge states. These phenomena were different from the observation by a recent report in which the positive charged interface states of SiO2/p-SiC were not positron sensitive. Further discussions are presented in this paper.

E6.24
Stoichiometric control of ZrO_2/SiO_2 films using atomic layer deposition. Lijuan Zhong[1], Fang Chen[2], Stephen A Campbell[2] and Wayne L Gladfelter[3]; [1]Dept. Chem Engn & Mats Sci, University of Minnesota, Minneapolis, Minnesota; [2]Dept. Elect & Comp Engn, University of Minnesota, Minneapolis, Minnesota; [3]Dept. Chemistry, University of Minnesota, Minneapolis, Minnesota.

The atomic layer deposition (ALD) of tri (tert-butoxy) silanol and anhydrous zirconium nitrate was used to deposit zirconium silicates on Si (100) substrates at a low temperature (162 ºC). The atomic/molecular layer-by-layer growth associated with the ALD technique allows growth of smooth and uniform films with controllable thickness. The highest growth rate obtained was 12Å/cycle. The film composition (Zr/(Si+Zr) ×100%) ranged from 3.3% to 48.6% dependent on the pulse time of each precursor. The roughness of films was 0.3% to 0.4% of the film thickness as revealed by atomic force microscopy. The refractive indices (n) were measured by ellipsometry and ranged from 1.4 to 1.8. The effective dielectric constants (κ) of films ranged from 3.8 to 11.1. Both the refractive indices and dielectric constants exhibited a linear dependence on the concentration of zirconia in the film.

E6.25
Improved structural properties of sputtered hafnium dioxide on silicon and silicon oxide for semiconductor and sensor applications. Heinrich Grueger, Christian Kunath, Eberhard Kurth, Stephan Sorge and Wolfram Pufe; Sensors Division, Fraunhofer IPMS, Dresden, Saxony, Germany.

Hafnium dioxide HfO2 is a candidate with promising properties for semiconductor industries as well as for optical and sensorical applications under harsh environments. The material can be deposited using various techniques such as CVD or PVD, some of them are suitable for replacement of silicon dioxide SiO2 and other gate dielectrics in MOS devices. The chemical inertness of HfO2 and the high band gap draw the attention of this paper towards application in optics as active and protective layer at the same time, chemical and physical sensors, such as moisture sensors and thin film capacities. In order to achieve optimized layer properties for the sensorical application in mind, the deposition process and the post-processing need to be tightly controlled. So, dense layers with a low amount of voids and a suitable grain structure can result. This way the layers feature the high inertness of HfO2 to the environment as well as to the underlayer. Layers with thicknesses between 25 and 150nm have been deposited by R.F. sputtering of high purity targets onto bare or oxidized silicon wafers under Ar- or Ar/O2-athmospheres. Initially the HfO2 has a mainly amorphous structure. Subsequent annealing controls the growth of recrystallized areas characterized by grain size and ratio between crystals and amourphous bodies. High heating rates (RTA) of about 50K/s and annealing temperatures ranging 800 to 1000 degree Celcius seem to be advantegous for the area of interest. The layers structure such as grain size, crystal type and transparency was investigated using AFM, TEM, XPS, SEM, XRD and ellipsometry. Layer tension was evaluated using laser deflection. The differences in structure found have been correlated to the results obtained in layer applications. The results are also discussed in comparision to SiO2 and tantalum-(V)-oxide Ta2O5.

E6.26
Abstract Withdrawn

E6.27
Flatband Voltage Shift of MOS Capacitors with Tantalum Nitride Gate Electrodes Induced by Post Metallization Annealing. Masaru Kadoshima[1], Katsuhiko Yamamoto[1], Hideaki Fujiwara[1], Koji Akiyama[1], Koji Tominaga[1], Nobuhisa Yamagishi[1], Kunihiko Iwamoto[1], Morifumi Ohno[1], Tetsuji Yasuda[2], Toshihide Nabatame[1] and Akira Toriumi[2,3]; [1]MIRAI-ASET, Tsukuba, Ibaraki, Japan; [2]MIRAI-ASRC, AIST, Tsukuba, Ibaraki, Japan; [3]The University of Tokyo, Tokyo, Japan.

Tantalum nitride (TaN) films are one of the alternative gate electrodes for scaled MOSFETs. However, reported values of the flatband voltage (V_{FB}) of MOS capacitors with TaN gate electrodes exhibit broad distributions [1, 2], presumably because V_{FB} is dependent on the fabrication process and deposition method. In the present study, we have investigated V_{FB} shifts of TaN gate MOS capacitors. TaN layers were deposited by DC magnetron sputtering or ultra high vacuum chemical vapor deposition (UHVCVD) using $Ta[NC(CH_3)_2C_2H_5][N(CH_3)_2]_3$ as a precursor. In the case of sputtered TaN gate, the effective work function (Φ_M) estimated from the relationship between V_{FB} and EOT in TaN/ SiO_2/ p-Si MOS capacitors was 4.35eV after post metallization annealing (PMA) at 400°C and shifted to the midgap (4.7eV) after PMA at 800°C. The similar V_{FB} shift by PMA was also observed in TaN/ Al_2O_3/ SiO_2/ p-Si and TaN/ Ta_2O_5/ SiO_2/ p-Si capacitors. Moreover, V_{FB} of MOS capacitors with TaN gate electrodes deposited by UHVCVD at 450°C also showed the same behavior by PMA at 800°C. These results strongly suggest that this V_{FB} shift caused by PMA does not originate from the reaction between TaN gate and the dielectric layer. This is mainly dependent on the PMA temperature regardless the deposition methods. Therefore, the maximum processing temperature after TaN gate electrode deposition is important in order to control the threshold voltage of TaN gate MOSFETs. This work was supported by NEDO. [1] Y. H. Kim et al., IEDM Technical Digest (2001) 667. [2] J. K. Schaeffer et al., J. Vac. Sci. Technol. (2003) 11.

E6.28
HfO2, ZrO2 and Al2O3 Atomic Layer Deposition: from molecule/surface interaction to film growth through multi-model methodology. Alain Esteve[1], guillaume mazaleyrat[1], leonard jeloaica[1] and mehdi djafari rouhani[1,2]; [1]MIS, LAAS-CNRS, Toulouse, France; [2]Laboratoire de Physique des Solides, Toulouse, France.

The continuing downscaling of devices has reached a point where traditional ultra-thin layers of thermally grown silicon dioxide have to be replaced by alternative high-k dielectrics. The associated nanoscale complex geometry requirements can only be met by specific experimental techniques such as Atomic Layer Deposition. In parallel, a new generation of modelling tools have to be developed to provide atomic scale expertise of technology process calibration. This last point necessitates multi-model modelling strategy: first principle based models to investigate the elementary chemical reactions and Kinetic Monte Carlo modelling to account for the subsequent layers or film structuring as a function of the experimental parameters. We present DFT calculations of the initial stage of high-k deposition on hydroxylated SiO2. Different aspects of possible reactions are investigated. The decomposition of HfCl4, ZrCl4 and Al(CH3)3 (TMA) precursor molecules and further reactions of the resulting configurations under water exposure are detailed. Reaction pathways and associated activation barriers are given. Zr and Hf based precursors exhibit different behaviour compared with TMA. In particular, TMA dissociation is found to be strongly exothermic. We then show how Kinetic Monte Carlo procedures can be derived from these elementary mechanisms. Preliminary simulations are linked with recent experimental results that underline the key role of the Monte Carlo technique to provide insights in both basic mechanism issues and processing considerations.

E6.29
Liquid precursor deposition and characterization of p-type transparent conducting oxide-Cu2SrO2. Banasri Roy[1], Dennis Readey[1,2], John Perkins[2], Philip Parilla[2], Charles Teplin[2], Tanya Kaydanova[2], Alex Miedaner[2], Calvin Curtis[2] and David Ginley[2]; [1]Metallurgical and Materials engg., Colorado School of Mines, Golden, Colorado; [2]NREL, NVPV, Golden, Colorado.

The p-type transparent conducting oxide Cu2SrO2 has been deposited by chemical solution route for the first time. Samples were made by spray deposition on fused silica substrates using an aqueous solution of Copper formate and Strontium acetate. Phase pure materials were obtained by using a two stage annealing sequence. An initial 30-minute 750C anneal in air converts the spray deposited precursor mixture to Cu2SrO3. A subsequent 4 hour anneal at 775C under ~10-5 Torr working oxygen pressure yields almost phase pure Cu2SrO2.This two step annealing process was found to be critical to the reproducible formation of phase pure Cu2SrO2. However, the morphology of these spray deposited samples was powdery and not transparent. So a sol-gel approach was taken to make good quality homogeneous films. The sol was made from Copper Acetate and Strontium Acetate using methanol as a solvent. Films were deposited by repeated spin coating of the sol followed by a bake at 4500C and finally a two-step annealing process similar to that used for the spray deposited samples was used to get Cu2SrO2. The phase purity of the films has been confirmed by X-ray diffraction method and the

conductivity (~ 10-3 S/cm) was measured by four-probe method. K-doping using K-tributoxide to made Cu2Sr1-xKxO2 is being investigated with the goal of increasing and optimising the p-type conductivity and other electro optical properties of this material σ

E6.30
Transparent Transistors Based on Semiconducting Oxides.
Yongwook Kwon[1], Y. Li[1], Y.W. Heo[1], M. Jones[1], V. R. Varadarajan[1], B.S. Jeong[1], J. Zhou[1], S. Li[2], H. Paul[1] and D. P. Norton[1]; [1]Materials Science and Engineering, University of Florida, Gainesville, Florida; [2]Electrical & Computer Engineering, University of Florida, Gainesville, Florida.

The synthesis and properties of transparent thin film transistors (TFTs) is reported using pulsed laser deposition. The filed effect transistors are with ZnO and $SrCu_2O_2$ serving as the channel material. Low leakage current density is achieved with amorphous $(CeTb)MgAl_{11}O_{19}$ (CTMA) serving as the gate oxide, whose dielectric strength is measured to be > 5MV/cm for structures fabricated on Indium Tin oxide (ITO) substrates. Capacitance-voltage properties show that n-type active layers are realized with undoped ZnO. Little hysteresis effects are observed when gate voltage is swept from accumulation to depletion. Charge densities in undoped ZnO are measured to be 10^{18} to 10^{19} / cm^3 using Hall measurement and CV plots. Current-voltage measurements for TFT operation are reported. Channel materials with thickness ranging from 20 to 200nm on patterned substrates show high conductance and modulation of channel conductance. C-V measurements with MOS structure using doped $Zn_xMg_{1-x}O$ and $SrCu_2O_2$ will also be described. The properties of depletion mode TFTs fabricated with doped and undoped oxide channel will be discussed in detail.

E6.31
Effects of Ge on Thermal Decomposition of Ultrathin Silicon/Germanium-on-Insulator.
Pengpeng Zhang[1], Bin Yang[1], Paul Rugheimer[1], Feng Liu[2] and Max G Lagally[1]; [1]University of Wisconsin-Madison, Madison, Wisconsin; [2]University of Utah, Salt Lake City, Utah.

Silicon-on-insulator (SOI) substrates have attracted much attention because they greatly enhance the performance and reduce the power consumption of CMOS transistors. As the Si template layer thickness in SOI is reduced, it becomes more and more thermally unstable, decomposing into silicon islands at temperatures approaching processing temperatures [1,2]. We have studied the effect of Ge deposition on the thermal decomposition of thin SOI. The thermal decomposition temperature of ultrathin SOI decreases with increasing Ge coverage. The long-range ordering of 3D Si islands seen in the decomposition of SOI is gradually lost with increasing Ge coverage. This observation can be understood in terms of misfit strain and surface energy anisotropy. As the Ge coverage increases, misfit strain increases, making the Si-Ge layer less stable. It should thus decompose more easily. Furthermore, the surface energy anisotropy between (111) and (131) facets on Si-Ge islands is smaller than that for the same facets on Si islands. Consequently, Si-Ge islands are not strongly faceted. The driving force for ordering along <013> directions that is the hallmark of decomposition on SOI is therefore absent when Ge is deposited on SOI, and the 3D Si-Ge islands are randomly distributed. The lowering of the decomposition temperature of SOI that contains Ge in or on the Si template layer suggests that the allowable processing temperatures or the thinness of SGOI that can be used may be limited. [1] B. Legrand, V. Agache, J. P. Nys, V. Senez, and D. Stievenard, Appl. Phys. Lett. 76, 3271, 2000; [2] R. Nuryadi, Y. Ishikawa, and M. Tabe Appl. Surf. Sci. 159, 121, 2000. Research supported by DARPA and DOE

E6.32
Study of work function of CVD WSix thin film on high K dielectric.
Sylvain Maitrejean[1], Stephane Allegret[2], Frederic Fillot[1], Thierry Farjot[1], Francois Martin[1], Bernard Guillaumot[2] and Gerard Passemard[3]; [1]CEA-LETI, Grenoble, France; [2]STMicroelectronics, Crolles, France; [3]STMicroelectronics, Grenoble, France.

To meet requirements of CMOS circuits at sub 65nm scale, gate oxide thickness shall decrease. Thus high K materials are needed as dielectric gate. In this setting, due to gate depletion effect, metallic material should be used as en alternative to polysilison gate. Moreover, specifications on threshold voltage require modulation of gate material work function with respect to NMOS or PMOS transistor. WSix work function is known to be sensitive to material stoichiometry. In this work, WSix thin films with x between 2.2 and 2.5 are evaluated as metal gate on HfO2 and SiO2 dielectric. Film chemical characteristics are correlated with work function measurements. Thin films are deposited using WF6 and dichlorosilane on a 200mm Si wafer industrial chamber. Thermal treatments are applied to sample in order to recrystallise the film and confirm it stability. MOS Capacitors are processed. Electrical characterizations (capacitance vs voltage) are used to extract work function with respect to film composition. The classical phase transformation from hexagonal to tetragonal after thermal anneal is observed using X-Ray diffraction. Nevertheless, no strong morphological and compositional changes are detected after anneal using AFM, SEM observations, RBS and SIMS measurements. This indicates that films are stable up to 800°C anneal. Nominal film stoichiometry is evaluated by RBS. Using these characterizations and SIMS data, concentration profiles are obtained. A W/Si gradient is observed between dielectric/film interface and film surface. At dielectric/WSix interface Si/W ratio is constant whatever the nominal stoichiometry. These results are in agreement with work function measurements.

E6.33
Oxide Reduction in Advanced Metal Stacks for Microelectronic Applications.
Wentao Qin, Alex Volinsky, Dennis Werho and David Theodore; Process and Materials Characterization Lab, Motorola, Tempe, Arizona.

Aluminum and copper are widely used for microelectronic interconnect applications. Interfacial oxides can cause device performance degradation and failure by significantly increasing electrical resistance. Interfacial oxide layers found in Al/Ta and Ta/Cu metal stacks were studied with Transmission Electron Microscopy (TEM) combined with Energy Dispersive Spectroscopy (EDS) and Parallel Electron Energy Loss Spectroscopy (PEELS). The analysis indicates that the observed interfacial oxide layers, Al2O3 and Ta2O5, result from spontaneous reductions of Ta oxide and Cu oxide, respectively. Classical thermodynamics enables interpretation of the results.

E6.34
Thickness Effect of C40 $TiSi_2$ to C54 $TiSi_2$ Transformation.
Ze Xiang Shen[1], Swee Ching Tan[1], Yuping Zheng[1] and Alex See[2]; [1]Physics, National University of Singapore, Singapore, Singapore; [2]Chartered Semiconductor Manufacturing, Singapore, Singapore.

$TiSi_2$ C54 is widely used as a low resistivity contacts in CMOS devices. C54 is normally formed by thermal annealing of the $TiSi_2$ C49 phase between 750-850 C. However, due to the so called narrow line effect, the C49 to C54 transformation on narrow poly-silicon lines requires very high annealing temperature, which could result in severe problems like punch through and agglomeration and even device failure. Recently, significant breakthroughs have been made such that the C54 phase is formed from a $TiSi_2$ C40 template, completely bypassing the C49 phase and allowing direct formation of C54 at a low temperature of around 700 C. The thin C40 film itself can also be transformed to C54 easily at a relatively low temperature, making it a real possibility to extend the application of $TiSi_2$ for sub quarter-micron devices. The promotional template effect of C40 phase on the formation of C54 phase has been discussed extensively, which is due primarily to the similarity between the basal planes of C40 and C54 where the C40 has an ABCABC arrangement while C54 has an ABCDABCD arrangement. However, how the C40 transforms to C54 is much less clear as the 3D structures of the two phases are very different and it is difficult to understand the low temperature needed to transform C40 to C54. In this presentation, we discuss the thickness effect of pure C40 $TiSi_2$, induced by two different types of pulsed lasers - Nd:YAG and excimer. The C40 $TiSi_2$ induced by Nd:YAG laser (~70 nm) is thicker than the C40 $TiSi_2$ induced by excimer laser (~15 nm). While the thinner C40 requires only RTP at 700 C for 60 s (corresponding to an activation energy E_{40} = 2.5 eV) to transform to C54, the thicker C40 $TiSi_2$ requires a very high temperature of around 1000 C for 60 s (E_{40} = 6.5 eV) to transform to C54, which is even higher than the activation energy for C49 to C54 transformation in the range of E_{49} = 3.5-6 eV. It is worth noting that the activation energy E49 increases when the thickness of C49 $TiSi_2$ layer decreases, reflecting the fact that the C54 phase nucleate at the triple grain boundaries of the C49 grains. However, the activation energy E_{40} increases with increase in C40 $TiSi_2$ layer thickness, demonstrating that the C40 to C54 transition is via a different mechanism.

SESSION E7: Epitaxial Oxides on Semiconductors
Chairs: Supratik Guha and Gerd Norga
Wednesday Morning, December 3, 2003
Room 207 (Hynes)

8:30 AM E7.1
Epitaxial $SrTiO_3$ Films on Silicon: Medium Energy Ion Scattering Studies.
Lyudmila Goncharova[1], Dmitri Starodub[1], Eric Garfunkel[1,2], Torgny Gustafsson[1], Venugopalan Vaithyanathan[3] and Darrell Schlom[3]; [1]Physics Department, Rutgers University, Piscataway, New Jersey; [2]Chemistry Department, Rutgers University, Piscataway, New Jersey; [3]Department of Material Science and Engineering, Penn State University, University Park, Pennsylvania.

Perovskite metal oxide films, such as $SrTiO_3$ (STO), have become a technologically important class of materials due to their interesting electronic, optical, and magnetic properties. They have significant potential to enable a variety of new applications, either as novel active materials, or as thin buffer layers enabling other integrated heterostructures to be grown on semiconductors such as silicon. For epitaxial films it is usually assumed critical to achieve structural matching of the two phases that meet at the interface while retaining chemical phase separation. Therefore it is necessary to eliminate or at least control any amorphous or compositionally mixed interfacial layer between the layers (epitaxial STO and Si, in our case) by controlling the deposition conditions and the specific growth sequence used in the experiments. We have used high-resolution medium energy (~ 100 keV) ion scattering (MEIS) to investigate the composition as a function of depth of thin (<25nm) crystalline SrTiO3 films on Si (100). This technique allows us to get quantitative information both about the film/vacuum and about the film/substrate interface structure. The thin $SrTiO_3$ films we have investigated were deposited on Si (001) at low temperatures in an excess of oxygen and then recrystallized through solid phase epitaxy by heating the films in vacuum. Our MEIS results show that films grown by this method have A-site (SrO) termination. Submonolayer amounts of strontium silicide, used in the initial stages of growth, are fully replaced with a crystalline silicate at the interface after growth is completed. In addition, Ti has diffused into the interface region. MEIS results indicate that the $SrTiO_3$/Si interface is crystalline; however the geometrical structure deviates significantly both from the bulk epitaxial film and from the substrate. Resulting interfacial composition and mechanisms for Ti, Sr, and Si diffusion in the interface region will be discussed.

8:45 AM E7.2
Characterization of the Interface between Epitaxial $SrTiO_3$ and Silicon. S. J. Wang[1], Ach Huan[1], W. Tian[2], X. Q. Pan[2], V. Vaithyanathan[3], D. G. Schlom[3], T. Gustafsson[4] and E. Garfunkel[4]; [1]Institute of Materials Research & Engineering, Singapore, Singapore; [2]Department of Materials Science and Engineering,, The University of Michigan, Ann Arbor, Michigan; [3]Department of Materials Science and Engineering,, Penn State University, University Park, Pennsylvania; [4]Chemistry and Physics Depts, Rutgers University, Piscataway, New Jersey.

Epitaxial oxides on semiconductors need to have excellent physical properties and chemical stability for a variety of potential applications including gate dielectrics, ferroelectric random access memories, and buffer layers for the integration of functional oxides for hybrid microelectronic devices. The atomic-level structure of the interface between the epitaxial oxide and semiconductor is vital to the functionality of such heterostructures. This interfacial structure depends on the materials involved and, very importantly, on the details of the deposition process. In this work we have studied the epitaxial interface between epitaxial $SrTiO_3$ films grown on (100) Si. The films were grown by molecular beam epitaxy (MBE). Several different interface bond structures have been reported for $SrTiO_3$/Si, including silicide at the crystalline interface, silicate at the disordering interface, and reduced silicon oxide at both the crystalline and amorphous interfaces. In this work, we report a crystalline silicate bond structure at the interface between epitaxial $SrTiO_3$ and silicon through a combination of high-resolution transmission electron microscopy (HRTEM), x-ray photoelectron spectroscopy (XPS), and theoretical analysis. Both HRTEM and XPS studies show that the interface is well crystallized and free of an amorphous layer. A crystalline Sr-silicate layer is identified from XPS depth profiling, which is different from the disordered silicate structure previously reported at such interfaces. The results show that the Sr-silicate layer has high thermal stability, is lattice matched with silicon, and can be used as an interfacial template for the growth of other epitaxial oxide layers. The effect of rapid thermal annealing on the microstructure and the electrical properties of the $SrTiO_3$/Si heterostructure has also been studied using SIMS, XPS, TEM, and electrical measurements.

9:00 AM *E7.3
Stability of alkaline earth barrier layers during epitaxial growth of (Ba, Sr)O on Si(100). Gerd J Norga[1], Alexandre Guiller[1], Jean Fompeyrine[1], Jean-Pierre Locquet[1], Heinz Siegwart[1], David Halley[1], Christophe Rossel[1], Chiara Marchiori[1,3] and J.W. Seo[2]; [1]Science and Technology, IBM Zurich Research Lab, Rueschlikon, Switzerland; [2]IPMC, EPFL, Lausanne, Switzerland; [3]Laboratorio MDM, INFM, Agrate Brianza, Italy.

High-temperature alkaline earth barrier layers play a crucial role for achieving interfacial SiO2-free epitaxial oxides on silicon (100). The stoichiometry and detailed atomic structure of these barrier layers remains the subject of intensive debate among theoreticians and experimentalists. In this paper, we present a new approach to probe the structure of the interface between the epitaxial oxide layer and silicon. Our method is based on the measurement of phase shifts in the RHEED oscillation signal, collected during epitaxial growth of (Ba, Sr)O on top of the barrier. We demonstrate that these phase shifts are a sensitive measure for the amount of alkaline earth barrier material, which is oxidized and subsequently incorporated in (Ba,Sr)O, grown commensurately on top. Our results suggest that depending upon the temperature of deposition temperature on clean, 2x1 reconstructed Si (100), different Sr surface phases form, with distinct stability against oxidation. Sr deposited at 600C and exposed to O2 at a partial pressure of about 1x10-8 mbar, becomes fully incorporated in the epitaxial (Ba,Sr)O layer grown on top. In contrast, Sr deposited at 750C, after exposure to O2 and subsequent BaSrO growth, remains present as an interfacial phase between Si and (Ba,Sr)O. The observed effect of deposition temperature on barrier stability sheds new light on the detailed structure of the silicon/alkaline earth barrier/epitaxial oxide interface.

10:00 AM E7.4
The Oxides/Semiconductors Interface: Experimental Characterization and Theoretical Calculations. Ach Huan[1,2] and S. J. Wang[1]; [1]Institute of Materials Research & Engineering, Singapore, Singapore; [2]Department of Physics, National University of Singapore, Singapore, Singapore.

The interfaces between oxides and semiconductors are very critical for the application of oxide thin films, including gate dielectrics and ferroelectric transistors. Much research has focussed on understanding and exploiting the properties of novel oxide/semiconductor interfaces to fulfill the stringent requirements for these and other applications. In this work, we will use a combination of characterization tools to determine the nature of the oxide/semiconductor interfaces, including high resolution transmission electron microscopy (HRTEM), X-ray photoelectron spectroscopy (XPS) and secondary ion mass spectroscopy (SIMS), in conjunction with first-principle initio calculations of the interfacial atomic structure. The epitaxial oxide films, Yittrium-stabilized ZrO_2, HfO_2 and Y_2O_3 have been fabricated on silicon and SiGe substrates using pulsed laser deposition technique. The appearance of an amorphous interfacial layer can be controlled by varying the growth process. HRTEM images show atomically sharp interfaces, while several different interfacial bonding structures have been observed between oxide and silicon, including silicide at the crystalline interface, silicate at the ordered or disordered interfaces and silicon oxide at an amorphous interface. The interfacial atomic structures are confirmed by HRTEM image simulation and first-principle calculation with good agreement with experimental and theoretical results. The dynamic growth mechanism of epitaxial oxides on semiconductors and the electrical properties are also discussed in the report.

10:15 AM E7.5
Structural and Dielectric Characterization of Epitaxial Rare-Earth Scandate Thin Films. Juergen Schubert[1], Y. Jia[2], M.D. Biegalski[2], O. Trithaveesak[1], S. Trolier-McKinstry[2] and D.G. Schlom[2]; [1]ISG 1-IT, Forschungszentrum Juelich GmbH, Juelich, Germany; [2]Department of Materials Science and Engineering, Penn State University, University Park, 16802, Pennsylvania.

The rare-earth scandates ($ReScO_3$, where Re is a rare earth element) were recently proposed as candidate materials for the replacement of SiO_2 in silicon MOSFETs in either amorphous or epitaxial form. That rare-earth scandates are promising for this application was based on measurements on single crystals of three different rare-earth scandates: $DyScO_3$, $GdScO_3$, and $SmScO_3$. All showed relatively high dielectric constants (K), high optical band gap energies, and stability in direct contact with silicon. In this work we investigate the dielectric properties and structural perfection of epitaxial $ReScO_3$ thin films, including compositions identical to those whose properties have been studied as single crystals (i.e., $DyScO_3$ and $GdScO_3$) as well as a new composition whose high melting temperature prevented it from being made and studied as a single crystal (i.e., $LaScO_3$ with T_m $\sim$2290°C). The $ReScO_3$ have an orthorhombic crystal structure (space group Pbnm) with lattice parameters fitting nicely to the lattice parameter of Si(100). To verify that the dielectric properties of $ReScO_3$ single crystals apply to epitaxial $ReScO_3$ thin films and to investigate the properties of new rare-earth scandates, we have prepared $GdScO_3$, $DyScO_3$, and $LaScO_3$ epitaxial thin films using pulsed-laser deposition. The films were grown on $SrTiO_3$(100) and $SrTiO_3$(100) covered with an epitaxial $SrRuO_3$ layer (50-100 nm thick) grown ex situ by pulsed-laser deposition as well. The growth temperature ranged from 500°C to 1000°C. The thin film growth was performed at a pressure of $5x10^{-2}$ Torr using a mixture of O_2 and O_3. The typical film thickness was in the 300 nm range. We have characterized the crystal structure of the films using Rutherford Backscattering spectrometry/channelling and four-circle x-ray diffraction measurements. All of the materials showed epitaxial growth on $SrTiO_3$(100). Channelling minimum yield values (χ_{min}) as low as 3% and rocking curve widths as narrow as 0.1° indicate the good

crystalline quality of these epitaxial layers. Electrical measurements were performed to determine the K-values of the different materials in thin film form. For $LaScO_3$ K-values of 26 were obtained.

10:30 AM *E7.6
Epitaxial semiconductor-crystalline oxide heterostructures for microelectronics. Supratik Guha, Ed Preisler, Vijay Narayanan, Nestor Bojarczuk and Huiling Shang; IBM T. J. Watson Research Center, Yorktown Heights, New York.

Projected transistor scaling trends requires one to think about ways of making ultrathin silicon and germanium layers on buried insulators. One way of doing this is via epitaxial growth of crystalline oxides on semiconductors followed by the epitaxy of semiconductors on these oxide surfaces. Compared to the usual semiconductor-on-semiconductor epitaxy that we have been used to over the past 30 years, controlling oxide-semiconductor layers and interfaces is a considerable challenge given that we are trying to bring together materials with quite different valence, ionicities, and bonding. Though microstructurally an oxide on silicon may have seemingly "perfect" registry of atoms across the oxide-semiconductor interface –it is unclear entirely what that buys us since the electrical consequences of such chemically dissimilar interfaces remain. While there has been quite a bit of activity in growing epitaxial oxides on silicon the past decade, the epitaxy of semiconductors on these oxides is a further challenge made difficult by surface energy considerations that drive a Volmer Weber initial growth mode. We will address these issues in reporting on our results on growing epitaxially matched lanthanum yttrium oxide insulating films on silicon and then growing silicon and germanium structures epitxially on top of these oxides.

11:00 AM E7.7
Electrical Characteristics of Metal - $(La_{0.27}Y_{0.73})_2O_3$ - Silicon Capacitors. Edward Preisler, Nestor Bojarczuk and Supratik Guha; IBM T. J. Watson Research Laboratory, Yorktown Heights, New York.

An investigation of metal-insulator-silicon capacitors, utilizing single crystal $(La_{0.27}Y_{0.73})_2O_3$ as the insulator is presented. Crystalline insulators are of interest because of the possibilities of obtaining an atomically flat interface and entirely eliminating the presence of dangling bonds at the interface. Capacitance – voltage measurements performed on MIS capacitors demonstrate a dielectric constant of 15 and suggest the absence of any interfacial silicon oxide layer. The equivalent oxide thickness of the sample with the thinnest dielectric layer is 13.5 Å. The flat-band voltage shift in as-grown samples scales linearly with the insulator thickness, indicating that fixed charge is isolated close to the semiconductor interface, or perhaps that a dipole layer forms at the epitaxial interface between the silicon and the insulator. Interface state densities were found to be in the mid $10^{12}cm^{-2}eV^{-1}$ range and did not vary significantly after post-metallization annealing.

11:15 AM E7.8
Epitaxial and amorphous La2Hf2O7 on silicon for high-k gates. Athanasios Dimoulas[1], George Vellianitis[1], George Apostolopoulos[1], Georgia Mavrou[1], Anastasios Travlos[1], J.C. Hooker[2] and Z.M. Rittersma[2]; [1]NCSR DEMOKRITOS, ATHENS, Greece; [2]Philips Research, Leuven, Belgium.

Ultimate device scaling with equivalent oxide thickness (EOT) below 0.5 nm requires gate dielectrics with permittivity k higher than 20, grown epitaxially on silicon with no interfacial layers. Up to now, perovskite SrTiO3 was the only known oxide with sufficient epitaxial quality on silicon [1]. In this work, we show that other materials like the lattice matched pyrochlore La2Hf2O7 can be grown epitaxially on Silicon with no interfacial layers using atomic oxygen beams from an RF plasma source in an MBE system. At 770 C, this material grows in a cube-on-cube epitaxy mode on silicon such that La2Hf2O7 (001) // Si (001) and La2Hf2O7<110> // Si<110> with clean, commensurate interfaces, although top surface morphology is rough due to the generation of large thermal strain. At lower temperatures around 700 C, the material changes epitaxial orientation such that La2Hf2O7 (111) // Si (001) while at even lower temperatures, the oxide is amorphous with smooth surface morphology. To examine the dielectric properties, we fabricated and tested MIS capacitors with a-La2Hf2O7 of different physical thickness. To take into account quantum confinement and interface trapping effects, we developed a Poisson-Schroedinger solver incorporating Shockley-Hall-Read statistics to describe the exchange of carriers at the interface. From the dependence of EOT on the oxide physical thickness we estimated a permittivity k of 18.1 (+/- 3.25). Record values of EOT~1 nm and gate leakage current density Jg ~ $2x10^{-3}$ A/cm2 @ 1V accumulation were obtained in a sample with a total physical thickness of 3.3 nm and an interfacial layer of 1 nm. Despite the medium k value, the material could be a promising candidate provided that epitaxial films with no interfacial layers and with smooth morphology can be obtained. [1] Mc Kee et al., Phys. Rev. Lett. 81, 3014 (1998).

SESSION E8: Oxide/Compound Semiconductor
Interfaces and Novel Devices
Chairs: Yong Liang and Jasprit Singh
Wednesday Afternoon, December 3, 2003
Room 207 (Hynes)

1:30 PM *E8.1
Interface Passivation for 4H-SiC/SiO_2 Using Sequential Anneals in Nitric Oxide and Hydrogen. John R Williams[1], T. Isaacs-Smith[1], R. M. Lawless[1], C. C. Tin[1], S. Dhar[2], A. Franceschetti[2,4], S. T. Pantelides[2,4], L. C. Feldman[2,4], G. Chung[3] and M. Chisholm[4]; [1]Physics Department, Auburn University, Auburn University, Alabama; [2]Department of Physics and Astronomy, Vanderbilt University, Nashville, Alabama; [3]Dow Corning Corporation, Tampa, Florida; [4]Oak Ridge National Laboratory, Oak Ridge, Tennessee.

Wide band gap, isotropic bulk electron mobility, high thermal conductivity and a native oxide (SiO_2) make the 4H polytype of silicon carbide a promising material for power switching applications. However historically, inversion-mode 4H-SiC MOSFETs have been characterized by lower-than-expected electron channel mobility as the result of a high interface trap density near the SiC conduction band edge. Over the past few years, a number of groups have reported the results of attempts to passivate the 4H-SiC/SiO_2 interface using post-oxidation anneals in various gases such as hydrogen, ammonia, nitric oxide and nitrous oxide. We have demonstrated that anneals in nitric oxide (NO) can be used to reduce the trap density at 0.1-0.2eV below the band edge from well above $10^{13}cm^{-2}eV^{-1}$ to around $10^{12}cm^{-2}eV^{-1}$, with corresponding increases in channel mobility from single digits to 40-50cm^2/V-s. Results using hydrogen have been less dramatic, though theory suggests that hydrogen and nitrogen (from NO) should passivate many of the same interfacial defects - e.g., carbon cluster states, oxygen vacancy states, and silicon and carbon dangling bonds. Herein, we report 4H-SiC/SiO_2 interface state densities following sequential post-oxidation anneals in pure NO and pure hydrogen. Guided by the notion that a cracking mechanism might make hydrogen annealing more effective, we performed hydrogen anneals after sputter deposition of platinum contacts on 30nm dry thermal oxide layers that were grown to make n-MOS capacitors. Interface state densities were measured using Hi-Lo (quasi-static) C-V techniques. Following a standard NO passivation anneal (1atm, 0.5l/min, 1175°C, 2hr), a post-metallization anneal in hydrogen (1atm, 1l/min, 500°C, 1hr) further reduces the trap density from approximately 1.5 x $10^{12}cm^{-2}eV^{-1}$ to about 5 x $10^{11}cm^{-2}eV^{-1}$ at an energy of 0.1eV below the 4H-SiC band edge. Lateral test MOSFETs are currently being fabricated, and the results of mobility measurements following sequential NO and hydrogen anneals will also be reported.

2:00 PM E8.2
Role of polarity on the adhesion and electronic structure of semiconductor/oxide interfaces: GaAs/$SrTiO_3$. Francois Bottin and Fabio Finocchi; Groupe Physique des Solides, Universite Paris 6-7 and CNRS, Paris, France.

Polar orientations represent a special class of surfaces, since each unit cell carries a net dipole moment along the surface normal, which would result in a macroscopic (i.e. thickness dependent) dipole moment across the sample (to be distinguished from the genuine surface dipole). Therefore, the stability of polar orientations can be achieved only through profound changes in the surface electronic structure that compensate the macroscopic dipole. They may imply the anomalous filling of surface states, or non-stoichiometric reconstructions, or the adsorption of charged species [1,2]. In this framework, the adhesion and the electronic properties of ultra-thin films deposited on polar oxide surfaces can be strongly affected by the substrate. As a paradigm, we consider a GaAs monolayer in epitaxy on the non polar (001) and polar (110) surfaces of $SrTiO_3$, through first-principles calculations. The GaAs/$SrTiO_3$ interface shows a quite small misfit and is potentially relevant from a technological point of view, as witnessed by several experimental studies carried out in academic institutions and private companies as well [3,4,5]. First, we determine the thermodynamic conditions needed to obtain sharp GaAs/$SrTiO_3$ contacts, avoiding the formation of Ga- or As- mixed oxides. Then, we simulate many different types of epitaxial configurations for each orientation, determining the most stables ones as a function of the chemical environment. Their electronic structure is carefully analysed through the characterization of the interface states and the electron population [6]. Third, we show that the adsorption energy of GaAs on $SrTiO_3$(110) is systematically higher than for GaAs/$SrTiO_3$(001), which can explain why in the former case good-quality and stable interfaces between Gallium Arsenide and Strontium Titanate can be produced [4]. Moreover, we analyse how

the chemical composition of the outermost $SrTiO_3$(110) layer can influence the growth of thick GaAs sample. [1] C. Noguera, J. Phys.: Condens. Matt. 12, R367 (2000). [2] F.Bottin, F. Finocchi and C. Noguera, Phys.Rev.B 67 (issue of 15 June 2003). [3] Motorola grows GaAs on silicon. Thin Film Manufacturing, Sep. 2001. URL: http://www.thinfilmmfg.com/Noteworthy/Noteworthy01/GaAs20Sept01.htm [4] C. Ping-ping, M. Zhong-lin, L. Wei, C. Wei-ying, L. Zhi-feng, and S. Xue-chu, Chin. J. Lumin. 22, 161 (2001). [5] H. Fujioka, J. Ohta, H. Katada, T.Ikeda, Y. Noguchi, and M. Oshima, J. Crystal Growth 229, 137 (2001); Q.X. Zhao et al., J. Crystal Growth 208, 117 (2000). [6] R.F.W. Bader, Chem. Rev. 91, 893 (1991).

2:15 PM *E8.3
Polar Heterostructures for Tailored Electronic and Optoelectronic Devices. Jasprit Singh, EECS, University of Michigan, Ann Arbor, Michigan.

In conventional semiconductor devices doping and band discontinuities are used to create responses needed for intelligent electronic and optoelectronic devices. This creates several limitations arising from doping fluctuations, inability to dope or fundamental chemistry considerations. In recent years work in the nitride technology has shown that polar heterostructures can allow us to overcome many issues related to heavy doping and offers new ways to cause band bending and band tailoring. There are a large number of potential material systems that have polar character which are not (yet) considered to be relevant to semiconductor technology. These include ferroelectrics, pyroelectrics and piezoelectric materials where polar charges as high as 1 electron per surface atom can be present. Such structures, if successfully integrated with semiconductors can yield novel physical properties with far reaching impact in devices. Polarization differences at interfaces can be used to create very large band bending which in turn can be used to induce electron (hole) gas, create tunnel junctions, cause lateral as well as vertical band engineering. We will examine the electrical and optical response of a few junctions based on material parameters chosen from the ferroelectric family. Applications to ultra shallow ohmic junctions, tunnel junctions, bipolar devices will be discussed. We will also address the level of perfection needed to make polar heterostructures useful. We find that monolayer control will be needed since most useful structures have to be in the range of 5 to 10 monolayers to be beneficial.

3:15 PM *E8.4
Interfacial Engineering for Hetero Integration of Crystalline Perovskite Oxides on GaAs and Si. Yong Liang[1], Jay Curless[1], Joe Kulik[2], Jimmy Yu[1], Ravi Droopad[1], Karen Moore[1] and Yi Wei[1]; [1]Motorola Labs, Tempe, Arizona; [2]PMCL, Motorola, Tempe, Arizona.

Metal oxides possess a wide range of novel electronic, optical, magnetic, and chemical properties that make them uniquely suitable for a number of potential technologies. Integration of crystalline oxides with semiconductors provides an opportunity through which the functional properties of oxides and mature technology of semiconductors can be exploited simultaneously. The challenge of the integration lies in chemical and structural dissimilarities at an oxide/semiconductor interface. In this presentation, we will show that using interfacial engineering, integrated systems with desired properties can be attained. We will first show that using a Ti pre-layer, epitaxial perovskite oxides such as SrTiO3 can be grown on GaAs. The chemical and electronic effects of the Ti layer will be discussed. Initial stages of SrTiO3 growth, band offsets and band bending at SrTiO3/GaAs interface, and interfacial structural properties have been examined by photoemission, RHEED, STM, and TEM, and the results will be presented at the meeting. In addition to GaAs, we will discuss growth of perovskite oxides on Si. We will focus on modification of surface structure and interface energy upon formation of a Sr template layer on Si. Using several surface techniques, we have examined effects of Sr on Si dimer structures and dimer-derived states, and changes of surface electronic structures upon Sr deposition and oxidation. These results provide us insight into role of the Sr template layer on hetero-epitaxy of crystalline SrTiO3 on Si.

3:45 PM *E8.5
The Oxide/Nitride Interface: a study for gate dielectrics and field passivations. Brent P Gila[1], Ben Luo[2], Jihyun Kim[2], Rishabh Mehandru[2], Andrea H Onstine[1], Eric Lambers[1], Kerry Siebein[1], Jeffery LaRoche[2], Cammy R Abernathy[1], Fan Ren[2], Steven J Pearton[1], Neil Moser[3] and Robert Fitch[3]; [1]Materials Science and Engineering, University of Florida, Gainesville, Florida; [2]Chemical Engineering, University of Florida, Gainesville, Florida; [3]Air Force Research Laboratory, Wright-Patterson AFB, Wright-Patterson AFB, Ohio.

Gallium Nitride (GaN) field effect transistors (FETs) have attracted considerable interest as high power electronics for use in the electric utility industry, defense and space applications, and hybrid vehicles. Depletion mode GaN MOSFETs have shown superior high temperature device performance compared to conventional GaN MESFETs. Fabrication of enhancement mode MOSFETs on GaN will require a more complete understanding of the formation of the oxide/nitride interface for further reduction of interfacial traps. By contrast, GaN based HEMT devices are more highly developed and are now being fabricated into preliminary MMIC prototypes. However, one major concern with the GaN HEMT device is the reduction of drain current under high source-drain voltage applications. This phenomenon, known as current collapse, is believed to be due to traps at both the exposed surface and in the underlying GaN buffer. Currently, this problem is greatly reduced by the addition of a dielectric on the top surface of the fabricated HEMT, which acts as a passivation layer to reduce the surface electrical traps. This talk will discuss the effects of substrate surface preparation of GaN, both in-situ and ex-situ and the subsequent gas-source MBE growth of Sc_2O_3 and MgO. Surface preparation techniques have been explored using RHEED, AES, SIMS and C-V measurements to produce films of low interface trap density, 1-2E11 $eV^{-1}cm^{-2}$. A similar study of the as-fabricated HEMT surface was carried out to create a cleaning procedure prior to dielectric passivation. Post-deposition materials characterization included AES, TEM, XRR and XPS, as well as gate pulse and isolation current measurements for the passivated HEMT devices. From this study, the relationship between the interface structure and chemistry and the quality of the oxide/nitride electrical interface has been determined. The resulting process has led to the near elimination of the current collapse phenomenon. In addition, the resulting oxide/nitride interface quality has allowed for the first demonstration of inversion in GaN.

4:15 PM E8.6
Growth of Epitaxial Oxides on GaN. Andrea Hope Onstine[1], B P Gila[1], A Herrero[1], J Kim[2], R Mehandru[2], C R Abernathy[1], F Ren[2] and S J Pearton[1]; [1]Materials Science and Engineering, University of Florida, Gainesville, Florida; [2]Chemical Engineering, University of Florida, Gainesville, Florida.

Fabrication of high performance normally off enhancement mode devices on gallium nitride will require both good interfacial electrical characteristics and good thermal stability. We have previously reported on the use of Sc_2O_3 and MgO as promising gate dielectrics for III-nitride devices. In this talk we will discuss the role of the dielectric microstructure in determining the electronic properties of GaN/oxide diodes and the relationship between growth parameters and microstructure. The best results have been obtained using a hybrid microstructure that is epitaxial at the interface and nanocrystalline in the middle and top of the film as determined by XTEM. This approach has yielded low densities of interface traps, $\sim$1-4x10^{11}eV-1cm-2, as measured by the AC conductance method. Even though the films are initially epitaxial, they possess large numbers of defects due to the large mismatch with GaN. Thus further improvements in interface electrical characteristics will require a reduction in the interfacial mismatch between the oxides and the GaN. In the Sc_2O_3 system this can be accomplished through the addition of small amounts of Mg. XRD of $Sc_xMg_{1-x}O$ films deposited at 100°C. These films show no evidence of phase separation, even after annealing at temperatures up to 1000°C. Electrical and structural characterization of the oxide/GaN interface as a function of oxide composition will also be presented.

4:30 PM E8.7
Structural and Electrical Properties of (111) Oriented $Pb(Zr_{0.3}Ti_{0.7})O_3$ Films on (0001) GaN/Sapphire Substrates. Bhaskar Srinivasan, Wei Cao and Sandwip K Dey; Chemical and Materials Engineering & Electrical Engineering, Arizona State University, Tempe, Arizona.

A ferroelectric oxide-semiconductor heterostructure ($Pb(Zr_{0.3}Ti_{0.7})O_3$ or PZT (30/70))/GaN/Sapphire) has been fabricated, and the nanostructure and nanochemistry, and its properties were characterized. X-ray diffraction and pole figure analysis confirmed a stoichiometric, phase-pure perovskite PZT films with (111) out-of-plane relationship on (0001) GaN. The depth profile analyses indicated a relatively sharp ferroelectric PZT/GaN interface, with insignificant interdiffusion of the Pb, Zr, or Ti elements into the GaN substrate. The metal-ferroelectric-semiconductor (Pt/PZT/doped GaN/Sapphire or MFS) configuration was fabricated, and Al was used as the bottom ohmic contact to carry out the high frequency capacitance-voltage, leakage current, and polarization characteristics. The dielectric permittivity at 100 kHz, estimated from the capacitance value in accumulation, was 200 but which decreased to 45 with decreasing annealing temperature. Additionally, the ferroelectric hysteresis loops were asymmetrical with lower polarization values compared to metal-ferroelectric-metal (Pt-PZT-Ru/GaN/Sapphire or MFM) configuration. However, a well-defined and a nearly square hysteresis loop, with Pr $\sim$ 30 $\mu C/cm^2$ and E_c $\sim$75 kV/cm, was observed for PZT films on

Ru/GaN/Sapphire. The observed electrical properties are discussed in the light of MFS and MFM configurations, and depolarization fields.

4:45 PM E8.8
Growth and Rectifying Electrical Characteristics of $La_{0.7}Sr_{0.3}MnO_3$/ZnO Hetero-structure. Ashutosh Tiwari, S. Ramachandran, C. Jin and J. Narayan; Materials Science & Engineering, North Carolina State University, Raleigh, North Carolina.

We have fabricated a p-n junction, consisting of hole doped (p type) manganite and electron doped (n type) ZnO layers grown on sapphire substrate. These junctions exhibit good electrical rectifying behavior over the temperature range 20-300K. Electrical characteristics of $La_{0.7}Sr_{0.3}MnO_3$ (LSMO) film in this hetero-structure is found to be strongly modified by the built-in electric field of the junction. It has been found that in the case of a 5 nm thin LSMO film, depletion region extends over entire film under the zero biasing condition. By applying the external bias voltage, the thickness of the depletion layer and hence the electrical and magnetic characteristics of LSMO film can be modified. Precise control over the electrical and magnetic characteristics of giant magnetoresistive LSMO films by using the built-in electric field of the LSMO/ZnO junction is an important step in the fast emerging magnetic industry. It also provides an opportunity to integrate various novel magnetic and magnetoelectronic properties of manganites with nonlinear optical and optoelectronics applications of ZnO.

SESSION E9: Joint Session with C9: Gate Dielectrics
and Functional Oxides on Silicon
Chair: Yoshihisa Fujisaki
Thursday Morning, December 4, 2003
Room 207 (Hynes)

8:30 AM *E9.1
Lanthanum Oxide Thin Films For Advanced Gate Dielectrics. Blech Vincent[1], Marie-Christine Hugon[2], Bernard Agius[2], Michel Touzeau[2] and Vincent Le Goascoz[1]; [1]Reseach & Development, STMicroelectronics, Crolles, France; [2]Plasma et Materiaux, LPGP, Orsay, France.

For the past two years, the researches on advanced gate dielectrics have gained considerable attention since the technology roadmaps predict the need of a sub-2nm gate dielectric for sub-0.13μm MOSFET devices in 2002. The thinning of the gate dielectric required by scaling rules, currently between 2 and 2.5nm in fabrication, will give origin to unacceptably high gate current arising from electron tunneling through the SiO_2 films. One possible solution is to use an alternative material to SiO_2 with dielectric constant (K) much higher than 3.9. Due to its high permittivity (K=38), La_2O_3 appears to be a good candidate. La_2O_3 films are deposited on Si substrates by rf magnetron sputtering of a La_2O_3 target in argon atmosphere. Thin film properties are studied as a function of deposition (rf power density, process pressure) and thermal annealing parameters(temperature, time). One of the most important steps in our searching of La_2O_3 film properties is to correlate the physical properties of the material (composition, density) determined by Rutherford Backscattering Spectroscopy (RBS), Nuclear Reaction Analysis (NRA) [$^{16}O(d,p1)^{17}O$ at 850keV] and X-reflectometry to the plasma characteristics investigated by optical diagnostics (Optical Emission and Absorption Spectroscopy). Whatever the deposition conditions, the film composition is O/La=1.3 $\pm$ 0.1 and their density is 7 $\pm$ 0.7g/cm^3 (ρbulk=6.5g/cm^3). We have performed high frequency (1MHz, 100kHz, 1kHz) capacitance-voltage C-V measurements on RuO_2/La_2O_3/Si MIS structure. With the device biased in accumulation regime, a permittivity of 30 was deduced. The C-V curves exhibit well defined accumulation, depletion and inversion regimes which indicate a low interface state density.

9:00 AM E9.2
Liquid Injection MOCVD of Rare-earth Oxides Using New Alkoxide Precursors. Paul Andrew Williams[1], Anthony C Jones[1,2], Helen C Aspinall[2], Jeffrey M Gaskell[2], Paul R Chalker[3], Paul A Marshall[3], John L Roberts[2] and Lesley M Smith[1]; [1]Epichem Limited, Bromborough, Wirral, United Kingdom; [2]Chemistry, University of Liverpool, Liverpool, Merseyside, United Kingdom; [3]Materials Science and Engineering, University of Liverpool, Liverpool, Merseyside, United Kingdom.

Thin films of rare earth oxides such as, La_2O_3, Pr_2O_3, Gd_2O_3 and Nd_2O_3 have potential applications as alternative high-κ gate dielectric layers in silicon-based field effect transistors. MOCVD is an attractive technique for the deposition of these materials, but progress has been restricted due to lack of suitable precursors. There are some reports on the use of metal-β-diketonate precursors, but these often require high growth temperatures and carbon contamination is a potential problem. Although metal alkoxides have been widely used in MOCVD, there have previously been no reports in the literature into the use of rare-earth alkoxide precursors in MOCVD. This is because the large ionic radius of the highly positively charged lanthanide (III) ions leads to the formation of bridging intermolecular metal-oxygen bonds, resulting in many of the simple alkoxide complexes being polymeric or oligomeric, with a corresponding low volatility. However, the sterically hindered donor functionalised alkoxide ligand 1-methoxy-2-methyl-2-propanolate, $OCMe_2CH_2OMe$ [mmp], facilitates the formation of the volatile metal alkoxide complexes [M(mmp)$_3$] (M = La, Pr, Gd etc?). In this paper the synthesis of a number of these new complexes is described together with their use in liquid injection MOCVD.

9:15 AM E9.3
Composition dependence of crystallization in alternative gate oxides. R. Bruce van Dover[1], Martin L Green[2], Lalita Manchanda[3] and Lynn F Schneemeyer[1]; [1]Materials Sci. & Eng, Cornell University, Ithaca, New York; [2]Agere Systems, Allentown, Pennsylvania; [3]SRC, Research Triangle Park, North Carolina.

Thin films comprising group-IV metal oxides are likely candidates for replacing SiO2 in high-performance/low power Si electronics where the effective electrical thickness of the gate oxide must be less than the equivalent of 1.0 nm of SiO2. Elemental oxides such as ZrO2 and HfO2 have dielectric constants that are in the suitable range, $\epsilon \sim$20-30, but crystallize readily under standard process conditions (1000 °C for 5-20 seconds) required to activate ion-implanted dopants. It is known that crystallization can be suppressed by alloying with a main-group oxide such as SiO2 or Al2O3, although these oxides have a much smaller dielectric constant and therefore strongly decrease the dielectric constant of the mixture. We have investigated the post-annealed crystallinity of various mixed transition-metal/main-group oxides using a composition-spread approach. This technique allowed us to determine that the mole fraction of main group oxide in the Zr-Si-O, Zr-Al-O, and Hf-Si-O systems must be greater than 83%, 65%, and 78%, respectively, in order to avoid crystallization. The kinetics of transformation suggest that this conclusion is not sensitive to the anneal time, though it is quite sensitive to the peak temperature. Evaluation of the dielectric constant in the same systems leads us to conclude that the useful dielectric constant is therefore limited to $\epsilon < 6.9$, 12.7, and 6.6, respectively. We conclude that the silicate systems are not likely to be useful as replacements for SiO2, while aluminates are more promising.

9:30 AM E9.4
Epitaxial thick film heterostructures of Pb(Mg1/3Nb2/3)O3-PbTiO3 relaxor ferroelectric films on silicon for high performance electromechanical systems. Dong Min Kim[1], Sang Don Bu[1], Chang Beom Eom[1], Valanoor Nagarajan[2], Jun Ouyang[2], Ramamoorthy Ramesh[2], Venu Vaithyanathan[3], Susan Trolier-Mckinstry[3], Darrell G. Schlom[3], W. Tian[4] and Xiaoqing Pan[4]; [1]Materials Science and Engineering, University of Wisconsin-Madison, Madison, Wisconsin; [2]Materials and Nuclear Engineering, University of Maryland, College Park, Maryland; [3]Materials Science and Engineering, The Pennsylvania State University, University Park, Pennsylvania; [4]Materials Science and Engineering, University of Michigan, Ann Arbor, Michigan.

Pb(Mg1/3Nb2/3)O3-PbTiO3 (PMN-PT) single crystal relaxor ferroelectrics yield significantly higher electromechanical coupling coefficient than conventional polycrystalline ferroelectric materials. A major challenge is to fabricate epitaxial PMN-PT thick films between epitaxial metallic oxides and integrate them into microelectromechanical systems on silicon wafer. We have created epitaxial thin films with the highest longitudinal piezoelectric tensor coefficient ever realized on silicon substrates by (1) using Pb(Mg1/3Nb2/3)-PbTiO3 (PMN-PT), the material which in single crystal form is known for its giant piezoelectric response, (2) using epitaxy to orient it optimally, and (3) nanostructuring it to reduce the constraint imposed by the underlying silicon substrate. When subdivided by focused ion beam processing to reduce mechanical constraints, a 4 μm thick film shows a low-field d33 of 425 pm/V that increases to over 700 pm/V under bias, which is a factor of 4 higher than the highest strain achieved in Pb(Zr,Ti)O3 thin films on silicon. These epitaxial heterostructure can be used for multilayered MEMS devices with high strain and low driving voltage for miniature devices, high frequency ultrasound transducer arrays for medical imaging, tunable dielectrics, and capacitors for charge and energy storage. We will discuss the effect of substrate constraint and thermal strain on the piezoelectric responses in heteroepitaxial PMN-PT thick films on silicon.

9:45 AM E9.5
***c*-axis oriented Epitaxial $BaTiO_3$ Films on (001) Si.** Venugopalan Vaithyanathan[1], James Lettieri[1], Darrell G. Schlom[1],

Jeremy Levy[2], Wei Tian[3] and Xiaoqing Q. Pan[3]; [1]Department of Materials Science and Engineering, Pennsylvania State University, University Park, Pennsylvania; [2]Department of Physics and Astronomy, University of Pittsburgh, Pittsburgh, Pennsylvania; [3]Department of Materials Science and Engineering, University of Michigan, Ann Arbor, Michigan.

We have been investigating the epitaxial growth of *c*-axis oriented $BaTiO_3$ on (001) Si for a novel quantum computing architecture in which an epitaxial ferroelectric film in close proximity to silicon is desired.[1] Silicon is used because of its weak spin-orbit coupling for electrons and relatively long transverse decoherence time. The ferroelectric must be oriented such that its switching results in an electric field effect to confine the electrons laterally in the underlying silicon. The 4.5% lattice mismatch between $BaTiO_3$ and (001) Si at a typical growth temperature of 600 °C, coupled with the much smaller thermal expansion coefficient of silicon than $BaTiO_3$, have until now prevented the growth of *c*-axis oriented epitaxial $BaTiO_3$ films on (001) Si. This large lattice mismatch leads to the rapid relaxation of the lattice constant of the $BaTiO_3$ film to its bulk cubic lattice constant at the elevated growth temperature. As such a relaxed $BaTiO_3$ film is cooled from its growth temperature, it experiences biaxial tension due to the larger thermal expansion coefficient of the $BaTiO_3$ film compared to the silicon substrate. When the film cools through the Curie temperature of the $BaTiO_3$, the *c*-axis of the $BaTiO_3$ aligns in the plane of the substrate (*a*-axis oriented $BaTiO_3$) to reduce the biaxial tension. To achieve the desired *c*-axis oriented epitaxial $BaTiO_3$ film on (001) Si for our application, a buffer layer of relaxed $Ba_xSr_{1-x}TiO_3$ is introduced between the Si and $BaTiO_3$ and the $BaTiO_3$ films are maintained thin enough that they are commensurately strained to the underlying relaxed $Ba_xSr_{1-x}TiO_3$ buffer layer. The films are grown by reactive MBE. *Insitu* characterization of the films by RHEED and *exsitu* characterization by XRD and TEM reveal epitaxial *c*-axis oriented $BaTiO_3$ films with rocking curve widths (FWHM in ω) as narrow as 0.44°. The orientation relationship between film and substrate is $BaTiO_3$ (001) // Si (001) and $BaTiO_3$ [100] // Si [110]. By applying a voltage between a conductive AFM tip and the silicon substrate, domains with up and down polarization have been written in the film at locations specified by the user. Piezo-response AFM has been used to observe the written domains, which have lateral extent down to ~100 nm. [1] J. Levy, Phys. Rev. A **64**, 052306 (2001).

10:30 AM *E9.6
Long Retention Performance of a MFIS Device Achieved by Introducing High-k $Al_2O_3/Si_3N_4/Si$ Buffer Layer.
Yoshihisa Fujisaki[1,2], Kunie Iseki[1] and Hiroshi Ishiwara[1]; [1]Frontier Collaborative Research Center, Tokyo Institute of Technology, Yokohama, Japan; [2]Reaearch and Development Association for Future Electron Devices, Tokyo, Japan.

We introduced high-k Al_2O_3/Si_3N_4 buffer layer in MFIS (Metal-Ferroelectric-Insulator-Semiconductor) devices to realize long retention characteristics and succeeded to achieve a retention time longer than 2×10^6 sec. This long retention character is mainly due to the high insulating property of the buffer layer by reducing the loss of retained charges with minimizing the leakage current. We prepared thin Si_3N_4 (0.9 nm) buffer layer by directly nitridizing Si substrate with atomic nitrogen radicals.[1] The nitridation was carried out at 700 °C. Then we deposited Al_2O_3 thin films on the buffer Si_3N_4 with atomic layer deposition (ALD) technique using $Al(CH_3)_3$ and H_2O precursors.[2] Since the ALD depositions were carried out at low temperature (300 °C), we had to anneal the film to eliminate the defects in the film. The post oxidations were performed at 1000 °C for 30 sec in 5%-O_2/95%-N_2 ambient. On this stacked buffer layer, we deposited 150 nm-thick $Bi_{3.45}La_{0.75}Ti_3O_{12}$ (BLT) ferroelectric films using LSMCD (Liquid Source Misted Chemical Deposition) technique. The BLT film were crystallized at 800 °C in oxygen ambient. The deposited BLT films oriented mainly along the c-axis of BLT crystal lattice normal to the Si substrate. Since our Si_3N_4 buffer layer is highly dense, it prevents the underlying Si substrate from being oxydized during the post oxidation of Al_2O_3 film and the crystallization of BLT film. Therefore, the stacked Al_2O_3/Si_3N_4 buffer layer can preserve high capacitance density and low leakage current even after highly oxidizing thermal treatments.[3] The interface state density between the ALD-Al_2O_3/Radical-Si_3N_4 stacked insulator and a Si substrate is as low as 10^{11} $cm^{-2}eV^{-1}$. The current density less than 10^{-9} A/cm^2 is realized under the 1V bias application using films with the capacitance density of 12fF/μm^2. The memory window larger than 2V was realized in C-V characteristics with ± 6V voltage scan. With this MFIS diode, we found that more than 60% charges are retained for 17 days. This excellent retention character is attributable to the high insulating property of the ALD-Al_2O_3/Radical-Si_3N_4 stacked insulator and also attributable to the perfect elimination of defects at the interfaces in the MFIS structure. This work was done under the auspices of the R&D Projects in Cooperation with Academic Institutions (Next-Generation Ferroelectric Memory), supported by the New Energy and Industrial Technology Development Organization (NEDO), and managed by the R&D Association for Future Electron Devices (FED). Reference 1. Y. Fujisaki and H. Ishiwara, Jpn. J. Appl. Phys. **39**, L1075 (2000). 2. A. Paranjpe. S. Gopinath, T. Omstead and R. Bubber, J. Electrochem. Soc. **148**(**9**), G465-G471(2001). 3. Y. Fujisaki, K. Iseki ,H. Ishiwara, M. Mao and R. Bubber, Appl. Phys. Lett. **82**, 3931 (2003).

11:00 AM E9.7
Investigation of Retention Properties for $YMnO_3$ Based Metal/Ferroelectric/Insulator/Semiconductor Capacitors.
Takeshi Yoshimura, Daisuke Ito, Hironori Sakata, Norimiti Shigemitsu, Kohei Haratake and Norifumi Fujimura; Graduate School of Engineering, Department of Applied Materials Science, Osaka Prefecture University, Sakai, Osaka, Japan.

Ferroelectric gate field-effect transistors (FETs) have been investigated for the applications to nonvolatile memory devices due to the nondestructive read operation and the advantages of decreasing memory cell size. Because of the difficulty to obtain the excellent ferroelectric-semiconductor interface, ferroelectric gate FETs with a metal-ferroelectric(-metal)-insulator-semiconductor (MF(M)IS) structure have been widely studied. We have investigated $YMnO_3$ films for MFIS type ferroelectric gate FET, because YMnO3 has suitable properties for this application such as small spontaneous polarization and low permittivity. We have succeeded in fabricating $YMnO_3$ epitaxial films with $2P_r$ of 3.4 $\mu C/cm^2$ on (111)Pt/sapphire substrates and epitaxially grown (0001)$YMnO_3$/(111)Y_2O_3/(111)Si capacitors with ferroelectric type C-V hysteresis loops. In this study, the degradation mechanism of memory retention for $Pt/YMnO_3/Y_2O_3/Si$ capacitors are discussed using the leakage current analysis and the pseudo isothermal capacitance transient spectrum (pseudo ICTS) and others. Although the retention time of as-deposited capacitors was 10^3 s, it was prolonged up to 10^4 s when the leakage current density was reduced from 4×10^{-8} A/cm^2 to 2×10^{-9} A/cm^2 by the annealing under N_2 ambience. For the leakage current of the $Pt/YMnO_3/Y_2O_3/Si$ capacitors, it was revealed that Schottky emission was dominant at memory retention state however Poole-Frenkel emission occurred when high voltage was applied. Since the activation energy of the Poole-Frenkel emission of the $Pt/YMnO_3/Y_2O_3/Si$ capacitors agreed with that of $Pt/YMnO_3/Pt$ capacitors, the origin of the Poole-Frenkel emission existed in the $YMnO_3$ layer. It was also found that applied voltage with unnecessarily long time to polarize the ferroelectric layer generated Poole-Frenkel defects in the ferroelectric layer and that the amount of the defects greatly affected the memory retention time. These results suggest that Poole-Frenkel defects work as trap sites of the charge and that the charge injection to the Poole-Frenkel defects occurs gradually until it neutralizes the remanent polarization of the $Pt/YMnO_3/Y_2O_3/Si$ capacitors.

11:15 AM E9.8
Characterization of Metal-Ferroelectric-Metal-Insulator-Semiconductor (MFMIS) FETs using $(Sr,Sm)_{0.8}Bi_{2.2}Ta_2O_9$ (SSBT) Thin Films.
Hirokazu Saiki[1] and Eisuke Tokumitsu[1,2]; [1]Precision & Intelligence Laboratory, Tokyo Institute of Technology, Yokohama, Kanagawa, Japan; [2]RIEC, IT-21, Tohoku University, Sendai, Miyagi, Japan.

Metal-ferroelectric-metal-insulator-semiconductor (MFMIS) structure has attracted considerable attention for ferroelectric-gate transistor applications. MFMIS structure has a merit that one can design the area of an MFM capacitor (S_F) and that of an MIS diode (S_I) independently. To match the ferroelectric polarization with the charge of FET channel, a large area ratio (S_I/S_F) is usually used in MFMIS-FETs. However, $S_I/S_{F=1}$ is desirable for large-scale integration. We previously reported that $Sr_{0.8-1.5x}Sm_xBi_{2.2}Ta_2O_9$ (SSBT) thin film has small remanent polarization and large coercive field, which are suitable for MFMIS structures. In this work, we have fabricated and characterized $Pt/Sr_{0.5}Sm_{0.2}Bi_{2.2}Ta_2O_9$(SSBT)/Pt/Ti/$SiO_2$/p-Si MFMIS-FET (W/L=50/5μm). The crystallization of SSBT was done in O$_2$ ambient at 850°C. The thickness of SSBT and SiO_2 is 130nm and 10nm, respectively. A memory window of about 2V was obtained with an applied gate voltage of ±5V from drain current-gate voltage (I_D-V_G) characteristic of MFMIS-FET even with S_I/S_F=1. This value of memory window agrees with the product of coercive field and thickness of SSBT films. This indicates that the saturated hysteresis loop of SSBT is available even if the MFM capacitor and the MIS diode have same area. This work was supported by a Grant-in-Aid for Scientific Research (No.14040208, No.14655117, and No.15360157) from the Ministry of Education, Science, Sports, and Culture. This work was performed under the auspices of the R&D Projects in Cooperation with Academic Institutions (Next-Generation Ferroelectric Memory), supported by NEDO and managed by FED.

11:30 AM E9.9
Selective Deposition Of C-Axis Oriented $Pb_5Ge_3O_{11}$ On Patterned Hi-K Gate Oxide By MOCVD Processes.
Tingkai Li, Bruce Ulrich, Dave Evans and Sheng Teng Hsu; PTL, Sharp Labs. of America, Inc., Camas, Washington.

MFIS (Metal/Ferroelectrics/Insulator/Silicon) transistor ferroelectric memory devices have been fabricated. C-axis oriented $Pb_5Ge_3O_{11}$ (PGO) thin films showed very good ferroelectric and electrical properties for 1T-memory device applications. Extremely high c-axis oriented PGO thin films can be deposited on high k gate oxide, and functional 1T-memory devices with PGO MFIS memory cell have been fabricated. The integration process-induces damage such as etching damage that degrades the properties of FRAM devices and high surface roughness resulted in difficulty for alignment. In order to solve this problem, selective deposition processes have been developed to simplify integration processes and improve the properties of MFIS transistor ferroelectric memory devices. Based on different deposition rates of ferroelectric materials on high-k oxide and silicon dioxide, we selective deposited a c-axis oriented PGO film on patterned high-k oxide such as ZrO_x (x=0-2), HfO_x (x=0-2), TiO_2, etc. and their mixtures other than on SiO_2. By patterning the high-k dielectric, the PGO deposition is limited to just the preferred pattern area. SEM, EDX and x-ray measurements further confirmed that c-axis oriented PGO thin films selectively deposited on high-k gate oxide other than on field SiO_2. Sometimes during annealing of the PGO, staining of the field oxide occurs. This can be eliminated by not depositing PGO in the field area. The morphology of the PGO film can be very rough which can cause subsequent alignments to be very difficult if not impossible. Again by confining the PGO deposition to just the patterned area will also eliminate the roughness problem for alignments. Also etching damage is eliminated since there is no need to etch the PGO film, which improved the properties of FeRAM devices.