SYMPOSIUM D

Materials and Processes for Nonvolatile Memories

November 30 - December 2, 2004

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* Invited paper

SESSION D1: Nonvolatile Memories with Discrete Storage Nodes
Chairs: Alain Claverie and Tsu-Jae King
Tuesday Morning, November 30, 2004
Back Bay B (Sheraton)

8:30 AM *D1.1
Future Direction of Non-Volatile Memory Technologies.
Albert Fazio, Intel Corporation, Santa Clara, California.

This paper reviews the future direction of nonvolatile memory technologies. Moore's law will continue to drive transistor based memory technology scaling but technology complexity will be increasing. New memory concepts, not relying on transistors as a basis of the memory cell, provide new opportunities for future low cost memories. Several of these new concepts will be summarized and contrasted with the mainstream transistor based flash memory technologies. However, the task of introducing any new memory technology is very large. History has shown us that even successful new memory approaches take several years in research labs prior to attaining viable initial products and then several generations further are required for manufacturing learning on the new approach before it can displace the established incumbent in the marketplace, for cost, performance and scalability. It is therefore expected that for many years to come, the majority of the nonvolatile memories shipped will be based on current mainstream flash technologies, which utilize transistor based charge storage memory cells and multi-level-cell concepts, for storing more than one logic bit in a single physical cell. In order to meet technology scaling, the mainstream transistor based flash technologies will start evolving to incorporate material and structural innovations. Dielectric scaling in non-volatile memories is approaching the point where new approaches will be required to meet the scaling requirements, while simultaneously meeting the reliability and performance requirements of future products. For both the tunnel oxide and the inter poly dielectric (IPD), high k materials are being explored as possible candidates to replace the traditional SiO2 and ONO (Oxide/Nitride/Oxide) films used today. The unique requirements of non-volatile memories dictate unique high-K material solutions from those being explored for traditional CMOS logic transistor scaling. Likewise, planar based memory cell scaling is approaching the point where physical space constraints force exploration of new materials and non-planar, 3D, scaling alternatives. Flash memory has historically utilized some 3D aspects, such as 3D wrapping of the floating gate for improved capacitive coupling. Both physical space limitations and transistor based electrical limitations, in the planar dimension, drive the need for more complex 3D scaling in the future. This paper will review the current status and discuss the approaches being explored to provide scaling solutions for future transistor based non-volatile memory products. Based on the introduction of material innovations, it is expected that the planar transistor based flash memory cell can scale into the 32nm node. Further, more complex, structural innovations will be required to maintain further scaling.

9:00 AM *D1.2
Non-Volatile Memory Technology: Floating Gate Cell Concept Evolution. Cesare Clementi and Roberto Bez; CRD, ST Microelectronics, Agrate Brianza, Italy.

In the recent years the NVM market has experienced a fast growth thanks to the Flash memory technology, particularly suitable for mobile applications. It is expected that in the next future portable systems will ask even more NVM both with high density and very high writing throughput for data storage applications, and with fast random access time for code execution in place. Nowadays two types of Flash architectures are considered as the industry standard: the common ground NOR, which is addressing both the code and data storage segments due to its versatility, and the NAND, optimized for the data storage market. Both of them are stacked gate cells, based on the concept of floating-gate (FG). Considering the evolution of the Flash, the technology scaling is one of the most important requirements that must be fulfilled to satisfy the strong market demand for low-cost memories. Till now the Flash scaling and the FG concept demonstrated to be really possible and to succeed in following the Moore's law down to the 90nm technology node. The Flash technology is considered solid enough to sustain in the next few years the scaling down to the 65nm node. The further scaling to and beyond the 45nm node will face instead new issues, mainly related to the cell gate channel length and to the tunnel oxide thickness, which could affect the cell functionality and reliability. Hence the possibility to extend further the FG cell concept is strictly based on the opportunity to introduce new material and integration solutions. They must be able to solve the problems related to the active (W and L of the cell) and to the passive (FG-FG, active-active distance) elements of the cell. For example high-k material could be fundamental to reduce the gate L either as composite dielectric for tunneling (crested barrier) or as inter-gate dielectric for coupling. Other materials, like W or NiSi2, can be crucial to obtain a thin control gate with a low resistivity. Another possibility for the scaling path consists in substituting into the Flash structure the FG with discrete traps, formed by nano-crystals. Different techniques were suggested to obtain a uniform layer of nanocrystals compatible with the Flash process. This approach is anyway still under development. The problem of the integration of new materials into a Si-based process is common to all the emerging technologies. FeRAM, MRAM or PCM are all trying to introduce in the basic CMOS process new materials, like perovskites, magnetic or chalcogenide to overcome the limits of the FG structure. All of them are anyway facing the issue of the compatibility with the standard elements of a manufacturable process. The maturity of these technologies is still low and the pace of their learning curve is fundamental to carry on the fight with the scaling of the floating-gate cell, which will remain the reference technology till the end of this decade.

9:30 AM D1.3
Lateral Distribution of Electrons Trapped in Nitride Layers.
Martino Lorenzini[1], Maarten Rosmeulen[1,2], Laurent Breuil[1], Luc Haspeslagh[1], Jan Van Houdt[1] and Kristin De Meyer[1,2]; [1]IMEC, Leuven, Belgium; [2]Katholieke Universiteit Leuven, Leuven, Belgium.

Recently, nitride-based trapping storage non-volatile memory concepts have received an increasing interest due to their smaller cell size, simpler fabrication process and double density. In these devices, the two-bit storage capability is achieved by storing the charge locally in the nitride layer in the vicinity of the source/drain junctions. A reverse read scheme allows for the detection of each single bit, provided the charge distributions are sufficiently spaced apart. Therefore, the characterization of the lateral distribution of the trapped charge is fundamental in understanding the scalability and retention properties of these concepts. In this work, the amplitude-sweep charge-pumping technique is applied to a) the investigation of the electron distribution in the nitride under different injecting conditions and b) to the analysis of the charge redistribution at high temperature. The lateral charge profile above the channel region is directly extracted from the measurements using a deconvolution-based procedure. The devices investigated consisted of a conventional n-channel MOSFET, manufactured using a 0.13 μm fabrication technology, which incorporates an oxide-nitride-oxide dielectric stack, consisting of a 7 nm thick thermally grown bottom oxide, a 10 nm nitride layer and a 8nm thick deposited blocking oxide. Drawn gate lengths ranging from 0.18 μm to 0.45 μm have been considered, with effective channel lengths about 50 nm shorter. To investigate the effect of different injecting conditions, virgin samples have been programmed by channel-hot-electron injection changing the amplitude and width of the gate pulse. Deviations from a steep rising edge shape of the charge-pumping signal are clearly sensed, which are indicative of localized trapped charge. Also, only a marginal increase in the maximum charge-pumping current has been observed, indicating little to no creation of additional interface states. The trapped charge has been found confined in about 60 nm in the vicinity of the drain junction, while the peak of the distribution as well as its width increases with increasing programming pulse height and width. Electrons can diffuse from the initial trapping locations under the influence of the concentration gradient and internal electric field. While no significant redistribution has been detected at room temperature over a period of a few weeks, a high-temperature bake enhances the lateral spread of the electron distribution. As the shape of the charge distribution changes, the charge-pumping signal modifies accordingly its rising edge. In principle, electrons can also leak away through the bottom or top oxide. However, their number, obtained by integration of the lateral distribution over the channel area, has been found practically constant during bakes up to 250°C, so that the sensed threshold voltage shifts appear to be solely determined by the lateral redistribution of the electrons in the nitride.

9:45 AM D1.4
Back-side Storage Non-Volatile Memories: Ultra-thin Silicon Single Crystal Silicon Layers with Complex Thin Film Structure Underneath. Helena Silva and Sandip Tiwari; School of Applied and Engineering Physics, Cornell University, Ithaca, New York.

A new geometry for scaled silicon non-volatile memories that makes use of back-side trapping, and can be simultaneously operated as a scaled transistor, has been demonstrated to be a viable device for the 10's of nm dimensions [1]. Unlike the conventional silicon non-volatile structures, where charge is stored between the silicon channel and the gate, in back-side trapping memories charge is stored underneath the transistor channel. The decoupling of the transistor function (front) from the memory function (back) gives this device its unique advantage in scalability and ability to operate simultaneously as a transistor and memory. However, a complex substrate that incorporates a trapping layer underneath a thin single-crystal silicon layer provides an interesting materials challenge. In our effort, the trapping layer is an oxide-nitride-oxide (ONO) stack. Charge is moved

between the ONO defects and the back silicon interface through a thin tunneling oxide by either hot-carrier injection or Fowler-Nordheim tunneling. Leakage of charges to the substrate (or back-gate) is minimized by the use of a thicker control oxide between the nitride and the substrate. We have developed a modified 'smart-cut' process to achieve the intended substrate: a thin single crystal silicon layer (10-15 nm) separated from the silicon wafer substrate by an ONO stack. The bonding interface in our process is in the control oxide layer. Different energies and hydrogen doses and their effects both on the bonding and exfoliation processes and in the final film quality have been studied, including the damage caused in the silicon layer by the hydrogen implantation. In SOI devices where the buried dielectric layer is of the order of a few hundreds of nanometers, the quality of the bonding interface may not be critical. However, in back-side trapping memories, which make use of the buried dielectric layers as active parts of the device (tunneling oxide, trapping layer and control oxide), and where, in order to achieve practical writing and erasing voltages, the total buried stack does not exceed 20 nm, the quality of the bonding interface is very important. Electrical characterization of fabricated devices shows no effects of an eventual defected region due to the fabrication process, when compared to front-side storage devices. Retention time and write-erase cycling endurance results are also similar to those in front-side memories showing that no significant additional leakage paths are introduced by the bonding process. In summary, we have developed a reliable and convenient fabrication process for back-side ONO storage memories. This modified 'smart-cut' process can in principle be used with other trapping materials as well, for memories or other devices that may employ multi-layer stacks underneath a single-crystal silicon layer. [1] H. Silva and S. Tiwari, "A nano-scale memory and transistor based on back-side trapping", Transactions. on Nanotechnology, 3, 2 (2004).

10:30 AM *D1.5
Integration and Performance Improvements of Silicon Nanocrystal Memories. Toshiro Hiramoto, Il-Gweon Kim, Masumi Saitoh and Kosuke Yanagidaira; Institute of Industrial Science, University of Tokyo, Tokyo, Japan.

Silicon nanocrystal memories are very promising for future non-volatile, high-density memory that can replace conventional floating gate memories. Although many research works have been reported previously on silicon nanocrystal memory, much more improvements of integration level, performance, and reliability will be achieved by proper optimizations of process and device structures. In this presentation, we will report (1) full process integration of silicon nanocrystal memory cells using advanced memory technology and (2) performance improvements of memory characteristics using ultra-small nano-scale SOI channel. Silicon nanocrystal memory cells with 4.6 F^2 cell size on NOR type are successfully integrated. The cell size is 0.077 μm^2 using the 130 nm memory technology. This small cell size is achieved by the self-aligned contact process using landing plug polysilicon contact and direct tungsten bitline. Successful two-bit-per-cell operation is also achieved by local hot carrier injection into source and drain sides, that results in distinct four states with different threshold voltages. The reliability issues are significantly improved by properly fluorinated effect during the process. We have also investigated the dependence of memory characteristics on SOI channel structures and channel size. Silicon nanocrystal memories with ultra-narrow channel, double-gate SOI channel, and single-gate ultra-thin body SOI channel are fabricated. In the ultra-narrow channel devices, the channel width is varied from several microns down to 5 nm. In the double-gate and single-gate devices, the channel thickness is varied down to 4 nm. It is found that the threshold voltage shift, writing speed, and retention time are drastically improved when the SOI channel size (channel width in ultra-narrow devices and channel thickness in double/single-gate devices) becomes smaller. These results confirm that the silicon nanocrystal memories are scalable and promising for high-density memories.

11:00 AM D1.6
Optimisation and Simulation of an Alternative Nano-flash Memory: The SASEM Device. Christophe Krzeminski[1], Emmanuel Dubois[1], Xiaohui Tang[2], Nicolas Reckinger[2], Andre Crahay[2] and Vincent Bayot[2]; [1]ISEN, IEMN, Villeneuve d'ascq, France; [2]DICE, Universite Catholique de Louvain, Louvain-la-Neuve, Belgium.

Since the conventional floating gate device is believed to be hardly scalable below the 65-nm technology node, alternative storage structures for nonvolatile memories are strongly needed. The feasibility to make a silicon-on-insulator nano flash memory device based on the differential oxidation rate resulting from gradients in the arsenic doping concentration has previously been reported. The key processes involved in the fabrication are arsenic implantation, lithography and wet oxidation. The resulting device is a triangular MOSFET with a nanocrystal floating gate embedded in the gate oxide. Our objective is now to improve the reliability of the process and to ensure the presence of the memory dot for various conditions. Furthermore, a clear understanding of the dot formation mechanisms and of the influence of self-limited oxidation effects on the final device should be undertaken. We investigate the wet oxidation step in details using the generalised stress-dependent Deal and Grove approach. The various geometrical parameters (e.g dot surface, dot-channel distance ...) of the nano-device have been simulated as a function of the oxidation temperature and the duration of this oxidation step. The time of oxidation is critical for the process reliability. We have shown that the dot shape and size is reduced by increasing the oxidation temperature. Furthermore, the temperature controls the difference between the time of oxidation necessary to create the dot and the time to consume it totally. Low temperature oxidation is then recommended in order to keep a reliable process. In a second part, we study the influence of the nanowire width and shape on the final device, all the other process parameters (dose, oxidation temperature, time) being kept constant. Simulations show that the choice of the linewidth for the central region is of upmost importance. We clearly confirm the experimental results showing the existence of two critical line widths that determine the creation or the consumption of the dot. In the linewidth range where the dot is created, the dot geometry changes and the dot radius is shown to linearly scale down. This results means that the properties of the SASEM device could be changed by a small variation in the central region. Finally, we study the influence of the shape of the nanowire before the oxidation step. Due to the high arsenic dose, overetching effects occur in the region of interest through electrostatic influence. This effect is beneficial for the assumed dimension in the central region (around 120 nm) and the dot is more easily separated in this case. However for lower dimensions of the SASEM device, this effect might be more problematic. To conclude, we stress that the optimisation of the arsenic dose is of crucial interest to study the downscaling. The simulation of the scaling issues and the impact on the various process parameters are the next priorities.

11:15 AM D1.7
Formation of Ni Nanocrystals Embedded in HfO_2 and SiO_2 and Process Integration for Application in Nonvolatile Memories. Zerlinda Y. L. Tan, S. K. Kumar Samanta, Won Jong Yoo and Sungjoo Lee; Electrical and Computer Engineering, National University of Singapore, Singapore, Singapore.

Flash memory using nanocrystals (NCs) as floating gate has received considerable attention because of its excellent electrical performance. Ni, despite its high work function (4.9eV), high density of state and increasing popularity in CMOS processes has not been studied for non-volatile memory applications. For higher programming efficiency and reduced charge loss, physically thick high-k materials with lower tunneling barriers have been proposed as an attractive alternative to conventional SiO_2. In this work, Ni nanocrystals were successfully formed on HfO_2 deposited by chemical vapor deposition and thermally grown SiO_2 using sputtering and rapid thermal anneal. Uniform and well separated Ni-NCs formed on both SiO_2 and HfO_2 were observed from Scanning electron microscopy (SEM) and auger electron spectroscopy (AES). We found that the size and density of Ni-NCs on SiO_2 and HfO_2 can be controlled by the initial film thickness and annealing temperature. The size of the Ni-NCs is reduced as the initial film thickness is reduced. The smallest NC size (10nm) and highest NC density ($2x10^{11}cm^{-2}$) was achieved at 600°C with 5nm initial thickness. At higher temperatures, NC/s size is increased and density is reduced. During annealing, the elastic energy carried by the stress in the thin Ni film is relieved causing the film to rupture into islands on the dielectric surface. The dewetting of thin Ni films may also be attributed to the reactivity of the metal absorbates to the oxygen in the substrate. The weaker bond enthalpy of Ni-O (382 $kJmol^{-1}$) compared to Hf-O (802 $kJmol^{-1}$) and Si-O (799 $kJmol^{-1}$), not only drives the three dimensional agglomeration of the Ni-NCs but also helps to ensure the chemical stability of Ni on HfO_2 and SiO_2. However, analysis of Ni-NCs mass loss on HfO_2 by AFM and X-ray photoelectron spectroscopy (XPS) shows that Ni can diffuse into HfO_2 after anneal. This is detrimental to the device performance. By annealing in NH_3 ambient for dot formation, XPS analysis shows that the nitrogen content in HfO_2 is increased and the mass loss of Ni-NCs is reduced, implying that Hf-N bond can block Ni diffusion in HfO_2 effectively. Nonvolatile memory devices using Ni-NC floating gate embedded in SiO_2 or HfO_2 were fabricated on p-type silicon substrates with 6nm tunnel oxide and 12nm control oxide. With HfO_2 tunneling oxide, a 1V memory window was obtained with a 5V CV sweep compared to the control sample without Ni-NCs. Devices with Ni-NCs embedded in SiO_2, however, required a 10-12V CV sweep to achieve the same memory window. This is due to the lower tunneling barrier of HfO_2 (1.5eV) compared to SiO_2 (3.5eV) and improved coupling of the Ni-NCs to the channel due to the lower effective oxide thickness of HfO_2 (1.3nm) compared to SiO_2 (6nm). These results demonstrate the successful integration of Ni-NCs for nonvolatile memory application.

11:30 AM D1.8
Influence of Thermal Treatments on the Chemistry and Self-Assembly of Ge Nanoparticles on SiO_2 Surfaces.
Scott K. Stanley, Shawn S. Coffee and John G. Ekerdt; Department of Chemical Engineering, The University of Texas at Austin, Austin, Texas.

Germanium and SiO_2 interactions are important to a host of next generation electronics devices such as single electron transistors, optical waveguides, and flash memories. For flash memory devices, germanium particles on insulator substrates are now being extensively studied as the charge storage elements because of higher carrier mobility and lower band edge when compared to Si particles. Many reports on the oxidation of Ge substrates and $Si_{1-x}Ge_x$ films have been published in the literature but remarkably few studies have been made on the interactions of Ge atoms or Ge films with insulator surfaces. In this work, a hot filament is used to thermally crack GeH_4 and deposit 0.5-20 ML Ge onto SiO_2 substrates. The substrates are 2.0-9.0 nm tunnel quality SiO_2/Si(100) which are held at temperatures of 300-970 K during deposition. Ge, GeO, and GeO_2 desorptions are studied through temperature programmed desorption (TPD) experiments at 300-1100 K. Ge desorption spectra are complex exhibiting multiple desorption features. Low temperature features are attributed to GeO. No GeO_2 desorption features are observed. GeO formation results from Ge etching of the substrate as evidenced by monitoring the X-ray photoelectron spectroscopy (XPS) Si 2p peak area during exposure to a beam of Ge atoms with substrate temperatures above the Ge desorption peaks identified through TPD experiments. Guided by TPD peak temperatures, Ge bonding changes are also studied during annealing sets with XPS. These results explain why Ge nanoparticle growth is not observed after conventional low pressure chemical vapor deposition (LPCVD) on oxide substrates. Methods to modify the conventional LPCVD process and allow deposition of Ge on oxide substrates are discussed. Our findings could also be helpful when considering a number of other studies involving agglomeration of $Si_{1-x}Ge_x$ films on oxide materials.

11:45 AM D1.9
Low Voltage and High Speed Silicon Nanocrystal Memories.
Josep Carreras, B. Garrido, J. Arbiol and J. R. Morante; Electronics, University of Barcelona, Barcelona, Barcelona, Spain.

Si nanocrystals (Si-nc) used as charge storage nodes have demonstrated potential for both high speed and non-volatile memory applications. We have studied a set of MOS structures ion-implanted with Si at high doses (10, 15 and 20 atomic %) at projected range (25 nm) in which Si-nc has been precipitated by annealing at 1100 °C. The structural information of the device has been obtained by EFTEM, revealing the presence of a central layer of Si-nc, distributed with a mean size of about 2.85 ± 0.20 nm, a control oxide completely free of Si-nc of 12.5 nm, and a tunnel oxide of about 2.5 nm. This small tunnel oxide distance enables the direct tunnel mechanism, which is desired for high speed applications and reliability considerations, but also causes the stored charge to back-tunnel to the p-type substrate even for zero gate bias condition, resulting in typical retention times ranging from few hours up to several months, depending on the concentration of Si-nc (Si excess). For developing low voltage memories we have focused on the highest Si excess sample, which shows fast write times (tens of microsecons) at very low gate fields (±2 MV/cm or ±6V). The onset of Fowler-Nordheim conduction has been estimated to be about ±6 MV/cm by J-V measurements, which means that the structure works in a direct tunnel regime, which is a must for reliable devices (no hot electrons). In order to increase the retention time, which diminish upon increasing the concentration of Si-nc (increasing Si excess) we have realized an additional annealing step in O_2 ambient for 16 and 32 minutes, resulting in a dramatic increase in the retention times, which is attributed to the growth of a high quality thin (1 and 1.7 nm respectively) tunnel oxide totally free of nanocrystals or Si clusters, Si excess and defects at the Si-SiO_2 interface. This additional oxidation step produces a decrease in the mean size of the Si-nc distribution. The increase of the average distance between the nanocrystals and the Si substrate leads to a decrease of the tunneling current, which depends strongly on the thickness of the tunnel oxide. Thus, we can increase the retention time beyond the 10 years limit (in compliance with the current non-volatility standards) without compromising too much the writing times, as can be traded-off by increasing slightly the program voltage up to ±2.7 MV/cm or ±8V. In summary, we have demonstrated a Si-nc MOS cell, suitable for applications in which high speed and low voltages are specially required, with retention characteristics optimized to comply with the non-volatility standard definition.

SESSION D2: Ferroelectric Memories
Chairs: Hongsik Jeong and Tsu-Jae King
Tuesday Afternoon, November 30, 2004
Back Bay B (Sheraton)

1:30 PM *D2.1
Ferroelectric Thin Film Depositions for Various Types of FeRAMs (Ferroelectric Random Access Memories).
Yoshihisa Fujisaki[1] and Hiroshi Ishiwara[2]; [1]Central research Lab., Hitachi Ltd, Kokubunji, Japan; [2]Interdisciplinary Graduate School of Science and Technology, Tokyo Institute of Technology, Tokyo, Japan.

Nonvolatile ferroelectric random access memories (FeRAMs) have received great attention in recent years because their writing speeds are much higher than those of Flash memories and their power consumption is much lower than those of other non-volatile memories.1, 2) LSIs as large as 64Mb have already been demonstrated and memories with Mb scale integration are now in production. These devices have the cell structure composed of one ferroelectric capacitor and one transistor that is similar to the DRAM cells. Hereafter, we call this structure as 1T1C type. For this structure, ferroelectric materials with large remnant polarizations such as PZT ((Pb, Zr)TiO3) and BLT ((Bi, La)4Ti3O12) are suitable. Another important structure for the nonvolatile FeRAM is the ferroelectric gate transistor. In this memory, one cell is composed of only one transistor with ferroelectric gate insulator. This device is then called 1T type memory. Therefore, it is vary suitable for the large-scale integration and the low-power and high-speed operation. Memories with this structure are now under development, but recently great improvements have been reported.3) Materials suitable for this structure should have relatively small remnant polarization and small coercive field. SBT (SrBi2Ta2O9) is thought to be the primary candidate for this device. We review the recent development of the film deposition techniques both for 1T1C and 1T types. We expect that the requirements for the low voltage operation is crucial for the 1T1C type devices and we have to replace the present PZT or BLT with the material having lower coercive fields. We proposed a new deposition technique to realize both high remnant polarization and low coercive fields for the BLT base material. The ferroelectric performance obtained with this new deposition process satisfies the requirements for Gb scale integration.4) As for the 1T type devices, items related to the film orientation control and the reduction of the film synthesis temperature should become the key factor to realize this type of memories. We investigated the mechanism how to align the ferroelectric crystal axis on amorphous buffer films. By controlling the initial nuclei of the film growth, we succeeded to make the films with almost 100% oriented to the specific crystal axis. Finally, we will summarize the process technologies required for the future FeRAMs. References 1) J. F. Scott and C. A. Paz de Araujo, Science 246 (1989) 1400. 2) C. A. Pas De Araujo, J. D. Cuchiaro, L. D. McMillan, M. C. Scott and J. F. Scott, Nature (London) 374 (1995) 627. 3) Y. Fujisaki, K. Iseki and H. Ishiwara, Mat. Res. Soc. Symp. Proc. 786 (2004) E9.6.1. 4) Y. Fujisaki, K. Iseki and H. Ishiwara, Jpn. J. Appl. Phys. 42 (2003) L267.

2:00 PM D2.2
Step Coverage and Composition of $Pb(Zr,Ti)O_3$ Capacitors Prepared on Sub-Micron Three-Dimensional Trench Structure by Metalorganic Chemical Vapor Deposition.
Atsushi Nagai[1], Gouji Asano[1], Jun Minamidate[1], Chel Jong Choi[2], Choong-Rae Cho[2], Youngsoo Park[2] and Hiroshi Funakubo[1]; [1]Tokyo Institute of Technology, Yokohama, Japan; [2]Samsung Advanced Institute of Technology, Yongin-Si, South Korea.

For high-density integration of ferroelectric random access memory (FeRAM), three-dimensional (3-D) capacitor structures should be realized. Metalorganic chemical vapor deposition (MOCVD) is one of the most suitable techniques for conformal deposition of the films on the 3-D structures. There have been numerous reports on MOCVD films for FeRAM application. However, not much work of MOCVD study has been reported on the sub-micron trench structures, which are widely accepted as the most feasible structures for high density FeRAM. In the present study, $Pb(Zr,Ti)O_3$ films, a promising material for high-density FeRAM, were deposited into narrow trenches by MOCVD. Polycrystalline PZT films were deposited directly on SiO_2/TiAlN/Ti/Si substrates having a trench structure with several aspect ratios by MOCVD with a liquid delivery system. $Pb(DPM)_2$, $Zr(MMP)_4$ and $Ti(MMP)_4$ were used as Pb, Zr and Ti source materials, respectively. Ethylcyclohexane and O_2 gas was also used as a solvent and an oxidant, respectively. The liquid sources were vaporized at individual vaporizers and mixed before introduced into a cold-wall type reaction chamber. The coverage properties of the PZT films in SiO_2 trenches were observed by scanning electron microscopy (SEM) and transmission electron microscopy (TEM). Compositional distribution of the PZT films was also investigated by energy dispersive x-ray spectroscopy (EDS) attached to TEM. In this study, we defined the ratio of film thicknesses at the sidewall (on SiO_2) and bottom (on TiAlN) of the trenches as effective step coverage. To fabricate the 3-D structured PZT capacitors, Ru bottom electrodes were deposited at 260 °C on SiO_2 trench substrates. On the trench substrates with the aspect ratio of 6.5:1 (the opening width and depth were 170 and 1080 nm, respectively), the effective step coverage of the

Ru films was achieved as high as 90 %. This result implies that Ru-based films can be adopted not only as the bottom electrode but also as the top one because the latter requires the deposition on PZT films with higher aspect ratio. When 35 nm-thick PZT films were deposited at 450 °C directly on SiO_2 trenches with the aspect ratio of 1.8:1 (the opening width and depth were 250 and 440 nm, respectively), the effective step coverage of the films was 70-75 %. In addition, a significant change of EDS peak intensity of PZT constituent elements was not observed along the depth direction at the sidewall of the SiO_2 trench. Almost the same values of the effective step coverage were obtained for 540 °C-deposited PZT films. These results suggest that uniformity of film thickness can be obtained within a wide deposition temperature region from this source materials combination.

2:15 PM D2.3
δ-Nb-doping Effect to the Interface Between IrO_2Top Electrode and Pb(Zr,Ti)O_3 by Metal Organic Chemical Vapor Deposition. Osamu Matsuura[1], Hideki Yamawaki[1], Masaai Nakabayashi[2], Yoshimasa Horii[2] and Yoshihiro Sugiyama[1]; [1]Fujitsu Laboratories Ltd., Atsugi, Japan; [2]Fujitsu Limited, Atsugi, Japan.

Ferroelectric Random Access Memory (FRAM) has advantage of high speed and low power consumption nonvolatile RAM, suitable for embedded memory, mobile use with high security. Considering larger-capacity memory, metal organic chemical vapor deposition (MOCVD) method should be necessary to form 3-dimensional ferroelectric capacitors, because low film porosity, thinner film controllability and good step coverage can be expected. Interface control between electrodes and ferroelectrics is essential role for the issues of remnant polarization (Pr), low leakage current density, high endurance to thermal imprint and fatigue free behavior. In this study, we investigate Nb-doping effect on electric characteristics using uniformly Nb-doped Pb(Zr,Ti)O_3 (UND-PZT) and δ-Nb-doped PZT (DND-PZT) on nondoped PZT by MOCVD. We used precursors of $Pb(DPM)_2$, $Zr(DMHD)_4$, $Ti(OiPr)_2(DPM)_2$, $Nb(DPM)_5$ diluted with THF. The source gases were regulated by liquid delivery system using vaporizer. The substrate temperature was set at 620°C. Highly oriented PZT was deposited on Ir/Ti/SiO_2/Si and had good ferroelectric characteristics as well as high endurance for imprint [1]. The PZT showed (111) preferred orientation measured by XRD. The composition of PZT was controlled at the Pb/Zr/Ti ratio of 105/40/60. Nb concentration (Nb/(Zr+Ti+Nb)) was 0 to 5 %. The total thickness of PZT was controlled to 120nm including 0-20nm of DND-PZT. First, we investigated the UND-PZT capacitors to reveal the influence of Nb-doping. Increasing the Nb concentration, hysteresis curve shifted positively and a leakage current density decreased by one or two order at lower bias (<1.8V). The shift suggests the existence of negative charge that increases the potential barrier for electron. The Pr decreased as increasing Nb concentration, which is caused by the decrease of the degree of tetragonal crystal as perovskite structure. Secondly, we investigated the ferroelectric capacitors with a DND-PZT. This capacitor structure also suppressed the leakage current at lower bias by about one order compared to nondoped PZT capacitor and decreased Pr slightly. Therefore, δ-Nb-doping to the top IrO_2 electrode/ PZT interface is effective to decrease the leakage current without decreasing Pr. Increasing Nb concentration, the leakage current with negative higher bias region (<-2V) increased. This asymmetrical behavior increased with increasing fraction of Nb-doping region. Since this behavior was also observed with UND-PZT, asymmetrical potential profile along growth direction can exist, which can be caused by defects related to PZT constituents. In summary, δ-Nb-doping at the interface between IrO_2 top electrode and PZT is effective to decrease the leakage current maintaining almost the same Pr as nondoped PZT. [1] Y. Horii et. al., IEDM2002, p.539

2:30 PM D2.4
Quantifying the Role of Electronic Charge Trap States on Imprint and Fatigue Behavior in Ferroelectric Poly(vinylidene fluoride-trifluoroethylene) (P(VDF-TrFE)) Thin Films. Connie Lew and Michael O. Thompson; Materials Science and Engineering, Cornell University, Ithaca, New York.

P(VDF-TrFE) ferroelectric thin films are a promising material for non-volatile memories. Fatigue, the loss of polarization with switching cycles, and imprint, the time-dependent tendency to resist polarization reversal, are key limitations that must be understood and minimized. Based on experimental measurements of the time and temperature dependence of imprint, we have investigated possible scenarios that link imprint, and potentially fatigue, to electronic charge trap states in the polymer. To quantify and characterize the density and dynamics of these traps, we have developed a fast-ramp thermally stimulated current (TSC) measurement technique suitable for monitoring the trap state dynamics within the seconds time-frame. Thin films of P(VDF-TrFE) with metal electrodes were fabricated on oxidized Si substrates. Following controlled polarization, fatigue, and imprint initialization, trap states were thermally filled/emptied through temperature cycling between 20-120°C with heating and cooling rates of 1-5°C/s. In addition to charge released and/or stored during thermal cycling, the final polarization state of the thin films was also determined. Imprint-induced filling of trap states has been verified from the TSC in the 1-1000 second time-frame. Similarly, thermally induced trap filling has been directly correlated with post-cycling imprint conditions. In addition, results show a significant asymmetry with field orientation (top versus bottom electrodes), suggesting that the trap density and characteristics are directly related to processing conditions and materials. Future experiments to correlate trap densities, energetics and kinetics with polymer and electrode compositions will be discussed.

3:15 PM *D2.5
Ferroelectric 1-T Memory Device – Will it be Viable for Nonvolatile Memory Application? Jin-Ping Han, [1]Semiconductor Electronics Division, NIST, Gaithersburg, Maryland; [2]IBM T.J. Watson Research Center, Yorktown Heights, New York.

The quest for a nonvolatile memory FET based on the metal-ferroelectric-semiconductor(MFS) or metal-ferroelectric-Insulator-semiconductor(MFIS) gate stack has greatly intensified in recent years because of the successful demonstration of ferroelectric thin films that can be integrated with Si-based CMOS technology. In principle, such a memory device could be building block for an ideal memory technology that offers random access, high speed, low power, high density and non-volatility. In practice, however, so far none of the reported ferroelectric memory transistors has achieved a memory retention time of more than a few days, a far cry from 10-year retention time requirement for non-volatile memory devices. A close look at the physics of the device operation reveals two major causes of the short retention: (1) depolarization fields; (2) finite gate leakage current and its associated charge trapping. The origins of these problem will be analyzed, and the semi-quantitative results of these analysis should help to illustrate the practical difficulties in attempting to realize a non-volatile 1-T memory device based on ferroelectrics. It will be revealed that grain size, surface roughness, thickness variation, interfacial properties, and crystallinity of the annealed ferroelectric SrBi2Ta2O9 (SBT) films have a strong impact on the size of the memory window, as does the choice of the buffer layer material. The aspects of the use of SiN as a buffer layer sandwiched between SBT and the Si substrate will be discussed, it's interesting to note that the switching of polarization of the ferroelectric SBT plays a key role for both the ferroelectric polarization dominated and the trapping dominated memory windows. Two possible solutions have been proposed to circumvent problems associated with the finite retention time in ferroelectric FET-type memories: (1) Refresh it as FEDRAM cell, (2) Single-crystallize the ferroelectric film. Acknowledgements: The author would like to thank NIST office of Microelectroncs Programs for financial support and Drs. E. Vogel, C.A. Richter, S-M. Koo at NIST for their insights and discussion. Part of the work was done at Yale University. The author would also like to thank Profs T.P. Ma, C.C. Broadbridge, K.-H. Kim, H.X. Liu, W. Tong, Drs W.J. Zhu, Z.J. Luo, Mr. Y.X. Liu, Mr.C.J. Xie for their help and support.

3:45 PM D2.6
Non-volatile thin film transistors using ferroelectric/ITO structures. Eisuke Tokumitsu and Masaru Senoo; Precision and Intelligence Lab., Tokyo Institute of Technology, Yokohama, Japan.

In this presentation, we report ferroelectric-gate thin film transistors (TFTs) using indium tin oxide (ITO) as a channel material. Ferroelectric-gate field-effect-transistors (FETs) are promising for future nonvolatile memory applications. However, it is difficult to fabricate ferroelectric-gate FETs with good electrical properties using silicon substrates because of the interaction between silicon and ferroelectric materials. In addition, mismatch between ferroelectric polarization and channel charge of silicon-based FETs makes it more difficult to obtain good electrical properties. On the other hand, the ferroelectric-gate TFTs using conductive oxides as channel materials were already reported. However, the reported drain current on/off ratios is usually very small. In this work, we report nonvolatile memory operations of ferroelectric-gate TFTs using ferroelectric/ITO structures which have the drain current on/off ratio of more than 10$\hat{3}$. Bottom-gate structure TFTs have been fabricated using ferroelectric Bi(4-x)La(x)Ti(3)O(12) (BLT) or Pb(Zr,Ti)O(3) (PZT) films, and ITO channel. Ferroelectric and ITO layers were formed by the sol-gel technique and RF sputtering, respectively. The channel length of the fabricated devices was varied from 40 to 120um. Drain current-drain voltage (ID-VD) characteristics of both BLT/ITO and PZT/ITO ferroelectric-gate TFTs exhibit typical n-channel transistor operations with clear current saturation. On-current as large as 1mA can be obtained for the BLT/ITO TFT when the applied gate voltage is 8V. Furthermore, drain current-gate voltage (ID-VG) characteristics demonstrate clear counterclockwise hysteresis loop due to the

ferroelectric gate insulator. The obtained memory windows are 4V and 2V for BLT/ITO and PZT/ITO structure devices, respectively. The on/off current ratio is more than 10$\hat{3}$ for both BLT/ITO and PZT/ITO devices, which indicates that the ITO channel is sufficiently depleted by the ferroelectric polarization.

4:00 PM D2.7
Solution-Processed Polymeric Ferroelectric Field Effect Transistors. Ronald Naber[1], Paul Blom[1], Gerwin Gelinck[2], Alwin Marsman[2] and Dago de Leeuw[2]; [1]Materials Science Centre, University of Groningen, Groningen, Netherlands; [2]Philips Research Laboratories, Eindhoven, Netherlands.

Field-effect transistors (FETs) with ferroelectric gate insulators are attractive for use as non-volatile memory elements. Their application has been strongly hampered by a relatively low on/off modulation (<100) and short retention (few days). In a recent all-organic ferroelectric FET with evaporated pentacene as semiconductor an on/off modulation of 50 has been achieved, with a retention time of a few hours (Adv. Mat., 16, 633 (2004)). In the present study we demonstrate polymeric ferroelectric FETs with all the active layers deposited by spin coating. In these devices the ferrolectric poly(vinylidene fluoride/ trifluoroethylene) is combined with a bisalkoxy-substituted poly(phenylene vinlyene) as semiconductor. The polymeric ferroelectric FETs have modulation ratios > 10$\hat{4}$, exceeding the state-of-the-art (both organic and inorganic) with two orders of magnitude. Furthermore, initial studies demonstrate that this high modulation ratio is unaffected after 24 hrs. Combined with a read/write operation within 1 ms these devices are a major step forward towards applications as memory elements in low-cost electronic circuits for electronic barcodes or display driver logic.

4:15 PM D2.8
Selection of ferroelectric/high-k gate stack combination for optimized FeFET performance. Zhen Xu[1,2], Matteo Viapiana[1,2], Ben Kaczer[1], Ludovic Goux[1], Guido Groeseneken[1,2] and Dirk Wouters[1]; [1]SPDT, IMEC, Leuven, Belgium; [2]ESAT-insys, KU leuven, Leuven, Belgium.

For the possible application of ferroelectric field-effect transistor (FeFET) type memories in embedded RAM applications, the scaling possibility towards future CMOS generation is a crucial property. One target is to obtain sufficient memory window at low operation voltage. Optimization of the gate stack materials (dielectric constant) and thicknesses is needed to get proper voltage division over the ferroelectric layer. We have studied different gate stack combinations of SBT (SrBi2Ta2O9) and BLT (Bi (4-x) LaxTi3O12) films on Al2O3/SiO2, HfO2/SiO2 or SiO2 insulator in Metal-Ferroelectric-Insulator-Silicon (MFIS) test structures. We have investigated Bi-layered perovskite films for the ferroelectric films as they have lower dielectric constant than e.g. PZT (PbZrxTi(1-x)O3), and as the highest polarization charge is not desired in FeFET application. The use of the high-k layer can be beneficial both as material diffusion barrier and by offering a lower total equivalent oxide thickness (EOT) than could be obtained by SiO2 or Si3N4 only, as the high ferroelectric charge switching at the ferroelectric/insulator interface may induce breakdown for too thin SiO2 films. We evaluated Al2O3/SiO2, HfO2/SiO2 as these are the gate stacks currently in development for the scaled CMOS devices. 6 nm HfO2 or 6nm Al2O3 is deposited by ALCVD on top of a 0.5 nm wet chemical SiO2, and 1 nm Rapid Thermal Oxidation SiO2,, resulting in a total EOT of 2 nm to 5 nm after the ferroelectric film crystallization anneal. The ferroelectric films were deposited by MOCVD (SBT) or spin-on (SBT, BLT) techniques, and different crystallization treatments (700-780oC) as well as film thicknesses (120-240 nm) were explored. The evaluation was based on both conventional high-frequency CV and pulsed-CV techniques to clarify the relative roles of trapping and true ferroelectric response. It was found that using the Al2O3/SiO2 insulator, strong trapping phenomena inhibit proper operation, while good ferroelectric performance is obtained on HfO2/SiO2. The relevant material properties (dielectric constant, Pr and EOT of high-k/SiO2) are calculated from the electrical response and used in a simulation model to predict the optimal stack configuration for low-voltage operation. Optimized stack performance will be presented.

4:30 PM D2.9
Effect of Ferroelectric/HfO_2/Si Structures on Electrical Properties of Ferroelectric-gate FETs. Koji Aizawa[1], Byung-Eun Park[2], Yoshihito Kawashima[3], Kazuhiro Takahashi[3] and Hiroshi Ishiwara[3]; [1]Precision & Intelligence Laboratory, Tokyo Institute of Technology, Yokohama, Japan; [2]Department of Electrical and Computer Engineering, University of Seoul, Seoul, South Korea; [3]Interdisciplinary Graduate School of Science and Engineering, Tokyo Institute of Technology, Yokohama, Japan.

Electrical properties of the p-channel metal-ferroelectric-insulator-silicon field effect transistors (MFIS FETs) using $Pt/SrBi_2Ta_2O_9(SBT)/HfO_2/Si$ and $Pt/(Bi,La)_4Ti_3O_{12}(BLT)/HfO_2/Si$ gate structures were investigated. An HfO_2 film as a buffer layer was deposited by a ultra-high-vacuum electron-beam evaporation method, and then annealed at 800°C in an oxygen ambient. The physical thickness of HfO_2 film is presumed to be approximately 10nm. 400-nm-thick SBT and BLT films were deposited on an HfO_2 buffer layer by sol-gel method. The channel width and channel length of the fabricated MFIS FETs were 50μm and 5μm, respectively. Typical drain current vs. gate voltage characteristics of the fabricated MFIS FETs with SBT/HfO_2 and BLT/HfO_2 structures showed clockwise hystereses due to polarization reversal of the ferroelectric films. The memory window (the width of the hysteresis loop) was approximately 1.0V in the SBT/HfO_2 structures and it was approximately 0.5V in the BLT/HfO_2 structures, when the gate voltage was swept between -5V and +5V. The data retention characteristics of the MFIS FETs with the SBT/HfO_2 and BLT/HfO_2 structures were measured after applying the single "write" pulse of either +10V or -10V in amplitude and 1μs in width. The reduction of the drain current on/off ratio was smaller than two decades even after over 10 days had elapsed. Most importantly, the significant drain current on/off ratio of the fabricated MFIS FETs using an SBT/HfO_2 structure was retained even after 30 days had elapsed at room temperature. It was also found in the fabricated MFIS FETs that the write pulse width as short as 20ns was enough for obtaining the significant drain current on/off ratio. The intrinsic leakage current across the ferroelectric/HfO_2 structure was found from the time dependence measurement of the leakage current to be lower than $1x10^{-10}$ A/cm^2. Therefore, these excellent properties of HfO_2 are considered to contribute mainly to retain stored data for a long time. It is conclude from these results that HfO_2 is one of the best buffer layer materials for realizing the single-transistor-type FeRAMs using MFIS FETs with long data retention and high operation speed.

4:45 PM D2.10
Device Structures and Characterization of One Transistor Ferroelectric Memory Devices. Tingkai Li, Sheng Teng Hsu, Bruce Ulrich and David Evans; PTL, Sharp Labs. of America, Inc., Camas, Washington.

Pt/PGO/HfO2/Si (MFIS), Pt/PGO/Ir/Polysilicon/SiO2/Si (MFMPIS) and Pt/PGO/Ir/InO2/Si (MFMMoxS) ferroelectric one-transistor devices have been fabricated. The working functions and properties of Pt/PGO/HfO2/Si (MFIS), Pt/PGO/Ir/Polysilicon/SiO2/Si (MFMPIS) and Pt/PGO/Ir/InO2/Si (MFMMoxS) ferroelectric one-transistor devices have also been measured. Compared with PGO MFIS one-transistor devices, PGO MFMPIS one-transistor devices showed lower operation voltage, smaller sub-threshold voltage swing, larger memory windows and better retention properties, but more difficult integration processes. MFMMoxS ferroelectric one-transistor devices exhibit the similar memory working function with MFMPIS memory devices, but much better retention properties. 1T MFMMoxS memory devices show the memory windows are 2 V, and the memory windows are saturated from 5V. After program to off and the on states, the drain current at Vg of 0.5V and Vd of 0.1V is about 5 x 10-12 A and 1 x 10-6 A respectively, the ratio of on state to off state is about 6 orders. All the MFMMoxS memory devices show that the threshold voltage of on state increases with retention time, and the threshold voltage of off state will be constant with retention time. The MFMMoxS memory devices exhibit very good retention properties. In order to find the reasons for the different properties between MFIS, MFMPIS and MFMMoxS one-transistor devices, the relationship between the properties and structures, including interface and microstructure, has been investigated and discussed.

SESSION D3: Poster Session: Ferroelectric II
Chairs: Yoshihisa Fujisaki and Jon Slaughter
Tuesday Evening, November 30, 2004
8:00 PM
Exhibition Hall D (Hynes)

D3.1
Improvement of Ferroelectric and Electrical properties of Sol-Gel Deposited $Bi_4Ti_3O_{12}$ Thin Films by Multiple Rapid Thermal Annealing Techniques. Hua Wang, Department of Information Material Science and Engineering, Guilin University of Electronic Technology, Guilin, Guangxi Province, China.

Ferroelectric $Bi_4Ti_3O_{12}$ (BIT) thin films were fabricated by sol-gel method and multiple rapid thermal annealing (MRTA) techniques on $Pt/Ti/SiO_2/p$-Si substrates. The effects of annealing temperature and time on the crystallinity, the ferroelectric and electrical properties of $Bi_4Ti_3O_{12}$ films derived by MRTA and by normal RTA were investigated. BIT films were polycrystalline and their x-ray diffraction

patterns exhibited peaks corresponding to the (117), (004), (006), (008) and (111) reflections of the perovskite phase of BIT. The grain size and the roughness of surface increase with the annealing temperature increase, but the maximal remnant polarization of $Bi_4Ti_3O_{12}$ films come forth when the annealing temperature is 650°C. The perovskite-phase of BIT thin films were formed at lower annealing temperature and smaller grain size were obtained in the BIT thin films prepared by MRTA compared with that by normal RTA. The typical values of remnant polarization of $Bi_4Ti_3O_{12}$ films derived by MRTA was 11 μC/cm^2, which was higher than that derived by conventional RTA about 15%, while the leakage current density was 8.9×10^{-8} A/cm^2 by MRTA, which was lower than that by normal RTA about 90%.

D3.2

Characterization of MFMIS and MFIS Structures for Non-volatile Memory Applications. Mosiur Rahman[1], Thottam S. Kalkur[1], Shunming Sun[1], Fred P. Gnadinger[2], David Dalton[2], Daesig Kim[2], Viorel Olariu[2] and David Klingensmith[2]; [1]ECE, University of Colorado at Colorado Springs, Colorado Springs, Colorado; [2]COVA Technologies Inc., Colorado Springs, Colorado.

To eliminate the interface reaction problems in MFS (metal-ferroelectric-semiconductor) and MFIS (metal-ferroelectric-insulator-semiconductor) structures, a gate layer sandwich of the MFMIS (metal-ferroelectric-metal-insulator-semiconductor) is proposed. This structure consists of Pt-SBT-Pt-ZrO2-SiO2-Si stacks. In the MFMIS structure the MIS capacitor is separated from the ferroelectric MFM capacitor through a metal as inter diffusion barrier. Therefore, the MIS capacitor with SiO2 and ZrO2 as an insulator with excellent interface properties can be used and MFM acts as an ideal ferroelectric capacitor. As MFMIS is a series combination of MFM and MIS capacitors, it behaves as a voltage divider. The gate voltage is divided according to the capacitance ratio of the MIS and MFM structures. Since the fabricated devices have access to the floating gate, characteristics of the MFM and MIS capacitors can be determined independently to compare the characteristics of the MFMIS structure as a single capacitor. Then transistor characteristics of this structure, MFMIS FET, can be evaluated in various operating regions. Measurements of various ratios of MIS capacitance to MFM capacitance at different polarization conditions have been performed to build a SPICE like circuit model which will completely describe and predict the behavior of the MFIS and MFMIS structures.

D3.3

Improvement of Ferroelectric Properties of Lead Zirconate Titanate Thin Films by Ion-substitution using Various Rare-earth Cations. Hiroshi Nakaki[1], Hiroshi Uchida[1], Shoji Okamoto[2], Shintaro Yokoyama[2], Hiroshi Funakubo[2] and Seiichiro Koda[1]; [1]Department of Chemistry, Sophia University, Tokyo, Japan; [2]Department of Innovative and Engineered Materials, Tokyo Institute of Technology, Yokohama, Japan.

Authors attempted the improvement of ferroelectric properties of PZT films by promoting the anisotropy of simple-perovskite crystal. Crystal anisotropy of PZT was controlled by the species and occupying site of substituent cation; B-site substitution using rare-earth cations whose ionic radii locate on smaller parts of its series (such as Y^{3+}, Gd^{3+}, Dy^{3+}, Yb^{3+}, etc.) can promote the anisotropy of PZT crystal, i.e., the ratio of PZT lattice parameters (c/a), whereas inverse phenomenon occurs in the case of A-site substitution using rare-earth cations whose ionic radii locate on larger parts of its series (such as La^{3+}, Nd^{3+}, etc). In this study, authors investigated the influences of the B-site substitution using some rare-earth cations on the properties of PZT film in order to confirm whether controlling the crystal anisotropy using rare-earth cation is effective for the improving the ferroelectric properties. PZT-based films were fabricated by a chemical solution deposition. Spin-coating solutions with chemical compositions of $Pb_{1.00}Ln_x(Zr_{0.40}Ti_{0.60})_{1-(3x/4)}O_3$ were prepared using lead acetate, zirconium iso-propoxide, titanium normal-buthoxide, rare-earth (Ln: Y, Gd, Dy and Yb) nitrates and 2-methoxyethanol as starting materials. These solutions were spin-coated on (111)Pt/Ti/SiO_2/(100)Si substrate, followed by a drying (150°C, 10 sec, in air) and a pyrolysis process (400°C, 3 min, in air). After repeating these processes several times, the resulting films were heat-treated for crystallization at 650°C for 5 min in air. Remanent polarization (P_r) of polycrystalline PZT film on (111)Pt/Ti/SiO_2/(100)Si was enhanced by Dy^{3+}- and Y^{3+}-substitution from 20 μC/cm^2 ($x = 0$) up to 25 and 26 μC/cm^2 respectively ($x = 0.02$). Enhancement of P_r value was achieved by increasing the crystal anisotropy of PZT, i.e., the ratio of PZT lattice parameters (c/a). On the other hand, ion substitution using Gd^{3+} and Yb^{3+} degraded the P_r value from 20 μC/cm^2 ($x = 0$) down to 15 and 16 μC/cm^2, respectively ($x = 0.02$) nevertheless the increase of crystal anisotropy. Leakage current densities of Gd^{3+}- and Yb^{3+}-substituted PZT films (= 10^{-5} 10^{-4} A/cm^2) were larger than those of Y^{3+}-, Dy^{3+}- and non-substituted PZT films (10^{-6} A/cm^2). The degradation of ferroelectric properties at Gd^{3+}- and Yb^{3+}-substituted PZT films is ascribed to the lattice defects derived from Pb^{2+}-deficiency and lower-valent cation doping respectively. We concluded that ion substitution using some rare-earth cations such as Y^{3+} and Dy^{3+} is one of promising technology for improving the ferroelectric property of PZT film.

D3.4

Perfectly c-axis oriented epitaxial lead titanate thin film deposited by a hydrothermal method for a data storage medium. Takeshi Morita and Yasuo Cho; Research Institute of Electrical Communication, Tohoku University, 2-1-1 Katahira, Aoba-ku, Sendai, Miyagi, Japan.

A hydrothermal method has various advantages; low deposition temperature, high-purity, deposition on a three-dimensional structure and a large thickness. Morita successfully measured the DE hysteresis properties of a hydrothermally deposited epitaxial PZT film using a $SrRuO_3$ bottom electrode on (100) $SrTiO_3$ single crystal[1]. It is important to note the extremely low reaction temperature of 150°C. An imprint of the PZT thin film, however, was too large to reverse and maintain the intended poling direction. Hence; this PZT thin film was not suitable for a FeRAM application and ultra-high density storage medium to construct a nano dot pattern with a conductive atomic force microscopy (AFM) probe. The present paper investigates the $PbTiO_3$ to improve lattice matching to the substrate. $PbTiO_3$ is an important perovskite-type ferroelectric material, although high quality crystal was previously thought to be quite difficult to obtain. The remanent polarization for lead titanate was predicted to be 81 μC/cm^2 and thus far, very little experimental data has been provided for this fundamental value, with the exception of that reported by Tabata[2]. By modifying the reaction conditions, the epitaxial $PbTiO_3$ film was obtained with the hydrothermal method at 150°C. The full width at half maximum (FWHM) of the rocking curve of the (002) $PbTiO_3$ film on $SrTiO_3$ was 0.060°. The reciprocal space mappings of (103) verified that the $PbTiO_3$ films had perfectly c-axis orientation. To study the ferroelectric properties, a $SrRuO_3$ thin film was deposited on $SrTiO_3$ single crystals, and the $PbTiO_3$ thin was deposited on $SrRuO_3/SrTiO_3$. The low reaction temperature realized the high insulation properties and superior purity crystal. The single crystal-like DE hysteresis curve showed a remanent polarization of 96.5 μC/cm^2. The scanning nonlinear dielectric microscopy (SNDM) observation verified that this film had perfectly c-oriented and did not contain an a-domain. In addition, no defects such as domain or grain boundaries were observed, even on the nano scale. This outstanding performance indicated that this $PbTiO_3$ was the appropriate medium for ultra-high density system. Pulse applied voltage was subsequently applied to pattern domain dots with various pulse parameters with metal coated AFM cantilever. The minimum dot radius of 12 nm was achieved under the trial parameters with -5 V and a 40 μsec pulse. This size corresponds to a data size of 1Tbit/inch^2. [1] T. Morita et al., Appl. Phys. Lett., vol. 84-25, 5094 (2004) [2] H. Tabata et al., Appl. Phys. Lett., vol. 64-4, 428 (1994)

D3.5

Switching Properties of PST ferroelectric films for memory applications using conductive oxide LSCO electrodes. Guerra Eduardo Martinez[1], Cruz Abel Fundora[1], Alonso Oscar Blanco[2] and Beltrones Jesus M. Siqueiros[1]; [1]Fisica de Materiales, Centro de Ciencias de la Materia Condensada-UNAM, Ensenada, B.C., Mexico; [2]Centro de Investigacion en Materiales, CUCEI-U.de G., Guadalajara, Mexico.

We have investigated the switching properties of ferroelectric lead-strontium titanate $Pb(Sr,Ti)O_3$ capacitors using epitaxial LSCO electrodes to evaluate its potential for non-volatile memory applications. The electrical performance of the PST based capacitors was evaluated through Polarization-Voltage (P-V) and Fatigue measurements. The ⟨001⟩ preferred orientated PST ferroelectric capacitor was not subjected to loss of its polarization up to 10^8 switching cycles at an applied voltage of 4 V and a frequency of 100 kHz. It is proposed that the high degree of ⟨001⟩ orientation of the PST films induced by the epitaxial LSCO is responsible for the good performance of the PST film capacitors. However, after 10^{10} switching cycles in fatigue tests, the decay of the non-volatile polarization of these films was about 20% of the initial value. We propose a simple model to describe two major microscopic scenarios for the supression of the switching polarization ($P_r{}^s$); i.e, pinning of ferroelectric domain walls (DWs) through the PST film (bulk scenario) and inhibition of the growth of opposite domains due to the nucleus suppression at the electrode interfaces (interface scenario). This model is supported by Auger Spectroscopy to determine the bulk and interfacial characteristics. The depth distribution of the elements of the PST film is nearly uniform through the whole bulk, however the composition of Pb and O were abnormal on the surface. It is

concluded than in spite of the good performance due to the favorable environment for the growth of PST system provided by the textured LSCO, a higher quality interface and a better control of composition it is necessary to improve its fatigue behavior.

D3.6

Excimer (XeCl) Laser Annealing of PbZr0.52Ti0.48O3 Thin Film at Low Temperature for TFT FRAM Application. Wenxu Xianyu[1], Takashi Noguchi[1,2], Hans Cho[1], Jangyeon Kwon[1] and Huaxinag Yin[1]; [1]Samsung Advanced Institute of Technology, Suwon, Gyunggi-Do, South Korea; [2]Sungkyunkwan University, Suwon, Gyunggi-Do, South Korea.

SoG (system on glass) technology is being developed to integrate multiple electronic functions onto glass substrates, with the final applications being mobile systems such as card-type displays and sheet-like computers. For these mobile internet-capable SoG applications, the key requirements are nonvolatile functionality, low power consumption, minimal added process complexity and compatibility with LTPS (low-temperature poly-silicon) technology. Ferro-electric random-access memory (FRAM) is a promising candidate for SoG memory devices because of its high access speed, low power consumption and simple two-mask process. In this study, we successfully produced PbZr0.52Ti0.48O3 (PZT) thin films with high crystallinity and high remnant polarization at low process temperatures using pulsed excimer laser (XeCl) irradiation. We also propose a new technology for fabrication of thin film transistor (TFT)-driven FRAM devices. In our experiments, amorphous PZT films were prepared on Pt/Ti/SiO2/Si substrates by a sol-gel method. A two-step process was used to crystallize the amorphous thin films: the films were annealed at 550 oC for 10 min to initiate the nucleation of the PZT perovskite phase, and then annealed with a XeCl excimer laser at 400 oC in a 120 Torr nitrogen gas atmosphere. Laser energy density was varied from 100 to 600 mJ/cm2 per pulse (pulse laser width of 180 ns). X-ray diffraction patterns showed that laser-annealing drastically improved the crystallinity of the PZT film, crystallizing it into the perovskite phase and not the pyrochlore phase. SEM photographs show that the PZT thin film has uniform-sized crystal grains. The ferroelectric properties were found to depend on the laser energy density, shot number, and gas pressure. Before the laser annealing, the films show hysteresis loops with low remnant polarization (Pr) and the loops do not saturate. After laser annealing, the films show highly saturated hysteresis loops, with the Pr increasing from 2.2 μC/cm2 to 23.0 μC/cm2.

D3.7

Optimization of the ferroelectric film for application in scaled FeFET. Matteo Viapiana[1,2], Zhen Xu[1,2], Ludovic Goux[1], Ben Kaczer[1], Guido Groeseneken[1,2] and Dirk Wouters[1]; [1]SPDT, IMEC, Leuven, Belgium; [2]ESAT-INSYS, KULeuven, Leuven, Belgium.

For the proper operation of a ferroelectric field-effect transistor (FeFET), both the electrical and structural properties of the ferroelectric film are of crucial importance. Relevant material properties are the remanent polarization, the coercive field and the dielectric constant. As the ferroelectric materials are crystalline and exhibit a strong anisotropy, good control of the crystal orientation is required. The ferroelectric thin films, however, are typically polycrystalline, so the grain boundary orientation and size distribution are important parameters especially towards further technology scaling. In this work, we characterized SBT (SrBi2Ta2O9) and BLT (Bi4-xLaxTi3O12) films deposited on Al2O3/SiO2 and HfO2/SiO2 insulator stacks or directly on SiO2 insulator, for their application in the Metal-Ferroelectric-Insulator-Si (MFIS) gate stack of a FeFET-based memory. The SBT and BLT films are deposited by spin-on followed by low temperature heat treatments for drying and pyrolysis, and is repeated for making thicker films. The final crystallization is done using a rapid thermal anneal (RTA) system. The electrical performance of the films was derived from high-frequency C-V evaluation of MFIS capacitor structures, and compared with that of Pt/FE/Pt metal-insulator-metal (MIM) capacitor structures using the same FE deposition process. It was found that good electrical properties of the MFIS structures could only be obtained at the higher crystallization temperature (780C, compared to 700C or lower for FE films directly deposited on Pt substrates), pointing to a more difficult nucleation on the metal oxide films. On the other hand, the value of the remanent polarization (Pr) as indirectly derived from the C-V measurements is much lower (typically <1uC/cm2) as compared to that obtained on MIM capacitors. Also, the MFIS structure on Al2O3 showed strong trapping behavior that may indicate a poor interface with the ferroelectric layer. The full electrical and structural characterization of the FE films on the different insulator stacks will be reported, and the results of SBT and BLT will be compared.

D3.8

Improvements in Electrical Properties of Hydrogen-Treated Ferroelectric Capacitors with PtOx Top Electrode for Memory Applications. Chun Kai Huang and Tai-Bor Wu; Material Science Engineering, Material Science Engineering, Hsinchu, Taiwan.

The electrical properties of reactive sputtered PtOx(x=0.4 1.2)/PbZr0.4Ti0.6O3 (PZT) /Pt and Pt/PZT/Pt capacitors against forming gas H2 annealing at 200°C were studied. It was found that the hydrogen degradation of the capacitors can be highly suppressed with the use of PtOx top electrode. The X-ray photoelectron spectroscopy analysis of the PtOx films shows a chemical shift of O1s spectra chemical shift in binding energy from 529.5 to 530.1eV before and after annealing. This oxygen chemical shift is in association with the trapped hydrogen atoms. A 1.5V voltage offsets of polarization-field hysteresis loop along with an increase of leakage current density were observed from that with Pt top electrode. The leakage current of the degraded capacitors was controlled by the mechanism of Schottky emission in temperature range of 273K to 423K and electrical field above 0.2 MV/cm and a reduction of barrier height was also observed. Ultraviolet photoemission spectroscopy analysis indicates that the work function of Pt was lowered for 0.5eV by the H2 annealing, resulting in the barrier height reduction. The secondary ion mass spectroscopy and elastic recoil detection analysis reveal that the high density defects were created by the catalytic reaction on the Pt surface and originated mainly at the interface of PZT and Pt electrodes. Pinning between domains and defect dipoles due to charged defects is suspected to dominate the initial stage of the degradation. The relationship between the defect density and barrier height is in good quantitative agreement with the Schottky barrier height model.

D3.9

Developments of Nonvolatile Memory using Well-Ordered Ferroelectric Linear Molecules. Kenji Ishida[1], Kazunari Katsumoto[1], Shuichiro Kuwajima[2], Toshihisa Horiuchi[1], Hirofumi Yamada[1] and Kazumi Matsushige[1]; [1]ES&E, Kyoto University, Kyoto, Japan; [2]Nanotech Support Project, Kyoto University, Kyoto, Japan.

Vinylidene fluoride (VDF) linear molecules with large electric dipoles, which is generated between fluorine and hydrogen atoms in the individual vinylidene fluoride (CH2CF2) units, exhibit ferroelectric properties. Especially, newly synthesized VDF oligomers with low molecular weight have performed novel ferroelctricities because of their high crystallinites. In this presentation, the ferroelectric and dielectric properties and its nonvolatile memory application of VDF oligomer molecular films will be discussed. The VDF oligomer, CF3-(CH2CF2)n-I;n=10-29, films of 5-100nm were fabricated by vacuum deposition without thermal decomposition. The structures, molecular orientation and surface morphology depend on the deposition parameters (substrate temperature;Ts, substrate species). The relative dielectric constant of the parallel oriented VDF oligomer films was estimated to be about 2.0 in the frequency range from 0.1Hz to 1MHz in room temperature. A rectangular polarization hysteresis loop was observed in well-ordered VDF oligomer thin films, and the remanent polarization evaluated to be 130mC/m2, which is the largest value among organic molecules. Fatigues of polarization reversal can be performed over 10^5 cycles. These results suggest that the VDF oligomer can be one of candidates for disposable ferroelectric memory with unique features such as flexible, wide areas and low costs of fabrication.

D3.10

Complex Oxide Nanostructures by Pulsed Laser Deposition through Nanostencils. Cristian Victor Cojocaru, Catalin Harnagea, Federico Rosei and Alain Pignolet; INRS-EMT, Universite du Quebec, Varennes, Quebec, Canada.

A flexible method for simultaneous nanoscale structures fabrication and patterning is described, using a combination of stencil mask and pulsed-laser deposition (PLD) techniques [1, 2]. A miniature shadow-mask with nano-apertures in a very thin microfabricated membrane (nanostencil) was first manufactured and then, mechanically attached to the substrate of choice. To create free-standing membranes with arrays of apertures of different shapes and dimensions below 500 nm, a combination of advanced lithography or high-precision ion milling by focused-ion-beam (FIB) and silicon micromachining techniques was used. Using PLD, complex oxides such as BaTiO3 and BiFeO3 were deposited directly through the stencil's holes onto various substrates (Si, Pt, SrTiO3 and SrRuO3). Ordered arrays of nanostructured complex oxides were obtained in a single deposition step, which replicate the aperture patterns in the stencil membrane. The morphology and composition of these nanostructures were characterized by scanning electron microscopy (SEM), atomic force microscopy (AFM) and X-ray diffraction (XRD). Analyses reveal periodic, entirely separated and well-defined structures over large areas corresponding to openings in the sieves (1mm length x 100 μm width). Ferroelectric properties of the patterned structures of different sizes were investigated by AFM piezoresponse method in order to

study size effects in ferroelectrics. Pulsed laser deposition parameters as well as the geometrical attachment of the stencil onto the substrate are important factors that must be tuned during the process in order to increase the steepness of the structures. Several other issues related with the deposition process such as large scale uniformity and periodicity of deposited nanostructures across the substrate and the stencil's life time were also investigated and will be presented and discussed. This approach offers a simple, reliable, parallel method for growing, patterning and positioning ferroelectric functional nanostructures on various substrates, which is of wide interest for applications in microelectronics, for instance for Ferroelectric Random Access Memories (FeRAM). It also represents a promising "tool" for local deposition of multiple geometries and high-purity nanostructures under high-vacuum or ultra-high vacuum conditions, in laboratories without expensive lithography equipment. [1] Jurgen Brugger et al. Microelectronic Engineering 53 (2000) 403 [2] Emiel A. Speets et al. Nano Letters, vol.4, no.5 (2004) 841-844

D3.11

Leakage Current and Ferroelectric Response of Bi1-xNdxTi3O12 Thin Films. Maharaj S. Tomar[1], R. E. Melgarejo[1], R. P. Guzman[1], Subhasish Basu Majumder[2] and R. S. Katiyar[2]; [1]Department of Physics, University of Puerto Rico, Mayaguez, Mayaguez, Puerto Rico; [2]Physics Department, University of Puerto Rico, San Juan, San Juan, Puerto Rico.

In the past few years, Nd substituted bismuth titanate spin coated films have shown fatigue free giant ferroelectric response, but there is a lack of information on their leakage current response. Bi1-xNd xTi3O12 films were prepared by sol-gel process and thin films were deposited by spin coating on Pt (Pt/TiO2/SiO2/Si) substrate. Top Pt electrode was deposited by dc sputtering, and the room temperature leakage current was measured on the films with compositions x= 0.00, 0.36, 0.56, and 0.75 in Pt/film/Pt capacitor configuration. Films were prepared under similar conditions and in each case the film thickness was 0.75 ?m. The measured leakage current in pure Bi4Ti3O12 film (x = 0.00) was much lower in comparison with Nd substituted films. The lowest leakage current (less than 10-10 A) was observed in the film with composition x = 0.75. The leakage current behavior could be explained by defect mediated phenomena. Ferroelectric response presented for different composition shows the highest polarization for the composition x = 0.56. These results indicate the potential application of Nd substituted bismuth titanate films in non-volatile ferroelectric memories. * This work is supported by DoD-ONR Grant No. N00014-02-1-0215, and is gratefully acknowledged.

D3.12

Dielectric and Fatigue Properties of PZT Thin Films Prepared From Oxide Precursors Method. Silvia T. Shibatta-Kagesawa[1], Cristiano A. Guarany[2], Eudes B. Araujo[2] and Nobuo Oki[1]; [1]Engenharia Eletrica, Universidade Estadual Paulista, Ilha Solteira, SP, Brazil; [2]Fisica e Quimica, Universidade Estadual Paulista, Ilha Solteira, SP, Brazil.

Fatigue is a serious problem for a ferroelectric film to overcome for non-volatile memory applications. In this phenomena, the remanent polarization and coercive field properties degrades with cycles increasing on hysteresis loops. The reasons have been attributed to different mechanisms such as a large voltage applied on ferroelectric film at every reading process in Ferroelectric Randon Access Memory (FeRAM) or memories for digital storage in computer, grain size effects and others. The aim of this work is to investigate the influence of the crystallization kinetics on dielectric and ferroelectric properties of the $Pb(Zr_{0,53}Ti_{0,47})O_3$ (PZT) thin films prepared by an alternative chemical method denominated Oxide Precursor Method. Films were crystallized air atmosphere on $Pt/Ti/SiO_2/Si$ substrates at 700°C for 1 hour, using a conventional furnace, and at 700°C for 1 and 5 min, using a rapid thermal annealing (RTA) process. Final films were crack free and presented 1 μm in thickness in average. Dielectric properties were studied as a function of frequency from 100 Hz to 1 MHz. Films crystallized from RTA shows a dielectric dispersion at low frequency but PZT film crystallized in conventional furnace this dispersion disappear. Ferroelectric properties were measured from hysteresis loops at 10 kHz. The obtained remanent polarization (P_r) and coercive field (E_c) were 3.2 $\mu C/cm^2$ and 53 kV/cm film crystallized in conventional furnace while in films crystallized from RTA these parameters were respectively around 3.7 $\mu C/cm^2$ and 55 kV/cm. In the fatigue process, the Pr value decreased up to 16% from initial value after 1.3 x 10^9 switching cycles, for film crystallized in conventional furnace, while for film crystallized from RTA Pr decreased up to 48% from initial value after 1.7 x 10^9 switching cycles.

D3.13

Characteristics of MFMISFET with $Pt/SrBi_2Ta_2O_9/Pt/Y_2O_3/Si$ Gate Structure. Sun Il Shim[1,2], Young Suk Kwon[2], Ik Soo Kim[2], Seong-Il Kim[2], Yong Tae Kim[2] and Jung Ho Park[1]; [1]Electronics Engineering, Korea University, Seoul, South Korea; [2]System Technology Division, Korea Institute of Science and Technology, Seoul, South Korea.

The metal-ferroelectric-semiconductor and metal-ferroelectric-insulator-semiconductor (MFS and MFIS) gate structure for the single transistor type ferroelectric random access memory (FeRAM) have inherent weak points in short retention for non-volatile memory and high operating voltage in spite of its advantages in non-destructive read operation and small cell size. For the full saturation of the ferroelectric film to obtain long retention, the insulator with high dielectric constant is requited. The alternative solution is metal-ferroelectric-metal -insulator-semiconductor (MFMIS) gate structure with different area ratio. The induced voltage to the ferroelectric film can be modulated by the area ratio between MFM capacitance and MIS capacitance. The Y_2O_3 thin film was introduced as a high-k insulating layer in this experiment. It has presented good characteristics as a buffer insulating layer in MFIS gate structure. The Y_2O_3 film with the thickness of 20 nm was deposited by rf sputtering of yttrium target in the reactive oxygen ambient and crystallized at 800 °C for 30 min in the oxygen ambient. $SrBi_2Ta_2O_9$ (SBT) film with the thickness of 280 nm was used as a ferroelectric material. The MFMIS capacitor was fabricated with various area ratios and the electrical characteristics were investigated. The capacitance - voltage characteristic with the area ratio from 2 to 10 was measured. The memory windows were increased from 0.4 V to 1.6 V at the operating voltage of 5 V with the area ratio from 2 to 10. The MFMISFET was fabricated and the electrical characteristics were investigated. It showed well-behaved counter clockwise drain current versus gate voltage characteristics and more than three orders of drain current difference between the programmed on state and the erased off state at 5 V operation

D3.14

Nanoelectromechanics of Ferroelectric Lithography and Near-Atomic Density Data Storage by Piezoresponse Force Microscopy. Sergei V. Kalinin[1], J. Shin[1,2], Arthur P. Baddorf[1], M. Kachanov[3], E. Karapetian[3] and A. Gruverman[4]; [1]Condensed Matter Sciences Division, Oak Ridge National Laboratory, Oak Ridge, Tennessee; [2]Department of Physics and Astronomy, The University of Tennessee, Knoxville, Tennessee; [3]Department of Mechanical Engineering, Tufts University, Medford, Massachusetts; [4]Department of Materials Science and Engineering, North Carolina State University, Raleigh, North Carolina.

The ability of ferroelectric materials to form stable sub-10 nm domains makes them one of the most promising materials for information storage applications. In the last several years, domain patterning using scanning probe technology was demonstrated to yield 40 nm domains, corresponding to 0.5 Tbit/in^2 recording density. At the same time, Piezoresponse Force Microscopy (PFM) is routinely demonstrated to provide readout with 3-5 nm resolution, i.e., two orders of magnitudes higher recording density. To increase the achievable recording density, an understanding of the tip-induced polarization switching process is crucial. Here we analyze nanoscale polarization switching in ferroelectric materials by PFM using exact solutions for electrostatic and coupled electroelastic fields below the tip. The solution of the coupled electroelastic problem for piezoelectric indentation is derived and used to obtain the tip-induced electric field and strain distribution in the ferroelectric material. This establishes a complete continuum mechanics description of the PFM imaging mechanism. The structure of tip-induced electroelastic fields is combined with the Landauer approach to provide a quantitative description of tip-induced polarization switching. It is proposed that the tip-induced domain switching can be mapped on the Landau theory of phase transitions with the domain size as an order parameter. For a point-charge interacting with a ferroelectric surface, switching of both first and second order is possible depending on the charge-surface separation. For a realistic tip shape, the domain nucleation process is first order in charge magnitude and polarization switching occurs only above a critical tip bias. In pure ferroelectric or ferroelastic switching, the late stages of the switching process can be described using a point charge/force model and arbitrarily large domains can be created; however, the description of the early stages of the nucleation process when the domain size is comparable with the tip radius of curvature requires the exact field structure to be taken into account. Optimal conditions for tip-induced polarization switching are determined and compared with experimental results for $LiNbO_3$ single crystals and $PbTiO_3$ epitaxial thin films. Research was sponsored by the U.S. Department of Energy, under contract DE-AC05-00OR22725 with UT-Battelle, LLC and by the National Science Foundation grant DMR-0072998. Research performed as a Eugene P. Wigner Fellow (SVK).

D3.15

Combinatorial Search of (Bi,Ce)4Ti3O12 and (Bi,La,Ce)4Ti3O12 Prepared by Liquid Source Misted

Chemical Deposition (LSMCD) and Multi-Target Sputtering System. Seong Ihl Woo[1,3], Ki Woong Kim[1,3], Min Ku Jeon[1,3], Kwang Seok Oh[1,3], Tai Suk Kim[1,3] and Yong Ki Park[2,3]; [1]Chemical and Biomolecular Engineering, Korea Advanced Institute of Science and Technology, Daejeon, South Korea; [2]Korea Research Institute of Chemical Technology, Daejeon, South Korea; [3]Center for Ultramicrochemical Process Systems (CUPS), Daejeon, South Korea.

We used the multi-target sputtering system equipped with movable mask to fabricate the Bi4-xCexTi3O12 (BCT, 0< x <4) from Bi2O3 /CeO2 /TiO2 multi-layers. Here, the movable mask gives the variance of Bi/Ce over the substrate. To improve the solid-state intermixing, the deposition process was carried out at 300°C. We mapped the structural characteristics and ferroelectrical properties of BCT array as a function of Ce content, x. Microbeam XRD data showed that there were three phases; Bi-layered structure (x<0.8), Bi2Ti2O7 + CeO2 (0.8< x <2), and Bi2O3 + CeO2 (x>2).In addition, raman spectra of BCT exhibited three characteristic peaks of TiO6 at 260, 550, and 847cm^1 in Bi-rich region but as Ce content is increased, these peaks were shifted to 205, 460, and 608 cm^1 relative to CeO2. To recognize the ferroelectric property, we deposited top electrode on the BCT array and then measured P-E hysteresis curve by using RT66A. In the Bi-rich region (x<0.8), the samples showed the ferroelectric characteristic and 2Pr ranged from 4 to 7 μC/cm^2 at 10V, but in the Ce rich region, BCT array showed the paraelectric properties. Therefore, we concluded that it is possible to mix the solid-state layers only in Bi-rich region and as Ce content was reduced, the ferroelectric property of BCT could be improved. On the basis of this conclusion, we fabricated other library of Bi3.75La0.25-xCexTi3O12 (BLCT) by liquid source misted chemical deposition (LSMCD) equipped with movable mask. Unlike the sputtering system, this deposition has an advantage that it could improve the homogeneity of library due to the liquid-liquid intermixing at R.T. Here, in the La-rich region (0.05< Ce content, x <0.1), we observed that the intensity of (117) peak indicating the degree of asymmetricity of TiO6 was maxmized and especially, these samples with this composition, 0.07<x<0.09, exhibited higher 2Pr (> 20μC/cm^2) and lower 2Ec (< 220kV/cm) at 10V than other samples. Therefore, we concluded that the ferroelectric properties were relative to the degree of TiO6 distortion. In addition, these samples exhibited good fatigue properties over 10^10 cycles.

D3.16
Cation Disorder and Structural Analysis of Ferroelectric (Bi,Ce)4Ti3O12 Using Neutron Powder Diffraction and Raman Spectroscopy. Seong Ihl Woo[1], Min Ku Jeon[1], Yong-Il Kim[2], Jung Min Sohn[1], Ki Woong Kim[1] and Tai Suk Kim[1]; [1]Dept. of Chemical and Biomolecular Engineering & Center for Ultramicrochemical Process Systems, Korea Advanced Institute of Science and Technology, Daejeon, South Korea; [2]Korea Research Institute of Standards and Science, Daejeon, South Korea.

Ferroelectric Bi4Ti3O12, BTO, and Bi(4-x)Ce(x)Ti(3)O(12) (x = 0.25, 0.5 and 0.75), BCT, samples were synthesized by a conventional solid state reaction. Before structural analysis of BTO and BCT, substitution site of Ce atoms was studied using Raman spectroscopy. BTO has a crystal structure in which bismuth oxide layers, Bi2O2, are interleaved with perovskite (Bi2Ti3O10) blocks along c-axis. Therefore, there are two possible substitution sites of Ce in BTO, Bi2O2 layers and perovskite units. In the Raman spectroscopic study, the band appeared at 65 cm-1, which originated from the Bi atoms in the Bi2O2 layers, showed little variation with increasing amount of substituted Ce. However, the triple bands at 90, 119 and 148 cm-1, which were assigned to the Bi atoms in the perovskite units, became diffusive and shifted to higher frequencies. From these results, substitution sites of Ce were determined to be the perovskite units only. Structural refinement was carried out using neutron powder diffraction data. Lattice parameters along a-axis decreased from 5.4474 to 5.4353, 5.4217 and 5.4110 with increasing amount of substituted Ce from 0 to 0.25, 0.5 and 0.75. From the atomic displacements along a-axis, spontaneous polarization values were calculated. The calculated spontaneous polarization values were 30.98, 25.56, 18.70 and 13.41 for Ce content of 0, 0.25, 0.5 and 0.75, respectively. These results were compared with BCT thin films prepared by pulsed laser deposition technique. The BCT films showed similar spontaneous values to those of calculated. However, remnant polarization values were reduced because of random orientation of the films. The remnant polarization are largely dependent on the orientation because BTO has its almost polarization along a-axis. Among the BCT films, largest remnant polarization of 16.3 uC/cm2 was observed when x was 0.25 and annealed at 650 degrees. The film exhibited fatigue-free behavior until 1.36 X 10^10 read/write cycles.

D3.17
Ultra-Thin $PbZr_{0.2}Ti_{0.8}O_3$ Films Grown by MOCVD for Non-Volatile Memory Applications. S.Y. Yang[1], Florin Zavaliche[2], V. Nagarajan[1], Jun Ouyang[1], S. Prasertchoung[1], H. Zheng[1], R. Droopad[3], J. Yu[3] and R. Ramesh[4]; [1]Materials Science and Engineering, University of Maryland, College Park, Maryland; [2]Materials Research Science and Engineering Center, University of Maryland, College Park, Maryland; [3]Physical Science Research Laboratories, Motorola Laboratories, Tempe, Arizona; [4]Materials Science and Engineering, University of California, Berkeley, California.

The stringent need for high-density, high-speed, and low-power memory devices has prompted an immense interest in studying the size effects in ferroic systems. In parallel, current nonvolatile memory manufacturing processes require a scalable process such as metal-organic chemical vapor deposition (MOCVD) to deposit the ferroelectric layers. With this in mind, we have investigated the scaling of ferroelectric properties with film thickness in $PbZr_{0.2}Ti_{0.8}O_3$ (PZT) films grown on $SrRuO_3/SrTiO_3(001)$ by liquid delivery MOCVD. The PZT films are single crystalline, c-oriented, and show bulk-like properties for thicknesses above 20nm. We observe a progressive decrease in the ferroelectric polarization as well as the piezo-response as the thickness is decreased; films as thin as 3nm are piezoelectric. In this work, we present our interpretation of the origins of this decrease as well as results of the MOCVD processing studies. This work is supported by the NSF MRSEC under contract No. DMR-00-80008.

D3.18
UV Assisted Rapid Thermal Processing of Strontium Bismuth Tantalate (SBT) Thin Films. Shane O'Brien[1], Paul Hurley[1], Gabriel Crean[1], Jo Johnson[2], Concetta Caputa[3] and Dirk Wouters[2]; [1]NMRC, Cork, Ireland; [2]IMEC, Leuven, Belgium; [3]STMicroelectronics, Catania, Italy.

Ferroelectric thin films of Strontium Bismuth Tantalate (SBT) have been found to have excellent fatigue resistance, even after 10^{12}cycles. Consequently, the SBT material system is attracting considerable interest at present. One of the major challenges associated with the development of SBT based non-volatile memories is the integration of the ferroelectric films with established Si-based CMOS technologies. In particular, the thermal budget associated with the crystallisation of the SBT thin films (typically 700-800°C) can influence the performance of the underlying MOSFET, resulting in shifts in device parameters (e.g., Vt) and introducing the possibility of metallic contamination at the active device level. Consequently, it is of interest to develop processes which reduce the overall thermal budget necessary to achieve ferroelectric crystallisation and the required remnant polarisation (Pr). The objective of this work is to present the results of an ultra violet (UV) assisted rapid thermal processing (UV-RTP) technique for SBT ferroelectric crystallisation. The SBT samples examined in this work were deposited by thermal MOCVD at 385°C on Pt/TiO2/SiO2/Si substrates. The SBT film was formed from three precursors: Bi(thd)3, for Bi, Sr(thd)2pmdeta for Sr, and Ta(O-iPr)4(thd) for Ta. The SBT film thickness was 120nm. The annealing of the samples was performed in a UV RTP system, with KrCl* excimer lamps at 222 nm (5.8eV). The anneals were performed in atmospheric pressure O2, and the temperature ramp rates were in the range 35-40°C. The crystallisation anneal is a two stage process, with a 300s period at the deposition temperature, and the second stage at the maximum anneal temperature (Tmax: 610-750°C). Experiments were performed with UV irradiation during the rapid thermal process. For selected samples, the second stage of the anneal was performed in a conventional furnace (700°C, O2, 60 minutes). The comparative measurements presented are based on SBT samples (3cm x 3cm) taken from the same 200 mm wafer. FTIR absorbance data and electrical characterization data are presented for the SBT samples processed via the different irradiation strategies. Data were also obtained from samples where the second stage of the crystalisation anneal was performed in a conventional furnace (700°C, 60 minutes, O2). The effect of UV irradiation in UV-RTP annealing will be discussed in detail and optimum UV-assisted conditions for SBT crystallization will be presented.

D3.19
Thin Ferroelectric Film between Double Schottky Barriers. Lyuba A. Delimova[1], Igor V. Grekhov[1], Dmitri V. Mashovets[1], Sangmin Shin[2], June-Mo Koo[3], Suk-Pil Kim[3] and Youngsoo Park[3]; [1]Solid State Electronics Division, Ioffe Institute RAS, St.Petersburg, Russian Federation; [2]Material and Devices Laboratory, Samsung Advanced Institute of technology, Suwon, South Korea; [3]Process Engineering Laboratory, Samsung Advanced Institute of technology, Suwon, South Korea.

A metal/ferroelectric/metal (M/F/M) capacitor structure is one of the key elements of modern nonvolatile ferroelectric memory. The basic operations of a memory element are information writing, storage, and reading. These functions are executed by applying an external bias of different value and polarity to an M/F/M structure. Therefore, the ability to predict the behavior of M/F/M structure and

find the distribution of the electric field E(x), potential Ψ(x) and polarization P(x) in thin ferroelectric film as functions of bias V is of great importance. Due to the field dependence of polarization, the E(x) definition is complicated. So, a standard way to find the E(x), Ψ(x), and P(x) in an M/F/M structure is to self-consistently solve a well known set of differential equations. We propose a new approach allowing us to analyze the behavior of a thin-film uniform M/F/M structure and find the E(x), Ψ(x), and P(x) distributions across the film thickness as a function of bias and the film electrical history. We consider each Schottky barrier as an independent source of the electric field, therefore, the total field in a film is a superposition of the fields produced by each Schottky barrier. To avoid a self-consistent solution of equations, we use an artificial expedient: virtually enlarge the film thickness to a value which equals the total width of the space charge regions (SCR) produced by Schottky barriers. We set the point of origin in the middle of the ferroelectric at the edge of the SCRs, where E(x=0) = 0, Ψ(x=0) = 0, and select these values as the boundary conditions. Numerically integrating the Poisson equation on both sides of the point of origin, we find E(x) and Ψ(x) induced by the left (x < 0) and right (x > 0) barrier. Returning to a thin ferroelectric film, the algebraic sum of both thick-film E(x) yields a thin-film distribution E(x). Integrating thin-film E(x) yields a thin-film Ψ(x) for a zero bias. An external bias applied to the structure sets new surface potentials at M/F interfaces that are the boundary conditions for the definition of Ψ(x,V), E(x,V), and P(E) as functions of bias. The values of the Schottky barrier height, saturation and remnant polarization, and coercive field necessary for calculations are found from the current-voltage characteristics and hysteresis loops. We use this model to describe a M/F/M structure showing a non-symmetrical hysteresis loop (HL). For this, we fulfilled calculations for two sets of ferroelectric parameters and showed that the experimental HL agrees reasonably with the upper part of one calculated HL and the lower part of the other calculated HL. It confirms the possibility of the model to describe the studied structure. The non-symmetrical HL indicates a presence of a non-compensated charge within the ferroelectric. Using a transient current measurement, we can select the contribution of interface traps to the non-compensated charge.

D3.20

Layered Tunnel Barrier Lowering in Multilayer High-k Heterostructures using Bias-dependent Internal Photoemission Spectroscopy. Julie D. Casperson[2], Douglas Bell[1], Damon B. Farmer[3], Roy G. Gordon[4] and Harry A. Atwater[2]; [1]Jet Propulsion Laboratory, Pasadena, California; [2]Thomas J. Watson Laboratory of Applied Physics, California Institute of Technology, Pasadena, California; [3]Division of Engineering and Applied Sciences, Harvard University, Cambridge, Massachusetts; [4]Department of Chemistry and Chemical Biology, Harvard University, Cambridge, Massachusetts.

Layered tunnel barriers have been proposed as replacements for SiO_2 for use as injection barriers in nanocrystal floating-gate memories. Due to the predicted larger change in conductance as a function of injection voltage, such barriers are expected to enable nanosecond programming and erase times with archival data retention times. We have utilized internal photoemission (IPE) spectroscopy to study barrier height lowering of Al_2O_3/HfO_2/SiO_2/Si layered tunnel barrier structures over a wide range of applied biases. Dielectric stacks of Al_2O_3 and HfO_2 were grown on n-Si substrates by atomic layer deposition (ALD). Individual layers were nominally 15 nm thick, with actual thicknesses determined by transmission electron microscopy. In addition, an interfacial layer is observed between the high-k layers and the Si substrate; this layer is attributed to SiO_2 formed during the UV/ozone clean and is common at high-k/Si interfaces. In these experiments, the unintentionally grown SiO_2 interfacial layer acts as another dielectric layer and in fact contributes to barrier lowering under bias. The IPE results are analyzed using a simple electrostatic model to yield effective barrier heights and overall band alignments across the entire voltage range. This treatment includes transport of carriers from both the silicon substrate and the aluminum gate contact. Using this technique we demonstrate substantial barrier lowering (0.75 eV) for Si-compatible dielectric heterostructures, and we discuss the application of these barriers to improved speed and reliability of floating gate nonvolatile memory devices.

D3.21

Electron Tunneling through Ultra Thin Ferroelectric Films. Adrian Ion Petraru[1], Nicholas A. Pertsev[3], Rene Meyer[1], Valanoor Nagarajan[1], Juergen Brugger[4], Andreas Gerber[1], Juergen Schubert[2], Chun Lin Jia[1], Ulrich Poppe[1], Hermann H. Kohlstedt[1] and Rainer Waser[1]; [1]Institut fuer Festkoerperforschung and CNI, Forschungszentrum Juelich GmbH, Juelich, Germany; [2]Institut fuer Schichten- und Grenzflaechen and CNI, Forschungszentrum Juelich GmbH, Juelich, Germany; [3]A. F. Ioffe Physico-Technical Institute, St. Petersburg, Russian Federation; [4]EPFL, Lausanne, Switzerland.

Recent theoretical and experimental work showed that ferroelectricity exists down to a few unit cells thick epitaxial films under appropriate boundary conditions. In this work we present the relevance of electron tunneling through ultrathin ferroelectric films. We will present our development of so-called ferroelectric tunnel junctions with the following layer sequence: $SrTiO_3$(substrate)/$SrRuO_3$(electrode)/$BaTiO_3$ or $PbZr_xTi_{1-x}O_3$ (as ferro-electric)/$SrRuO_3$ or Pt as top electrode. The aim of our work is to study fundamental aspects of electron tunneling and electron transport through a ferroelectric material and the influence of the transport current on the ferroelectric polarization state of the barrier material. For thicknesses ranging between 240 nm and 8 nm common ferroelectric hysteresis loops were observed. For thinner barriers with the thickness ranging from 6 nm to 4 nm, the $I-V$ characteristics showed switching events with two resistive states. We will present a theoretical approach on the basis of the deformation potential model to combine the tunneling transfer matrix element with the strain state of the barrier. In addition the influence of the polarization state and the structure at the bottom and top interfaces will be discussed with respect to the tunnel barrier heights. The calculated $I-V$ curves will be discussed from the point of symmetry with the measured $I-V$ characteristics. Investigations on ultra thin $PbZr_{0.52}Ti_{0.48}O_3$ films are in progress, for film thicknesses in the range of 4 nm - 2 nm. Small area junctions of about 0.6 μm^2 having Pt as top electrode were fabricated using a Si_3N_4 stencil mask technique. $I-V$ measurements were performed in the temperature range of 180 K - 300 K by a conductive AFM technique.

SESSION D4/I7: Joint Session: Magnetoresistive Random Access Memory
Chairs: Russel Cowburn and Jon Slaughter
Wednesday Morning, December 1, 2004
Back Bay B (Sheraton)

8:30 AM *D4.1/I7.1

Magnetoresistive Random Access Memory. Johan Akerman, Philip Brown, Brian Butcher, Renu Dave, Mark DeHerrera, Mark Durlam, Brad Engel, Mark Griswold, Greg Grynkewich, Jason Janesky, John Martin, Srinivas Pietambaram, Nick Rizzo, Jon Slaughter, Ken Smith, Ji-Jun Sun and Tehrani Saied; Freescale Semiconductor, Chandler, Arizona.

Magnetoresistive random access memory (MRAM) employs a magnetoresistive device integrated with standard silicon-based microelectronics, resulting in a combination of qualities not found in other memory technologies: MRAM is non-volatile, has unlimited read and write endurance, and has demonstrated high-speed read and write operations. Recent technology developments of MRAM based on Magnetic Tunnel Junction (MTJ) devices is reviewed. The properties of our unique toggle-switching MRAM bit is discussed and compared to those of the conventional switching approach. For the first time a comprehensive review of the reliability of the MTJ tunneling dielectric and the current carrying write lines will be presented. Scaling of these results to operating conditions demonstrates the reliability of our 4Mb MRAM chip.

9:00 AM *D4.2/I7.2

Spin-Transfer Switching In Nanometer-Sized Magnetic Tunnel Junctions For MRAM Application. Yiming Huai, R & D Department, Grandis Inc., 1266 Cadillac Court, Milpitas, California.

Spin-polarized current induced magnetization switching has stimulated considerable interest in recent years due to its rich fundamental physics and great potential for new magnetoelectronic applications.[1] Low switching current density and high read signal are required for the application of the spin transfer switching to non-volatile magnetic memory (MRAM). We present here a study of spin transfer switching in nanometer-sized magnetic tunnel junctions (MTJs) with low resistance-area product (RA) ranged from 1-10 $\Omega\mu m^2$ and TMR=1-30%. Bottom PtMn and IrMn exchange-biased MTJ films were deposited in a magnetron sputtering cluster system. A thin tunneling barrier was formed by natural oxidation of the pre-deposited thin Al layer. MTJ films were subsequently patterned into nanometer ellipse shaped pillars using both deep UV lithography (combined with resist trimming)[2] and e-beam lithography. Spin-transfer switching has been consistently observed in patterned MTJs with dimensions down to 0.1x0.2 μm^2. Low switching current density Jc 10^6 A/cm^2 has been achieved using low moment free layer CoFeB. High TMR values about 30% were obtained in spin-transfer induced switching and attributed to homogenous and continues thin Al_2O_3 barrier grown on smooth bottom lead with a roughness (RMS) of 2-3 $\AA$. These result could have potential applications for a spin transfer based MRAM. [1] J. A. Katine, F. J. Albert, R. A. Buhrman, E. B. Myers, and D. C. Ralph, Phys. Rev. Lett. 84, 3149 (2000); J. Grollier, V.Gros, A. Hamzic, J. M. George, H. Jaffes, A. Fert, G. Faini, J. Ben Youssef, and H. Le Gall, Appl. Phys. Lett. 78, 3663 (2001); J. Z. Sun, D. J. Monsma, D. W. Abraham, M. J. Rooks, and

R. H. Koch, ibid. 81, 2202 (2002); M. R. Puffall, W. H. Rippard, and T. J. Silva, resistance ibid. 83, 323 (2003); S. Urazhdin, H. Kurt, W. P. Pratt, and J. Bass, ibid. 83, 114 (2003). [2] Yiming Huai, Frank Albert, Paul Nguyen, Mahendra Pakala and Thierry Valet, Appl. Phys. Lett. 84, 3118 (2004).

9:30 AM D4.3/I7.3

Magnetotransport in Flux-Closure Multilayered Nanomagnets. Fernando J. Castano, D. Morecroft, W. Jung and C. A. Ross; Materials Science and Engineering, Massachusetts Institute of Technology, Cambridge, Massachusetts.

During the last decade considerable attention has been devoted to the fabrication and characterization of thin film magnets with sub-micron lateral dimensions (nanomagnets). Multilayered nanomagnets can be engineered to exhibit large resistance changes depending on the relative orientation of the magnetization within each of the magnetic layers comprising the structure. This in turn allows for bits of information to be stored by controlling the magnetic configurations exhibited by these small elements. Present magnetic random access memory (MRAM) designs use large arrays of elongated nanomagnets which can be read and written using conductor lines [1]. Ring-shaped nanomagnets have been proposed as alternative MRAM cells [2], in part due to the existence of a range of stable magnetic configurations which could allow for high-density MRAM devices storing more than one bit per nanomagnet. The magnetotransport properties of ring-shaped single-magnetic-layer structures with widths of 200 nm and diameters exceeding 1 micron have previously been investigated [3]. In this contribution we report on the magnetic and magnetotransport properties of sub-micron diameter elliptical-ring magnets with widths of 90 nm and above. The rings are fabricated using single layer NiFe or Co, or NiFe (6 nm)/ Cu (3-6 nm)/ Co (4 nm) pseudo-spin-valve thin film structures. A multilevel lithography process involving electron-beam lithography and lift-off processing was used to fabricate magnetic rings with gold contacts. Magnetometry shows that single layer rings transform between onion (bidomain) and vortex (flux-closed) states, at switching fields which increase with decreasing ring diameter and ring width. For example, 360 nm diameter, 160 nm wide Co rings have an onion-vortex transition at 150 Oe and a vortex-reverse onion transition at 850 Oe, while the corresponding values for a 110 nm wide ring are 240 Oe and 1900 Oe. Resistance changes result only from anisotropic magnetoresistance of the material. In the case of multilayer rings, more complex magnetic behavior occurs because each layer has different switching fields, and magnetotransport effects originate from giant magnetoresistance in the structure. The magnetotransport properties reflect the different states within each magnetic layer, as well as the exchange and magnetostatic coupling between layers. In particular, the effects of varying the width of the rings and the thickness of the Cu spacer layer on the magnetic and magnetotransport behavior will be discussed. [1]S. Durlam et al, IEDM technical Digest 2004, session 34, paper#6. [2] J.G. Zhu et al, J. Appl. Phys. 87 6668 (2000). [3] M. Klaui et at, Phys. Rev. Lett. 90, Art. No.097202 (2003).

9:45 AM D4.4/I7.4

Size Dependent Properties of Current-Confined CPP Spin Valve Device. Hao Meng, Jianguo Wang, Yunfei Ding and Jian-Ping Wang; Electrical and Computer Engineering, University of Minnesota, Minneapolis, Minnesota.

Current-perpendicular-to-plane (CPP) spin valve device has the potential to replace the current-in-plane (CIP) device for high density magnetic recording head and other spintronics applications. In order to achieve its intrinsic high magneto-resistance (MR) ratio, the resistance coming from the active layers of CPP spin valve has to be increased [1]. Several approaches such as dual spin valve structure, nano-oxide layer, and new materials have been investigated by many groups. Another effective approach to increase the resistance is to reduce the current crossing area. In this work, size effects on the CPP spin valve were investigated. A series of samples with small pillar area (75×135 nm^2, 100×217 nm^2 and 184×415 nm^2 with ellipse shape) were fabricated in our lab. The processes include thin film sputtering, electron-beam lithography, ion milling etching and magnetic annealing. Nano-oxide-layers (NOL) were also introduced in the present work and functioning as current confine to further reduce the effective area for current passing through. With dot size decreasing, higher MR and MR ratio were achieved, which indicates that device is approaching to its intrinsic MR ratio with size decreasing. However, the results show a non-linear relationship between dot area and MR ratio. This is because that the conducting lead contact resistance in the MR measurement is still too high to be neglected, thus the spin valve active layer resistance couldn't dominate the measurement result, which causes MR ratio lower than the intrinsic value. Detail results will be presented in full paper. 1. Atsushi Tanaka, Yoshihiko Seyama, Arata Jogo, Hirotaka Oshima, Reiko Kondo, Hitoshi Kishi, Chikayoshi Kamata, Yutaka Shimizu, Shin Eguchi, and Kazuaki Satoh, "Readout Performance of Confined-Current-Path Current-Perpendicular-to-Plane Heads", IEEE Trans. Magn., 40, 203, (2004) Corresponding Author Email: jpwang@ece.umn.edu

SESSION D5: Nanoparticle Memories
Chairs: Alain Claverie and Dimitris Tsoukalas
Wednesday Afternoon, December 1, 2004
Back Bay B (Sheraton)

1:30 PM *D5.1

Semiconductor Nanocrystal Floating-gate Memory Devices. Panagiotis S. Dimitrakis and Pascal Normand; Institute of Microelectronics, National Center of Scientific Research "Demokritos", Aghia Paraskevi, Greece.

To overcome the limitations of the current nonvolatile semiconductor memory (NVSM) technologies and successfully respond to new market opportunities (e.g. portable devices) several novel fabrication routes are being actively investigated. These technological alternatives face tough requirements including low-power consumption, low-voltage operation, high-density and high-speed information storage. To meet these requirements, metal-oxide-semiconductor transistors using a high-density (10^{12} cm^{-2}) of laterally uncoupled nanocrystal dots with diameters of 5nm and below embedded in the gate dielectric have been proposed. As the optimum mean size of the NCs is below the current lithography resolution, an attractive approach to fabricate nanocrystals is through a self-assembling process. Among the different processing routes explored during the last few years the ion beam synthesis (IBS) technique has received substantial attention because of its flexibility and its manufacturing advantages. The potential of IBS for nanocrystals memory applications has been recently enhanced through the synthesis in the ultra-low-energy (ULE) regime (typically 1keV) of single silicon nanocrystals layers in thin SiO_2 films. In terms of structural possibilities, a combination of ULE-IBS conditions and oxide thickness allows for the formation of Si nanocrystals at a location from the SiO_2/Si interface that can be tailored for DRAM-like or EEPROM-like applications. Despite these attractive technological options, many fabrication issues remain to be solved before establishing a reliable process leading to reproducible memory devices. Charge neutralization, energy and impurity contamination during implantation, the effect of the post-implantation cleaning process, and the implantation-related oxide and SiO_2/Si interface damage are significant issues that will be outlined through an analysis of electrical data and their linkage to structural parameters. The overcoming of concerns pertaining to the aforementioned issues allows for the fabrication of competitive and reliable memory structures, as it will be demonstrated for the case of laboratory prototype NC-FG MOSFETs aiming at low-voltage non-volatile memory applications. Particular emphasis will be placed on our recent research development for integrating the ULE-IBS technique in a conventional 0.15μm flash memory technology. Finally, advantages and disadvantages of ULE-IBS relative to other synthesis techniques will be discussed.

2:00 PM D5.2

Manipulation of 2D-Arrays of Si Nanocrystals Embedded in a Thin SiO2 Layer by Low Energy Implantation. Caroline Bonafos[1], Gerard Benassayag[1], Sylvie Schamm[1], Hubert Coffin[1], Nikolay Cherkashin[1], Alain Claverie[1], Pascal Normand[2], Panagiotis Dimitrakis[2], Michele Perego[3], Marco Fanciulli[3], Torsten Mueller[4], Karl Heinz Heinig[4], Tence Marcel[5] and Christian Colliex[5]; [1]CEMES/CNRS, Toulouse, France; [2]Institute of Microelectronics NCSR Demokritos, Aghia Praskevi, Greece; [3]MDM/INFM, Agrate, Italy; [4]FZR Rossendorf, Dresden, Germany; [5]LPS, Paris Sud university, Orsay, France.

Silicon nanocrystal-based memories could potentially become an evolutionary replacement for the polycrystalline silicon used in conventional programmable flash memory for today electronic equipment. In silicon nanocrystal based metal-oxide-semiconductor (MOS) memory structures a fine control of the Si nanocrystals (ncs) location in the gate oxide is required for the pinpointing of optimal device architectures. In this work, we show how to manipulate and control the depth-position, size and surface density of two dimensional (2D) arrays of Si ncs embedded in thin (<10 nm) SiO2 layers, fabricated by ultra-low energy (typically 1 keV) ion implantation. Specific experimental methods have been developed to characterize these populations of ncs. They include Fresnel imaging for the measurement of the injection distance between the channel and the ncs band, spatially resolved Electron Energy Loss Spectroscopy (EELS) using the spectrum-imaging mode of a Scanning Transmission Electron Microscope (STEM) to measure the size distribution and density of the ncs population and Time-of-Flight Secondary Ion Mass Spectroscopy (ToF-SIMS) to measure the depth-distribution of excess silicon in the oxide layer. We have used all these techniques to study the influence of implantation and annealing conditions and oxide thickness on the characteristics of the ncs populations and understand

how they affect the charge storage properties of associated devices (capacitors and transistors). Finally, we show that the injection distance between the ncs band and the channel can be tuned from 10 to 2 nm by a judicious combination of ion beam energy and initial SiO2 thickness. This trade-off is the result of a competition between ion implantation, sputtering and interfacial mixing. The density of the ncs can be varied from 1011 to 3x1012/cm2 by increasing the ion dose. Annealing under slightly oxidizing ambient has been found essential for the optimization of the memory properties of the devices. During such oxidations, the oxide integrity is restored, the ncs are passivated and a separation of connected ncs takes place, making possible a further increase of the ncs density and a decrease of their mean size. Both EEPROM-like and NVRAM-like transistors have been fabricated following this route. Their characteristics will be discussed in relation with the characteristics of the 2D arrays of ncs on which they rely. These devices show comparable data retention and endurance characteristics than the actual SONOS-like structures and appear as very attractive in the future for deep submicron CMOS technology.

2:15 PM D5.3
Chemical Vapor Deposition of Ge Nanocrystals on HfO_2 for Nonvolatile Memory Device Application. Ying Qian Wang, Jing Hao Chen, Won Jong Yoo and Yee-Chia Yeo; Electrical and Computer Engineering, National University of Singapore, Singapore, Singapore.

Flash memory devices employing nanocrystals (NCs) have drawn considerable attention as one of the most promising candidates for future nonvolatile, high density, and low power memory IC application. By using a high-k dielectric in place of the conventional SiO_2 based dielectric, NCs flash memory can achieve significantly improved programming efficiency and data retention. To date, there is limited work on the integration of high-k dielectric materials with NCs, especially Ge nanocrystals embedded in HfO_2. In this study, chemical vapor deposition (CVD) of germanium nanocrystals using GeH_4 gas directly on hafnium oxide is investigated. Atomic force microscopy (AFM), X-ray diffraction (XRD), and X-ray photoelectron spectroscopy (XPS), and second electron microscopy (SEM) were utilized to characterize the Ge nanocrystals. The dependence of the Ge nanocrystal size and density on deposition temperature, deposition time (10 s to 40 s), and flow rate (60 sccm to 120 sccm) was explored. It was found that the formation of Ge nanocrystals on HfO_2 does not substantially occur at temperatures below 550°C, but becomes significant at 600°C. At a deposition temperature of 600°C, with increasing deposition time, the NC size initially increases and then decreases, while the NC density follows the opposite trend. The NC size and density also depend on the GeH_4 gas flow rate. The tradeoff between amount of available gas reactant and gas residence time results in a maximum NC density at a flow rate of 80sccm. In this experiment, the largest Ge NC density achieved is $10^{11}cm^{-2}$, with a mean NC diameter of about 16nm. A MOS capacitor with CVD Ge NCs embedded in HfO_2 was fabricated. For comparison, a control capacitor with HfO_2 dielectrics but without Ge NCs was also fabricated. Capacitance-voltage characteristics of the capacitors were measured by counter-clockwise scanning from -6V to 6V and then 6V to -6V to see the memory effect., The control sample shows a 0.5V hysteresis, which may be attributed to traps in the HfO_2 dielectric. On the other hand, the Ge NC device shows a 2V hysteresis. The difference in hysteresis behavior indicates that Ge NCs actually contribute significantly to the memory effect.

2:30 PM D5.4
Characterization of Number Fluctuations in Gate-last Metal Nanocrystal Nonvolatile Memory Array Beyond 90nm CMOS Technology. Chungho Lee, Udayan Ganguly and Edwin C. Kan; Electrical and Computer Engineering, Cornell University, Ithaca, New York.

Fluctuation on number of nanocrystals in a small MOS gate area poses one of the main bottlenecks for the scalability of nanocrystal-based nonvolatile memories [1-3] beyond 90nm CMOS technology. If the nanocrystal formation or deposition is done before the gate stack patterning in a self-aligned source/drain process, there needs to be at least 100 nanocrystals within the effective gate area to control the number fluctuation below 10%. For typical nanocrystal diameter and spacing around 3-4nm, the effective gate area will be larger than 80nm by 80nm to satisfy the parametric yield requirements. This number fluctuation problem in gate area scaling can be much alleviated by the gate-last MOS process [4] where nanocrystal self-assembly is performed after the gate patterning. Self-alignment of source and drain can still be achieved through a dummy gate replacement. Due to the additional surfaces at the side-walls and corners in the effective gate area seen by the metal atoms, physical self-assembly of nanocrystals from wetting layers will preferentially be uniform away from the perimeter by interface energy minimization, and significantly reduce number fluctuations in the arrays of nonvolatile memory devices. In this paper, we experimentally characterize the statistics of number fluctuation, the size distribution, and the correlation of the size and number density in gate patterns with various feature sizes from 30nm to 250nm. The dummy gate regions with 50nm oxide wall are defined by e-beam lithography and RIE (Reactive Ion Etching). Metal nanocrystals of Au, Ag, and Pt are formed on 2.5nm tunneling oxide by direct-deposit self-assembly (i.e., evaporation and post-annealing) in the gate stack. As a tight control of nanocrystals in the confined gate regions, various process parameters (i.e., initial film thickness, annealing temperature, etc.) [5, 6] are investigated and optimized. The statistical evaluation of metal nanocrystal formation is performed by SEM and STEM. References: 1. H. I. Hanafi, S. Tiwari, and I. Khan, IEEE Trans. Electron Devices 43, 1553 (1996). 2. Z. Liu, C. Lee, V. Narayanan, G. Pei and E. C. Kan, IEEE Trans. Electron Devices 49, 1606 (2002). 3. C. Lee, A. Gorur-Seetharam and E. C. Kan, IEDM, 2003, p. 557. 4. O. C. Chi, H. Kim, J. P. McVittie, B. B. Triplett, P. C. McIntyre and K. C. Saraswat, ISDRS, 2003, p. 464. 5. Z. Liu, C. Lee, G. Pei, V. Narayanan and E. C. Kan, MRS, 2001, p. A5.3.1. 6. C. Lee, Z. Liu and E. C. Kan, MRS, 2002, p.F8.18.1.

3:15 PM D5.5
Reliable, Fast and Long Retention Si Nanocrystal Non-Volatile Memories. Josep Carreras, B. Garrido, J. Arbiol and J. R. Morante; Electronics, University of Barcelona, Barcelona, Barcelona, Spain.

We report in this work a Si-nanocrystal (Si-nc) MOS memory which shows, at the same time, fast writing times and long charge retention. This has been achieved by optimizing a structure reported previously that exhibited excellent retention characteristics. For the new structure, 15 keV Si ions have been implanted in a 40 nm thick oxide at high doses in order to obtain Si excess ranging from the 10 to the 20 atomic % at projected range (25nm). An annealing step at 1100 °C has been performed to precipitate the nanocrystals. We show that there is a Si excess compromise (density depth profile of Si-nc) in which write times are improved at least 3 orders of magnitude (in the submillisecond range) while still maintaining a virtually infinite retention time. Such behaviour has been correlated with the structural characterization by EFTEM, which reveals a control oxide completely free of Si-nc and thick enough (11 nm) to prevent tunnelling from/to the gate electrode. The Si-nc are located around the projected range and they show a mean size of 2.6 ± 0.2 nm. The tunnel oxide is not completely free of Si-nc or clusters, as observed by EFTEM, but there is a significant reduction in mean size and density when approaching to the p-type substrate. We believe that these small Si-nc or clusters in the tunnel oxide play an outstanding role in improving the performance of the devices. For charging (writing), when a gate bias is applied to the structure, these clusters assist like traps when tunnelling to the central region. On the contrary, when the Si-nc are already charged, these nanoclusters do not contribute to favour the discharge process as they have larger band-gaps (due to quantum confinement) than the bigger Si-nc in the center of the layer, thus not being energetically favourable for the stored charge to back-tunnel. This simple model, based on the correlation of the most important electrical memory parameters and the structural information, has helped us to understand the importance of the implantation dose as a technological parameter when a trade-off between write and retention times is required. For our samples, this dose is about of 15% Si excess. Finally, endurance tests have been performed, showing a completely flat and stable programming window after 10^6 Write/Erase programming pulses.

3:30 PM D5.6
Local Self-Order Observed During Chemical Vapor Deposition of Silicon Quantum Dots for Application in Nanocrystal Memories. Rosaria A. Puglisi[1], Salvatore Lombardo[1], Giuseppe Nicotra[1], Corrado Spinella[1], Cosimo Gerardi[2], Barbara De Salvo[3], Luca Perniola[4] and Giuseppe Iannaccone[4]; [1]Istituto per la Microelettronica e i Microsistemi, Consiglio Nazionale delle Ricerche, Catania, Italy; [2]STMicroelectronics, Catania, Italy; [3]CEA-LETI, Grenoble, France; [4]Universita' di Pisa, Pisa, Italy.

Si quantum dots have been obtained by chemical vapor deposition of silane on silicon dioxide and implemented in a flash-like memory device. The dot formation process has been studied in the regime of the sub-monolayer depositions and of surface coverages of about 20 - 30%. Several substrate temperatures, post-deposition annealing temperatures, and substrate preparation conditions have been studied. Energy filtered transmission electron microscopy with very high spatial and chemical resolution is adopted to evaluate the dot size and inter-dot distance distributions. It is shown that the nucleation process, though continuous under typical deposition conditions, is not a random process. The dots appear separated by Si-free denuded zones, due to the silicon adatom capture mechanism. The dot size is shown to scale with the size of its own capture zone. The effect will be discussed in the framework of a scaling model, based on a modification of the classical Voronoi tessellation approach [1]. In nanocrystal memory devices, it has been proposed that the

dispersion from cell to cell of the surface fraction (Fdot) covered with Si dots in the gate area is the main limitation for nanocrystal memory scaling [2]. This dispersion affects the threshold voltage (VT) distribution in the nanocrystal memory array. In the presence of a non-random dot nucleation, with Si-free capture zones around each dot, the dispersion of the Fdot distribution is shown to be lower compared to the case of fully random nucleation. This difference is quantified, compared to data, and extrapolated to small gate area values. [1] R.A. Puglisi et al., Surface Science (2004) [2] B. DeSalvo et al., IEDM Int. Electron. Dev. Meeting Proc. (2003)

3:45 PM D5.7
A Model of Silicon Nanocrystal Nucleation and Growth on SiO_2 by CVD. Matthew W. Stoker, Tushar P. Merchant, Rajesh Rao, Ramachandran Muralidhar, Sherry G. Straub and Bruce E. White; Advanced Products Research and Development Laboratory (APRDL), Freescale Semiconductor Inc., Tempe, Arizona.

Silicon nanocrystals can be used in non-volatile memory devices to reduce susceptibility to charge loss via tunnel oxide defects, allowing scaling to smaller sizes than possible with conventional Flash memory technology. In order to optimize device performance, it is desirable to maximize the nanocrystal density and surface coverage, while maintaining sufficient inter-crystallite separation to limit electron tunneling between adjacent crystallites. Ideally, crystallite densities in excess of $10^{12}/cm^2$ with relatively narrow particle size distributions must be obtained, posing a significant challenge for process development and control. In order to facilitate development of such a process, a rate-expression-based model has been developed for the nucleation and growth of silicon nanocrystals on SiO_2 in a CVD process. The model addresses the phenomena of nucleation, growth, and coalescence and includes the effects of exclusion zones surrounding the growing nuclei. The model uses a phenomenological expression to describe the nucleation rate and assumes that following nucleation, crystallite growth is dominated by gas-phase deposition processes, analogous to CVD of polycrystalline silicon. The model-predicted time-evolutions of crystallite densities and crystallite size distributions are consistent with experimental distributions as measured by Scanning Electron Microscopy (SEM). By coupling the model to a reactor-scale model of polysilicon CVD, it is possible to predict variations in the crystallite size distributions at various locations across a wafer as a function of reactor settings (temperature, pressure, flow rates, etc.). This in turn can be used for process control and optimization in order to ensure uniform deposition of nanocrystals in a large-scale manufacturing environment.

4:00 PM D5.8
Monte Carlo Simulations of Silicon Nanocrystals in an Insulator Matrix. George Hadjisavvas and Pantelis C. Kelires; Physics Department, University of Crete, Heraclion, Crete, Greece.

Si nanocrystals (nc) embedded in an insulator matrix, usually a-SiO_2, have been extensively studied in recent years because of their photoemission and nonvolatile memory properties. Possible sources of light emission are proposed to be the quantum confinement and localized surface states. The latter are also believed to be a key factor for the memory properties. However, some important issues remain unclear. For example, since confinement depends on the size and density of the nanocrystals, it is essential to know their stability in the amorphous matrix as they become smaller. Also, the atomic structure of the interface, i.e., kind and proportion of bonds, is a crucial paremeter, yet it is not well known. We present here results of Monte Carlo simulations which shed light onto these issues. We consider Si nanocrystals in amorphous silicon dioxide. In our approach, the generation of the embedding a-SiO_2 structure is achieved via a modified Wooten-Winer-Weaire method. Starting from crystalline beta-cristobalite, the network is amorphized through bond-breaking and switching moves. The Si nc is positioned at the center of the cell. The energies are calculated using the Keating potential. We introduce novel bond-conversion moves of the type Si-Si to Si-O-Si, and vice versa. This allows us to study interdiffusion in the system. We find a significant proportion of Si-O-Si bridge bonds at the interface, not considered previously. A penetration of oxygen into the nc, limited to few Angstroms, is observed. The interface has a non-abrupt nature. From an oxidation-number analysis, it comes out that its width is about seven Angstroms. The energetics show that this region is highly strained, and that the stability of the nc's increases as their size increases and when they approach each other (formation of a dense array.) We found a critical diameter of 1.5 nm, below which the nc's are unstable. This is accompanied by heavy deformation and oxidation of the core of the nc. Spherical and faceted nc's of the same size have about equal energies. We are currently examining the nanocrystal nucleation process in the amorphous matrix.

4:15 PM D5.9
Characterization of Electronic Charged States of Silicon Nanocrystals as a Floating Gate in MOS Structures. Seiichi Miyazaki[1], Taku Shibaguchi[1] and Mitsuhisa Ikeda[2]; [1]Graduate School of Advanced Sciences of Matters, Hiroshima University, Higashi-Hiroshima, Japan; [2]Research Center for Nanodevices and Systems, Hiroshima University, Higashi-Hiroshima, Japan.

Discrete charged states in Si quantum dots (QDs) embedded in SiO_2 is a crucial factor for multivalued memory operations of Si-QDs floating gate MOS devices. We have studied capacitance-voltage and transient current-voltage characteristics of MOS capacitors with Si-QDs floating gate in dark and under visible light illumination at room temperature to gain a better understanding of discrete charged states of the Si-QDs floating gate. ~3nm-thick SiO_2 as a tunnel oxide layer was first grown on p-type and n-type Si(100) at 1000°C in 2%O_2 diluted with N_2. Hemispherical Si nanocrystals as QDs were self-assembled on the tunnel oxide by LPCVD using SiH_4 at 575°C. The areal dot density and the average dot height were controlled at $2.5x10^{11}cm^{-2}$ and 8nm, respectively. After the dot surface oxidation at 850?C in 2% O_2 diluted with N_2, a 7.5nm-thick control oxide was formed by conformal deposition of a 3.3nm-thick amorphous Si layer by LPCVD using 10% Si_2H_6 diluted with He at 440°C and complete oxidation of the Si layer at 1000°C in 2% O_2 diluted with N_2. Al-gates with a size of 1mm in diameter were formed for MOS capacitors. Capacitance-voltage (C-V) characteristics of Al-gate MOS capacitors on p-type and n-type Si(100) show unique hystereses due to the charging and discharging of the Si-QDs floating gate with a symmetric patter reflecting the Fermi level of the substrate. This confirms that the undoped Si-QDs floating gate acts as a storage node for both electrons and holes. Namely, the contribution of traps with a specific energy state to the observed C-V hystereses can be ruled out. For each of high-frequency C-V curves measured in dark, a single capacitance peak appears only around a flat-band voltage condition, which is attributed to the quick flat-band voltage shift caused by the collective emission of charges (electrons in the MOS capacitors on p-Si(100) or holes in the MOS capacitor on n-Si(100)) retaining in the Si-QDs floating gate as confirmed from the corresponding transient current peak. Under visible light illumination, another capacitance peak due to collective injection of charges (electrons in the MOS capacitors on p-Si(100) or holes in the MOS capacitor on n-Si(100)) to the electrically neutral Si-QDs floating gate becomes observable in a weak-inversion condition as a result of photogenerated carriers (electrons in p-Si(100) or holes in n-Si(100)) in the vicinity of the area masked with the Al gate flow into beneath the gate oxide. Acknowledgements: This work was supported in part by Grant-in Aids for scientific research of priority area (A) and for the 21st Century COE program //Nanoelectronics for Tera-bit Information Processing// from the Ministry of Education, Science, Sports and Culture of Japan.

4:30 PM D5.10
Modeling of Capacitance of Silicon Nano-Crystals in MOS Structure. Thottam S. Kalkur, David Hess and Bo Lojek; Dept. of Electrical and Computer Engineering, University of Colorado at Colorado Springs, Colorado Springs, Colorado.

Non-volatile memories based on silcon nano-crystals are attracting the attention of many investigators because of their superior retention and endurance characteristics to conventional floating gate structures. The capacitance versus voltage characteristics of the nano-crystal based MOS structures must be known accurately in order model the memory element. Typical capacitance calculations assume symmetry between the conducting surfaces, zero electric field inside the conducting surfaces and dimensions that allow for negligible fringing electric field effects. In this paper, the capacitance of the nano-crystals are calaculated using standard electrostatic methods. The calculated results were compared with the commercially available 3-dimensional field solvers (Ansoft tools). The models are used to predict the effects of charge, tunnel oxide thickness, and fringing fields on capacitnace.

SESSION D6: Poster Session: Materials for Nonvolatile Memories
Chairs: Caroline Bonafos and Panagiotis Dimitrakis
Wednesday Evening, December 1, 2004
8:00 PM
Exhibition Hall D (Hynes)

D6.1
Improved Size Dispersion of Silicon Nanocrystals Grown in a Batch LPCVD Reactor. Yuet Mei Wan[1], Kees van der Jeugd[1], Thierry Baron[2], Barbara De Salvo[2] and Pierre Mur[2]; [1]ASM, Leuven, Belgium; [2]CEA-DRT-LETI, Grenoble, France.

Nanocrystal memories are widely invoked as potential solutions to overcome the scaling limitations of conventional FLASH memories beyond the 80nm technology node. In this study, the deposition of uniform silicon nanocrystals has been developed and optimized in a commercially available vertical batch furnace, an A400 from ASM. It

has been shown that low pressure chemical vapor deposition (LPCVD) of nanocrystals is feasible in a batch reactor but with a large size dispersion of the silicon nanocrystals. To improve the size dispersion of the nanocrystals, a novel 2-step process with silane was introduced. In the conventional 1-step process, the oxide surface is exposed to silane at the same partial pressure and temperature during both nucleation and growth of the silicon nanocrystals. In this novel 2-step process, the surface is first exposed briefly to silane at a higher temperature (580-600oC) and following that, the temperature is lowered to allow selective growth on the existing silicon nuclei over the oxide surface. With such an approach, the nucleation step can be separated from the growth step and consequently the size dispersion can be improved by a factor of 2. These nanocrystals have been incorporated onto device wafers and the electrical data will be collected and presented, along with the SEM and ellipsometry results.

D6.2

Ge Nanocrystals in MOS-Memory Structures Produced by Molecular-Beam Epitaxy and Rapid-Thermal Processing.

Arne Nylandsted Larsen[1], A. Kanjilal[1], John L. Hansen[1], Peter Gaiduk[1], Pascal Normand[2], Panagiotis Dimitrakis[2], Dimitris Tsoukalas[2], Nikolay Cherkashin[3] and Alain Claverie[3]; [1]Institute of Physics and Astronomy, University of Aarhus, Aarhus, Denmark; [2]Institute of Microelectronics, NCSR Demokritos, Athens, Greece; [3]CEMES/CNRS, Toulouse, France.

A considerable attention is presently focused on semiconductor nanoparticles embedded into the silicon oxide of a MOSFET device for future high speed and low power consuming logic and memory devices, and a variety of fabrication procedures and structures are being tested. We have developed a new method of forming a sheet of Ge nanocrystals in a SiO2 layer based on molecular beam epitaxy (MBE) and rapid thermal processing (RTP)[1−3]. The method is, among other things, distinguished by giving sharp distributions of nanocrystal-size and tunneling-oxide thickness. The method takes advantage of the very high precision by which a very thin Ge layer can be deposited by MBE. This Ge layer is first deposited by MBE on a thermally grown SiO2 layer on a (001) Si wafer, followed by MBE deposition of a Si capping layer. The structure is subsequently oxidized by RTP in an oxygen ambiance followed by a reduction process at elevated temperature in a nitrogen ambiance. With proper choice of process parameters the nanocrystal size can be varied between 3 and 8 nm and the aerial density between approximately $1x10^{11}$ and $1x10^{12}$ dots/cm^2. The tunneling oxide thickness is determined by the thickness of the thermally grown SiO2 layer, and is typically 4 nm. C-V measurements of MOS capacitors reveal hole and electron injection from the substrate into the nanocrystals. Memory windows of about 0.2 and 0.5 V for gate-voltage sweeps of 3 and 6 V, respectively, are achieved. 1 "Structural and electrical properties of silicon dioxide layers with embedded germanium nanocrystals grown by molecular beam epitaxy"; A.Kanjilal, J. Lundsgaard Hansen, P.Gaiduk, A.Nylandsted Larsen, N.Cherkashin, A.Claverie, P.Normand, E.Kapelanakis. D.Skarlatos and T.Tsoukalas, Appl.Phys.Lett. 82, 1212 (2003) 2 "Size and aerial density distributions of Ge nanocrystals in a SiO2 layer produced by molecular beam epitaxy and rapid thermal processing"; A. Kanjilal, J. Lundsgaard Hansen, P. Gaiduk, A. Nylandsted Larsen, P. Normand, P. Dimitrakis, and D. Tsoukalas, N. Cherkashin and A. Claverie, to be publ. in Appl.Phys.A 3 "Method for production of a layered structure with nanocrystals in dielectric layer"; A.Nylandsted Larsen, J.Lundsgaard Hansen, P.Gaiduk, and K.-H.Heinig, PCT Request, 2003

D6.3

Investigation of Programming Voltage Scaling in Memory Devices using SiGe Nanocrystals.

Rohit Gupta[1], S. K. Samanta[1], Won Jong Yoo[1], Ganesh Samudra[1], Daniel Chan[1], L. K. Bera[2] and N. Balasubramanian[2]; [1]Electrical and Computer Engineering, National University of Singapore, Singapore, Singapore; [2]Institute of Microelectronics, Singapore, Singapore.

It is well understood that distributed floating gates of semiconductor can be an alternate solution for scaling of the conventional memory devices. Where SiO_2 is being used as a tunneling barrier, which has a high barrier height, voltage scaling is difficult. However, high-k dielectrics as tunneling/control dielectrics ensure further reduction of programming and erase voltages due to low tunneling barriers. In this research SiGe nanocrystals (NC) by LPCVD were used to fabricate memory transistors with HfO_2 (as well as SiO_2) tunneling / control dielectrics and TiN as metal gate. NCs were first deposited on HfO_2 and SiO_2 and characterized by atomic force microscopy (AFM), Auger electron spectroscopy (AES), x-ray photoelectron spectroscopy (XPS), cross-sectional TEM (X-TEM), and Raman spectroscopy methods. With AFM studies it was found that at lower pressures (0.5Torr) the properties of dielectric substrate do not seem to play a major role in SiGe NC deposition from the fact that the density, distribution, and minimum size are roughly the same. Meanwhile, material composition depends on the deposition pressure, deposition time, substrate temperature, and on underlying substrate material (nucleation site density) as measured by AES, AFM. The XPS analysis reveals that, in SiGe NCs there are various oxidation states of Ge up to +4 but Si is found to have only zero oxidation state. Multiple oxidation state of $Ge^{(0to+4)}$ alloyed with Si^0 can lead to various defects in NCs, which can be discrete charge storage nodes in memory devices. The cross-sectional TEM picture shows the presence of, partially crystalline and electrically isolated, SiGe NCs embedded in SiO_2 and HfO_2. Memory effects were clearly observed at room temperature from floating gate MOSFET devices: threshold voltage shift of about 0.8 V, with electrical stress of $V_{gs} = +6V$ for 1s in HfO_2 devices. However, the same threshold voltage shift was obtained with $V_{gs} = +18V$ for 10s for SiO_2 memory transistors. Experimental conditions to simulate the Channel Hot Electron (CHE) and Fowler Nordheim (FN) programming mechanisms were tested for various gate and drain voltages to investigate the effects of isolation of nanocrystals on programming speed. It was found that programming using CHE is faster than that using FN. Furthermore, we demonstrate that CHE programming can be an interesting feature to result in multilevel charge storage.

D6.4

Synthesis and electrical characterization of a MOS memory containing Pt nanoparticles deposited at a SiO_2/ HfO_2 interface.

Christos Sargentis[1], Konstantinos Giannakopoulos[2], Anastasios Travlos[2] and Dimitris Tsamakis[1]; [1]Electrical and Computer Engineering, National Technical University of Athens, Athens, Greece; [2]Institute of materials Science, National Centre for Scientific Research "Demokritos", Ag. Paraskevi Attikis, Athens, Greece.

MOS memory devices containing semiconductor nanocrystals have drawn considerable attention recently, due to their advantages when compared to the conventional non-floating memories [1]. At the same time is only a little work done on memory devices containing metal nanocrystals[2,3] despite the fact that this would have given them many advantages in comparison with devices based on semiconductor nanocrystals. The main aim of these efforts is to increase the retention time of carriers within the nanocrystals, without increasing the power consumption of the device and without decreasing the time of write-erase process. By using metal nanocrystals we have in our disposal a large variety of work functions and it is easier to tradeoff between the speed of write-erase process and the charge retention time. In this work we describe the fabrication of a MOS memory with embedded Pt nanoparticles in the SiO_2/ HfO_2 interface of a MOS device. We chose to work with Pt nanocrystals due to the fact that they have a large work function. In addition, using as upper oxide a high-k oxide our device, has a great degree of scalability. On n-Si (100) wafers we deposited 3,5 nm of SiO_2 (tunnel oxide) using Chemical Vapor Deposition. On top of this surface we deposited a very thin (1 nm) platinum (Pt) layer. Separate Pt nanoparticles of high density were formed. Then we evaporated HfO_2 oxide with a second electron gun at 200 ° C in a oxygen rich ambient, so that this oxide becomes as stoihiometric as possible. The above device shows a clear hysteresis behavior on C-V characteristics. No hysteresis was observed in similar samples that did not contain nanocrystals. References: 1) S. Tiwari et al. ,Small silicon memories:confinement, single-electron, and interface state considerations, Appl. Phys.A 71, p.403-414 (2000) 2) Z. Liu et al.,Metal nanocrystals memories.Part I:Device, design and fabrication, IEEE transactions on electron devices vol. 49 (9),p.1606-1613, September 2002 3) Q. Wang et al. ,Sinthesis and electron storage characteristics of isolated silver nanodots on/ embedded in Al_2O_3 gate dielectric, article in press Applied surface Science (2004)

D6.5

Zn Nanocrystal Formation by Photo-MOCVD Method.

Keein Bang, Sangsu Kim, Seungyup Myong and Koengsu Lim; Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea.

Recently, nanocrystal memories employing discrete traps as a charge storage media have attracted a lot of research attention as the promising candidates to replace conventional DRAMs or Flash memories. Until now, for nanocrystal floating gate memory fabrication, most researches are focused on Si or Ge nanocrystal memories. However, in order to maintain good retention characteristics in Si or Ge nanocrystal memories, the programming voltages cannot be scaled down easily. Interface and dopant fluctuations at the Si/Ge nanocrystal interface also cause device design difficulty. On the other hand, metal nanocrystals have many advantages over the semiconductor counterparts including high density of states around the Fermi level, stronger coupling with the conduction channel, a wide range of available work functions, and smaller energy perturbation due to carrier confinement. Metal nanocrystals also provide a great degree of scalability for the nanocrystals size. However, most researches to fabricate metal nanocrystals are concentrated on evaporation or sputtering method,

followed by thermal annealing. These methods are complicated and time-consuming. In this paper, new method for metal nanocrystal fabrication will be introduced by using Zn with the photo-MOCVD (Metal-Organic Chemical Vapor Deposition) method. Photo-MOCVD is based on photo-chemical process involving photo-dissociation. The photon wavelengths emitted from the mercury light source are 184nm and 254nm. In this system diethylzinc (DEZ) which is liquid source is used to fabricate Zn nanocrystal and decomposed by the UV source. DEZ source is heated in the thermostat to 20 ° C and carried from source cylinder to the reactant chamber by Ar carrier gas. Fundamentally it is not physical vapor deposition but chemical vapor deposition method. Hence, there are several parameters to adjust for optimal condition such as chamber pressure, flow rate of carrier gas and substrate temperature. In the experiment, DEZ thermostat was set to 20 °C, substrate temperature was set to 150 °C and flow rate of carrier gas was changed from 20 sccm to 50 sccm. Thereafter, Zn nanocrystal shape was investigated with the process time varied. AFM (Atomic Force Microscope) and SEM (Scanning Electron Microscope) were used to identify the Zn nanocrystal. As a result, dense Zn nanocrystals were obtained when the chamber pressure was 2 Torr, the substrate temperature was set to 150 °C, flow rate of carrier gas was set to 30 sccm, and the process time was 1 min. Dense Zn nanocrystals fabricated by photo-MOCVD can be easily applied to the Zn nanocrystal memory.

D6.6

Oxidation of Si nanocrystals obtained by low energy ion implantation in a thin SiO2 layer. Hubert Coffin[1], Caroline Bonafos[1], Nikolay Cherkashin[1], Sylvie Schamm[1], Gerard Ben Assayag[1], Gerald Zanchi[1], Panagiotis Dimitrakis[2], Pascal Normand[2], Marcel Tence[3], Christian Colliex[3] and Alain Claverie[1]; [1]CEMES-CNRS, Toulouse, France; [2]Institute of Microelectronics NCSR Demokritos, Aghia Praskevi, Greece; [3]Laboratoire de Physique des Solides, Orsay, France.

Performance and scalability of non-volatile memories can be improved by new devices based on Multi-dot Floating Gate MOSFETs where Si nanocrystals embedded in a thin oxide are used as charge storage elements. In this work, we report on a systematic study of the nucleation and oxidation of the Si dots fabricated by ultra-low energy (1keV) ion implantation followed by thermal annealing. Annealing under slightly oxidizing ambient has been found essential for the optimization of the memory properties of the devices. Specific experimental methods have been developed to characterize the population of ncs. They include Fresnel imaging for the measurement of the injection distance between the channel and the ncs band and spatially resolved Electron Energy Loss Spectroscopy (EELS) using the spectrum-imaging mode of a Scanning Transmission Electron Microscope (STEM) to measure the size distribution and density of the ncs population. We have used all these techniques to study the influence of implantation and annealing conditions on the characteristics of the ncs populations. After an annealing under N2 we observe the formation of ncs only for doses sufficiently high (> 5.1015 cm-2). For a dose of 1016 cm-2 a high density of spherical ncs is observed by EFSTEM and for the highest implanted dose (2x1016 cm-2) coalescence of the ncs takes place. On the other hand, we show that during the oxidation (under N2+O2), the oxide integrity is restored, the ncs are passivated and a separation of connected ncs takes place, making possible a further increase of the ncs density and a decrease of their mean size. After a long time annealing the SiO2/Si interface is also oxidized. The ncs oxidation results in an expansion of the SiO2 layer which only concerns the control oxide for short annealing times and reaches the injection oxide for longer annealing durations, when interface oxidation also takes place. Finally, an extended spherical Deal-Grove model for self-limiting oxidation to fabricated silicon ncs is presented. It proposes that the stress effects, due to oxide deformation, slows down the chemical oxidation rate and leads to a self limiting oxide growth. The model results are in good agreement with the experimental data. Electrical measurements of associated devices show strong charge storage effects at low gate voltages and enhanced charge retention times are observed for the oxidised samples. These results indicate that a combination of low-energy silicon implants and annealing in diluted oxygen allows for the fabrication of improved low-voltage nonvolatile memory devices.

D6.7

Gold Langmuir-Blodgett Deposited Nanoparticles for Non-Volatile Memories. Panagiotis S. Dimitrakis[1], Stavroula Koliopoulou[1], Dimitris Tsoukalas[2], Pascal Normand[1], Shashi Paul[3], C. Pearson[3], A. Molloy[3] and M. C. Petty[3]; [1]Institute of Microelectronics, National Center of Scientific Research "Demokritos", Aghia Paraskevi, Greece; [2]School of Applied Sciences, Nattional Technical University of Athens, Zografou, Greece; [3]Centre for Molecular and Nanoscale Electronics, University of Durham, Durham, United Kingdom.

Metallic or semiconducting nanoparticles are under investigation as charge storage elements to replace the continuous polysilicon layer of EEPROM devices. One challenging aspect remains the method of formation of the nanoparticles and its integration with silicon technology. We have recently demonstrated that gold nanoparticles deposited by the Langmuir-Blodgett (LB) technique within the insulator of an MIS capacitor show a memory effect due to charge storage [1]. In this work, we investigate the integration and resulting electrical properties of a MISFET device that incorporates a monolayer of LB-deposited organically passivated gold nanoparticles as floating gate dot elements. The FET device is fabricated on a Silicon-on-Insulator substrate using conventional silicon processing. The nanoparticle layer is separated from the channel area of the FET with a 5 nm thermal SiO2 layer and is isolated from Al gate contact with a LB-deposited organic insulator layer. The memory effect is tested using voltage pulses on the gate of the device and monitored through drain current measurements. We observe that the nanocrystals can be charged either from the channel through the thermal oxide layer or from the gate through the organic insulator. For higher voltage pulses (> 5 V) charging from the gate dominates and memory windows greater than 1V are observed. For smaller voltage pulses, the phenomenon is reversed and charging occurs from the channel. Endurance characteristics of the device for both charging directions will be discussed and conclusions for further research will be presented. [1] S. Paul et al. Nano Letts., 3 (2003) 533.

D6.8

Micro-structural Evolution of Granular Thin Films of $Cu_{80}Co_{20}$ as a Result of Annealing. Fionnbarr Timothy O'Grady, Jordan Shefer Peck, Nam Kim and Jian Qing Wang; Department of Physics, Applied Physics and Astronomy, Binghamton University, Binghamton, New York.

Zero-field cooled and field-cooled magnetic susceptibility curves were measured on granular thin films of $Cu_{80}Co_{20}$ using a SQUID magnetometer. The thin films were co-sputtered in a high vacuum with a base pressure of $1.0x10^{-7}$ Torr from two elemental targets. The samples were annealed in vacuum at temperatures of 100°C, 200°C, 300°C, and 400°C, respectively. Both in-situ and ex-situ samples were studied and the ex-situ samples were covered with photo resist in order to prevent surface oxidation. As deposited samples showed the standard single peak susceptibility curve [(1,2)], characteristic of super-paramagnetic particles; however, with annealing we observed the emergence of a second peak at a higher temperature. As annealing temperature increased the first peak that occurred around 30 to 50K decreased in height while the second, which occurred around 240 to 300K, grew. These anomalous features were observed in films with varied thickness values ranging from 35 to 100 nm, as well as in in-situ annealed films. They appeared to result from microstructure evolution, namely an increase in large particle population at the expense of smaller particles, accompanying the process of annealing. It is likely that the film contains a mixture of small particles and larger particles that are induced by annealing, which gives rise to the double peak structure. By analyzing these curves together with magnetization curves of the same samples and making use of the Langevin and Curie-Weise Law we can determine the population ratio of small particles to large particles for a given film. (1) C. Papusoi et al. J. Magnetism and Magnetic Materials 195 (1999) 708 - 732 (2) H. J. Blythe et al, Journal of Materials Science 31 (1996) 6431-6439

D6.9

The Effect of Composition and Annealing Environment on Formation of Nanocrystal Si Memory using ECR-PECVD-Deposited Silicon-Rich Silicon Oxide. Daigil Cha[1], Jung H. Shin[1], Soo-Hwan Jeong[2], Young Kwan Cha[2] and In K. Yoo[2]; [1]Physics, KAIST, Daejeon, South Korea; [2]U-team, Samsung Advanced Institute of Technology, Suwon, South Korea.

Nanocrystal Si (nc-Si) based nonvolatile memory devices have received much attention recently as a promising alternative to conventional poly-Si based floating gate memory devices, with promises of low-voltage programming with a faster programming speed and improved retention time. In fabricating such nc-Si memory, easy, manufacture-friendly formation of a dense, uniform layer of small nc-Si with controlled separation from the channel is the key. In this paper, we report on fabricating such nc-Si memory with a 3 nm sized nc-Si with electron-cyclotron resonance plasma enhanced chemical vapor deposition (ECR-PECVD). 3 nm-thick SiO_x (x<2) layer was deposited on a p-type Si substrate with a 4 nm thick thermal oxide by ECR-PECVD using SiH_4 and O_2 as source gases. After deposition of the SiO_x layer, a 7 nm thick gate oxide of stoichiometric SiO_2 layer was deposited by reducing the SiH_4 flow rate, thus producing the entire nc-Si memory structure in one simple deposition step. After deposition, nc-Si was precipitated inside the SiO_x layer by a 30 min anneal at 900°C. High-resolution transmission electron microscopy revealed formation of a single layer of a dense array of nc-Si, and confirmed that the diameter and location of the nc-Si were controlled by the thickness of the original SiO_x layer and the thermal oxide layer,

respectively. High-frequency capacitance - voltage (CV) measurements show clear charge-trap and memory effects due to the nc-Si with flat band shift of 2.8V, corresponding to electron/hole trap density of ($4.3X10^{12}$ / $3.7X10^{12}cm^{-2}$), and negligible dissipation of stored charge even after 48 hrs. Interestingly, such memory effects were observed only when the sample was annealed in oxidizing environment (9/1 mixture of N_2 and O_2), and not when annealed in an inert environment (Ar). Furthermore, formation of nc-Si in 3 nm thin SiO_x layer required a much higher excess Si content than that necessary for a thick SiO_x film. These results indicate that precipitation kinetics of nc-Si in ultra-thin SiO_x layers may be different from that in thick SiO_x layers, and that $in-situ$ oxidation of the SiO_x layer plays an important role in determining the precipitation kinetics. A more detailed analysis of the oxidation and precipitation kinetics as well as memory performance will be presented.

D6.10
Abstract Withdrawn

D6.11
Abstract Withdrawn

D6.12
Small Magnetic Clusters of Ga and In with As and V.
Liudmila A. Pozhar[1], Alan T. Yeates[2], Frank Szmulowicz[3] and William C. Mitchel[3]; [1]Chemistry, Western Kentucky University, Bowling Green, Kentucky; [2]Polymer Materials Branch, Materials and Manufacturing Directorate, Air Force Research Lab, Wright-Patterson Air Force Base, Ohio; [3]Sensor Materials Branch, Materials and Manufacturing Directorate, Air Force Research Lab, Wright-Patterson Air Force Base, Ohio.

Ga3As and In3As molecules, and the smallest pre-designed clusters of Ga and In with As have been recently studied [1] in detail by means of the Hartree-Fock (HF)-based, multi-configuration self-consistent field (MCSCF) method. The data so obtained proved that manipulations with the cluster structure, stoichiometry and form can lead to changes up to an order of magnitude in clusters' electronic energy level patterns and direct optical transition energies. In this work the above studies have been extended to include several small, pre-designed magnetic clusters of Ga and In with As atoms some of which are replaced by V atoms. With magnetic semiconductor element clusters, a recognition that experimentally developed clusters may be more functional if grown in confinement, can be of utmost importance. The major reason is that the density of magnetic memory elements confined in sub-nanoscale pores arrays provided by alumina and silica membranes (pore width of several atomic diameters) can be increased by several orders of magnitude as compared to that existing at present. At the same time, the confinement may reduce significantly spin-disordering temperature effects, thus preserving desirable ferromagnetic properties of such confined magnetic semiconductor clusters or wires. The pre-designed small pyramidal clusters of Ga-As-V and In-As-V atoms have been studied by means of the Hartree-Fock-based, MCSCF method. Their electronic energy level patterns and direct optical transition energies have been compared to those specific to "pure" small Ga-As and In-As clusters of the same structure and numbers of Ga and In atoms studied earlier. This comparison allows elucidation of the effects of inclusion of magnetic atoms on optical properties of otherwise non-magnetic semiconductor element clusters. [1] L.A. Pozhar, A.T. Yeates, F. Szmulowicz and W.C. Mitchel, Small Atomic Clusters: Templates for Sub-Nanoscale Heterostructure Units with Pre-Designed Charge Transport Properties, Phys. Rev. Lett. (2004, in press); L.A. Pozhar, A.T. Yeates, F. Szmulowicz and W.C. Mitchel, Virtual Synthesis of Sub-Nanoscale Materials with Prescribed Physical Properties, 2003 Fall Meet. Proc., Symp. L: Continuous Nanophase and Nanostructured Materials, Eds. S.Komarneni, J.C. Parker and J.J. Watkins, December 1-5, Boston, MA (6 p), in: MRS Proceedings, 788, L11.40, (6p) (2004); L.A. Pozhar, A.T. Yeates, F. Szmulowicz and W.C. Mitchel, Virtual Fabrication of Electronic Materials of Prescribed Physical Properties, Proc. 2003 Ann. AIChE Meet., November 16-23, 2003, San Francisco, CA (10 p).

D6.13
Magnetism in Co-Doped Insulating Oxide Thin Films for Spintronic Applications.
S. R. Rao Mamidanna[1], Darshan C. Kundaliya[1], S. Dhar[1], Claudio Cardoso[1], Sascha J. Welz[2], S. B. Ogale[4,1], S.R. Shinde[1], S. E. Lofland[3], Nigel D. Browning[5] and T. Venkatesan[1]; [1]Center for Superconductivity Research, Department of Physics, University of Maryland, College Park, Maryland; [2]Chemical Engineering and Materials Science, University of California at Davis, Davis, California; [3]Departmen of Chemistry and Physics, Rowan University, Rowan, New Jersey; [4]Departmen of Materials Science, University of Maryland, College Park, Maryland; [5]Lawrence Berkeley National Laboratory, National Center for Electron Microscopy, Berkeley, California.

Synthesis of new ferromagnetic insulator (FI) thin films is important in order to observe the spin-filter effect as FI tunnel barriers can form the basis for the realization of quantum computation in solid state devices [1]. In general, ferromagnetic insulators (FI) are not common because in most insulating solids spins tend to order antiferromagnetically. A few ferromagnetic insulators belonging to the Europium-chalcogenide family are known, however the corresponding Curie temperatures are far below room temperature [2]. In a recent work, we have observed giant moment and above room temperature ferromagnetism in Co-doped Hafnia films [3]. Hafnia (HfO_2) thin films have the potential to replace SiO_2 layers in MOS devices due to their low-leakage current rates. We report in this work the observation of interesting magnetic properties of dilutely Co-doped (5 mol%) high-k dielectric HfO_2, and other systems viz., CeO_2 (CEO), SrTiO_3 (STO) and In_2O_3 (INO). Above room temperature ferromagnetism is observed in all the systems in their epitaxial thin film form. Giant magnetic moment (6.8 B/Co) is observed in HfO_2:Co thin films grown by PLD and the moment varies for other thin film systems (CEO, STO and INO) for the same amount of Co-doping. Recently a great deal of interest has been generated world wide in the search for ferromagnetism in diluted magnetic systems [4,5]. However, all such systems are either conducting or semiconducting in contrast to the current case of highly insulating matrix. Co-doping in Hafnia stabilizes the monoclinic phase at low growth temperature (700ôC). Magnetic moment observed as a function of time was quite stable and was filtted to an equation of the type M_f = M_i exp(-t/τ), where M_i and M_f are the initial (starting) and final time of the measurement. The value of τ 10ô s which indictaes a robust ferromagnetism. TEM results do not show the formation of clusters and Co-valence state observed from EELS study is +2. Rutherford backscattering (RBS) studies indicate the stabilization of the monoclinic phase. Our preliminary results also show magnetism in room temperature grown Co-doped Hafnia thin films on Si-substrate. Magnetism in HfO_2 thin films can have prospective applications in magneto-optic devices. Details of the relationship between the dielectric constant and magnetic moment will be discussed in the context of a vacancy (defect) model. 1. D.P. DiVincenzo, J. Appl. Phys. 85, 4785 (1999). 2. L. Esaki, P.J. Stiles, and S. von Molnar, Phys. Rev. Lett. 19, 852 (1967). 3. M.S.R. Rao et al. Appl.Phys.Lett. (submitted0 4. J.K. Furdyna, J. Appl. Phys. 64, R29-R64 (1988). 5. S.B. Ogale et al. Phys. Rev. Lett. 91, 077205 (2003). The authors acknowledge the support received from DARPA (grant # N000140210962) and NSF-MRSEC (#DMR 00-80008)

D6.14
Growth Temperature and Properties of GeSbTe Films.
Wendong Song, Lu Ping Shi, Xiangshui Miao, Xiang Hu, Rong Zhao and Joon Fatt Chong; Data Storage Institute, Singapore, Singapore.

Chalcogenide semiconductors have attracted much attention because of their interesting electrical, optical and thermal properties. For example, Ge2Sb2Te5 material can be used in the phase-change rewritable optical disk and nonvolatile memory due to its different electrical and optical properties at amorphous and crystal states. Usually, Ge2Sb2Te5 films are prepared at the room temperature. The phase-change was taken place by laser irradiation or pulse current heating. In this paper, we studied Ge2Sb2Te5 films at different growth temperatures and showed some interesting results observed. A KrF excimer laser was used as an external energy source to ablate a Ge2Sb2Te5 target mounted at 45 degree with respect to the laser beam. Single-crystal Al2O3 and Si substrates were mounted on a stainless steel holder by silver paste with a distance of 6 cm from the facing target. A background pressure of 10-6 Torr was achieved with a turbomolecular pump. The films were deposited at laser fluence of 2 J/cm2 and a repetition rate of 10 Hz. After film growth, substrates cool down to room temperature at the same pressure. Six groups of Ge2Sb2Te5 films were prepared at the different growth temperatures. Another two groups of samples grown at room temperature were annealed for ten minutes at high temperatures. We found that no films were grown on the substrates at 340 oC or above. At 300 oC or below, films can be obtained on the substrates. This indicates the critical growth temperature of Ge2Sb2Te5 films is between 300 and 340 oC. The electrical and optical properties as well as crystal structure of thin films at different growth temperatures were analysized by four-probe measurement, Hall effects, Ellipsometer and XRD. It was found that resistivity, carrier density and n & k of thin films strongly depend on the growth temperature.

D6.15
Polarization Switchings in Epitaxial and Polycrystalline Ferroelectric Pb(Zr,Ti)O_3 Films.
Ye Won So[1], D. J. Kim[1], T. W. Noh[1], Jong-Gul Yoon[2] and T. K. Song[3]; [1]School of Physics and ReCOE, Seoul National University, Seoul, South Korea; [2]Department of Physics, Suwon University, Suwon, Kyunggi-do, South Korea; [3]Department of Ceramic Science and Engineering, Changwon National University, Changwon, Kyungnam, South Korea.

Understanding polarization switching behaviors in ferroelectric (FE) films is of great importance in both scientific interests and applications, such as nonvolatile memory devices. In FE single crystals, polarization switching behaviors have been successfully explained by the Kolmogorov-Avrami-Ishibashi (KAI) model.[1] In this model, the switching process can be explained in terms of domain nucleation and growth, and is limited by the domain wall motions. Recently, Tagantsev *etal.* showed that polarization switching behaviors of polycrystalline PZT films with (111) preferred orientation differ from the KAI model and proposed the nucleation limited switching (NLS) model.[2] To obtain further insights on the switching behaviors in FE thin films, we performed systematic studies on epitaxial and polycrystalline films under various applied electric fields and compared their results. Both epitaxial and randomly oriented polycrystalline $Pb(Zr_{0.4}Ti_{0.6})O_3$ (PZT) films were fabricated by the pulsed laser deposition. They were grown at 600 °C on the $SrRuO_3/SrTiO_3(001)$ and $SrRuO_3/SiO_2/Si$, respectively. The polycrystalline PZT films with (111) preferred orientation were prepared by sol-gel method on Si substrates with $Pt/IrO_2/Ir$ bottom electrode. We found that these three kinds of the FE films showed drastically different switching behaviors. For the epitaxial film, the polarization switching always occurred in a very short time scale, i.e. within just 1-2 decades of the switching time, independent of the applied electric field. The switching curves can be fitted with the KAI model reasonably well. On the other hand, a full switching of polarization in polycrystalline film could not be observed in most of our experimental conditions, and switching did occur in several decades of switching time. Since the domain wall propagation could be limited by the grain boundary, the nucleation rate can be one limiting factor, as suggested in NLS model. However, our polycrystalline film of (111) preferred orientation showed the saturated switching of polarization at high field, but no saturated behavior at low field. These results suggest that there should be more than one limiting factor for the FE switching behaviors. These electrical properties will be discussed with the local domain propagation behaviors of the PZT films, measured with a piezoelectric force microscope. [1] A. N. Kolmogorov, Izv. Akad. Nauk. Ser. Math. **3**, 355 (1937); M. Avrami, J. Chem. Phys. **8**, 212 (1940); H. Orihara, S. Hashimoto, and Y. Ishibashi, J. Phys. Soc. Jpn. **63**, 1031 (1994). [2] A. Tagantsev *etal.*, Phys. Rev. B **66**, 214109 (2002).

D6.16

Material Characteristics Change in $Ge_2Sb_2Te_5$ Film through its Patterning Processes for Phase-Change Random Access Memory Integration. Byeong-Ok Cho, Suk-Ho Joo, Kyung-Rae Byun, Jong-Chan Shin, Hee-Seok Kim, U-In Chung and Joo-Tae Moon; Process Development Team, Memory Division, Samsung Electronics Co., Ltd., Yongin-City, Gyeonggi-Do, South Korea.

PRAM (Phase-Change Random Access Memory) is a non-volatile memory device based on the drastic resistivity change between amorphous and crystalline phases of its core material, i.e., chalcogenide film such as GST ($Ge_2Sb_2Te_5$). Though dry etch and ashing for the patterning of GST film are key processes to the PRAM high-density integration, few studies have been reported on the impact of the processes on the material characteristics and the electrical behaviors of the film. In this article, we investigated the effect of process conditions on the etch profile of GST pattern, the film surface composition and chemical bonding, and the film structure. We chose a combination of etch gases as basic dry etch chemistry for the GST patterning based on a thermodynamic analysis. We prepared p-type Si wafers on which silicon oxide bottom layer, N-doped GST, TiN top electrode, and silicon oxide hard mask were sequentially deposited and finally photo-patterned as test samples. We obtained an optimal process window for the best etch profile considering the sidewall undercut and the bottom residues. We observed plasma gas phase by OES (optical emission spectroscopy) and found that Ge atomic peak at 305 nm best represented the GST etch process in the plasma so the peak was set as the main EPD (end point detection) signal. We analyzed the surface atomic compositions and chemical bonding of GST film changing from their as-deposited to post-etch and post-ashing states by XPS (X-ray photoelectron spectroscopy). We also used TEM (Transmission electron microscopy) and EDS (Energy Dispersive Spectroscopy) for the change in the film structure and compositions through patterning of real PRAM devices. Finally, we investigated potential device issues that can be related to the changes in material characteristics mentioned above.

D6.17

Preparation of Strontium Bismuth Tantalate Thin Films by Liqiud-Delivery Metalorganic Chemical Vapor Deposition. Mindaugas Silinskas[1], Serhiy Matichyn[1], Marco Lisker[1], Bodo Kalkofen[1], Tatyana Hur'yeva[1], Bernd Garke[2] and Edmund Burte[1]; [1]Institute of Micro and Sensor Systems, Otto von Guericke University Magdeburg, Magdeburg, Germany; [2]Institute of Theoretical Physics, Otto von Guericke University Magdeburg, Magdeburg, Germany.

Thin films of Bi_XO, Sr_XTa_YO, and $Sr_XBi_YTa_ZO$ (SBT) were deposited by metalorganic chemical vapor deposition (MOCVD) on 150 mm silicon (100) wafers. Some of the wafers were pre-deposited with Pt or Ir electrodes. The substrate temperature and the deposition pressure were varied from 300 to 650 C and from 0.35 to 7 mbar, respectively. Trisallylbismuth ($Bi(//)_3$) or triphenylbismuth ($Bi(C_6H_5)_3$) and strontium bis-pentaethoxymethoxyethoxy tantalate ($Sr[Ta(OEt)_5(OC_2H_4OMe)]_2$) were used as Bi precursor and as Sr-Ta precursor, respectively. A liquid delivery system was used to supply and to vaporize the precursor into the reactor. X-ray photoelectron spectroscopy (XPS), ellipsometry, X-ray diffraction (XRD), and electrical measurements were carried out to characterize the film properties. The growth rate of the MOCVD of BiO_X and Sr_XTa_YO was compared to the growth rate of SBT to obtain information about mutual interactions between the precursors. The growth rate of bismuth oxide thin films deposited from trisallylbismuth was low (10 nm/h at 0.35 mbar) and did virtually not depend on the temperature. On the contrary, the growth rate of strontium tantalate films depended strongly on the temperature. The deposition rate of the SBT films was similar to rate of the bismuth oxide film deposition, which slightly increased with increasing substrate temperature. However, the deposition rate of SBT was always lower than the deposition rate of the single precursors. The growth rate significantly depended on the deposition pressure. A decrease of the deposition pressure in the reactor chamber reduced the deposition rate of BiO_X, Sr_XTa_YO, and SBT but on the other hand, it improved the uniformity of the film thickness. The XPS measurements showed a deficit of bismuth in the SBT films even though the concentration of the Bi precursor was several times higher compared to the other precursors. The XPS depth-profiling by Ar+ ion sputtering indicated different bond characteristics of Ti, Sr, and Bi before and after ion beam bombardment.

D6.18

A New Crystalline to Crystalline Phase Change Memory Cell Using $(Ge_1Sb_2Te_4)_{0.8}(Sn_1Bi_2Te_4)_{0.2}$ Alloy. Dong-ho Ahn[1], D.H. Kang[2], H.S. Kwon[1], M.H. Kwon[1], H.M. Kim[1], T.Y. Lee[1], T.G. Kim[2], K.S. Lee[2], T.S. Lee[2], I.H. Kim[2], W.M. Kim[2], B. Cheong[2] and K.B. Kim[1]; [1]Materials and Science Engineering, Seoul National University, Seoul, South Korea; [2]Thin Film Materials Research Center, Korea Institute of Science and Technology, Seoul, South Korea.

A new phase change memory cell using resistance transition between two crystalline phases of $(Ge_1Sb_2Te_4)_{0.8}(Sn_1Bi_2Te_4)_{0.2}$ chalcogenide alloy is proposed in this study. $Sn_1Bi_2Te_4$ of 20 mole % not only accelerates the crystallization of $Ge_1Sb_2Te_4$ through forming a complete solid solution alloy but also changes the basic concept of binary phase transition memory element which has amorphous and crystalline (fcc) states. In this new phase change memory device, phase change material has no amorphous phase but the data is stored in different forms of crystalline phases. Transition of cell resistance from low conducting crystalline state (fcc) to high conducting crystalline state (hcp) and vice-versa is very abrupt and fast (70 ns), and also each cell resistance values correspond the resistivity of each phases of $(Ge_1Sb_2Te_4)_{0.8}(Sn_1Bi_2Te_4)_{0.2}$. Additional research is needed for direct observation of fast fcc to hcp transformation by electrical stress, however this phenomenon will increase the cyclability of the device since it reduces the volume change between two phases.

D6.19

All-Organic Single-Transistor Permanent Memory Device. Raoul Schroeder, Leszek A. Majewski and Martin Grell; Department of Physics and Astronomy, University of Sheffield, Sheffield, United Kingdom.

Organic field-effect transistors (OFETs) show great potential for applications in flexible, mobile, and ultra-low-cost electronics. However, to fully achieve this goal, equally cheap and versatile memories will have to be developed for products such as radio-frequency identification devices (RFIDs) and throw away circuitry. Here, we present a solution to this problem, an organic single transistor permanent memory device, which we call the 'FerrOFET'. This memory device is a single transistor memory that is built around a polymeric gate insulator with ferroelectric-like properties in the amorphous phase: poly-m-xylylene adipamide (MXD6), a cheap, commercially available nylon. To stay close to current commercial OFET production techniques, we deposited MXD6 from solution, using a high boiling point solvent, and used pentacene as the semiconductor material. The memory of the 'FerrOFET' is written by applying a sufficiently large gate voltage, -15 V to write state '1' and +10 V to write state '0', for an MXD6 insulator thickness of 200 nm. It can subsequently be read with no gate voltage applied. In state '1', the current is about 1000 times larger than in state '0', which is a very competitive value compared to inorganic ferroelectric transistor memories. The memory is retained for several hours without refresh, showing only a small decline in on-state current over several hours after an initial fast depolarisation, which is already

orders of magnitudes better than regular transistor/capacitor memory cells. The device operates flawlessly in air. The 'FerrOFET', therefore, is a memory transistor very similar in capabilities to inorganic ferroelectric memories, but can be manufactured at a very small fraction of the cost and at ambient temperatures. Therefore, we anticipate that the 'FerrOFET' will be the choice of memory for organic transistor circuits, as it is very easy to integrate with current organic transistor technologies, exhibits excellent characteristics, and conserves energy in mobile modules due to the high memory retention.

D6.20
Contribution of a-Domain on the Ferroelectric Property of (100)/(001)-Oriented Epitaxial PZT Films. Hiroshi Funakubo[1], Hitoshi Morioka[1], Risako Ueno[1], Shintaro Yokoyama[1] and Keisuke Saito[2]; [1]Tokyo Institute of Technology, Yokohama, Japan; [2]PANalytical Division, Tokyo, Japan.

Epitaxially grown (100)/(001)-oriented epitaxial PZT films have been widely investigated to understand the basic characteristics of the PZT because of the lack of the single crystal data. However, the systematic research for the films by changing the volume fraction of (001) orientation, $\nu(001)$, has been hardly reported. We have already succeeded in growing perfectly polar-axis-, (001)-, oriented $Pb(Zr_{0.35}Ti_{0.65})O_3$ films by MOCVD and succeeded in obtaining the large spontaneous polarization value up to 90 $\mu C/cm^2$. In the present study, we grew the (100)/(001)-oriented epitaxial PZT films with $\nu(001)$ and investigated the change of the electrical property of the films with $\nu(001)$. Epitaxial $Pb(Zr_{0.35}Ti_{0.65})O_3$ films with $\nu(001)$ from 6 to 100% were grown on $(100)SrRuO_3//(100)SrTiO_3$ substrates by changing the deposition temperature and the film thickness. $\nu(001)$ decreased with decreasing the deposition temperature and increasing the film thickness. Full width at the half maximum ($FWHM$) of the PZT *200* XRD peaks was within the 0.4 and 1.0 degree and the lattice parameter was almost independent of the $\nu(001)$. These suggest that the film quality and the residual strain were almost independent of the $\nu(001)$. Dielectric constant at 1 kHz increased from 300 to 500 with decreasing the $\nu(001)$, suggest that the dielectric constant along the polar axis was smaller than that perpendicular to the polar axis. Saturation polarization (P_{sat}) and the remanent polarization (P_r) linearly decreased with decreasing $\nu(001)$, suggesting that domain switching from (100) to (001) orientation was hardly observed by the clamping from the substrate. On the other hand, the clear relationships between the coercive field value and the $\nu(001)$ were not detected. This shows that the obvious contribution of (100) domain to the E_c value was not detected within the limit of the present study.

D6.21
Enhanced Spontaneous Polarization of Dysprosium-substituted Lead Zirconate Titanate Thin Films by a Chemical Solution Deposition Method. Hiroshi Uchida[1], Hiroshi Nakaki[1], Shoji Okamoto[2], Shintaro Yokoyama[2], Hiroshi Funakubo[2] and Seiichiro Koda[1]; [1]Department of Chemistry, Sophia University, Tokyo, Japan; [2]Department of Innovative and Engineered Materials, Tokyo Institute of Technology, Yokohama, Japan.

Enhancing the ferroelectric properties of lead zirconate titanate ($Pb(Zr,Ti)O_3$; PZT) film is required for developing the integration of nonvolatile random access memories. Authors attempted the improvement of ferroelectric properties of PZT films by promoting the anisotropy of simple-perovskite crystal. Crystal anisotropy of PZT was controlled by the species and occupying site of substituent cation; B-site substitution using rare-earth cations whose ionic radii locate on smaller parts of its series (such as Y^{3+}, Gd^{3+}, Dy^{3+}, Yb^{3+}, etc.) can promote the anisotropy of PZT crystal, i.e., the ratio of PZT lattice parameters (c/a), whereas inverse phenomenon occurs in the case of A-site substitution using rare-earth cations whose ionic radii locate on larger parts of its series (such as La^{3+}, Nd^{3+}, etc). In this study, authors especially focused on the dysprosium (Dy^{3+}) ion as a substituent cation for improving the ferroelectric properties of PZT films because Dy^{3+} ion has relatively larger ionic radius in the group of rare-earth cations that are to occupy B-site in PZT crystal. The influences of the ion substitution using Dy^{3+} ion on the ferroelectric properties of PZT films were investigated. PZT-based films were fabricated by a chemical solution deposition. Spin-coating solutions with chemical compositions of $Pb_{1.00-(3x/2)}Dy_x(Zr_{0.40}Ti_{0.60})O_3$ and $Pb_{1.00}Ln_x(Zr_{0.40}Ti_{0.60})_{1-(3x/4)}O_3$ (denoted A-PDZT and B-PDZT respectively) were prepared using lead acetate, zirconium iso-propoxide, titanium normal-buthoxide, dysprosium nitrate and 2-methoxyethanol as starting materials. These solutions were spin-coated on $(111)Pt/Ti/SiO_2/(100)Si$ and $(111)SrRuO_3/(111)Pt/(100)YSZ/(100)Si$ substrates, followed by a drying (150°C, 10 sec, in air) and a pyrolysis process (400°C, 3 min, in air). After repeating these processes several times, the resulting films were heat-treated for crystallization at 650°C for 5 min in air. Polycristalline PZT films were obtained on $(111)Pt/Ti/SiO_2/(100)Si$ substrate, while epitaxially-grown (111)PZT films were fabricated on $(111)SrRuO_3/(111)Pt/(100)YSZ/(100)Si$ substrate. Remanent polarization (P_r) of A-PDZT films degraded gradually with increasing the amount of Dy^{3+}-substitution. On the other hand, the P_r value of polycrystalline PZT film on $(111)Pt/Ti/SiO_2/(100)Si$ was enhanced by Dy_{3+}-substitution from 20 $\mu C/cm_2$ ($x = 0$) up to 26 $\mu C/cm_2$ ($x = 0.02$) in the case of B-PDZT. Spontaneous polarization (P_s) of Dy^{3+}-substituted PZT ($x = 0.02$) to {001} direction was estimated from P_r value of Dy^{3+}-substitited epitaxially-grown (111) PZT film on $(111)SrRuO_3/(111)Pt/(100)YSZ//(100)Si$ to be 84 $\mu C/cm^2$ that was signifcantly larger than that of non-substituted PZT (= 71 $\mu C/cm^2$). We concluded that the enhancement of P_s value was achieved by promoting the crystal anisotropy of PZT because increasing the ratio of PZT lattice parameters (c/a) was accompanied with these results.

SESSION D7: Organic and Resistive Memories
Chairs: Shashi Paul and Dimitris Tsoukalas
Thursday Morning, December 2, 2004
Back Bay B (Sheraton)

8:30 AM *D7.1
Organic Thin Film Nonvolatile Memory Devices. Yang Yang, Materials Sci. & Eng., UCLA, Los Angeles, California.

Organic functional thin films and related devices, with emphasis on LEDs, transistors, and solar cells, have attracted strong attentions in the past decade. On the other hand, organic memory device, one of the most important electronic devices, was left untouched until recently when a high performance organic bistable and memory was reported. (Appl. Phys. Lett. 82, 1419, (2003)) The UCLA organic memory devices take the advantages of the nano technology by incorporating nano-particles into the organic matrix system. The performance of the devices makes them attractive for memory cell type of applications. The two states, the 0 and 1 states, of the devices differ in their electrical conductivity by several orders in magnitude and show remarkable stability, i.e. once the device reaches either state; it tends to remain in that state for a prolonged period of time. More importantly, the high and low conductivity states of our memory devices can be precisely controlled by the application of a positive voltage pulse (to write) or a negative voltage pulse (to erase), respectively. Those organic memory devices can be formed by either large-area vacuum coating technology or by wet polymer coating processing, are promising for the next generation of nonvolatile and rewritable memory devices with low-cost and high-performance advantages.

9:00 AM D7.2
Organic Memory Devices Using C_{60} and Polymer.
Alokik Kanwal, Shashi Paul and Manish Chhowalla; Ceramics and Materials Engineering, Rutgers University, Piscataway, New Jersey.

The ease of fabrication and use of inexpensive substrates has generated tremendous interest in organic electronics [1] while molecular electronics offers the potential of miniaturization down to a few atoms. However, unlike organic electronic devices, molecular devices are extremely difficult to assemble making mass production impossible with the existing technology. Although several types of single molecule devices have been demonstrated, molecular memories have shown promise towards technological feasibility [2]. In contrast, there has been a relatively few reports of organic memory devices, although recently they have received higher profile [3]. Here, we describe an all organic molecular memory device that combines the advantages of molecular and organic electronics. We accomplish this by combining C_{60} molecules with poly-vinyl-phenol (PVP) by dissolving in iso-propanol. The solution is spun onto a glass substrate with aluminum tracks, 2 mm in width and 25 mm in length. The top aluminum tracks are then evaporated, through a shadow mask, in a perpendicular direction. This results in metal-organic-metal (MOM) structures. The current-voltage measurements show a large hystersis in the blend devices and none in the pure PVP devices. The blend devices exhibit high and low conductance states, rapid switching times of less than 30 nanoseconds, low power consumption of less than 0.01 pJ, long term cycling stability and data retention times lasting for more than several hours which renders them suitable for membership in the class of non-volatile, high speed and inexpensive memory devices. We have also fabricated a memory cell with dimensions of 50nm x 50nm in order to demonstrate that miniaturization is feasible. A detailed study of the electrical behavior of non-volatile MOM memory devices will be discussed in this presentation. The blend thin films have been thoroughly characterized using Raman spectroscopy, atomic force microscopy and scanning electron microscopy. Based on the structural and electrical measurements, we will propose a model for conduction mechanism and memory effects. 1. Forrest, S.R. , The path to ubiquitous and low-cost organic electronic appliances on plastic, Nature 428, 911-918 (2004). 2. Reed M A, Chen J, Rawlett A

M, Price D W and Tour J M "Molecular random access memory cell" Appl., Phys., Lett. 78, 3735-3737 (2001). 3. Scott, J.C., Is there an immortal memory?, Science, 304, 62-63 (2004)

9:15 AM D7.3

Multilevel Molecular Memory. Chao Li[1], Wendy Fan[2], Bo Lei[1], Jie Han[2], Meyya Meyyappan[2] and Chongwu Zhou[1]; [1]EE, Univ. of Southern California, LA, California; [2]1Center for Nanotechnology, NASA Ames Research Center, Moffett Field, California.

ABSTRACT We will present the design, fabrication and evaluation of novel multilevel molecular memory devices.1-2 These devices have been demonstrated for nonvolatile data storage up to three bits (eight levels) per cell, in contrast to the standard one-bit-per-cell (two levels) technology. In the demonstration, charges were precisely placed at up to eight discrete levels in redox active molecules self-assembled on a single-crystal semiconducting nanowire field effect transistor. Gate voltage pulses and current sensing were used for writing and reading operations, respectively. Charge storage stability was tested up to retention of 600 hours, as compared to the longest retention of a few hours previously reported for one-bit-per-cell molecular memories. Furthermore, the origin of the memory and the relation to the molecular structure have been systematically studied.3-4 Comparison between silicon and molecular devices shows that multilevel molecular memory enables low-power, ultra-dense and high-performance nonvolatile data storage to go beyond the silicon technology scaling limit. 1. C. Li, et al. Multilevel memory based on molecular devices, Appl. Phys. Lett. 84, 1949 (2004). 2. Multilevel molecular memory, Physics Today 57, 9 (2004). 3. C. Li, et al. Charge storage behavior of nanowire transistors functionalized with bis(terpyridine)-Fe(II) molecules: dependence on molecular structure, JACS, online released (2004). 4. C. Li, et al. Data storage studies on nanowire transistors with self-assembled porphyrin molecules, JPCB, online released (2004).

9:30 AM D7.4

Nano-trap memory: a crosspoint memory element based on charge trapping in metallic nano-particles.

Luisa Dominica Bozano, Kenneth R. Carter, Vaughn R. Deline and J. Campbell Scott; Research, IBM, San Jose, California.

The combination of thin-film semiconducting polymers or small molecule organic materials with metal nanoparticles is used to fabricate high density two terminal voltage-switchable memory devices. The ON and OFF states of the devices are read by measuring the current at 1 V and can be controlled by applying voltage pulses at Von (3-4 V) or Voff (6-9 V), respectively. These values correspond to the local maximum and minimum in the current density versus voltage graph behavior, that for these devices has a characteristic N-shape (i.e. with a negative differential resistance region). Multistable states can also be achieved. Device's properties, Von, Voff, Vthreshold (threshold voltage at which the device switches to high current) and the ON/OFF ratio, as well as lifetime, cyclability, and retention time are studied in terms of the materials properties of the semiconducting matrix and metallic nanoparticles, temperature and morphologyical properties of the composite.

9:45 AM D7.5

Experimental Observation of Non-Volatile Charge Injection and Molecular Redox in Fullerenes C60 and C70 in an EEPROM Type Device. Udayan Ganguly[1], Chungho Lee[2] and Edwin C. Kan[2]; [1]Materials Science and Engineering, Cornell University, Ithaca, New York; [2]School of Electrical and Computer Engineering, Cornell University, Ithaca, New York.

Nonvolatile charge injection into small molecules like fullerenes, in nanocrystal EEPROM-like structure provides a programmable method for in situ chemical redox operations. While metal nanocrystal based EEPROMs, [1-3] which use nanocrystal size-dependant coulomb blockade effect for multi-level charge storage, are inhibited by finite nanocrystal size distribution, in the case of fullerenes, multilevel charge storage occurs by charge injection into different molecular orbitals (MOs). We report improved experimental observation of multiple non-volatile charge injection to study injection energy levels of fullerenes by enhanced gate oxide and interface quality to control charge trap related noise as further study of integration of fullerenes into CMOS gate stack [4]. An ultra-thin 2.7 nm tunneling oxide is grown on p-type Si wafer. The wafers are treated with an acetone and isopropanol rinse to enhance evaporated silicon dioxide quality on thermal oxide [4]. Fullerenes (C60 and C70) are evaporated thermally to different thicknesses measured on the quartz crystal monitor (QCM) to produce sub-monolayer coverage for optimal fullerene surface concentration. Evaporated and a hybrid oxide made of evaporated oxide capped with PECVD oxide are tested as control oxide. The different gate stacks are subjected to a set of different annealing temperatures in inert N2 environment to explore process window and control charge traps at the various interfaces between fullerene, deposited oxide and thermal oxide interfaces. The backside contact is deposited by Al evaporation followed by a forming gas anneal (FGA) at 450C for 30 min. Finally the top gate is patterned by aluminum lift off. Charge injection and CV measurements are performed to investigate injection voltage dependent charge injection for C60 and C70. Unlike metal nanocrystal memories, where a finite size distribution of metal nanocrystals manifests in trap-like continuous charging behavior, in fullerenes the charging injection shows steps versus voltage of injection. Hence, charging of fullerene MOs [5] are clearly distinguished from trap filling. Step heights of charge injections provide an estimate of the functional fullerene number density. MO energy levels are determined with respect to the Si band structure from voltages at which step like charge injections occur. References: [1] Z. Liu, C. Lee, G. Pei, V. Narayanan and E. C. Kan, (MRS) Material Research Symposium, Boston, MA, Nov. 26-30, 2001, Proc. Vol. 686, A5.3. [2] Z. Liu, C. Lee, V. Narayanan, G. Pei and E. C. Kan, IEEE Trans. Electron Devices, vol. 49, no. 9, p.1606-1613, Sept. 2002. [3] C. Lee, Z. Liu and E. C. Kan, (MRS) Material Research Symposium, Boston, MA, Dec. 2002, Proc. Vol. 737, F8.18. [4] U. Ganguly, C. Lee and E. C. Kan, (MRS) Material Research Symposium, Boston, MA, Dec. 1-5, 2003, Proc. Vol. 789, N16.3. [5] W. H. Green Jr., M. G. G. Fitzgerald, P. W. Fowler, A. Ceulemans and B. C. Titeca, J. Phys. Chem. 100, 14892 (1996)

10:30 AM *D7.6

Prospect of Emerging Nonvolatile Memories. Hongsik Jeong and Kinam Kim; Advanced Technology Development Team, Semiconductor R&D Center, Samsung Electronics Co.,Ltd., Yongin-City, South Korea.

Conventional nonvolatile memories like flash have successfully meet the need of a market such as high density and low cost. The flash memory market has rapidly grown and needed a high density memory which result in the innovation of flash memory technology. However, there have been concerns about whether this successful progress can be maintained in nano era and can satisfy the needs of diversified IT market in the future. Although flash memory has the great advantage of high density with small cell size, it has the disadvantage of slow writing speed and limited endurance. These will be significant drawbacks for the future memory candidates in which fast writing speed and good reliability is essential. The challenges ahead for conventional nonvolatile memories forces many research groups and companies to develop alternative memories with ideal characteristics such as nonvolatility, high density, high speed and low power. In this article, we will evaluate the characteristics of emerging nonvolatile memories such as ferroelectric random access memory (FRAM), magnetoresistive random access memory (MRAM) and phase change random access memory (PRAM). These memories have been recently focused because of the possibility that they can overcome the challenges conventional memories facing. Finally we will review critical technology barriers in developing emerging nonvolatile memories and predict the promising technology to overcome the barriers, which will be technology guidelines for a future memory develoment.

11:00 AM D7.7

Superlattice-like Structure for non Rotation and non Volatile Phase Change Memory Cell. Tow Chong Chong, Lu Ping Shi, Rong Zhao, Pik Kee Tan, Xiang Shui Miao and Hao Meng; Data Storage Institute, Singapore, Singapore.

Chalcogenide Random Access Memory (CRAM), also known as Ovonic Unified Memory (OUM), is an inexpensive nonvolatile semiconductor memory with the potential to be high-performance, high endurance, and low power. This novel memory is based on the phase change of chalcogenide alloy materials. The key to the chalcogenide materials is the switching property between amorphous state and crystalline state by electrical pulses. Increasing switching speed and reducing programming current is highly desired for high performance CRAM. In this paper, we propose a new phase change stack to approach this aim. The electronic properties of superlattice have been widely studied in the last few decades. They are dependent on the periods and thickness of the superlattice. Moreover, the band gap engineering through superlattice will result in a change of the phase-change activation energy that may enhance nucleation and rapid crystal growth. On the other hand, thermal properties of superlattice structures have recently attracted increasing attention due to their excellent properties such as thermal management properties. Theoretical and experimental studies have revealed that the thermal conductivity along both in-plane and cross-plane direction deviates significantly from the corresponding bulk materials due to interface phonon scattering and the phonon confinement effect. Based on the above considerations, the electrical and thermal properties of phase change materials can be adjusted by engineering the SLL structure and hence the phase change behavior can be controlled. In this work a new structure of phase change memory cell was proposed to increase speed. In this structure a superlattice-like structure (SLL) was applied to the recording layer of the

phase-change memory. Unlike the conventional single phase change layer, the SLL recording layer consists of alternating thin layers with two different phase change materials, i.e. GeTe and Sb2Te3. Although neither GeTe nor Sb2Te3 could be used as a phase change layer material for memory, present experimental results have shown that the phase change memory with the SLL structure demonstrate a much better recording property that could match practical application requirements. The devices demonstrated marvelous performance of fast speed and small current. Different parameters of SLL phase change memory cell, such as thickness of elemental layer, ratio of GeTe and Sb2Te3, and total thickness of SLL layer, were varied and the properties were compared in order to get optimized structure. The mechanism and issues encountered was investigated by means of simulation and experiments. The issued encountered in designing the recording stacks are also discussed.

11:15 AM D7.8
Investigation of Resistive Switching in Cr-Doped $SrZrO_3$ Perovskite Structures. Hwan-Soo Lee[1,3], Sukwon Choi[2], Paul A. Salvador[2] and James A. Bain[1,3]; [1]Electrical and Computer Engineering, Carnegie Mellon University, Pittsburgh, Pennsylvania; [2]Materials Science and Engineering, Carnegie Mellon University, Pittsburgh, Pennsylvania; [3]Data Storage Systems Center, Carnegie Mellon University, Pittsburgh, Pennsylvania.

We have prepared capacitor-like epitaxial thin film stacks of perovskite materials on $SrTiO_3$ substrates having the following structures: substrate/$SrRuO_3$/Cr (0.2 at.%)-doped $SrZrO_3$/Ti/Au. These structures are similar to the reported by others [1], and were prepared by pulsed laser deposition (PLD). The $SrRuO_3$ film as a bottom electrode was epitaxially grown on $SrTiO_3$ (001) substrates. Half of the area of these elecrodes was then masked off prior to the deposition of each $SrZrO_3$ film. Both films were deposited at 700 °C and O_2 pressure ranging from 50 mTorr to 150 mTorr. Electrodes of Ti/Au with diameter of 250 μm were sputter-deposited on top of the $SrZrO_3$ film as well as on the exposed $SrRuO_3$ film, using a second shadow mask. The epitaxy of the films was checked by x-ray diffraction (XRD) and transmission electron microscopy (TEM). The XRD spectra of the $SrZrO_3$ films on $SrTiO_3$ substrates showed strong (001) and (002) peaks at angles of 21.6° and 44.0°, respectively in θ-2θ scanning, with no other peaks in the range of 2Θ = 20-60°. Well-defined fourfold symmetry in in-plane orientation was observed through ϕ scans of the (111) peak of the $SrZrO_3$ film and the (111) peak of the $SrTiO_3$ substrate. This suggests a good epitaxial growth along the (001) orientations. The lattice mismatch between the $SrZrO_3$ films and the $SrTiO_3$ (001) substrate is about 5.3%, calculated from the XRD spectra. In this study, we have focused on hysteretic behavior in resitance, which may permit their use in two terminal non-volatile memory devices. Electrical transport measurements with current perpendicular to the plane were carried out using a Keithley 2400 source meter in current-controlled mode. By sweeping the current (I) to negative and subsequently to positive values (with respect to the bottom $SrRuO_3$ electrode), a reversible and reproducible transition in junction resistance could be observed. Typical I-V characteristics of a 220-nm-thick $SrZrO_3$ film showed resistance changes of a factor of approximately 10 between the high (as deposited) and low-resistance states, after accounting for the series resistance of the $SrRuO_3$ electrode. Total measured resistances (junction plus contacts and electrodes) were in the range of 15 kOhms for the high resistance state and 3 kOhms for low resistance state, with approximately half of the latter value being electrode series resistance. Switching currents showed a variation of about ±30% in their values in for repeated cycling throuhgh the switching event. In this study, we further discuss process parameters such as oxygen pressure during growth and cooling, and their effects on hysteretic properties and switching behavior. References) [1] A. Beck et al, "Reproducible switching effect in thin oxide films for memory applications," Appl. Phys. Lett., **77**, 139 (2000).

11:30 AM D7.9
Effect of the Bottom Electrode Contact (BEC) on the Phase Transformation of N_2 doped $Ge_2Sb_2Te_5$(NGST) in a Phase-Change Random Access Memory. Suyoun Lee[1], Y. J. Song[1], Y. N. Hwang[1], S. H. Lee[1], J. H. Park[1], K. C. Ryoo[1], S. J. Ahn[1], C. W. Jeong[1], J. H. Oh[1], J. M. Shin[1], F. Yeung[1], W. C. Jeong[1], Y. T. Kim[2], J. B. Park[3], K. H. Koh[1], G. T. Jeong[1], H. S. Jeong[1] and Kinam Kim[1]; [1]Advanced Technology Development Team, Samsung Electronics, Yongin, South Korea; [2]CAE Team, Samsung Electronics Co.,Ltd, Yongin-City, South Korea; [3]AE Lab, Samsung Advanced Institute of Technology, Yongin-City, South Korea.

With respect to the operation of a Phase-change Random Access Memory (PRAM or PcRAM), we studied the dependence of the phase transformation of the N_2 doped $Ge_2Sb_2Te_5$(NGST) on the electrical and thermal resistance of the BEC. The high resistive BEC was made by oxidizing the high conductive metallic BEC and the resistance was controlled with the extent of oxidation. We found that the needed current (Ireset) to amorphize that material was highly reduced with the increase of the resistance. This result was qualitatively consistent with the calculation of temperature profile using the heat transport equation in that material. In addition, we characterized a junction between NGST and BEC in the frame of the metal-amorphous semiconductor (M/a-Sm) junction and investigated the effect of the estimated junction parameters on the operation of a PRAM. Finally, the prospect of a high density PRAM using high resistive BEC will be addressed.

11:45 AM D7.10
Giant Resistance Switching in Metal-Insulator-Oxide Conductor (MOC) Junctions. Rickard Fors, Sergey I. Khartsev and Alexander M. Grishin; Condensed Matter Physics, Royal Institute of Technology, Stockholm-Kista, Sweden.

Heteroepitaxial CeO2(80nm)/L0:67Ca0:33MnO3(400nm) film structures have been pulsed laser deposited on LaAlO3(001) single crystals to fabricate two terminal resistance switching devices. Ag/CeO2/La0.67Ca0.33MnO3 junctions exhibit reproducible switching between a high resistance state (HRS) with insulating properties and a semiconducting or metallic low resistance state (LRS) with resistance ratios up to 100000. Reversible electrical switching is a polar effect achievable both in continuous sweeping mode and in the pulse regime. Successive temperature crossover of electronic transport from the thermal activation of the deep levels (Ea = 320 meV) at high temperatures to thermal activation of the shallow levels (Ea = 40 meV) and finally at low temperatures to the regime of temperature independent resistance, usually associated with Fowler-Nordheim quantum tunneling, has been found for the insulating HRS. The temperature dependence of the LRS reveals a para-to-ferromagnetic phase transition in the La0.67Ca0.33MnO3 (LCMO) electrode at Tc = 260 K and an anomaly at lower temperatures 200 K corresponding to the Curie temperature of the Mn4+ depleted part of the LCMO film. Current-voltage characteristics in the LRS are highly nonlinear, and show negative differential conductance (NDC). We suggest that the reversible resistance switching occurs due to the electric field induced nucleation of filament-type conducting valence-shifted CeOx domains inside the insulating CeO2 matrix. The abrupt insulator-to-metal transition is the result of localization of 4f electronic states in Ce3+ ions and the subsequent appearance of hole conductivity in the oxygen p-bands. NDC at low temperatures is relied upon the interband scattering of CeOx carriers from a low energy, high mobility valley into a high energy valley with low mobility.