MONDAY

ORAL PRESENTATIONS

* Invited Paper

Plenary Session

Session Chairs: James Cooper and Peter Sandvik
Monday Morning, September 18, 2017
Thurgood Marshall Ballroom
8:30 am – 10:15 am

8:30 AM
Welcome / Opening Ceremony
Robert Stahlbush, United States Naval Research Laboratory

8:45 AM *MO.PL.1
Advancing 4H-SiC Crystal Technology to the Next Stage
Hidekazu Tsuchida; Central Research Institute of Electric Power Industry (CRIEPI), Japan.

9:30 AM *MO.PL.2
Recent Developments Accelerating SiC Adoption
Anup Bhalla; United Silicon Carbon, Inc., United States.

Invited Poster Announcement

Session Chairs: James Cooper and Peter Sandvik
Monday Morning, September 18, 2017
Thurgood Marshall Ballroom
10:15 am – 10:30 am

10:15 AM *MO.AIP.1
SEMI Standards for SiC
James D. Oliver[1, 2], Russ Kremer[3, 2] and Arnd-Dietrich Weber[4, 2]; [1]Northrop Grumman, United States; [2]SEMI, United States; [3]Freiberger Compound Materials, United States; [4]SiCrystal AG, Germany.

10:18 AM *MO.BIP.2
Electrostatic-Energy Model for Single Shockley Stacking Fault Formation in 4H-SiC Crystals
Akifumi Iijima, Jun Suda and Tsunenobu Kimoto; Kyoto University, Japan.

10:21 AM *MO.CIP.3
About the Electrical Activation of 1×10^{20} cm^{-3} Ion Implanted Al in 4H-SiC at Temperatures in the Range 1500 - 1950°C
Roberta Nipoti[1], Alberto Carnera[2], Giovanni Alfieri[3] and Lukas Kranz[3]; [1]CNR, Italy; [2]Univ.y of Padova, Italy; [3]ABB, Switzerland.

10:24 AM *MO.DIP.4
Reliability and Ruggedness of 1200V SiC Planar Gate MOSFETs Fabricated in a High Volume CMOS Foundry
Sauvik Chowdhury, Levi Gant, Blake Powell, Kasturirangan Rangaswamy and Kevin Matocha; Monolith Semiconductor, United States.

10:27 AM *MO.EIP.5
Piezoresistive Characteristics of NMOS FET Technology on 4H-SiC
Richard C. Jaeger[1], Jeffrey C. Suhling[2], Leonid Fursin[3] and William Simon[3]; [1]Auburn Univ., United States; [2]Auburn Univ., United States; [3]United Silicon Carbide Inc., United States.

10:30 AM BREAK

Diodes and Bipolar Devices I

Session Chairs: Leonid Fursin and Alexander Lebedev
Monday Morning, September 18, 2017
Thurgood Marshall Ballroom, North Salon
11:00 am – 12:45 pm

11:00 AM *MO.KN.D1.1 (Keynote)
Progress and Challenge in High to Ultra-High Voltage SiC Power Device Technology
Yoshiyuki Yonezawa; National Institute of Advanced Industrial Science and Technology (AIST), Japan.

11:45 AM MO.D1.1
Blocking Performance Improvements for 4H-SiC P-GTO Thyristors with Carrier Lifetime Enhancement Processes
Sei-Hyung Ryu[1], Daniel J. Lichtenwalner[1], Michael O'Loughlin[1], Edward R. Van Brunt[1], Craig Capell[1], Charlotte Jonas[1], Yemane Lemma[1], Qingchun J. Zhang[1], Jim Richmond[1], Al Burk[1], Brett Hull[1], Matthew McCain[1], Shadi Sabri[1], Heather O'Brien[2], Aderinto Ogunniyi[2], Aivars Lelis[2], Jeff Casady[1], Dave Grider[1], Scott Allen[1] and Palmour W. John[1]; [1]Wolfspeed, A Cree Company, United States; [2]U.S. Army Research Laboratory, United States.

12:00 PM MO.D1.2
Experimental Demonstration on Ultra High Voltage and High Speed 4H-SiC DSRD with Smaller Numbers of Die Stacks for Pulse Power Applications
Taiga Goto; University of Tsukuba, Japan.

12:15 PM MO.D1.3
Fabrication of 2.5kV 4H-SiC PiN Diodes with High Energy Implantation (>12MeV) of Al^+ and B^+
Reza Ghandi, Peter Losee, Alexander Bolotnikov and David Lilienfeld; GE Global Research, United States.

12:30 PM MO.D1.4
Conductivity Modulated Ultra-High Voltage Implantation-Free 4H-SiC PiN Diodes
Arash Salemi, Hossein Elahipanah, Carl-Mikael Zetterling and Mikael Östling; KTH Royal Institute of Technology, Sweden.

State of the Art and New Approaches in SiC Materials

Session Chairs: Noboru Ohtani and Peter Wellmann
Monday Morning, September 18, 2017
Thurgood Marshall Ballroom, West Salon
11:00 am – 12:45 pm

11:00 AM MO.A1.1
Growth Conditions and *In Situ* Computed Tomography Analysis of Facetted Bulk Growth of SiC Boules
Matthias Arzig[1], Michael Salamon[2], Norman Uhlmann[2], Bertil Johansen[3] and Peter J. Wellmann[1]; [1]FAU, Germany; [2]FHG IIS, Germany; [3]SG, Norway.

11:15 AM MO.A1.2
X-Ray Topography Analysis of 4H-SiC Crystals Grown by High-Temperature Gas Source Method
Isaho Kamata[1], Norihiro Hoshino[1], Yuichiro Tokuda[2], Emi Makino[2], Takahiro Kanda[2], Naohiro Sugiyama[2, 3], Hironari Kuno[2], Jun Kojima[2] and Hidekazu Tsuchida[1]; [1]CRIEPI (Central Research Institute of Electric Power Industry), Japan; [2]Denso Corporation, Japan; [3]National Institute of Advanced Industrial and Technology (AIST), Japan.

11:30 AM MO.A1.3
High-Quality SiC Solution Growth Using Dislocation Conversion on C Face
Shiyu Xiao[1], Shunta Harada[2, 1], Xinbo Liu[1], Kenta Murayama[2], Ryota Murai[3], Miho Tagawa[2, 1] and Toru Ujihara[2, 1, 4]; [1]Nagoya University, Japan; [2]Nagoya University, Japan; [3]Nagoya University, Japan; [4]National Institute of Advanced Industrial Science and Technology, Japan.

11:45 AM MO.A1.4
Homoepitaxial Growth of Isotopically Enriched 3C- 6H- and 4H-$^{28}Si^{12}C$
Jawad Ul Hassan[1], Robin Karhu[1], Björn Lundqvist[1], Ivan G. Ivanov[1], Björn Magnusson[2], Örjan Danielsson[1], Olof Kordina[1] and Erik Janzén[1]; [1]Linköping University, Sweden; [2]Norstel AB, Sweden.

12:00 PM *MO.KN.A2.1 (Keynote)
Status and Challenges for Large-Diameter SiC Substrates
Yuri Khlebnikov[1], Robert Leonard[1], S. Bubel[1], J. Ambati[1], Adrian Powell[2], A. R. Paisley[1], E. Deyneka[1], I. Currier[1], V. Tsvetkov[1], J. Seaman[1], Michael O'Loughlin[1], Edward R. Van Brunt[1], Al Burk[1] and E. Balkas[1]; [1]Wolfspeed, United States; [2]Cree, Inc., United States.

MOS Processing

Session Chairs: Philippe Godignon and Aivars Lelis
Monday Afternoon, September 18, 2017
Thurgood Marshall Ballroom, North Salon
2:15 pm – 4:15 pm

2:15 PM MO.C2.1
Novel Gate Insulator Process by Nitrogen Annealing for Si-face SiC MOSFET with High-Mobility and High-Reliability
Shunsuke Asaba, Tatsuo Shimizu, Yukio Nakabayashi, Shigeto Fukatsu, Toshihide Ito and Ryosuke Iijima; Toshiba Corporation, Japan.

2:30 PM MO.C2.2
Unraveling the Oxidation Mechanisms Taking Place in Early Steps of 4H-SiC Dry Thermal Oxidation
Gustavo Dartora[2], Eduardo Pitthan[2] and Fernanda Stedile[2, 1]; [1]Universidade Federal do Rio Grande do Sul, Brazil; [2]Universidade Federal do Rio Grande do Sul, Brazil.

2:45 PM MO.C2.3
Isotropic Oxidation of SiC by Atomic Oxygen and Investigation of RIE Induced Effects for Development of 4H-SiC Trench MOSFETs
Asanka Jayawardena[1], Ayayi C. Ahyi[1], Tamara Isaacs-Smith[1], Gang Liu[2], Robert G. Shaw[2] and Sarit Dhar[1]; [1]Auburn University, United States; [2]Texas Instruments Incorporated, United States.

3:00 PM MO.C2.4
Effect of High Temperature Forming Gas Annealing on Electrical Properties of 4H-SiC Lateral MOSFETs with Lanthanum Silicate and ALD SiO_2 Gate Dielectric
Minseok Kang, Kevin Lawless, Bongmook Lee and Veena Misra; North Carolina State University, United States.

3:15 PM MO.C2.5
Interface Property of SiO_2/4H-SiC(0001) Structures Formed by Ultrahigh-Temperature Oxidation under Low Oxygen Partial Pressure
Takuji Hosoi[1], Yoshihito Katsu[1], Daisuke Nagai[1], Hidenori Tsuji[1, 2], Mitsuru Sometani[3], Takayoshi Shimura[1] and Heiji Watanabe[1]; [1]Osaka University, Japan; [2]Fuji Electric Co., Ltd, Japan; [3]National Institute of Advanced Industrial Science and Technology, Japan.

3:30 PM *MO.KN.C2.1 (Keynote)
Processing Comparison of SiC Planar and Trench MOSFETs—The Case for Trenches
Dethard Peters[1] and Wolfgang Bergner[2]; [1]Infineon Technologies AG, Germany; [2]Infineon Technologies Austria, AG, Austria.

Lifetime and Optical Characterization

Session Chair: Peder Bergman and Marko Tadjer
Monday Afternoon, September 18, 2017
Thurgood Marshall Ballroom, West Salon
2:15 pm – 4:15 pm

2:15 PM *MO.KN.B2.1 (Keynote)
Epitaxial Material Challenges for High-Voltage SiC Devices
Tsunenobu Kimoto; Kyoto University, Japan.

3:00 PM MO.B2.1
Microscopic FCA System for Depth-Resolved Carrier Lifetime Measurement
Shinichi Mae[1], Takeshi Tawara[2, 3], Hidekazu Tsuchida[4] and Masashi Kato[1]; [1]Nagoya Institute of Technology, Japan; [2]National Institute of Advanced Industrial Science and Technology, Japan; [3]Fuji Electric Co., Ltd., Japan; [4]Central Research Institute of Electric Power Industry, Japan.

3:15 PM MO.B2.2
Depth Profiling of Carrier Lifetime in Thick 4H-SiC Epilayers Via TPA
Nadeemullah A. Mahadik[1], Robert Stahlbush[1], Paul Klein[2], Ani Khachatrian[2] and Stephen Buchner[1]; [1]Naval Research Laboratory, United States; [2]Sotera Defense, United States.

3:30 PM MO.B2.3
Short Minority Carrier Lifetimes in Al- and (Al+B)-Doped P-Type Epilayers
Koichi Murata[1], Takeshi Tawara[2, 3], Anli Yang[1] and Hidekazu Tsuchida[1]; [1]Central Research Institute of Electric Power Industry (CRIEPI), Japan; [2]National Institute of Advanced Industrial Science and Technology (AIST), Japan; [3]Fuji Electric Co., Ltd., Japan.

3:45 PM MO.B2.4
Analysis of Carrier Capture and Recombination Processes in Intentionally N+B Doped *N*-Type 4H-SiC Epilayers
Anli Yang[1], Tetsuya Miyazawa[1], Takeshi Tawara[2], Koichi Murata[1] and Hidekazu Tsuchida[1]; [1]Central Research Institute of Electric Power Industry (CRIEPI), Japan; [2]National Institute of Advanced Industrial Science and Technology, Japan.

4:00 PM MO.B2.5
Aluminum Doping Concentration Calibration by Photoluminescence in High-Quality Uncompensated P-Type 4H-SiC
Satoshi Asada[2], Tsunenobu Kimoto[2] and Ivan G. Ivanov[1]; [1]Linköping University, Sweden; [2]Kyoto University, Japan.

Tutorial

SiC MOSFET Design II

Session Chair: Victor Veliadis
Monday Afternoon, September 18, 2017
Thurgood Marshall Ballroom, North Salon
5:15 pm – 6:15 pm

5:15 PM
SiC MOSFET Design—Advantages, Challenges and Strategies
B. Jayant Baliga, North Carolina State University