SYMPOSIUM D

Advanced Materials and Devices for Large-Area Electronics

April 17 – 20, 2001

Chairs

James S. Im
Div of Materials Science & Engineering
Columbia Univ
500 W 120th St
New York, NY 10027-6623
212-854-8341

Thomas E. Felter
Lawrence Livermore Natl Lab
PO Box 808
Livermore, CA 94550
925-422-8012

Juergen H. Werner
Inst fur Physikalische Elektronik
Stuttgart Univ
Stuttgart, 70569 GERMANY
49-711-685-7141

Shuichi Uchikoga
LCD R&D Center
Toshiba Corp
Saitama, 366-8510 JAPAN
81-48-574-2882

Hyun Jae Kim
AMLCD Division
Samsung Electronics Co
San 24 Nongseo-Ri
Kyungki-Do, 449-771 KOREA
82-331-209-3485

Tolis T. Voutsas
Sharp Laboratories of America
Camas, WA 98607
360-834-8646

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SESSION D1: LARGE AREA ELECTRONICS I: LITHOGRAPHY/PATTERNING

Chairs: Tolis T. Voutsas and Hans-Juergen Kahlert
Tuesday Morning, April 17, 2001
Franciscan I (Argent)

8:30 AM *D1.1
LARGE-AREA, HIGH-RESOLUTION MATERIALS SURFACE PROCESSING WITH EXCIMER LASERS. Kanti Jain, Marc Zemel, Marc Klosner, Robert Sposili, Anvik Corporation, Hawthorne, NY.

Advances in microelectronics, such as higher speeds and higher densities, continue to place greater demands on electronic systems fabrication and on the equipment used in their production. One of the basic needs of microelectronics manufacturing is the ability to modify material surfaces in very localized areas. Examples of processes requiring such high-resolution surface modification include photolithography, micromachining, and patterned annealing/ recrystallization. Simultaneously, the demand for higher production efficiencies continues to drive manufacturing processes towards larger areas and higher throughputs. Excimer lasers provide many advantages for surface processing of materials. Significant amounts of energy in the ultraviolet range can be delivered to a surface in a controlled manner with rapidity and precision. The high-power ultraviolet radiation can be used to produce a wide variety of materials surface modifications, including photo-induced polymerization/dissolution of photoresists, ablation of organic and inorganic materials, and patterned annealing/recrystallization of metals and semiconductors. While excimer-laser-based systems with high-resolution patterning capability have been extensively developed, available systems are not well suited for patterning over large areas, nor are they designed for high-fluence applications such as ablation and recrystallization. Conversely, conventional excimer laser annealing systems are designed to process the entire surface of a material in a flood illumination manner, and do not possess the capability to process materials in well-defined localized areas. This paper will describe recent advances in excimer laser projection technology that make it possible to conduct localized materials processing to produce features as small as 1 micron in size over a large area in a highly efficient, high-throughput manner. The technology can be used for any application requiring patterning of such features over large rigid or flexible substrates, including lithography for displays and printed circuit boards, large-area ablation and annealing/recrystallization.

9:00 AM *D1.2
ABLATION LITHOGRAPHY FOR TFT-LCD. Kenkichi Suzuki, Nobuaki Hayashi, Displays, Hitachi, Ltd., Mobara, JAPAN; Hiroshi Masuhara, Applied Phys. Dept., Osaka Univ., Osaka, JAPAN; Thomas Lippert, PSI, Villingen, SWITZERLAND.

This paper presents a proposal of two technologies to break through the throughput of the TFT-LCD lithography. They are based on the photo-decomposition ablation of polymer materials by excimer laser. One is "self-development", in which the exposure is at the same time development of resist films. The other is "resist transfer" which makes use of explosive propellant by polymer ablation. The former technology consists of four basic techniques; excimer laser source, exposure & aligner machine system, dielectric multiplayer masks, and ablation resist materials. Using an experimental exposure & aligner equipment, we made a TFT pattern on 300×400 mm^2 glass substrate, and proved feasibility for large area lithography. We fabricated various kinds of masks, and also simulated a limitation in resolution due to the dielectric multilayer structure. The result is it is almost same to Cr masks up to N.A.= 0.2 optical system, which is sufficient for a-Si TFT. The most important factor of the throughput is the ablation rate of the resist material. The maximum rate is found to be 0.1 μ/shot at 100mJ/cm^2 measuring more than two hundred materials. The resultant throughput time by the technology is estimated to be 2 or 3 times of that of up-to-date manufacturing lines, and it is mainly due to the ablation rate. The main components of the resist transfer are a transfer film and imaging optics. The transfer film is consists of an UV transparent base film, ablation layer and positive type resist film. A resist pattern is imaged from the rear of the base film on to the ablation layer. Only one shot illumination is enough to produce gas, which thrust out the resist film partly hardened by leaked UV light. The scheme ensures 10 to 100 times throughput in principle. Both the technologies indicate importance of resist materials, and renewal of basic researches on polymer ablation would open new fields of LCD industry.

9:30 AM D1.3
MINIATURIZATION OF OFFSET PRINTING DOWN TO THE MICROSCALE. Anton A. Darhuber, Scott M. Miller, Sandra M. Troian, Jeffrey M. Davis, Princeton Univ, Dept of Chemical Engineering, Princeton, NJ; Sigurd Wagner, Princeton Univ, Dept of Electrical Engineering, Princeton, NJ.

We are exploring the wet printing of liquid microstructures in the range of 1-100 microns as a fast and parallel method of fabricating microelectronic patterns and components. Besides the materials issues pertinent to ink formulation for rheological control and the design and fabrication of the printing plates, successful liquid transfer requires precise and uniform distribution of liquid on micropatterned surfaces. Our fundamental studies of offset printing at the microscale have focused on the hydrodynamic behavior of liquid deposition, transfer, and pattern stabilization. The printing plates consist of silicon wafers or glass slides of patterned wettability imposed by selective monolayer silanization. The liquid inks consist of polar liquids or polymer solutions that adhere only to the hydrophilic regions. Selective ink deposition with a film thickness in the micron range is obtained either by dip-coating or meniscus coating. The breakup and recession of the initial liquid coating to the hydrophilic regions of the printing plate can be controlled to produce liquid structures of uniform height, independent of pattern geometry. For the case of straight lines, we have developed a model, which predicts the deposited film height as a function of the relevant material and process parameters. The dynamics of liquid transfer and plate separation normally cause pattern distortions, as the liquid spreads over or recedes from the nonporous target substrate. To overcome this difficulty, the liquid-solid contact line on the target surface must be pinned during transfer. We have studied this process with curable inks that solidify upon exposure to ultraviolet light. Using design rules for the printing process obtained by experiment and simulations, we have so far successfully printed thin patterned films with dimensions ranging from 5-100 microns on both silicon and glass. This research is supported by the MLP program of DARPA.

SESSION D2: LARGE AREA ELECTRONICS II: NOVEL METHODS AND APPLICATIONS

Chairs: Tolis T. Voutsas and Hans-Juergen Kahlert
Tuesday Morning, April 17, 2001
Franciscan I (Argent)

10:15 AM *D2.1
MONOCRYSTALLINE SILICON FILMS FROM TRANSFER PROCESSES FOR THIN FILM DEVICES. Ralf B. Bergmann, Institute of Physical Electronics, University of Stuttgart, GERMANY.

A large number of approaches are currently being investigated around the world to fabricate monocrystalline silicon films for silicon on insulator devices, active matrix displays and thin film solar cells on foreign substrates. Approaches based on the formation of polycrystalline silicon films are limited in material quality and therefore cannot satisfactorily serve all the above mentioned areas of device application. The paper discusses prospects and limitations of approaches aimed at the formation of monocrystalline silicon films on insulating or foreign substrates and describes the transfer of quasi-monocrystalline silicon films, an approach developed at our institute. Using silicon absorber films epitaxially grown on quasi-monocrystalline silicon, we fabricate thin film solar cells on glass with a conversion efficiency of 14%. Our device results not only demonstrate the high quality of our monocrystalline films but also demonstrate the feasibility of device processing based on quasi-monocrystalline silicon films.

10:45 AM *D2.2
TRENDS IN MICROELECTRONIC SYSTEMS INTEGRATION: FROM SYSTEM ON A CHIP TO SYSTEM IN A PACKAGE. Robert H. Reuss, Babu R. Chalamala, and Simon Thomas, Motorola, Inc., Semiconductor Products Sector, Digital DNA Laboratory, Tempe, AZ; Marc Chason, Daniel Gamota and Janice Danvir, Motorola, Inc., Advanced Technology Center, Schaumburg, IL.

The continued shift towards the integration of diverse functions into single chips and chip assemblies requires a new vision in microelectronic systems integration. Over the last decade or so, there has been a tremendous push towards systems on chip (SoC) approach for increased functionality. While systems on a chip has received much deserved credit for the size and cost reduction of many products, a true system on a chip solution has not been practical for a number of applications. In some cases, this is simply an issue of chip size, in others material compatibility (Si and GaAs), in yet others electrical compatibility (high voltage, RF, analog, with digital) and in some others the overall cost of integration on silicon, even if technically feasible. The need to combine diverse materials and technologies to achieve increased functionality with decreased size and weight, along with the ever present pressure for lower cost, has created the opportunity for new system level integration opportunities. Among the new concepts, system in a package (SiP) and system on a substrate (SoS) have received the most attention. System in a package is a natural extension of system on a chip concept. Currently, there are aggressive programs to develop SiP capabilities to allow rapid, cost effective design and fabrication of sub-system level packages.

System on a substrate is an emerging concept based on the integration of technologies in a wide area of electronics. SoS will take the next step to the full system level (e.g. a monolithic radio). However, there is another important concept that seeks the same objective of system-level integration, but with a different set of drivers. In situations where the product is required to be a certain size (e.g. a display or a smart card), further size reductions of the components is no longer productive. This creates the opportunity for alternative technologies such as thin film transistors and plastic substrates. Integration of these technologies offers the potential for significant cost savings because of lower manufacturing costs, and light weight, wearable, flexible products by elimination of today's rigid substrates. Such technologies not only offer new capabilities, but also change the basic premise of the electronics industry. We could move from the microelectronics to the macroelectronics era. In this paper, we will present an overview of this diverse and emerging technology.

11:15 AM D2.3
FLAT PANEL IMAGERS BASED ON EXCIMER LASER ANNEALED, POLY-Si THIN FILM TRANSISTOR TECHNOLOGY. J.P. Lu, K. Van Schuylenbergh, R.T. Fulks, J. Ho, Y. Wang, R. Lau, P. Nylen, P. Mei, M. Mulato, J.B. Boyce, and R.A. Street, Xerox Palo Alto Research Center, Palo Alto, CA.

Pulsed Excimer-Laser Annealing (ELA) has become an important technology to produce high performance, ploy-Si Thin Film Transistors (TFTs) for large area electronics. The much-improved performance of these poly-Si TFTs over the conventional hydrogenated amorphous Si TFTs enables the possibility of building next generation flat panel imagers with higher-level integration and better noise performance. Both the on-glass integration of peripheral driver electronics to reduce the cost of interconnection and the integration of pixel level amplifier to improve the noise performance of large area imagers have attracted much interest and are under development based on this new technology. In this talk, we will report the progress and current status of our effort in building advanced flat panel imagers based on poly-Si TFT technology. With our low leakage current (0.02fA/μm), high performance (mobility > 100 cm^2/Vs) poly-Si TFT process, we have successfully demonstrated a prototype imager (384x256 pixels) using poly-Si TFTs as pixel switches. Good image quality and good uniformity have been achieved as a result of the low and narrow distribution of TFT leakage current (average 13 fA/pixel, with full width half maximum of 20 fA). Integrated peripheral driver electronics have been designed with high tolerance of process variations. On-glass, integrated gate-line drivers including 256 stages static shift registers and buffers for driving high capacitive load have been realized and have been shown to run the prototype imagers successfully without using external gate-line electronics. Poly-Si TFT process, integrated peripheral circuits, and performance of the poly-Si prototype imager, as well as the development of pixel level electronics will be discussed.

11:30 AM D2.4
JOINED-WAFER SILICON A NEW TECHNOLOGY FOT LARGE AREA ELECTRONICS? Jürgen H. Werner, Xinmin Cao, Titus Rinke, and Ralf B. Bergmann, University of Stuttgart, Institute of Physical Electronics, Stuttgart, GERMANY.

Today, the growth of silicon single crystals is limited to a diameter of 12 inches. As a consequence, bulk Si wafers as well as films from transfer techniques are also limited to this size. The new technique of joined-wafer silicon (jw-Si) promises a new way for the preparation of *single* crystalline, large area silicon films, layers, and probably also wafers of - in principle unlimited size. The underlying concept of jw-Si is simple: Two (or more) rectangular "prime" wafers are joined together, for example, by closing the gap between their edges by lateral epitaxy. In a second step thin single crystalline layers are "peeled-off" from this large area "master" sheet by any technique such as SMARTCUT, ELTRAN, or QMS-Si. The peeled-off film is then transferred to a "slave" substrate, such as an oxidized Si wafer, a substrate from ceramics, or from glass. Before forming the master sheet by lateral epitaxy, the edges of the "prime" wafers may be structured with the help of micromechanical techniques. The surfaces of both wafers (or films) might be oxidized in order to suppress epitaxy there. After the lateral epitaxy or welding, the two wafers (or films) are joined to a larger single crystal. With this technique, one is not limited to the circular shape of wafers from bulk crystal growth. Our first experiments showed that wafers of silicon can be joined together over several cm length even without particularly careful sample preparation. Thus, we have a proof of concept for jw-Si.

11:45 AM D2.5
LARGE AREA MEMS: MATERIALS ISSUES AND APPLICATIONS. J.H. Daniel, B. Krusor, M. Mulato, R.B. Apte, R. Lau, Y. Wang, J.P. Lu, R.A. Street, Xerox Palo Alto Research Center, Palo Alto, CA; A. Goredema, D.C. Boils-Boissier, P.M. Kazmaier, Xerox Research Center Canada, Mississauga, Ontario, CANADA.

Conventional MEMS devices are based on silicon micro-machining and their maximum size is limited by the wafer. In contrast, we are exploring micro-machining for large area applications on substrates such as glass using polymeric materials. Our research is focused on the photopolymer SU-8, and we apply the MEMS fabrication technology to large area image sensors and displays. There are many challenges concerning the materials and processes, since large area compatibility is essential and integration with large area electronics may be required. The adhesion of SU-8 to the underlying layers as well as stress in the SU-8 are issues which have been studied using modified SU-8 materials together with adhesion promoters. Three applications of SU8 MEMS are discussed to motivate the technology and illustrate large area applications: First, in the fabrication of an X-ray imager, high aspect ratio SU-8, 200-400 microns thick, is employed to form a micro-patterned phosphor screen to increase image resolution. The SU-8 cell structure is made reflective by sputter-coating aluminum and phosphor powder is filled into the cells using a doctor-blading method. The performance of this screen is compared with commercially available phosphor layers. Second, a similar approach of patterning SU-8 into arrays of micro-cells is applied to an electrophoretic display. The SU-8 cells prevent agglomeration of the color pigments and they define the pixels in active-matrix electrophoretic displays. The formation of SU-8 cells on top of an active matrix array will be discussed. Third, SU-8 is alsoinvestigated as a thick (tens of microns) inter-layer dielectric (ILD) for reduced capacitive coupling in large area electronic circuits. In particular, SU-8 is integrated into the fabrication of an X-ray image sensor array. Initial results concerning the compatibility of SU-8 with the amorphous silicon deposition for the photo sensors will be shown.

SESSION D3: METAL INDUCED CRYSTALLIZATION OF a-Si FILMS
Chairs: Stephen J. Fonash and Tolis T. Voutsas
Tuesday Afternoon, April 17, 2001
Franciscan I (Argent)

1:30 PM *D3.1
SILICIDE MEDIATED CRYSTALLIZATION OF AMORPHOUS SILICON. Jin Jang, Seong Jin Park, Kyung Hee Univ, Dept of Physics and TFT-LCD Natl Lab, Seoul, KOREA.

Low-temperature polycrystalline Si (poly-Si) has become of great interest for large-area electronics such as flat panel display (FPD), solar cell and image sensor. Poly-Si films can be prepared by several methods: solid-phase crystallization (SPC) of amorphous silicon (a-Si), excimer laser annealing (ELA), metal induced lateral crystallization (MILC), silicide mediated crystallization (SMC) and direct deposition by plasma enhanced chemical vapor deposition (PECVD). Among them, ELA, SMC and direct deposition methods can be utilized for large-area poly-Si on glass substrate. However, the poly-Si formed by direct deposition has a lot of defects that degrade the performace of electronic devices. Also, ELA has some problems should be solved such as large-area uniformity and high manufacturing cost. We proposed an alternative method for the formation of high quality low-temperature poly-Si. A-Si could be crystallized into poly-Si by means of field enhanced SMC (FE-SMC) method. In this crystallization method, main factor accelerating crystallization speed is not electric current but electric field. As for microstucture, $< 111 >$ directional needlelike crystallite grown from precipitate with $\{110\}$ faces oriented to the film surfce is dominantly observed. It means that the film is mostly crystallized by in-plane growth of needlelike crystallites from the migration of $< 110 >$ oriented $NiSi_2$ precipitates. Even at 350°C, Ni atoms migrate in the a-Si network and form $NiSi_2$ precipitates that induce crystallization. The formation of nuclei and crystallization from them will be discussed in detail. In addition, the effect of impurity (P and B) on the SMC will be explained together with TFT performances. The field effect mobility above 120cm^2/Vs has been achieved using the SMC poly-Si crystallized at 450°C within 30 min.

2:00 PM D3.2
OPTICALLY ASSISTED METAL-INDUCED CRYSTALLIZATION OF THIN Si FILMS FOR LOW-COST SOLAR CELLS. Wei Chen, Bhushan Sopori, Kim Jones, Robert Reedy, National Renewable Energy Laboratory, Golden, CO; N.M. Ravindra, New Jersey Institute of Technology, Newark, NJ; Roger Aparacio, Robert Birkmire, University of Delaware, Institute of Energy Conversion, Newark, DE; Scott Morrison, Ken Coats and Arun Madan, MV Systems, Golden, CO.

We have grown large-grain, crystalline Si thin films on glass/quartz substrates using optically enhanced, Al-induced crystallization (OEAIC) of amorphous silicon (a-Si). The a-Si films, 0.5 to 10 μm thick, were deposited on Al-coated glass substrates by various deposition methods including sputtering, hot-wire CVD, and plasma

CVD at temperatures up to 600°C. The resultant amorphous or fine-grain Si samples were processed by optically heating the films with a tungsten halogen light source operated to produce an IR-rich spectrum. In our experiments, we controlled the incident light flux (hence, the process temperature) of the sample and the process time. The optical heating for grain enhancement was compared with furnace heating to identify the role of illumination. The samples were analyzed for grain size, initiation and degree of crystallization, and propagation of growth front, and the depth profile of Al. Major results include the following: ♦ Microcrystalline Si can be made by optical processing at temperatures < 550°C with much shorter time, compared with thermal crystallization/grain-enhancement techniques. ♦ Crystallization of Si films by optical processing can be mediated by the presence of Al at temperature as low as 200°C. Strong crystallization and grain enhancement (grain size exceeding 1 μm) occurs when the processing temperature exceeds 450°C. ♦ OEAIC induces much stronger initial reactions on the Al/Si interface than the conventional annealing process. OEAIC also provides better control on Al content in the crystallized film. ♦ The initial crystallization is mediated by an Al/Si reaction at the interface. Once the crystallization has started, the crystallization front moves into a-Si without requiring high Al content. This paper will discuss the role of metal and the optical excitation in crystallization and will explain the temperature dependence and the role of metal in crystallization using a qualitative model for metal-induced crystallization.

2:15 PM D3.3
THE VARIATION OF MILC DEPENDING ON THE DEPOSITION TEMPERATURE OF AMORPHOUS SILICON. Yeo-Geon Yoon, Gi-Bum Kim, Seok-Woon Lee and Seung-Ki Joo, School of Material Science and Engineering, Seoul National Univ, Seoul, KOREA.

There is a need for low temperature crystallization of amorphous Si(a-Si) thin films on glass substrate for integrated TFT-LCD. Metal-Induced Lateral Crystallization (MILC) is a very advantageous method for low temperature (below 500°C) crystallization of a-Si. We studied the effect of the deposition temperature of a-Si thin films on the MILC. a-Si thin films were prepared by Plasma Enhanced Chemical Vapor Deposition (PECVD) with silane and hydrogen gas at 100-400°C. 50Å-thick Nickel films were deposited on it by magnetron sputtering system for the purpose of MILC. Then specimens were annealed in 3 zone tube furnace at 450-550°C in N_2 ambient. a-Si films deposited at higher deposition temperature($>$ 250°C) showed faster MILC rate than a-Si films deposited at lower temperature ($<$ 200°C). The variation of the deposition temperatures of a-Si films also made the differences of crystal-growing shapes. Low temperature a-Si films were crystallized in the shape of needle. But high temperature a-Si films showed a flat interface between a-Si and poly-Si. These effects were resulted from the difference of the hydrogen concentration in a-Si and of the structural change of a-Si during the dehydrogenation.

2:30 PM D3.4
HIGH QUALITY POLY-Si FILM AND TRANSISTOR FORMED BY NICKEL-INDUCED-LATERAL-CRYSTALLIZATION AND PULSED-RAPID-THERMAL-ANNEALING. T.C. Leung, M.C. Poon, C.F. Cheung, G.K. Zhu, Dept. of Electrical and Electronic Engineering, Hong Kong University of Science and Technology, Sai Kung, HONG KONG.

Low temperature high quality poly-silicon (poly-Si) film can have numerous novel applications in Large Area Electronics. Recently, nickel-induced-lateral- crystallization (NILC) of amorphous Si (a-Si) has successfully achieved large grain (micron size) poly-Si film and SOI like thin film transistor (TFT). However the poly-Si growth rate is slow (~1.5μm/hour at 550°C) and annealing time is usually very long. This work presents a new method to combine NILC and pulsed-rapid-thermal-annealing (PRTA) to shorten the anneal time and to obtain high quality low temperature poly-Si and TFTs. 1000Å of LPCVD a-Si was deposited on 7000Å of thermal oxide, followed by 4000Å of LTO. LTO was patterned and 50Å of nickel was deposited. NILC of a-Si was then performed at a new PRTA process of 650-750°C for 3-10 sec (heating) and 20-60 sec (cooling) for 10-30 cycles in N2. Results show that the poly-Si growth rate can be much increased to 1-2μm/minute. The poly-Si and the fabricated TFTs have much improved quality and I-V characteristics when compared to those obtained from the conventional 550°C long time process. The poly-Si and TFT parameters such as length, grain size, uniformity, mobility and quality due to different heating and cooling time, temperature and cycles, will also be reported and discussed.

2:45 PM D3.5
EXCIMER LASER ANNEALING EFFECT ON THE MILC AND THE MIC POLY-CRYSTALLINE SILICON FILMS. Kee-Chan Park, In-Hyuk Song, Jin-Woo Park, Sang-Hoon Jung, Seoul National Univ., School of Electrical Engineering, Seoul, KOREA.

Metal induced lateral crystallization (MILC) of a-Si film is promising for large area electronics. MILC features low cost, uniform crystallization over large area and low crystallization temperature due to the catalytic action of Ni during the crystallization of a-Si. However the electrical characteristics of MILC poly-crystalline silicon (poly-Si) film may not be comparable to that of excimer laser annealed (ELA) poly-Si film. The superior electrical characteristics of the ELA poly-Si film are attributed to the lower defect density due to melting and resolidification mechanism of ELA. The purpose of our work is to report a new low-temperature recrystallization method of a-Si film by combining the merits of MILC and ELA. We irradiated XeCl excimer laser on the MIC and the MILC poly-Si film which had Ni content of 5 at. % and 0.002 at. % respectively. Transmission electron microscopy (TEM) and secondary ion mass spectrometry (SIMS) analysis were used to investigate the mechanism of poly-Si grain growth in ELA of the MIC and the MILC poly-Si film which had different Ni content. As the Ni content in the poly-Si film increases, the melting temperature of the poly-Si film decreases and the nucleation rate of the poly-Si grain increases. Poly-Si grains nucleated from the Ni-rich MIC poly-Si grow into the MILC poly-Si which is not yet crystallized due to low nucleation rate. 2 μ long poly-Si grains were successfully grown at the boundary between the MIC poly-Si and the MILC poly-Si after the laser annealing for the laser energy density of 370mJ/cm^2. It should be noted that the poly-Si grain size crystallized by the conventional ELA is less than 0.5 μ long. Out experimental results show that the combination of ELA and MILC may be very useful for the fabrication of the high-performance poly-Si thin film transistors.

SESSION D4: CONTROLLED LATERAL SOLIDIFICATION OF Si FILMS
Chairs: Eric Fogarassy and Juergen H. Werner
Tuesday Afternoon, April 17, 2001
Franciscan I (Argent)

3:30 PM *D4.1
ADVANCED EXCIMER-LASER RECRYSTALLIZATION TECHNOLOGY FOR CRYSTAL-Si THIN-FILM DEVICES. Masakiyo Matsumura, Dept of Physical Electronics, Tokyo Institute of Technology, Meguro-ku, Tokyo, JAPAN.

An advanced excimer-laser annealing method of Si thin-films has been reviewed aiming at ultra-large grain growth with high packing density by a single shot light pulse irradiation. Key concepts are two-dimensional modulation of laser light intensity on the sample surface, reduction of heat removal rate from the molten Si thin layer of high temperature to the cool underlayer, and enlargement of the effective specific-heat while keeping the effective thermal-conductivity low for the annealed layers. There were two possible solutions for the first condition. The first one is an application of a couple of phase shift masks; one having smooth phase shift patterns placed at several mm apart from the sample, and the other having step-like phase shift patterns placed just on the sample. Another solution is a half-tone phase-modulation method using a semi-transparent phase-shift mask. The second condition was cleared by changing the SiO_2 underlayer to the porous SiO_2 or organic SOG underlayer. The third condition was satisfied, in the case of a KrF excimer laser, by the bi-layer structure of the SiON capping layer and the ultra-thin Si layer, since SiON has a reasonable light absorption coefficient, a low thermal conductivity, a large specific heat and a sufficient heat tolerance.

4:00 PM *D4.2
A NEW POLY-Si TFT WITH A SINGLE GRAIN BOUNDARY BY XECL ELA ON PREPATTERNED Al LAYER. Min-Koo Han, Sang-Hoon Jung, Jae-Hong Jeon, School of Electrical Engineering, Seoul National University, Seoul, KOREA.

Polycrystalline thin film transistor (poly-Si TFT) recrystallized by excimer laser annealing (ELA) is a promising device for active matrix liquid crystal displays (AMLCDs) due to high field-effect mobility and driving capability. The characteristics of poly-Si TFT are critically dependent on the grain size and the in-grain defect density. Various efforts have been paid in order to increase the grain size. Sequential lateral solidification (SLS) may be the most effective. However SLS requires a rather sophisticated beam scan process. Recently, we have reported that the excimer laser irradiation on amorphous silicon (a-Si) with prepatterned aluminum (Al) layer induces the lateral grain growth effectively. The laser irradiation on a-Si film with the Al pattern results in the selective melting of a-Si due to its high UV-reflectance. The large temperature gradient between the molten and unmolten regions causes the nucleation to be initiated preferentially at the edge of Al pattern and the lateral grain size increases up to micrometer range. Our method does not require any additional accurate motion controllers and is carried out by a single pulse while the SLS requires an elaborated beam scanning. We report a single grain boundary poly-Si TFT fabricated by the proposed excimer laser annealing. The Al patterns have been allocated on the

source and drain. After the excimer laser irradiation for the recrystallization of the channel layer, the nucleation is initiated at both the edges of the source and drain, and the grains grow in a lateral direction. The lateral grains form a single grain boundary impinging at the center of the channel. It should be noted that the sub-grain boundaries along the grain growth could be neglected because the current path is parallel with the direction of the sub-grain boundaries. The homogeneous nucleation, which may occur in the center of a long channel poly-Si TFT, has been eliminated by the reduction of the channel length. The electrical characteristics of the proposed poly-Si TFT have been improved considerably due to the lowered grain boundary density. We also report the various electrical characteristics such as high mobility as high as $200cm^2/Vsec$ and low leakage current.

4:30 PM D4.3

A NEW DOUBLE LASER RECRYSTALLIZATION TECHNIQUE TO INDUCE ULTRA-LARGE POLY-Si GRAINS. Minghong Lee and Seungjae Moon, University of California, Department of Mechanical Engineering, Berkeley, CA; Mutsuko Hatano, Hitachi Ltd., Hitachi Laboratory, Tokyo, JAPAN; Costas P. Grigoropoulos, University of California, Department of Mechanical Engineering, Berkeley, CA.

A new double laser recrystallization technique which can produce ultra-large direction- and location-controlled lateral grains is presented. An excimer laser and a pulse modulated Ar laser are used. Grains of tens of micrometers in size are obtained. The effect of different parameters on lateral grain growth is investigated. These parameters include the time delay between the two lasers, the excimer laser fluence, the Ar laser power and the pulse duration. The process is insensitive to both the excimer laser fluence and the Ar laser power fluctuations. Preheating and melting of the a-Si film with the Ar laser before firing the excimer laser is found to be necessary for inducing lateral grain growth. The transient excimer laser irradiation is believed to generate nucleation sites for initiating the subsequent lateral grain growth. The solidification dynamics of the process is probed by high spatial and temporal resolution flash laser imaging. The surface roughness of the recrystallized poly-Si is measured by atomic force microscope.

4:45 PM D4.4

A NEW SAMPLE STRUCTURE FOR EXCIMER-LASER GROWTH OF LARGE AND ULTRATHIN Si GRAINS. Wen-Chang Yeh and Masakiyo Matsumura, Dept. Physical Electronics, Tokyo Institute of Technology, Tokyo, JAPAN.

$20\mu m$-long (about 50 times larger than the typical size) grains were grown in the ultrathin Si layer of 50nm in thickness on the conventional SiO_2 underlayer by a Phase-Modulated Excimer-Laser Annealing (PMELA) method using a KrF excimer laser [1]. This dramatic enlargement results from the light-absorbable, heat-tolerant and thermally low conductive SiON capping layer on the Si film [2]. Large acceptable heat energy and its slow removal rate are the most important requirements for long lateral grain growth based on the PMELA method. These conditions could be satisfied by a layered structure of the thick SiON layer and the ultrathin Si layer as follows. The ultrathin Si layer reduces the lateral diffusion of heat, resulting in keeping of a suitable temperature gradient along the Si layer for a long time. The reduced latent heat suppresses unwanted and local temperature elevation at the melt-solid interface [3]. These effects keep the grain growth rate at the highest value. The thick SiON layer stores a large amount of energy by absorbing KrF laser light, and transfer it vertically to the molten Si film for a long time, resulting in elongation of the grain growth time. These accumulated effects elongate dramatically the grain growth length, which is given by a product of the growth time and the growth rate. And the organic SOG or porous underlayer can reduce further the heat removal rate from the molten Si layer, and, in turn, will further elongation of the grain size [4-5]. It is worthy to note that the similar effects are expected also, but only a limited amount, for the layered structure of SiO_2 and Si. This is because SiO_2 cannot absorb the KrF excimer-laser light and thus the excess heat in the SiO_2 layer prepared from the Si thin layer within a short time is limited. References: [1]Yeh et al., To be published in Jpn. J. Appl. Phys., [2]Ozawa et al., Jpn. J. Appl. Phys., 38 (1999) 5700., [3]Yeh et al., To be published in Jpn. J. Appl. Phys., [4]Yeh et al., To be published in Jpn. J. Appl. Phys., [5]Yoshimoto et al., AMLCD 2000.

SESSION D5: POSTER SESSION MATERIALS AND DEVICES FOR LARGE AREA ELECTRONICS

Chairs: James S. Im, Thomas E. Felter, Juergen H. Werner, Shuichi Uchikoga and Hyun Jae Kim
Tuesday Evening, April 17, 2001
8:00 PM
Metropolitan Ballroom (Argent)

D5.1

VERY LOW TEMPERATURE E-GUN EVAPORATED SILICON DIOXIDE ON PLASTIC SUBSTRATES. Cheon-Hong Kim, Sang-Hoon Jung and Min-Koo Han, School of Electrical Engineering, Seoul National University, Seoul, KOREA.

Thin film devices on plastic substrates have attracted a considerable attention for large-area electronics due to their lightweight, flexibility and robustness. It is well known that a high-quality oxide deposited at very low temperature less than 200°C is a key factor to fabricate the devices. The SiO_2 deposited by widely used PECVD (plasma-enhanced chemical vapor deposition) at very low temperature would suffer from high-energy ion damage and inherent hydrogen inclusion. The purpose of our work is to report that a high-quality SiO_2 film suitable for the gate oxide on plastic substrates is successfully obtained by electron-gun (E-gun) evaporation at even room temperature. It should be noted that our E-gun evaporated oxide film is free from high-energy ion damage and hydrogen atoms. We have also investigated the effects of N_2O/N_2 plasma treatment on the E-gun evaporated oxide films. The SiO_2 powders with a purity of 99.999% were put in a cleaned graphite crucible. After a vacuum chamber was evacuated to a pressure of 10^{-6}Torr, the SiO_2 powders were evaporated by E-gun source with an emission current of about 100mA. Some samples were exposed to N_2O/N_2 plasma at 100°C in order to improve the oxide quality by high-energy oxygen and nitrogen radicals. MOS capacitors were fabricated on p-type silicon wafer to investigate high frequency (1MHz) C-V characteristics. Any hydrogen-related peak in the E-gun evaporated oxide film was not observed by the FTIR (Fourier-transformed infrared) absorption spectrum. The flat band voltage shift was less than ?V, which was comparable to that of TEOS (tetraethoxysilane) oxide deposited at 390°C. For the N_2O/N_2 plasma-treated samples for 1 minute, the flat band voltage shift was considerably reduced up to about ?V. Our experimental results show that very low temperature SiO_2 suitable for plastic substrates has been successfully obtained by the E-gun evaporation and N_2O/N_2 plasma post-treatment.

D5.2

STUDY ON THE POLYCRYSTALLINE SILICON FILMS DEPOSITED BY INDUCTIVELY COUPLED PLASMA CHEMICAL VAPOR DEPOSITION. Byeong Yeon Moon, Jae Hyung Youn, Sung Hwan Won and Jin Jang Department of Physics and Department of Information Display, Kyunghee University, Seoul, KOREA; S.M. Pietruszko, Institute of Microelectronics and Optoelectronics, Warsaw University of Technology, Warsaw, POLAND.

Polycrystalline silicon (poly-Si) thin films have been deposited by an inductively coupled plasma chemical vapor deposition (ICP-CVD) using SiH_4/H_2 mixtures. The plasma was generated by an inductively coupled azimuthal electrical field produced from a spiral antenna on the top of a dielectric quartz plate. The dielectric quartz plate was set on the stainless steel reactor chamber. The feeding gases were introduced from the dispersal ring into the reactor chamber for uniform gas flow. The SiH_4 flow rate and the deposition temperature were fixed at 1 sccm and 500 C, respectively. The hydrogen flow rate was varied between 0 and 40 sccm and a RF power between 500 and 1500 W was applied over a 6" inductor. The deposition rate increases gradually with increasing RF power and then decreases. A minimum value of 5.6 A/s is shown at 500 W ($3.1 W/cm^2$). When the RF power is 1000 W ($6.4 W/cm^2$), the deposition rate has a maximum value of 7.4 A/s. The increase in the deposition rate with increasing RF power correspond to the generation of more precursors and radicals. The Raman spectroscopy shown, that the amorphous peak was not found. Raman polycrystalline volume fraction increases to 83.6% with increasing RF power up to 1000 W, and then decreases when it is higher than 1000 W. The poly-Si deposited at 1 kW has a minimum FWHM and a maximum Raman peak intensity. An optimum RF power seems to be around 1 kW. The XRD peak intensity increases and FWHM decreases with increasing RF power up to 1000 W, thus suggesting the growth of larger grains. Conclusions: The quality of poly-Si can be improved by increasing RF power and hydrogen dilution ratio. The poly-Si deposited at a RF power of 1000 W with an addition of H_2, showed a Raman polycrystalline volume fraction of 85.7%, FWHM of $6.4 cm^{-1}$, deposition rate of 9.64 A/s and SEM grain size of $\sim$3000 A.

D5.3

CHARACTERISTICS OF LARGE-AREA PLASMA ENHANCED CHEMICAL VAPOR DEPOSITED TEOS OXIDE WITH VARIOUS SHORT-TIME PLASMA TREATMENTS. Ting-Kuo Chang, Ching-Wei Lin, Teh-Hung Teng, Huang-Chung Cheng, Institute of Electronics, National Chiao Tung University, Hsinchu, Taiwan, R.O.C.; Yih-Shing Lee, Electronics Research & Service Organization, Industrial Technology Research Institute, Hsinchu, Taiwan, R.O.C.

The plasma enhanced chemical deposited TEOS oxide has been widely used in large-area electronics applications. Among these

applications, high quality gate dielectric is one of the most important issues for fabricating high performance low-temperature polysilicon thin film transistors (TFTs). However, as-deposited TEOS oxide can hardly attain this requirement, especially for interface states and oxide electrical strength. As a result, post annealing or other post treatments are necessary to enhance the oxide quality. In this work, we investigated the effects of various short-time plasma treatments on large-area plasma enhanced chemical deposited TEOS oxide. Different plasma treatments such as N_2, O_2, N_2O, and NH_3 were applied in our experiments. Material analyses and electrical characteristics were used to examine the phonomena of plasma treatments. It was shown that the electrical strength after plasma treatments was enhanced. Besides, NH_3 plasma performed the highest passivation efficiency and the oxide with NH_3 plasma treatment has the most prominent improvements in interface states. The reliability including charge to breakdown (Q_{bd}) and bias temperature stress (BTS) was also analyzed in these samples. Although better pre-stress characteristics were observed in those samples treated by NH_3-plasma, samples with N_2O plasma treatment show superior stress endurance. Consequently, N_2O plasma treatment is the best candidate for future TFTs under long-term reliability.

D5.4
GROWTH AND CHARACTERIZATION OF Cd_2SnO_4 THIN FILMS BY METAL-ORGANIC CHEMICAL VAPOR DEPOSITION (MOCVD). Andrew W. Metz, Jason R. Babcock, Nikki L. Edleman, Tobin J. Marks, Northwestern University, Department of Chemistry, Evanston, IL; Melissa A. Lane, Carl R. Kannewurf, Northwestern University, Department of Electrical and Computer Engineering, Evanston, IL.

Cd_2SnO_4 has received a great deal of attention as a next-generation transparent conducting oxide (TCO). Its high mobility is paramount to the goal of attaining extremely high conductivities while maintaining high transparencies in these materials. Although PVD (sputtering, etc.) has been demonstrated as a viable Cd_2SnO_4 thin film preparation route, growth by MOCVD has not been previously achieved. MOCVD-derived films often have advantageous properties versus those of films prepared by other methods, and large-area depositions under higher O_2 pressures are more easily attained with MOCVD. We report here the *in situ* growth of crystalline phase-pure, highly conductive and transparent Cd_2SnO_4 films by MOCVD. Details of precursor synthesis, film growth, and film characterization will be presented in this contribution.

D5.5
ANALYSIS OF ITO FILMS DEPOSITED ON VARIOUS POLYMER SUBSTRATES FOR HIGH RESOLUTION PLASTIC FILM LCDS. Sung Kyu Park, Jeong In Han, Won Keun Kim, Chan Jae Lee and Min Gi Kwak, Korea Electronics Technology Institute, Kyunggi, KOREA.

The excellent electrical, optical and chemical properties of the indium tin oxide (ITO) thin films (1000 ± 100 Å) were obtained by depositing on polymer substrates. The materials of substrates are polyethersulfone (PES), polyethylene terephthalate (PET) and polycarbonate (PC) which have gas barrier layer and anti-glare coating for plastic film LCD. The experiments were carried out by rf-magnetron sputter using a special instrument and buffer layers. This instrument eliminated a tensile force perpendicular to the direction of the stretching force of the polymer substrate during the deposition process. In addition, buffer layers flattened the surface of substrate. Therefore, we obtained a very flat polymer substrate deposited ITO film and investigated the influences of buffer layers and the instrument. Moreover, the influences of an oxygen partial pressure a temperature of substrate and post-deposition annealing on ITO films sputtered onto polymer substrates were clarified in this presentation. Oxygen contents inside the polymer matrix structure due to the gas absorption property of the polymer substrate caused different oxygen effects from a glass substrate. The difference of the oxygen effect between glass and polymer substrates was investigated by X-ray diffractometer (XRD) and scanning electron microscope (SEM) images. From these experiments, we obtained 20-25 Ω/□ of ITO films under 0.2% oxygen contents and vacuum annealing at the temperature of 180°. Consequently, a prototype reflective color plastic film LCD (liquid crystal display) was fabricated using the PES polymer substrates to confirm whether the ITO films could be realized in accordance with our experimental results.

D5.6
AN INVESTIGATION OF NUCLEATION AND GROWTH OF ELECTROCHEMICALLY DEPOSITED $CuInSe_2$ FILMS. Lee Newsom[a], Fride Vullum[b], Ashish Marya[c], and Saibal Mitra[a]. [a]Department of Physics and Engineering Physics; [b]Department of Chemical Engineering; [c]Department of Mechanical Engineering, University of Tulsa, Tulsa, OK.

Electrochemical deposition of photovoltaic materials has attracted a lot of attention because of the ease and scalability of the process. We have investigated the nucleation and growth of electrochemically deposited $CuInSe_2$ (CIS). CIS was deposited on rotating Mo and stainless steel substrates from a solution of 1 mM $CuSO_4$, 10 mM $In_2(SO_4)_3$, 5 mM SeO_2, and sodium citrate. The deposition time was varied from 5 s to 600 s and the as-deposited films were studied using XRD, SEM and/or AFM. Our initial results indicate the presence of at least two phases. The onset of nucleation and subsequent film growth of both phases was studied. The films were then annealed at moderate temperatures (less than 250°C) and changes in grain morphology studied.

D5.7
POLYCRYSTALLINE LEAD IODIDE FILMS FOR X-RAY IMAGING: OPTICAL, ELECTRICAL AND X-RAY COUNTING CHARACTERIZATION. Laura Fornaro, Edgardo Saucedo, Luis Mussio, Alvaro Gancharov, Radiochemistry Department, Faculty of Chemistry, Montevideo, URUGUAY; Francisco E.G. Guimaraes, Antonio Carlos Hernandes, Instituto de Fisica de Sao Carlos, Universidade de Sao Paulo, Sao Carlos, SP, BRAZIL.

Lead iodide purified by zone refining and by repeated sublimation was used for growing Polycrystalline films by physical vapor deposition. Palladium film was deposited by thermal deposition as rear contact onto glass and alumina substrates up to 2x2 square inches in size. Onto it, lead iodide Polycrystalline films were grown by sublimation using a demountable chamber with vertical arrangement. Source temperatures of about 390°C under vacuum (5×10^{-5} mmHg), substrate temperatures of about 200°C, source - substrate distances of 5 cm and deposition times of 10 days were the optimum parameters for best film performance. Film thickness was measured by X-ray transmission at 59.5 keV giving values from 50 to 100 μm, with an uniformity of 10%. Optical and atomic force microscopy were performed to the films and an average grain size of 0.2 μm was measured. Low temperature photoluminescence was performed to the films and peak position and broadness confirmed starting material's high purity. Also, films were characterized by X-ray diffraction, giving a [ΣI (0 0 1)] / [ΣI (h k l)] relation of 0.8 that indicates a strong growing preferred orientation along c axis. Front palladium thermal deposition contacs and acrylic encapsulation were done onto the films and electrical properties such as apparent resistivity (8×10^{12} Ω·cm) and current density (2000 pA/cm^2 at 50 V) were obtained. X-ray film efficiency was checked by measuring integral current as response to 241-Am irradiation and to an X-ray generator, giving a relation irradiate to non-irradiate of 20. Finally, film and detector characterizations were correlate with starting material, deposition parameters and with previous results for the same and alternative materials like mercuric iodide.

D5.8
PROPERTIES OF DOPED ZnO THIN FILMS DEPOSITED BY SPRAY PYROLYSIS AND MAGNETRON SPUTTERING. P. Nunes[a], E. Fortunato[a], F. Braz Fernandes[a], P. Vilarinho R. Martins[a], [a]CENIMAT, Department of Materials Science, Faculty of Sciences and Technology, New University of Lisbon and CEMOP-UNINOVA, Monte de Caparica, PORTUGAL; Department of Ceramics and Glass Engineering/ UIMC, University of Aveiro, Aveiro, PORTUGAL.

Zinc oxide based thin films are of extreme importance in the optoelectronic field due to its excellent chemical and mechanical stability. ZnO thin films have been prepared by a variety of methods such as spray pyrolysis, evaporation, sputtering and chemical vapour deposition. The most common techniques used to produce ZnO thin films are the spray pyrolysis and the magnetron sputtering techniques, respectively a low and high cost process. The aim of this work is compare the properties of the films produced by these two techniques. The ZnO thin films deposited by r.f. magnetron sputtering, in the case of the films deposited by spray pyrolysis several dopants were used such as Aluminium, Indium and Gallium. In this paper we present a study of the electrical (Hall mobility, electrical resistivity and carrier concentration), optical (transmission and reflectance), structural and morphological (XRD and SEM) properties of zinc oxide thin films. The films deposited by sputtering and spray pyrolysis presented a resistivity on the order of 10-3Wcm and a transmitance of 85%, properties required for applications on the optolectronic field such as position sensors. The essentially different observed were on the morphological properties. The films produce by spray pyrolysis has a more roughness surface than the ones produced by sputtering.

D5.9
VARISTOR BEAHAVIOR IN LEAD BASED PEROVSKITE COMPOUNDS. Seema Sharma and R.N.P. Choudhary, Department of Physics, A.N. College, Patna, INDIA; Department of Physics, Indian Institute of Technology, Kharagpur, INDIA.

Varistor ceramics are technologically important because of their

highly non-ohmic behavior in current-voltage (I-V) characteristics, with excellent capacity of withstanding surges, enabling them to be used as transient surge suppressors against abnormal high voltage surges to protect electronic circuits, electronic power distribution ,transmission and telephone systems. Since the discovery of varistor behavior in ZnO, there has been a constant search for new varistors in a number of simple or complex oxides, carbides, ceramics, polymers and composites with higher non-linear coefficients (α) than that of ZnO varistor. Recently, it was reported that addition of smaller amount of oxides, such as V_2O_5, Mn_3O_4, BiO_3, CaO, Cr_2O_3, MnO, Sb_2O_3 and glass, to ZnO shows an enhancement in the degree of non-linearity in current-voltage (I-V) characteristics.Our preliminary studies of dc electrical conductivity of some lead-based oxide ceramics of the perovskite structural family as a function of electric field at different temperatures have attracted our attention to examine their varistor behavior because of highly non-ohmic I-V characteristics. As not much work has been reported on the use of such ceramics for varistor applications, we propose to study some lead-based perovskite materials for this purpose. In this attempt we have studied the structural, microstructural, dielectric and electrical properties of many complex perovskite compounds.As we are mainly interested to examine the existence and nature of ferroelectric phase transition and variable resistance nature in the $Pb(Cd_{1/2}X_{1/2})O_3$ compound(where X=W and Mo), we have studied its preliminary structural, microstructural, dielectric and electrical properties. Polycrystalline samples of $Pb(Cd_{1/2}X_{1/2})O_3$ (X= Mo and W) were synthesized by high-temperature solid-state reaction technique. The structural (X-ray diffraction) study of the compounds shows the formation of single-phase compound in orthorhombic crystal system. The SEM micrographs of the compounds show that some grains are well developed up to size of 2-3 μm. The cluster of grains up to the size of $\sim$10 μm are also seen at some places in the micrographs.The dielectric permittivity and loss tangent of the compound was obtained both as a function of frequency (10^3-10^4 Hz) at room temperature and temperature (30 -320°C) at 10 kHz. Both the ac and dc conductivity has been studied over a wide range of temperature and activation energy (E_a) of the compound was calculated from them. The temperature variation of resistivity shows that the compound has positive temperature coefficient of resistance (PTCR). The current-voltage (I-V) characteristics of the compound studied at different temperatures reveals that the compound has excellent varistor behavior.

D5.10

ZINC OXIDE THIN FILM DEPOSITED BY RF MAGNETRON SPUTTERING ON MYLAR SUBSTRATES AT ROOM TEMPERATURE. Elvira Fortunato, Patrícia Nunes, Daniel Costa, Donatello Brida, Andreia. Machado, Isabel Ferreira, Rodrigo Martins, FCT-UNL, Caparica, PORTUGAL.

Highly transparent and conducting Al-doped zinc oxide (ZnO:Al) thin films have been prepared by the first time on polyester (Mylar type D, 100 mm thickness) substrate at room temperature by rf magnetron sputtering. The structural, optical and electrical properties of the deposited films have been studied. The samples are polycrystalline with a hexagonal wurtzite structure and a strong crystallographic c-axis orientation (002) perpendicular to the substrate surface. The ZnO:Al thin films with a 83% transmittance in the visible region and a resistivity as low as $3.6x10^{-2}$ Wcm have been obtained, as deposited and without deterioration of the substrate. The films were grown under different rf power and were characterised by: X-ray diffraction, HRSEM; HRTEM, Hall effect and optical transmittance. The obtained results are comparable to those ones obtained in glass substrates, opening a new field of low cost, light weight, small volume, flexible and unbreakable large area optoelectronics devices.

D5.11

Abstract Withdrawn.

D5.12

CHARACTERIZATION OF THIN FILM METAL OXIDE SEMICONDUCTORS DEPOSITED ON POLYMERIC SUBSTRATES. Elvira Fortunato, Patrícia Nunes, Daniel Costa, Donatello Brida, Andreia. Machado, Isabel Ferreira, Rodrigo Martins, FCT-UNL, Caparica, PORTUGAL.

One of the main failure mechanisms of laptop computers, cellular phones, active matrix liquid crystal displays and similar portable devices is the breakage of the glass of the display. To solve this problem much research efforts is focused on the fabrication of thin film electronics on plastic substrates to replace the glass, making these devices flexible, lightweight and unbreakable. In this paper we present results on transparent conducting indium tin oxide (ITO), zinc oxide (ZnO) and tin oxide (SnO_2) deposited by spray pyrolysis and rf magnetron sputtering on polyimide substrates with different thicknesses and thermal properties. Although these oxides have been extensively studied on glass substrates, no detail work has been reported on polymeric substrates, especially the mechanical stresses developed in the deposited films. These stresses arise from the thermal expansion mismatch between the substrate and the material. One of the solutions is to re-optimise the deposition process condition of growing them at T<100°C or even at room temperature. The films grown under different substrate temperatures were characterised by: X-ray diffraction; scanning electron microscope, Hall measurements, optical transmittance and atomic force microscope. In order to compare the results, in the experiment performed the same film was also deposited on glass substrate, taken as reference.

D5.13

PERFORMANCE PRESENTED BY LARGE AREA ZnO THIN FILMS DEPOSITED BY SPRAY PYROLYSIS. P. Nunes, E. Fortunato, R. Martins, CENIMAT, Department of Materials Science, Faculty of Sciences and Technology, New University of Lisbon and CEMOP-UNINOVA, Monte de Caparica, PORTUGAL.

Zinc oxide (ZnO) is one of the most used transparent conductive oxide, especially in optoelectronic applications, due to its high optical transmittance and low electrical resistivity. ZnO thin films have been prepared by a variety of methods such as spray pyrolysis, evaporation, sputtering and chemical vapour deposition. In this work we used the spray pyrolysis technique for the deposition of ZnO thin films because this is a simple, low cost and versatile technique. In this paper we present a study on the effect of several deposition parameters (gas flow, the speed of the nozzle and distance between the nozzle and the substrate) on the electrical (Hall mobility, electrical resistivity and carrier concentration), optical (transmission and reflectance) properties of large area zinc oxide thin films and also on the films uniformity. With the aim to determine which is the are the most suitable deposition parameters to obtain transparent and conductive thin films with a high uniformity. The results show that the ZnO:In thin films presented a resistivity of $5.87x10^{-3}$Wcm, a transmitance of 85% and a uniformity of 80%.

D5.14

POLYCRYSTALLINE AND AMORPHOUS CHROMIUM OXIDE FILMS PREPARED BY MOCVD. Yuneng Chang, Shengfu Huang, Minche Huang Lunghwa Inst. of Tech., Dept of Chemical Engineering, Gueishan, Taoyuan, TAIWAN ROC.

In this paper, we will report the methodology we used to prepare polycrystalline or amorphous chromium oxide (Cr2O3) thin films. A cold wall thermal atmospheric CVD reactor was employed to accommodate decomposition of chromium acetylacetonate (Cr(acac)3, Cr(C5H7O2)3)) precursor. In oxygen containing environment, the deposited films were polycrystalline Cr2O3. In inert gas ambient. XPS, XRD, SEM, and IR were used to identify film composition, oxidation states of Cr, microstructure and surface morphology. According to depth profiling AES (DPA) results, decreasing oxygen concentration in CVD chamber, even under oxygen free environment, will cause deposited film structure transformed to amorphous state, whereas film Cr/O ratio still maintained stoichiometry(Cr:O = 2:3). SEM results show that films prepared in the process window were surface smooth and amorphous Cr2O3. Film analysis results indicated that under inert CVD environment, film oxygen atoms were provided by acetylacetonyl (acac, C5H7O2) ligands on the Cr(acac)3 precursor. During film growth, there is few reactive species to help acac form stable and desorb products. Thereby the acac ligands, released from surface adsorbed Cr(acac)3, would tend to stay a longer period, and occupy a large area on the surface. Such phenomena retarded the surface diffusion rates of individual surface adatoms like chromium and oxygen, and caused lattice fail to make regular arrangement. The fine grain structure, as revealed by SEM, is an indication of limitations on surface migration of adatoms. IR spectra and narrow scans XPS of Cr2p also show imperfect coordination, implying irregular arrangement of film atoms, a typical property of amorphous solid.

D5.15

PECVD AMORPHOUS SILICON NITRIDE AT 120°C FOR A-Si:H TFTS. D. Stryahilev, A. Sazonov, A. Nathan, Dept of Electrical and Computer Engineering, University of Waterloo, CANADA.

Low temperature amorphous silicon nitride (a-SiNx) is used as gate dielectric for TFTs fabricated on plastic substrates and as passivation layer for OLEDs and pin photodiode image arrays for retina implants. Whereas the a-SiNx technology at $\sim$300°C is well established, the reduction of deposition temperature below 150°C usually leads to porous material with high hydrogen concentration and poor dielectric performance. In this paper, we study the effect of a-SiNx films stoichiometry and their properties on the electrical integrity and masking ability. The films deposited at 120°C by PECVD from SiH_4-NH_3 gas mixture with N_2 dilution had the N/Si ratio of 1.4 to 1.7, the hydrogen concentration of 25 to 40 at.% and were fabricated with tensile or compressive stress. The electrical quality was monitored by IV measurements. The electrical resistivity of 10^{16} $\Omega\cdot$cm

and breakdown voltage of 3 MV/cm were achieved for our PECVD nitride films. The performance of a-Si:H based fully wet etched TFTs utilizing our nitride as the gate dielectric and passivation layers has also been evaluated.

D5.16
CHARGE CARRIER TRANSPORT IN a-Si:H/a-SiC:H HETERO-JUNCTION WITH BLOCKING LAYER. Yu. Vygranenko, A. Fantoni, M. Fernandes, P. Louro, A. Maçarico and M. Vieira Electronics and Communications Dept., ISEL, Lisbon, PORTUGAL.

1-D numerical simulation of the charge carrier transport and photogeneration in the TCO/ a-$Si_{1-x}C_x$:H p-i-n /metal structure was performed for the same layer composition and thickness as in the fabricated single element image transducers. Calculated dark and light I-V characteristics were in good agreement with the experimental data. The p-i-n sensing element requests a specific doping profile. Preliminary tests showed that to achieve high performance the doping level of the front p-layer must be high and, in contrary, the conductivity of the back n-layer should be lowered up to 10^{-10} - 10^{-12} $\Omega^{-1}cm^{-1}$. Such an insulator-like back layer blocks photocarrier collection in the illuminated regions and prevents excess signal charge from smearing. Numerical simulation demonstrates that it is not possible to create the effective blocking layer in an a-Si:H p-i-n homojunction and achieve the required device characteristics even at extremely low doping levels. If a wide-gap a-SiC:H alloy is used as doped layer material, the electron density in the blocking layer can be reduced down to the free carrier concentration in the a-Si:H absorber layer. Detailed simulation studies of the p-i-n heterojunction with such blocking layer have been carried out at zero volt bias and light intensity 10^{-6}-10^{-1} W/cm^2. The energy gap of 2 eV, electron density of 10^7 cm^{-3} and standard physical properties of hydrogenated amorphous silicon carbide were taken as n-layer parameters. The simulated band diagrams, electric field distribution, free carrier population, generation-recombination profiles, electron and hole current densities were analysed. Results show that under illumination the potential drop across the blocking layer is dominant for light intensity in the operating range of the image sensor. In this case, the charge carrier transport in the i-layer changes from drift to diffusion.

D5.17
IMAGE ACQUISITION USING NON-PIXELED AMORPHOUS SILICON BASED SENSORS. M. Fernandes, Yu. Vygranenko, J. Martins and M. Vieira, Electronics and Communication Dept., ISEL, Lisbon, PORTUGAL.

Large area hydrogenated amorphous silicon p-i-n structures with low conductivity doped layers were proposed as single element image sensors. The image acquisition technique consists in using a modulated light beam to scan the entire active area and recording the photoresponse in each scanning position. We suggest to enhance the system performance by optimizing the readout parameters such as the intensity cross-section and wavelength of scanner beam, acquisition time and bias conditions. The main output device characteristics as image responsivity, signal to noise ratio and spatial resolution were analyzed in open circuit, short circuit and photodiode modes. The results show that the highest signal to noise ratio can be achieved in short circuit mode. The relation between optimal scan beam intensity and photodiode parameters (current sensitivity, saturation current density, ideality factor and serial resistance) was obtained by analyzing the device electrical model and confirmed by experiment. It was shown that the sensor resolution is related to the basic device parameters and, in practice, limited by the acquisition time and scanning beam properties. The scanning beam spot size limits the resolution due to the overlapping of dark and illuminated zones leading to a blurring effect on the final image and a consequent degradation in the resolution. The measurement was carried out using as scanner a focused laser source (λ=633 nm) with a spot size smaller than 50 μm. Different scanner wavelengths were used to determine their influence on the sensor response. The dynamic behavior of the sensor was also analyzed, revealing that acquisition of moving images is possible. As conclusion we show that the performance of this type of sensor is enhanced by a tight control of the signal acquisition technique and parameters as scanner light source, mechanical system and bias conditions.

D5.18
EFFECT OF TEMPERATURE AND ILLUMINATION ON THE INSTABILITY OF A-Si:H TFTS UNDER AC GATE BIAS STRESS. Teh-Hung Teng, Chun-Yao Huang, Ching-Wei Lin, Ting-Kuo Chang, Cheng-Jer Yang, Huang-Chung Cheng, National Chiao-Tung Univ, Dept of Electronics Engineering and Inst of Electronics, HsinChu, TAIWAN.

Hydrogenated amorphous silicon thin film transistors (a-Si:H TFTs) are now widely used as switch devices in large-area electronic devices such as active matrix liquid crystal displays (AMLCDs). For a-Si:H TFTs, the instability can degrade their electrical characteristics and affect the lifetime. Hence, improving reliability has become an important issue. The instability causing variation of electrical characteristics of the a-Si:H TFTs is attributed to two mechanisms: the charge trapping in a gate insulator of SiNx and the state creation in an a-Si:H film. Generally, the instability of a-Si:H TFTs is discussed under DC bias stress. However, the TFTs used in LCDs are operated under the AC mode. This work systematically focuses on the behavior of a-Si:H TFTs under various signal frequencies of bias stress with temperature or illumination to determine the relationship between TFTs instability and signal frequency. For the instability analysis of a-Si:H TFTs, the threshold voltage shift and the subthreshold swing change are two important electrical characteristics in interest. In order to find the threshold voltage shift and the subthreshold swing change for Bias-Temperature-Stress (BTS) and Bias-Illumination-Stress (BIS), either the substrate heating (50°C) or the illumination was applied on the a-Si:H TFTs under AC gate bias stress. Excess carriers from thermal-generation electron-hole pairs or photo-excited electron-hole pairs may significantly influence the instability of a-Si:H TFTs during bias stress. The instability mechanisms originated from the carrier-induced defect creation were enhanced by thermal generation in the BTS case and emphasized by photo-excitation in the BIS one as well. Both stress conditions will induce larger threshold voltage shifts and higher cut-off frequencies than those for normal bias stresses.

D5.19
LOW-TEMPERATURE CRYSTALLIZATION OF AMORPHOUS Si FILMS USING $AlCl_3$. Jin Hyung Ahn, Ji Hye Eom, and Byung Tae Ahn, Korea Advanced Institute of Science and Technology, Dept of Materials Science and Engineering, Taejon, KOREA.

It is known that the direct contact between Al and a-Si enhances the crystallization of a-Si film. But the poly-Si films by Al induced crystallization suffer the problems of rough surface and pores. In our study, we utilized $AlCl_3$ vapor instead of Al metal film. The crystallization was enhanced in $AlCl_3$ atmosphere. The Al content in the poly-Si film was below the detection limit of AES. And the surface of the poly-Si film was as smooth as that of the a-Si film. The enhancement of grain size by combining the first stage nucleation by $AlCl_3$ and the second stage growth by microwave annealing is under study and will be presented.

D5.20
STUDY OF CRYSTAL GROWTH IN GRAIN-FILTERS FOR LOCATION-CONTROLLED EXCIMER LASER CRYSTAL-LIZATION. Paul Ch. van der Wilt, Barry D. van Dijk, Jurgen Bertens, and Ryoichi Ishihara, DIMES, Delft University of Technology, Delft, THE NETHERLANDS.

Excimer-laser crystallization of amorphous silicon films is a well-established method to fabricate large-grain polycrystalline silicon films on glass substrates. However, thin-film transistors made in these films have poor device-to-device uniformity due to the random location of the grain boundaries. Single-crystal TFTs would have better uniformity and also better device characteristics. We have developed a method to control the location of grains each large enough to contain the channel area of one TFT. Growth of these grains is preceded by a vertical growth phase through a narrow hole (<100 nm). As normally during regrowth of a partially melted film, occlusion of grains will occur. When the melt-depth to hole-diameter ratio is sufficiently large, all but one grain will be occluded, hence the term grain-filter. This grain will then seed the lateral grain growth [Spring MRS 2000, Q7.4]. Narrow holes were made by decreasing diameter of 1 μm holes in silicondioxide with a second conformal oxide deposition. The effective melt-depth to hole-diameter ratio was increased by methods such as substrate heating and sharpening of the edges of the hole. Latter was achieved either with chemical-mechanical planarization or plasma planarization processes. From these experiments it was found that a high yield of low defect-density silicon islands could be obtained. Preliminary analysis with electron back scattering patterns (EBSP) confirmed that random high-angle grain-boundaries were suppressed. Twin boundaries and low-angle grain-boundaries, however, were still present in most cases. These defects, which are considerably less detrimental to electrical properties, might be originating from (the onset of) the lateral growth. To study this, an experiment was performed in which grain growth was seeded by monocrystalline silicon wafers rather than explosively crystallized silicon. For this experiment, narrow holes were etched directly in the silicondioxide after controlled reflow and shrinkage of the photoresist pattern.

D5.21
NUMERICAL SIMULATION AND ANALYSIS OF EXCIMER-LASER-INDUCED LATERAL SOLIDIFICATION OF THIN Si FILMS. Dongbyum Kim, Hans S. Cho, Alexander B. Limanov, and James S. Im, Columbia University, Program in Materials Science, New

York, NY; John P. Leonard, Harvard University, Division of Engineering and Applied Sciences.

In the controlled superlateral growth (C-SLG) method, an excimer laser beam is used to induce and manipulate rapid lateral solidification of thin Si films. The C-SLG process can be used to realize localized regions consisting of large grains, and furthermore constitutes the basis of the sequential lateral solidification (SLS) method. A number of important details such as the maximum extent to which the lateral solidification proceeds depend on the complex interplay of various external and internal parameters. Previously, the capability to accurately simulate and quantitatively analyze such a process was lacking due primarily to the difficulties of properly incorporating the stochastic nature of nucleation into a numerical model, particularly under highly transient and deeply supercooled conditions under which multiple nucleation events can take place. Using a recently developed three-dimensional numerical model that successfully simulates the nucleation of solids in a manner that is consistent with the aforementioned stochastic nature, as well as kinetic considerations, we have analyzed the details of the melting and solidification of Si films during the C-SLG process. We will start by presenting results obtained from sets of simulations in which the incident energy density, film thickness, and the pulse duration are varied. A remarkable correlation is found between the results of simulations and experiments that verifies the validity of the model. We will then present results from a set of simulations that quantitatively reveal the negative effects on the optimization of lateral growth that arise when a beamlet used to induce controlled melting has a gradual (e.g., Gaussian-like, as opposed to rectangular) spatial intensity profile. Finally, we will propose – and provide simulation results that support – a novel multi-layer substrate modification scheme that permits thermal engineering of the lateral solidification for enhancing the extent to which lateral growth can proceed. This work was supported by DARPA under project N66001-98-1-8913.

D5.22
SILICIDE FORMATION BY PULSED EXCIMER LASER ANNEALING. Connie Lew, Michael O. Thompson, Cornell University, Dept of MS&E, Ithaca, NY.

Silicide formation can occur at the interface of metal and a-Si films upon annealing with a pulsed excimer laser (XeCl-308 nm). During laser-induced melting, the melt front reaches the Si/metal interface, where liquid phase kinetics allow reaction to take place to form silicide, despite the $<$100 ns time-scale. Formation of silicides by this process is potentially advantageous in the processing of Schottky junctions for vertical diodes and stacked diodes in memory applications. Several Si/metal film stacks have been investigated, including Si/Ni/Cr, Si/Ti, Si/Mo/Cr, and Si/Ta/Cr by e-gun evaporation. All film stacks were deposited on thermally oxidized Si substrates. The films were each laser-annealed at various energy densities in order to determine the onset of melt, the minimum fluence required for reaction to take place at the Si/metal interface, and the minimum fluence at which film ablation occurs. Surface reflectance measurements were used to monitor the melt duration at varying energy densities. Rutherford Backscattering (RBS) and transmission electron microscopy (TEM) were used to analyze films and identify both the onset of silicide formation, phase formation, and the crystal structure. Electrical characteristics of Schottky junctions were also measured. Si melt threshold is typically $\sim$100 mJ/cm^2. Reaction occurs at fluences of the full melt of Si. At $\sim$240 mJ/cm^2, RBS shows that both Ti and Ni react with Si to form TiSi and NiSi, respectively. Silicide formation occurs because the melting temperature of the metals (Ti = 1935K; Ni = 1726K) is comparable to that of Si (1683K). At higher fluences $>$300 mJ/cm^2, the process is limited by increasing thermal stress in the metal/Si films, which leads to ablation. With the higher melting temperature metals, no reaction is observed.

D5.23
A NOVEL POLY-Si TFT IN LINE-CROSSOVER WITH HIGH APERTURE RATIO AND SMALL SIGNAL DELAY OF AMLCD PANEL. Jin-Woo Park, In-Hyuk Song, Kee-Chan Park, Sang-Hoon Jung and Min-Koo Han, Seoul National University, School of Electrical Engineering, Seoul, KOREA.

Poly-Si TFTs (Polycrystalline Silicon Thin Film Transistor) have attracted a considerable interest in possible application for AMLCD due to high mobility and current driving capacity. The high resolution TFT-LCD panel requires small pixel size. However, the pixel size becomes small, an aperture ratio is decreased because TFT size and line width are not decreased. It is desirable design a small size pixel for poly-Si TFT-LCD with high aperture ratio. The purpose of our work is to propose a new TFT which integrates a TFT at a gate-data line crossover in order to improve the aperture ratio of the panel. We employ a low dielectric air-gap between gate-data line crossover, which reduces the capacitance between gate and data lines, so that the signal delay of the data line is decreased significantly. The new panel is successfully fabricated by locating the TFT under the data line. An air-gap between a data line bridge and a TFT without any contact to a data line was successfully formed by a sacrificial photoresist layer. The sacrificial layer photoresist was treated by thermal curing which is immune to a high temperature plasma process such as an oxide deposition or a metal sputtering on the organic photoresist. Our experimental results show that TFT was successfully formed in the line-crossover. The TFT was covered by a data-line-bridge completely so that the aperture ratio of the panel was improved. The pixel size is about 150μm*50μm and the TFT area cover by data line is about 20μm*30μm, so the aperture ratio of the AMLCD panel was improved by about 4%. Our experimental electrical data shows that the TFT in line-crossover was operated successfully, and the air-gap between a data-line-bridge and a TFT with a gate-line reduces the delay time by about 9 times compared with the conventional structured panel. The proposed TFT in line-crossover structure was successfully integrating the TFT into a gate-data line-crossover. The aperture ratio of an AMLCD panel was improved by about 4% because of covering the TFT by a metal line, and the signal delay of data line was decreased significantly by a low-dielectric air-gap between data-line-bridge and the TFT with a gate-line.

D5.24
EFFECT OF a-SiC:H FILM COMPOSITION ON THE PERFORMANCE OF LARGE AREA OPTICAL SENSORS. P. Louro, Yu. Vygranenko, M. Fernandes and M. Vieira, Electronic and Communications Dept., ISEL, Lisbon, PORTUGAL; M. Shubert, Institut fur Physikalische Electronik, Pfaffenwaldring, GERMANY.

Preliminary studies on the use of glass/ZnO:Al/pin a-Si:H/Al structures as image sensors have recently shown its potential capability. The improvement of the device characteristics can be achieved by applying a wide band gap a- $Si_{1-x}C_x$:H as interface material. This optimisation demands a full understanding of the transport mechanism in p-i-n a-Si:H/a-SiC:H heterojunctions on the grounds of the physical properties of each layer. The work presented concerns the electrical, optical characterisation of the a- $Si_{1-x}C_x$:H films deposited by Plasma Enhanced Chemical Vapor Deposition in order to contribute to this knowledge. The efforts were focused mainly on doped n- and p-type layer at high and low doping levels with and without carbon, as well as intrinsic layers. Optical characterisation of the single layers was performed with UV/VIS/NIR spectrophotometry to measure the thickness of the films, the optical gap and the refractive index of the material; as well as to estimate the absorption coefficient. These results were also complemented with CPM measurements. Electrical characterisation consisted mainly on the measurement of the conductivity versus temperature and activation energy determination. The photoconductivity of each layer was also evaluated as well as the I(V) dependence. Structural characterisation was performed with IR spectrophotometry in order to evaluate the amount of hydrogen and estimate the quality of the material. These experimental results were used as a basis for the numerical simulation of the energy band diagram, the electrical field and the carrier concentration distribution of the whole structures in thermodynamic equilibrium and under illumination. Further comparison with the sensor performance gave satisfactory agreement. Results show that the conduction band offset is the most limiting parameter for the optimal collection of the photogenerated carriers. As the optical gap increases and the conductivity of the doped layers decreases, the transport mechanism changes from a drift to a diffusion limited process.

D5.25
PLASMA PRETREATMENT OF THE SILICON SUBSTRATE FOR AN OPTIMIZED FIELD EMISSION MPCVD DIAMOND VACUUM DEVICE. Reinhart Job, Vadim Raiko, Alexander G. Ulyashin, Juergen Engemann, Wolfgang R. Fahrner.

The influence of hydrogen plasma pretreatments of the p-type monocrystalline silicon substrate on the field emission properties of deposited diamond on silicon is discussed. Diamond films are deposited on p-type Czochralski (Cz) silicon by microwave plasma assisted CVD (MPCVD). The pretreatment as well as the subsequent diamond deposition were performed in various methane/hydrogen gas mixtures in the range of 450 - 650°C. Field emission (FE) characteristics of as grown and thermally treated diamond on silicon structures were investigated. It was found that a pretreatment of the Cz-Si substrate in a hydrogen plasma at 450°C and 650°C can substantially improve the field emission properties of diamond on silicon. The threshold field strength decreased from 12-16 V/mm to 5-10 V/mm due to such hydrogen plasma pretreatments at 450°C and 650°C. A possible mechanism for the improved emission of electrons from diamond on Cz silicon is discussed. Especially the formation of thermal donors (TD) in the substrate and their influence on the field emission efficiency are discussed. The TDs are generated during the pretreatments by the hydrogen plasma or even during the deposition of the MPCVD diamond layers on the Si substrate. It can be concluded that the formation of local levels in the band gap of the Si

substrate originating from a hydrogen plasma pretreatment can significantly improve the FE properties of the diamond on Si structure. The physical model for the explanation of the results and the consequences for an advanced development of FE vacuum devices with enhanced properties are discussed.

D5.26
EMISSION PROPERTIES OF NANOSTRUCTURED CARBON FIELD-EMISSION CATHODES. N.N. Chubun, A.G. Chakhovskoi, C.E. Hunt, Department of Electrical and Computer Engineering, University of California at Davis, Davis, CA; A.N. Obraztsov, A.P. Volkov, Department of Physics, Moscow State University, Moscow, RUSSIA.

Large area planar field-emission cathode structures consisting of multi-wall carbon nanotubes (CNT) and nanosized graphite flakes with sharp edges have been investigated as an electron source for flat panel display and vacuum cathodoluminescent light source application. Layers of nanotubes were grown on silicon and molybdenum substrates up to 3" in diameter using a high-temperature (1050° C) pyrolitic plasma-assisted CVD method and alternatively, using a low-temperature catalytic method. The result is a vertically-oriented nanotube 'grass' of 1-2 micrometer height which is chemically bonded with the substrates. Additional orientation of the nanotubes, occurring in the electrostatic field during the first activation of the cathodes, was observed. Field emission properties of diode and triode structures were studied in a vacuum chamber and in sealed light-source prototype devices. CNT cathodes with an area up to 1 square inch were tested under DC currents up to 1 milliamps in triode mode. Grid voltages up to 1000 V and anode bias up to 5 kV were applied. Flat-panel display prototype packages were used for testing of the CNT cathodes in diode configuration. For samples measured in a UHV chamber, the distance between the cathode assembly and the phosphor anode was optimized using a linear translation manipulator. Low-voltage phosphors were used for monitoring of the distribution of the emission sites of the large area cathodes. Turn-on fields varied from 0.8 to 2 V per micron depending on the extraction electrode configuration. No significant dependence of emission characteristics and current stability from residual gases pressure was observed in the range from 10^{-5} to 10^{-8} Torr. Current fluctuations of 1-2% were achieved using loading resistor. Emission properties of the carbon nanostructured cathodes were directly compared to carbon fiber and carbon foam emitters showing potentially greater reproducibility and uniformity of field emission of the oriented nanostructures.

D5.27
SILICON FIELD EMITTER ARRAYS INTEGRATED WITH MOSFET DEVICES. Ching-yin Hong and Akintunde I. Akinwande, Massachusetts Institute of Technology, Microsystems Technology Laboratories, Cambridge, MA.

While the performance of silicon field emission arrays (FEAs) is adequate for a number of applications, Si FEAs are plagued with two major problems – (1) high addressing voltages and (2) non-uniformity and instability of emission current. Both problems are linked to the fact that electrons tunnel through a barrier. The emission current depends exponentially on the height (work function) and width (tip radius & field factor) of the barrier. The emission current is sensitive to small changes in the barrier height or width. In contrast to the current approach of using a "ballast" feedback resistor to improve emission current uniformity, we used a lateral diffused (LD-) MOSFET as a voltage controlled current source in series with the FEAs. Our preliminary device used identical oxide thickness for both the FEA and the MOSFET regions. We report a turn-on voltage of 24V for the FEAs and a threshold voltage of 2.5 V for the LD-MOSFET (L=100 μm, W=10 μm and Ld=10 μm). Analysis of the FEAs using FN formulation showed that a silicon tip radius of 8.17 nm would fit our I-V data. This extracted tip radius is very close to the tip radius (10 nm) measured by SEM. We demonstrated control of electron emission from a MOSFET/FEA structure by the MOSFET gate voltage: the MOSFET/FEA is off when the transistor gate voltage is below threshold voltage of the MOSFET irrespective of the FEA gate voltage. When the MOSFET gate voltage is above the threshold voltage, an inversion layer in the MOSFET channel supplies electrons to the FEA. At low FEA gate voltages, the MOSFET/FEA IV characteristics follow FN behavior; however at high FEA gate voltages, the device displays saturation characteristics because of the limited electron supply to the field emitter. In this region, current is controlled by MOSFET. We shall report on temporal and spatial uniformity of MOSFET FEAs when operated in this regime.

D5.28
INVESTIGATION OF MgO AND Mg_2TiO_4 THIN FILMS BY ELECTROSTAIC SPRAY DEPOSITION METHOD FOR A PROTECTIVE LAYER OF AC-PLASMA DISPLAY PANEL. Soo Gil Kim, Hyeong Joon Kim, School of Material Sci. & Eng., Seoul Nat'l Univ., Seoul, KOREA; Young-Kee Kim, and Chung-Hoo Park, Dept. of Electrical Eng., Pusan Nat'l Univ., Pusan, KOREA.

It has been reported that MgO as a protective layer of the dielectrics in AC-plasma display panel improves the discharge characteristics and the panel's life time. However, MgO is able to absord species from the ambient air either dissociatively or reactively. H_2O and CO_2 are chemisorbed to form hydroxide and carbonate, respectively. Minute amounts of any contamination of the MgO may affect the panel's performance by changing the gas pressure of the panel and the electric state of MgO surface. The surfaces of the Mg_2TiO_4 spinel layers exhibit a considerably higher degradation stability than those of MgO when stored in ambient air. We had focused our efforts on developing a new protective layer of AC-PDP using electrostatic spray deposition method. MgO and Mg_2TiO_4 thin films were deposited on Si (100) and corning 7059 glass substrates and AC-PDP test panels by using $Mg(tmhd)_2$ and $Ti(O^iPr)_2(tmhd)_2$ as the precursor dissolved in a liquid solution of tetra hydro furan and 1-octyl alcohol. X-ray diffraction analysis exhibited well aligned growth of MgO and Mg_2TiO_4 deposited at 350 $\sim$ 400°C of substrate temperature in (200) and (400), respectively. Comparing the dielectric constant and the resistivity appeared to be quite similar. And the oxides showed optical transmittances of 90% in the visible range. Mg_2TiO_4 films exhibited a significant panel performance such as stable firing and sustain voltages with duration time in the ambient.

SESSION D6: HIGH PERFORMANCE LARGE AREA ELECTRONICS: INDUSTRIAL ACTIVITIES
Chairs: Hyun Jae Kim and Shuichi Uchikoga
Wednesday Morning, April 18, 2001
Franciscan I (Argent)

8:30 AM *D6.1
LOW-TEMPERATURE POLY-Si TFT BY EXCIMER LASER ANNEALING. Tohru Nishibe, Toshiba Corporation, LCD R&D Center, Fukaya, JAPAN.

Poly-Si TFT-LCD has begun its way to an advanced display by integrating the driver circuits onto the glass substrate. Improvement of poly-Si TFT is essential in order to achieve value-added display where circuits for various functions are integrated on one substrate. Value-added displays include such displays as system-on-glass, paper-like displays. Furthermore, high-resolution, brightness and good color reproducibility are the important items which add values to the future display. This report will focus on technologies such as crystallization, gate insulator formation and low temperature process. Near-crystalline silicon is required to obtain high carrier mobility. High quality oxide is necessary for controlling TFT stability. Development of low temprature process is essential to achieve display with new concept, such as flexible displays. Future display be also presented in this report.

9:00 AM *D6.2
UV-OPTICS FOR EXCIMER LASER BASED CRYSTALLIZATION PROCESSES. Hans-Jürgen Kahlert, MicroLas Lasersystem GmbH, Göttingen, GERMANY.

Laser based crystallization of thin amorphous films on glass substrates have entered into industrial applications since several years. The excimer laser based process provides a low temperature procedure to obtain polycrystalline silicon films on flat panel display substrates to fabricate thin film transistors (TFTs). The keys to this application are a uniform illumination of the substrate and a corresponding scanning procedure. Line Beam systems provide up to 365mm long homogeneous exposure fields operated with up to 300 W average power 308nm excimer lasers. The paper covers a technical overview of Line Beam Optics layout, recent developments and results. Further high resolution optics are described and discussed for sequential lateral solidification (1,2,3) (SLS) processes. The SLS application has demonstrated to efficiently produce directionally solidified microstructures or even grain-boundary free regions on Si-films. Diffraction limited resolution in the range of several micrometers and high optical throughput are important parameters to this application. General considerations are presented to describe technical limits which compromise laser beam related coherence effects, optimum uniform illumination, adequate resolution and depth of focus and reasonable optical efficiency for the practical application. References: (1) J.S. Im and H.J. Kim, "On the super lateral growth phenomenon observed in excimer laser-induced crystallization oh thin Si films", Appl. Phys. Lett., Vol. 64, No 18, 2303-2305, 1994 (2) M.A. Crowder, P.G. Carey, P.M. Smith, R.S. Sposili, H.S. Cho and J.S. Im, "Low-temperature single-crystal Si TFTs fabricated on Si films processes via sequential lateral solidification", IEEE Electron Devices Letters, Vol. 19, No.8, 306-308, 1998 (3) R.S. Sposili, J.S. Im, "Line-scan sequential lateral solidification of Si thin films", Applied Physics A 67, 273-276, 1998

9:30 AM *D6.3

LPS TFT-LCD FOR NEW MOBILE MARKET. Aki Imaya, Sharp Corporation, Camas, WA.

The display market has been changing with the emergence of the new Mobile Multimedia applications. As a result, new capabilities are demanded of the displays, such as high resolution, small size, proper weight etc.
Simultaneously, the display is trying to be more compact and more versatile by integrating several new and novel functions. Low Temperature Poly Silicon TFT is one of the most expected devices to realize the integrated circuits on the display panels.
In this presentation, the requirements for the new mobile market will be presented and discussed.

SESSION D7: EXCIMER LASERS ANNEALING OF Si
Chairs: Hyun Jae Kim and Shuichi Uchikoga
Wednesday Morning, April 18, 2001
Franciscan I (Argent)

10:30 AM *D7.1

LONG-PULSE DURATION EXCIMER LASER PROCESSING IN THE FABRICATION OF HIGH PERFORMANCE POLYSILICON TFTS FOR LARGE AREA ELECTRONICS. Eric Fogarassy, Laboratoire CNRS-PHASE, Strasbourg, FRANCE.

Excimer laser crystallization of amorphous silicon on cheap glass appears to be very promising to prepare high quality poly-Si TFTs for large area display applications. The rapid deposition of laser energy on a nanosecond time scale into the near surface region of the a-Si layer leads to its melting and regrowth into polysilicon, while keeping the substrate at low ($< 600°C$) temperature. In order to optimize the final quality of the poly-Si film and the formation of a large-grained material through the so-called Super Lateral Growth (SLG) regime, it is necessary to control extremely carefully the surface melt dynamics of the process, which strongly depends on the temporal characteristics of the laser pulse. Industrial excimer sources with pulse durations ranging from 10 to 200 ns are now available and offer new possibilities to optimize the laser crystallization process and device performance. In this work, was investigated the excimer laser crystallization of thin (< 100 nm) a-Si films deposited onto SiO_2-coated glass substrates, using a novel 200 ns-pulse duration XeCl excimer source. X-ray pre-ionization enables this laser to reach a pulse-to-pulse stability close to 2.5% and a beam homogenizer delivers a very uniform (better than 2.5%) energy distribution over a large area (~ 25 cm^2) and an energy density up to 1 J/cm^2 per pulse. Experiments were carried out in air both in the single and multi-shot mode. The melting threshold, melt duration, depth of fusion and critical fluence corresponding to the SLG regime were characterized by time-resolved reflectivity measurements, Raman spectroscopy, scanning electron and atomic force microscopy. The numerical analysis, based on the one-dimensional heat flow equation, was also performed and compared to the experimental results. Finally, the n-type poly-Si TFTs prepared in the optimized conditions of irradiation exhibited field effect mobilities in excess of 200 cm^2/Vs.

11:00 AM *D7.2

RESENT PROGRESS IN HIGH POWER, HIGH REPETITION RATE EXCIMER LASERS DEVELOPMENT FOR PRODUCING NEXT GENERATION LARGE-AREA ELECTRONIC DEVICE. V. Borisov, A. Demin, A. Eltzov, O. Kristoforov, Yu. Kirykhin, A. Vinokhodov, V. Vodchits, State Research Centre of Russian Federation Troitsk Institute for Innovation and Fusion Research (TRINITI), RUSSIA; D. Basting, M. Rahe, U. Stamm, R. Osmanov, Lambda Physik AG, Göttingen, GERMANY.

Today highest level of a stabilized average power for commercial available excimer lasers, new Lambda STEEL, is 300W (1J x 300Hz). TRINITI with support of Lambda Physik is developing next generation of excimer lasers for high-performance large area electronic devices and product. The key of these excimer lasers is conjunction of simple, reliable UV preionizer based on creeping discharge and highly efficient gas flow system. These features allow developing compact, high power excimer lasers with wide possibilities to change combination of output energy (E), repetition rate (f), pulse duration (t) and wavelength (λ). For example, new prototype of XeCl laser with stabilized average power 400W (E = 2J, f = 200Hz, t = 70ns, λ = 308nm, gas-life time more than 15 million pulses, and pulse-to-pulse energy stability(s) in range 1 - 2%) was developed. This prototype can be used for conventional Excimer-Laser Crystallization (ELC) technique to increase of panels size. Other prototype of XeCl laser allows achieving average power about 600W. This prototype has optimal combination of parameters (E = 4J, f = 150Hz, t = 120ns, λ = 308nm) for new ELC technique - Sequential Lateral Solidification (SLS) proposed by Columbia University research group. Also detail characteristics of 600W KrF lasers (E = 1J, f = 600Hz, t = 30ns, λ = 248nm, or E = 0,15J, f = 4000Hz, t = 28ns, λ = 248nm) as well as 250W ArF laser (E = 0,063J, f = 4000Hz, t = 24ns, λ = 193nm) will be presented.

11:30 AM D7.3

THE EFFECT OF SPUTTERING GAS ON THE MATERIALS AND ELECTRICAL CHARACTERISTICS OF p-Si FILMS FORMED BY DC MAGNETRON SPUTTERING. Tolis Voutsas, Sharp Labs. of America Inc., LCD Process Technology Group, Camas, WA.

In this work we will discuss the feasibility of sputtered-Si as a precursor for low-temperature p-Si films. We used DC sputtering to deposit thin Si films (30-100nm) that were subsequently crystallized by excimer-laser annealing using XeCl (308nm) irradiation. The as-deposited films were sputtered with different gases including Ar, He and Ar-He mixtures. As-sputtered films were characterized by spectroscopic ellipsometry to determine their optical properties, including optical bandgap, index of refraction and absorption coefficient. As expected, He sputtering led to less dense films that Ar. However, the plasma voltage (during deposition) was also lower in these cases. It was found that mixing of Ar and He gases within an appropriate ratio range produced sputtered films with good optical properties, at much lower plasma voltages that Ar alone. The lower voltage application should be beneficial from the point of view of reducing microarcing and for allowing higher DC power levels (to improve deposition rate). Polysilicon TFTs fabricated at the optimum Ar-He ratios (1-3% He in Ar) indicate identical performance between pure-Ar and Ar-He sputtered TFTs.

11:45 AM D7.4

ORIGIN OF INHOMOGENEITY IN PULSED EXCIMER-LASER CRYSTALLIZED SILICON FILMS STUDIED BY COMPUTER SIMULATION. Toshio Kudo, Daiji Ichishima, Sumitomo Heavy Industries Ltd, Research & Development Center, Hiratsuka, JAPAN; Cheng-Guo Jin, TIC Corporation, ACT Center, Yokohama, JAPAN.

An excimer laser annealing process is still a bottleneck in low-temperature poly-SiTFT production technology, because energy fluctuation during pulsed laser irradiation induces inhomogeneity in poly-Si films. It is a key to the issue that is to understand mechanism to induce the size fluctuation of Si grains under overlapped line-bean irradiation. Due to the short irradiation of pulse laser, however, it is not so easy to observe the time dependence of poly-Si texture in the crystallization process of a-Si films. So the visualized poly-Si simulation we developed should be used to study the size fluctuation of Si grains in the polycrystallization process. The simulation model is characterized by the homogeneous nucleation and the growing & shrinking of Si grains. The 2D numerical calculation was carried out under the following conditions: an a-Si layer 1um wide and 500A thick / a SiO_2 underlayer 1000A thick / a glass substrate / room temperature / vacuum / a pulsed XeCl excimer laser (308nm) / a Gaussian profile / the pulse duration (14ns) / the full width at half maximum (FWHM: 0.6mm) / an overlap ratio of 98% (a step of scanning: 0.06mm). Introducing the real energy fluctuation (a peak-to-peak value: 5.3%), we obtained the following knowledge about the origin of inhomogeneity in the poly-Si films: 1) Energy fluctuation around the top of the Gaussian beam (FWHM: 0.6mm) is essential to the inhomogeneity. 2) Such energy fluctuation being over a threshold value, micro-crystals generate over all and prove fatal to the homogeneity. 3) The inhomogeneity from one fatal fluctuation is not recovered even under overlapping irradiation. We'll also discuss about the origin of inhomogeneity from the fluctuation of optical axis and the dependence of laser beam shape, and from the interference effect for each other.

SESSION D8/I8: JOINT SESSION
COMMERCIALIZATION OF BONDED SILICON-ON INSULATOR (SOI)
Chair: Marin Alexe
Wednesday Afternoon, April 18, 2001
Golden Gate C1 (Marriott)

1:30 PM *D8.1/I8.1

COMMERCIALIZATION OF THICK AND THIN SOI BY THE SMART CUT^{TM} PROCESS. A.J. Auberton-Hervé, SOITEC, Bernin, FRANCE.

The semiconductor industry growth and success in following the Moore law has been supported by some key strategic materials and key technology enabling the introduction of these new materials. In the new material hardly demanded by the semiconductor industry, three receive today most of the attention: Copper, low k dielectrics and SOI. Among these materials, two are in the interconnection

domain and only SOI concerns the improvement of the silicon itself. As interconnections are no more the IC's performance limitation, silicon is again at the center of the speed enhancement. The key drivers for SOI are today speed and low power consumption. Due to the increasing demand for portable systems with higher autonomy and better performance, SOI is today considered as the necessary change in the silicon material evolution. In the "bag of tricks" available for the engineers, the Smart Cut^{TM} technology offers a major breakthrough by providing the solution to the following issue: how to get a deposition technique which bring a pure monocrystalline film on top of any kind of substrate (amorphous, crystalline, plastic...)? Smart Cut^{TM} process is already in use for large volume SOI wafer production. Availability of high quality SOI wafers achieved using Smart Cut^{TM} process has already been demonstrated as SOI Unibond roadmap meets the most advanced requirements for 0.13 μm technology. This paper shows that such wafer quality can be adapted to customer demand with flexibility concerning the layer thickness specifications from a few 10nm for both the silicon and the buried oxide layers to micrometer range. Volume production data are shown for 2 typical 8" products (one thin and the other thick), enhancing control of silicon and buried oxide thickness uniformities, particles control over 0.16μm and HF defect monitoring. Production capacity including 300mm projection is also discussed with the necessary volume required by 0.18μm and below technologies.

2:00 PM *D8.2/I8.2

BONDING, SPLITTING AND THINNING BY POROUS Si IN ELTRAN^{TM}; SOI-Epi Wafers^{TM}. Kenji Yamagata and Takao Yonehara, ELTRAN Business Center, Canon Inc., Kanagawa, JAPAN.

ELTRAN is a unique technology categorized in Bonding and Etch-back SOI and has been originated, developed and produced by Canon. In this process, there are several novel technologies using porous silicon material, that is, silicon epitaxial growth on its surface, water jet splitting at the interface of double stacked porous layers after bonding, and selective etching of porous silicon with very high selectivity of 1E5. Accordingly the porous silicon material plays an important role in ELTRAN process. Especially the SOI layer quality is decided by silicon epitaxial growth onto porous silicon surface, therefore porous fabrication step is very important. We have developed the fully automatic anodization machine for the mass production. In this machine, it is possible to anodize allover the surface of multiple silicon wafers in a batch with a good uniformity and to control the porous thickness and porosity by a computer system. In order to design the machine to achieve such features, we carried out the computer simulation on porous silicon formation with the three dimensional current field analysis by a finite element method. It was found out that the porous silicon thickness uniformity depended on the cathode size and distance between a cathode and a silicon wafer in the anodization system. Generally in bonding SOI wafer manufacturing, cost issue is very crucial so that we have also developed the fully automatic water jet splitting system for mass production. As a result the fabrication cost could be reduced by splitting and recycling technology of the bonded wafers. Furthermore we are developing another type of an anodization machine and improving the water jet machine in order to extend this technology to 300mm wafer. It has succeeded to produce the uniform porous silicon layer, and split over the entire 300mm wafers, which enables us to produce 300mm SOI wafers.

2:30 PM *D8.3/I8.3

ATOMIC-LAYER CLEAVING AND NON-CONTACT THINNING FOR FABRICATION LAMINATED ELECTRONIC AND PHOTONIC STRUCTURES. M.I. Current, M. Fuerfanger, S. Kang, M. Korolik, I. Malik, S. Farrens, L. Feng, F. Henley, Silicon Genesis, Campbell, CA.

Use of new approaches to film deposition and ion beam modification techniques provide avenues for enhanced bond strengths and engineered cleave plane structures which result in layer transfer of electronic and photonic materials for efficient fabrication of laminated electronic and photonic structures. These structures include Silicon-on-Insulator wafers and a variety of optical signal couplers, routers and sensors. The ability to form cleaved layers containing Si, SiGe alloys and SiO_2 with Angstrom-level surface finish after room-temperature separation provides an opportunity to bond a new crystalline structure directly onto the transferred layer without the need for contract polishes and etching of damaged layers. A suite of innovative layer transfer techniques, which includes plasma-activated bonding, CVD film deposition, light-ion implantation and non-contact, post-cleaving thinning and smoothing processes, will be described. Applications for multi-level structures such as integral fabrication of SOI wafers with multi-layer high-mobility channel structures, multi-level SOI wafers for fabrication of self-aligned dual-gate CMOS and a variety of optical structures will be discussed.

SESSION D9/I9: JOINT SESSION
SILICON-ON-INSULATOR
Chair: Bernard Aspar
Wednesday Afternoon, April 18, 2001
Golden Gate C1 (Marriott)

3:30 PM D9.1/I9.1

ORIENTATION AND BORON CONCENTRATION DEPENDENCE OF Si LAYER TRANSFER BY MECHANICAL EXFOLIATION. K. Henttinen, T. Suni and I. Suni, VTT Electronics, Microelectronics Center, Espoo, FINLAND; S.S. Lau, University of California-San Diego, Department of Electrical & Computer Engr., La Jolla, CA.

It has been shown that H-implanted silicon can be exfoliated by mechanical means without thermal annealing at moderately high temperatures, i.e. 400-500°C. The key to this splitting method is to render the implanted region weaker than the bonded interface between the donor and the handle wafer. When subjected to a mechanical splitting force, the weaker region yields to the splitting force and cause delamination. Mechanical layer transfer has the advantage of producing a smooth delaminated surface and intrinsically low temperature process for the matching of dissimilar materials. The mechanical splitting process is affected by the crystal orientation and boron concentration in a similar fashion as observed for thermal splitting. We have measured the strength of the H-implanted region of <100>, <111> and <110> oriented silicon wafers by the crack opening method. The required energy for mechanical layer splitting is lowest for <100> silicon and highest for <110> silicon. These results are compared to the data reported for surface blistering of hydrogen implanted and annealed silicon wafers of various orientations. The influence of boron doping on the mechanical splitting process has been found to decrease with boron implantation at doses $> 10^{13}$ cm^{-2}. The various aspects of the mechanical and the thermal exfoliation processes will be discussed.

3:45 PM D9.2/I9.2

STRUCTURED MONOCRYSTALLINE Si FILMS FROM LAYER-TRANSFER USING THE POROUS Si (PSI) PROCESS. Richard Auer, Gregor Kuchler and Rolf Brendel, Bavarian Center for Applied Energy Research (ZAE Bayern), Erlangen, GERMANY.

We report on the successful fabrication of monocrystalline Si solar cells with a thickness of 3 to 20 microns having two- and three-dimensionally structured surfaces. We fabricate the structured films with the porous Si (PSI) process: Prior to epitaxy the surface of a Si wafer is structured by wet chemical etching and then transformed into porous Si; thus permitting layer detachment after bonding or gluing the epitaxial film to a glass carrier. The film surfaces have grooves or pyramids. The latter are periodic or random, upright or inverted. The epitaxial growth is controlled to yield either a conformal film growth or films with one surface structured and the other side planar. The surface structures modify the interaction of the epitaxial film with light and thus enable the fabrication of novel devices such as infrared diffraction grids and thin-film solar cells. For solar cells from crystalline Si, the absorption enhancement is a necessity. Applying Monte Carlo ray tracing studies we select those surface textures with particularly high absorption. The first thin-film Si solar cells that we fabricate from 17 micron-thick films with randomly positioned inverted pyramids have a power conversion efficiency exceeding 10%. The analysis of the measured internal quantum efficiency confirms efficient light trapping. The absorption enhancement is caused by an average optical path length that is 14 times the layer thickness. The fabrication of structured thin-film Si cells by layer-transfer opens a new path for the fabrication of thin monocrystalline solar modules.

4:00 PM D9.3/I9.3

TRANSFER AND HANDLING OF THIN SEMICONDUCTOR MATERIALS BY A COMBINATION OF WAFER BONDING AND CONTROLLED CRACK PROPAGATION. Joerg Bagdahn, Johns Hopkins University, Dept of Mechanical Engineering, Baltimore, MD; Dieter Katzer, Matthias Petzold, Fraunhofer Institute for Mechanics of Materials, Halle, GERMANY; Maik Wiemer, Fraunhofer Institute for Microintegration and Reliability, Chemnitz, GERMANY; Viorel Dragoi, Marin Alexe, Ulrich Gösele, Max-Planck-Institute for Microstructure Physics, Halle, GERMANY.

Many wafer bonding techniques, such as Si-Si fusion bonding using hydrophilic conditions and Si-glass anodic bonding, are based on the formation of covalent Si-O atomic bonds in the joint interface. If the interface is mechanically loaded below the fracture limit, a slow (subcritical) crack growth can occur in the bond interface depending on stress level and environmental conditions. This process can be related to a stress-activated chemical corrosion of the Si-O bonds similar to the behavior of mechanically loaded glasses and ceramics. On the other hand, most of the semiconductor bulk materials, such as Si or GaAs, are well known to be insensitive to stress corrosion processes. Therefore, the subcritical crack growth is confined to the

wafer bond interface preventing the crack to kink into the wafer material. The effect enables a controlled cleaving of direct or anodic bonded wafers and may, consequently also be utilized for the transfer and handling of thin semiconductor materials. The presented approach consists of three basic steps. First, a process wafer is bonded with a handle wafer. Subsequently, the process wafer can be back-ground to the required thickness. In the second step, all necessary technological processes such as oxidization, implantation, film deposition, high temperature annealing or etching can be performed on the process wafer without any restrictions due to the handle substrate. In the third step, the process wafer is cleaved from the handle wafer using a controlled subcritical crack growth in the bonded interface. The handle wafer will not be destroyed and can, therefore be used again for further process steps. The paper presents the fracture mechanics fundamentals of subcritical crack propagation in wafer bonded interfaces. It will be shown that an accurate control of the applied loading conditions allows to perform the separation process with a cleavage velocity in the range of millimeters per second. First results of handling and transferring of thin silicon, pyrex, GaAs and InP wafer materials will be presented and discussed with respect to potential applications in microelectronics, optoelectronics and micromechanics.

4:15 PM D9.4/I9.4
NOVEL Si/SiGe DEVICE STRUCTURES ON SiGe-ON-INSULATOR (SGOI) SUBSTRATES. Jack O. Chu, L.J. Huang, J.A. Ott, C. D'Emic, D.F. Canaperi, P.M. Mooney, S.J. Koester, H.-S. Philip Wong, IBM Research Division, T.J. Watson Research Center, Yorktown Heights, NY.

Currently Si/SiGe FET devices rely on the growth of a relaxed SiGe buffer to create the strain between Si and SiGe layer to generate quantum wells with enhanced transport properties. However, there is no straightforward integration scheme for fabricating such high performance devices on an insulator for reducing parasitic junction capacitance and for low power operations. This presentation will emphasize the fabrication of novel Si/SiGe heterostructures on SiGe-On-Insulator (SGOI) substrates fabricated for the first time by wafer bonding and hydrogen-induced layer transfer. Process flows will be described for the H-induced layer transfer of a relaxed SiGe layer, with Ge content ranging from 15% to 25%, to a Si handle wafer (5" or 8") that had 300nm thermally grown SiO_2. By using this technique, SGOI substrates can be generated with different Ge contents to effectively control the amount of strain which will be imparted to the SiGe device structures during its growth on these SGOI. For device fabrication, high quality strained Si and SiGe layers, as chacterized by X-ray and XTEM analysis, have been successfully grown of these SGOI structures after a CMP step using the UHV/CVD technique in the temperature range 500-550C. In particular, we grew several n-type modulation-doped SiGe heterostructures on these SGOI substrates which yielded high electron mobility in the range of 1500-2000 cm^2/Vs and about 40,000 cm^2/Vs at room temperature and 30K, respectively. This is the first time a modulation-doped SiGe heterostructure has been fabricated on an insulator. Similarly, the growth of p-type MODFETs' are currently in process and enhanced hole mobility in the range of 500-1000 cm^2/Vs is expected.

4:30 PM D9.5/I9.5
GETTERING CONTROL AT BONDING INTERFACE IN ELTRAN^{TM}. K. Momoi, M. Ito, N. Sato, N. Honma and T. Yonehara, Canon Inc., ELTRAN Business Center, Kanagawa, JAPAN.

Metal gettering capability in SOI wafers that is different from bulk wafers would be a key to establish the robust process for high dense SOI devices. Only a few reports have discussed the gettering mechanism of bonded SOI. In this paper, the correlation of gettering site formation at the bonding interface with bonding pre-treatments was studied for ELTRAN^{TM} SOI-Epi wafers^{TM}, which is characterized by bonding of epitaxial Si on porous Si, splitting and etching back of porous Si. A thermally oxidized epitaxial Si over porous Si was bonded with a Si handle wafer. Both hydrophobic and hydrophilic handle wafer surfaces were examined. The surfaces of the completed ELTRAN wafers were artificially contaminated by Fe, Ni and Cu, and were annealed at 1050°C for 3 hours in nitrogen ambient to diffuse them into the wafers. ICP-MS analysis in conjunction with a step etching method revealed that the metal concentration in the top Si layer in case of the hydrophobic treatment was 1/4 - 1/17 lower than that of both buried oxide (BOX) and the bonding interface. This result suggests that the bonding interface has the metal gettering capability. It was found by X-TEM observation that small cavities, "nano gaps", which had a few nm deep and anisotropic rectangular shapes with the density of $10^{11}/cm^2$ were generated at the bonding interface only by the hydrophobic treatment, although they were not observed in the hydrophilic. Diffused metals were presumably segregated at the inner surface of the "nano gaps". Further investigation about the gettering mechanism by the "nano gaps" will be discussed in the meeting. It was possible to form and reproduce the gettering sites by controlling the surface treatments prior to wafer bonding. This technology would be promising because no additional steps are necessary for SOI wafer manufacturing.

4:45 PM D9.6/I9.6
CHARACTERIZATION OF OPTICAL LIFETIME IN SILICON-ON-INSULATOR WAFERS BY PHOTOLUMINESCENCE DECAY METHOD. Shigeo Ibuka, Michio Tajima, Institute of Space and Astronautical Science, Sagamihara, JAPAN; Atsushi Ogura, NEC Corporation, System Devices and Fundamental Research, Tsukuba, JAPAN.

We report observation of the lifetime of the luminescence due to an electron-hole droplet (EHD) in silicon-on-insulator (SOI) wafers, and demonstrate its application to characterization of the crystalline and interfacial quality of SOI wafers. Formation of the EHD in a superficial Si layer was realized using pulsed ultraviolet laser light as an excitation source, because of its shallow penetration depth and confinement of photo-excited carriers within the layer. The EHD lifetime of SOI wafers was shorter than that of a bulk Si wafer, and was further reduced after removal of the surface oxide layer. We also found that the lifetime of bonded SOI wafers was shorter in the wafer with a bonding interface between the superficial layer and oxide interlayer than in the wafer with the interface between the interlayer and substrate. These findings can be explained by the difference in the recombination process via surface and interface states, suggesting that the EHD lifetime is applicable to the characterization of the surface, interface and bond quality of SOI wafers. The EHD lifetime also depended on wafer vendors and the fabrication techniques in commercial SOI wafers with the same thickness and surface conditions, although there were negligible differences in the luminescence spectral shape among the wafers. We believe that the dependence originates from the crystalline and interfacial quality of the superficial Si layer. We therefore propose that the EHD lifetime measurement has great potential for characterization of SOI wafers. This work was supported partly by JSPS Research for Future Programs under the project: "Ultimate Characterization Technique of SOI Wafers for Nano-Scale LSI Devices".

SESSION D10: SEQUENTIAL LATERAL SOLIDIFICATION OF Si FILM

Chairs: Tolis T. Voutsas and Shuichi Uchikoga
Thursday Morning, April 19, 2001
Franciscan I (Argent)

8:30 AM *D10.1
SINGLE-AXIS PROJECTION SCHEME FOR CONDUCTING SEQUENTIAL LATERAL SOLIDIFICATION OF Si FILMS FOR LARGE-AREA ELECTRONICS. A. Limanov, Institute of Crystallography Russian Academy of Sciences, Moscow, RUSSIA; and V. Borisov, TRINITI, Troitsk, RUSSIA.

Sequential Lateral Solidification (SLS) method allows obtaining high-quality Si films on low temperature glasses with mobility above 500 cm^2/Vs. Conventional SLS is performed by two-axis projection of narrow slit mask to induce local melting, and in order to obtain high efficiency from low per-pulse increment; mask with large two-dimensional array of narrow slits is used. By such a way, SLS process is performed similar to lithography process requiring medium resolution spherical UV optics and precision stepper stage. This work deals with a simple alternative approach, which uses a single axis (i.e., cylinder) projection optics. The method employs a long single melting line extended many centimeters in length. The line is formed by projection of single slit in bulk metal mask. Some aspects of efficiency, potential, and technical challenge of the method will be discussed. This method is particularly useful with low pulse energy and high frequency excimer lasers, and one of most efficient way of providing directionally crystallized Si films over a large area. Also, several types of excimer lasers were tested for SLS technique. It was found that among any parameters pulse duration is a more important one, e.g., an increase in pulse duration from 25 to 150 ns results in increase of lateral growth distance by about four times. Most efficient single-axis SLS process was obtained by using high repetition rate (up to 3 KHz), high aspect ration (aperture 2 x 30 mm^2) laser. Effective crystallization velocity up to several mm per second was obtained for the case.

9:00 AM *D10.2
HIGH PERFORMANCE POLY-Si TFTs FORMED IN SLS MATERIALS. S.D. Brotherton, Philips Research Labs, Surrey, UNITED KINGDOM; M.A. Crowder, A.B. Limanov, J.S. Im, Prog. in Materials Science and Engineering, Columbia Univ., New York, NY.

Sequential Lateral Solidification (SLS) has been established to yield large grain poly-Si [1], in which the microstructure has been correlated with the details of the laser irradiation conditions[2]. In

this paper, we further correlate those conditions with the properties of the TFTs formed in the SLS material. The results to be reported will include the dependence of device characteristics on film thickness, laser energy density and pulse translation distance. The dependence on pulse translation distance is such that there is an abrupt change in the results depending upon whether the translation distance is small enough to lead to continuous grain propagation or is larger than half the beamlet width, such that continuous propagation is not maintained and the resulting microstructure contains a regular array of grain boundaries. This latter situation results from the maximum throughput conditions of just two shot irradiations. These two sets of conditions will be contrasted both in terms of basic device characteristics, as well as the uniformity of those parameters. From these results, we will demonstrate that SLS can be used to produce high performance TFTs (mobility $>$ 400 cm^2/Vs and leakage currents of $<$ 40fA/mm), and that, under optimal conditions, uniformity of $\sim \pm 2\%$ has been achieved.

9:30 AM D10.3
NUMERICAL MODELING OF HIGH REPETITION RATE PULSED LASER CRYSTALLIZATION OF SILICON FILMS ON GLASS.
Juergen R. Koehler, Ralf Dassow and Juergen H. Werner, University of Stuttgart, Institute of Physical Electronics, Stuttgart, GERMANY.

We use a pulsed frequency-doubled diode pumped Nd:YVO_4 laser to crystallize amorphous silicon films on glass. Thin film transistors with n-type and and p-type channels fabricated from these films display field effect mobilities of 510 cm^2/Vs and $230 cm^2/Vs$ respectively, each with a standard deviation of less than 5%. Our contribution investigates the crystallization behavior for pulsed lasers with very high repetition rates up to 100 kHz for films of different thicknesses. We determine the influence of the lasers repetition rate as well as of the film thickness on the grain size of the resulting polycrystalline silicon films. Our experimental results indicate a strong dependence of the grain size on the film thickness as well as on the repetition rate of the laser, as long as the repetition rate exceeds 20 kHz. The grain size increases from 0.27 μm to 3.59 μm if both the film thickness and the repetition rate increase from 50 nm to 300 nm and 20 kHz to 100 kHz, respectively. In order to model the experimental results, we use a purpose developed two-dimensional finite difference numerical model. The program calculates the spatial and temporal evolution of the temperature in the silicon film and in the glass substrate. Our model considers the most relevant physical processes like temporal evolution and spatial distribution of the laser pulse, phase dependent surface reflection, surface-interface interference, temperature dependent absorption, free carrier absorption, latent heat as well as the substrate displacement between two laser pulses. The numerical results indicate an almost linear correlation between the solidification velocity and the grain size. Both, an increase of the film thickness, and the increase of the repetition rate decrease the solidification velocity. Thicker silicon films contain more latent heat and therefore cool down less rapidly, whereas higher repetition rates lead to a significant heating up of the substrate, with the consequence of a smaller temperature gradient at the silicon-glass interface. The results of our model are in good agreement with the experimentally measured grain sizes.

9:45 AM D10.4
SEQUENTIAL LATERAL SOLIDIFICATION SCHEMES FOR RAPID CRYSTALLIZATION OF As-DEPOSITED AMORPHOUS SILICON FILMS.
Robert S. Sposili, M.A. Crowder, and James S. Im, Division of Materials Science and Engineering, Department of Applied Physics and Applied Math, Columbia University, New York, NY.

High-performance silicon-based TFTs require low-defect-density crystalline thin silicon films as a starting material. The sequential lateral solidification (SLS) process has been shown to be capable of producing such materials and shown to possess a wide energy-density processing window. SLS is an intrinsically flexible method that can be implemented using many different schemes and configurations. An unfortunate consequence of the flexibility of the process is the persistence of misconceptions about the effective overall crystallization rate associated with the method, particularly when implemented using an excimer laser (as opposed to other high-power UV lasers) and two-axis projection-irradiation. In this paper, we reveal specific technical schemes - using the aforementioned combination of an excimer laser and projection irradiation - for implementing SLS that result in very high effective overall crystallization rates. We will illustrate rapid crystalli-zation using as an example a two-shot irradiation SLS scheme, which results in uniform and large-grained polycrystalline material covering the entire film. This approach makes use of a continuous serpentine sweep of the beam over the substrate, and thus minimizes the potential delays associated with stepping and settling of the translation stage. Based on currently available equipment specifications (1 J/ pulse, 300 Hz, 40% optical efficiency, 1 J/cm^2 fluence at the sample plane, 550 mm $\times$ 670 mm substrate size), effective crystallization rates greater than 50 cm^2 /s can be realized. TEM and SEM micrographs of the resulting material will be presented, and the important parame-ters will be discussed. We will also discuss how these rapid crystallization schemes can be extended to produce location-controlled directionally solidified microstructures and small single-crystal regions at similarly high rates of crystallization. This can be implemented, for example, using a 1:1 projection scheme, which utilizes split-beam irradiation to reduce the fluence at the mask plane below the mask damage threshold. This work was supported by DARPA under project N66001-98-1-8913.

SESSION D11: MICROSTRUCTURE ANALYSIS OF CRYSTALLIZED Si FILMS

Chair: Tolis T. Voutsas
Thursday Morning, April 19, 2001
Franciscan I (Argent)

10:30 AM *D11.1
MICRO-STRUCTURE FORMATION DURING LASER CRYSTALLIZATION OF SILICON FILMS.
Horst P. Strunk, Department of Materials Science and Engineering, Institute of Microcharacterization, University of Erlangen-Nuremberg, GERMANY.

Laser crystallization of silicon films is one of the potential techniques that may lead to starting material for the production of high quality transistor arrays in displays and of advanced thin film solar cells. The re-solidification that follows the laser irradiation of a precursor silicon film proceeds rather rapidly. The accompanying kinetic effects need to be analyzed and controlled in order to achieve a micro-structure of the resulting films that is compatible with the required electronic and optical properties. The main parameters of the micro-structure are the grain size, the surface normals of the grains, and the grain boundary population. In view of the electronic requirements, layers are desirable with very large grains, which simulate single crystalline material, with a narrow distribution of surface normals, preferably around 001 to account for current semiconductor technology, and with electrically inactive grain boundaries. Based on extensive investigations of a variety of differently laser crystallized silicon films, characteristic micro-structures will be analyzed and compared in view of finding process parameters of optimized silicon films.

11:00 AM D11.2
MICROTEXTURE AND ORIENTATION ANALYSIS OF DIRECTIONALLY SOLIDIFIED Si FILMS USING ELECTRON BACKSCATTER DIFFRACTION METHOD.
H.-C. Jin, J.R. Abelson, University of Illinois, Department of MS&E and the Coordinated Science Laboratory, Urbana, IL; M.A. Crowder, A.B. Limanov, J.S. Im, Columbia University, Materials Science Program, New York, NY.

Polycrystalline silicon (poly-Si) thin films with directionally solidified microstructures can be achieved via sequential lateral solidification (SLS) process. In this paper, we examine the in-plane orientation and texture of the microstructure using an electron backscatter diffraction (EBSD) method in order to study the nature of the planar defects found in the material. A predominant $< 100 >$ in-plane direction of the grains along the direction of the solidification, arising presumably from competitive growth and occlusion, was observed. The disorientation and coincidence site lattice (CSL) boundary statistics show that there exist many low-angle boundaries and CSL boundaries within the material. Furthermore, most of these low-angle grain boundaries originate initially from the subboundaries that are formed within a grain. The fraction of these boundaries increases along the direction of solidification, while the CSL boundary population decreases. The CSL boundary distribution is dominated by $\Sigma = 3^n$ boundaries that are presumably formed by a deformation twinning process in diamond crystals. We will discuss the implications of the findings on the defect generation mechanism and on the electrical properties of the directionally solidified crystalline Si films obtained using SLS. Additionally, we will present EBSD results obtained from examining SLS processed silicon-on-insulator (SOI) films where the results show a strong orientation dependence of twin boundary formation.

11:15 AM D11.3
CHARACTERIZATION AND ANALYSIS OF PLANAR DEFECTS IN SEQUENTIAL LATERAL SOLIDIFICATION PROCESSED Si FILMS.
M.A. Crowder, A.B. Limanov, and James S. Im, Prog. in Materials Science and Engineering, Columbia Univ., New York, NY.

A variety of planar defects can be found within sequential lateral solidification (SLS) processed Si films, with sub-grain boundaries, stacking faults, and microtwins being the major intragrain defects. In the present investigation we utilize silicon-on-insulator (SOI) films as the starting material in order to systematically investigate the causes and mechanisms that lead to the generation of these defects. The use of SOI samples permits systematic analysis of the defect formation

mechanisms since the material is devoid of preexisting planar defects, and the exact orientation of the precursor/seed region relative to the solidification direction is known.
In this investigation, we focus primarily on examining the generation of sub-grain boundaries that result from SLS processing with straight-slit beamlets. We find that there are three distinct regions in the SLS processed SOI films: (1) an initial planar defect-free area (the extent of which can depend on laser fluence and orientation); (2) an area within which the sub-grain boundaries appear and propagate in a well-defined direction relative to the crystallographic orientation; and (3) a final steady-state area characterized by (a) sub-grain boundaries aligning to the scan direction, and (b) the in-plane texture becoming more random. These SOI experiments clearly indicate that sub-grain boundary generation requires an incubation area, and the crystal orientation changes continuously as the solidification proceeds. We discuss the implications of these results on the plastic deformation model, which we have proposed previously in order to account for the formation of sub-grain boundaries in SLS processed Si films. Finally, we point out how the results are consistent with the existence of the planar defect-free region found in chevron shaped beamlet crystallized regions.
This work was supported by DARPA under project N66001-98-1-8913.

11:30 AM D11.4
(100)-TEXTURED LASER-CRYSTALLIZED SILICON THIN FILMS ON GLASS SUBSTRATES. Melanie Nerding, Silke Christiansen, Horst P. Strunk, Universität Erlangen-Nürnberg, Institut für Werkstoffwissenschaften, Lehrstuhl für Mikrocharakterisierung, Erlangen, GERMANY; Gerd Esser, Uwe Urmoneit, Andreas Otto, Universität Erlangen-Nürnberg, Lehrstuhl für Fertigungstechnologie, Erlangen, GERMANY; J.I. Christiansen, Universität Erlangen-Nürnberg, Physikalisches Institut, Erlangen, GERMANY.

We investigate the microstructure of polycrystalline silicon films (grain size, texture and grain boundary population) on glass substrates that are realized from amorphous silicon precursor layers by scanning the raw beam of a continuous wave Ar^{+}- ion laser operated at a wavelength of 514.5 nm over the a-Si thereby crystallizing it. Transmission electron microscopy together with electron back-scattering diffraction analysis reveal that the grains assume under optimized processing conditions a width of about 10 μm and under certain processing conditions a preferred (100)-surface normal orientation forms. Whether or not a texture forms depends on the parameters that can be varied: i) dwell time of the laser (as varied by the scan velocity), ii) intensity, iii) overlap between adjacent scan lines, iv) defocus of the laser beam, v) a-Si layer thickness . The materials applicability for devices in large area electronics strongly depends on the texture, the average grain size and the defect density and population. The grain boundary population is dominated in the textured films by coincidence boundaries, essentially twin boundaries of first and second order as well as Σ=5 boundaries.

11:45 AM D11.5
INTERFACIAL MICROCRYSTALLIZATION ENCOUNTERED DURING EXCIMER-LASER INDUCED RAPID SOLIDIFICATION OF THIN Si FILMS. Hans S. Cho, Dongbyum Kim, Alexander B. Limanov, Mark A. Crowder, and James S. Im, Program in Materials Science and Engineering, Columbia University, New York, NY.

Excimer-laser-induced rapid solidification of thin Si films on glass and plastic substrates is an important means for obtaining crystallized Si films for high-performance thin films transistor and photovoltaic devices. It is recognized that the interface-led liquid-to-solid phase transition of Si can occur via either of two well-defined solidification modes, epitaxial growth or interfacial amorphization, depending on the temperature of the freezing interface. Here we propose that there exists an additional mode of solidification that can be differentiated from the above-mentioned modes, that leads to the formation of extremely defective microcrystalline (non-amorphous) materials. This mode of solidification can be viewed effectively as a transitional phenomenon bridging the epitaxial (occurring at high interface temperatures/low interface velocities) and amorphous (low temperatures/high velocities) modes, occurring at an intermediate interfacial temperature range. A working model is presented by which the microcrystalline mode of solidification (i.e., interfacial microcrystallization) is described by an effective interface response function over this range of temperature. Possible kinetic mechanisms are suggested and evaluated, ranging from defective crystalline growth to dual-phase participation, to account for the origin of the phenomenon. We argue that the phenomenon may be frequently manifested in rapid solidification of Si films, and responsible for a number of unusual microstructural features that have been observed in excimer-laser-crystallized Si. These include the heavily defective/near amorphous regions associated with breakdown of epitaxial growth during lateral solidification of ultra-thin films, the fine-grained microstructure that results from explosive crystallization, and the various microstructural features and patterns that arise from nucleation-initiated solidification within the bulk of completely melted films. The details of such features (imaged using TEM, SEM, and AFM) will be interpreted in terms of the thermal evolution of the solidification interface, as suggested by the proposed model. This work was supported by DOE under project DE-FG02-94ER45520.

SESSION D12: HIGH PERFORMANCE TFTs

Chair: Masakiyo Matsumura
Thursday Afternoon, April 19, 2001
Franciscan I (Argent)

1:30 PM *D12.1
SHORT-CHANNEL THIN FILM TRANSISTOR MODELS FOR CIRCUIT SIMULATOR. Michael S. Shur, Rensselaer Polytechnic Institute, Department of Electrical, Computer and System Engineering and Center for Integrated Electronics and Electronics Manufacturing, Troy, NY.

We review short-channel TFT models suitable for implementation in a circuit simulator, such as AIM-Spice [1], and for parameter extraction and device testing. The models cover all regimes of operation (leakage, subthreshold, and above threshold), and account for short channel effects, which are different for different types of TFTs. In poly-Si TFTs, these effects include mobility degradation at high gate biases, velocity saturation, drain-induced barrier lowering, effects of the series resistance, and floating-body effects. [2] We discuss the role of self-heating in short channel devices (in a-Si TFTs, self-heating and kink effects become important in devices with gate length shorter than approximately four micron [3]). The AC model that incorporates a fraction of the channel resistance in series with the gate-to-source and gate-to-drain capacitances accurately reproduces the frequency dispersion. With certain modifications, amorphous silicon TFT model is suitable for the simulation of organic TFTs, where dominant short channel effects are linked to a large nonlinear series resistance. [4] Future challenges include the analysis of A2B6 and A4B6 TFTs fabricated on flexible substrates or even on cloth or a thread. [1] T. A. Fjeldly, T. Ytterdal and M. Shur, 'Introduction to device modeling and circuit simulation,' Wiley, NY 1997. [2] B. Iniguez, L. Wang, Z. Xu, T.A. Fjeldly and M.S. Shur, Short Channel AIM-Spice Models for Amorphous and Polysilicon Thin Film Transistors, in Future Trends in Microelectronics. The Road Ahead, John Wiley and Sons, 1999, p. 213 [3] L. Wang, T.A. Fjeldly, B. Iniguez, and M.S. Shur, Self-heating and Kink Effects in a-Si:H Thin Film Transistors, IEEE Trans. Electron Devices, Vol. 47, p. 387, February 2000 [4] P.V. Necliudov, M.S. Shur, D.J. Gundlach, T.N. Jackson, Modeling of organic thin film transistors of different designs, J. Appl. Phys., December 15 (2000)

2:00 PM D12.2
POLY-Si THIN FILM TRANSISTORS AND DIODES ON GLASS-CERAMIC SUBSTRATES. Sergei M. Krasulya, Nikolay I. Nemchuk, Dieter G. Ast, Cornell University, Dept of Materials Science and Engineering, Ithaca, NY; J. Gregory Couillard, Corning Incorporated, Corning, NY.

We report the device characteristics of polysilicon thin film transistors and p-i-n diodes fabricated at 900°C on a novel glass-ceramic substrate developed by Corning Incorporated. The substrate is transparent and matches the coefficient of thermal expansion of Si. Its use offers a viable alternative to traditionally used glass substrates for the fabrication of high performance active matrix LCDs using poly-Si transistors. The high strain point of the substrate in excess of 900°C permits prolonged processing at 900°C and, thus, allows to replace the costly process of laser recrystallization by either conventional thermal annealing or by using metal induced crystallization followed by a high temperature upgrading step. To verify that devices could be fabricated on of this substrate at high temperatures, we developed a simple 900°C process to fabricate poly-Si thin film transistors and solar cell prototypes (p-i-n diodes). In this process, the silicon layer is patterned prior to the high temperature step. A very important step in device fabrication is the design and deposition of the barrier layer. This barrier layer is needed to prevent the diffusion of detrimental chemical elements from the substrate into the thin poly-Si film. To verify that our barrier layer(s) prevented the outmigration of impurities, we fabricated devices on barrier layer coated glass-ceramic substrates as well as on oxidized silicon and fused silica. Thin film transistors fabricated on glass-ceramics had electrical characteristics similar to those made on oxidized silicon and fused silica substrates. Small differences in TFT performance were found to be caused by the different surface roughness of the substrates used rather than chemical differences. On the other hand, p-i-n diode on different substrates had markedly different electrical characteristics. The origin of these differences was traced to the relationship of thermal expansion coefficient of the substrates to that of the deposited silicon film. In the case of glass ceramics and oxidized silicon substrates, the expansion coefficient is matched and no residual stress develops. On fused silica, however, the poly-Si film is under a high tension after the

final 900°C step. In small devices, such as TFTs, these stresses are insufficient to cause cracking, but in large area devices cracks develop that degrade the electrical performance.

2:15 PM D12.3
SINGLE-CRYSTAL THIN FILM TRANSISTOR BY GRAIN-FILTER LOCATION-CONTROLLED EXCIMER LASER CRYSTALLIZATION. Barry D. van Dijk, Paul Ch. van der Wilt, G. Jurgen Bertens, Ryoichi Ishihara, Delft University of Technology, DIMES, Delft, THE NETHERLANDS.

There is a wide interest for fabricating single-crystal thin film transistors (TFTs) in a low-temperature process. In liquid crystal displays such transistors could for instance facilitate integration of the system (e.g. memory and CPU) on the glass substrate. A way to obtain single-crystal silicon, is to eliminate grain boundaries in polycrystalline silicon; this requires control of the location of the grain. We have developed a method to control the location of large silicon grains **[1]**. In this method a narrow hole was made in an isolating layer, which was subsequently filled with amorphous silicon. The film was illuminated by a single shot of excimer laser light, with such an energy that the silicon in the hole was nearly completely molten. The unmolten portion in the narrow hole seeds vertical grain growth. During this stage, crystal-orientation dependent competitive growth ideally results in only one grain reaching the edge of the hole. This grain then grows laterally into a large single-crystal island, and growth continues until impingement with grains grown from copious nucleation in the undercooled melt. Thin film transistors were fabricated inside location controlled grains using a low temperature process. The gate dielectric is silicondioxide, deposited by LPCVD using silane and oxigen as source gasses. Source and drain areas were defined by a self-aligned ion implantation, using the aluminium gate as a mask. The dopants were activated by excimer laser annealing. TFTs with different channel widths and lengths were fabricated. In a first experiment TFTs with a high field-effect mobility for electrons of 450 cm^2/Vs were made. However, the off-current and subthreshold slope were high, 10^{-10} A and 1.9 V/dec, respectively. Grain analysis by Schimmel etching showed that still few grain boundaries were present. By improving grain quality we expect to improve the off-current and the subthreshold slope.
[1] P.Ch. van der Wilt et.al., Symposium Proceedings of MRS Spring 2000 Meeting, Symposium Q, to be published.

2:30 PM D12.4
EFFECT OF EXCIMER LASER ANNEALING ON ULTRA-LOW TEMPERATURE GATE DIELECTIRCS. Wonsuk Chung, Michael O. Thompson, Cornell Univ, Dept of MS&E, Ithaca, NY.

Thin-film poly-crystalline transistors on low temperature substrates (plastic, glass) are normally fabricated as metal gate devices. Formation of poly-Si gates requires an additional laser-annealing step to crystallize the films, subjecting the gate dielectrics to similar conditions. In this work, we have investigated the effect of such excimer laser induced crystallization of poly-Si on low temperature (<150°C) gate dielectrics. PECVD conditions were optimized for growth of low temperature oxides, including gas flow rates and ratios, power densities and pressures. Pre-annealing conditions at 150°C are optimal under silane deficit, high power, and low-pressure conditions. Dielectrics, as deposited, were characterized by ellipsometry, TEM, RBS and FRES, FTIR, P-etch, and CV/IV electrical methods. Stacks of optimized SiO_2/Si and Si/SiO_2/Si structures (on both Si wafer and thin TFT Si) were then irradiated using an homogenized 308nm excimer laser at fluences varying from 50mJ/cm^2 to 700mJ/cm^2, for varying numbers of shots. Structural and electrical changes in the oxide and poly-Si gate were measured. Residual H in the oxide is readily released by the laser process. At moderate fluences, the threshold voltage is found to decrease by as much as 4 volts (from 12 volts as deposited). Results suggest that significant thermal annealing can occur during the laser irradiation and is adequate to explain the bulk and interface improvements. Preliminary data for TFT devices fabricated by intentional laser annealing of the gate dielectric will be presented.

2:45 PM D12.5
FABRICATION AND CHARACTERIZATION OF POLY-Si SCHOTTKY-BARRIER THIN-FILM TRANSISTORS. Horng-Chih Lin, Tiao-Yuan Huang, National Nano Device Laboratories, Hsin-Chu, TAIWAN; K.-L. Yeh, R.-G. Huang, M.-F. Wang, National Chiao-Tung University, Institute of Electronics, Hsin-Chu, TAIWAN.

Poly-Si Schottky-barrier thin-film transistors (SB-TFT's) were fabricated and characterized. SB-TFT's were fabricated by skipping the normal channel and source/drain (S/D) implantation steps. Instead, a self-aligned silicidation (salicide) process was performed to form the Schottky-barrier S/D. This results in a greatly simplified “implantless” processing, and features a low thermal budget, as post-implant annealing step is also eliminated. Moreover, SB-TFT's exhibit ambipolar (i.e., both p- and n-channel) operation capability, which is very useful for CMOS logic applications. In this study, SB-TFT's were first fabricated by using the sidewall spacer to isolate the gate and S/D regions during salicidation. However, it was found that these SB-TFT's depict poor on/off current ratio (<103) as well as severe GIDL (gate-induced drain leakage)-like leakage current. To overcome these shortcomings, a novel SB-TFT structure is also proposed in this study to improve the device performance. The new device consists of a field-induced-drain region (i.e., an offset drain region controlled by a metal field-plate lying on top of the passivation oxide) sandwiched between the silicided drain and the active channel region. Carrier types and the conductivity of the transistor are controlled by the metal field-plate. Since the metal field plate is formed during regular metal patterning, no additional processing steps are required. Our results show that the new devices can significantly improve the on/off current ratio to 106 for both p- and n-channel operations, while effectively eliminating the GIDL-like leakage.

3:30 PM *D12.6
LOW TEMPERATURE PROCESS TECHNOLOGIES FOR THE NEXT GENERATION HIGH PERFORMANCE POLYCRYSTALLINE SILICON THIN-FILM TRANSISTORS. Seiichiro Higashi, Seiko Epson Corp., Base Technology Research Center, Nagano, JAPAN.

Basic analyses and developments on low temperature process technologies for the next generation high performance polycrystalline Si thin-film transistors (poly-Si TFTs) are reported. There are three important process technologies in TFT fabrication, which are laser crystallization, plasma treatment of poly-Si films and SiO_2/Si interface formation. The pulsed laser induced fast melting and solidification of Si thin films were investigated using $in-situ$ measurements of transient reflectance and conductance of Si films. The experiment suggested that the complete melting of the Si films and subsequent supercooling induce microcrystallization and amorphization. The homogeneous nucleation phenomenon at 640 K below the melting point resulted in microcrystallization. The analyses on the electrical properties of laser crystallized poly-Si films suggested that the trap states were localized at the grain boundaries. In addition, the density of the trap states was found to be in the order of 10^{18} cm^{-3}. Plasma treatments to the poly-Si films at 250°C efficiently terminated these trap states and reduced the density of trap states in the order of 10^{16} cm^{-3}. As a result, laser crystallization and subsequent plasma treatment offer good quality polycrystalline Si films. In order to deposit SiO_2 films with less plasma damage to the Si surface, electron cyclotron resonance plasma enhanced chemical vapor deposition (ECR PECVD) was investigated. SiO_2 film depositions at room temperature and subsequent H_2O vapor annealing at 333°C realized SiO_2/Si interfaces with the density of interface trap states (D_{it}) of 1.8x10^{10} $cm^{-2}eV^{-1}$. This result suggests that it is possible to form device quality SiO_2/Si interfaces whose D_{it} is comparable to that of thermally grown SiO_2 films. As seen in the above investigations, we have developed low temperature process technologies that can offer good quality poly-Si films and SiO_2/Si interfaces. This result strongly suggests the possibility of realizing high performance poly-Si TFTs.

4:00 PM D12.7
CHARACTERIZATION OF LOW TEMPERATURE POLYSILICON TFTS WITH SELF-ALIGNED GRADED LDD STRUCTURE. Ching-Wei Lin, Li-Jing Cheng, Yin-Lung Lu, and Huang-Chung Cheng, National Chiao Tung University, Institute of Electronics, Hsinchu, Taiwan, R.O.C.

A new process for manufacturing low temperature polysilicon (LTPS) TFTs with self-aligned graded LDD structure was demonstrated. The graded LDD structure was self-aligned by side-etch of Al under the photo-resist followed by excimer laser dopant activation. The graded LDD polysilicon TFTs were suitable for high speed operation and active matrix switches applications because they possessed low-leakage-current characteristic without sacrificing driving capability significantly and increasing overlap capacitance. Furthermore, due to graded dopant distribution in LDD regions, drain electric field could be reduced further, as a result, graded LDD polysilicon TFTs provided high reliability and desired output characteristics for high voltage operations. In this paper, effects of LDD length and laser shot number during dopant activation on the performance and reliability of TFTs were also discussed.

SESSION D13: LOW TEMPERATURE DEPOSITION OF SiO_2
Chairs: Jin Jang and Hyun Jae Kim
Thursday Afternoon, April 19, 2001
Franciscan I (Argent)

4:15 PM D13.1
HIGH QUALITY GROWTH OF SiO_2 AT 80°C BY ELECTRON

CYCLOTRON RESONANCE (ECR) FOR THIN FILM TRANSISTORS. Riyaz Rashid, A.J. Flewitt, John Robertson, W.I. Milne, Cambridge University, Dept. of Engineering, UNITED KINGDOM.

Polysilicon is required for the next generation of active matrix liquid crystal display (AMLCD) technology, which integrates complementary metal oxide semiconductor (CMOS) switching circuits onto the display substrates. These devices require thin, made at low temperature, high quality dielectrics. SiO_2 is the insulator of choice because its wide band gap (9eV) acts as a large barrier for both electrons and holes, and has excellent interfacial properties. Low temperature rf plasma enhanced chemical vapor deposition (rf-PECVD) oxides incorporate considerable hydrogen (5-15 at.%) as O-H and Si-H bonds, which cause instabilities. In ECR-PECVD, a highly ionised plasma ($\sim 10^{16} m^{-3}$) with low ion energies ($\sim$10eV) gives more efficient dehydrogenation while not creating extra defects. Further H removal is provided by He ions, which also help densify the films. In the deposition of ECR oxides, O_2 and He are injected upstream of the resonance zone and SiH_4 is injected downstream near the growth surface. O_2 is used rather than N_2O so that N-H groups are not incorporated. High quality material at 80°C, with a resistivity of $>10^{14} \Omega$cm and an average breakdown strength of $5 MVcm^{-1}$ has been produced using a oxygen/silane ratio of >2:1. The physical properties include a refractive index of 1.45 and etch rates in buffered HF below $10 Å s^{-1}$. The hydrogen content in these films were less than 3 at.% mainly bonded as Si-OH while no significant SiH impurity groups were detected. Low interface state densities of $10^{11} eV^{-1} cm^{-2}$ and fixed oxide densities of about $10^{10} cm^{-2}$ have been achieved for these as-deposited oxides compared to thermal oxides. The stability is being tested in devices.

4:30 PM D13.2
PREPARATION AND CHARACTERIZATION OF LOW TEMPERATURE SILICON DIOXIDE THIN FILMS USING TETRAMETHYSILANE (TMS) FOR MICROFABRICATION APPLICATIONS. Xin Lin, Motorola SPS, Mesa, AZ; Stephen Fonash, The Pennsylvania State University, University Park, PA.

Low temperature silicon dioxide depositions have been carried out by plasma enhanced chemical vapor deposition (PECVD) using TMS as Si precursor at 100–200°C in the pressure range of 2–8 Torr. An RF power of 40 W and a TMS:O_2 gas flow rate ratio of 1:500 without inert gas dilution were used in the depositions. It was found that the current-voltage (I-V) characteristics of as-deposited oxide films improved as the substrate temperature increased or deposition pressure decreased. Oxide films deposited at 2–3 Torr exhibited typical Fowler-Nordheim (F-N) tunneling characteristics and breakdown voltages greater than 8 MV/cm. The best capacitance-voltage (C-V) characteristics, giving a small flat band voltage shift, small amounts of positive oxide charge, a small hysteresis in bi-directional C-V sweep, and a low interface trap density, were obtained at 3 Torr. Post-deposition annealing in forming gas at the deposition temperature was performed and proved to be an effective approach to improving the electrical properties of the deposited oxide films without compromising the low temperature aspect of the process. By annealing at 200°C, the F-N tunneling barrier height increased by as much as 0.6 eV, the flat-band voltage and the hysteresis in C-V sweep were reduced by 0.74 V and 0.08 V, respectively. In addition, hydrogen was found to play a key role in the annealing treatment and its mechanisms were discussed.

4:45 PM D13.3
THE ELECTRICAL PROPERTIES OF $SrTa_2O_6$ THIN FILMS DEPOSITED BY CYCLIC PLASMA ENHANCED CHEMICAL VAPOR DEPOSITION(C-PECVD). Won-Jae Lee, Chang-Ho Shin, In-Kyu You, Il-Suk Yang, Byoung-Gon Yu, Kyoung-Ik Cho, Micro-Electronics Technology Laboratory, ETRI, Daejon, KOREA; Soon-Gil Yoon, Dept of Materials Engineering, Chungnam National University, Daejon, KOREA; Chun Su Lee, Genitech. Inc, Daejon, KOREA.

Thin dielectric layers are of the great importance and range widely in applications such as the dielectrics in semiconductor devices and in electrolytic capacitors, and the protective layer in electroluminescent (EL) thin film display. In particular, alternate materials with a permittivity higher than that of SiO_2 are needed to be able to use thicker gate dielectrics in achieving the required capacitances without tunneling currents, and thereby continue the evolution toward higher integration densities. The reduction of thin film to nanometer dimension for new technologies requires exquisite control of film thickness, morphology, crystallinity and conformallity. Many of these requirements can be achieved by growth controlled at single atomic layers by means of binary reaction sequence chemistry. Atomic layer deposition (ALD) offers excellent large-area uniformity and conformality and enables simple and accurate control of film thickness and composition at an atomic layer level. In this study, high dielectric $SrTa_2O_6$ films were deposited on platinized silicon substrate by alternating supply of $Sr[Ta(OEt)]_2$dmae and O_2 for ALD process. Deposition of all STO films were carried out at the substrate temperatures of between 200 and 300°C and at a pressure of 1.5 torr. Ar gas was used as the carrier gas and purge gas. The plasma was generated to activate oxygen gas in the period of O_2 gas pulse. Finally, the electrical properties of $SrTa_2O_6$ (STO) thin films prepared by ALD technique on $Pt/SiO_2/Si$ substrates with annealing temperatures have been investigated. It was observed that the uniform and conformal STO thin films were successfully deposited using ALD. While the grain size and dielectric constant of STO films increased with increasing annealing temperatures, the leakage current characteristics of STO films slightly deteriorated. The leakage current density of a 40nm-STO film was about $5 \times 10^{-8} A/cm^2$ at 3V.

SESSION D14: FIELD EMISSION DISPLAYS I: ARRAYS
Chair: Andrei Chakhovskoi
Friday Morning, April 20, 2001
Franciscan I (Argent)

8:30 AM *D14.1
SMART FIELD EMISSION ARRAYS. A.I. Tayo Akinwande, D.G. Pflug, C.Y. Hong, M. Ding and P.R. Herz, Microsystems Technology Laboratories, Massachusetts Institute of Technology, Cambridge, MA.

Field emission devices based on metals and semiconductors are under investigation for display and microwave amplifier applications. There is particular interest in field emission from silicon because of the reproducibility and uniformity of silicon fabrication technology. Major challenges of silicon field emission devices include high turn-on voltage, non-uniformity and instability of the current. We report the following: reduction of the turn-on voltage to a value less than 10 V through the use of aperture scaling using interferometric lithography and very uniform field emission from silicon field emission arrays. In this paper, a MOSFET is added in series with Si FEAs resulting in a device whose emission current is controlled by the gate of the MOSFET. In this device, the supply of electrons by the inversion layer of the MOSFET limits emission current rather than transmission through the surface barrier. In this mode of operation, the MOSFET stabilizes the current and lowers the switch voltage of the FEA. We report the control of emission current from a MOSFET/FEA structure which has a MOSFET threshold voltage of -2.4 V and controls emission current over 4 orders of magnitude with a 0.3 V MOSFET gate voltage swing.

9:00 AM D14.2
OXIDATION OF MOLYBDENUM THIN FILMS AND ITS IMPACT ON MOLYBDENUM FIELD EMITTER ARRAYS. Babu R. Chalamala, Robert H. Reuss, Motorola, Inc., Semiconductor Products Sector, Digital DNA Laboratory, Tempe, AZ; Yi Wei, Motorola, Inc., Motorola Labs, Tempe, AZ; John M. Bernhard, Edward D. Sosa, David E. Golden, Department of Physics, University of North Texas, Denton, TX; Sanjeev Aggarwal, R. Ramesh, Department of Material Science, University of Maryland, College Park, MD.

Oxidation of emitter surfaces is a serious problem for Mo field emitter arrays. In this paper, we present studies on the oxidation and related changes in the electronic properties of Mo thin films as a function of annealing temperature. Experiments were done on Mo thin films prepared on Si substrates. These films were thermally oxidized and characterized using a variety of techniques including x-ray diffraction, x-ray photoelectron spectroscopy, ultraviolet photoelectron spectroscopy and thermal desorption spectroscopy methods. For films oxidized below 400°C, partial oxidation was observed, with MoO_3(110) being the principal oxide phase. However, at a temperature of 500°C and above, oxidation of the film was complete. Electrical characteristics of the films undergo a rapid transition from semiconductive to highly insulating at temperatures between 475 to 500°C. Temperature programmed desorption spectra showed that the oxides are stable at elevated temperature with only a principal O_2 desorption peak at approximately 786°C along with two much smaller peaks at 586 and 665°C. However, release of gas phase components of Mo and MoO_2 were not observed at the lower temperature, indicating that the O_2 desorption at the lower temperature is either due to a phase transition or outgassing of excess bound oxygen from the film. The work function of the MoO_3 phase of the oxide was found to be 2.52 eV and the MoO_2 phase 3.20 eV. In contrast, the reference work function value for Mo(110) film was 4.6 eV. Even though the oxides have a low work function, they are insulating and do not have free electrons in their conduction bands. Thus when thin insulating oxides are formed on field emitters, the net effective tunneling barrier increases, leading to emission current degradation.

9:15 AM D14.3
DOUBLE-GATED SINGLY-ADDRESSABLE POLYSILICON TIP ARRAY FABRICATION AND CHARACTERIZATION.
N.N. Chubun, A.G. Chakhovskoi, M. Hajra and C.E. Hunt, Dept. of Electrical and Computer Engineering, University of California, Davis, CA.

Polysilicon-on-insulator singly-addressable arrays, consisting of double-gated field emission cells, were fabricated and tested. The field-emission tips were formed by a subtractive technique, using 2 μm thick polysilicon strips on the insulating substrate. The tip structure was oxidized for dielectric isolation and coated with a 0.4 μm polysilicon layer as a first gate electrode. The polysilicon layer was then oxidized to provide second isolation layer for separation from a 0.1 μm gold film, deposited as a second gate electrode. Finally, an 1.0 μm aperture was opened, using wet etching of the silicon dioxide. The structure allows us to electrically address a single tip at the intersection of any cathode row and polysilicon gate line. An independent voltage can be applied to the second gate film of any tip to focus the electron beam of an operating tip, or, conversely, to reduce the dark current of the emission cell which is switched off. The emission properties and electron-optic features of the cathode array are reported. The influence of the anode, placed in a close proximity, on the emission characteristics of the array are assessed

9:30 AM D14.4
NUMERICAL SIMULATION OF ELECTRON TRANSMISSION THROUGH MODIFIED SCHOTTKY BARRIERS.
Kevin L. Jensen, Naval Research Laboratory, Washington, DC.

Injecting charge into the conduction band of diamond and other wide band gap materials is a prerequisite for exploiting their low or negative electron affinity characteristics as electron sources for rf amplifier devices. The lure of competitive emission current densities at low applied fields therefore motivates interest in such cold cathodes as replacements for traditional thermionic electron sources. The modeling of electron transport through such films will require a knowledge of the incident electron energy distribution through (or over) the Schottky barrier which exists at the metal-semiconductor (or semiconductor-semiconductor) interface. Estimations of tunneling current and energy distributions are complicated by a host of modifications, such as interfacial layers, quadratic potentials associated with a depletion layer, neutral or charged defects, and the like. Previous work showed that the inclusion of a defect-like potential within a tunneling barrier could substantially enhance emitted current in the vicinity of the inclusion [1]. Further, a numerical method (Modified 1-D Airy Function Approach) for evaluating emission current for arbitrary potential profiles has been recently perfected [2]. We apply the modified Airy Function approach to a depletion layer barrier with a statistical distribution of defect-like modifications in order to make qualitative estimates of enhanced transmission. In particular, while the quadratic nature of the barrier tends to decrease the current density, the presence of a defect-like potential near the interface tends to enhance the transmitted current substantially. Estimates of the defect statistics will be addressed: in particular the average site-to-site separation for a triangular lattice, the dependence on distance from the interface, and the potential presence of an interfacial layer, will be addressed. [1] K.L. Jensen, J.L. Shaw, Mat. Res. Soc. Symp. Proc. Vol. 621, R3.3.1 (2000). [2] K.L. Jensen, (to appear in 198th ECS Symposium I1 Proceedings Volume, (Oct. 2000).

SESSION D15: FIELD EMISSION DISPLAYS II: MATERIALS

Chair: Huei Pei Kuo
Friday Morning, April 20, 2001
Franciscan I (Argent)

10:15 AM *D15.1
IN SITU OPTIMIZATION OF MICOFABRICATED CATHODE EMISSION.
P.R. Schowebel, Applied Physical Sciences Laboratory, SRI International, Menlo Park, CA; J.A. Panitz, Dept of Physics and Astronomy, University of New Mexico, Albuquerque, NM.

The use of microfabricated field emission cathodes in applications of technological importance has been hindered by difficulties in obtaining acceptable emission characteristics in the vacuum environment of the device. We have investigated in situ surface cleaning and annealing using pulsed electron emission to achieve high current densities at the emitter apex. Pulsed electron emission produces surface temperatures in excess of 800°C for tens of microseconds. This enhances the temporal stability and the spatial uniformity of emission under normal operating conditions. The microfabricated structure required to survive the pulsing procedure may allow the emitter apex to be characterized by Imaging Atom-Probe mass spectroscopy.

10:45 AM D15.2
ANOMALIES IN THE BEHAVIOR OF Mo FIELD EMITTER ARRAYS IN INERT GASES AND SOME INSIGHTS INTO THE DEGRADATION MECHANISMS.
Robert H. Reuss and Babu R. Chalamala, Motorola, Inc., Semiconductor Products Sector, Digital DNA Laboratory, Tempe, AZ.

The operational life of field emission displays is related to the package pressure. During residual gas analysis of a large number of field emission displays, we found that Ar was a dominant gas species inside these packages. After a careful analysis of the device fabrication process, we traced the source of Ar to sputtered metal films. So far, most of studies on the interaction between field emitter arrays and residual gases have been limited to oxygenic species. As Ar is a major constituent of the display vacuum, a good understanding of its effects on the emission characteristics of Mo field emitter arrays is necessary. In this paper, we present experimental results on the effects of Ar, Xe and He on Mo field emitter arrays, and propose mechanisms to explain the observed behavior. Experiments were done on a large number of Mo arrays for exposure times ranging 20 to 100 hours at various partial pressures of He, Ar and Xe. We found that the emission current change is most pronounced in the early part of gas exposures, with further exposure resulting in current saturation. When compared to emission changes due to oxygen, the emission current drop due to inert gas exposures is far more pronounced. To the first degree, we did not observe any noticeable effect of sputtering. Further, we found that a simple adsorption model is not adequate to explain the behavior. This is based on the fact that emission current recovery takes a long time. Ion implantation, not just adsorption, is proposed as the key factor in current degradation of emitters during inert gas exposure. The observed results are consistent with implantation and slow out-diffusion of the implanted gases. This is supported by the following observations: emission current degradation occurs only when the device is operating, recovery is faster for the heavier gases, and the current recovery appears to follow a diffusion type behavior. Further support comes from the fact that package pressure inside sealed displays was found to drop rapidly during device operation, thus indicating ion pumping type behavior. All of these observations are consistent with an implantation model driven by creation of ions from electron interaction with ambient gas.

11:00 AM *D15.3
THE GYRICON DISPLAY AND ELECTRONIC REUSEABLE PAPER.
Nicholas Sheridon, Xerox PARC, Palo Alto, CA.

(ABSTRACT NOT AVAILABLE)

11:30 AM D15.4
DEVELOPMENT OF POROUS SILICON FIELD EMISSION CATHODES COATED BY ULTRATHIN DLC FILMS.
Anatoli A. Evtukh, Volodimir G. Litovchenko, Yurii M. Litvin, Dmitrii V. Fedin, Yurii V. Rassamakin, Adrei V. Sarikov, Institute of Semiconductor Physics, Kiev, UKRAINE; Andrei G. Chakhovskoi, ECE Department, University of California, Davis, CA; Thomas E. Felter, Lawrence Livermore National Laboratory, Livermore, CA.

The main requirements to electron field emission cathodes are their efficiency, stability and uniformity. In this work we combined the properties of porous silicon layers and DLC (diamond like carbon) films to obtain field emission cathode with improved parameters. The layered structures consisting of porous silicon and DLC film were formed as phase n-Si surface and silicon tips created with chemical etching. The conditions of the anodic and stain etching of silicon in HF-containing solution under illumination have been changed widely. The investigation of the influence of thin ($\leq$ 10nm) DLC film overcoating porous silicon layer on electron emission have been performed. The parameters of emission efficiency such as field enhancement coefficients, effective emission areas and threshold voltages have been estimated from current-voltage dependencies to compare and characterize different layer structures. The improvement of the emission efficiency of silicon tip arrays with porous layers coated by thin DLC film have been observed. These silicon base structures are promising for flat panel display applications. The experimental results show that porous silicon exhibits substantial decrease of V_{th} (above 1.5-2 times), increase of effective emission areas (about 2-4 orders of magnitude with respect to 10^{-14} -10^{-12} cm^2 for crystalline Si tip). The main result after deposition of DLC is a substantial decrease of the work function (from 4 eV to 2 eV).

11:45 AM D15.5
FIELD EMISSION FROM NOVEL ROOM TEMPERATURE GROWN CARBON BASED MULTILAYERED CATHODES.
B.S. Satyanarayana, K. Nishimura[a] and A. Hiraki, KUT Academic & Industrial Collaboration Centre, Kochi University of Technology, Kochi, JAPAN; [a]Kochi Prefectural Industrial Tech. Centre, Kochi, JAPAN.

There is an increasing interest in carbon based nanostructured materials like the nano-diamond, nanotubes and nanocluster or nanostructured carbon for possible use as electron emitters. The interest stems from the feasibility of diverse applications, which include field emission displays, electron-beam lithography, electron and ion guns, sensors, electron microscopes and microprobes, low & medium power microwave sources and Tera hz communication devices. The need is for electron emitters capable of emitting high emission currents at low fields accompanied by a high emission site density. Most materials mentioned above are grown at high temperatures, which makes scaling of the process, for large area or deposition on low cost substrates very difficult. Reported here is a study on, a room temperature process grown carbon based multilayered cold cathode. The cathode consists of a layer of nanodiamond and an over coat of nanocluster carbon. The nano- diamond with varying diamond concentrations and sizes was coated on to the substrate by a pretreatment of the substrates using pure nanocrystalline diamond particles suspended in a colloidol solution. The nanocluster carbon films were then deposited at room temperature on the nanoseeded diamond deposited substrates using the cathodic arc process. Some of the hetrostructured microcathodes were observed to exhibit very low field electron emission (1mA/cm^2 emission current at 1.5-2 V/μm applied field). The emission behaviour was observed to be dependent on the nanoseeded diamond size and concentration for a given optimised nanocluster carbon film composition. Also discussed is the mechanism of emission from these films.

SESSION D16: NANO TECHNOLOGY FOR FED

Chair: Capp A. Spindt
Friday Afternoon, April 20, 2001
Franciscan I (Argent)

1:30 PM *D16.1
CANDESCENT'S HIGH VOLTAGE FIELD EMISSION DISPLAY DESIGN. Chris Curtin, Candescent Technologies, San Jose, CA.

The latest status of Candescents Field Emission display which incorporates P22 phosphors operated at 8 kV and Mo cold-cathode field emitters which are addressed with low voltage CMOS IC drivers will be described. Operation at a faceplate potential of 8 kV is possible due to the use of high aspect ratio ceramic support walls which span the 1.27 mm gap between the 1.1 mm thick glass substrates and maintain the parallel field lines between the two substrates. Maintenance of parallel field lines by linearly distributing the potential along the ceramic surfaces is achieved by a resistive material formulation and special coatings to avoid surface charging. The use of the standard color CRT P22 phosphors ensures the standard color coordinates are achieved as well as high efficacy. Like the industry standard color CRT, the FED phosphor screen is coated with a thin aluminum layer to effectively double the light output. Low voltage addressing is achieved by construction of sub-micron metal tips, centered in 0.12 micron gate holes. The 0.12 micron holes are fabricated by ion bombardment of a thin resist film deposited on the top of the second metal in a thin film metal-insulator-metal stack. Each high-energy ion results in a track through the resist film that has a substantially higher etch rate in a subsequent development step. The etched hole in the resist film is used to etch a hole in the second thin film metal, which then forms an etch mask for the insulator layer. After completion of these etching steps, the Mo metal emitters are formed by evaporation through the small holes in the second metal film.

2:00 PM D16.2
FIELD EMISSION CHARACTERISTIC OF SILICON CATHODES COATED WITH GaN NANO-PARTICLES. M. Hajra, N.N. Chubun, A.G. Chakhovskoi, C.E. Hunt, Electrical and Computer Engineering Dept. University of California, Davis, CA; V. Zhirnov, Semiconductor Research Corp, Durham, NC; S.H. Risbud, Chemical Engineering and Materials Science Dept., University of California, Davis, CA.

Nanocrystalline nitride materials exhibit novel properties when their dimensions are small enough to reveal quantum confinement effects (quantum dots). Recently, nanocrystalline GaN clusters were successfully synthesized using reactive laser ablation of gallium metal in a nitrogenating ambient. The method uses a pulsed Nd: YAG (266 nm) laser beam focused on the target through UV grade quartz windows. Products of the synthesis are deposited by dielectrophoresis on ungated field emission arrays consisting of n-type silicon and polysilicon micro-emitters formed using a subtractive tip fabrication technique. As a result, hexagonal GaN crystallites as small as 2nm diameter coat these emitters. Coating of the silicon emitter surface can improve the field emission performance of the cathodes approaching that created a negative electron affinity surface at the point of greatest electron supply and greatest tunneling field. The tips were evaluated using I-V measurements in the diode configuration. A flat Si anode, spaced nominally 1micrometer from the cathode, was used. The field emission characteristics are measured in a high vacuum chamber at a pressure of 10^{-8} Torr. The result suggests that there is a noticeable reduction in the operating voltage of the emission surfaces and a significant stabilization of the emission current.

2:15 PM D16.3
FABRICATION AND CHARACTERIZATION OF LOW TURN-ON VOLTAGE CARBON NANOTUBE FIELD EMISSION TRIODE. K.J. Chen, H.C. Cheng, F.G. Tantair, W.K. Hong, J.B. Lin, Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, Hsinchu, TAIWAN; K.H. Chen, Institute of Atomic and Molecular Sciences, Academia Sinica, Taipei, TAIWAN; L.C. Chen, Center for Condensed Matter Sciences, National Taiwan University, Taipei, TAIWAN.

A self-aligned, low turn-on voltage carbon nanotube field emission triode is proposed and the experimental results is reported. Based on the selective growth technique, the carbon nanotube was selectively deposited within the self-aligned emitter area by the microwave plasma enhanced chemical vapor deposition system. The fabricated device contains 4x4 emitting triode cells and each individual cell is 4um in diameter. With the phosphor coated ITO glass as the anode positioned 1mm above, the fabricated device was measured in a high vacuum chamber. The low turn-on gate voltage of 33V and the extremely high emission current density of 0.7A/cm^2 was achieved as the gate bias reached 50V. These results demonstrate a bright future of carbon nanotube for its potential application in field emission display.

2:30 PM *D16.4
SURFACES IN PHOSPHORS FOR FLAT PANEL DISPLAYS. Paul Holloway, Billie Abrams, Lizandra Williams, and Joe Thomes, Dept. of MS&E, University of Florida, Gainesville, FL.

The surface (or interface) of a phosphor may vary from the interior in a number of important ways, including morphology, composition, and/or structure. Each variation may affect luminescence in a variety of ways. For example surface morphology clearly affects light emission and scattering at surfaces and interfaces. Composition of the surface may be different from the interior due to thermodynamically driven segregation that may lead to concentration quenching and/or shifts in the color coordinates, as well as decreased efficiency. Surface compositional changes may also be induced over the lifetime of cathodoluminescence phosphors by outgassing and by electron-stimulated surface chemical reactions (ESSCRs) which degrade performance. Recognition of ESSCRs has led to intensive studies of phosphor surface composition changes by design through coatings. In addition to composition and morphology, the properties of phosphors may result from changes in the atomic structure at the surface or interface. These structural changes generally result in new quantum mechanical electron states that may be beneficial or detrimental. Charged interface states may bend the conduction and valence bands which may control brightness and efficiency though their effects on nonradiative vs. radiative carrier recombination, carrier diffusion and separation, and phosphor charging. These and other aspects of the influences of phosphors surfaces upon their performance will be discussed.

SESSION D17: MATERIALS AND DEVICES FOR FLAT PANEL DISPLAYS

Chair: Thomas E. Felter
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Franciscan I (Argent)

3:15 PM D17.1
SYNTHESIS and LUMINESCENT PROPERTIES of GaN and GaN-Mn BLUE NANOCRYSTALLINE THIN-FILM PHOSPHOR for FED. V. Bondar, Lviv National University, Department of Physics, Lviv, UKRAINE; T. Felter, Lawrence Livermore National Laboratory, Livermore, CA; C. Hunt, I. Kukharsky, A. Chakhovskoi, University of California at Davis, Department of Electrical and Computer Engineering, Davis, CA.

Nanocrystalline GaN luminescent thin films have been synthesized using rf-magnetron sputtering. The nanocrystallite size grows exponentially from 10nm to 40nm with increasing substrate temperature for deposition at 450 to 600K. GaN films show blue cathodoluminescence with a maximum at 450nm. The correlation between luminescence intensity and the density of shallow level donors has been found. The shallow level donors are nitrogen vacancies and determine the conductivity of the GaN films. The luminescence intensity increases with increasing conductivity. This correlation is in agreement with the donor-acceptor nature of the luminescence center. Evidently, the luminescence center is the donor-acceptor pair

consisting of shallow-level donors and deep-level acceptors. The deep acceptors are probably related to magnesium or zinc type dopants. The proposed model is in agreement with literature data obtained on optically-detected magnetic resonance in GaN:Mg crystals which show that shallow-level donors are included in centers responsible for blue luminescence in GaN:Mg. When doping gallium nitride with manganese, the increase in blue emission is observed together with the emergence of red emission. The most probable mechanism to explain this finding is indirect activation where manganese stimulates creation of donor-acceptor pairs consisting of intrinsic defects responsible for the blue emission. Based on ESR spectra it was found that the manganese dopant is introduced during growth of GaN films in the form of Mn_2 ions both into low-symmetry (resonant lines with geff=6 and geff=4.3) and high-symmetry (resonant line with geff=2.0) positions of the crystal lattice. The results may be explained in terms of a non-homogenous distribution of crystal field parameters for Mn_2 emission centers in the GaN structure. Therefore, it is possible that red luminescence of GaN films is caused by intracenter transitions in manganese ions.

3:30 PM *D17.2
MICROENCAPSULATED ELECTROPHORETIC DISPLAYS FOR LARGE AREA DISPLAY APPLICATIONS. Paul Drzaic, E Ink Corporation, Cambridge, MA.

I will describe recent progress in the development of microencapsulated electrophoretic ("electronic ink") display materials and devices. Electronic ink has several attributes which make it attractive for display applications, including scalability to large sizes, extremely low power, compatibility with film substrates, and excellent optical appearance over wide viewing angles. While large area direct drive signs are currently being manufactured, we are also developing additional means of addressing displays, including the use of active matrix arrays. The status of these developments, and future outlook, will be discussed.

4:00 PM D17.3
THE SLURRY-BASED 3-DIMENSIONAL PRINTING PROCESS (3DP TM) FOR THE PRODUCTION OF LARGE AREA PLASMA DISPLAYS. Richard K. Holman, Yawen Li, Hong-Ren Wang, Michael J. Cima, MIT, Dept of Materials Science and Engineering, Cambridge, MA; Emanuel Sachs, MIT, Dept of Mechanical Engineering, Cambridge, MA; Yasushi Enokido, Hiroyasu Tsuchiya, TDK Corporation, JAPAN.

The plasma display panel (PDP) is one of the foremost emerging technologies for large area displays. The key structural feature of the PDP display is the glass parallel rib structure, which contains the phosphor material and gas mixture. A number of techniques are currently utilized to produce this rib structure, e.g. screen printing and sandblasting. While geometrically simple, the scale and aspect ratio of the rib structure present major challenges, particularly in terms of yield. For example, in home display devices the ribs must be of the order of 50 microns by 50 microns by a meter or more, spaced only 50 microns apart. The slurry-based 3-Dimensional Printing process (3DP) may represent a viable, high yield alternative to current manufacturing techniques. Slurry-based 3DP is a solid freeform fabrication (SFF) technique developed at MIT capable of mass production of fine ceramic components with extremely complex geometries and fired densities in excess of 99% of theoretical density. The key challenge to producing SiO_2 glass or glass-ceramic PDP's by 3DP is achieving the 50 micron or smaller feature size necessary to compete with existing technologies. Initial prototypes in a model material system (alumina) feature rib widths of $\sim$300 microns, which is inadequate for all but the largest displays. Thus the goal of this research is twofold: to identify factors controlling minimum feature size in 3DP, and then to apply this knowledge to the production of large area PDP's. Key aspects of the process that were examined include the mechanical aspects of binder deposition (printing), including impact phenomena and deposition style, and chemical aspects such as binder adsorption and wetting/spreading. An entirely new method of binder deposition was examined, which could hold the key to producing PDP ribs of the size required to make 3DP a viable and attractive alternative to other manufacturing techniques.

4:15 PM D17.4
STUDY ON NANO-CRYSTALLINE SILICON FILM FIELD-EMISSION PRESSURE SENSOR. Bo Liao, Jie Zhang, Xiaoning Liu, Department of Electronic Engineering, Beijing Institute of Technology, Beijing, CHINA.

In this paper, a kind of body silicon MEMS field-emission pressure sensor based on the mechanism of quantum tunnel effect was fabricated, and also the semiconductor nano-technology was effectively introduced into the microelectro-mechanical systems which combined the microelectronic with the silicon micro-mechanical process technique to realize the unity of the three. The specific sensor was simulated by the computer. Via the ANSYS software, through the finite-element method, the mechanical characteristics of the sensor was analysed.