SYMPOSIUM I

Wafer Bonding and Thinning Techniques for Materials Integration

April 16 – 18, 2001

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TUTORIAL

ST I: WAFER BONDING AND THINNING TECHNIQUES FOR MATERIAL INTEGRATION
Monday, April 16, 2001
1:00 p.m. - 5:00 p.m.
Salon 1/2 (Marriott)

Wafer bonding has increasingly become a technology of choice for materials integration in microelectronics, optoelectronics and microelectromechanical systems (MEMS). This tutorial will bring together the latest information on wafer bonding, and describe the status of the technology, major accomplishments, challenges and opportunities for future research and applications. We will cover a range of materials including silicon, III-V compounds and oxides as well as specialized topics such as low-temperature bonding, thinning processes based on hydrogen-induced layer splitting, and the potential use of wafer bonding for surface protection. The tutorial will also include some discussion on controversial subjects such as "universal compliant substrates".

The tutorial covers the following topics :

- Introduction to wafer bonding and a brief history of the
- Cleaning
- Bonding requirements and procedures
- Examination of bonding
- Silicon direct bonding & Silicon-on-insulator
- Direct bonding of non-silicon materials; III-V compounds, SiC, Oxides and thin films
- Low temperature bonding
- Bonding via interlayers
- Thinning techniques
- Electronic properties of bonded
- Examples of applications and novel devices
- Outlook

Instructor:
Marin Alexe, Max Planck Institute for Microstructure Physics

SESSION I1: WAFER BONDING HISTORY AND PROSPECTS
Chair: Ulrich M. Goesele
Tuesday Morning, April 17, 2001
Golden Gate C1 (Marriott)

8:30 AM *I1.1
DIRECT BONDING IN A HISTORICAL CONTEXT OF MATERIALS AND TECHNOLOGY SCIENCE. Jan Haisma, Philips Research, Valkenswaard, NETHERLANDS.

Bonding in the most general sense, is almost as old as the history of technology of which cold welding and fusion-bonding are vivid examples. Direct bonding, however, is a more recent, advanced bonding technology at ambient circumstances of two solid elements which have to be as to their surface state, sufficiently flat (ore enantiomorphic), smooth and clean, so that contact once brought about, spontaneously results in a dynamic bonding process, electrically driven by Van der Waals forces. Direct bonding, strengthened by annealing, is basically equivalent to fusion bonding. UHV bonding at room temperature, in this context, is a specialty of the highest physical order.
Sir Isaac Newton has been the first to 'see' a direct bond in the black spot between a flat and convex body in 'optical contact'. The history of direct bonding will be presented interwoven in the history of materials science, bonding technology, optics and physics. Direct bonding as a phenomenon will be described and high-lights from earlier and recent times elucidated. Its physical background will be a guideline.

9:00 AM *I1.2
INTEGRATION OF MATERIALS AND DEVICE RESEARCH ENABLED BY WAFER BONDING AND LAYER TRANSFER. Q.-Y. Tong, Wafer Bonding Lab. Research Triangle Institute, RTP, NC and Ziptronix, RTP, NC.

Wafer bonding and layer transfer technology has emerged as a versatile approach for integrated research and development of materials and devices. It does not only provide a flexible way to prepare integrated materials but also breaks the barrier between materials science and device engineering since it appears to be one of the fundamental technologies for 3-D device fabrication and for integration of partially or fully processed functional layers. The device performance can be significantly enhanced when both sides of device layers can be processed such as in the double gate CMOS and in HBTs. The processed device layers can be considered as unique materials layers and can also be integrated. The integration of integrated circuits of different types provides a promising solution to realize micro-systems or SOC (system on a chip) products. Two of the main challenges are to develop methods that form strong bond between required materials at low temperatures and to cut the device layer without compromising the device integrity. The advances in low temperature bonding of hydrophilic and hydrophobic silicon, compound semiconductors and other materials in ambient and in UHV are reviewed, and application examples are discussed.

9:30 AM *I1.3
WAFER BONDING AND ITS IMPACT ON DEVICES FOR OPTICAL COMMUNICATIONS. P. Daniel Dapkus, Zhi Jian Wei, Kostadin Djordjev, Yuanming Deng, Ryan Stevenson, Thiruvikraman Sadagopan and J.D. O'Brien, The Photonics Center, University of Southern California, Los Angeles, CA.

Wafer fusion or bonding is rapidly becoming an important tool for optical device fabrication. The ability to integrate different materials onto a common substrate and the ability to process both sides of a thin film structure using this process provides new degrees of freedom in the design of lasers, detectors, and wavelength division multiplexing devices and circuits. In this talk we will review the successes that have been achieved in the use of wafer bonding to fabricate long wavelength VCSELs, bottom emitting VCSEL arrays, heterojunction detectors, and photonic integrated circuit components. Detailed discussion of the fabrication of large VCSEL and detector arrays fabricated by wafer bonding GaAs based optoelectronic devices to sapphire for application free space communications systems will be given. We will also discuss the use of wafer bonding to the fabrication of vertically coupled microresonator devices for application to integrated wavelength multiplexers, demultiplexers, lasers and wavelength selective detectors. This application utilizes the ability to process two sides of an epitaxial wafer by transferring the film from the growth substrate to a carrier substrate. This approach enables one to utilize stacked waveguide epitaxial structures to form complex three dimension device and optical circuit structures. Included in the discussions will be studies of interface characteristics, thermal expansion mismatch process parameters to insure uniformity, electrical conductivity and mechanical stability and device performance.

SESSION I2: PHYSICS AND CHEMISTRY OF WAFER BONDING
Chair: Tony E. Haynes
Tuesday Morning, April 17, 2001
Golden Gate C1 (Marriott)

10:30 AM *I2.1
INTERFACIAL CHEMISTRY IN DIRECT WAFER BONDING. Yves J. Chabal, Marcus K. Weldon, Lucent Technologies, Bell Labs, Murray Hill, NJ.

Direct wafer bonding presents an interesting alternative to epitaxy for materials integration. When coupled with film exfoliation techniques such as SmartCut, it allows the "deposition" of a variety of thin crystalline films on a host of substrates. For applications when the quality of the interface is important (e.g. electronic transport), understanding the chemical evolution of the interface during the thermal bonding process becomes critical. We discuss here the experimental techniques used to study the chemical evolution of bonded interfaces, focusing mostly on direct Si/Si wafer bonding. We show how infrared absorption spectroscopy gives detailed information on ubiquitous species at hydrophobic or hydrophilic interfaces, such as hydrogen, water, hydroxyl and oxides. From such studies, a mechanistic picture of the process leading to the formation of chemical bonds between the two wafers can be inferred, including the appearance of bubbles or microvoids at specific stages of the process. This understanding makes it possible to refine the process parameters and constitutes a basis for unraveling direct bonding of dissimilar materials.

11:00 AM I2.2
PLASMA INDUCED CHEMICAL CHANGES AT SILICA SURFACES DURING PRE-BONDING TREATMENTS.
D.M. Hansen, C.E. Albaugh, P.D. Moran, and T.F. Kuech, Department of Chemical Engineering, University of Wisconsin-Madison, Madison, WI.

Plasma-treated and DI H_2O rinsed oxide layers are commonly used in wafer bonding applications. Borosilicate glass (BSG) layers deposited by low-pressure chemical vapor deposition (LPCVD) treated with an O_2 plasma in reactive ion etching (RIE) mode at 0.6 W/cm^2 and rinsed with DI H_2O readily bond to GaAs and Si. The chemical role of this pre-bonding treatment was investigated using attenuated total reflection Fourier transform infrared (ATR-FTIR) spectroscopy. The peak intensities for both the Si-O and B-O absorbance bands decreased in intensity as a result the plasma treatment consistent with the uniform sputter etching of BSG. The effect of changing the total plasma treatment time was investigated in terms of the total amount of material removed. Polarization dependent ATR-FTIR revealed that the H_2O/OH absorbance bands decreased in peak intensity with the OH groups preferentially oriented perpendicular to the sample surface after the plasma treatment. The subsequent DI H_2O rinse restores the water to the surface while changing the surface BSG composition. ATR-FTIR studies suggest that for oxide compositions greater than 10 mole % B_2O_3, the top 4 nm of B_2O_3 was removed or leached from the oxide layer during the DI H_2O rinse.

11:15 AM *I2.3
MOLECULAR DYNAMICS SIMULATIONS OF WAFER BONDING.
Kurt Scheerschmidt, Max Planck Institute of Microstructure Physics, Halle, GERMANY.

Molecular dynamics (MD) simulations using suitably fitted empirical potentials have been employed to describe atomic interactions at interfaces controlling the macroscopic wafer bonding process initiated by the adhesion of two surfaces /1/. The MD ensemble (NpT or NVE) is coupled elastically to the surrounding bulk wafers, and the energy dissipation is controlled by the transfer rates of the kinetic energy at the borders. The comparison of the relaxed interface structures with experiments is possible by using simulated electron microscope images on the basis of the MD models and by analysing dynamical properties (pair and velocity correlations, vibration spectra, etc.). Calculated bonding energies and forces strongly depend on the surface termination, native oxides, adsorbates, and the process control, as shown by MD simulations of hydrogen on hydrophobic Si /2/, by water-silanol reactions on silica surfaces /3/ describing hydrophilic termination, and by studying surface reconstructions and the bondability of SiC(0001) /4/. Fast heat transfer, twisted starting configuration, the presence of steps or the including of small rotational misorientations, result in special interface configurations mostly no longer perfectly coordinated (cf. e.g. /5/). Simulations based on potentials derived from the bond order expansion (second moment tight-binding approximation) lead to an enhancement of the physical reliability of the method and to the predictability of the bonding behaviour of a wide variety of materials (e.g. diamond /7/).
/1/ K. Scheerschmidt, D. Conrad, A. Belov, and D. Timpel, Mater. Sci. Semic. Process. 3 (2000) 129. - /2/ D. Conrad, K. Scheerschmidt, and U. Goesele, Appl. Phys. Lett. 71 (1997) 2307. - /3/ D. Timpel, M. Schaible, and K. Scheerschmidt, J. Appl. Phys. 85 (1999) 2627. - /4/ Ch. Koitzsch, D. Conrad, K. Scheerschmidt, and U. Goesele, J. Appl. Phys. (2000), in print. - /5/ A. Yu. Belov and K. Scheerschmidt, Philos. Mag. Lett. 79 (1999) 107. - /6/ D. Conrad, K. Scheerschmidt, and U. Goesele, Appl. Phys. Lett. 77 (2000) 49.

11:45 AM I2.4
WAFER BONDING OF SILICON CARBIDE AND GALLIUM NITRIDE.
Jaeseob Lee, T. Cook, J.D. Hartman, R.F. Davis, North Carolina State Univ, Dept of MS&E, NC; E. Bryan, R.J. Nemanich, North Carolina State Univ, Dept of Physics, Raleigh, NC.

The development of heterojunctions between different wide bandgap semiconductors may provide opportunities for new high power devices. For instance, a GaN-SiC interface could prove important for development of a compact high power heterojunction bipolar transistor. The growth of GaN directly onto SiC requires a buffer layer which severely limits the electrical properties of the interface. As an alternative approach, we are exploring the formation of a GaN-SiC heterojunction interface through wafer bonding. The GaN materials were prepared by CVD growth onto 50mm diameter SiC. A similar $(0001)_{Si}$ 6H- SiC wafer was used for the bonding pair. Both SiC wafers were n-type as was the GaN layer. The wafer surfaces were characterized with AFM and auger electron spectroscopy. Prior to bonding the wafers were diced into 10mm x 10mm sections. Various wet chemical treatments were employed to prepare the surfaces for bonding. In some instances, spontaneous bonding was observed at room temperature. The spontaneous bonded wafers survived heating to 300°C, but the bonding extended over a small fraction of the surface. To obtain a stronger bond, the wafers were bonded in a UHV system equipped with a central post to initiate bonding and sample heating to > 900°C. Several different heating processes were explored. A mechanically strong bond was obtained through a UHV cyclic annealing treatment of 5 anneals at 890°C for 30 min each. Visible inspection of the bonded couple showed uniform bonding over the whole surface and the couple could not be separated. Both back sides of the SiC wafers were metallized with Ti and the electrical properties indicated ohmic behavior which is consistent with expectations for bonding of n-type samples.

SESSION I3: ION IMPLANTATION FOR LAYER TRANSFER

Chair: Michael Nastasi
Tuesday Afternoon, April 17, 2001
Golden Gate C1 (Marriott)

1:30 PM *I3.1
A REVIEW OF NEW HETEROSTRUCTURES OBTAINED WITH SMART-CUT^{TM} TECHNOLOGY.
B. Aspar, C. Lagahe, H. Moriceau, A. Soubie, E. Jalaguier, B. Biasse, CEA/LETI, Departement de Microtechnologies, Grenoble, FRANCE; T. Barge, O. Rayssac, F. Letertre, SOITEC, Bernin, FRANCE.

The Smart-Cut^{TM} technology is based on proton implantation and wafer bonding. Proton implantation induces formation of an in-depth weakened layer, located at the mean ion penetration depth, which leads to delamination of a thin film from a thick substrate. Wafer bonding and layer transfer enable different materials to be associated to form multi-layer substrates. This is particularly advantageous when a thin monocrystalline layer is required on a support which does not allow epitaxy of this layer. This process, first developed to obtain Silicon On Insulator (SOI) materials, is now an industrial process which provides high quality materials in large quantities. Moreover, this process is generic because a large number of material combinations can be achieved. Splitting was successfully performed in semi-conductors such as silicon, SiC, GaAs, InP, Ge but also in more complex material like $LiNbO_3$. The ability to obtain thin films by means of the Smart-Cut^{TM} process combined with specific bonding via insulating layers, thermally conductive or metallic layers has also been demonstrated. Complex structures can be elaborated by transferring several levels of thin layers onto a same substrate. Stack of SOI layers are thus obtained. This process is also compatible with patterned layers. Homogeneous thin film can be transferred on patterned support as well as patterned thin film on support. In conclusion, Smart-Cut^{TM} technology allows a great deal of combinations (material and bonding layer) which open up new scope for developments.

2:00 PM I3.2
TEM MEASUREMENTS OF HYDROGEN PRESSURE IN CAVITIES FORMED BY PROTON IMPLANTATION IN SILICON.
Jérémie Grisolia, G. Ben Assayag, A. Claverie, CEMES/CNRS, Toulouse, FRANCE; R.E. Kroon, J.H. Neethling, University of Port Elizabeth, Dept of Physics, SOUTH AFRICA; B. Aspar, C. Lagahe, LETI/CEA, Dept of Microtechnologies, Grenoble, FRANCE.

Recently, the combination of hydrogen implantation and wafer bonding has shown its interest to transfer thin films of various materials onto various handle wafers. Under specific experimental conditions, thermal treatment of hydrogen implanted wafer can lead to exfoliation of a thin top-layer from its substrate. In silicon, proton implantation can result in the formation of one specific type of extended defect involving hydrogen: 2D-cavities often named "platelets". We have recently established that, upon annealing, these platelets grow in size, reduce their density following an Ostwald ripening type mechanism. Under specific process conditions, these platelets can lead to the formation of microsplitting involving a crack propagation mechanism which will eventually induce the fracture of the wafer. For this reason, it is important to establish the link between platelet growth and stress accumulation in the layers. In this paper, we have used TEM and image simulation techniques to measure the strain field around such defects and thus to deduce the hydrogen pressure inside them. Having noted that the strain field around a platelet gives an image similar to that of a dislocation loop of extrinsic character, we have developed such an analogy and extracted an effective Burgers vector for the platelets through a best fit procedure between experimental and simulated images. This allows us to calculate the elastic energy stored in the platelets as a function of their size. Since any increment of this elastic energy is due to the work generated by a change in PdV, this pressure can be determined. Simulated values ranging from 14 to 10 GPa are found for typical platelet sizes varying from 6 to 9 nm in radius. From these results, a picture emerges in which stress-interactions between neighboring platelets, and not only their size increase via Ostwald Ripening, are involved in the later microsplitting.

2:15 PM I3.3
BLISTERING ON SILICON SURFACE CAUSED BY GETTERING OF HYDROGEN ON POST-IMPLANTATION DEFECTS.
Alex Usenko, William Carr, Silicon Wafer Technologies, Newark, NJ.

A known process of thinning of silicon by slicing submicron-thick crystalline films from substrates uses direct implantation of protons. Here is described a different way of delivering of hydrogen to a cleavage plane. A defect-rich buried layer is formed with implantation. Defects in the as-implanted silicon work as traps for hydrogen. Then monatomic hydrogen is delivered to the trap layer. Electrolytic charging is used to deliver hydrogen. To check a sliceability, the samples where annealed. Experiment shows blistering of silicon wafer surface. Evidence of blistering is a sign of possible cleavage. The electrolytic charging was performed in a simple two-electrode cell. Front side of as-implanted silicon wafer was exposed to an electrolyte. Back side of the wafer was contacted with aluminum layer and connected to a current source. The electrolyte was buffered hydrofluoric acid. Buffering was used to improve uniformity of charging. To increase charging current the wafer was illuminated with visible light. Graphite rod was used as a positive electrode in the cell. Hydrogen charging was performed at room temperature. Few Coulombs per square centimeter of the wafer were passed through the cell during the hydrogenation process. Depth of blisters is about 1/2 of projection range of the implanted ions. It means that the hydrogen platelets are formed at the maximum of vacancy-enriched post-implantation defects. The process of electrolytic hydrogen charging may be used in future to manufacture silicon-on-insulator wafers with very thin top silicon layer. The thin top layer SOI are advantageable substrates for mainstream CMOS integrated circuit manufacturing.

2:30 PM *I3.4
SLICING AND BONDING OF SINGLE-CRYSTAL FERRO-ELECTRIC AND MAGNETIC OXIDE FILMS.
M. Levy, Michigan Technological University, Dept of Physics, Houghton, MI; T. Izuhara, A. Radojevic, R.M. Osgood, Jr., Columbia University, Dept of Applied Physics, New York, NY; M. Reeves, George Washington University, Dept of Physics, Washington, DC; H. Bakhru, SUNY at Albany, Dept of Physics, Albany, NY.

Ferroelectric and magnetic oxides are of critical importance for the development of advanced photonic, microwave, and micromechanical devices. Of particular interest is the heterogeneous integration of single-crystal films of these materials onto various platforms for high performing "on-chip" applications. We report on an ion-implantation-based technique, crystal ion slicing, used to fabricate single-crystal oxide films. The films include highly efficient materials used in piezoelectric actuator applications (PZN-PT), electro-optic devices ($LiNbO_3$), optical isolators (yttrium iron garnets), and frequency-agile microwave tunable resonator devices ($KTaO_3$). Excellent performance, comparable to that of the original single-crystal bulk material, is achieved. To prepare the samples for crystal ion slicing, singly charged 3.8MeV helium ions are implanted normal to the surface without masking, at doses near 5 X 10^{16} ions/cm^2. The energy of the implantation can be adjusted to select film thickness. Helium is chosen as the implantation species because of its small atomic mass, thus yielding a damage-layer that is buried several microns beneath the surface. This sacrificial layer is subsequently etched away and the top film detached, allowing precise thickness control below 10 μm. Little radiation damage is generated in the film itself since the stopping power at high ionic energies is mostly electronic, while post-implant annealing is effective in eliminating residual damage. The films can be bonded onto a variety of substrates, crystalline or amorphous, semiconductor or glass. Bonding between yttrium iron garnet (YIG) films and various semiconductors is realized by direct wafer bonding. The control of shear stress at the garnet/semiconductor interface is important and can be achieved by temperature tuning during the bonding process. We also report on the anodic bonding of YIG films onto glass. An interfacial metallic layer is used in this case to enable and critically enhance the charge transfer mechanism during the bonding process.

SESSION I4: PROPERTIES OF MISMATCHED INTERFACES

Chair: Qing-Yi Tong
Tuesday Afternoon, April 17, 2001
Golden Gate C1 (Marriott)

3:30 PM *I4.1
ASSESSMENT OF WAFER BONDING AND THINNING TECHNIQUES FOR PRODUCING COMPLIANT SUBSTRATES.
K.D. Hobart, F.J. Kub, M.E. Twigg and M. Fatemi, Naval Research Laboratory, Washington, DC.

This talk will review recent advances in the fabrication of "compliant substrates" as well as the relative success such compliant substrates have had in improving material quality of heteroepitaxial films. Fabrication processes that utilize precision thin film transfer techniques such as Smart-Cut will be emphasized, although results based on conventional thin film transfer using bond-and-etch-back will also be compared. The author will provide details on a fabrication scheme that combines Smart-Cut and bond-and-etch-back processes that enables the production of bonded semiconductor films as thin as 1 nm as well as the use of this process for the fabrication compliant substrates. Finally, film relaxation processes on various compliant substrate structures will be compared and a perspective on the future direction of compliant substrate fabrication technology and applications will be provided.

4:00 PM I4.2
ATOMICALLY FLAT SILICON/GERMANIUM (100) INTERFACES: UHV BONDING.
M.J Cox, M.J. Kim and R.W. Carpenter, Science and Engineering of Materials, Center for Solid State Science, Arizona State University, Tempe, AZ.

Germanium (100) and silicon (100) wafers have been successfully bonded at both 450 and 750°C, to form structurally sharp interfaces. Prebonding surface preparation is critically important for formation of strong interfaces, in agreement with our results for previous bonding of other materials. Both flatness and substrate surface chemistry are important. In-situ Auger spectroscopy measurements of substrate composition are invaluable predictors of bonding behaviors. High-resolution electron microscopy showed that the bonded interfaces were essentially atomically flat. Lattice mismatch is accommodated at the outset by interface dislocations. The only strain observed at the interface resulted from differential contraction. Dislocation did not propagate away from the interfaces into the wafer interiors. This method of interface syntheses is an interesting and potentially useful alternative to Ge film deposition on Si, using surfactants and vicinal surfaces to try to reduce the effects of misfit strain and threading dislocations.

4:15 PM I4.3
SUBSURFACE DISLOCATIONS NETWORKS OBTAINED BY DIRECT WAFER BONDING: A WAY TO NANOSTRUCTURE SELF ORGANIZATION.
F. Fournel, N. Magnea, J. Eymery, K. Rousseau, J.L. Rouvière, H. Moriceau[a], B. Aspar[a], CEA/Grenoble, Département de Recherche Fondamentale and [a]LETI/Département de Microtechnologies, Grenoble Cedex, FRANCE.

New substrates for epitaxy with a nanometric surface patterning are elaborated by direct bonding of ultra thin films of silicon with Si wafers. Due to the disorientation of the two crystals, the direct bonding produces nanometric networks of dislocations strictly localized in the bonding interface. The periodic modulation of the surface potential resulting from the dislocations strain field can be used as a template for self organized epitaxy. On wafers bonded with a precisely chosen twist angles (ranging from 0° to 5°), HREM observations show the excellent cristallinity of the Si film down to thickness of 5 nm and confirm the presence of a quasi perfect network of dissociated screw dislocations. Grazing incidence X-Ray diffraction are used to measure the extension of strain field of the dislocations. STM images reveal the influence at the surface of the strain field, linked to the dislocations, which may open a new way for an epitaxial growth of self-organized quantum dots. To check the method, silicon nanocrystals have been deposited by LPCVD on these new substrates covered by a 1 nm thick oxide. The nanocrystals are self-organized in a pattern reproducing the symmetry of the buried dislocations array.

4:30 PM I4.4
ELECTRICAL CHARACTERISATION OF UHV-BONDED SILICON INTERFACES.
Alexander Reznicek, Stephan Senz, Otwin Breitenstein, Ulrich Gösele, Max-Planck-Institute of Microstructure Physics, Halle/Saale, GERMANY.

Direct wafer bonding can be used to produce artificial grain boundaries. In our experiments two 100 mm diameter (100) Si wafers (n-doping: 10^{14}) are first cleaned by standard chemical cleaning (RCA 1, 2). The surface is terminated by hydrogen after a HF dipping. The wafers are pre-bonded in air to protect the surface. After introduction into the UHV system the wafers are separated again. The hydrogen termination is released in a heating chamber. RHEED confirmed a surface reconstruction. The wafers are then cooled down to room temperature and bonded in UHV. The bonding energy is very close to the bulk bonding energy. Measurements of whole n-n wafers showed a linear relationship of voltage and current at low averaged current density of 0.05 A/cm^2. The current flow is inhomogeneous, which is visible in IR-thermography images. Above 0.1 V the current density first saturates, but increases super-linearly for higher voltages. The electrical properties of a grain boundary can be modelled by a double

Schottky-barrier. The barrier height decreases with increasing applied voltage. C-V measurements show a strong dependence of capacitance on frequency, temperature and applied voltage. The capacitance increases with higher temperature and lower frequency. The interface state density can be estimated from the low temperature and high frequency capacitance limit as $D_{it}=1\times 10^{11}$ $cm^{-2}eV^{-1}$ assuming a constant density of states. We can conclude that in order to avoid the undesireable effect of the potential barrier and trap states at the bonding interface a high doping near the interface is required for the application of wafer bonding to devices with a high current density across the bonded interface.

4:45 PM I4.5
OHMIC, METAL-FREE BONDING OF GERMANIUM FILM TRANSFERRED BY DIRECT WAFER BONDING TO SILICON. James M. Zahler, California Institute of Technology, Dept of Chemical Engineering, Pasadena, CA; Harry A. Atwater, Shahrooz Zaghi, California Institute of Technology, Dept of Applied Physics, Pasadena, CA; Charles Chu, Peter Iles, Tecstar Inc., City of Industry, CA.

Compound semiconductor heterostructures grown on bulk germanium substrates have been used to create high efficiency multi-junction solar cells with efficiencies greater than 30%. Film transfer of germanium onto silicon is being explored as a means of cost and weight reduction for these heterostructures. We have successfully used direct wafer bonding along with hydrogen-induced layer splitting of germanium to form an ohmic bond and transfer single crystal germanium(100) films to silicon(100) substrates without using a metallic bonding layer. Germanium wafers with $5x10^{16}cm^{-2}$ H_2^+ at 160keV were used to transfer ~600nm thick films of 0.5cm x 1.0cm area. The metal-free nature of the bond makes the bonded wafers suitable for subsequent epitaxial growth of the layered solar cells at high temperatures without concern about metal contamination of the device active region. Preliminary results indicate that hydrophobic surface passivation and less than 1nm rms roughness as measured by contact mode AFM are suitable surface conditions for reversible room temperature bonding to occur. Annealing at 160°C strengthens the bonding, and layer splitting is induced by a thermal cycle up to 470°C. The bond has been shown to be stable during thermal cycling from room temperature to 750°C. Contact mode AFM analysis of the transferred germanium surface generated by the formation of micro-bubbles and micro-cracks along the hydrogen-induced layer-splitting interface reveals a minimum rms surface roughness of 2.3nm. Preliminary electrical measuremsnts indicate ohmic I-V characteristics for germanium substrates bonded to silicon substrates, but with a high (~50Ω) resistance, which is probably limited by contact resistance. Further electrical characterization of the silicon-germanium interface by measurement of the current-voltage and capacitance-voltage characteristics of the bonded layers will be reported, along with TEM analysis of the silicon-germanium interface. Also, the suitability of the transferred germanium surface for subsequent GaAs growth by MOCVD will be discussed.

SESSION I5: POSTER SESSION
WAFER BONDING & THINNING

Chairs: Tony E. Haynes, Ulrich M. Goesele, Michael Nastasi and Takao Yonehara
Tuesday Evening, April 17, 2001
8:00 PM
Salon 1-7 (Marriott)

I5.1
ANODIC BONDING AT ROOM TEMPERATURE. Volker Baier, Institute for Physical High Technology, Micro Systems Division, Jena, GERMANY; Andreas Gebhardt, VITRON Spezialwerkstoffe GmbH, Jena, GERMANY; Stefan Barth, Hermsdorfer Institut für Technische Keramik e. V. (HITK), Magnetwerkstoffe, Hermsdorf, GERMANY.

For our anodic bonding experiments we used special phosphate glasses (niobium-phosphate glasses). They were optimized particularly with regard to elevated alkali ion conductivity at room temperature. The glasses were especially developed with high contents of Li- or Na-ions. The compounds anodically bonded at room temperature showed the strength of the breakage of the glass. Only a few seconds up to a few minutes at voltages of maximum 500 V are necessary for the bonding. The glasses have a thermal expansion coefficient which is not fitted to that of silicon. Therefore, general stability of the bonded compounds was achieved only at temperature jumps up to 100 K. For higher temperature jumps the probability of breakage increased continuously. It is possible to get thin films of these glasses with dc- and ac- magnetron sputter techniques for example on silicon. These thin layers are anodically bondable. Many applications are possible due to this low temperature bonding technique like encapsulation of probes with low boiling liquids (like water), biological probes, components which do not withstand higher temperatures, etc.

I5.2
Abstract Withdrawn.

I5.3
Si/GaAs HETEROSTRUCTURES FABRICATED BY DIRECT WAFER BONDING. Viorel Dragoi, Marin Alexe, Manfred Reiche, Ionut Radu, Max Planck Institute of Microstructure Physics, Halle, GERMANY; Eric Thallner, Christian Schaefer, Paul Lindner, Electronic Visions Group, Schaerding, AUSTRIA.

A high scientific interest is focused on the fabrication of Si/III-V compound semiconductor heterostructures for the integration of optoelectronic devices into Si integrated circuits technology. Different growth methods are currently applied to prepare III-V layers on silicon substrates (epitaxy, different CVD methods). Most of them result in a high defect density in the layers due to the 4% lattice mismatch and thermal stresses, reducing the efficiency of the devices. Semiconductor direct wafer bonding (DWB) can be an alternative technique for preparing heterogeneous substrates. The main problem for DWB is the thermal mismatch of the two materials: the thermal expansion coefficient (TEC) of GaAs is almost double than that of Si. For the direct bonding of GaAs and Si wafers (100 mm diameter) we obtained very low surface energies: about 10 mJ/m^2 for room temperature bonded wafers and 50 mJ/m^2 after annealing at 250°C. Annealing at higher temperatures leads to debonding of the wafers due to the thermal mismatch. In order to avoid this problem, different wafer bonding techniques can be applied: bonding in hydrogen atmosphere, plasma activation, patterning of the wafers prior to the bonding process or bonding via intermediate layers. A bonding approach using a glass intermediate layer was successfully applied for the GaAs/Si bonding. In this case, the surface energy obtained after bonding at room temperature was about 450 mJ/m^2 and increased to about 2 J/m^2 after annealing at only 200°C. Using this bonding procedure and a mechanical thinning procedure consisting in grinding followed by chemical mechanical polishing we transferred a 10 μm thick single crystalline GaAs layer on Si substrate. Heterostructures fabricated by this procedure can be heated to 450°C without damaging the bonded interface or the wafers involved. In this paper we report our new developments in fabrication of GaAs/Si heterostructures using different DWB methods.

I5.4
SIMULATIONS OF THE EFFECT OF MOISTURE ON INTERFACE FORMATION AND BONDING BETWEEN SILICA AND OXYNITRIDE SURFACES. Stephen H. Garofalini and Frances C. Hill, Department of Ceramic and Materials Engineering, Rutgers University, Piscataway, NJ.

Molecular dynamics computer simulations have been used to study the interactions occurring during interface formation relevant to wafer bonding in the presence of moisture. The role of water between the surfaces on interface behavior will be presented. Simulations show the dual effects of water between surfaces on bonding behavior; specifically, a beneficial effect of enhancing hydrogen bonding between surfaces followed by a deleterious effect if water is trapped between the bonding surfaces. This trapped water can affect subsequent bonding behavior and, experimentally, high temperature anneals are required to remove water from between surfaces in order to achieve strong bonding.

I5.5
EFFECTS OF WAFER CLEANING AND HEAT TREATMENT IN GLASS/SILICON WAFER DIRECT BONDING. Hong-Seok Min, Young-Chang Joo, Seoul National University, School of MS&E, Seoul, KOREA; Oh-Sung Song, University of Seoul, Department of MS&E, Seoul, KOREA.

Optimizing the conditions of wafer cleaning and heat treatment are important in wafer direct bonding of dissimilar materials such as glass/Si and GaAs/Si. We have investigated these effects in glass/Si bonding using 4-inch Pyrex glass wafers and 4-inch silicon wafers. Various wafer cleaning methods were examined; SPM (H_2SO_4:H_2O_2=4:1, 120°C), RCA (NH_4OH:H_2O_2:H_2O=1:1:5, 80°C), and combinations of those. The best room temperature bonding result was achieved when wafers were cleaned SPM followed by RCA cleaning. The minimum increase in surface roughness measured by AFM (atomic force microscope) confirmed such results. During successive heat treatments, the bonding strength was improved with increased annealing temperatures up to 400°C, but debonding was observed at 450°C. The difference in thermal expansion coefficients between glass and Si wafer led debonding. When annealed at fixed temperatures (300 and 400°C), bonding strength was enhanced until 28 hours, but then decreased for further anneal. To find the cause of decrease in bonding strength in excessively long annealing time, the ion distribution at Si surface was investigated using SIMS (secondary ion mass spectrometry). Ions such as sodium, which had been existed

only in glass before annealing, were found at Si surface for long annealed samples. Decrease in bonding strength can be caused by the diffused sodium ions to pass the glass/Si interface. Therefore, maximum bonding strength can be achieved when the cleaning procedure and the ion concentrations at interface are optimized in glass/Si wafer direct bonding.

I5.6
SiC-Si GROOVED SURFACE BONDING. Konstantin Kostine, Dept of Mat. Science, Kiel Univ, GERMANY; Tatiana Argunova, Igor Grekhov, Ludmila Kostina, Dept of Sol. St. El. Ioffe Phys.-Techn. Inst, Andrei Tur'yanskii, Ivan Pirshin, Dept of Sol. St. of Lebedev Phys. Inst, Il'ya Prudnikov, Dept of Phys, Moscow State Univ., RUSSIA.

It is known that the technology of silicon carbide epitaxial layer transfer onto oxidized silicon substrates by wafer bonding, though successive as a whole, appeared to be shortcomings due to roughness of silicon carbide surface. The purpose of the present paper is to demonstrate a way by which the influence of the surface roughness can be sufficiently reduced. Silicon carbide wafers, both Lely crystals and CVD layers, were directly bonded to silicon wafers with an artificial grooved surface relief of mesoscopic depth. Silicon carbide wafers were hydrogen etched. The bonding was realized at elevated temperatures. The continuity of the interface was studied by X-ray diffraction topography. Fracture strength was assessed by cutting of the samples. Orthogonal relief was made on silicon wafer by a photolithography technique. The groove spacing was taken to provide a high probability for a maximum height roughness to coincide with a groove. RMS and lateral coherence length values of silicon carbide surfaces were determined from X-ray scattering diagrams and AFM data. The extraction of the contributions caused by curvature and surface roughness gave an opportunity to compare the calculated RMS and the lateral coherence length values for two wavelengths. Different models were used for the simulation of the profiles. The results showed an easier smooth-to-grooved surface bonding accomplished by the formation or the boundary with better continuity and strength. The obtained data was explained due to an elastically compliant character of grooved surface wafers.

I5.7
DIRECT BONDING OF SILICON WAFERS WITH SIMULTANEOUS DOPANT DIFFUSION. Konstantin Kostine, Dept of Material Science, Techn. Fac. Chr. Albr. University of Kiel, GERMANY; Igor Grekhov, Tatiana Argunova, Ludmila Kostina, Natalia Shmidt, Solid State Electronics Division, A.F.Ioffe Physico-Technical Institute RAS, St. Petersburg, RUSSIA.

Direct bonding technology is used, as a rule, to bond to desired substrates semiconductor wafers which are bulk as well as partially or fully processed (containing pn-junctions or surface oxides). However, the impurity introduction before bonding often results in deteriorating the wafer surface quality as well as in arising the elastic strains, which may violate the bonding procedure requirements and even make it impossible. In this paper the formation of p- or n-type conductivity layers in silicon wafers is proposed to be performed directly in the course of direct bonding procedure. In our experiments it was tried via an initial attachment of 60 mm in diameter mirrow polished silicon wafers in the aqueous solutions of aluminum and gallium nitrates as well as of phosphorous and boron acids with the subsequent annealing at elevated temperatures. A mesoscopic relief as an orthogonal net of grooves was made on one wafer from each pair before bonding to decrease the influence of surface morphology on interface structural quality. Measurement of diffusion profiles as well as of diode structure current-voltage characteristics, X-ray diffraction topography and SEM techniques were attracted for the evaluation of sutability of developed technology and for the comparison of obtained results. The wafer curvature radius before and after bonding was measured by X-ray diffractometry. In particular, measurement of aluminum diffusion profile between n-type wafers confirms the possibility of aluminum diffusion into the polished silicon surface in the oxidized environment from the source chemically deposited at the bonding interface. An essential improvement of bonding interface continuity was revealed in the bonded compositions fabricated using aluminum nitrate solution instead of clean DI water. Comparative histograms of percent of bonded area were built. A model is suggested which explains the observed fact by the increase of the bonding area at the initial bonding stage due to aluminum-hydroxyl group built-in between water molecules adsorbed by contacted wafer surfaces. Impurity diffusion during high temperature treatment results in the formation of pn-junction rather far from interfacial region. It means that diode current-voltage characteristic is not so much influenced by the bonding interface quality and should look like a typical one for the conventional diffusion pn-junction, which was also confirmed in our experiments.

I5.8
Transferred to I4.2

I5.9
RE-DISTRIBUTION OF HYDROGEN DURING LOW TEMPERATURE ANNEALING OF H-IMPLANTED Si. C. Miclaus, M.S. Goorsky, Y.M. Kim, and Y.H. Xie, University of California-Los Angeles, Department of Materials Science and Engineering, Los Angeles, CA.

The structural changes that accommodate wafer splitting after hydrogen implantation of silicon wafers and the transfer of split layers to a handle substrate were investigated as a function of low annealing temperatures. Most previous work on the changes that occur to hydrogen implanted layers have focused on higher temperature ranges ($\geq$450°C); the distribution of hydrogen during low temperatures (100 - 300°C) can be important for direct wafer bonding and to any process in which low temperature bonding is required. (004) silicon substrates were implanted with hydrogen with a dose that ranged from $5\times10^{15}cm^{-2}$ to $8\times10^{16}cm^{-2}$ and energies of either 30kV or 140kV. The changes in the implanted layer properties were investigated using triple axis x-ray diffraction and atomic force microscopy after annealing at 100°C - 300°C for short times. For annealing temperatures up to 150°C, the strain-induced implant profile did not change appreciably nor did the surface roughness increase, indicating that, for these implant conditions, the implant is stable. Annealing at 200°C or higher for 10 minutes or more led to increased surface roughness and a change to the implant profile, although blister formation did not occur. Blister formation was observed for annealing at 300°C. Higher surface roughness and blistering is not conducive to successful wafer bonding, so these measurements helped to determine the annealing sequence that is appropriate for bonding a hydrophobic implanted wafer with a hydrophobic handle wafer. Hydrophobic bonded wafers were successfully fabricated with the transferred layer showing similar structural properties as a thin epitaxial film of the same thickness.

I5.10
THERMOMECHANICAL STRESS IN SILICON ON QUARTZ WAFER BONDING AND SMART CUT© PROCESS. Yu-Lin Chao, Duke Univ., Dept. of Mechanical Engineering and Material Science, Durham, NC; Qin-Yi Tong, Microelectronics Center, Research Triangle Institute, RTP, NC; Ulrich M. Gösele, Max-Plank Institute of Microstructure Physics, Halle, GERMANY.

The thermal stress behavior of silicon/quartz bonded wafer pairs is examined. Sliding, debonding, and cracking are the observed mechanisms of relaxation. When the elastic energy due to the different thermal expansion coefficients of silicon and quartz exceeds the bonding energy, sliding will start and lead to a serrated curve on the curvature-versus-temperature graph. Finally, debonding will occur once the peeling stress exceeds the interface bonding strength. The debonded parts crack due to the overhang structure, and debonding-cracking processes continue during a further temperature increase. The stress behavior of the hydrogen-implantation induced layer splitting process (the so-called 'Smart-Cut process') of silicon/quartz pairs is also monitored in a stress measurement setup. It is observed that Smart-Cut process is a sudden process in agreement with the observations reported in the literature.

I5.11
HYDRIDE FORMATION IN HIGHLY DISORDERED BURIED LAYERS FORMED BY HYDROGEN AND DEUTERIUM IMPLANTATION OF SILICON. V.P. Popov, L.N. Safronov, D.V. Kilanov, V.I. Obodnikov, Institute of Semiconductor Physics, Novosibirsk, RUSSIA; A.P. Stepovik, V.T. Gromov, Federal Nuclear Center, Snezhinsk, RUSSIA.

FTIR study of buried highly disordered Si layers formed for ion slicing by high fluence hydrogen or deuterium implantation (up to 1.5×10^{17} cm^{-2}) using high constant current beams with means of current up to 1 mA/cm^2 and energy 200 keV in the temperature interval 80 - 420 K was carried out in the present work. Calorimetric measurements and computations of temperature regime in a thin layer on irradiation condition with a high-power ion beam and temperature of substrate were performed. Expressions, permitting to select the most optimal relations between substrate thickness, ion flux power, and times of irradiation and sample cooling in the given temperature range, were obtained. High defect concentration in combination with the very active hydrogen impurity causes the formation of highli disordered buried layers. The transformation of defects and hydrogen profiles in these layers during annealing in temperature range of 500 - 1300 K was investigated with additional SIMS. It was shown by FTIR that the density of Si-H bonds was largest directly after high current irradiation and equal of H content for lower temperatures. At highest temperatures and lower currents the density of Si-H bonds was below one tenth of the fluence. At lower temperatures different hydride lines were practically unresolved after irradiation and looks like in a-Si:H. During heat treatment their concentration fell below sensitivity limit

($0.5x10^{14}$ cm^{-2}) at 1100 K but high FTIR spectral separation allowed to obtain a kinetic of mono- di- and trihydride evaluation at lower temperatures of annealing. The kinetics for H and D containing bonds are compared. Perspectives for deuterium ion slicing are discussed.

I5.12
(111) AND (100) NANOMETER THICK SILICON FILMS IN SOI STRUCTURES FORMED DURING STEP BY STEP OXIDATION AND ETCHING. V.P. Popov, I.V. Antonova, T.A. Gavrilova, A.K. Gutakovskii, Inst of Semiconductor Physics, Novosibirsk, RUSSIA.

High dose hydrogen implantation with subsequent annealing allows one to delaminate a thin layer of silicon from a thick substrate and to connect it to an oxidized silicon wafer. The main advantages of this technology are high quality buried oxide, top silicon layer, and high flatness of interface between layers. A thickness of initial silicon top layer is managed by energy of implanted hydrogen ions and can be in the range of 200-2000 nm for ordinary implanter. A scatter of the silicon layer thickness for wafer with diameter of 100 mm is lower than 5 nm. The further reduction of the SOI film thickness has been attended by dry oxidation of wafer followed by stripping in diluted HF. This conventional technological process provides for example the thickness of SOI about of 3nm with a dispersion of 1 nm for 100 mm wafer. The thickness and uniformity of the remaining SOI films and interface layers were determined by spectroscopic ellipsometry measurements. Transmission electron microscopy (TEM) and high resolution electron microscopy (HREM) investigations approved the high perfection of final silicon layer and silicon/oxide interface. Step-by-step thermal oxidation and diluted fluoride stripping were used for creation of extremely thin ($\sim$1 nm) (111) and (100) silicon film using hydrogen ion sliced SOI structure. Changes of oxidation rate and film morphology were investigated by SEM, TEM, and HREM measurements at different temperatures and oxidizing atmosphere. Observed retardation of oxidation rates of thin Si films discussed in the frame of self limiting phenomenon. Optimal conditions for thinning procedure was obtained.

I5.13
AN ETCH-BACK PROCESS TO INTEGRATE SiGe INTO A DESIRABLE SUBSTRATE. Lijuan Huang, David R. DiMilia, Jack O. Chu, IBM T.J. Watson Research, Yorktown Heights, NY.

SiGe material has found important applications in microelectronics and optoelectronics. In particular, the strained Si/SiGe structure is promising for fabricating high speed complementary metal-oxide-semiconductor (CMOS) transistors; The SiGe on Si heterostructures are also good candidates to produce photodetectors to provide Si-based far infrared detection for the optical communication. Conventionally, a Si/SiGe structure can be achieved by epitaxial growth approaches on a Si substrate. However, for the optimum performance of SiGe based devices and circuits, it is important to have the ability to integrate SiGe into a selected substrate such as an insulator or a heavily doped Si substrate. This paper reports a new approach based on wafer bonding and etch-back processes for the transferring of high quality SiGe material onto a desirable substrate such as Si, sapphire, quartz, etc. A relaxed SiGe layer grown on a 5-inch Si substrate using the UHV/CVD technique, with Ge content ranging from 15% to 80%, will be polished by a Chemical-Mechanical Planarization (CMP) step and subsequently bonded to a selected handle substrate such as a 5-inch Si wafer with or without a thermally grown SiO_2 layer. After a mechanical polishing process which removes most of the original Si substrate, a wet etch process will be employed to etch away the remaining thin Si layer stopping at the relaxed SiGe layer. We have demonstrated significantly high etching selectivity of Si to SiGe up to 1800 in a solution of ethylenediamine, pyrocatechol, pyrazine and water (EPPW) or a KOH solution. The obtained SiGe/Si structure will be further smoothed for device fabrication. In this process, a high quality SiGe layer with a thickness in the range of 300nm-2mm can be integrated into a chosen substrate for desirable applications. The SiGe layer serves both as the etch-stop layer and as the core material for device fabrication, which significantly simplifies the material integration process. Furthermore, by avoiding hydrogen or oxygen implantation and/or high temperatuare annealing steps, the described process provide us with the flexibility of obtaining a relaxed SiGe layer with high Ge content as desired for the growth of high strained Si layer on SiGe and for the fabrication of photodetectors that would absorb light in the range of 1.3-1.6μm.

I5.14
4-INCH SILICON-ON-DIAMOND STRUCTURED WAFER AND RADIATION HARDNESS INTEGRATED CIRCUITS. Changzhi Gu, Yue Sun, Xianyi Lu, Zengsun Jin, State Key Laboratory for Superhard Materials, Jilin University, Changchun, CHINA.

The annealing technology in H plasma and microwave plasma assistant chemical vapor deposition method were used to synthesize uniform and low interface state density diamond thin film on 4-inch mirror-polished Si wafer seeded by fine diamond powders before the deposition. Silicon-on-diamond (SOD) structured wafer was utilized by means of bonding in high temperature and thinning with machine and chemical methods. 54HT109 CMOS logical circuit were fabricated with SOD wafer. The total-dose radiation characteristics of SOD circuits were performed using a cobalt-60 radiation resource, the results present that SOD circuits have a obvious ability of radiation hardness comparing with the same circuits made by bulk silicon wafer. The SOD circuits can also work at 300°C. The properties working under high temperature and radiation for SOD circuits can be attributed to the high thermal conductivity, electrical resistivity, hole mobility and low interface state density between diamond film and silicon layer.

I5.15
ANODIC BOND QUALITY AND IMPACT ON PRESSURE SENSOR LONG-TERM STABILITY. Henry Allen, Kamrul Ramzan, Jim Knutti, Silicon Microstructures, Inc., Fremont, CA; Carl Ross, Tim Milliman, Jeff Frye, Motorola AIEG, Northbrook, IL and Elma, NY.

Silicon Pressure sensors have historically been fabricating by bonding a glass wafer to a micro-machined silicon wafer. The sensor may be sealed as an absolute pressure sensor by using planar glass and can then be used for detection of barometric pressure changes. It has generally been assumed that as long as the glass and silicon are reasonable clean, then the silicon-glass seal is good and the part becomes a reliable, stable sensor. This paper addresses a low-level drift that was identified in such an absolute pressure sensor. A Zero drift in the range of 0.1% FS was detectable under humidity stresses. The stress always caused drift in the same direction, indicating an effective increased pressure in the sealed cavity. The impact of various cleaning processes in reducing drift are reported. The improved process assure reliable product for applications such as automotive and altimeter applications.

I5.16
A NOVEL METHOD OF FABRICATING SILICON CARBIDE ON INSULATOR (SiCOI) SUBTRATES FOR USE IN MEMS. Hung-I Kuo, Christian Zorman and Mehran Mehregany, Department of Electrical Engineering and Computer Science, Case Western Reserve University, Cleveland, OH.

Silicon carbide is the leading material for MEMS in harsh environment applications, due to its outstanding electrical, chemical and mechanical properties. Silicon carbide-on-oxide wafers are attractive substrates for SiC surface micromachined devices fabricated on Si wafers, since the buried oxide layer provides both electrical isolation and serves as a sacrificial layer. Wafer bonding is commonly used to fabricate these substrates, but unfortunately bonding yields are often very low (less than 50%) due to high tensile stresses in the SiC films. This paper reports on a novel, bonding-free method to fabricate silicon carbide on insulator substrates. The process bypasses wafer bonding by using a high deposition rate polysilicon process in conjunction with wet chemical etching to produce wafer-thick polysilicon layers that serve as substrates for the SiCOI structures. Because wafer bonding is not used, insulators of various material types (i.e., silicon nitride) and thickness can be used. Using this method, transfer rates over 99% are readily achievable. To demonstrate the versatility of these SiCOI substrates, both surface micromachined devices (lateral resonators) and electronic devices (Schottky diodes) were fabricated and tested. The extended paper will detail the substrate and device fabrication processes and present device test results.

I5.17
WAFER BONDING BETWEEN MAGNETIC GARNET AND LITHIUM NIOBATE FOR SEMI-LEAKY ISOLATOR. Hideki Yokoi, Tetsuya Mizumoto, Masafumi Shimizu, Tokyo Institute of Technology, Dept of Electrical and Electronic Engineering, Tokyo, JAPAN.

An optical isolator is indispensable in protecting optical active devices from unwanted reflected light. A semi-leaky isolator is very attractive because of its compact one-section structure and easy control of magnetization. The device utilizes the unidirectional mode coupling in an anisotropic / magneto-optic waveguide. Therefore, an optical contact between the anisotropic material and the magneto-optic one must be accomplished. To realize the device, we studied wafer bonding between a lithium niobate and a magnetic garnet. As the magnetic garnet, a cerium-substituted yttrium iron garnet was deposited on a garnet substrate. Prior to contacting the two wafers, the lithium niobate was activated by oxygen plasma. The magnetic garnet was slightly etched by phosphoric acid. They were placed in contact at room temperature and loaded into an annealing furnace for the heat treatment. The samples were successfully bonded with the heat treatment at temperatures ranged between 110 and 220°C. The

rib waveguide fabricated on the magnetic garnet was also successfully bonded with the lithium niobate. The anisotropic / magneto-optic waveguide for the semi-leaky isolator was obtained by wafer bonding.

SESSION I6: APPLICATIONS & DEVICES I
Chair: Michael Current
Wednesday Morning, April 18, 2001
Golden Gate C1 (Marriott)

8:30 AM *I6.1
INTEGRATION OF InGaN-BASED OPTOELECTRONICS WITH DISSIMILAR SUBSTRATES BY WAFER BONDING AND LASER LIFT-OFF. William S. Wong, Michael Kneissl, David W. Treat, Mark Teepe, Naoko Miyashita, Noble M. Johnson, Xerox PARC, Palo Alto, CA.

In many cases, the integration and enhancement of thin-film microsystems by direct deposition involves substantial sacrifices in the thin-film quality and performance. The ability to combine III-nitride-based thin-film devices with dissimilar substrate materials through a lift-off and transfer process allows for the direct integration of materials systems selected and pre-fabricated exclusively for optimal device performance rather than for growth compatibility. For example, integrating silicon with GaN-based devices creates opportunities to combine Si-based integrated-circuit technology with III-nitride optoelectronics for display and sensor applications. Furthermore, transferring pre-fabricated devices from common sapphire growth substrates onto more thermally and electrically conductive substrates such as Cu may achieve enhanced GaN-based device performance. In this talk, a robust, simple and fast "cut and paste" methodology for materials integration is described using wafer bonding and excimer laser lift-off (LLO). Examples ranging from the integration of (In,Ga)N-based light-emitting diodes (LEDs) with Si by means of transient liquid phase (TLP) Pd-In wafer bonding and LLO, in which the separation of the GaN is accomplished by laser irradiation through the transparent sapphire substrate, to blue lasers on copper substrates will be discussed. By using a low-temperature TLP bonding process in conjunction with LLO, blue LEDs on sapphire were transferred onto Si substrates. The resulting LEDs on Si could be driven up to forward currents of 100 mA at 5.4 Volts with an emission wavelength of 455 nm. In addition, the fabrication of continuous-wave InGaN multiple-quantum-well laser diodes will be described. Reduced threshold currents and increased differential quantum efficiencies were measured for LDs on Cu due to a 50% reduction of the thermal impedance compared to LDs on sapphire. Light output for LDs on Cu was three times greater than comparable LDs on sapphire with a maximum output of 100 mW demonstrating the effectiveness of the "cut and paste" methodology to enhance thin-film microsystems.

9:00 AM I6.2
REALIZATION OF InAs/AlSb/GaSb NPN HETEROJUNCTION BIPOLAR TRANSISTORS ON SAPPHIRE SUBSTRATES BY WAFER BONDING AND NATIVE SUBSTRATE REMOVAL.
P.D. Moran, Department of Chemical Engineering, University of Wisconsin, Madison, WI; D. Chow and A. Hunter, Hughes Research Laboratories, Malibu, CA; T.F. Kuech, Department of Chemical Engineering, University of Wisconsin, Madison, WI.

Antimonide-based (lattice constant = 0.61nm) Heterojunction Bipolar Transistor (HBT) structures were grown on a GaSb substrate, subsequently transferred to a sapphire substrate, and then fabricated into functional HBTs. This presentation describes the process employed to integrate the 0.61nm HBTs with a sapphire substrate and the impact of this process on the device structure. The HBT structure consisted of a 300nm n InAs/InAsSb superlattice subcollector, a 300nm n-type InAs/AlSb superlattice collector, a 75nm p AlGaSb base, a 51nm n-type InAs/AlSb superlattice emitter, and a n InAs/InAsSb superlattice layer for facilitating electrical contact. The layers in the structure were grown in reverse order on a GaSb substrate and directly bonded to sapphire. The GaSb native substrate was then removed. High resolution x-ray diffraction peaks from the transferred structure were broadened from approximately 120"FWHM to 260"FWHM after transfer to sapphire. Triple crystal diffraction analysis showed the broadening to be primarily due to a bending of the device layers as they conform to the sapphire substrate. I-V measurements of the collector-base junction after transferring the layers showed that the rectifying characteristics of the junctions remained intact. The 0.61nm-HBT-on- Al2O3 structure was processed to yield functional HBTs on sapphire substrates. This result represents an important first step towards integrating high-speed, low power logic circuits based on the 0.61nm materials with sapphire, a substrate with high frequency dielectric characteristics superior to those of the native GaSb substrate.

9:15 AM I6.3
CRYSTAL ION SLICING OF DOMAIN MICROENGINEERED ELECTRO-OPTIC DEVICES ON LITHIUM NIOBATE.
David A. Scrymgeour, V. Gopalan, Materials Research Laboratory , Pennsylvania State Univ, University Park, PA; Tony E. Haynes, Solid State Division, Oak Ridge National Laboratory, Oak Ridge, TN; Miguel Levy, Physics Department, Michigan Technological University, Houghton, MI.

The ability to control the angular position of a laser beam with high speed is of interest in many applications including optical communications, optical data storage, laser printing, and display technologies. Active solid-state electro-optic scanners based on micro-patterned $LiNbO_3$ and $LiTaO_3$ have several advantages over mechanical and other systems including small device size and high operating speed (intrinsic response frequencies >100GHz). However, widespread application of these devices is currently limited because of the large voltage required to operate devices fabricated in single crystals. A solution to this problem is to make the devices thinner. By crystal ion-slicing of domain-engineered devices fabricated on wafers, operating voltages can be significantly reduced. We report successful fabrication of 4-10 micron thick domain microengineered $LiNbO_3$ device films prepared by a combination of He-ion implantation and chemical etching. A systematic study of the processing conditions for the slicing reveals that the key parameters for successful slicing are implantation energy, temperature and time of pre lift-off anneal, and liftoff chemistry of the etchant. The surface of the sliced crystal shows crystallographic etch lines which are minimized with pre-annealing and by reducing etching time by optimizing the etchant solution. The effects of the lift-off process on pre-existing domain structures, and the scanning performance of a resulting sliced electro-optic scanner device, currently being tested, will be presented.

9:30 AM *I6.4
PHOTONIC CRYSTAL FABRICATION BY A WAFER BONDING APPROACH. Susumu Noda, Dept of Electronic Science and Engineering, Kyoto University, Kyoto, JAPAN.

Various important scientific and engineering applications such as control of spontaneous emission, zero-threshold lasing, sharp bending of light, and so on, are expected by using photonic bandgap (PBG) crystals and artificially introduced defect states and/or light-emitters. To realize the potential of photonic crystals as much as possible, the following requirements should be satisfied: (i) construction of a three-dimensional (3D) crystal with a complete PBG in optical wavelength region, (ii) introduction of an arbitrary defect into the crystal at an arbitrary position, (iii) introduction of an efficient light-emitter, and (iv) use of an electronically conductive crystal, which is desirable for actual device application. Although various important approaches have been proposed and investigated to construct the 3D crystals, there have been no reports which satisfy the above requirements simultaneously. Recently, we developed complete 3D PBG crystals at infrared ($5\sim10\mu$m) to near-infrared wavelengths ($1\sim2\mu$m) based on a method where III-V semiconductor stripes are stacked with a wafer-bonding and a laser-beam assisted very precise alignment technique to construct a diamond structure. Since the crystal is constructed with III-V semiconductors which are widely utilized for optoelectronic devices, the requirement (iii) is satisfied. Moreover, as the wafer-bonding enables us to construct an arbitrary structure and to form an electronically conductive interface, all the above requirements (i)-(iv) will be satisfied. In this symposium, I will review our approach to create the full 3D PBG crystals[1].

[1]S. Noda, K. Tomoda, N. Yamamoto, and A. Chutinan, Science, vol. 289, 604 (2000).

SESSION I7: APPLICATIONS & DEVICES II
Chair: Takao Yonehara
Wednesday Morning, April 18, 2001
Golden Gate C1 (Marriott)

10:30 AM *I7.1
APPLICATIONS OF WAFER BONDING AND LAYER TRANSFER FOR ADVANCED CMOS DEVICES. H.-S. Philip Wong, Don Canaperi, Kevin K. Chan, Guy M. Cohen, Kathryn Wilder Guarini, Lijuan Huang, Erin C. Jones, and Paul M. Solomon, IBM T. J. Watson Research Center, Yorktown Heights, NY.

As CMOS devices scale into the nanometer regime, the material set and device structures employed by conventional FET are beginning to reach their limits. In this paper, device features of CMOS at the nanometer regime are examined. This includes new devices formed by different device structures such as the double-gate FET and back-gate FET, as well as new devices made of new materials and combinations of new materials such as silicon germanium. Wafer bonding and layer transfer techniques are essential process elements for these new

structures and materials. Examples of using wafer bonding to achieve the double-gate FET are given. Layer transfer of SiGe to achieve SiGe on insulator will be described.

11:00 AM I7.2
MULTIPLE WAFER BONDING FOR MEMS APPLICATIONS. M. Reiche, Max Planck Institute of Microstructure Physics, Halle, GERMANY; M. Haueis, J. Dual, ETH Zürich, Institut of Mechanics, Zürich, SWITZERLAND; C. Cavalloni, Kistler Instrumente AG, Winterthur, SWITZERLAND; R. Buser, Interstate University of Applied Science Buchs, Buchs, SWITZERLAND.

Most of the microelectromechanical systems (MEMS) require a 3-dimensional architecture which can efficiently be realized by multiple semiconductor wafer direct bonding. The present paper demonstrates the method on a force sensor for high resolution measurements of static loads. To minimize temperature stress an all-in silicon solution was developed in contrast to micromachined resonant force sensors published already in the literature. The following process steps are discussed in detail: (i.) Preparation of a SOI wafer package by a first wafer bonding step. A prepatterned and oxidized handle wafer was bonded to a top wafer. (ii.) The top wafer was thinned by grinding and polishing down to a thickness of 80 μm. (iii.) After patterning the top layer a third wafer (also patterned) was bonded on it. This second wafer bonding step includes a prealignment and bonding under vacuum followed by a low-temperature annealing. Analyses of the wafer stacks after the individual bonding steps are presented (interfacial defects, mechanical strength, effect of the BOX thickness of the SOI wafer and the annealing temperature, respectively, on geometrical parameters (bow), effect of the bow on the aligned wafer bonding, etc.). The presented force sensor integrates load coupling, the excitation and detection of the vibration of the microresonator in one and the same single crystal silicon package. Details of the sensor structure are published elsewhere [1]. First measurements proved a sensitivity of 26 Hz/N and a resolution better than 3 mN. [1] M. Haueis et al., submitted to Transducers 2001, Munich

11:15 AM I7.3
PACKAGING OF ULTRATHIN SEMICONDUCTOR DEVICES THROUGH THE ELO PACKAGING PROCESS. Mike Sickmiller, Dawei Zheng, ELO Technologies, Inc., Torrance, CA.

The trend in semiconductor packaging is moving toward thinner and thinner packages. Likewise, chip profile is moving toward thinner and thinner chips. Presented here is a technique used to obtain a semiconductor package containing chips as slim as one micron in thickness. The ELO Packaging Process yields ultrathin chips for applications such as advanced heat sinking, high-efficiency optoelectronics, multiple stacked chips in a single package, and thin mechanically flexible semiconductor circuits. This technology is being developed around both the fab and packaging house so as not to interfere with the conventional semiconductor fabrication process flow. Through a combination of back-grinding and chemical etch techniques, chips have been thinned to as little as 1 um and bonded to a variety of new host substrates. Several bonding methods have been utilized, including thin solder or epoxy layers, to bond these functional chips to a variety of new substrates. Ultrathin microwave power amplifiers have been bonded to heat sinks and optoelectronic devices have been bonded to transparent substrates. In both cases, the ultrathin chip configuration coupled with the desired substrate can increase performance of the chip by a factor of 10X.

11:30 AM I7.4
A NOVEL ULTRA-MINIATURE CATHETER-TIP PRESSURE SENSOR FABRICATED USING SILICON AND GLASS THINNING TECHNIQUES. Henry Allen, Kamrul Ramzan, Jim Knutti, Silicon Microstructures, Inc., Fremont, CA; Stan Withers, EndoSonics Corporation, Rancho Cordova, CA.

A novel subminiature pressure sensor for blood pressure measurement has been fabricated. The device is only 250 microns wide and 70 microns thick. It is 1.1 mm in length. The sensor is housed in a guide-wire lead for use in measuring coronary artery blood pressure. The device has less than a 5 micron thick silicon diaphragm and senses pressure using a 1/2 bridge piezoresistive network. Glass is processed to provide depressions above the sensing area as well as above the connection area of the device. A full-thickness silicon wafer is processed using standard micromachining techniques. V-Groove notches are micro-machined on the top surface of the silicon to provide locators/guides for the lead-wires. Diaphragm windows are patterned on the back of the silicon wafer and the wafer is etched down to form the 5 micron diaphragm, using electro-chemical etch-stop techniques. The Glass and Silicon wafers are aggressively cleaned prior to bond. The glass and silicon wafers are then precisely aligned to better than 10 microns and bonded using anodic bonding techniques. The glass/silicon wafer sandwich then has the silicon thinned from 400 microns to 35 microns using both grinding and polishing. Then the full-thickness glass wafer is etched in HF to a thickness of 35 microns as well, for a composite 70 micron thick structure. The wafer is then diced to form the micromechanical structure. Measurement and control issues will be discussed.

11:45 AM I7.5
LAYER TRANSFER OF SILICON USING POLYMER AND TEOS BONDING. Cynthia Colinge, José E. Bahia, California State University, Dept. of Electrical Engineering, Sacramento, CA; Brian Roberds, Intel Corp., Hillsboro, OR.

Some of the recent challenges outlined in the 1997 Semiconductor Industry Association (SIA) National Technology Roadmap for Semiconductors (NTRS) include reducing minimum feature size to increase the density of devices per chip, and increasing the number of functions on a chip. One novel approach that could double the density of devices per area without the need of new lithography would be to stack layers of devices in a three-dimensional structure. In this presentation, recent research using hydrogen splitting and polymer bonding for layer stacking will be discussed. The processing steps used here include; bonding a hydrogen implanted wafer to an intermediate handle substrate, delamination using ion cut, bonding the intermediate structure to a second wafer, and finally debonding for removal of the handle substrate. The process could be repeated for stacking multiple thin-film silicon layers using a low-K polymer between active devices. Materials and processing steps will be discussed including the advantages and limitations of using low-K dielectric polymers and TEOS for the bonding/debonding.

SESSION I8/D8: JOINT SESSION COMMERCIALIZATION OF BONDED SILICON-ON INSULATOR (SOI)

Chair: Marin Alexe
Wednesday Afternoon, April 18, 2001
Golden Gate C1 (Marriott)

1:30 PM *I8.1/D8.1
COMMERCIALIZATION OF THICK AND THIN SOI BY THE SMART CUT^{TM} PROCESS. A.J. Auberton-Hervé, SOITEC, Bernin, FRANCE.

The semiconductor industry growth and success in following the Moore law has been supported by some key strategic materials and key technology enabling the introduction of these new materials. In the new material hardly demanded by the semiconductor industry, three receive today most of the attention: Copper, low k dielectrics and SOI. Among these materials, two are in the interconnection domain and only SOI concerns the improvement of the silicon itself. As interconnections are no more the IC's performance limitation, silicon is again at the center of the speed enhancement. The key drivers for SOI are today speed and low power consumption. Due to the increasing demand for portable systems with higher autonomy and better performance, SOI is today considered as the necessary change in the silicon material evolution. In the "bag of tricks" available for the engineers, the Smart Cut^{TM} technology offers a major breakthrough by providing the solution to the following issue: how to get a deposition technique which bring a pure monocrystalline film on top of any kind of substrate (amorphous, crystalline, plastic...)? Smart Cut^{TM} process is already in use for large volume SOI wafer production. Availability of high quality SOI wafers achieved using Smart Cut^{TM} process has already been demonstrated as SOI Unibond roadmap meets the most advanced requirements for 0.13 μm technology. This paper shows that such wafer quality can be adapted to customer demand with flexibility concerning the layer thickness specifications from a few 10nm for both the silicon and the buried oxide layers to micrometer range. Volume production data are shown for 2 typical 8" products (one thin and the other thick), enhancing control of silicon and buried oxide thickness uniformities, particles control over 0.16μm and HF defect monitoring. Production capacity including 300mm projection is also discussed with the necessary volume required by 0.18μm and below technologies.

2:00 PM *I8.2/D8.2
BONDING, SPLITTING AND THINNING BY POROUS Si IN ELTRAN^{TM}; SOI-Epi Wafers^{TM}. Kenji Yamagata and Takao Yonehara, ELTRAN Business Center, Canon Inc., Kanagawa, JAPAN.

ELTRAN is a unique technology categorized in Bonding and Etch-back SOI and has been originated, developed and produced by Canon. In this process, there are several novel technologies using porous silicon material, that is, silicon epitaxial growth on its surface, water jet splitting at the interface of double stacked porous layers after bonding, and selective etching of porous silicon with very high selectivity of 1E5. Accordingly the porous silicon material plays an

important role in ELTRAN process. Especially the SOI layer quality is decided by silicon epitaxial growth onto porous silicon surface, therefore porous fabrication step is very important. We have developed the fully automatic anodization machine for the mass production. In this machine, it is possible to anodize allover the surface of multiple silicon wafers in a batch with a good uniformity and to control the porous thickness and porosity by a computer system. In order to design the machine to achieve such features, we carried out the computer simulation on porous silicon formation with the three dimensional current field analysis by a finite element method. It was found out that the porous silicon thickness uniformity depended on the cathode size and distance between a cathode and a silicon wafer in the anodization system. Generally in bonding SOI wafer manufacturing, cost issue is very crucial so that we have also developed the fully automatic water jet splitting system for mass production. As a result the fabrication cost could be reduced by splitting and recycling technology of the bonded wafers. Furthermore we are developing another type of an anodization machine and improving the water jet machine in order to extend this technology to 300mm wafer. It has succeeded to produce the uniform porous silicon layer, and split over the entire 300mm wafers, which enables us to produce 300mm SOI wafers.

2:30 PM *I8.3/D8.3

ATOMIC-LAYER CLEAVING AND NON-CONTACT THINNING FOR FABRICATION LAMINATED ELECTRONIC AND PHOTONIC STRUCTURES. M.I. Current, M. Fuerfanger, S. Kang, M. Korolik, I. Malik, S. Farrens, L. Feng, F. Henley, Silicon Genesis, Campbell, CA.

Use of new approaches to film deposition and ion beam modification techniques provide avenues for enhanced bond strengths and engineered cleave plane structures which result in layer transfer of electronic and photonic materials for efficient fabrication of laminated electronic and photonic structures. These structures include Silicon-on-Insulator wafers and a variety of optical signal couplers, routers and sensors. The ability to form cleaved layers containing Si, SiGe alloys and SiO_2 with Angstrom-level surface finish after room-temperature separation provides an opportunity to bond a new crystalline structure directly onto the transferred layer without the need for contract polishes and etching of damaged layers. A suite of innovative layer transfer techniques, which includes plasma-activated bonding, CVD film deposition, light-ion implantation and non-contact, post-cleaving thinning and smoothing processes, will be described. Applications for multi-level structures such as integral fabrication of SOI wafers with multi-layer high-mobility channel structures, multi-level SOI wafers for fabrication of self-aligned dual-gate CMOS and a variety of optical structures will be discussed.

SESSION I9/D9: JOINT SESSION
SILICON-ON-INSULATOR
Chair: Bernard Aspar
Wednesday Afternoon, April 18, 2001
Golden Gate C1 (Marriott)

3:30 PM I9.1/D9.1

ORIENTATION AND BORON CONCENTRATION DEPENDENCE OF Si LAYER TRANSFER BY MECHANICAL EXFOLIATION. K. Henttinen, T. Suni and I. Suni, VTT Electronics, Microelectronics Center, Espoo, FINLAND; S.S. Lau, University of California-San Diego, Department of Electrical & Computer Engr., La Jolla, CA.

It has been shown that H-implanted silicon can be exfoliated by mechanical means without thermal annealing at moderately high temperatures, i.e. 400-500°C. The key to this splitting method is to render the implanted region weaker than the bonded interface between the donor and the handle wafer. When subjected to a mechanical splitting force, the weaker region yields to the splitting force and cause delamination. Mechanical layer transfer has the advantage of producing a smooth delaminated surface and intrinsically low temperature process for the matching of dissimilar materials. The mechanical splitting process is affected by the crystal orientation and boron concentration in a similar fashion as observed for thermal splitting. We have measured the strength of the H-implanted region of <100>, <111> and <110> oriented silicon wafers by the crack opening method. The required energy for mechanical layer splitting is lowest for <100> silicon and highest for <110> silicon. These results are compared to the data reported for surface blistering of hydrogen implanted and annealed silicon wafers of various orientations. The influence of boron doping on the mechanical splitting process has been found to decrease with boron implantation at doses $> 10^{13}$ cm^{-2}. The various aspects of the mechanical and the thermal exfoliation processes will be discussed.

3:45 PM I9.2/D9.2

STRUCTURED MONOCRYSTALLINE Si FILMS FROM LAYER-TRANSFER USING THE POROUS Si (PSI) PROCESS. Richard Auer, Gregor Kuchler and Rolf Brendel, Bavarian Center for Applied Energy Research (ZAE Bayern), Erlangen, GERMANY.

We report on the successful fabrication of monocrystalline Si solar cells with a thickness of 3 to 20 microns having two- and three-dimensionally structured surfaces. We fabricate the structured films with the porous Si (PSI) process: Prior to epitaxy the surface of a Si wafer is structured by wet chemical etching and then transformed into porous Si; thus permitting layer detachment after bonding or gluing the epitaxial film to a glass carrier. The film surfaces have grooves or pyramids. The latter are periodic or random, upright or inverted. The epitaxial growth is controlled to yield either a conformal film growth or films with one surface structured and the other side planar. The surface structures modify the interaction of the epitaxial film with light and thus enable the fabrication of novel devices such as infrared diffraction grids and thin-film solar cells. For solar cells from crystalline Si, the absorption enhancement is a necessity. Applying Monte Carlo ray tracing studies we select those surface textures with particularly high absorption. The first thin-film Si solar cells that we fabricate from 17 micron-thick films with randomly positioned inverted pyramids have a power conversion efficiency exceeding 10%. The analysis of the measured internal quantum efficiency confirms efficient light trapping. The absorption enhancement is caused by an average optical path length that is 14 times the layer thickness. The fabrication of structured thin-film Si cells by layer-transfer opens a new path for the fabrication of thin monocrystalline solar modules.

4:00 PM I9.3/D9.3

TRANSFER AND HANDLING OF THIN SEMICONDUCTOR MATERIALS BY A COMBINATION OF WAFER BONDING AND CONTROLLED CRACK PROPAGATION. Joerg Bagdahn, Johns Hopkins University, Dept of Mechanical Engineering, Baltimore, MD; Dieter Katzer, Matthias Petzold, Fraunhofer Institute for Mechanics of Materials, Halle, GERMANY; Maik Wiemer, Fraunhofer Institute for Microintegration and Reliability, Chemnitz, GERMANY; Viorel Dragoi, Marin Alexe, Ulrich Gösele, Max-Planck-Institute for Microstructure Physics, Halle, GERMANY.

Many wafer bonding techniques, such as Si-Si fusion bonding using hydrophilic conditions and Si-glass anodic bonding, are based on the formation of covalent Si-O atomic bonds in the joint interface. If the interface is mechanically loaded below the fracture limit, a slow (subcritical) crack growth can occur in the bond interface depending on stress level and environmental conditions. This process can be related to a stress-activated chemical corrosion of the Si-O bonds similar to the behavior of mechanically loaded glasses and ceramics. On the other hand, most of the semiconductor bulk materials, such as Si or GaAs, are well known to be insensitive to stress corrosion processes. Therefore, the subcritical crack growth is confined to the wafer bond interface preventing the crack to kink into the wafer material. The effect enables a controlled cleaving of direct or anodic bonded wafers and may, consequently also be utilized for the transfer and handling of thin semiconductor materials. The presented approach consists of three basic steps. First, a process wafer is bonded with a handle wafer. Subsequently, the process wafer can be back-ground to the required thickness. In the second step, all necessary technological processes such as oxidization, implantation, film deposition, high temperature annealing or etching can be performed on the process wafer without any restrictions due to the handle substrate. In the third step, the process wafer is cleaved from the handle wafer using a controlled subcritical crack growth in the bonded interface. The handle wafer will not be destroyed and can, therefore be used again for further process steps. The paper presents the fracture mechanics fundamentals of subcritical crack propagation in wafer bonded interfaces. It will be shown that an accurate control of the applied loading conditions allows to perform the separation process with a cleavage velocity in the range of millimeters per second. First results of handling and transferring of thin silicon, pyrex, GaAs and InP wafer materials will be presented and discussed with respect to potential applications in microelectronics, optoelectronics and micromechanics.

4:15 PM I9.4/D9.4

NOVEL Si/SiGe DEVICE STRUCTURES ON SiGe-ON-INSULATOR (SGOI) SUBSTRATES. Jack O. Chu, L.J. Huang, J.A. Ott, C. D'Emic, D.F. Canaperi, P.M. Mooney, S.J. Koester, H.-S. Philip Wong, IBM Research Division, T.J. Watson Research Center, Yorktown Heights, NY.

Currently Si/SiGe FET devices rely on the growth of a relaxed SiGe buffer to create the strain between Si and SiGe layer to generate quantum wells with enhanced transport properties. However, there is no straightforward integration scheme for fabricating such high

performance devices on an insulator for reducing parasitic junction capacitance and for low power operations. This presentation will emphasize the fabrication of novel Si/SiGe heterostructures on SiGe-On-Insulator (SGOI) substrates fabricated for the first time by wafer bonding and hydrogen-induced layer transfer. Process flows will be described for the H-induced layer transfer of a relaxed SiGe layer, with Ge content ranging from 15% to 25%, to a Si handle wafer (5" or 8") that had 300nm thermally grown SiO_2. By using this technique, SGOI substrates can be generated with different Ge contents to effectively control the amount of strain which will be imparted to the SiGe device structures during its growth on these SGOI. For device fabrication, high quality strained Si and SiGe layers, as chacterized by X-ray and XTEM analysis, have been successfully grown of these SGOI structures after a CMP step using the UHV/CVD technique in the temperature range 500-550C. In particular, we grew several n-type modulation-doped SiGe heterostructures on these SGOI substrates which yielded high electron mobility in the range of 1500-2000 cm^2/Vs and about 40,000 cm^2/Vs at room temperature and 30K, respectively. This is the first time a modulation-doped SiGe heterostructure has been fabricated on an insulator. Similarly, the growth of p-type MODFETs' are currently in process and enhanced hole mobility in the range of 500-1000 cm^2/Vs is expected.

4:30 PM I9.5/D9.5

GETTERING CONTROL AT BONDING INTERFACE IN ELTRAN^{TM}. K. Momoi, M. Ito, N. Sato, N. Honma and T. Yonehara, Canon Inc., ELTRAN Business Center, Kanagawa, JAPAN.

Metal gettering capability in SOI wafers that is different from bulk wafers would be a key to establish the robust process for high dense SOI devices. Only a few reports have discussed the gettering mechanism of bonded SOI. In this paper, the correlation of gettering site formation at the bonding interface with bonding pre-treatments was studied for ELTRAN^{TM} SOI-Epi wafers^{TM}, which is characterized by bonding of epitaxial Si on porous Si, splitting and etching back of porous Si. A thermally oxidized epitaxial Si over porous Si was bonded with a Si handle wafer. Both hydrophobic and hydrophilic handle wafer surfaces were examined. The surfaces of the completed ELTRAN wafers were artificially contaminated by Fe, Ni and Cu, and were annealed at 1050°C for 3 hours in nitrogen ambient to diffuse them into the wafers. ICP-MS analysis in conjunction with a step etching method revealed that the metal concentration in the top Si layer in case of the hydrophobic treatment was 1/4 - 1/17 lower than that of both buried oxide (BOX) and the bonding interface. This result suggests that the bonding interface has the metal gettering capability. It was found by X-TEM observation that small cavities, "nano gaps", which had a few nm deep and anisotropic rectangular shapes with the density of $10^{11}/cm^2$ were generated at the bonding interface only by the hydrophobic treatment, although they were not observed in the hydrophilic. Diffused metals were presumably segregated at the inner surface of the "nano gaps". Further investigation about the gettering mechanism by the "nano gaps" will be discussed in the meeting. It was possible to form and reproduce the gettering sites by controlling the surface treatments prior to wafer bonding. This technology would be promising because no additional steps are necessary for SOI wafer manufacturing.

4:45 PM I9.6/D9.6

CHARACTERIZATION OF OPTICAL LIFETIME IN SILICON-ON-INSULATOR WAFERS BY PHOTOLUMINESCENCE DECAY METHOD. Shigeo Ibuka, Michio Tajima, Institute of Space and Astronautical Science, Sagamihara, JAPAN; Atsushi Ogura, NEC Corporation, System Devices and Fundamental Research, Tsukuba, JAPAN.

We report observation of the lifetime of the luminescence due to an electron-hole droplet (EHD) in silicon-on-insulator (SOI) wafers, and demonstrate its application to characterization of the crystalline and interfacial quality of SOI wafers. Formation of the EHD in a superficial Si layer was realized using pulsed ultraviolet laser light as an excitation source, because of its shallow penetration depth and confinement of photo-excited carriers within the layer. The EHD lifetime of SOI wafers was shorter than that of a bulk Si wafer, and was further reduced after removal of the surface oxide layer. We also found that the lifetime of bonded SOI wafers was shorter in the wafer with a bonding interface between the superficial layer and oxide interlayer than in the wafer with the interface between the interlayer and substrate. These findings can be explained by the difference in the recombination process via surface and interface states, suggesting that the EHD lifetime is applicable to the characterization of the surface, interface and bond quality of SOI wafers. The EHD lifetime also depended on wafer vendors and the fabrication techniques in commercial SOI wafers with the same thickness and surface conditions, although there were negligible differences in the luminescence spectral shape among the wafers. We believe that the dependence originates from the crystalline and interfacial quality of the superficial Si layer. We therefore propose that the EHD lifetime measurement has great potential for characterization of SOI wafers. This work was supported partly by JSPS Research for Future Programs under the project: "Ultimate Characterization Technique of SOI Wafers for Nano-Scale LSI Devices".