SYMPOSIUM K

Gate Stack and Silicide Issues in Si Processing II

April 17 – 19, 2001

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* Invited paper

SESSION K1: HIGH-k MATERIALS
Chairs: Christopher C. Hobbs and Wayne L. Gladfelter
Tuesday Morning, April 17, 2001
Golden Gate C2 (Marriott)

8:30 AM *K1.1
MATERIALS PROPERTIES OF NOVEL ULTRA-THIN HIGH-k AND MEDIUM-k GATE DIELECTRICS. Ran Liu, Motorola, DigitalDNA Laboratories, Mesa, AZ.

Rapid shrinking in device dimensions calls for replacements of SiO_2 by new gate insulators in future generations of MOSFET. Among many desirable properties, potential candidates must have higher dielectric constant, low leakage current, and thermal stability against intermixing or diffusion to ensure sharp interfaces with both the substrate Si and the gate metal (or poly-Si). Extensive characterizations of such materials in thin-film form are crucial not only for selections of the alternative gate dielectrics and processes but also for developments of appropriate metrology of the high-k films on Si. This paper will report recent results on structural and compositional properties of thin film $SrTiO_3$ and various transition metal oxides (ZrO_2, HfO_2, and TiO_2) and their silicates, characterized using RBS, AES, SIMS, SEM, TEM, AFM, XPS, XRD, XRF, spectroscopic ellipsometry, and far-infrared absorption spectroscopy.

9:00 AM K1.2
THERMAL STABILITY OF ZrO_2:SiO_2 AND HfO_2:SiO_2 BINARY OXIDE FILMS. Deborah A. Neumayer, Eduard Cartier, IBM T.J. Watson Research Center, Yorktown Heights, NY.

The thermal stability, microstructure, and electrical properties of ZrO_2:SiO_2 (ZSO) and HfO_2:SiO_2 (HSO) binary oxide films prepared by chemical solution deposition (CSD) was examined as a function of Zr/Si and Hf/Si ratio and annealing temperature to help asses their suitability as a replacement for silicon dioxide gate dielectric in complementary metal oxide semiconductor (CMOS) transistors. The ZSO and HSO CSD solutions were prepared from a mixture of zirconium, hafnium and silicon butoxyethoxides dissolved in butoxyethanol. The films were spun onto SiO_xN_y coated Si wafers and furnace annealed at temperatures from 500-1200°C in oxygen for 30 minutes. At Zr or Hf concentrations $\geq$ 50%, phase separation and crystallization of tetragonal ZrO_2 and HfO_2 was observed at 800°C. At Zr or Hf concentrations $\geq$25%, phase separation and crystallization was observed at 1000°C. As annealing temperature increased, a progressive change in microstructure was observed in the FTIR spectra. Additionally, the FTIR spectra suggest that Hf is far more disruptive of the silica network than Zr even at Hf concentrations less than 25%. The dielectric constant was observed to be concentration and annealing temperature dependent with higher dielectric constants observed at higher Zr and Hf contents and lower annealing temperatures.

9:15 AM K1.3
ZrO_2 FOR USE AS A GATE DIELECTRIC MATERIAL - COMPOSITIONAL MORPHOLOGICAL AND ELECTRICAL STUDY. You-Sheng Lin, Jane P. Chang, Department of Chemical Engineering, University of California Los Angeles, Los Angeles, CA; Sagy C. Levy, Robin S. Bloom, Avishai Kepten, Steag CVD Systems Inc., San Jose, CA.

The scaling down of Complementary Metal Oxide Semiconductor devices has increased the demand for gate dielectrics with a higher dielectric constant than Silicon Dioxide. ZrO_2 is one of the promising candidates to replace silicon dioxide as a gate material. In this work the surface preparation, rapid thermal deposition of ZrO_2, and insitu rapid thermal annealing of the deposited ZrO_2 film were carried out in an Integrated Cluster tool. We studied the reaction kinetics by examining the samples deposited under various conditions with XPS, that characterized the film composition and chemical states. Combined with the deposition rate determined by spectroscopic ellipsometry measurements we extracted the activation energies to be 19kJ/mol. The effect of substrate temperatures during precursor exposure and oxidation on film roughness was studied with AFM, and minimal surface roughening was achieved by manipulating process deposition conditions and the subsequent annealing. It was shown that roughness increased with the deposition time. Next we examined the interface property as function of the process parameters using TEM and angle resolved XPS. It was found that the film is consisted of two layers- a top ZrO_2 layer and a $ZrSi_xO_y$ base layer. The interfacial property was correlated to the MOS capacitor device analysis. Flat band shift was extracted from C-V measurement and was found to correlate with oxidation temperature. Flat band voltage shift was also correlated to the precursor exposure time. Increasing the precursor exposute time resulted in an increase in the normalized leakage current. Increasing oxidation temperature resulted in a decrease in the normalized leakage current. Transistor data also gave an insight to the interfacial property, and the charge mobility was correlated to TEM and XPS results. From transistor data analysis It was found that the interface states value, extracted from the subtreshold swing, is close to the one of thermal oxide.

9:30 AM K1.4
ULTRA-THIN ZIRCONIUM OXIDE FILMS DEPOSITED BY RAPID THERMAL CHEMICAL VAPOR DEPOSITION AS ALTERNATIVE GATE DIELECTRIC. You-Sheng Lin and Jane P. Chang, Department of Chemical Engineering, University of California, Los Angeles, CA.

ZrO_2 is investigated in this work to replace SiO_2 as the gate dielectric material in metal-oxide-semiconductor devices and was deposited on Si(100) wafers by rapid thermal chemical vapor deposition process using a zirconium t-butoxide $Zr(OC_4H_9)_4$ precursor and oxygen. Nearly atomic layer like deposition was achieved by introducing the two chemistries sequentially into the reactor. The deposited ZrO_2 film was nearly stoichiometric, fully oxidized, and amorphous as analyzed by XPS and XRD. The refractive index of 2.1 and less than 0.2 nm thickness variation across 4" and 6" wafers were determined by spectroscopic ellipsometry for 20-60 Å thick films. The deposited films were extremely smooth (RMS 1.5 Å) based on AFM measurement. The high resolution TEM image showed an interfacial layer between ZrO_2 and the silicon substrate. This interfacial layer is believed to be zirconium silicate based on thermodynamic calculation and etching resistance measured at the interface. To test the conformality of the deposited film, ZrO_2 was deposited on nanometer scale features with an aspect ratio of 4 and excellent step coverage was observed from SEM measurement. NMOS transistors and MOS capacitors of a $Al/ZrO_2/Si$, $poly\text{-}Si/ZrO_2/Si$, and $Al/ZrO_2/Si_3N_4/Si$ structures were fabricated and tested The dielectric constant of RTCVD ZrO_2 was 16-18, which was slightly lower that of the bulk ZrO_2. This is attributed to the carbon incorporation, as determined by XPS, and the formation of zirconium silicate at the interface. The C-V hysteresis was found to be 120 mV, which is higher than the desired <50 mV value, and we are investigating various post-deposition annealing chemistries to minimize the oxide charges. We found that a thin layer of Si_3N_4 grown in-situ prior to the ZrO_2 deposition improve the interfacial properties and are currently investigating their effect on the devices electrical performance.

10:15 AM K1.5
$Si/ZrO_2/Si$ GATE STACK SYSTEMS. Charles M. Perkins, Paul McIntyre, and Baylor Triplett, Dept. of Materials Science and Engineering, Stanford University, Stanford, CA; Krishna Saraswat, Dept. of Electrical Engineering, Stanford University, Stanford, CA.

Alternative gate dielectrics have gained a significant audience due to their potential of extending CMOS scaling. To alleviate integration issues, many people prefer that these new dielectrics first be used in conjunction with silicon-based electrodes. In this work, material and electrical properties of gate stack structures composed of ZrO_2 gate dielectrics and polysilicon electrodes are reported. The ZrO_2 films were deposited by atomic layer chemical vapor deposition (ALCVD) after different substrate preparations. Polysilicon electrodes were deposited using different temperatures, ambients, and surface preparations. The structure, composition, and interfacial characteristics of these gate stacks were examined using electron diffraction, x-ray photoelectron spectroscopy, and cross-sectional transmission electron microscopy. The ZrO_2 films were found to be polycrystalline with a tetragonal crystal structure. An interfacial silicate layer with a moderate dielectric constant formed between the ZrO_2 layer and the substrate during ALCVD growth on oxide-terminated silicon. Initial annealing data show the ZrO_2 films to be stable with respect to the silicon substrate up to 1000°C in an N_2 ambient. Additional data will be presented regarding the stability of ZrO_2 with polysilicon electrodes. MOS capacitors were fabricated with these structures to measure capacitance-voltage and leakage-voltage properties.

10:30 AM K1.6
$SrTiO_3$ DERIVATIVE STRUCTURES FOR ALTERNATIVE GATE DIELECTRICS. J.H. Haeni, J. Lettieri, S. Trolier-McKinstry, D.G. Schlom, Dept of Materials Science and Engineering, Penn State University, University Park, PA; W. Tian, X.Q. Pan, Dept of Materials Science and Engineering, University of Michigan; H. Chang, I. Takeuchi, X.-D. Xiang, Lawrence Berkeley National Laboratory; C.A. Billman, F.J. Walker, R.A. McKee, Oak Ridge National Laboratory.

Recently, $SrTiO_3$, the $n = \infty$ member of the $Sr_{n+1}Ti_nO_{3n+1}$ homologous series, has received much attention as a promising material for an epitaxial alternative gate dielectric for Si MOSFET's. Despite the advantage of a high dielectric constant, it suffers from several disadvantages including unfavorable band alignment with silicon, a small bandgap, and a tendency to be reduced when heated in a hydrogen environment. In the search for an alternative to $SrTiO_3$,

we have synthesized the first five members of the $Sr_{n+1}Ti_nO_{3n+1}$ homologous series by MBE on oxide substrates. In addition, we have grown the first member of this series, Sr_2TiO_4 epitaxially on silicon (100). Sr_2TiO_4 offers several potential advantages to $SrTiO_3$ as an alternative gate dielectric. Not only is Sr_2TiO_4 better lattice matched to Si (100) which could lead to improved interface properties, it is anticipated that with a crystal structure which is a composite of SrO (bandgap 5.3 eV) and $SrTiO_3$ (bandgap 3.3 eV), Sr_2TiO_4 should have an intermediate bandgap, reducing gate leakage. In addition, we have shown that Sr_2TiO_4 is not reduced when heated to over 1400°C in a reducing environment. Electrical measurements on these films will be presented along with structural characterization with 4-circle x-ray diffraction and high-resolution TEM.

10:45 AM K1.7
LANTHANUM AND ZIRCONIUM OXIDES FOR ALTERNATIVE HIGH PERMITTIVITY GATE DIELECTRICS. Dwi Wicaksana[a], Susanne Stemmer[b], H. Scmidt[c], B. Busch[c], Jon-Paul Maria[a] and Angus Kingon[a]; [a]North Carolina State University, Dept of MS&E, Raleigh, NC; [b]Rice University, Dept of Mechanical Engineering and Materials Science, Houston, TX; [c]Rutgers University, Dept of Chemistry, Piscataway, NJ.

To evaluate their applicability for high permittivity (high K) alternative gate dielectrics La_2O_3 and ZrO_2 thin films have been studied. Films with thicknesses ranging from 1.5 nm to 10 nm were grown on highly doped 200-mm silicon wafers incorporating several interfacial layers by reactive evaporation. Films were post processed using tube furnace anneals, a low-pressure vertical furnace, or rapid thermal annealing. Conditions were chosen to reflect some of the high temperature steps encountered in an actual transistor fabrication process flow. Sputter deposited Pt gate electrodes were used to complete MOS structures. Post-metallization annealing was performed under oxygen/air and forming gas ambients. After heat treatments of 1000°C, electrical characterization showed material with an equivalent oxide thickness (t_{ox}) of less than 2 nm and leakage currents between 10^{-4} and 10^{-5} A/cm^2. Post deposition annealing was performed as a function of oxygen partial pressure. For 3 nm thick La_2O_3 films, the critical pressure above which interface growth occurred was approximately 5×10^{-4} Torr pO_2. Between this pressure and approximately 10^{-8} Torr pO_2, interface growth and dielectric decomposition was negligible. Comparisons were made between chemical oxide interfaces and HF-last surfaces, films deposited on chemically grown SiO_2 exhibited the best thermal stability, showing a little dependence of tox and leakage current on process temperatures as high as 1000°C. The ambient during post-metallization annealing strongly affected interface charges as indicated by C-V curves. Additional measurements include ion scattering spectrometry, and scanning transmission electron microscopy (with EELS analysis). The important results of these analyses indicate temperature limits for chemical stability, as-deposited oxygen stoichiometry, and the evolution of interface formation during post-deposition processing. A critical comparison to the behavior of ZrO_2 thin films will be presented. This comparison will be given in the context of proposed reaction mechanisms.

11:00 AM K1.8
HfO_2 FILM FORMATION BY METALORGANIC CHEMICAL VAPOR DEPOSITION. A. Hoshino, T. Suzuki and H. Machida, TRI Chemical Laboratory Inc., Technical & Development Department, Yamanashi, JAPAN; A. Ogura, NEC Corp., Tsukuba, JAPAN; Y. Ohshita, Toyota Technological Institute, Nagoya, JAPAN.

HfO_2 film has high dielectric constant and good thermal stability, so replacing the SiO_2 layer with HfO_2 should improve MOS device characteristics. So far, PVD, such as sputtering or MBE, has been mostly used for HfO_2 film deposition. However, CVD is strongly desired for future fine devices because structures such as the damascene gate and vertical MOSFET require conformal deposition. In this study, we formed thin HfO_2 films by metalorganic chemical vapor deposition (MOCVD) using high purity tetrakis-diethylamido-hafnium (TDEAH: $Hf(NEt_2)_4$) as a Hf precursor for the first time. TDEAH is a stable liquid at room temperature. Its vapor pressure is moderate enough for the CVD process. Here, it was vaporized by a bubbling system. The HfO_2 films were deposited with and without diluted oxygen supply. Typical substrate temperatures, carrier gas (N_2) flow rate, and oxidant gas (O_2 diluted by N_2: 1%) flow rate were 300-500°C, 40 sccm, and 0-100 sccm. The composition of the HfO_2 films deposited without O_2 supply was almost stoichiometric due to the residual O_2 gas (base pressure: $< 2 \times 10^{-6}$ Torr). However, these films contained many C and N contaminants. The C contamination severely increased at the substrate temperature of 500°C, which might originate from the ethyl radicals generated by the decomposition of TDEAH. The concentrations of both C and N were significantly reduced by increasing the pressure during deposition or by increasing the oxygen flow rate. We assume the O_2 atoms reacted preferentially with Hf-N bonds in the TDEAH and consequently contributed to the reduction of the C and N concentration in the film. We believe, therefore, TDEAH is useful as a precursor for HfO_2 film deposition, even though the TDEAH molecule contains C and N.

11:15 AM K1.9
ULTRATHIN GADOLINIUM SILICATE GATE DIELECTRIC FILMS ON SILICON. James Gupta, Dolf Landheer, John McCaffrey, Irwin Sproule, Institute for Microstructural Sciences, National Research Council of Canada, Ottawa, CANADA; William Lennard, Dept of Physics and Astronomy, The University of Western Ontario, London, CANADA.

$GdSi_xO_y$ gate dielectric films were deposited on Si(001) substrates using ultrahigh vacuum electron-beam evaporation from pressed-powder targets. Transmission electron microscopy (TEM) showed that the films were amorphous as-deposited and remained amorphous when annealed to temperatures up to 900°C. Alloy compositions were determined by $in-situ$ X-Ray photoelectron emission spectroscopy (XPS), Auger depth profiling and Rutherford backscattering spectrometry (RBS). Film thicknesses were determined by X-Ray reflectivity and TEM. The bonding chemistry and composition of the films were consistent with $Gd_2(SiO_4)O$ oxyorthosilicates. XPS results showed that, due to their highly electropositive character, the Gd atoms donate charge to the orthosilicate tetrahedra, which increases the O $1s$:Si $2p$ XPS peak spacings relative to those measured in SiO_2. Capacitance-voltage analysis of $Au/GdSi_xO_y/Si$ structures indicate an equivalent oxide thickness (EOT) of 13.4 Å for a $GdSi_{0.56}O_{2.59}$ film. The same film has a low leakage current of approximately 8.7×10^{-3} Acm^{-2} at +1 V, a reduction of 5.9×10^3 compared to current density estimates of SiO_2 films with the same specific capacitance. Post-metallization forming gas anneals reduce the leakage further, to a net reduction of 8.7×10^4, at a physical thickness of 45 Å and EOT of 11.0 Å.

11:30 AM K1.10
INTERFACE REACTIONS DURING GROUP III (Al, Y) HIGH-k OXIDE AND SILICATE DEPOSITION ON SILICON. G.N. Parsons, D. Niu and M.J. Kelly, Dept. of Chemical Engineering, North Carolina State University, Raleigh, NC.

Unwanted interface layers often result when high-k dielectric materials (including , HfO_2, ZrO_2, Al_2O_3, Y_2O_3, and metal silicates) are deposited on silicon, where unwanted reactions consume the silicon substrate. For many of the high-k materials of interest, the interface layers are not expected from simple bulk equilibrium thermodynamics, but rather, result from the non-equilibrium nature of deposition reactions. This indicates that the relative rates of individual elementary reaction steps, and their relation to deposition time and temperature, determine the composition and structure at the interface. Silicon pre-oxidation and nitridation can enable controlled interface structure, but these layers decrease capacitance and are typically not sufficient to completely stop silicon consumption reactions. Using ex-situ XPS, IR, MEIS, IV and CV analysis, we have studied and compared interface reactions when thin layers of group III and group IV metals (Al, Y, Zr) are deposited on clean silicon, in-situ oxidized silicon, and in-situ nitrided silicon. We find that the interface oxidation and nitridation slows silicon consumption during oxidation of deposited yttrium or zirconium, but for both cases, the metal reacts with oxygen and silicon to form a mixed oxide (i.e. silicate) structure. Controlled oxidation can enable structures with equivalent oxide thicknesses of $\sim 10\AA$ with leakage current less than 0.5 A/cm^2 at 1V. XPS analysis of thin ($<40\AA$ physical thickness) Y and Zr silicate layers before and after annealing at >900°C in Ar indicates that the Y silicate structure does not substantially change, consistent with other reports of enhanced stability of group III silicate films. Initial studies of gate metal reactions with group III and IV metal oxides will also be discussed.

SESSION K2: PROCESSING OF HIGH-k GATE DIELECTRICS

Chairs: Stephen A. Campbell and Ran Liu
Tuesday Afternoon, April 17, 2001
Golden Gate C2 (Marriott)

1:30 PM *K2.1
CHALLENGES IN INTEGRATING HIGH-k GATE DIELECTRIC FILM TO THE CONVENTIONAL CMOS PROCESS IN A PRODUCTION FAB. Avinash Agarwal, Michael Freiler, Loyd Perrymore, Chris Sparks, Bill Bowers, Pat Lysaght, Georgia Dempsey, Bill Nguyen, Renate Bergmann, Jae E. Lim, Will Chism, Steven Lin, Jerry Chen, Bob Murto, Howard R. Huff, International Sematech, Austin TX; Eric Shero, ASM America, Phoenix, AZ.

Continued scaling of MOSFET is likely to require replacing SiOxNy

gate dielectric with a high-k film as early as the 100 or 70 nm technology nodes in some high performance and low power applications. ZrO_2 and it's alloys with SiO_2 are currently among the leading candidates for high K gate dielectric application. We have integrated ALCVD deposited ZrO_2 with the industry standard conventional MOSFET process flow with poly Si electrode. The integrated high-k gate stack in a conventional transistor flow should not only meet all the performance requirements of scaled transistors, but the gate dielectric film should be able withstand high temperature anneal steps. The impact of different source/drain (S/D) anneal temperatures on the key transistor properties as well as high K gate stack stability was characterized. ZrO_2 was found to start reacting with poly Si electrode at 850°C and higher temperatures. However, lowering the S/D anneal temperature was found to degrade the poly Si sheet resistance, transconductance and saturation current significantly. Since the impact of contamination by these new materials introduced in a production fab is not yet established, it becomes very critical to prevent cross-contamination of process tools in the fab. Various wet chemistries were evaluated for removing high K film inadverdently deposited on wafer backside and it was found that ZrO_2 etches very slowly with etch rates as low as 0.5 nm/min in 10:1 HF and 1.2 nm/min in hot H_3PO_4. A new clean recipe using a sequence of hot HF and HNO_3 was developed which was able to lower Zr contamination on the wafer backside to as low as 1.8 E10 /cm^2. The patterning of a high-k gate stack with poly Si electrode is another area that requires considerable focus and evaluation of new dry as well as wet etch chemistries for ZrO_2 to be able to form the transistor structure successfully. Poly Si gate over ZrO_2 gate dielectric film was successfully patterned using the standard poly Si gate etch for the main etch followed by a F based chemistry for clearing the majority of the ZrO_2 remaining over the S/D area. HF based wet clean was used to remove the remaining ZrO_2 and final interfacial layer between the ZrO_2 film and the Si substrate. Electrical test results of the high K transistors will be compared to the baseline SiOxNy transistor performance.

2:00 PM K2.2
ENGINEERED TANTALUM ALUMINATE AND HAFNIUM ALUMINATE ALD FILMS FOR ULTRATHIN DIELECTRIC FILMS WITH IMPROVED ELECTRICAL AND THERMAL PROPERTIES.
Robert B. Clark-Phelps, Anuranjan Srivastava, Lance Cleveland, Thomas E. Seidel, and Ofer Sneh, Genus, Inc., Sunnyvale, CA.

Continued scaling of device dimensions requires deposition of high-quality thin films with a thickness of 50 angstroms or less. Nucleation effects in typical CVD processes make it difficult to achieve continuous films in this thickness regime. Atomic layer deposition (ALD), a technique developed over 25 years ago but applied to IC processing only recently, enables deposition of ultra-thin films with atomic-scale precision. This technique offers 100 per cent step coverage of high aspect ratio features, as-deposited films which are amorphous and free of pinholes, excellent within-wafer uniformity and wafer-to-wafer uniformity, and favorable electrical properties. Moreover, ALD offers the opportunity to engineer material properties by creating layered structures (nanolaminates) and mixtures (alloys) which combine advantageous properties of different materials. These last features may be critical in efforts to replace silicon dioxide as the industrys dielectric workhorse if no single material emerges as a suitable direct replacement. The nanolaminate capability of ALD will be discussed with physical and electrical data on nanolaminates of aluminum oxide with tantalum pentoxide and aluminum oxide with hafnium oxide. Individual nanolaminate layers can be varied from tens of angstroms to as little as 1-2 atomic layers. Data for AlO_x/TaO_x and AlO_x/HfO_x alloys will also be presented demonstrating the ability to create materials with controlled, variable composition. The alloy and nanolaminate capabilities enable the creation of graded interfaces and atomically smooth transitions between different materials. Prospects for application of these materials to gate stacks and capacitors will be assessed.

2:15 PM K2.3
HIGH-k OXIDE GATE STACKS ON SILICON INCORPORATING UHV SILICON NITRIDE INTERFACIAL LAYERS.
Mark A. Shriver, Ann M. Gabrys, T.K. Higman, S.A. Campbell, University of Minnesota, Department of Electrical and Computer Engineering, Minneapolis, MN.

In order to meet the semiconductor industry's performance road-maps, future MOSFET devices must have an equivalent oxide thickness less than 1 nm. Current high permittivity (high-k) material deposition techniques produce a low-permittivity SiO2 interfacial layer which consequently increases the equivalent oxide thickness, in many cases making 1nm an impossibility. In an effort to improve the interface between high-k dielectrics and a silicon substrate we have proposed forming a thin interfacial layer of Si3N4 under ultra-high vacuum (UHV) conditions. This interfacial nitride layer must also have a low interface state density for use in high-performance MOSFET's. The nitride layer in this study is formed by lamp heating in ammonia gas which forms a very uniform, self-limiting film. Gate stacks were produced by first growing an Si3N4 film under UHV and then transferring the sample in-situ to an adjoining CVD system where a high-k dielectric layer (in this case HfO2) was deposited. After forming capacitors from these films, capacitance vs. voltage (C-V) techniques were used to determine the interface state density and equivalent oxide thickness of the films. Gate stack films were produced on Si(100) and Si(111) and the results were compared. Capacitors made from these gate stacks show a minimal stretchout in the high frequency C-V, indicative of a low overall interface state density. Low frequency C-V mesurements suggest that most of these interface states are clustered near the band edges for both n- and p-type substrates with a comparatively small number in the mid-gap region. The data indicates that capacitors made from gate stacks deposited on Si(111) have a lower overall interface state density than the Si(100) gate stacks when the nitride layer is included as an interfacial layer beteen the silicon and the high-k material.

2:30 PM K2.4
ALTERNATING LAYER CHEMICAL VAPOR DEPOSITION (ALCVD) OF METAL SILICATES FOR GATE INSULATORS.
Roy G. Gordon, Jill Becker, Dennis Hausmann and Seigi Suh, Harvard Univ, Dept of Chemistry and Chemical Biology, Harvard Univ, Cambridge, MA.

A new process was developed for ALCVD of silicates of metals such as lanthanum, yttrium, zirconium and hafnium at low substrate temperatures (200-300°C). The silicon and oxygen source is tris(tert-butoxy)silanol, $(^tBuO)_3SiOH$, and the metal precusors are metal amides. A typical reaction is $ZrL_4 + (^tBuO)_3SiOH \rightarrow ZrSiO_4 + 2\ HL + 3\ H_2C{=}C(CH_3)_2 + 2\ CH_3N{=}CHCH_3$ in which the ligand L is ethylmethylamide, -NEtMe. The precursor vapors were alternately pulsed into a heated reactor. A monolayer of the metal compound is chemisorbed onto a hydroxyl-terminated surface by the self-limiting reaction $2\ *\text{-}OH + ZrL_4 \rightarrow (*\text{-}O)_2ZrL_2 + 2\ HL$ in which some of the ligands desorb as amine vapor. The remaining ligands then desorb as imine vapor after a β-hydrogen shift: $(*\text{-}O)_2ZrL_2 \rightarrow (*\text{-}O)_2ZrH_2 + CH_3N{=}CHCH_3$ The next pulse of silanol precursor is chemisorbed to this surface by the self-limiting reaction $(^tBuO)_3SiOH + (*\text{-}O)_2ZrH_2 \rightarrow (*\text{-}O)_2ZrH(OSi(^tBuO)_3) + H_2$ Then the tert-butyl groups detach by β-hydrogen elimination to give surface hydroxyl groups and gaseous isobutene: $(*\text{-}O)_2ZrH(OSi(^tBuO)_3) \rightarrow (*\text{-}O)_2ZrH(OSi(OH)_3) + 3\ H_2C{=}C(CH_3)_2$ The remaining hydrogen attached to the metal is eliminated by condensation with a neighboring hydroxyl, leaving two surface hydroxyls on each silicon. $(*\text{-}O)_2ZrH(OSi(OH)_3) \rightarrow (*\text{-}O)_2ZrO_2Si(OH)_2 + H_2$ These two hydroxyls are ready to react with another zirconium precursor molecule, to start the cycle again. Each cycle of these reactions adds about 0.3 nm to the thickness of the film. Similar reactions were used to deposit silicates of hafnium, yttrium and lanthanum. The thickness uniformity and conformality of these films are excellent, because of the self-limiting nature of the surface reactions. Film compositions, measured by Rutherford Backscattering Spectroscopy, showed silicon/metal ratios slightly greater than unity. The interfaces between the films and the silicon substrate remain sharp because of the non-oxidizing and low-temperature conditions used. The films are amorphous. Electrical properties of the films will be reported.

2:45 PM K2.5
PREPARATION OF NOVEL LANTHANUM OXIDE GATE DIELECTRICS BY METALORGANIC CHEMICAL VAPOR DEPOSITION.
Chae Hyun Wang, Dong Jin Won, Jin Hyung Jun, Young Jin Lee, Doo Jin Choi, Dept. of Ceramic Engineering, Yonsei University, Seoul, SOUTH KOREA.

La_2O_3 is an attractive material, which has high permittivity and thermodynamic stability in contact with Si. We investigated the possibility of La_2O_3 film as an alternative gate dielectric for advanced CMOS applications. La_2O_3 thin films were successfully grown directly on Si by metalorganic chemical vapor deposition (MOCVD) at the temperature from 350°C to 600°C, using new precursor of $La(tmhd)_3$ with tetraglyme adduct as a source precursor. The functions of the tetraglyme is to fill the coordination sites on the lanthanum and produce a more monomeric species with a lower sublimation temperature compared to $La(tmhd)_3$. Growth and structural properties of La_2O_3 films have been studied using x-ray diffraction, ellipsometery, atomic force microscopy, and x-ray photoelectron microscopy. Growth kinetics was controlled by the surface reaction in the low temperature region up to 500°C, which shows apparent activation energy of about 1.0kcal/mol. Structure of as-grown films at 350°C changed from amorphous to polycrystalline of cubic and hexagonal with increasing the deposition and post annealing temperature. Post annealing process was conducted at the temperature from 600°C to 900°C in N_2 and O_2 atmosphere for the improvement of electrical properties. Electrical properties of as-grown films and annealed films have been characterized by

capacitance-voltage (C-V) and current-voltage (I-V) measurements. Dielectric constant of 10∼30 were obtained by high frequency C-V measurement for the films of 30∼50nm thickness. I-V measurements show leakage current of 4.3×10^{-6} and 1.4×10^{-7} A/cm^2 at 1MV/cm for the as-grown and annealed films, respectively.

3:30 PM K2.6
TANTALUM-ALUMINUM OXIDE: A REPLACEMENT HIGH-k GATE DIELECTRIC FOR THERMALLY-GROWN SILICON DIOXIDE. Robert Johnson, Joon Goo Hong, Gerald Lucovsky, NC State Univ, Dept of Physics, Raleigh, NC.

In an effort to increase the effective crystallization temperature of replacement gate dielectrics, and reduce interfacial fixed charge, aluminum and tantalum oxide alloys have been prepared by remote plasma enhanced chemical vapor deposition. This paper reports studies of chemical, structural, and physical properties, and performance in metal-oxide-semiconductor capacitors. Metal-organic precursors were delivered from separate bubblers, mixed and injected down stream from the plasma excitation region of a remote plasma reactor. The reaction was driven by a plasma-excited oxygen-helium mixture. The initial stages of deposition were monitored by on-line Auger electron spectroscopy, AES. The relative intensities of substrate silicon and interfacial silicon oxide features indicated less than about 0.5 nm of interfacial silicon oxide was formed during the 300C deposition. The relative intensities of aluminum and tantalum features varied monotonically with respective flow ratios and the positions of AES spectral features indicated oxidation was complete, and bonding in the middle of the alloy range was qualitatively different in either end-member. This was accompanied by a systematic shift in the position the oxygen AES feature. Thick films were analyzed by FTIR. The mid-IR alloy spectra were not a compositionally weighted mixture of the end-member oxides, but instead were dominated by a broad feature that tracked between the dominant features of the end-member oxides. FTIR spectra were monitored as a function of post deposition annealing in argon at temperatures to 1000C. The effective crystallization temperature increased to 1000C for alloys in the middle of the system, exceeding the respective 800C and 900C crystallization temperatures of tantalum and aluminum oxide. The paper will present a model for the local atomic bonding, and also include data on capacitors that track a transition from negative fixed interfacial fixed charge in aluminum oxide devices to positive interfacial fixed charge in tantalum oxide devices.

3:45 PM K2.7
HIGH-k METAL OXIDE/SiO_2 STACK GATE DIELECTRIC PREPARED BY REACTION OF METAL WITH SiO_2. Jeshik Shin and Hyunsang Hwang, KJIST, Dept of MS&E, Kwangju, KOREA.

Although the high-k gate dielectric materials have been investigated as an alternative to conventional SiO_2 gate dielectrics, the instability of these high-k materials on silicon substrate at high temperature causes serious problems. A unique process for the preparation of high permittivity metal oxide by direct thermal reaction of metal on SiO_2 is described. Using a high temperature reaction between SiO_2 and a reactive metal such as Ti and Ta, a high-k metal oxide/SiO_2 stack structure can be formed. Compared with conventional reactive sputter deposited metal oxide, samples prepared by this new process exhibit excellent electrical characteristics, including high capacitance, a low leakage current, and a very low interface state density. In addition, the electrical characteristics of metal/oxynitride stack are superior to that of a metal/oxide stack. The improvement of electrical characteristics of metal/oxynitride stack can be explained by less metal penetration through the oxynitride layer which was confirmed by transmission electron microscopy (TEM) and energy dispersive x-ray (EDX) analysis. By optimizing the process conditions, we were able to prepare a capacitor with a CET as thin as 1.5nm, a leakage current less than 1A/cm^2 at -1.5V, and an excellent interface state density as low as 1x10^{11} /cm^2-eV.

4:00 PM K2.8
CONTROL OF INTERFACE REACTIONS IN GATE STACKS BASED ON ZrO_2. M.A. Gribelyuk, IBM Microelectronics, Hopewell Junction, NY; E.P. Gusev, M. Copel, S. Callegari, D.A. Buchanan, IBM T. J. Watson Research Center, Yorktown Heights, NY.

Thermal stability presents one of the major challenges in implementation of novel high-k gate dielectrics in future CMOS devices. We have used high resolution TEM in combination with image simulations to determine the mechanism of the ZrO_2-Si reaction. The as-grown ZrO_2 film deposited at T= 300°C by ALCVD is crystalline. Both orthorhombic and monoclinic modifications coexist in the film. It was found that crystalline ZrSi and $ZrSi_2$ based structures are formed as result of the T= 1000°C anneal. The above structures show nearly epitaxial relationship to Si {100}. The reaction leads to severe roughening of Si surface and formation of islands of reaction products. No silicates were observed. However, thermal stability can be substantially improved if smart interlayers with moderate dielectric properties are placed between Si and ZrO_2. We show that in this case the gate dielectric stack Si/interlayer/ZrO_2/poly-Si shows stability up to T= 1000°C. Very limited reaction has been observed at both interfaces ZrO_2/Si and ZrO_2/poly-Si. Our results suggest a promise of successful integration of ZrO_2 as the new gate dielectric material in the future deep submicron CMOS devices.

4:15 PM K2.9
ATOMIC-SCALE CHARACTERIZATION OF HIGH-k GATE STACKS. D.A. Muller, G. Wilk, J. Kwo, M. Hong, Bell Labs, Lucent Technologies, Murray Hill, NJ.

We apply atomic-scale electron energy loss spectroscopy (EELS) to obtain direct evidence of the interfacial structures of potential high-k gate materials, including silicates and rare-earth oxides. The spectroscopy provides spatially resolved chemical and bonding information at buried interfaces for both as-grown and processed films, which sheds light on the interfacial electronic structure and cation distributions. The common processing problems of oxygen diffusion through high-k stacks to form interfacial oxides and silicates, as well as reactions with the gate electrode (especially for Al, TiN and Si) can be unambiguously identified, even in nanotransistors. Using the model (and still relevant) system of Si-SiO_2 interfaces, we illustrate how the electronic structure evolves gradually over 3-5 angstroms, even when the interface is chemically abrupt. While this places a fundamental limit on the thickness of SiO_2 gate oxides, it has also proved beneficial in designing high-k replacements, which must obey similar constraints.

4:30 PM K2.10
CHARACTERIZATION OF TiO_2 FILMS GROWN AT LOW TEMPERATURES FOR ALTERNATIVE GATE DIELECTRIC APPLICATION. Jun-Ying Zhang, Ian W. Boyd, Electronic & Electrical Engineering, University College London, London, UNITED KINGDOM.

Photo-induced chemical vapor deposited titanium oxide film is one of the most promising candidates for ultrathin gate insulators in the future CMOS technologies. In this paper we report the growth of thin titanium oxide films on Si (100) and quartz at low temperatures (*350°C) by photo-induced chemical vapor deposition (photo-CVD) with 222 nm UV radiation using a novel injection liquid source, which overcomes the reproducible problem in conventional bubblers. The properties of the films formed have been studied using ellipsometry, UV spectrophotometry and Fourier transform infrared spectroscopy (FTIR) measurements. Nanostructured films on Si wafer were observed by atomic force microscopy (AFM). It was found that crystalline TiO_2 films could be formed at deposition temperatures as low as 210°C by x-ray diffraction (XRD). The influence of the deposition temperature on the film is discussed. The refractive index as high as 2.5 can be obtained at a deposition temperature of 350°C, while an optical transmittance of between 85-90% in the visible region of the spectrum was obtained at different deposition temperatures. Physical and optical characterization both reveal good film qualities, rending this technique promising for a wide range of industrial application in low temperature microelectronic and optoelectronic material processing as well as for many heat sensitive compounds.

4:45 PM K2.11
PHASE DIAGRAM SIMULATIONS IN AMORPHOUS METAL SILICATE SYSTEMS. Hyoungsub Kim, Paul C. McIntyre, Stanford Univ, Dept of MS&E, Stanford, CA; Krishina Saraswat, Stanford Univ, Dept of Electrical Engineering, Stanford, CA.

As MOS transistor size decreases and higher speeds are required, the gate oxide must be aggressively decreased down to 1.5 nm for a 0.1 μm channel length transistor. However, as the thickness of SiO_2 decreases, the leakage current across the dielectric increases enormously through direct tunneling. At present, in order to reduce the leakage current, high-k materials, including ZrO_2 and Zr-silicate, have been widely investigated because they offer the opportunity to scale device dimensions further, while retaining sufficient physical thickness of the dielectric to avoid direct tunneling. During high temperature annealing of amorphous Zr- and Hf-silicate films, it has been suggested that the silicate layer decomposes into ZrO_2 rich and SiO_2 rich regions. This phase separation may occur by either a nucleation and growth process or by spinodal decomposition (a diffusional phase separation by local concentration fluctuations). In this presentation, we report a thermodynamic analysis of bulk $ZrO_2$2-SiO_2 phase equilibria, in which we investigate the possibility of spinodal decomposition for an amorphous silicate that is modeled as a super-cooled liquid solution. Based on published ZrO_2-SiO_2 phase diagrams, a "sub-regular model" was used for the excess free energy of mixing and measured invariant points were adopted for this simulation. The resulting calculated phase diagram matches the experimental results reasonably well, and possible composition range

of decomposition was calculated at typical processing temperatures from 500°C to 1200°C. Results of similar thermodynamic analyses are also reported for other metal silicate systems.

SESSION K3: POSTER SESSION
GATE STACK AND SILICIDE ISSUES IN Si PROCESSING II
Chairs: Stephen A. Campbell and Christopher C. Hobbs
Tuesday Evening, April 17, 2001
8:00 PM
Salon 1-7 (Marriott)

K3.1
PROMISING GATE STACK WITH Ru & RuO_2 GATE ELECTRODES AND Y_2O_3 GATE DIELECTRIC. Huicai Zhong, Greg Heuss and Veena Misra, Department of Electrical Engineering, North Carolina State University, Raleigh, NC; Jason Kelly, Greg Parson Department of Chemical Engineering, North Carolina State University, Raleigh, NC.

Aggressive scaling of CMOS technology makes the evaluation of high-conductivity metal gate and alternative gate dielectrics becomes important. High conductivity and excellent thermal stability are required to decrease gate depletion effect and improve interface between gate electrode and dielectrics. In the meanwhile, gate dielectric materials having high dielectric constant, low leakage current, good thermal stability, interface characteristics comparable to Si-SiO_2 are needed as alternative dielectrics. Ru(Ruthenium) and RuO_2 are attractive gate electrodes because of large workfunction(~5eV), low resistivity and excellent thermal/chemical stability. Our recent work has shown that RuO_2 films on SiO_2 and ZrO_2 at high temperatures produce excellent electrical characteristics with good thermal stability. In this work, we have studied the electrical and thermal stability of Ru and RuO_2 electrode on Y_2O_3 dielectrics in contrast with ZrO_2 dielectric. Very low resistivity Ru and rutile stoichiometric RuO_2, deposited via reactive sputtering, were evaluated as gate electrodes on ultrathin Y_2O_3 (~2.4nm) films for Si-PMOS devices. Thermal and chemical stability of the electrodes was studied at annealing temperatures up to 800°C in N_2 and subsequently forming gas annealing. XRD and XPS were measured to study grain structure and interface reactions. Electrical properties were evaluated via MOS capacitors. The role of oxygen inside Y_2O_3 dielectrics was studied by comparing EOT change as a function of annealing temperature for capacitors with Y_2O_3 and ZrO_2 dielectrics. For capacitors with Ru gate on ZrO_2 and Y_2O_3 films, excellent stability of equivalent oxide thickness was detected. Flatband voltage and gate current as a function of annealing temperature were also studied. It is found that capacitors with Y_2O_3 having much less positive flatband voltage shift after high-temperature annealing. This indicates that Ru and RuO_2 on Y_2O_3 dielectric is a promising gate stack for P-MOSFETs.

K3.2
PRELIMINARY FIRST PRINCIPLES STUDY OF HAFNIUM AND ZIRCONIUM ALUMINATES AS REPLACEMENT HIGH-k DIELECTRICS. Michael Haverty, Gyuchang Jun, Stanford Univ, Dept of MS&E, Stanford, CA; Atsushi Kawamoto, Stanford Univ, Dept of Electrical Engineering, Stanford, CA; Kyeongjae Cho, Stanford Univ, Dept of Mechanical Engineering, Stanford, CA.

Density Functional Theory calculations may be used to study the energetic and electrical properties of novel materials prior to fabrication to hasten the process of research and development. This study focuses on calculations of the substitution of Hf and Zr atoms into bulk κ-Al_2O_3. This crystalline form of alumina contains both tetrahedral and octahedral Al sites as in amorphous Al_2O_3 thin films. The first part of the study explores the strain energy introduced by the substitution of the Hf and Zr atoms for Al in bulk κ-alumina. Next, the relaxed structure of a stack of κ-Al_2O_3 | 6 $\AA$ SiO_2 | Si(100) substrate is studied. The effects of Hf and Zr substitution for the Al atoms in this interfacial structure are also investigated.

K3.3
UV OZONE GROWTH AND STRUCTURE-PROPERTY RELATIONS IN ULTRA-THIN ZrO_2 DIELECTRICS. Shriram Ramanathan, Paul McIntyre, Stanford University, Dept. of MS&E, Stanford, CA; Carl Maggiore, Los Alamos National Laboratory, Los Alamos, NM; Glen Wilk, David Muller, Bell Laboratories, Lucent Technologies, Murray Hill, NJ.

At present, there is great effort to synthesize and characterize new materials that might replace SiO_2 as the gate dielectric in MOS devices. Zirconium oxide is considered to be a potential replacement owing to its relatively high dielectric constant and stability with respect to solid state reaction with Si. However, much work remains to be done in growing thin oxide films with good structural and electrical properties. In this work, we report on the growth of thin ZrO_2 films by UV-Ozone oxidation. This oxidation process is performed by exposing a thin Zr film (grown by UHV sputtering onto an oxide or oxynitride-passivated Si surface) to oxygen in presence of UV light. The light interacts with oxygen gas to form oxygen radicals and ozone, which significantly enhance the kinetics of oxidation. It is important to study the kinetics of oxidation to control the growth of these films. Quantitative measurements of the oxide thickness have been performed using the technique of nuclear reaction analysis. The oxidation was found to follow a logarithmic rate law and showed significant dependence on oxygen pressure. To study the structural and chemical properties of the interface between the dielectric and the substrate at atomic resolution, detailed analyses have been performed using a scanning transmission electron microscope. The results reveal a conformal ZrO_2 film, however the interface between the ZrO_2 and the underlayer is found to be slightly diffuse from quantitative electron energy loss spectroscopy studies. We have also made MOS capacitors with these films to measure the I-V and C-V properties. The electrical properties of these devices will be discussed in detail with correlation to the film microstructure.

K3.4
CHARACTERISTICS OF $TaN_x/ZrO_2/SiO_2/Si$ MOS STRUCTURES. Dae-Gyu Park, Kwan-Yong Lim, Heung-Jae Cho, Tae-Ho Cha, Jae-Young Kim, In-Seok Yeo and Jin Won Park, Hyundai Electronics Industries Company Ltd., Advanced Process Team, Memory Research and Development Division, KOREA; Henk de Waard, ASM America, Marko Tuominen, ASM Microchemistry, FINLAND.

We report the characteristics of TaNx/ZrO2/SiO2/Si metal-oxide-semiconductor (MOS) capacitors. Interfacial SiO2 (~ 0.7 nm) was rapid thermally grown in dry O2 and ZrO2 (4-10 nm) was prepared by atomic layer chemical vapor deposition (ALCVD). Then, the metal gate electrode TaNx (50 nm) was deposited by reactive sputtering at room temperature, followed by photolithography and reactive ion etching. The flatband voltage (Vfb) and capacitance equivalent thickness (CET) of TaNx/ZrO2(8nm)/SiO2/p-Si nMOS capacitor is 0.61V and 1.9 nm, respectively. The Vfb and CET of TaNx/ZrO2(10nm)/SiO2/n-Si pMOS capacitor is 0.21 V and 2.5 nm, espectively. It appears that the work function of TaNx gate electrode is suitable for low power nMOSFET application. The gate leakage current of TaNx/ZrO2/SiO2/p-Si nMOS capacitor having the CET of 1.7 nm and 1.9 nm is -4E-5 A/cm2 and < -1E-7 A/cm2 at -1 V. The interface state density and reliability characteristics of TaNx/ZrO2/SiO2/Si MOS structure with post metal anneal will be discussed. We would appreciate Mervi Linnermo of ASM Microchemistry for the ALCVD deposition.

K3.5
CHARACTERIZATION OF THIN HAFNIUM DIOXIDE DEPOSITED BY CVD. Rich Gregory, Peter Fejes, Ran Liu, Stefan Zollner, Mark Wagner, Vidya Kaushik, Bich-Yen Nguyen, Motorola Inc., Materials and Structures Laboratories, Mesa, AZ.

Hafnium dioxide (hafnia, HfO_2) is a tetravalent transition metal oxide under consideration as a medium-k replacement for the current gate dielectric SiO_2 in a standard CMOS processing scheme (poly-Si gate, implant doping, dopant activation anneal). Hafnia has potential advantage over other metal oxides because it does not react with the poly-Si gate during the dopant anneal to form a silicide. Five HfO_2 films were grown by CVD at 550°C for different times (20, 40, 60, 120, and 240 seconds). These films have been characterized by SE, RBS, XRD, and TEM for the purpose of determining the growth rate and the crystal structure for different thicknesses. RBS indicates stoichiometric HfO_2 for all films in the series. Thus, from these data and SE, one derives a deposition rate of approximately 3$\AA$ per second at 550°C. XRD θ-2θ scans reveal monoclinic structure for all films including the 20-second-deposited film (62$\AA$ thick). However, these data show evidence of changing texture as deposition times go from very short to very long. TEM cross sections of the thinnest film reveal d-spacings corresponding to monoclinic HfO_2 [-1 1 -1] spacing of 2.825$\AA$ and monoclinic HfO_2 [1 1 -1] spacing of 3.145$\AA$. Some of the TEM images show material composed of overlapping crystallites. This observation seems to corroborate the XRD data that show changes in texture over the range of deposition times. Issues of concern include possible diffusion of Hf into underlying Si, but RBS spectra indicate no such occurrence.

K3.6
FORMATION OF RELIABLE W/POLY-Si GATE ELECTRODE BY NH_3 ANNEALING FOR THE APPLICATION OF 0.10μm MOSFET AND BEYOND. Chang Hee Han, Min Soo Park, Ji-Soo Park, Yun Seok Chun, Moon-Sig Joo, Hyeon-Soo Kim, and Jin Won Park Advanced process Development Dept. 3, Memory R&D, Hyundai Electronics Industries Co., Ltd, Ichon-si, Kyoungki-do, KOREA.

In this paper, we studied an NH_3 annealing for the barrier formation

process of W/poly-Si gate instead of the deposition of barrier layer. The chemical and physical properties of barrier layer formed by NH_3 annealing were investigated. We evaluated the properties of ammonia treated W/poly-Si gate as a gate electrode and characterized 0.10μm CMOS device with it. We deposited 70nm-thick W films on poly-Si film without any barrier layer such as TiN, TaN, WNx etc and annealed them above 600°C in Ar, N_2, and NH_3 ambient. Ar and N_2 annealing caused the formation of tungsten silicide and micro void at the W/poly-Si interface, while NH_3 annealing kept sharp interface between W and poly-Si. In terms of thermodynamics, W is natural to react with Si to form WSix above 600°C unless they were isolated by barrier layer. About 20Å-thick layer was observed in NH_3 annealed samples by TEM analysis. SIMS and XPS analysis revealed that it was composed of W and Si-N bond. This layer is thought to block the silicidation of W operating as barrier layer. NH_3 annealed W/poly films were stable up to the elevated temperature of 1000°C. Ammonia annealed W/poly-Si gate showed low sheet resistance below 4Ω/sq. at a line width of 0.10 μm after the post annealing at 850°C for 70 min. 0.10μm CMOS device with NH_3 annealed W/poly-Si gate showed good device performance. In this work, It is found that an annealing of W film on poly-Si in an NH_3 ambient resulted in formation of low resistivity W and highly reliable in-situ formed barrier layer, simultaneously. This NH_3 annealed W/poly-Si gate was acceptable to apply to 0.10 μm CMOS device and beyond.

K3.7
EFFECT OF PRE-COOLING TREATMENT ON THE FORMATION OF C54 PHASE TITANIUM SILICIDE. Lin Zhang, Yong Keun Lee, Nanyang Technological Univ, School of Materials Engineering, SINGAPORE.

In this paper, the effect of pre-cooling treatment on the low resistivity C54 phase titanium silicide film growth was investigated. Our experimental results and micro-structural analysis show that, by introducing such cooling treatment into the titanium silicide process to precede the conventional rapid thermal annealing, the low resistivity C54 phase formation can be enhanced. Defects at the Si/Ti interface caused by the thermal mismatch between titanium and silicion layers during the cooling treatment were found to contribute to the increase of the C49 nucleus sites. This help to supply more C49 grain boundaries and tripple junction sites at which the C54 phase could nucleate. Our discovery has the potential to reduce the complexity and cost associate with forming low resistivity titanium silicide on sub-micron structures for future ULSI application.

K3.8
ULTRA-THIN UNIFORM NICKEL MONO SILICIDE PREPARED BY A DC-SPUTTER. Youngsuk Ahn, Ohsung Song, The Univ. Seoul, Dept of Materials Science and Engineering, Seoul, KOREA.

New silicide materials with low resistivity and thickness uniformity are required to enhance the speed of MOSFETs (metal oxide semiconductor field effect transistors), as semiconductor devices are integrated with the shorter the channel length even to 0.10. Nickel monosilicide (NiSi) is a promising candidate because it doesn't show any increase of resistivity even when the line width was under 0.10. In addition to, NiSi is comfortable to the shallow junction transistors, as it is created by one nickel atom and one silicon atom. However it is not well understood that stability and microstructure evolution of nickel silicides with silicidation temperatures. In this study, we prepared nickel silicides on the 4° $\gg$ p-Si(100) wafer by using a dc-sputter in the temperature range of 200-1000°. The electrical and microstructure changes were measured with the silicidation temperatures. Electrical properties of the materials at each silicidation temperature were measured by a four-point probe. Microstructure was executed by a cross-sectional TEM (transmission electron microscope). Surface roughness of each specimen was measured by a SPM (scanning probe microscope). We confirmed that stable NiSi formed with the lowest sheet resistivity below 2/ in the range of 400-700° through the four point measurement. HR-TEM showed that 150°10-thick uniform NiSi layer was formed at the silicidation temperatures of 400 700°. We observed a uniform unidentified 10°-thick amorphous layer, natural SiO2 layer, at top of NiSi layers. The existence of amorphous layer seems to help to form uniform NiSi layers. SPM reveals that the surface roughness changes abruptly while phase transformation from NiSi to NiSi2. Based on our SPM result, SPM roughness may be effective as the in-line monitoring to confirm the stable Ni silicide phase with silicidation temperatures. As the summary, we prepared uniform of 150°-thick planar NiSi which can be employed to 0.10 class MOSFET devices.

SESSION K4: ELECTRICAL PERFORMANCE OF NOVEL GATE DIELECTRICS
Chairs: David A. Muller and Michael A. Gribelyuk
Wednesday Morning, April 18, 2001
Golden Gate C2 (Marriott)

8:30 AM *K4.1
CHEMICAL VAPOR DEPOSITION OF AMORPHOUS FILMS OF TITANIA, ZIRCONIA OR HAFNIA ALLOYED WITH SILICA. Wayne L. Gladfelter, Ryan C. Smith, Charles J. Taylor, Jeffrey T. Roberts, University of Minnesota, Dept of Chemistry, Minneapolis, MN; Noel Hoilien, Stephen A. Campbell, University of Minnesota, Dept of Electrical and Computer Engineering, Minneapolis, MN; Mike Tiner, Rama Hegde, Christopher Hobbs, Motorola Advanced Products Research and Development Lab, Austin, TX.

The electrical properties, as measured by dielectric constant and leakage current characteristics, of thin dielectric layers on silicon depend on the composition and microstructure of both the bulk film and the interface. This paper will describe our effort to reduce the impact of grain boundaries by alloying a glass-forming oxide (SiO_2) with TiO_2, ZrO_2 or HfO_2 in a chemical vapor deposition process. Amorphous thin films of composition $Ti_xSi_{1-x}O_2$ have been grown by low pressure chemical vapor deposition on silicon (100) substrates using $Si(OEt)_4$ and either $Ti(OiPr)_4$ or anhydrous $Ti(NO_3)_4$ as the sources of SiO_2 and TiO_2, respectively. The substrate temperature was varied between 300 and 535°C, and the precursor flow rates ranged from 5 to 100 sccm. Under these conditions growth rates ranging from 0.6 to 90.0 nm/min were observed. Films were amorphous to X-rays as deposited and SEM micrographs showed smooth, featureless film surfaces. Cross-sectional TEM showed no compositional inhomogeneity. RBS revealed that x (from the formula $Ti_xSi_{1-x}O_2$) was dependent upon the choice of TiO_2 precursor. For films grown using TTIP-TEOS x could be varied by systematic variation of the flow of N_2 through the precursor vessels or the deposition temperature. For the case of TN-TEOS x remained close to 0.5. The results suggested the existence of a specific chemical reaction between TN and TEOS prior to film deposition. This hypothesis was tested by reacting TEOS with a CCl_4 solution of TN at room temperature. The products were ethyl nitrate and an amorphous white powder having a Ti:Si ratio of 1.09 (based on ICP-MS analysis). Studies of the reaction of TEOS and silane with $Zr(NO_3)_4$ and $Hf(NO_3)_4$ will also be discussed. The presentation will focus on the CVD process and film characterization including measurement of the C-V and I-V characteristics of thin film capacitors.

9:00 AM K4.2
TRANSISTORS BUILT WITH ZrO_2 AND HfO_2 DEPOSITED FROM NITRATOS. Stephen A. Campbell, Noel Hoilien, Tiezhong Ma, Fang Chen, Univ of Minnesota, Dept of Electrical Engineering, Minneapolis, MN; Ryan Smith, Wayne Gladfelter, Univ of Minnesota, Dept of Chemistry, Minneapolis, MN.

Field effect transistors have been built in a non-self-aligned, gate-last process with ZrO_2 and HfO_2 as gate insulators. The ZrO_2 and HfO_2 films were grown with the carbon-free precursors, $Zr(NO_3)_4$ (ZN) and $Hf(NO_3)_4$ (HN), respectively. The films were grown at about 5 torr with the substrate heated in rapid-thermal fashion. In general, low-field mobilities for these devices fall below the universal curve while high-field mobilities exceed the universal curve. This behavior is attributed to the heavily nitrided oxide interfacial layer between the silicon substrate and the ZrO_2 or HfO_2 since such behavior is commonly reported for heavily nitrided oxides.

9:15 AM K4.3
ELECTRONIC STRUCTURE AND PROPERTIES OF TETRAHEDRAL HAFNIUM AND ZIRCONIUM SILICATES. John Jameson, Walter A. Harrison, Stanford Univ., Dept. of Applied Physics, Stanford, CA; P.B. Griffin, J.D. Plummer, Stanford Univ., Dept. of Electrical Engineering, Stanford, CA.

We investigate the electronic structure and properties of amorphous hafnium and zirconium silicates in the limit that all metal and silicon atoms are tetrahedrally bonded to four oxygen atoms. We view the material as being composed of relatively uncoupled "bonding units" with stoichiometries $MSiO_4$ (M=Hf or Zr) and $SiSiO_4$, and we develop a tight binding model to describe the electronic structure of these bonding units. Using this model, we investigate the scaling of the energy gap, optical susceptibility, and statice susceptibility of tetrahedral hafnium and zirconium silicates over the range of stoichiometries from SiO_2 to $MSiO_4$. In addition, we explore the changes in material properties that might result from applied stress or various types of impurities. Comparison to experiment is provided wherever possible.

9:30 AM K4.4
ELECTRICAL CHARACTERISTICS OF ZrO_2 PREPARED BY WET OXIDATION OF Zr LAYER. Sanghun Jeon and Hyunsang Hwang, KJIST, Dept of MS&E, Kwangju, KOREA.

As MOS devices scaled down, thermally stable high K gate dielectrics are required. Excellent electrical properties of ZrO_2 by reactive sputtering method have recently been reported. However, since

reactive sputtering in oxygen ambient causes the plasma oxidation of the silicon substrate which increases the effective oxide thickness, a surface pre-treatment and process optimization are necessary. We investigated wet oxidation of ultra-thin zirconium metal layer on Si (100). Ultra-thin zirconium layer on Si was deposited by using conventional radio frequency magnetron sputtering from Zr metal target at room temperature. Wet oxidation of zirconium metal layer was performed at temperature below 400°C. The accumulation capacitance as high as 123fF/μm^2 was observed for ZrO_2 prepared by light oxidation of Zr metal layer. However, a significant reduction in accumulation capacitance was observed with increasing frequency, especially for lightly oxidized samples. The anomalous high capacitance and dispersion characteristics can be explained by space charge polarization of metallic zirconium in zirconium oxide which was confirmed by XPS. Based on AFM analysis, a significant increase of surface roughness was observed for lightly oxidized samples which might be related to non-uniform oxidation and non-stoichiometry of ZrO_2. By optimizing process conditions to minimize dispersion characteristics, we obtained ZrO_2 with capacitance equivalent oxide thickness of 10.9$\AA$ and leakage current density less than 10mA/cm^2 at -1.5V.

9:45 AM K4.5
ELECTRICAL CHARACTERISTICS OF THERMALLY STABLE ZrO_xN_y. Sanghun Jeon, Chel-Jong Choi, Tae-Yeon Seong, and Hyunsang Hwang, JIST, Dept of MS&E, Kwangju, KOREA.

As MOS devices scaled down, thermally stable high K gate dielectrics are required. Excellent electrical properties of zirconium oxide by the process optimization has recently been reported. However, there are some potential concerns about low temperature crystallization, and the degradation of equivalent oxide thickness due to the thickness increase and the formation of silicate at high temperature. We investigated thermally stable ZrO_xN_y with ~3-5 at. % nitrogen prepared by NH_3 annealing of ZrO_2 for use in gate dielectric application. Ultra-thin zirconium oxide was deposited by means of conventional reactive sputtering. Rapid thermal nitridation was performed in an atmosphere of NH_3 at 700°C. An additional wet oxidation was performed at various temperatures. Compared with reactive sputtered ZrO_2, Compared with conventional ZrO_2, ZrO_xN_y exhibits excellent electrical characteristics such as high accumulation capacitance, low leakage current density and better thermal stability. Based on high resolution TEM analysis of both samples annealed at 800°C for 5 min, ZrO_2 was polycrystalline structure but ZrO_xN_y was amorphous structure. The improvement of electrical characteristics of ZrO_xN_y can be explained by both the reduction of trap density and better thermal stability due to the nitrogen incorporation.

10:30 AM K4.6
$TaO_xN_y/ZrSi_xO_y$ STACK GATE DIELECTRIC FOR MOS DEVICE APPLICATIONS. Hyungsuk Jung, Hyundoek Yang, Kiju Im and Hyunsang Hwang, KJIST, Dept of MS&E, Kwangju, KOREA.

We reported excellent electrical characteristics of TaO_xN_y gate dielectric on silicon substrate prepared by nitridation and reoxidation of Ta_2O_5. Although the TaO_xN_y film exhibits dielectric constants higher than 60, the interfacial SiO_2 is necessary to prevent intermixing and high interface state density problems. Recently, zirconium oxide and zirconium silicate have been investigated as alternatives to SiO_2 gate dielectrics due to high dielectric constant and their excellent thermal stability with silicon substrates. We investigated a unique process for the preparation of high quality tantalum oxynitride (TaO_xN_y) with zirconium silicate ($ZrSi_xO_y$) as an interfacial layer for use in gate dielectric applications. Compared with conventional native silicon oxide and oxynitride as an interfacial layer, tantalum oxynitride MOS capacitors using zirconium silicate as an interfacial layer exhibit lower leakage current levels at the same equivalent oxide thickness. We were able to confirm stack structure by auger electron spectroscopy and transmission electron microscope analysis. The estimated dielectric constant of TaO_xN_y and $ZrSi_xO_y$ were approximately 67 and 7, respectively. In addition, $TiO_2/ZrSi_xO_y$ stack structure also exhibits excellent electrical characteristics. The zirconium silicate is a promising interfacial layer for future high-k gate dielectric applications.

10:45 AM K4.7
ELECTRICAL AND STRUCTURAL CHARACTERISTICS OF ULTRA-THIN TiO_2/Ti-Si-O STACKED GATE INSULATOR FORMED BY RF SPUTTERING TECHNIQUE. Masato Koyama, Akio Kaneko, Ikuo Fujiwara, Masahiro Koike and Akira Nishiyama, Toshiba Corporation, R&D Center, Advanced LSI Technology Laboratory, Yokohama, JAPAN; Motonaka Yabuki, Masahiko Yoshiki, Mitsuo Koike, Toshiba Corporation, R&D Center, Environmental Engineering and Analysis Center, Yokohama, JAPAN.

It has been widely reported that high-k TiO_2 films form interfacial layer with Si during the TiO_2 deposition process and that this layer restricts the reduction of equivalent oxide thickness due to its low-k property. We closely investigated the electrical and structural characteristics of TiO_2/interfacial layer/Si stack fabricated by RF sputtering with TiO_2 target on H-terminated Si surface at room temperature. It has been revealed that the interfacial layer consists of Ti-Si-O and the dielectric constant is well above that of SiO_2. The existence of titanium in the interfacial layer was confirmed by high spatial resolution Electron Energy Loss Spectroscopy (EELS) measurement. By the optimization of the sputtering condition we could successfully reduce the interfacial layer thickness and obtained equivalent oxide thickness of 1.3 nm for the ultra-thin TiO_2/Ti-Si-O stacked gate insulator. The leakage current density though this insulator stack was as low as 0.1A/cm^2 at the gate voltage of -1V. The subthreshold-swing of MISFET with thin TiO_2 gate stack as the gate dielectric was under 80mV/dec, indicating its low interface state density with Si substrate. In addition, the flatband-voltage is an acceptable value. Detailed electrical and physical analyses of the gate stack as well as its endurance against high temperature annealing will be presented.

11:00 AM K4.8
INVESTIGATION ON THE THERMAL AND ELECTRICAL PROPERTIES OF Ti-Si-O FILM FORMED BY COMPOSITE SPUTTERING DEPOSITION. Akira Nishiyama, Akio Kaneko, Masato Koyama, Yoshiki Kamata, Ikuo Fujiwara and Masahiro Koike, Toshiba Corp., R&D Center, Advanced LSI Technology Lab., Yokohama, JAPAN; Masahiko Yoshiki and Mitsuo Koike, Toshiba Corp., R&D Center, Environmental Engineering and Analysis Center, Yokohama, JAPAN.

With the objective of suppressing leakage current and avoiding the power consumption increase in future LSIs, various high-permittivity dielectric materials have been investigated for the new gate insulator of MISFETs. Among the candidates, TiO_2 has a relativily high permittivity and it has been revealed that the deposition of the material directly on the Si substrate forms Ti-Si-O as the interfacial layer. In this work, we investigated the thermal and electrical properties of Ti-Si-O film formed by sputter deposition with various compositional changes. Composite targets of TiO_2 and SiO_2 were used for the sputtering on HF-terminated Si(100) substrate at 300°C. $(TiO_2)_{1-x}(SiO_2)_x$ films with x ranging from 0 to 0.75 were formed. The film thickness was about 100nm. It was confirmed that as-deposited films were all amorphous regardless of the x value. Annealing in an Ar ambient at 800°C resulted in the phase separation and TiO_2 of anatase phase was segregated in the amorphous material (presumably Ti containing SiO_x). The grain size of TiO_2 measured by X-ray diffraction diminished from about 90 nm to 5nm with the increase in the SiO_2 content. The thermal grooving, which is typical for polycrystalline TiO_2 after high temperature annealing, was greatly suppressed when SiO_2 content increased, indicating the robustness of the film up to 1000°C. C-V measurement of the films was performed and revealed that the permittivities of the $(TiO_2)_{1-x}(SiO_2)_x$ with x of 0.43 and 0.75 were 29 and 16, respectively. These values are lower than that of anatase TiO_2 but considerably larger than that of SiO_2, indicating the feasibility of the film for the gate dielectric as well as the interfacial layer between TiO_2 and Si substrate.

11:15 AM K4.9
COMPARISON OF CONDUCTANCE AND CAPACITANCE TECHNIQUES FOR MEASUREMENT OF INTERFACE STATES IN THIN OXIDES. T.K. Higman, University of Minnesota, Department of Electrical and Computer Engineering, Minneapolis, MN.

The current efforts to produce high-k gate oxides should ultimately lead to gate stacks with equivalent SiO2 thicknesses of less than 1 nm. The most common method for characterization of interfacial trap density (Dit) in these films is by analyzing capacitance-voltage (C-V) data where the high and/or low frequency capacitance vs. gate bias is compared to a theoretical ideal. Unfortunately, this method can be inaccurate when measuring ultra-thin oxides as the basic theory assumes relatively thick oxides and correspondingly low leakage through the films. Ultra-thin oxides result in high oxide capacitances of several uF/cm2 and the resulting differences between measured high frequency C-V data and theoretical curves are quite small - even for relatively large Dits of 1e11/eV-cm2. This makes extraction of Dit by high frequency C-V very difficult and chronically underestimates Dit. In addition, small leakage currents (with associated conductances less than 1 nS/cm2) can cause significant, unanticipated deviations from the theoretical high frequency C-V. An alternate approach is to use the conductance vs. frequency method where the energy lost to recombination via interface states is used to calculate Dit. This method has generally been avoided due to additional complexity in data collection and analysis. Data taken from high-k gate stacks produced in our laboratory (HfO2 on silicon) shows that when the three methods (high and low frequency C-V and conductance) are compared, the differences in calculated Dit can exceed 5e10/eV-cm2 - with high frequency C-V measurements consistently being the least

accurate. We show that when C-V data is combined with conductance vs. frequency data a complete picture of the interface state density throughout the band can be obtained. While this is primarily intended as a discusson of appropriate measurement techniques, data on thin HfO2 films with integrated Dits of less than 1e11 will be presented.

11:30 AM K4.10
BAND OFFSETS OF MEDIUM K GATE OXIDES. John Robertson, Cambridge Univ, Cambridge, UNITED KINGDOM.

Medium dielectric constant (K) oxides are presently being evaluated for use as the gate dielectrics in future silicon devices. New gate oxides, which are in direct contact with the Si channel, must meet four requirements: (1) no reaction with Si. (2) low diffusion oxygen coefficient. (3) potential barriers over 1 V for both electrons and holes to give low leakage currents. (4) defect-free interfaces with Si, to minimise carrier scattering. These requirements point towards amorphous oxides or compounds of Zr, Hf, La or Al. We have calculated the band offsets on Si of many candidate oxides using the method of charge neutrality levels. La_2O_3, Y_2O_3, ZrO_2, Al_2O_3 and $ZrSiO_4$ are found to have offsets over 1.5 eV for both electrons and holes, making them possible gate dielectrics. However, simple oxides like Zr, Hf and La have limited glass forming ability. Silicates of Zr, Hf or La improves the glass stability, but at the expense of a much reduced K value. Zr aluminate would combine the stability with a K over 10.

11:45 AM K4.11
ATOMIC BONDING COORDINATION, NETWORK STRUCTURE AND RELATED PROPERTIES FOR SILICON-OXIDE RICH ZIRCONIUM SILICATE ALLOYS. Bruce Rayner, Donghun Kang, Gerald Lucovsky, NC State Univ, Dept of Physics, Raleigh, NC.

Relationships between bonding, and physical, chemical, and electrical properties of plasma deposited silicon dioxide-rich zirconium-silicate alloys were studied. Films with varying zirconium oxide fraction were deposited on Si(100) by remote plasma enhanced-metal organic chemical vapor deposition. Film composition was determined by Rutherford backscattering spectrometry (RBS). RBS results, coupled with on-line Auger electron spectroscopy (AES) indicates that films were fully oxidized, stoichiometric alloys along a join-line between silicon dioxide and the compound silicate. Atomic bonding as a function of composition, was investigated by Fourier transform infrared spectroscopy (FTIR), x-ray photoelectron spectroscopy (XPS), AES, and extended x-ray absorption fine structure (EXAFS). Film morphology, non-crystalline or crystalline, was determined by x-ray diffraction (XRD). The band gap and optical dielectric constant were obtained by spectroscopic ellipsometry. Measurements were made as a function of post-deposition annealing temperature in argon for 30-60 s to determine stability against phase separation and/or crystallization. Electrical measurements, capacitance-voltage and current-voltage, were made on metal-oxide-semiconductor capacitors to determine the dielectric constant and leakage current as a function of composition and post deposition annealing. Some important results are: i) films deposited at 300C are stable to annealing temperatures of 900C, ii) at 900C, silicon oxide-rich alloys show a chemical phase separation into silicon dioxide and zirconium oxide, whilst films at, or near the compound silicate composition indicate crystallization of the zirconium oxide, iii) as the zirconium oxide fraction increases, the coordination of zirconium increase from four at very low concentration to eight at the compound silicate composition, and iv) the dielectric constant shows an enhancement at low zirconium content that is correlated with atomic coordination. The four fold coordinated Zr bonding is more covalent and contributes more to the dielectric constant that the more ionic bonding at higher concentrations. The results of other experiments include the electrical data will presented at the symposium.

SESSION K5: NOVEL GATE STRUCTURES
Chairs: Larry A. Clevenger and Peter B. Griffin
Wednesday Afternoon, April 18, 2001
Golden Gate C2 (Marriott)

1:30 PM K5.1
DUAL WORK FUNCTION CMOS GATE TECHNOLOGY BASED ON METAL INTERDIFFUSION. Igor Polishchuk, Pushkar Ranade, Tsu-Jae King and Chenming Hu, University of California, Berkeley, CA.

Metal gate electrodes bring about several advantages compared to traditional polycrystalline Si gates as CMOS technology continues to scale beyond 100 nm node. These include reduction in poly-depletion effect, reduction in sheet resistance, and potentially better thermal stability on high-K gate dielectrics. The main challenge is that, unlike with polysilicon, one would have to use two metallic materials with different work functions in order to achieve the right threshold voltages for both n-MOS and p-MOS. A straightforward way to implement dual metal CMOS, is to etch away the first metal from either n- or p-MOS side, and then deposit a second metal with a different work function. Unfortunately, this would entail exposing the gate dielectric to the etchant, leading to undesirable dielectric thinning and likely reliability problems. In our process, we deposit a thin (10 nm) layer of Ti (a low work function metal) followed by a layer of Ni (a high work function metal). Then Ni (the top layer) is removed from n-MOS devices so that only Ti remains over the n-MOS and determines its threshold voltage. Due to high diffusivity of Ni in Ti, after a 30 min 400°C anneal, Ni diffuses through the Ti layer to the dielectric interface. Thus, Ni determines the p-MOS threshold voltage. Ni-Ti interdiffusion was confirmed by X-ray photoelectron spectroscopy (XPS) analysis. Capacitance vs. voltage measurements show a flat-band voltage shift in excess of 1V resulting from Ni-Ti interdiffusion. Ti electrode gives a work function of 3.9 eV (suitable for n-MOS), while Ni gives a work function of 5.4 eV (suitable for p-MOS).

1:45 PM K5.2
INTEGRATION OF MOLYBDENUM GATE ELECTRODE WITH ADVANCED GATE DIELECTRICS FOR FUTURE CMOS TECHNOLOGY. Pushkar Ranade, Ronald Lin, Qiang Lu, Yee-Chia Yeo, Hideki Takeuchi, Tsu-Jae King, Chenming Hu, University of California at Berkeley, Berkeley, CA.

As CMOS technology is scaled beyond the 100nm node, the issues of gate depletion and dopant penetration warrant the investigation of alternative gate electrode materials to replace poly-Si. Molybdenum (Mo) is a promising metal gate candidate with good thermal stability, low coefficient of thermal expansion, and high conductivity. In an earlier publication [1], it was proposed that the work function, Φ_M, of nitrogen-implanted Mo could be tuned over a range spanning the Si energy band gap. In this paper, the study of Mo as a candidate gate electrode material is extended to investigate process integration issues. Mo-gated CMOS transistors were successfully fabricated using a conventional process flow, using various advanced gate dielectrics: Si_3N_4, $ZrSiO_4$, ZrO_2 and HfO_2. Extracted mobility values were in good agreement with the universal mobility model, providing evidence that Mo is stable on high-k dielectrics. Equivalent oxide thickness and work function were determined by matching measured capacitance-vs.-voltage (C-V) characteristics with quantum-mechanical simulation, and the gate-stack interfaces were analyzed by high resolution TEM. The experimental work function data were then compared to theoretical models for Φ_M vs. k. Mo-gated MOS capacitors were fabricated with experimental splits for implant energy and dose, as well as for annealing ambient, and the gate work functions were extracted from C-V measurements. Experimental results for other gate implant species were also obtained. We conclude that the observed dependence of the gate work function on gate-dielectric permittivity presents a significant challenge for metal gate electrode technology. In light of this, the ability to engineer the Mo gate work function over a relatively large range makes it an attractive candidate for future CMOS technology. [1]. P. Ranade, et al, MRS Symposium Proceedings, Spring 2000, in press

2:00 PM K5.3
FABRICATION AND CHARACTERIZATION OF CMOS TRANSISTORS WITH TITANIUM-NITRIDE METAL GATE. Meng-Fan Wang, Ya-Chen Kao, National Chiao-Tung University, Institute of Electronics, Hsin-Chu, TAIWAN; Horng-Chih Lin, Tiao-Yuan Huang, National Nano Device Laboratories, Hsin-Chu, TAIWAN.

Recently, several metallic materials have been considered for replacing the polycrystalline Si as the gate electrode of complementary metal-oxide-semiconductor (CMOS) devices in order to reduce gate resistance and poly depletion effect (PDE). However, thermal stability remains as one of the major concerns for realizing the metal-gated CMOS fabrication. In this work, we have fabricated CMOS transistors with TiN gate and investigated effects of post-source/drain (S/D) implant annealing on the device characteristics. Thickness of gate oxide is 3 nm. Rapid thermal annealing (RTA) with temperature ranging form 700 to 1000°C was used to activate the S/D dopants. It is found that the device's junction leakage and threshold voltage tend to decrease with increasing RTA temperature. Nevertheless, device's off current is dominated by the gate-induced gate leakage (GILD), which would be enhanced with increasing RTA temperature. Gate leakage also increases with a higher annealing temperature. These results indicate that metal penetration is presumably responsible for the observed phenomenon. Plasma charging damage characteristics have also been characterized using designed antenna structures. Results show that the immunity to the antenna effects would be degraded if metal gate used.

2:15 PM K5.4
EVALUATION OF DEPOSTION BEHAVIOR ON DCS BASED

POLYCIDE (WSi). Young-Kyou Park, Jaihyung Won, Ho-Shik Kim and Jung-Ho Park[a], Kiheung Plant, Memory Division, Samsung Electronics, Kyunggi-Do, KOREA. [a] Department of Electronics Engineering, Korea University, Seoul, KOREA.

DCS based CVD WSix that is formed by Tungsten Fluoride (WF_6) and Dichlorosilane (SiH_2Cl_2; DCS). The reaction is very favorable thermodynamically, which follows good purity of WSi as seldom Fluorine (F) concentration. It makes to restrain expansion of gate oxide and good step coverage. And furthermore, stable stoichiometry due to make low resistivity has been widely applied in the very large-scale integrated circuit (VLSI) fabrications. However, since the major impurity, Chlorine (Cl) affects different behaviors from the Mono Silane (SiH_4; MS) based WSi, DCS can not be used in same condition as the normal MS based WSi. This work provides that it is evaluated by related deposition behaviors on crystalline quality of sub-poly-silicon film and on the chlorine condensation effects of DCS based WSi. It is characterized that the resistivity of polycide changes on phase transition of process-temperature dependencies.

2:30 PM K5.5
ELECTRICAL AND MATERIAL PROPERTIES OF A SINGLE WORK FUNCTION 0.15 UM TUNGSTEN GATE STACK FOR 1GB DRAM APPLICATIONS. L.A. Clevenger[a], O. Gluschenkov[a], R. Iggulden[a], I. McStay[b], W. Robl[b], P. Shafer[a] and K. Wong[a]. [a]IBM Microelectronics, Semiconductor R&D Center, Hopewell Junction, NY; [b]Infineon Technologies, Hopewell Junction, NY; DRAM Development Alliance IBM/Infineon, IBM Semiconductor R&D Ctr, Hopewell Junction, NY.

Abstract A 0.15 um-single work function tungsten gate CMOS technology has been develop for 1Gb DRAM applications. This technology has a factor of four lower sheet resistance and about 15% smaller stack height than a comparable WSix based gate approach. The tungsten gate technology consists of a thin tungsten conducting layer on top of a tungsten nitride diffusion barrier, which is on top of n-doped poly-Si thin film. The lower sheet resistance and the smaller stack height of the tungsten gates are two factors that enables the creation of smaller and cheaper DRAM chips with increased performance. In order to achieve this low sheet resistance, we determined that the tungsten gate structure must be annealed with enough thermal budget (>900C) to cause the film to transform into the lower resistance phase. However, too much thermal annealing caused voids to form at the tungsten/poly-Si interface. These voids were formed by the diffusion of silicon through a tungsten nitride diffusion barrier into the tungsten thin film. The electrical interface resistance of the tungsten nitride diffusion barrier was measured in 0.2 um structures and was determined to be dependent on the tungsten nitride deposition and annealing conditions. Using a combination of annealing after tungsten deposition to transform the tungsten into the lower resistance phase and modifying the deposition conditions of the tungsten nitride diffusion barrier which minimized interface resistance, we were able to produce a 0.15 um tungsten gate technology. This technology has similar NFET and PFET drive currents and threshold voltages compared to 0.15 um WSix gate devices with a factor of four lower sheet resistance.

2:45 PM K5.6
REDUCTION OF WHISKER-ORIGINATED SHORT BETWEEN W POLYMETAL AND CONTACT PLUG. Yasushi Akasaka, Yoshio Ozawa, Nobuaki Yasutake, Hitomi Yasutake, Susumu Yoshikawa, Yusuke Kohyama, Katsuhiko Hieda, Kyoichi Suguro, Semiconductor Company, Toshiba Corporation, Yokohama, JAPAN; Toshihiro Nakanishi, Hiroshi Suzuki, Fujitsu Laboratories Ltd., Yokohama, JAPAN; Yuji Yokoyama, Fujitsu Limited, Yokohama, JAPAN.

W polymetal is an attractive candidate for low resistivity gate electrode for the 0.15μm or smaller nodes of ULSIs. Tolerance between gate and contact can be minimized, because self-aligned contact (SAC) is applicable for this structure. Whisker formation caused by oxidation of W is one of the most serious problems in W polymetal technology. It may result in electrical short between gate electrode and contact plugs. The whisker formation is effectively suppressed by deoxidizing WO_X of the W surface before high temperature processing. [1] W/WN_X/poly-Si (40/5/70nm) stacked gate electrodes with SiN caps (150nm) and SiN spacers (20nm) were formed. Self-aligned poly-Si plugs were also formed. The whisker-originated short was observed by emission microscopy and TEM for the first time. The points where electrical short occurred in test structures were identified by emission microscope. The whisker was found within SiN gate spacer by cross-sectional TEM observation. From this result, it is confirmed that the whisker is one of the main causes of the SAC short. As we have already reported, deoxidization of the W surface just before thermal processing should be effective for suppressing whisker growth. The effect of deoxidizing WO_X was confirmed by the electrical short measurement of 256K test structures. By applying NH_3 reduction step before LP-CVD of SiN film, the short yield was found to be markedly improved. Therefore we believe this deoxidizing method is extremely useful to achieve a high yield of polymetal gate electrode in Giga-bit scale LSIs. [1] Y. Akasaka et al., Jpn. J. Appl. Phys. 38, 2385 (1999).

3:30 PM K5.7
ANNEALING BEHAVIOUR OF WSi_x FILMS PREPARED BY CVD. Monica Katiyar, Rohit Kumar Gupta, Deepak, IIT Kanpur, Department of Materials and Metallurgical Engineering, Kanpur, INDIA; Pratap Kumar Shahoo, V.N. Kulkarni, IIT Kanpur, Department of Physics; Olubunmi Adetutu, Motorola, Inc., Phoenix, AZ.

Tungsten polycide (WSi_x/poly-Si) gate is well established in VLSI circuits, but it can not be used in devices with ULSI dimensions. Other lower resistivity silicides are being investigated to replace WSi_x layer, but we feel that innovation in processing can reduce the resistivity of the tungsten ploycide. After all, resistivity of single crystal WSi_2 is comparable to other low resistivity silicides of Ti, Co, and Ni. For some reason, thin film WSi_2 has higher resistivity compared to the singlecrystal form. WSi_x thin films are normally deposited by chemical vapour deposition and are amorphous in nature, and need to be annealed at high temperature to obtain low resistivity. Most reports use an anneal process at about 900-1000°C for 30 minutes in a conventional furnace or 5 minutes in a RTP furnace. This annealing process is not well understood, especially for non-stoichiometric compositions. We are focusing on this annealing process for films deposited on Si and SiO_2 substrate. The characterization methods used were time-resolved X-ray diffraction, Resistivity measurement, and Rutherford backscattering spectroscopy analysis. Annealing was carried out for various times and temperatures in N_2. We observe that the standard annealing process is not sufficient for complete crystallization of the 5000$\AA$ thick WSi_x films on Si substrate. For the first time, we also report the dependence of annealing behaviour of nonstoichiometric WSi_x film on the substrate type. A simple model will be developed to explain the difference in the kinetics of phase transformation of the films on different substrates. The understanding of phase transformation kinetics would be the key to developing processes that will be able to produce lowest resistivity WSi_x films.

3:45 PM K5.8
EFFECTS OF Ge CONTENT AND ANNEAL AMBIENT ON THE BORON PENETRATION OF THE W/WN/POLY-SiGe/SiO_2/Si MOS STRCUTURE. Tae-Hang Ahn, Dae-Gyu Park, Moon-Sig Joo, In-Seok Yeo and Jin Won Park, Hyundai Electronics Ind. Ltd., Advanced Process Team, Ichon-Si, KOREA.

We investigated the effects of Ge content and anneal ambient on the B penetration of the W/WN/poly-SiGe/SiO2/n-Si pMOS capacitors to gauge the flatband voltage (Vfb) stability during gate reoxidation process. Boron penetration of W/WN/poly-SiGe/n-Si structure was probed by C-V measurement and SIMS profile as a function of Ge content (0, 20, 60% Ge) and anneal ambient (N2 and H2) at 950°. We observed that the Vfb shift with anneal in N2 ambient was reduced with Ge content, which is consistent with earlier work. On the contrary, the Vfb shift of p poly-SiGe (20% Ge) in H2 ambient was ~ 0.7 V, corresponding to a p-type dopant level of 3x1012 B ions/cm2, compared to that in N2. This suggests that B penetration in low Ge mole fraction (20%) is enhanced in H2. On the other hand, the Vfb shift of poly-SiGe (60% Ge) was remarkably reduced even in H2 compared to that of poly-SiGe (0 and 20% Ge). The reliability characteristics of W/WN/poly-SiGe/SiO2/Si with Ge content and anneal condition will be discussed.

4:00 PM K5.9
A STUDY ON THE PHYSICAL AND ELECTRICAL PROPERTY OF POLY $Si_{1-X}Ge_X$ GATE STRUCTURES. FOR CMOS TECHNOLOGY. Sung-Kwan Kang, Dae-Hong Ko, Yonsei Univ, Dept of Ceramic Engineering, Seoul, KOREA; Tae-Hang Ahn, In-Seok Yeo, Hyundai Electronics Industries Co. Ltd., Kyungki-do, KOREA; Ki-Chul Lee, Tae-Wan Lee, Young-Ho Lee, Ju-sung Co. Ltd., Kyungki-do, KOREA.

Polycrystalline $Si_{1-X}Ge_X$ films have been suggested as a promising alternative to the currently employed poly-Si gate electrode for CMOS technology since poly $Si_{1-X}Ge_X$ gate materials show a lower resistivity than the poly-Si, and also their workfunction can be controlled by changing the Ge content in the films. We investigated the formation of poly $Si_{1-X}Ge_X$ films grown by LPCVD using SiH_4 and GeH_4 gases, and studied their physical properties as well as electrical characteristics using TEM, XRD, RBS, XPS, and SIMS as well as C-V, I-V, and 4-point probe measurements. The deposition process was performed at the temperature range between 575°C and 625°C. The films with Ge content from 0% to 80% were obtained by changing the flux of the GeH_4 gas and the deposition rate of the poly $Si_{1-X}Ge_X$ films was about 500 $\AA$ /min. The resistivity of the poly

$Si_{1-X}Ge_X$ films decreased as the Ge content increased, and was about one half of that of poly-Si films at the Ge content of 45%. The C-V measurements of the MOSCAP structures with W/WN_X/poly $Si_{1-X}Ge_X$ gates stack demonstrated that the flat band voltage of the poly $Si_{1-X}Ge_X$ films was lower than that of poly-Si films by 0.3V, and show less gate-poly-depletion-effect than that of poly-Si gates. Also, Q_{BD} increase with Ge content in the gate.

4:15 PM K5.10
A STUDY ON THE POLYCRYSTALLINE SILICON GERMANIUM GATE ELECTRODE FABRICATION TECHNOLOGY FOR COBALT SILICIDE PROCESS. Hidekazu Sato, Takae Sukegawa, Toshifumi Mori, Kousuke Suzuki and Haruhisa Mori, Fujitsu Limited, Mie, JAPAN.

As the dimensions of ultra large scale integrated circuits (ULSI) devices continue to shrink, conventionally used polycide or silicide gate stacks with poly-Si films show serious issues of gate depletion, and boron penetration and so on. Recently, polycrystalline silicon germanium (poly-SiGe) films have received an attention as a gate electrode material because they are not only compatible with the conventional complementary metal oxide semiconductor (CMOS) fabrication process but also effective to reduce gate poly-Si depletion and boron penetration phenomena, simultaneously. Most of the poly-SiGe gate devices have been fabricated with a poly-Si cap layer in order to preserve the standard cobalt silicide process. In fact, a critical amount the of poly-Si cap layer is indispensable for successful slicidation by minimizing Ge diffusion into the poly-Si cap layer during post high temperature process. However, the correlation between the concentrations of Ge in the poly-Si cap layer and quality of the cobalt disilicide ($CoSi_2$) has not been much discussed. In the present work, we studied dependence on the concentration of the Ge in poly-Si cap layer on the poly-SiGe for high quality $CoSi_2$ formation. The poly-SiGe and poly-Si cap layer was deposited on eight-inch wafers using an atmospheric pressure chemical vapor deposition (APCVD) system. The 100% silane (SiH_4) and 1.5% germane (GeH_4) in hydrogen ware used as the silicon and germanium gas source. The silicide process is performed by the 2-steps anneal method by using the TiN capping technology. It is found that the diffusion rate of Ge in an n-type poly-Si cap layer is higher than that in a p-type poly-Si cap layer, and the resistivity of $CoSi_2$ increases as the Ge content in a poly-Si cap layer increases. We are going to be demonstrated results of optimization for the poly-SiGe gate electrode fabrication technology for the cobalt silicidation process.

4:30 PM K5.11
ETCHING OF ADVANCED GATE - STACK MATERIALS IN A CONVENTIONAL CMOS PROCESS FLOW. Michael B. Freiler, Avinash K. Agarwal, Bill Bowers, Will Chism, International SEMATECH, Austin, TX; Lee Chen, Tokyo Electron America, Austin, TX; Hiromasa Mochiki, Tokyo Electron Massachusetts, Beverly, MA.

The insertion of advanced gate - stack materials, such as metal gate conductors and / or high permittivity gate dielectrics, into the standard CMOS process flow presents many challenges for dry etch. One challenge is the need to develop new gate etch chemistries and processes for metal gates, while maintaining the needed selectivity to the gate dielectric. Also, integration needs may require dry etching to remove or thin the gate dielectric itself, requiring the development of new etch processes. A survey of dry etches of various possible metal gate materials (Ta, TaN, W, WN, and TiN on SiO2) has identified useful etch chemistries; we will show how the TiN etch process can be transferred to Ta2O5 dielectric. Etch - related considerations, in particular those related to the use of wet versus dry processing for removal of the gate dielectric, of substituting ZrO2 gate dielectric into the standard CMOS process flow will also be discussed.

4:45 PM K5.12
GRAIN DISTRIBUTION OF POLYSILICON FILMS IMPLANTED WITH BORON. R. Brindos[a], H-H. Vuong, A.T. Fiory, K. Short, R. Spolenak, K. Evans-Lutterodt, J. Grazul, C.S. Rafferty, Bell Laboratories, Lucent Technologies, Murray Hill, NJ. [a]Permanent address Univ of Florida, Gainesville, FL.

In today's processing world the use of long time furnace anneals is not practical for shallow junction fabrication. Instead, Rapid Thermal Annealing (RTA) systems have reduced the time needed for annealing from hours in a furnace. However, limited information is available on grain growth of poly-silicon films using RTA type conditions. The aim of this experimental work is to determine the grain growth behavior of poly-silicon films after boron implantation and RTA annealing. Comparisons of as-deposited amorphous silicon and as-deposited poly-silicon are made in terms of grain distribution and grain orientation upon annealing at high temperatures in an RTA system. Both high and low boron implant doses are investigated in each system. Plan-view and cross-sectional TEM was used in accordance with digital image techniques to quantify the grain size before and after annealing. X-ray pole figure measurements were done to determine whether any change in the distribution of crystallographic direction occurs during annealing. Cross-sectional TEM shows a rapid increase in grain size at all temperatures studied. The rapid size increase continues in the growth direction until the thickness of the film is reached. After the thickness of the film is reached there is slower growth in the grains in the plane of the film. The in plane grain growth was studied using Plan-view TEM and analysis shows that the average grain size is increasing but is not fully complete even after a 1050°C 16sec anneal. From pole figure analysis no shift in preferred grain orientation is noted in either system as a function of annealing, although the growth orientations of each system are quite different. It is determined that the boron dose does not play a significant role in the grain growth and that there is an orientation difference between the two systems that does not change during annealing.

SESSION K6: NOVEL SILICIDE PROCESSES
Chair: Anne Lauwers
Thursday Morning, April 19, 2001
Golden Gate C2 (Marriott)

8:30 AM *K6.1
IN SITU CHARACTERIZATION OF LOW RESISTIVITY SILICIDES FOR CONTACTS IN ULSI CMOS DEVICES. C. Cabral, Jr., C. Lavoie, J. Jordan-Sweet, J.M.E. Harper, IBM T.J. Watson Research Center, Yorktown Heights, NY.

In complementary metal oxide semiconductor (CMOS) devices silicides are widely used as Ohmic contacts to source, drain and gate regions as well as for local interconnects. The advantages of using silicides stem from the low resistivities and high thermal stability they provide. The salicide process is the integration technique used to incorporate the silicide into the CMOS device. It consists of depositing a blanket metal, annealing to a first low temperature to form a precursor phase, selectively etching the metal from non-silicon surfaces and performing a second higher temperature anneal to from the desirable low resistivity phase. Three silicides consisting of titanium (C54-$TiSi_2$), cobalt ($CoSi_2$) and nickel (NiSi) provide the necessary properties for CMOS integration. Of the three choices Ti silicide is the most widely used but in recent years Co silicide has been found to overcome some of the limitations in C54-$TiSi_2$ formation on sub-micron sized features. The trade offs between the silicide choices will be demonstrated with the use of the *in situ* analytical techniques of time resolved synchrotron x-ray diffraction, sheet resistance and elastic light scattering. The formation, resistance and thermal stability of the metal rich, monosilicide and disilicide phases will be compared.

9:00 AM K6.2
X-RAY TECHNIQUES FOR SILICIDES. Douglas J. Tweet, Jer-shen Maa and Sheng Teng Hsu, Sharp Laboratories of America, Camas, WA.

We have found that the addition of a thin layer of Co or Ir between Ni and the Si substrate dramatically improves the thermal stability of the resulting silicide. Here we describe the use of four different x-ray techniques to obtain complementary information on film structure, providing a possible explanation for the observed thermal stability. Ni and the interlayer metal were deposited by sequential e-beam evaporation. Rapid thermal anneals were performed in Ar ambient for typically 60 sec at temperatures from 300°C to 850°C. Low resolution x-ray diffraction can determine the phases in poly-crystalline films. For Ni films (no interlayer metal) this technique was used to find that the monosilicide phase observed at lower temperatures disappeared at anneals above 700°C. For Ni/Co films this phase disappeared above 500°C. High resolution x-ray diffraction (HRXRD) is used to examine well-oriented single crystals. With HRXRD near the Si(004) substrate peak it was discovered that at the higher temperatures the films had coalesced into nearly perfect alloy disilicide single crystals. Comparing Ni, Ni/Co, Ni/Co/Ni, and Ni/Ir films it was shown that the Ni/Co films had much better crystalline perfection. Furthermore, the Ni/Co films retained their structure during 850°C anneals lasting up to 30 minutes. HRXRD reciprocal space maps of the Si(224) region were then used to measure the lattice constant parallel to the surface. The Ni/Co films were found to be epitaxially strained to the Si substrate for anneals as low as 700°C. Finally, x-ray reflectivity (XRR) was used to measure the roughness and absolute thickness of the films. The as-deposited Ni/Co films were much flatter and more uniform than the Ni films. These results suggest the interlayer metal may improve the thermal stability and epitaxial quality by improving initial morphology and forming a diffusion barrier, regulating the silicidation process.

9:15 AM K6.3
EFFECTS OF A Ta INTERLAYER ON THE TITANIUM SILICIDE FORMATION: C40 FORMATION AND HIGHER SCALABILITY

OF THE $TiSi_2$ PROCESS. F. La Via, CNR-IMETEM, Catania, ITALY; G. Corallo, F. Mammoliti, S. Privitera and M.G. Grimaldi, Catania University, Phisics Department, Catania, ITALY.

The effect of a thin Ta layer at the Si/Ti interface on the intermediate phase formation and on the transition to the final C54 phase has been studied in detail. by in-situ sheet resistance, X-Ray Diffraction, Rutherford Backscattering Spectroscopy and Transmission Electron Microscopy analysis. A new intermediate phase has been detected: the hexagonal C40-$TiSi_2$. This phase grows on the C40-$TaSi_2$ that is formed at the interface with silicon. The lattice parameters of the C40-$TiSi_2$ ($a = 4.70 \pm 0.1$ Å $c = 6.49 \pm 0.01$ Å) have been obtained by X-Ray diffraction. The activation energies of the C40 formation (1.0 ± 0.1 eV) and the C40-C54 phase transition (2.3 ± 0.4 eV) have been determined. The final phase begins to form at the interface with the tantalum disilicide film and both the transformation kinetics and the film morphology are consistent with an increase by two order of magnitude of the nucleation density with respect to the C49-C54 transition. The nucleation rate and the growth velocity have been obtained from the experimental data using the Schneidman model. Using these results the scalability limit of this process can be fixed using a Monte Carlo code that takes into account all the nucleation parameters.

9:30 AM K6.4
DIRECT FORMATION OF C54 PHASE ON THE BASIS OF LASER-INDUCED C40 $TiSi_2$ AND ITS APPLICATIONS IN DEEP SUB-MICRON TECHNOLOGY. S.Y. Chen, Z.X. Shen, S.Y. Xu, Dept of Physics, National Univ of Singapore, SINGAPORE; A.K. See, L.H. Chan, W.S. Li, Chartered Semiconductor Manufacturing Ltd., SINGAPORE.

Titanium disilicide ($TiSi_2$) is the most widely used materials as contacts and interconnects for IC fabrication. Current salicidation process involves two-step rapid thermal annealing (RTA) and a selective Ti etch in between. The C49 $TiSi_2$ with a low resistivity of 60∼70 $\mu\Omega$cm is first formed by low temperature annealing. After the second annealing at a higher temperature of 750∼850°C, the C49 $TiSi_2$ transforms to the low resistivity and stable C54 phase of $TiSi_2$. The C54 $TiSi_2$ is the preferred phase for IC manufacturing in terms of its lower resistivity and better thermal stability. However, due to the well-known "fine line effect", the transformation to C54 phase is extremely difficult in narrow poly-Si lines. Moreover, the high temperature required for the transformation causes excessive dopant diffusion and other detrimental effects such as agglomeration and "punch through". Therefore, low temperature salicidation process eliminating the "fine line effect" is highly desirable. In our experiments, a simple and novel salicidation process applying pulsed laser annealing technique as the first annealing step was used to induce $TiSi_2$ formation. The samples of 35nm Ti sputter deposited on Si substrates were subjected to KrF (λ=248nm, τ_{FWHM}=20ns) excimer laser irradiation. Both micro-Raman spectroscopy and transmission electron microscope (TEM) results reveal the formation of a third phase of Ti disilicide, the pure C40 $TiSi_2$ after laser irradiation. C40 $TiSi_2$ has a basal plane very similar (< 0.3% mismatch) to the one of C54 phase. As a result, direct C54 formation on the basis of C40 template bypassing the C49 phase is accomplished at the second annealing temperature as low as 600°C. The template C40 $TiSi_2$ will also transform to C54 phase and a layer of pure C54 $TiSi_2$ is achieved at 600°C. This salicidation process has been applied to 0.25 μm technology and beyond. "Fine line effect" is completely eliminated.

10:15 AM K6.5
INCREASED THERMAL STABILITY OF COBALT SILICIDE FILMS BY COBALT AND TANTALUM ALLOY FILMS. Min-Joo Kim, Deok-Hyung Lee, Dae-Hong Ko, Yonsei Univ., Dept. of Ceramic Engineering, Seoul, KOREA; Ja-Hum Ku, Siyoung Choi, Kazuyuki Fujihara, Ho-Kyu Kang, Process Development Team, Semiconductor R&D Division, Samsung Electronics Ltd., KOREA; Cheol-Woong Yang, Sungkyunkwan Univ. School of Metallurgical and Materials Engineering, Suwon, KOREA; Hoo-Jeung Lee, Stanford University, Stanford, CA.

We investigated the silicidation reaction and thermal stability of Co silicide films using Co-Ta alloy films on (100) Si substrate. Co films and $Co_{1-X}Ta_X$ alloy films were deposited on Si substrate by DC magnetron sputtering. The content of Ta in $Co_{1-X}Ta_X$ alloy films was controlled at about 8 atomic %. Upon rapid thermal annealing (RTA) process, the silicidation reaction occurs between the Co-Ta films and Si substrate. With an increase in annealing temperature, the sheet resistance values decreased abruptly, which is due to the formation of Co-silicide layers. Compared with Co/Si systems, the transformation from the high resistive CoSi to the low resistive $CoSi_2$ phase in Co-Ta/Si systems occurs at higher temperature. We found that the phase transformation of Co-silicide in Co-Ta/Si systems is delayed due to the existence of Ta as diffusion barrier for Co flux to Si. For thermal stability test, samples were annealed in the furnace at 950°C up to 210 min in Ar ambient. We observed that the sheet resistance of Co silicide films from Co-Ta/Si systems maintained low value, while the sheet resistance of Co-silicide from Co/Si systems increased significantly. The improvement of thermal stability of Co-silicide films from Co-Ta alloy films is due to the presence of Ta. During the reaction, Ta diffuses into surface or grain boundaries of $CoSi_2$ layers, which slowed down the agglomeration process of the films. We conclude that the increased uniformity and thermal stability of $CoSi_2$ films are due to the formation of Ta compounds formed at the grain boundaries and surface of $CoSi_2$ films.

10:30 AM K6.6
A COMPARATIVE STUDY OF NiSi FORMATION USING A Ti CAPPING LAYER AND A THIN MIDDLE Ti LAYER. W.L. Tan, K.L. Pey, Centre for Integrated Circuit Failure Analysis and Reliability, Faculty of Engineering, National University of Singapore, SINGAPORE; Simon Y.M. Chooi, Chartered Semiconductor Manufacturing Ltd., SINGAPORE; J.H. Ye, Institute of Materials Research and Engineering, SINGAPORE.

NiSi formation is known to be hindered by an interfacial native oxide. Such oxide is easily formed on the Si substrate through inefficient cleaning or a long time lag prior to Ni deposition. In this study, two methodologies were investigated to remove this layer of native oxide and promote NiSi formation when no DHF dip was performed prior to metal deposition: Firstly, the deposition of 100Å Ti cap layer after Ni deposition and secondly, the deposition of a middle 50Å Ti prior to Ni deposition. All the samples were then rapid thermal annealed from 500 to 800°C. Phase characterization was carried out using XRD while XPS depth profiling was performed to study the distribution of nickel, titanium, oxygen and silicon. XTEM was used to study the layers of silicide formed after annealing. It was found that for the Ni / Ti / SiO_2 / Si system, a uniform layer of NiSi was formed after annealing at 500°C and conversion to $NiSi_2$ took place after 750°C. However, for the Ti / Ni / SiO_2 / Si system, a non-uniform layer of NiSi was formed only at 600°C although concomitantly with small regions of unreduced SiO_2. Similarly, $NiSi_2$ also forms above 750°C. Furthermore, even at low temperature (∼500-600°C), facets of $NiSi_2$ were identified under the thick NiSi layers, embedded in the Si substrate. In addition, ternary phases like $Ti_xNi_ySi_z$ were found at the surface of the sample. The mechanism for the nickel silicide formation observed would be discussed.

10:45 AM K6.7
THE INFLUENCE OF Ti AND TiN ON THE THERMAL STABILITY OF $CoSi_2$. Christophe Detavernier, Univ Gent, Dept of Solid State Sciences, Gent, BELGIUM; Guo-Ping Ru, Fudan Univ, Dept of Electr. Eng., Shanghai, CHINA; Roland Van Meirhaeghe, Univ Gent, Gent, BELGIUM; Karen Maex, IMEC, Leuven, BELGIUM.

In the self-aligned silicide (SALICIDE) process, the formation of the silicide layer requires the consumption of silicon from the substrate. Therefore, the silicide thickness has to be reduced simultaneously with the junction depth. Unfortunately, thin silicide films are more prone to thermal agglomeration. Therefore, characterization of the thermal stability of thin silicides and the prevention from agglomeration have attracted much attention recently. In this work, AFM and sheet resistance measurements are used to characterize the thermal stability of thin $CoSi_2$ films. We were particularly interested in the influence of different multilayer structures on the topography and surface roughness. Four different multilayer structures (Co/Si, TiN/Co/Si, Ti/Co/Si and Co/Ti/Si) were investigated. Thermal degradation of $CoSi_2$ formed from a standard Co/Si structure is found to have an activation energy of about 4.2 eV, independent of layer thickness (in agreement with previous results by Alberti et al.). A TiN capping layer is shown to improve the thermal stability. However, if the TiN layer is too thick (e.g. 50 nm), a new failure mode is observed: although the TiN prevents grain boundary grooving of the silicide, the thermal stress induced by the TiN causes the $CoSi_2$ layer to crack. For a Ti capping layer, a strong increase of the thermal stability of the $CoSi_2$ layer is observed, even if the Ti capping layer is removed by selective etching after the first RTP annealing. The presence of a very thin Ti-O-N containing layer on the $CoSi_2$ surface seems to strongly decrease surface diffusion and in this way reduce the tendency for grain boundary grooving.

11:00 AM K6.8
INFLUENCE OF THE REACTION OF Co WITH RM-CAPPING LAYER ON $CoSi_2$ FORMATION IN $Si/SiO_x/Co/RM$ SYSTEM. Gi Bum Kim, Joon Seop Kwak, Hong Koo Baik, Depart. of Metallurgical Engineering, Yonsei University, Seoul, KOREA; Sung Man Lee, Depart. of Advanced Materials Science and Engineering, Kangwon National University, Chunchon, KOREA; Sang Ho Oh, Chan Gyung Park, Depart. of Materials Science and Engineering, POSTECH, Pohang, KOREA.

Silicides are commonly used in the microelectronics industry for reducing the resistance of gates, diffusions, and local interconnects. Among the metal silicides in electrical devices, $CoSi_2$ is regarded as superior in terms of low resistivity and linewidth-independent sheet resistance. Achieving epitaxial silicide growth provides special advantages, such as low resistivity, absence of fast grain boundary diffusion paths, favorable interfacial properties, film uniformity, and thermal stability against agglomeration. For the formation of an epitaxial $CoSi_2$ film, solid-state interactions between Co and the Si substrate using interlayer such as Ti or chemical oxide have been suggested. The success of epitaxial growth using these methods was believed to be due to the fact that Co flux is controlled through the interlayer. In the formation of epitaxial $CoSi_2$ using SiO_x layer, only in the thickness range of 1 - 3nm Co were $CoSi_2$ layers grown continuous and single crystalline. However, an epitaxial $CoSi_2$ film of about 45nm was successfully produced using Ti-capping on $Si/SiO_x/Co$ system. Although several attempts have been made to investigate the effects of capping layer on $CoSi_2$ formation, little work has been performed on the effect of solid phase reaction between Co and capping layer during the formation of thick epitaxial $CoSi_2$ layer. In this study, to clearly discern the role of the capping layer, we have investigated the influence of reaction of Co with RM-capping layer on the $Si/SiO_x/Co/RM$ system

11:15 AM K6.9
STABILITY IMPROVEMENT OF NICKEL SILICIDE WITH COBALT INTERLAYER ON SILICON,POLYSILICON AND SILICON-GERMANIUM. Jer-shen Maa, Yoshi Ono, Douglas J. Tweet, Fengyan Zhang and Sheng Teng Hsu, Sharp Laboratories of America, Camas, WA.

Nickel silicide is a candidate material for use in future CMOS device generations. Besides the advantages of low resistivity and reduced Si consumption of the monosilicide, very low junction leakage has been demonstrated in conjunction with plasma doped ultra-shallow junctions. Application of nickel silicide on SiGe raised source and drain structure has been reported. The major drawback of nickel silicide is its poor thermal stability. This limits its use in typical CMOS applications. Enhancement of the thermal stability of nickel silicide has been reported previously by the addition of Pt. However, electrically active defects were detected on n-type silicon. Improved thermal stability on Si is achieved by adding a thin Co interlayer before Ni deposition. The film can withstand RTA as high as 850°C. The thermal stability was evaluated by measuring the junction leakage of an ultra-shallow junction with a 40 nm junction depth. Thermal stability of nickel silicide on polysilicon is very poor even around 500 to 700 degree Celsius. With the addition of thin Co interlayer, stability is improved to 850C. Nickel silicide on SiGe also shows poor thermal stability at temperature higher than 700C. Again by adding this thin Co interlayer stability is improved to 850C. Sheet resistance of silicide in the range of 5 to 10 ohm/square is demonstrated. The films were characterized by x-ray diffraction, TEM and RBS. The improved stability and low junction leakage is attributed to a very smooth interface.

11:30 AM K6.10
SILICIDE FORMATION FOR Ni AND Pd BILAYEYS ON Si(100) SUBSTRATES. Xin-Ping Qu, Christophe Detavernier, Roland L. Van Meirhaeghe and Felix Cardon, Dept of Solid State Science, Univ Gent, Gent, BELGIUM.

Nickel monosilicide (NiSi) is one of the most promising potential candidates to replace C54-$TiSi_2$ for deep submicron MOSFET devices, because its sheet resistance remains unchanged for linewidths down to 0.1μm. However, NiSi is not stable at temperatures higher than 750°C and will transform to high resistive $NiSi_2$. Therefore efforts were undertaken to control the $NiSi_2$ nucleation by adding impurities such as Pt or Au. In this paper, the effect of the addition of Pd on the silicide formation is studied. The Ni(10nm) and Pd(0.1~10nm) layers were sequentially deposited on Si(100) wafers in an e-beam evaporation system and followed by rapid thermal annealing from 250°C to 950°C. XPS, XRD and the four point probe technique were used to study the phase formation, chemical composition and sheet resistance of the films. The results show that the addition of Pd increases the $NiSi_2$ nucleation temperature. The higher the Pd addition, the higher the $NiSi_2$ nucleation temperature. Additionally, the Ni effect on the nucleation behaviour of PdSi from Pd_2Si was also studied. The results show that with the addition of Ni, the nucleation temperature of PdSi was decreased. XRD on a Ni/Pd/Si sample annealed at 650°C shows that a ternary silicide $Ni_xPd_{1-x}Si$ layer formed. The phenomena are explained by the classical theory for nucleation.

11:45 AM K6.11
STABILITY OF Ni SILICIDE ON POLY-Si METAL OXIDE SEMICONDUCTOR GATE CONFIGURATION. P.S. Lee, National Univ of Singapore, Dept of Materials Science, SINGAPORE; K.L. Pey, National Univ of Singapore, Dept of Electrical Engineering, SINGAPORE; D. Mangelinck, Institute of Materials Research and Engineering, SINGAPORE; J. Ding, National Univ of Singapore, Dept of Materials Science, SINGAPORE; T. Osipowicz, National Univ of Singapore, Dept of Physics, SINGAPORE; A. See, Chartered Semiconductor Manufacturing Ltd., SINGAPORE.

Stability of Ni silicide on poly-Si is a key issue in integration of Ni salicide technology. Reaction of Ni on poly-Si, where metal atom is the dominant diffusing species during silicide formation, is complicated by the additional driving force of poly-Si grain growth. This leads to layer inversion resulting in large Si grains replacing the silicide layer. This effect is critical for forming uniform silicide on the poly-Si gate stack of MOSFETs, which in turn determines the performance of the transistors. In this study, investigation has been carried out to examine the phase formation and morphological changes of Ni films on undoped LPCVD (Low Pressure Chemical Vapor Deposition) poly-Si/SiO_2 and BF_2^+ implanted poly-Si/SiO_2 as the silicidation temperature varies by rapid thermal processing (RTP). XTEM (Cross Transmission Electron Microscope), RBS (Ruthurford Backscattering Spectroscopy) and XRD (X-ray Diffraction) were used to characterize the films. Dopants in poly-Si (in this case, BF_2 ions) as well as the dopant activation process were found to play a role in delaying the poly-Si inversion to a higher temperature. Sheet resistance of the films was measured at various silicidation temperatures. The less extensive layer inversion on the BF_2 doped poly-Si has resulted in a decreased sheet resistance (5.5 ohm/sq) compared to the high and unstable sheet resistance ($\geq$ 17.5 ohms/sq) of the undoped poly-Si at a silicidation temperature of 700°C. The controlling factors of grain boundary energy and interface energies will be discussed.

SESSION K7: SHALLOW JUNCTIONS AND INTEGRATION ISSUES IN FEOL

Chairs: Cyril Cabral, Jr., Francesco La Via and Stephen A. Campbell
Thursday Afternoon, April 19, 2001
Golden Gate C2 (Marriott)

1:30 PM K7.1
ELECTRICAL PERFORMANCE AND SCALABILITY OF Ni-MONOSILICIDE TOWARDS SUB 0.13 MICRON TECHNOLOGIES. Anne Lauwers, Muriel de Potter, Richard Lindsay, An Steegen, Nico Roelandts, Fred Loosen, Christa Vrancken, Karen Maex, IMEC, Leuven, BELGIUM.

Self-aligned silicides are widely used in MOS manufacturing to reduce the sheet resistance and contact resistance of the gate poly-silicon and diffusion areas. At the moment Co-silicide is the preferred self-aligned silicide for technologies below 0.25 micron because on top of its low resistivity it provides an excellent scalability and lower stress build-up as compared to Ti-silicide. To be compatible with the continuously decreasing junction depth, silicide thickness is being scaled down to lower the silicon consumption at the expense of a higher sheet resistance. Ni-monosilicide has the interesting characteristic that the same sheet resistance can be obtained with less Si consumption as compared to Co-disilicide. In addition, it is known that the stress build-up during Ni-silicidation is lower as compared to Co-silicide. In this work the relationship between the silicide thickness, sheet resistance and silicon consumption will be experimentally checked for Co-disilicide and Ni-monosilicide. The reverse bias leakage current of shallow Ni-silicided and Co-silicided junctions will be compared for varying junction depth and varying silicide thickness. It will be demonstrated that for a particular junction depth and for a particular sheet resistance, a lower reverse bias leakage current is obtained for a Ni-silicided junction as compared to its Co-silicided counterpart due to the reduction in silicon consumption. In previous work it has been demonstrated that the role of the Ti cap is very important for Co-silicidation. In this work sheet resistance of Ni-silicided narrow lines will be studied and scalability of Ni-silicidation with and without Ti cap will be discussed.

1:45 PM K7.2
A STUDY ON SOLID PHASE REACTIONS OF Ni, Pt and Ta ON Si-Ge ALLOYS AS CONTACTS TO ULTRA-SHALLOW P^+N JUNCTIONS FOR CMOS TECHNOLOGY NODES BEYOND 70NM. Jing Liu, Hongxiang Mo and Mehmet C. Öztürk, Department of Electrical and Computer Engineering, North Carolina State University, Raleigh, NC.

Recently, selectively deposited, in-situ boron doped strained Si-Ge layers were successfully used to form p^+n junctions that meet the source/drain junction requirements of CMOS technology nodes beyond 70 nm. Strained Si-Ge is attractive as an intermediate contact layer due to its above equilibrium dopant activation and narrower

bandgap which provides a smaller Schottky barrier height, essential for low contact resistance. Previous research on the metal/SiGe system mainly focused on Co and Ti solid phase reactions to form self-aligned germanosilicide contacts. Efforts on Co were largely unsuccessful. Ti germanosilicide showed promise, however, similar to $TiSi_2$, it involved the C49-C54 phase transformation, which is likely to be problematic on thin polysilicon lines. The objective of this study is to find a better silicide (or germanosilicide) material on Si-Ge junctions. In this study Ni, Pt and Ta were considered as three candidates. Metal deposition on Si-Ge was achieved by sputtering. Among the metals considered, Ta, Pt and Ni reached a low resistivity phase upon annealing at various temperatures. X-ray diffraction results suggest that Pt and Ni form the low sheet resistance, mono-germanosilicide phases of Pt(SiGe) and Ni(SiGe) around 350°C. For Pt, low sheet resistance was preserved upon annealing up to 750°C. On the other hand, Ni germanosilicide was less stable and its sheet resistance steadily increased above 500°C. Ta required 800°C to reach the low resistivity phase. For Ta, at 800°C a pure disilicide was formed instead of a germanosilicide. For Ni, Pt and Ta, XRD results indicate a SiGe peak which corresponds to an alloy with a higher Ge percentage, which may imply the presence of a Ge rich layer immediately under the germanosilicide (or silicide). This is expected to lead to a lower bandgap material under the contact metal resulting in a lower contact resistance.

2:00 PM K7.3
$CoSi_2$ THERMAL STABILITY IMPROVED BY A NITROGEN IMPLANT. Alessandra Alberti, Francesco La Via, CNR-IMETEM, Catania, ITALY; Sebastiano Ravesi STMicroelectronics, Catania, ITALY.

Silicides are widely used in the ULSI technology for many applications. They are becoming essential to counteract the increasing resistance of contacts and interconnects on bipolar as well as on MOS transistors. Cobalt silicide ($CoSi_2$) is usually preferred to other silicides because of its low resistivity (15-20 $\mu\Omega$ •cm), high chemical and good thermal stability. In most applications thin silicide layers are employed on polycrystalline silicon, and are covered by a thick oxide layer deposited by CVD (vapox). In this work, a standard vapox/$CoSi_2$/poly-silicon multilayer (300/70/130 nm) has been studied under high temperature anneals between 850 e 1100°C and compared to an uncapped silicide as reference sample. It was demonstrated by sheet resistance measurements that the thick silicon oxide cap (vapox) does not further contribute to silicide degradation upon anneals but even improves the layer stability. Surface agglomeration is then reduced but the $CoSi_2$/Si interface continues to be considerably modified by the anneal. To improve the stability of the multilayer, the silicide/poly-silicon interface was modified by implanting nitrogen into the substrate before silicidation. Using nitrogen at sutable energy and dose, the roughnening process at the silicide/silicon interface has been considerably slowed down, as demonstrated by Rutherford Backscattering Spettroscopy (RBS) and Transmission Electron Microscopy (TEM) analyses. Nitrogen is able to pin the silicide/silicon interface and even delay the grooving process at the grain boundaries. Structural modification upon anneal at high temperature, i.e. layer agglomeration and hole formation through the silicide, directly affect the sheet resistance of the multilayer structure. Once using nitrogen, which delays the structural degradation of the multilayer, the process window for electrical stability was considerably extended by 75°C. The improvement of the silicide stability was finally modelled in terms of substrate amorphization and formation of cavities which are confined at the silicide /silicon interface during silicidation.

2:15 PM K7.4
$CoSi_2$ FORMATION USING A Ti CAPPING LAYER - INFLUENCE OF PROCESSING CONDITIONS ON $CoSi_2$ NUCLEATION. Christophe Detavernier, Roland Van Meirhaeghe, Universiteit Gent, Dept. Solid State Sciences, Gent, BELGIUM; Karen Maex, Imec, Leuven, BELGIUM.

To improve the robustness of the cobalt silicidation process, a reactive Ti capping layer may be used to protect the silicidation reaction from oxygen contamination. However, the Ti capping layer does not act as a purely passive, protective coating during the silicidation reaction. Instead, the presence of a Ti capping layer directly influences the nucleation of the $CoSi_2$. Firstly, the presence of the capping layer induces an increase in the formation temperature of $CoSi_2$ (by about 60-80°C). Secondly, the $CoSi_2$ that is formed in the presence of a Ti capping layer has a strong preferential (220) orientation. In a standard two-step SALICIDE process, several parameters must be chosen: layer thickness, temperature and duration of RTP1, selective etching chemistry and temperature and duration of RTP2. In this work, a detailed study was made to determine the influence of several processing parameters on the nucleation temperature and preferential orientation of $CoSi_2$ in the Ti/Co/Si system. For increasing thickness of the Ti capping layer, decreasing thickness of the Co layer, increasing RTP1 temperature and single step etching, the largest increase in nucleation temperature is observed. The amount of preferential (220) orientation is correlated with the formation temperature: the higher the temperature at which the $CoSi_2$ is formed, the stronger the preferential orientation. It will be shown that both the increase in nucleation temperature and the preferential orientation are caused by the presence of a small amount of Ti that has diffused from the capping layer into the CoSi layer and that acts there as a contaminant. Finally, it will be shown that the addition of Ni (i.e. a Ti/Co/Ni/Si or Ti/Ni/Co/Si structure) decreases the nucleation temperature of the $CoSi_2$.

2:30 PM K7.5
THIN FILM EDGE INDUCED STRESSES IN SUBSTRATES. S.P. Wong, H.J. Peng, Chinese University of Hong Kong, Department of Electronic Engineering and Materials Science & Technology Research Centre, Hong Kong, CHINA; Shounan Zhao, South China University of Technology, Department of Applied Physics, Guangzhou, CHINA.

It is well known that stresses in the substrate are of importance in Si technology and film edge can produce large and localized stress in the silicon substrates. There has been substantial amount of both theoretical and experimental research efforts in the past two decades to study the problem of film-edge induced stresses in substrates, including the micro-Raman study of localized stress distribution in Si induced by long stripes of metal or metal silicide thin films. However, a satisfactory analytical solution has not been available so far in the literature. In this work, we shall report on the exact solutions of linear elasticity we have obtained for this problem. The substrate in consideration is of finite thickness H in the y direction and extends to infinity in the x and z directions. It is half-covered by a thin film on the left half xz-plane (y=0 and x<0). Far from the film edge and on the side without the thin film, all stress components are zero. Far from the film edge and under the thin film, the stress distribution is in accordance with that given by the bimetallic strip theory. On the surface except right at the film edge, and at the bottom of the substrate, the normal stress component σ_{yy} vanishes. With this solution, the stress distributions in substrates under the edges of long strips or long windows of thin film can also be obtained by superposition. Examples of comparison between experimental results reported in the literature and theoretical results derived from these exact solutions will be presented. This work is partially supported by the Research Grants Council of Hong Kong SAR (Ref. No.: CUHK 4155/97E).

3:15 PM K7.6
PLASMA ASSISTED JET VAPOR NITRIDIZATION OF SiO_2 DEPOSITED ON Si. Vidyut Gopal, Alain Duboust, Liang Chen, Applied Materials Inc., Santa Clara, CA.

We have investigated the nitridization of 2.5 nm thick SiO_2 films deposited on Si wafers for gate dielectric applications. A N_2 plasma with He as the carrier gas was generated in an applicator by using a microwave excitation source. The plasma was introduced as a high-velocity jet into a modified Applied Materials CVD chamber. High-energy nitrogen species in the plasma impinged on the wafer surface and diffused through the oxide to form silicon oxynitride (SiON) with a higher dielectric constant than SiO_2. The use of plasma enabled the nitridization to be carried out at room temperature, making this process very attractive due to the low thermal budget. Here, optical emission spectroscopy was used to study the N_2/He plasma generated by varying parameters such as N_2 composition, excitation power, gas pressure and flow rate. Wafers were processed under the same conditions. The increase in thickness of the oxide film due to nitrogen incorporation, and the uniformity of the nitridization were monitored by ellipsometry. The intensity of representative nitrogen-related emission lines correlated well with the trends in film thickness for different processing conditions. Our results indicate that optimum nitridization resulted under conditions of high gas flow rate (several standard liters per minute) and low chamber pressure (below 1 Torr), and by using a high spacing (10-50 cms) between the applicator and the wafer. A low N_2 concentration (less than 15 % by volume) was found to produce the highest film thickness and the best uniformity. The excitation power was found not to have a strong impact on the efficiency of nitidization. This is significant since higher power would lead to more plasma contamination and film damage. Possible explanations for the observed trends will also be presented.

3:30 PM K7.7
DETECTING ELECTRICAL CHARGE IN THE ULTRA THIN SILICON OXIDE LAYER BY Hg-SCHOTTKY CAPACITANCE-VOLTAGE METHOD. Dennis Liu, Vladimir Drobny, and John Moquin, Texas Instruments, Tucson, AZ; Qi Wang and Hossein Paravi, Fairchild Semiconductor, West Jordan, UT.

The electrical charge or charge trapping phenomena in the ultra thin

silicon oxide layer (or any thin dielectric layer) is one of the most serious challenges in wafer processing. The trapping process is often releated to the impurities, contaminations, as well as the sub-stochiometry of the oxide layer at interface. This issue becomes especially critical as device is scaled down toward 0.1 um range. The traditional MOS Capacitance-Voltage (MOS CV) method which has been used to study the electrical charge in relative thicker dielectric layer on semiconductor can not detect the charge in the ultra thin silicon oxide layer. This work has developed a new concept/method to study the electrical charge in the ultra thin oxide layer by using Hg-Schottky Capacitance-Voltage (Schottky CV) measurement. The silicon thermal oxide layer about 12A in thickness with and without Cu-doped have been tested with this new method. The results show that this new method can be used to qualitatively identify the electrical charge trapped in the ultra thin silicon oxide layer and the possible contamination associated with the trapping level. The interaction among sub-stochiometric oxide structure, imbedded metal impurities, and Schottky CV measurement have been discussed in detail.

3:45 PM K7.8
ELECTRICAL AND STRUCTURAL PROPERTIES OF CATALYTIC-NITRIDED SiO_2 FILMS. Akira Izumi, Hidekazu Sato and Hideki Matsumura, JAIST (Japan Advanced Institute of Science and Technology), Ishikawa, JAPAN.

Low-temperature nitridation of SiO_2 surface has performed using activated species produced by catalytically decomposed NH_3 on heated tungsten. The properties of catalytic-nitrided SiO_2 films were investigated, and following results are obtained. 1) The surface of SiO_2/Si(100) is nitrided at temperatures as low as 200°C. 2) XPS spectra of N(1s) revealed that the incorporated nitrogen atoms are bound to silicon and oxygen in the SiO_2 films and the SiO_2 film is nitrided about 10 at. %. 3) Angle-resolved XPS measurements reveal the position of the nitrided layer is located at the top-surface of SiO_2. 4) The dielectric constant is controlled from 4.0 to 4.4 with changing the nitridation time. 5) C-V measurements reveal that small injection type hysterisis is completely disappeared after the nitridation treatment. Above results indicate that the catalytic-nitrided SiO_2 is useful for future ULSI gate insulator.

4:00 PM K7.9
ATOMIC SCALE NITRIDATION OF SILICON OXIDE SURFACES BY REMOTE-PLASMA-EXCITED NITROGEN. Yoji Saito, Koichi Tokuda, Seikei Univ, Dept of Electrical Engineering and Electronics, Tokyo, JAPAN.

Nitrogen incorporation into the silicon dioxide gate dielectric at the polycrystalline silicon gate interface is effective prevent the transport of boron to the substrate in MOS devices. We have incorporated several percent of nitrogen only near the top surfaces of thermally grown oxides by surface fluorination at room temperature followed by an atomic nitrogen treatment at 550°C. The process gases contain no hydrogen, which can induce electronic traps in the films. The thin oxide films, 5-10 nm thick, formed on silicon substrates were exposed to unexcited F_2 diluted in He for 1-2 min, where the partial pressure of F_2 was 0.01-0.05 Torr. Then, N_2 gas was introduced into the reaction chamber through a plasma discharge tube: the total pressure was maintained 0.4-1 Torr and the applied microwave power (2.45GHz) was 90 W. The typical nitridation time was 60 min. The depth profiles and the bonding of incorporated nitrogen atoms have been studied by angle-resolved x-ray photoelectron spectroscopy. MOS devices were fabricated using the nitrided oxide films without hydrogenation and boron doped polycrystalline silicon gate, and measured capacitance-voltage, C-V, characteristics. We confirmed that the nitrided oxide would prevent the boron penetration in comparison with the conventional oxide films. The proposed technique identifies a unique process for obtaining high quality ultrathin dielectrics.

4:15 PM K7.10
A COMPARATIVE STUDY OF THE THICKNESS EVALUATION OF ULTRATHIN GATE OXIDE USING VARIOUS TECHNIQUES. Hyosik Chang and Hyunsang Hwang, KJIST, Dept of MS&E, Kwangju, KOREA; Hyunkyong Kim, Hyunmo Cho, Hwackjoo Lee and Daewon Moon Korea Research Institute of Standards and Science, Taejon, KOREA.

Accurate Determination of gate oxides thickness is critical for the development of ULSI devices. To estimate the accuracy of various methods, Medium Energy Ion Scattering (MEIS), spectroscopic ellipsometry (SE), high-resolution transmission electron microscopy (HRTEM), capacitance-voltage (C-V) and current-voltage (I-V) analysis were performed to determined the physical thickness of silicon dioxide films prepared by standard industry process. MEIS can analyze the composition and structure of ultrathin films with atomic layer depth resolution (_0.4nm). The thickness determined by the Si MEIS peak was 1.5 nm thicker than that by the O MEIS peak. The thickness determined by SE and TEM was between the two values, while SE gave ~0.3 nm thicker value. Including the thickness of interface, TEM thickness approached that of Si MEIS peak thickness. Due to the high leakage current of ultrathin gate oxide, conventional methodology for extracting oxide thickness using accumulation capacitance at high electric field is not acceptable. Considering universal relationship of accumulation layer thickness and the oxide electric field, it is possible to estimate oxide thickness using C-V data obtained at low electric field. In addition, based on accurate modeling of Fowler-Nordheim and direct tunneling current for wide range of oxide thickness, we have obtain accurate oxide thickness. The electrical thickness was very close to the thickness determined by O MEIS peak thickness. Comparison and correlation of these measurement results allows us to obtain a precise value of the oxide thickness down to 2nm.

4:30 PM K7.11
ION BEAM SYNTHESIZED GROUP IV NANOCLUSTERS IN SiO_2 LAYERS: A PROMISING APPROACH FOR NON-VOLATILE MEMORIES AND SILICON BASED LIGHT EMITTERS. T. Gebel[a,b], L. Rebohle[a,b], J. Zhao[a], J.v. Borany[a], K.-H. Stegemann[c], B. Mrstik[d] and W. Skorupa[a,b], [1]Forschungszentrum Rossendorf, Institute of Ion Beam Physics and Materials Research, Dresden, GERMANY; [b]Nanoparc GmbH, Dresden-Rossendorf, GERMANY; [c]ZMD GmbH, Zentrum für Mikroelektronik Dresden, Dresden, GERMANY; [d]Naval Research Laboratory, Code 6816, Washington, DC.

Ion beam synthesis (IBS) as a powerful tool for the modification of ultrathin layers allows the formation of functional nanostructured layers for micro- and optoelectronics. Such modified SiO_2 layers are promising candidates for future non-volatile memory devices. Furthermore SiO_2 layers containing nanostructures produced by IBS using group IV elements show strong blue-violet photo- and electroluminescence (EL) which is of great interest for novel optoelectronic devices. In this paper we will report on our recent progress in the microstructural and electrical investigation of Ge and Si rich silicon dioxide layers. The group IV elements were implanted into thermally grown SiO_2 layers to atomic concentrations of 0.3 .. 6% followed by different annealing steps. The microstructural properties were investigated using TEM, RBS and EDX. Electrical measurements using IV, Photo - IV and CV methods were focused on the injection and conduction mechanism as well as charge storage properties. The determined position of the charge centroid correlates well with the microstructural results. It will also be shown by a method combining IV and CV measurements that not only electron injection from the substrate but also hole injection from the top electrode takes place. A direct comparison of these results to the EL properties provides new impact in the understanding of the EL excitation mechanism.