SYMPOSIUM L

Materials, Technology, and Reliability for Advanced Interconnects and Low-k Dielectrics

April 16 – 20, 2001

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TUTORIAL

ST L/N/EE: ADVANCED TECHNIQUES FOR MATERIALS CHARACTERIZATION AND RELIABILITY TESTING

Monday, April 16, 2001
1:30 p.m. - 5:00 p.m.
Salon 10/11 (Marriott)

Advanced microelectronic interconnection structures make use of high-conductivity copper conductors with low dielectric-constant insulators at extremely small dimensions. As a consequence, issues arise in the characterization and reliability of these structures that are not found in the well-used aluminum-silica system. Differences appear in: the microstructure of the copper metallization and the changes induced in it by processing, thermal loading and electromigration; the mechanical characteristics of the surrounding dielectric; and, the resulting interdependence of the reliability of the interconnection structure and the changes in the metal microstructure as constrained by the dielectric. This tutorial will cover these topics, introducing participants to the issues involved and the fundamental reliability concerns for both the metallization and its supporting dielectric encapsulant. Advanced methods for characterizing electromigration behavior (especially that of copper), mechanical properties of dielectrics (especially those of low-k materials), and metallization microstructure (by X-Ray diffraction) will be described.

Instructors:
Du Nguyen, IBM Microelectronics
Hari Rathore, IBM Microelectronics
Robert F. Cook, University of Minnesota
Stuart R. Stock, Georgia Institute of Technology

SESSION L1: Cu/LOW-k INTEGRATION AND PROCESSING
Chair: Robert D. Miller
Tuesday Morning, April 17, 2001
Golden Gate B2 (Marriott)

8:30 AM *L1.1
HIGH PERFORMANCE SILK(TM)/COPPER BEOL INTERCONNECTS. Jeffrey C. Hedrick, E.P. Barth, G.A. Biery, S. Cohen, T. Dalton, C.R. Davis, K.W. Lee, V. McGahay, H.A. Nye, D. Restaino, C. Tyberg, E. Simonyi, R.D. Goldblatt and J.G. Ryan, IBM Semiconductor Research and Development Center, Thomas J. Watson Research Center, Yorktown Heights, NY.

Back-End-of-Line (BEOL) interconnect performance improvement requires the reduction of resistance and capacitance. IBM introduced copper metallization for the 0.22 mm technology node and a lower permittivity fluorosilicate glass for the 0.18 mm technology node. For the 0.13 mm technology generation, a low-k thermosetting polymer, SiLK(TM), will be integrated copper and implemented into manufacturing. This will be the first true low-k dielectric to be fully integrated with copper wiring. The selection of SiLK(TM) and the challenges of low-k integration will be described.

9:00 AM L1.2
ADHESION STUDY BETWEEN MATERIALS FOR INTEGRATION OF COPPER AND INORGANIC LOW-k DIELECTRICS. Filip Lanckmans[a], S.H. Brongersma, S. Poortmans, T. Conard, H. Bender, E. Beyne, K. Maex[a], IMEC, Leuven, BELGIUM, [a]also at E.E. Dept., K.U.-Leuven, BELGIUM.

Copper and low-k materials are chosen to replace aluminum/silicon dioxide based interconnects for improving the density and the performance of interconnects. A main challenge regarding reliability is the adhesion between the various materials used in the back end of the line. In this work, shear testing is used to quantitatively determine the adhesion strength. The focus is put on the interfaces between several inorganic low-k dielectrics, hard mask materials and metals (copper and barriers). The inorganic materials form an important class among the low-k dielectrics. A distinction can be made between chemical vapor deposited SiO_xC_y based materials (k≈3) and porous silicon dioxide based spin-on dielectrics (k≈2). Besides silicon dioxide, silicon carbide and nitride are used as hard mask materials. The test structure itself consists of circular copper dots placed on top of different layers. During shear testing, a needle pushes laterally against the copper dot until failure occurs at the weakest interface (adhesive failure) or within the weakest material (cohesive failure). The maximum needle force is monitored. By changing the presence or the sequence of the different materials in the test structure, several types of interfaces can be evaluated. The influence of different heat treatments and size of the copper dots is discussed. X-ray photoelectron spectroscopy, scanning electron microscopy and auger electron spectroscopy provide a deeper understanding of the failed interface and are necessary to explain the measured shear test data. Based on the experimental data, finite element simulations are carried out to calculate the stresses in the structure before failure. The simulations allow predicting the failure behavior when several parameters are changed, such as the shape of the test structure, the thickness of the different layers and the material properties.

9:15 AM L1.3
CMP GOVERNING PROPERTIES OF POROUS SILICA ILD FILM (ALCAP^{TM}-S). Hiroyuki Hanahata, Takaaki Ioka, Miki Miyamoto, Sanae Kamano, Akiko Kageyama, Tsuneaki Tanabe, Asahi Chemical Industry Co., Ltd, Central Technology Laboratory; Shinya Matsuno, Asahi Chemical Industry Co., Ltd, Analytical and Computational Laboratory, Shizuoka, JAPAN.

The porous silica ILD films (ALCAP^{TM}-S) whose dielectric constants were in range 1.7-2.8 were successfully prepared via organic polymer / silica hybrid and an attempt was made to correlate the basic properties such as Young's modulus, hardness, and cohesive strength with CMP compatibility. In addition to these properties the effect of the film thickness was also studied. Main issues at CMP are reported to be cohesive failure as well as delamination between the film and a cap layer, however, the former can be avoided when the cohesive strength becomes >60 MPa, evaluated by the modified Stud-pull test) and the latter by an increase in Young's modulus and hardness without hysteresis loss. Surprisingly, results on a tape-pull test were found to be affected by the modulus and hardness and could be a measure of delamination at CMP. With decreasing the film thickness below 0.5 μm, the film tends to be CMP compatible, mainly due to an apparent increase in the modulus and hardness by the substrate effect.

9:30 AM L1.4
EFFECTIVE DIELECTRIC CONSTANT OF INTERCONNECT STRUCTURES COMBINING SPIN-ON LOW-k DIELECTRIC, ETCH-STOP, AND HARDMASK LAYERS. Shilpa Thanawala, Lei Jin, Fan Zhang, Zhefei Chen, Jude Dunne, Brian Daniels, Honeywell International, Honeywell Electronic Materials, Sunnyvale, CA.

Low-dielectric constant materials (k < 3) have found widespread application in recent years in the semiconductor industry. Films comprised of SiOxCy materials are deposited by CVD and have dielectric constants in the region of 2.6 to 2.9. Organic (polyarylene ether) and siloxane polymers are spin deposited and have a dielectric constant between 2.5 and 2.8. Nanoporous silica films are also spin deposited and have dielectric constants in the 1.9 to 2.4 regime. Typically these low-k materials are integrated with etch-stop and hardmask layers such as SiNx (k ~ 8) and SiCx (k ~ 5) which increase the effective dielectric constant of the combined stack. In addition SiNx and SiCx are typically plasma-deposited and can damage low-k materials, thereby further increasing the effective dielectric constant of the stack. This paper presents an alternate integration scheme through the substitution of SiNx and SiCx etch-stop and hardmask layers with low-k spin-on etch-stop and hardmask layers. Nanoporous silica dielectric (Nanoglass^{TM}) layers were integrated with both low-k organic and siloxane based spin-on etch-stop and hardmask layers. The effective dielectric constants of both stack types were measured. The experimental results are consistent with simulations of these structures in that the effective dielectric constant of stacks containing low-k etch-stops can be substantially lower than stacks containing conventional plasma-deposited etch-stops. Thermal and mechanical data, including thermal stability, adhesion, hardness, and elastic modulus are also reported. Integration issues such as etch selectivity and exposure to standard Cu CMP conditions will also be discussed.

9:45 AM L1.5
VIA POISONING-FREE DUAL DAMASCENE ETCHING FOR ORGANIC LOW-k MATERIAL INTEGRATION. Yu Chang Kim, Min Chul Kil, Yun Seok Cho, Jin Woong Kim, Hee Koo Yoon, Hyundai Electronics Industries, Memory R&D Div, Ichon, KOREA.

Dual damascene processes have been investigated in the integration of organic low dielectric constant (low-k) material such as SiLK-H (k = 2.7). Among the dual damascene scheme, via first dual damascene full etch (VFDD-F) scheme has the advantages in the process performance and process reliability over any other dual damascene scheme in oxide and also low-k dual damascene process. But we found that the integration of SiLK-H using VFDD-F scheme has process issues such as via poisoning and non-uniform DUV photoresist (PR) via-filling, at trench mask patterning. The former induces cylindrical defects over via pattern because via overhang-PR acts as a micro-mask during trench hard mask (HM) oxide etch. And the latter causes etch-through of underlying metal etch barrier and attack of underlying metal in some damascene pattern because underlying metal etch barrier is exposed directly to plasma during trench etch. So the solution to such process issues relating SiLK-H VFDD-F scheme was driven to look

for. We etched SiLK-H with oxidizing gas, O_2/N_2, using ECR etcher with high-density plasma source. And then we developed trench HM oxide etch recipe with low selectivity to DUV PR to remove trench HM oxide and via overhang-DUV PR simultaneously. Also VFDD partial etch (VFDD-P) scheme that SiLK-H at via is etched partially was employed. VFDD-P scheme offers the advantage over VFDD-F scheme with respect to DUV PR via-filling, inhibiting etch-through of the metal etch barrier as a result. The combination of trench HM oxide etch with low selectivity to DUV PR and VFDD-P scheme promises well-defined SiLK-H dual damascene integration excluding process issues above mentioned in SiLK-H VFDD-F scheme.

SESSION L2: CVD LOW-k DIELECTRICS

Chair: Andrew J. McKerrow
Tuesday Morning, April 17, 2001
Golden Gate B2 (Marriott)

10:30 AM *L2.1

INTEGRATED CVD LOW k TO 0.10μm AND BEYOND.
Hichem M'Saad, Applied Materials, Inc., Dielectric Systems and Modules, Santa Clara, CA.

This paper discusses the integration aspects of chemical-vapor deposited low k dielectric films in copper dual damascene structures, starting with an FSG/SiN dielectric/Cu diffusion barrier baseline at the 0.15μm technology node and transitioning to Black Diamond^{TM}/BLOk^{TM} in more advanced 0.13-0.10μm devices.
In FSG/SiN structures, reliability testing demonstrated that interface delamination is a function of the hydrogen content in the nitride. This finding has led to the development of a low hydrogen damascene nitride. Furthermore, a correlation between the deposition chemistry of the PECVD FSG and the stability of the film is demonstrated. Fluorine was found to outdiffuse to adjacent layers when deposited using silane precursor while it remains bound in the FSG film when deposited using TEOS-based chemistry. Hence, fluorine in silane-based FSG is not tightly bound to the silicon even at very low concentrations ([F]<4 at.%). Indeed, this fluorine outdiffusion is responsible for observed catastrophic failure of the FSG/low hydrogen nitride structures when subjected to furnace anneal. No failure was observed with TEOS FSG. For these reasons, the combination of TEOS FSG/low H SiN is more appropriate as first generation dielectric films in copper dual damascene structures.
For $\leq$0.13μm Cu damascene, ILD and barrier/etch stop k reduction were achieved by substituting Black Diamond^{TM} for FSG and BLOk^{TM} for SiN. BLOk^{TM}, being a CVD hydrogenated amorphous silicon carbide, showed similar electrical leakage and Cu diffusion performance to the low hydrogen SiN with an added advantage of a lower k.
Prior to SiN or BLOk^{TM} deposition, copper oxide needs to be removed since CuO can reduce electromigration lifetimes, increase via resistance and cause poor adhesion at the Cu/dielectric interface. However, CuO removal can result in the formation of copper silicide and hillocks. It is demonstrated that these side effects can be eliminated through the control of the kinetics of the ammonium treatment process.
Black Diamond^{TM}/BLOk^{TM} dual damascene integration showed an etch selectivity >10:1 and a 35% reduction in capacitance relative to oxide/SiN. Excellent profile control was achieved without a middle etch stop. Good adhesion properties and compatibility to CMP have also been achieved. Black Diamond^{TM} has been successfully integrated in an eight level metal dual damascene structure while maintaining reliability standards. The extension of CVD low k to $\leq$0.10μm generation was demonstrated with a Black Diamond^{TM} film of k less than 2.5. Single damascene integration results of this film will be described.

11:00 AM L2.2

PATTERNING OF LOW-k CVD FILMS. Hilton G. Pryce Lewis, Karen K. Gleason, Daniel D. Burkey, Massachusetts Institute of Technology, Dept of Chemical Engineering, Cambridge, MA; Gina L. Weibel, Christopher K. Ober, Dept of MS&E, Cornell University, Ithaca, NY.

Thin films produced by chemical vapor deposition (CVD) show promise as materials capable of undergoing patterning by lithographic means. In this paper, we consider the use of fluorocarbon and organosilicon films deposited by hot filament CVD (HFCVD) for producing nanometer-scale features. HFCVD is a non-plasma technique which offers the ability to tailor the chemistry of films with polymer-like structure. Both fluorine- and silicon- containing polymeric materials are under consideration as candidates in next-generation microelectronics technologies. Their transparency makes them ideal resist candidates for 157-nm lithography, and their low dielectric constant makes them strong contenders as interconnect materials. As one part of this paper, we present a collaboration aimed at merging the role of resist and low-k dielectric. Specifically, we are investigating a direct dielectric patterning process in which a material is deposited by CVD, exposed, and developed using no wet chemistry. The film is exposed using e-beam or a 157-nm source, and developed using supercritical CO_2 as a dry developing medium. The patterned film then serves as a low-k interconnect material. This technology would greatly simplify future device manufacture by reducing the number of steps involved in patterning. Furthermore, supercritical CO_2 offers many processing advantages over wet development, including improved resolution and the prevention of pattern collapse. With such a scheme, we have demonstrated positive-tone contrast in fluorocarbon HFCVD films and fully-developed images of 500-nm have been obtained from e-beam exposure. In another aspect of this work, the novel structure of organosilicon HFCVD films makes them potentially exciting materials for nanofabrication. Thin films deposited from cyclic precursors are extremely smooth and show evidence of incorporation of ring structures. Ring size may thus determine resolution limits for patterning such a material.

11:15 AM L2.3

PECVD DEPOSITED SiCOH FILMS WITH REDUCED DIELECTRIC CONSTANTS. A. Grill, V. Patel, IBM-T.J.Watson Research Center, Yorktown Heights, NY.

Carbon doped oxide low-dielectric constant (low-k) materials comprised of Si, C, O and H, (SiCOH films) prepared by plasma enhanced chemical vapor deposition (PECVD) have been demonstrated previously with dielectric constants of about 2.7-2.8. These k values appear to be almost independent of the deposition tool or used precursor. However, the dielectric constant of such materials can be further lowered by enhancing the atomic level porosity in the films. This nanoporosity enhancement can be achieved by depositing multiphase films containing at least one thermally-unstable phase and annealing the films to remove this labile phase from the material. Dual phase materials have been prepared in the present study by PECVD from mixtures of SiCOH precursors with hydrocarbons. The films have been characterized as-deposited and after thermal anneals of up to 8 hours at 400°C by Rutherford backscattering (RBS) and forward recoil elastic scattering (FRES) and by FTIR. The dimensional stability of the materials has been determined by measuring the changes in the step heights produced in the films. The electrical properties have been measured on metal insulator silicon (MIS) structures. It was found that, after an initial anneal resulting in a significant loss of CH and some SiH bonds, accompanied by a thickness losses of up to 40%, the films stabilized. Depending on the deposition conditions, choice of the hydrocarbon, and its concentration in the feed gas the dielectric constant of the stabilized films reached values significantly lower than previously reported. These results indicate the extendibility potential of the carbon doped oxide PECVD dielectrics to future generations of ULSI chips.

11:30 AM L2.4

IMPROVEMENT OF THE PROPERTIES OF LOW DIELECTRIC CONSTANT PLASMA POLYMERIZED DECAHYDRON-APHTHALENE THIN FILMS BY THE POST-DEPOSITION HEAT TREATMENT. Jaeyoung Yang, Cheonman Shim and Donggeun Jung Department of Physics, Brain Korea 21 Physics Research Division and Institute of Basic Science, Sungkyunkwan University, Suwon, SOUTH KOREA.

Effects of post-deposition heat treatment on the properties of plasma polymerized decahydronaphthalene (PPDHN) thin films were studied. For the PPDHN thin film with as-deposited relative dielectric constant k of 2.53, as the heat treatment temperature increased from 150°C to 350°C, k decreased from 2.45 to 2.13. With the increase of the temperature of heat treatment, thermal stability of the PPDHN thin film improved. Changes of the k value and thermal stability were related to changes of C-H, C=O and O-H group density.

11:45 AM L2.5

CAP FILMS AFTER CMP FOR COPPER PLUS LOW-k INTERCONNECTS. S. Gates, S. Cohen, J. Fitzsimmons[a], D. Restaino[a], C. Parks[a], E. Simonyi, S. Purushothaman IBM T.J. Watson Research Center, Yorktown Heights, NY; [a]IBM Microelectronics, Hopewell Junction, NY.

Integration of copper interconnects with a low-k dielectric requires a thin dielectric barrier used to terminate each damascene layer after chemical mechanical polish (CMP), known as the "post-CMP Cap". Amorphous SiNitride and SiCarbide are candidates for the post-CMP Cap. We report here on amorphous Si, C, H alloy (a-SiCH) films deposited by PE CVD from methylsilane precursors, and on the addition of NH3 to the deposition chemistry to produce Si, N, C, H alloys ("SiNCH"). Basic film properties for these films (k, I-V curves, hardness, modulus) will be discussed. Investigations of the Cu barrier properties of these materials using electrical (triangular voltage sweep) and analytical (SIMS profile) methods will be presented.

SESSION L3: SPIN-COATED LOW-K DIELECTRICS
Chair: Filip Stefaan Lanckmans
Tuesday Afternoon, April 17, 2001
Golden Gate B2 (Marriott)

1:30 PM *L3.1
NANOPOROUS, LOW DIELECTRIC CONSTANT ORGANOSILICATE MATERIALS DERIVED FROM INORGANIC/ORGANIC POLYMER BLENDS. Willi Volksen, Robert Miller, Teddie Magbitang, Craig Hawker, James Hedrick, Elbert Huang, Mike Toney, Phil Rice, Robert Zafran, IBM Almaden Research Center, San Jose, CA; Ken Rodbell, Steve Cohen, Michael Lane, IBM T.J. Watson Research Center, Yorktown, NY; Kelvin Lynn, Mihail Petkov, Mark Weber, Washington State University, Pullman, WA; Paul Ho, Michael Kiene, University of Texas, Austin, TX; Matthew Stavis, Oberlin College, Oberlin, OH.

The approach of introducing porosity to lower the dielectric constant of known dielectric materials is most readily realized for silicates. Within this class of materials, the organosilicates, which exhibit significantly lower dielectric constants as compared to SiO_2, can be readily converted into nanoporous coatings by a variety of approaches. One such approach, reported previously, utilizes inorganic/organic polymer hybrids derived from a thermally decomposable organic component dispersed in an organosilicate matrix. Nanoporous coatings are then formed by heating spin-coated thin films of the inorganic/organic polymer blends to elevated temperatures. The proper selection of hybrid components with respect to pore generator architecture, molecular weight of both organic and inorganic polymers as well as formulation solvent are critical in being able to reproducibly generate nanoporous structures. Formulation considerations, such precursor selection, solution stability and coating quality, as well as coating characterization with respect to mechanical, electrical, thermal and structural aspects will be presented.

2:00 PM L3.2
DESIGN OF ULTRA LOW-DIELECTRIC CONSTANT ORGANOSILICATES USING BLOCK COPOLYMERS AS TEMPLATES. Shu Yang, C.-S. Pai, Peter Mirau, Om Nalamasu, Elsa Reichmanis, Bell Laboratories, Lucent Technologies, Murray Hill, NJ; Yaw S. Obeng, Bell Laboratories, Lucent Technologies, Orlando, FL; Eric Lin, National Institute of Standards and Technology, Gaithersburg, MD; David Gidley, Dept. of Physics, University of Michigan, Ann Arbor, MI.

As device features in next generation integrated circuits (IC) continue to shrink to increase processor speed, RC greatly limits chip performance and reliability by increasing power dissipation and wire cross-talk in multilevel interconnects. A low dielectric constant (k) material needs to be identified, which must have good thermal stability (above 400°C), low coefficient of thermal expansion (CTE), low moisture uptake, high glass transition temperature (Tg), strong mechanical properties, high electric breakdown field, good thermal conductivity and good adhesion to various substrates. A new class of organosilicate has been developed that can attain an ultra low-dielectric constant, k of less than 2.0, while exhibiting good mechanical strength. A series of triblock polymers, poly(ethylene oxide-b-propylene oxide-b-ethylene oxide) (PEO-b-PPO-b-PEO), are used as sacrificial materials in poly(methyl silsesquioxane) (MSQ) to generate pores in the MSQ matrices when heated above 400°C. Dielectric constants equal to or less than 2.0 have been achieved with high dielectric breakdown strength (> 2 MV/cm) when more than 30 wt% loading of triblock polymers. It is confirmed by both small angle neutron scattering (SANS) and positronium annihilation lifetime spectroscopy (PALS) that these materials have extremely small pores, 2-4 nm. Specular X-ray reflectivity (SXR) measurement reveals that the density decreases from 1.3 g/cm^3, the density of MSQ, to 0.8-0.9 g/cm^3, in porous MSQ. Additionally, the Young's modulus is found to be strong, $\sim$3 GPa for a material with a dielectric constant of $\sim$2.0.

2:15 PM L3.3
ZEOLITE LOW-k DIELECTRICS. Zhengbao Wang, Huanting Wang, Yushan Yan, Department of Chemical & Environmental Engineering, University of California at Riverside, Riverside, CA.

Ultra low-k materials are needed for the future generation microprocessors as device dimension continues to scale down [1-2]. One major class of low k materials that has been intensively studied is porous silica by sol-gel method [2]. Sol-gel silica offers low-k but has concerns of low mechanical strength, low heat conductivity, wide pore size distribution, and hydrophilicity [2]. Recently, surfactant-templated mesoporous materials also are studied [3, 4]. But due to their amorphous nature, mesoporous materials may face similar concerns such as low mechanical strength and hydrophilicity. Here we show that microporous crystalline pure-silica zeolites (e.g., silicalite with uniform pores of size 5.5 angstrom) offer a promising alternative as ultra low-k (e.g., as low as 2.1) materials because of their high mechanical strength, high heat conductivity, uniform pore size, and hydrophobicity. Two types of silicalite films on silicon wafer (low-R, high-R, nitride and oxide covered) were prepared. The first was by in-situ crystallization using a synthesis solution 0.32TPAOH: TEOS: 165H2O. The second type was prepared by spin-coating of silicalite nanocrystals (15-30 nm) followed by heat treatment. In-situ crystallization produces continuous films (thickness: 0.2 to 0.4 um, modulus: 30-40 GPa by nanoindentation, k: 2.7-3.0 at 1 MHz, k stability: fairly stable in ambient air RH=60%, water adsorption: none by IR, CMP compatibility: easily polished to a smooth finish). Silicalite films with higher porosity (extra inter-particle porosity is added) and lower k (e.g., k=2.1) were prepared by spin-coating of nanocrystals followed by heat treatment. [1] The International Technology Roadmap for Semiconductors, 1999. [2] R.D. Miller, Science, 1999, 286, 421. [3] P. Yang, D. Zhao, B.F. Chmelka, and G.D. Stucky, Proceedings of Sematech Ultra Low K Workshop, Orlando, Florida, March 16, 1999. [4] C.J. Brinker, Y. Lu, and H. Fan, Proceedings of Sematech Ultra Low K Workshop, Orlando, Florida, March 16, 1999.

2:30 PM L3.4
SELF-ASSEMBLED POROUS POLY(BRIDGED SILSESQUIOXANE) LOW k FILMS. Hongyou Fan and C. Jeffrey Brinker, Sandia National Lab, Albuquerque, NM.

We report an evaporation-induced self-assembly procedure to prepare a series of poly(bridgedsilsesquioxane) low k thin films that incorporate organic moieties into the nanoporous framework as molecularly dispersed bridging ligands. By varying the surfactants and co-solvent used in film synthesis, the film porosity and thereby the film dielectric constants were controlled. Capacitance-voltage measurements along with a variety of structural characterization procedures were performed to begin to elucidate structure-property relationships of this new class of surfactant-templated mesophases. Our results indicate that porous poly(bridgedsilsesquioxane) films exhibit promising mechanical and thermal stability. Sandia National Laboratories is a multi-program laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the U.S. Department of Energy under Contract DE-AC04-94AL85000.

2:45 PM L3.5
NANOPOROUS LOW-κ DIELECTRIC MATERIALS. Michael Gallagher, Nick Pugliano, Maureen Roche, Jeff Calvert, Shipley Company, L.L.C., Marlborough, MA; Yujian You, Robert Gore, Nikoi Annan, Michael Talley, Scott Ibbitson, and Angelo Lamola, Rohm and Haas Company, Spring House, PA.

Porous organosiloxane films are generated by the thermal removal of sacrificial polymer particles (porogen particles) from spin-coated films. The porosity level in the film is controlled by adjusting the ratio of porogen particles to organosiloxane matrix in the composite solution. By varying the chemical composition of the sacrificial polymers, we have been able to compatiblize the porogen particles with organosiloxane matrices as well as to adjust the temperature at which the porogen particles are removed to produce porous films. The process for preparing the porogen particles is robust and scaleable. The thin films obtained by this approach are uniform, clear, and smooth. They can be prepared at thicknesses up to1.5 micrometers and are free of cracks and delamination. Thermogravimetric analysis of the composite films indicates near quantitative removal of the porogen particles, minimal residue and no significant out-gassing upon additional thermal treatments. The pores, obtained after thermal treatment, have been shown to template the porogen particles. The mean pore size and mean particle size measured by light scattering, small-angle x-ray (SAXS) and small-angle neutron scattering (SANS) are less than 5 nanometers. The nature of porosity (closed cell), pore size and pore size distribution in the films has been examined by transmission electron microscopy, SAXS and SANS experiments. The dielectric constant of the porous organosiloxane film is tunable from a κ value of 2.8 to 1.85 and controlled by the initial porogen particle loading. Additional electrical and mechanical properties of these films will be described in this presentation.

SESSION L4: COPPER THIN FILM MICROSTRUCTURE
Chair: Stefan P. Hau-Riege
Tuesday Afternoon, April 17, 2001
Golden Gate B2 (Marriott)

3:30 PM L4.1
VOID FORMATION AT TWIN BOUNDARIES IN Cu THIN FILMS DURING THERMAL CYCLING. Atsuko Sekiguchi, Junichi Koike, Kouichi Maruyama, Tohoku Univ, Dept of Material Science, Sendai, JAPAN.

Cu thin films have attracted much attention as a new on-chip interconnect material because of its high electrical conductivity and good resistance to elctro-/stress-migration. Void formation has been reported in Cu thin films and is a major reason for device failure during processing. The present work is aimed at understanding the void formation mechanism during thermal cycling. Copper thin films of 900nm in thickness were prepared by electrolytic plating on Ta (20nm)/SiO_2 (1700nm)/Si (300mm) substrates. Stress change was determined by measuring sample curvature. The calculated mechanism map was compared with stress-temperature curves . Microstructural change was examined by SEM and TEM. Stress distribution of a void region was calculated using a three dimensional finite element method (FEM) computer code. Actual crystallographic orientations of twins were determined by Kikuchi pattern analysis and FEM calculation. Comparison between stress-temperature curves and deformation mechanism maps revealed that dislocation-glide creep is a major deformation mechanism leading to void formation during thermal cycling. SEM observation showed that void formation occurred not only at grain boundaries but also in grain interior. TEM observation showed that void formation occurred at intersecting points of twin/twin and twin/grain-boundary. FEM simulation revealed that elastic anisotropy of neighboring twin variants caused a large shear-stress concentration at twin interfaces accompanying voids. The calculation was consistent with TEM observation that dislocation density was high along twin interfaces accompanying voids while it was low along twin interfaces without voids. Based on these results, it is considered that shear stress concentration causes the twin interfaces to act as preferential dislocation glide planes, leading to dislocation pile up and void formation at the intersections.

3:45 PM L4.2
EFFECTS OF SEED THICKNESS AND BARRIER STRESS ON MICROSTRUCTURE AND STRESS EVOLUTION IN ELECTROPLATED Cu FILMS. Meike Hauschildt, Ennis T. Ogawa, Seung-Hyun Rhee, Dongwen Gan, Paul S. Ho, Univ. of Texas, Microelectronics Research Center, Austin, TX.

The development of Cu electroplating in damascene technology has highlighted an interesting phenomenon: room-temperature microstructure evolution. This process involves grain growth, texture development, and changes in resistivity and stress and strongly depends upon the deposition conditions and initial state of the deposited film. The plating process and microstructure evolution are further complicated by the interconnect trench geometry. With subsequent device scaling, better understanding of the electroplated (EP) stack must be determined, especially with regard to seed thickness, which will be limited in narrower trenches. With this in mind, we have characterized the seed thickness dependence in blanket films to provide a foundation required to understand the microstructure and plating characteristics in damascene trenches. Our results show a strong dependence of sheet resistance, stress and microstructure evolution of the EP Cu film on seed layer thickness, with an increased rate of room temperature recrystallization with decreasing seed thickness. The microstructure changes include an increase in grain size, a decrease in (111) texture strength and the development of a small (200) texture component over time. However, the changes in the film do not seem to occur at the same rate: the change in stress seems to lag the sheet resistance. A possible explanation for the lag is that resistivity identifies grain growth in the plated copper and stress describes the combined change in the seed and the EP layer. FIB imaging indeed shows that grain size changes occur in the plated Cu film before the seed and that thicker seed films transform more slowly than thinner ones. TEM and FIB grain size analyses reveal that resistance change and grain size evolution correlate well, whereas (111) texture and film stress change are concurrent. Finally, issues concerning barrier stress and annealing studies at low temperatures will be addressed.

4:00 PM L4.3
DISSOCIATION OF DILUTE Cu(Co), Cu(Nb), AND Cu(B) ALLOY THIN FILMS: RESISTIVITY, GRAIN GROWTH AND TEXTURE EVOLUTION. A. Gungor, K. Barmak, Carnegie Mellon Univ, Dept of MS&E, Pittsburgh, PA; C. Cabral Jr., IBM T.J. Watson Research Center, Yorktown Heights, NY; A. Ozcan, Boston Univ, Dept of Physics, Boston, MA; C. Lavoie, J.M. E. Harper, IBM T.J. Watson Research Center, Yorktown Heights, NY.

The dissociation of dilute, supersaturated Cu(Co), Cu(Nb) and Cu(B) alloy thin films during thermal annealing resulted in the lowest resistivity for Cu(B) and strongest $< 111 >$ fiber texture for Cu(Nb). Note that Cu(Co) belongs to category II while Cu(Nb) and Cu(B) belong to category III of the three Cu alloy dissociation modes recently proposed by Barmak et al.(2000)[1]. In category II, the solute element has finite, high-temperature solubility in Cu and the phase diagram exhibits a peritectic, while category III solutes have extremely limited solubility in Cu, even at high temperatures. Electron beam evaporated films, with two nominal solute contents of 1 and 3 at%, and three nominal film thicknesses of 50, 100, 500 nm were investigated. In Situ resistance measurements, conventional and in situ synchrotron x-ray diffraction, pole figure analysis, scanning electron microscopy, Rutherford back scattering and positron induced x-ray emission were used to follow alloy dissociation, grain growth and texture evolution in the films. In Situ resistance-temperature measurements showed that most of the resistance drop occurred during heating to the isothermal anneal temperature (0.17-6 C/s, 300 to 600 C), with the resistance changing little even after prolonged annealing. For isothermal annealing at 400 C, Cu(Nb) and Cu(Co) films showed the largest and the smallest resistance decrease, respectively, while Cu(B) attained the lowest final resistivity of all three films, comparable to that for pure evaporated Cu. By comparison to the final resistivity of Cu(B), the final resistivity of Cu(Nb) increased with decreasing film thickness, either because the dissociation did not proceed as far or because the film agglomerated more easily, or both. Annealing also resulted in grain growth and in the strengthening of film texture. The Cu(3 at% Nb) film showed the most interesting behavior by developing $< 111 >$ fiber texture, in contrast to other films, including pure Cu, which have an additional $< 100 >$ fiber component.
[1] K. Barmak, G.A. Lucadamo, C. Cabral, Jr., C. Lavoie, and J.M.E. Harper, J. Appl. Phys. 87, 2204 (2000)

4:15 PM L4.4
MICROSTRUCTURAL MANIPULATION OF COPPER FILMS VIA PULSED-LASER INDUCED MELTING AND SOLIDIFICATION. J.W. Lau, M.A. Crowder, A.B. Limanov, James S. Im, Division in MS&E, Department of Applied Physics and Applied Mathematics, Columbia University, New York, NY; A. Gungor and K. Barmak, Department of MS&E, Carnegie Mellon University, Pittsburgh, PA.

There are a number of cases where incentives exist for manipulating the microstructure of metallic films. Solidification of as-deposited metallic films represents an unusual approach that has not been as thoroughly explored as deposition or solid phase phenomena based processes (e.g. grain growth). In this paper, we show that a particular melt-mediated crystallization technique, referred to as sequential lateral solidification (SLS), can be used in order to manipulate the microstructure of copper films on either SiO_2 or a tantalum adhesion layer. SLS is a pulsed energy-beam/laser-based process, which was originally developed in order to provide low-defect density crystalline silicon films on high temperature intolerant amorphous substrates such as glass (for thin film transistors). Depending on the details of the process (i.e. beamlet pattern and translation sequence), one can obtain a variety of microstructures including location-controlled single crystal regions and grain boundary location-engineered polycrystalline films; we will present SEM and TEM micrographs of SLS processed copper films with such microstructures. For metallization applications, it should be possible to employ such a capability in order to attain electromigration resistant copper lines with enhanced conductivity. In this investigation, we have utilized three different sample configurations: 1 μm and 1000 $\AA$ copper films on oxidized Si wafers, and 1000 $\AA$ copper film on tantalum coated oxidized Si wafers. The samples were irradiated with a XeCl (308 nm, 30 ns FWHM) excimer laser at various energy densities and translation distances. Beam shaping is accomplished via a 4x demagnification projection-imaging scheme, using a mask with patterned apertures. In addition to the details of experimental findings, we will review the basic definition and the requirements of the SLS method as well as elaborating on the physical factors (i.e., interface response function, nucleation kinetics of the solid, and transient thermal profile at and near the interface) that govern the process.

4:30 PM L4.5
GRAIN GROWTH IN ELECTROPLATED COPPER. Sywert H. Brongersma, Emma Kerr, Iwan Vervoort, IMEC, Leuven, BELGIUM; Karen Maex. IMEC, Leuven and E.E. Dept, K.U.-Leuven, BELGIUM.

Electrodeposition of Copper was introduced in interconnect technology because of its potential to provide excellent filling of high aspect ratio trenches. However, it necessitates the use of several additives, e.g. a brightener [B], that also induces a less desirable phenomenon known as self-annealing where secondary grain growth occurs at room temperature over a period of days or weeks. This is accompanied by a stress reduction and a ~20% decrease in sheet resistance. The time-scale on which these changes occur depends critically on variables such as layer thickness h, plating current I, seedlayer, and the constituents of the plating bath. Using Cu layers on 8" Si(100) wafers with a native oxide and 30 nm TaN barrier layer, a detailed study on the correlation between stress, sheet-resistance, grain morphology and impurities is conducted at both room and elevated temperatures. Both higher [B] and lower I are shown to significantly lower the as-deposited tensile stress, mainly due to a higher number of impurities incorporated in to the Copper film. This is consistent with an increase in the time needed for a full anneal

because these impurities hamper grain boundary motion. Additionally, the stress decrease from tensile values to close to zero at room temperature contradicts a description in terms of the elimination of grain boundary volume, which should give a change towards a more tensile film. Thermal cycling of these layers shows a significant desorption of several C-O-H compounds between 85 and 120 C, accompanied by a stress reduction. This data, combined with a study on the evolution of grain morphology and sheet resistance at elevated temperatures for various plating conditions has now lead to a detailed understanding of the changes that occur during grain growth in our Copper layers. Apparent discrepancies with other groups will also be discussed.

4:45 PM L4.6

PROPERTIES OF SPUTTERED BILAYER WN_x /W DIFFUSION BARRIERS BETWEEN Si AND Cu. Kevin D. Leedy, Air Force Research Laboratory, Sensors Directorate, Wright-Patterson AFB, OH; M.J. O'Keefe, E.J. Dahlgren, University of Missouri-Rolla, Dept. of Metallurgical Engineering, Rolla, MO; J.T. Grant, Research Institute, University of Dayton, Dayton, OH.

Copper interconnect metallizations in next generation integrated circuits will require thin diffusion barrier layers (<20 nm) between the Cu and low-k dielectric which may also function as seed layers for subsequent material depositions. One possible structure entails an adherent lower resistivity film deposited directly on the intended diffusion barrier, such as W on WN_x. In this study, sputtered WN_x/W bilayer thin films were investigated as diffusion barriers between Si and Cu. The total thickness of the WN_x/W bilayer was fixed at 20 nm while the WN_x thickness was varied from 0 to 20 nm. After deposition of the barrier films, a 100 nm thick Cu film was sputtered over the α-W and amorphous WN_x bilayer. The as-deposited WN_x/W/Cu film stress was found to be strongly dependent on the relative amount of WN_x and W present. The influence of 400°C and 650°C inert ambient anneals on the phase stability of the Si/WN_x/W/Cu structure was also investigated. Microstructural characterization using transmission electron microscopy and x-ray diffraction and chemical analysis by x-ray photoelectron spectroscopy of the films were used to identify the as-deposited and transformed phases.

SESSION L5: DIFFUSION BARRIER & METAL THIN FILMS - DEPOSITION & INTEGRATION

Chairs: Mihal E. Gross and Ivo Raaijmakers
Wednesday Morning, April 18, 2001
Golden Gate B2 (Marriott)

8:30 AM *L5.1

ADHESION AND MECHANICAL BEHAVIOR OF BARRIERS IN INTERCONNECT STRUCTURES. Reinhold H. Dauskardt, Department of Materials Science and Engineering, Stanford University, Stanford, CA.

The drive towards smaller length scales and complexity of device structures and their packages has lead to significant challenges with regard to mechanical reliability for microelectronic technologies. Debonding of interfaces, fracture of brittle dielectric layers, stress-corrosion cracking and thermomechanical fatigue processes may occur at all levels of processing, during proof testing, or even in-service. Problems have been compounded by the implementation of new porous low-k dielectric materials, new Cu metallization schemes, and the barriers that separate them. These issues are discussed for a number of typical materials found in current interconnect structures. The effect of barrier elastic properties and thickness on the deformation of adjacent ductile metal and polymer layers will be discussed. Multiscale simulations involving interface debonding and attendant deformation of adjacent materials will be described. Models describing the kinetics of subcritical debonding including the effects of environment and temperature are reviewed.

9:00 AM L5.2

FUNDAMENTAL BEAM STUDIES OF RADICAL ENHANCED ATOMIC LAYER CHEMICAL VAPOR DEPOSITION OF NITRIDE DIFFUSION BARRIERS. Frank Greer, John Coburn, David Fraser, David Graves, U.C. Berkeley, Dept of Chemical Engineering, Berkeley, CA.

As device dimensions continue to shrink and aspect ratios continue to increase in microelectronics manufacturing, it will become increasingly difficult to deposit highly conformal thin films for applications such as copper diffusion barrier layers. Atomic Layer Chemical Vapor Deposition (ALCVD) has been proposed as one way to achieve these highly conformal thin films due to the layer-by-layer growth that is possible when a metallic precursor and a stable reactive species, such as ammonia, are introduced sequentially into a deposition chamber. One problem with conventional ALCVD is that the deposition temperatures that are required to achieve reasonable growth rates and good quality films with low impurity concentrations can be relatively high, and may turn out to be incompatible with integration of these barrier films with temperature-sensitive films such as organic low-k materials. It has been recently proposed that by using a more reactive specie like a radical as the second reactant, atomic layer film deposition at lower temperatures may be possible. This work focuses on investigating the feasibility of performing Radical Enhanced Atomic Layer Chemical Vapor Deposition (REAL CVD) of titanium nitride at low surface temperatures using TiCl4, nitrogen radicals, and hydrogen radicals. By directing independent beams of each of these species at a given surface (in this case, silicon and silicon dioxide coated on Quartz Crystal Microbalances), deposition parameters of interest such as the sticking probability and reaction probability of these species have been measured as a function of surface temperature and surface preparation. By using these parameters and a simplified model of reactive species transport, the feasibility of REALCVD of nitrides will be discussed. Various measurements of the film quality and composition including XPS and AES analysis of the deposited films will also be presented, paying particular attention to the residual chlorine content of the films.

9:15 AM L5.3

ENGINEERED LOW RESISTIVITY TANTALUM NITRIDE FILMS BY ATOMIC LAYER DEPOSITION. Ana R. Londergan, Jereld L. Winkler, Kim Vu, Lawrence D. Matthysse, Thomas E. Seidel, and Ofer Sneh, Genus Inc., Sunnyvale, CA.

Atomic Layer Deposition (ALD) is an emerging ultra-thin film deposition technique for advanced microelectronics applications. Enabling features of ALD are precise control over film thickness, excellent conformality and relative insensitivity to wafer size. Additionally, ALD allows interface and film engineering that can be utilized to maximize device performance within the minimum real estate requirements. In this work we report the results for ALD tantalum nitride films with an emphasis on film engineering. Tantalum nitride is deposited by sequential surface reactions of tantalum and nitrogen precursors. Film engineering is achieved by manipulating the surface species distribution and type following the nitrogen precursor reaction. The electrical and structural properties of these tantalum nitride films are then thoroughly characterized. Formation of several metastable phases of tantalum nitride materials is identified and correlated with a wide range in nitrogen incorporation and film resistivity. In this presentation we will discuss our strategy and data that aim at metastable useful Ta(N) films with target resistivity in the range of 500-2000 micro ohm-cm. For example, ultra-thin Ta(N) films are found to exhibit sharp interfaces, high density and 100% step coverage over aggressive topography. Specifically, applications for copper interconnect barrier and MIM capacitor electrodes will be addressed.

9:30 AM L5.4

CVD TANTALUM AND TANTALUM NITRIDE DIFFUSION BARRIER FOR COPPER METALLIZATION. Cory Wajda, Joe Hillman, Steve Caliendo, Gene Xu, TEL, Gilbert, AZ.

As feature sizes shrink and aspect ratios grow for IC copper metallization, the need for an alternative to conventional PVD tantalum based copper diffusion barriers will arise. Inorganic CVD of tantalum and tantalum nitride diffusion barriers using TaF_5 as the tantalum precursor has been demonstrated as a promising process with good step coverage, good copper barrier properties, low impurities content, low resistivity, and a low deposition temperature. This work presents a modulated CVD tantalum and tantalum nitride film stack deposited by CVD using TaF_5 as the precursor. The modulated tantalum and tantalum nitride stack consists of thin, alternating layers of plasma enhanced CVD tantalum and thermal CVD tantalum nitride. The modulated structure provides the benefits of the high step coverage and copper diffusion barrier properties of thermal CVD tantalum nitride with the low resistivity of PECVD tantalum. A warm wall, parallel plate CVD reaction chamber was used on a 200 mm cluster tool with a pre-clean chamber and an ionized PVD copper chamber, enabling fully integrated CVD tantalum barrier and PVD copper processing. The CVD deposition temperature was 350°C, and the pressure was 2 torr. Deposited films were analyzed for sheet resistance, step coverage (TEM), nitrogen to tantalum ratio and fluorine content (RBS), crystalline phase, surface roughness and density (XRD and XRR), fluorine depth profile (SIMS), and adhesion (tape tests, stud pull tests, and CMP after copper seed and electroplating). The modulated barrier has a resistivity less than 500 $\mu\Omega\cdot$cm, 50% sidewall coverage, and fluorine content of 9 atomic percent as measured by SIMS depth profile. Excellent copper diffusion barrier performance of 20 nm thick barrier films has been demonstrated. IPVD copper seed morphology and electroplating performance have also been investigated.

9:45 AM L5.5
COMPARISON OF TiN AND TiAlN AS A DIFFUSION BARRIER DEPOSITED BY ATOMIC LAYER DEPOSITION METHOD. June-Woo Lee, Jae-Hyeong Koo, Tae-Han Doh, Young-Jae Kim, Yangdo Kim, Young Do Kim, Hyeongtag Jeon, Hanyang Univ, Div of MS&E, Seoul, KOREA.

Atomic layer deposition method is one of the new deposition method to grow nano scale thin films. This method has a lot of unique advantages over other conventional chemical vapor deposition method such as an excellent thickness uniformity, conformal step coverage, low pin hole density and complete elimination of particle generation. In this experiment, we deposited the TiN and TiAlN films by this ALD method with using organometallic precursors of tetrakis(ethylmethylamido)titanium(TEMAT), dimethyl aluminum hydride-one ethyl piperdine(DMAH-EPP) and NH_3. Ti, Al sources and NH_3 reactant gas were separately supplied and Ar gas was purged between each source and reactant supply to suppress the direct reaction. The TiN and TiAlN films were grown at process pressures about 2 Torr and at various temperatures(150-300°C). The growth rate of these thin films were measured and exhibited the linear relationship with the number of process cycles. The step coverage of these films were examined by scanning electron microscopy(SEM). And the other physical properties such as the chemical composition, crystallinity and the interface morphology were examined with Auger electron spectroscopy(AES), X-ray diffraction(XRD), and transmission electron microscopy(TEM). And the diffusion barrier characteristics was measured after depositing the Cu layer on the top of TiN and TiAlN films. Etch pit test and AES analysis were conducted to examine the breakdown of the diffusion barrier characteristics and the diffusion of Cu through the diffusion barrier films. With these results we will compare the charateristics of these diffusion barriers of TiN and TiAlN and discuss the growth mechanism of TiN and TiAlN thin film which were deposited by an atomic layer deposition method.

10:30 AM L5.6
A STUDY ON THE PROPERTIES OF DIFFERENT IMP Ta, Ta(N) AND MULTI-LAYER Ta/Ta(N) AS DIFFUSION BARRIERS FOR Cu METALLIZATION. He Lei[a,b]; C.Y. Li[b]; J.J. Wu[b]; Y. Qian[b]; Kangsoo Lee[b]; Z.Q. Zeng[c]; H.D. Liu[d]; Joseph Xie[a,b], [a]Singapore-MIT Alliance, Advanced Materials Program, Singapore, SINGAPORE; [b]Institute of Microelectronics, Dept of Deep Submicron Integrated Circuit, Singapore, SINGAPORE; [c]Nanyang Technological University, School of Materials Engineering, Singapore, SINGAPORE; [d]Rudolph Technologies, Inc., Flanders, NJ.

We report a study on the properties of Ionized Metal Plasma (IMP) Ta, Ta(N) and multi-layer Ta/Ta(N) based on a comparative evaluation of their performance as diffusion barriers in Cu based metallization schemes. The film structures used in this study are: IMP Cu(2000Å)/IMP Ta(250Å)/Si; IMP Cu(2000Å)/IMP Ta(N)(250Å)/Si; and IMP Cu(2000Å)/IMP multi-layer Ta/Ta(N)(250Å)/Si. The samples were annealed in N_2 ambient at 500°C, 550°C, 600°C and 650°C, respectively, for 30 minutes. The failure behavior and film properties of different barriers were investigated using MetaPULSE, Film stress measurement (FSM), Four-point probe (FPP), X-ray diffractometry (XRD), Rutherford backscattering spectrometry (RBS), Atomic force microscopy (AFM), and Transmission electron microscopy (TEM). It has been observed clearly from the sheet resistance measurements that failures of Ta(N) and Ta barriers occurred at 550°C and 600°C respectively, whereas the multi-layer Ta/Ta(N) could still survive from the annealing up to 650°C. Evidence showing the formation of Cu_3Si in the failed film stacks was found from XRD spectra. Based on our studies, two kinds of diffusion mechanisms coexist: one is Cu migration through barrier layers into the Si substrate, leading to barrier failure; and the other is atomic intermixing between Cu and Ta, which does not cause the barrier failure. Depending on the barrier's microstructures, the dominant diffusion mechanism is different, and the multi-layer Ta/Ta(N) has appeared to be the most robust one among the three barriers made in between the Cu layer and Si substrate.

10:45 AM L5.7
EFFECT OF SILICON CONCENTRATION IN CVD SiTiN THIN FILMS FOR DIFFUSION BARRIER APPLICATIONS AGAINST COPPER IN INTEGRATED CIRCUITS. Dalaver Anjum, Serge Oktyabrsky, Eric Eisenbraun, Alain Kaloyeros, Univ at Albany-SUNY, Albany, NY.

Ultrathin (~12 nm thick) TiSiN films were deposited by a chemical vapor deposition (CVD) process at 370 and 420°C using ammonia, silicon tetraiodide, titanium tetraiodide and hydrogen chemistry. To evaluate the influence of silicon content on the film properties, a series of films with different Si/Ti flow ratios of precursors was grown. Using the X-ray photoelectron scpectroscopy (XPS) Si concentration in the films were found to increase from 0 to ~24% as Si to Ti precursors flow ratio was increased from 0 to 30 sccm, respectively. Four-point probe results were consistent with XPS observeations and showed a gradual growth of the resistivity, from 2 m Ω·cm to 48 m Ω·cm. Transmission electron microscopy (TEM) analysis of these films revealed a reduction of the grain size (~8 nm to ~1.5) with increasing Si content. Rutherford backscattering spectrometry (RBS) of ennealed Cu/TiSiN/Si stacks confirmed the Cu diffusion through TiSiN films at 500°C annealing temperature. However, the failure was found to be the worst for pure TiN film relative to Si containing films. Cross-sectional TEM of these stacks showed Cu-silicide formation at the Si interface at 450°C in the case of pure TiN barriers, while for Si containing films silicide formation was observed only at 500°C. The results prove that application of the nanocrystalline TiSiN thin film barriers provide a significant advantage in the barrier reliability.

11:00 AM L5.8
THE INFLUENCE OF MICROSTRUCTURE IN ELECTROLESS DEPOSITED, COBALT BASED THIN FILMS ON DIFFUSION BARRIER INTEGRITY IN COPPER METALLIZATION. Amit Kohn, Moshe Eizenberg, Technion - Israel Institute of Technology, Dept. of Materials Engineering, Haifa, ISRAEL; Yosi Shacham-Diamand, Tel-Aviv University, Dept. of Physical Electronics, Ramat-Aviv, ISRAEL.

Electroless deposited cobalt based thin films were investigated as diffusion barriers for copper metallization. Electrochemical deposition can be dominated by reaction kinetics resulting in a nanocrystalline or amorphous metallic layer. This microstructure is suitable for application as a diffusion barrier as it eliminates the direct, fast diffusion path via the grain boundaries. In electroless deposition of cobalt, nanocrystalline h.c.p cobalt grains were obtained by incorporation of phosphorus and tungsten. When this non-equilibrium structure was subjected to thermal treatments, TEM and XRD studies revealed phenomena of microstructural evolution such as nucleation, crystalization, grain growth along a preferred basal plane (0002) orientation, and phase transformation. The diffusion barrier quality was evaluated by capacitance versus voltage and capacitance versus time measurements of MOS structures and compared to SIMS depth profiles. These evaluations indicate that 30 nm thick films of $Co_{0.9} W_{0.02} P_{0.08}$, $Co_{0.9} P_{0.1}$ and $Co_{0.96} W_{0.04}$ can function as effective barriers against copper diffusion up to 450°C. The relative quality of the various cobalt films as diffusion barriers and their integrity lifetime as a function of thermal treatment temperature and time are explained based on the mechanisms of microstructurul evolution.

11:15 AM L5.9
A LOW COST Cu SEED LAYER DEPOSITION FOR ULSI METALLIZATION. Ching-Han Jan, Xuan-Kai Wang, and Fon-Shan Huang, Institute of Electronics Engineering, National Tsing-Hua University, Hsin-Chu, TAIWAN.

A novel method of Cu seed layer deposition for ULSI metallization is reported. We deposited tantalum (Ta) film as a barrier layer on SiO_2. Low Pressure Chemistry Vapor Deposition (LPCVD) poly-silicon films with various thickness were then coated on Ta. A mixture solution of hydrofluoric acid and cupric sulfate saturated aqueous solution was used to form Cu nucleus on poly-silicon surface. Through sequential electrochemical reaction, the Cu seed layer was grown to replace poly-silicon layer. The rapid thermal annealing at temperature 350°C in N_2 ambient was adopted in order to improve the adhesion between Cu and Ta film. The copper film with thickness 5000A was then electroplated on the Cu seed layer. Furthermore, Auger, SEM cross section of via, and XRD were measured to understand the composition profile near the interface, step coverage on the via, and texture of the grains. The thermal stability was studied by the C-V measurement of the capacitor (Cu/Ta (500A) / SiO_2/Si) sintered at temperature from 300°C to 500°C. We found the thermal stable temperature is up to 450°C. SIMS depth profiles give the consistent results with data from the above electrical test.

11:30 AM L5.10
SUPERCONFORMAL ELECTRODEPOSITION OF COPPER IN 500 TO 75 NANOMETER FEATURES. Daniel Josell, Thomas Moffat, John Bonevich, William Huber, Gery Stafford and David Kelly, National Institute of Standards and Technology, Gaithersburg, MD; Andrei Stanishevsky, Institute for Plasma Research, Department of Physics, University of Maryland, College Park, MD.

We identify an electric yields superconformal electrodeposition of copper in trenches ranging from 500 to 90 nm in width (all 500 nm deep), a unique hysteretic response in the current-voltage (i-E) deposition characteristics of the "superfilling" electrolyte, and a 23% decrease of the resistivity of the electrodeposited copper in less than one day at room temperature. Trenches as small as 75 nm wide and 250 nm deep were also filled. Superconformal electrodeposition was obtained using an acid cupric sulfate electrolyte containing chloride (Cl), polyethylene glycol (PEG), and 3-mercapto-1-propanesulfonate

(MPSA). In contrast, deposition from additive-free electrolyte, electrolytes containing the binary combinations Cl-PEG or Cl-MPSA, or simply benzotriazole yielded a continuous void within the centers of the trenches. A large hysteresis in the i-E deposition characteristics is associated with the "superfilling" Cl-PEG-MPSA electrolyte and can be utilized to monitor and explore additive efficacy and consumption. Resistivity measurements performed on corresponding blanket films were used to quantify the relationship between the extent of additive incorporation and its influence on microstructural evolution. The films deposited from the "superfilling" Cl-PEG-MPSA electrolyte exhibit room-temperature recrystallization that results in a 23% drop in resistivity within a few hours of deposition. Reduction of void volume formed during conformal deposition from the nonfilling electrolytes through combination of geometrical leveling effect for trenches with sloping sidewalls and more rapid deposition at trench openings is also demonstrated. This is relevant because some studies have used trenches with sloping sidewalls because they were the best materials available. However, it is perhaps of greater interest as an intentional mechanism for obtaining improved filling of trenches and vias, e.g., from electrolytes that do not provide perfect fill but might be desirable for other reasons.

11:45 AM L5.11
REACTIVE DEPOSITION OF CONFORMAL METAL FILMS FROM SUPERCRITICAL CARBON DIOXIDE SOLUTION.
James J. Watkins, Jason M. Blackburn, David P. Long, University of Massachusetts, Dept. of Chemical Engineering, Amherst, MA.

The fabrication of devices of increasing complexity and decreasing dimensions is placing stringent demands on metal deposition technologies. These include conformal coverage of complex surfaces, complete filling of narrow, high aspect ratio structures, reductions in the thermal budget during fabrication, and mitigation of the negative environmental impact of current processes. Chemical fluid deposition (CFD) is a novel approach to metal deposition that can meet these challenges. CFD involves the chemical reduction of organometallic compounds in supercritical carbon dioxide to yield high purity deposits at low temperature. Since supercritical CO2 can exhibit densities that approach those of a liquid solvent while retaining the transport properties of a gas, the technique is essentially a hybrid of chemical vapor deposition (CVD) and electroless plating. One advantage of this approach is the elimination of precursor volatility constraints. In CFD precursor transport occurs in solution at fluid phase concentrations several orders of magnitude above those employed in CVD, which precludes mass transfer limitations and promotes excellent step coverage. Here, we describe the deposition of high purity films of Cu, Pt, Pd, Ni and Au and their alloys by hydrogen reduction of appropriate precursors in CO2. We also demonstrate that the conditions employed provide complete filling of high aspect ratio, sub-100 nm - wide trenches etched in Si wafers. Moreover, since aqueous plating baths are avoided and the process effluent contains only CO2, light hydrocarbons and excess H2, this approach offers considerable environmental advantages relative to current practice.

SESSION L6: COPPER ELECTROMIGRATION
Chairs: Paul S. Ho and Masanori Murakami
Wednesday Afternoon, April 18, 2001
Golden Gate B2 (Marriott)

1:30 PM *L6.1
ELECTROMIGRATION IN DUAL DAMASCENE COPPER INTERCONNECTS.
Ken-ichi Yanai, Hideya Matsuyama, Ken Shono, Ken-ichi Watanabe[a], Satoshi Otsuka[a], Shingi Sugatani[a], LSI Quality Assurance Division, [a]Technology Development Division, Fujitsu Limited, Mie, JAPAN.

Electromigration lifetime of Cu interconnects has been studied. The lifetime has been found to decrease with reduction of line width, even if the grain is bamboo structure. This result indicates the diffusion path is not grain boundary but SiN/Cu or Cu/TaN interface. Ea was about 1eV, for both stripe and LDEM pattern. Cu films were prepared using dual damascene process and conventional electro plating system. Thickness of Cu film was 0.45μm. Barrier metal was sputtered TaN of 25nm thickness. Interlevel dielectric was 0.49μm and cover layer was SiN/SiO_2 of 0.7μm thickness. Via size was 0.27μm. Two types of test structures were prepared for this study. One was a single level stripe pattern (stripe pattern) that is 1500μm long. The other was a two-level via pattern (LDEM pattern) that had the metal segment length changing from 2μm to 200μm. Electromigration test was done at the temperature from 250°C to 350°C, for activation energy (Ea) evaluation. The stress current density was from 1.4E6 to 4.0E6 A/cm^2. Metal width was changed from 0.27μm to 8.0μm to examine the line width effect. The failure sites were inspected using SEM and TEM. In stripe pattern, similar activation energy was obtained between 2μm and 0.27μm widths. Those activation energies were 0.98eV and 1.06eV. Current acceleration factor n was 2.07. In LDEM pattern, the activation energy was 1.03eV(w=0.27μm). Current acceleration factor n is 1.75. Failure analysis was conducted on some samples. For the narrow lines (w=0.27μm), voids were seen at the cathode side. In addition, some hillocks were seen at the anode side. The failure sites were found in SiN/Cu interfaces. In the LDEM pattern, voids are formed at the interface of Cu beneath via and SiN/Cu interfaces near vias at the cathode side. The medium grain size of Cu was about 1μm observed by TEM.

2:00 PM L6.2
REAL TIME OBSERVATION OF ELECTROMIGRATION BY OPTICAL AND SCANNING ELECTRON MICROSCOPY.
Finn Giuliani, Slade Cargill, Department of MS&E, Lehigh University, Bethlehem, PA.

We have used optical and scanning electron microscopes to observe electromigration in Al and Al (Cu) lines. The samples have been either pure Al (width 2.6 μm, length 300 μm with a 0.7 μm SiO_2 passivation layer) or Al-0.25 at.% Cu (width 10 μm, length 100 μm with a 1.5 μm SiO_2 passivation layer). The optical microscope was used with a CCD camera, heating stage, current source and voltmeter. For the SEM studies, the same heating stage and electronics were used and the passivation layers were removed by reactive ion etching. In some cases Cu concentration was monitored by energy dispersive x-ray analysis During electromigration the line resistance was monitored and images were recorded at regular intervals to observe void growth and other morphological changes. Relationships between void growth, Cu concentration, current density and temperature will be discussed.

2:15 PM L6.3
IN-SITU SEM INVESTIGATION OF ELECTROMIGRATION IN DAMASCENE Cu-LINES.
R. Mönig, C.A. Volkert, R. Spolenak[a], E. Arzt, Max-Planck-Institut für Metallforschung, GERMANY. [a]Bell Labs, Lucent Technologies, Murray Hill, NJ.

Cu interconnects are increasingly being used in high performance microelectronic circuits. They are believed to have better reliability than Al interconnects, but the reason for this improvement is still not clear. In this study, we have investigated the electromigration behavior of Blech-type test structures fabricated by a damascene process. In-situ measurements of void formation in Si_3N_4 passivated electroplated Cu segments were performed using back-scattered electrons in an SEM at a temperature of 370°C. The segments varied in length from 10μm to 100μm and in width from 0.3μm to 5μm. We observed the existence of a critical current below which no void formation occured. Above this critical current, voids formed after an incubation period, grew, and eventually saturated. The voids could be closed by reversing the current and new voids formed near the opposite end of the segment. We will also present results on the current density dependence of the rate of void growth as well as on the microstructure and damage morphology which were characterized using focused ion beam microscopy.

2:30 PM L6.4
EFFECT OF CURRENT CROWDING ON VACANCY DIFFUSION AND VOID FORMATION IN ELECTROMIGRATION.
Everett C.C. Yeh, C.Y. Liu, K.N. Tu, Dept of MS&E, UCLA, Los Angeles, CA; Chih Chen, Dept of MS&E, National Chiao Tung Univ, Hsinchu, TAIWAN.

In multi-level interconnects, current crowding occurs whenever the current changes direction, such as when passing through a via. We postulate that point defects such as vacancies and solute atoms have a lower probability of occurring in high-density regions than in low current-density regions. Therefore, besides the electron wind force, we propose that in current crowding, the current-density gradient can exert an additional driving force to cause excess vacancies (point defects) to migrate from high to low current-density regions. As a consequence, the voids tend to form in low current-density regions, which is contrary to intuition. The magnitude of the current gradient, which changes to a driving force when a potential in the gradient is defined, was simulated. The current gradient force is found to be high enough to affect the atomic rearrangement during electromigration. As the line width scales down, the effects of current gradient force become more and more significant. Also, the current density gradient due to current crowding exists under both dc and ac load conditions.

2:45 PM L6.5
EFFECT OF DIFFUSION BARRIER ON THE ELECTROMIGRATION RELIABILITY OF Cu/OXIDE AND Cu/LOW-k DAMASCENE INTERCONNECTS.
S.H. Kang, S. Karthikeyan, I.O. Oladeji, S. Merchant, M. Oh, A.S. Oates, Bell Laboratories, Lucent Technologies, Orlando, FL; M.E. Gross, Bell Laboratories, Lucent Technologies, Murray Hill, NJ; N. Kamat, C.S. Seet, S.K. Hong, Chartered Semiconductor, Singapore, SINGAPORE.

Dual damascene Cu interconnects require a thin diffusion barrier inserted between Cu and dielectric films. While its primary function is to prevent Cu diffusion through dielectric films under thermal and electrical stress, the architecture and the microstructural property of the barrier can significantly affect the electromigration reliability of Cu. For example, the microstructure of the Cu film is often influenced by that of the underlying barrier film. Also, the characteristic of resistance variation (dR/dt) when electromigration depletes Cu depends on the resistivity and the thickness of the barrier film that may control the current-shunting effect. In order to understand the effect of barrier configuration and properties on the electromigration reliability of Cu, we have studied various Cu/oxide and Cu/low-k damascene interconnects that incorporate several different combinations of Ta and TaN. The results show that the electromigration lifetime and the activation energy of failure widely vary as a function of barrier type and property. It appears that the difference in electromigration performance is associated with a few factors that affect the integrity and the microstructural property of the Cu interconnects including the barrier-Cu and the barrier-dielectric interfaces. The electromigration results were examined also using a thermoelectric finite element model that can solve resistance variation and Joule heating as a function of electromigration-induced voiding.

3:30 PM *L6.6

CHARACTERISTICS OF MULTI-MODEL ELECTROMIGRATION RELIABILITY IN DUAL-DAMASCENE Cu INTERCONNECTS. Ennis T. Ogawa, Ki-Don Lee, Hideki Matsuhashi, Kil-Soo Ko, Patrick R. Justison, Alex J. Bierwag, Anup N. Ramamurthi, and Paul S. Ho, Univ. of Texas, Microelectronics Research Center, Austin, TX; Volker A. Blaschke and Robert H. Havemann, International SEMATECH, Austin, TX.

An electromigration (EM) study has determined the lifetime characteristics and failure behavior of two-level, dual-damascene, Cu/oxide interconnects under a variety of temperature and current conditions. Through the use of multiply-linked interconnect ensembles, statistical evidence of two distinct ("weak-" and "strong-mode") failures in dual-damascene Cu/oxide interconnects is noted. A combination of single and repeated (N = 1, 10, 100) serial chains of nominally identical interconnects (0.5 μm wide, 300 μm long) are used in conjunction with statistical analysis based on "weakest-link" concepts. So far, more than 10,000 interconnects have been evaluated with the multi-link methodology. The scaling behavior of interconnect clustering shows that the presence of a bimodal distribution of failures has significant impact on interconnect lifetime characteristics. These differences are shown to be potentially important for evaluating interconnect lifetime in very large interconnect arrays similar those in functional ultra-large scale integration (ULSI) devices, especially for the study of early failures. Through focused ion beam analysis, two distinct failure locations are identified that impact reliability within a metallization level containing dual-damascene interconnections: (1) cathode via-bottom voiding; (2) cathode-end trench voiding above the via. Of the two modes, via-voiding is considered the weaker mode and is probably more susceptible to process variation. This variability may show pronounced differences in the relative population of failure types and would certainly be an issue for optimal process flow as device scaling continues. The weaker mode activation energy is about 1.0 eV - consistent with interfacial transport - while accurate stronger mode determination is somewhat hindered by its longer lifetime. Also, anode extrusion damage may also have impact when level-to-level reliability is considered. In addition, results on the short length or Blech effect in dual-damascene interconnections will be discussed.

4:00 PM L6.7

STRESS VOIDING IN WIDE COPPER LINES. T.M. Shaw, L. Gignac, I.C. Noyan, X-H, Lui, R.R. Rosenberg, IBM Research Division, T.J. Watson Research Center, Yorktown Heights, NY; E. Levine, S.E. Greco, P. Mclaughlin. P-C. Wang, G.A. Biery, IBM Microelectronics Division, Hopewell Junction, NY.

The results of a study of stress void formation in wide passivated copper lines will be presented. Heat treatment of the lines was carried out using a hot-stage optical microscope. This allowed direct observations of void closure and formation to be made at temperature during an annealing cycle. We find that even under conditions where overall stress in the lines is predominantly biaxial void nucleation and growth still occurs. Based on the observations we suggest that localized regions of hydrostatic stress can arise at grain boundaries in wide copper lines due to the anisotropic elastic properties of copper and localized shear processes such as grain boundary sliding.

4:15 PM L6.8

IN-SITU X-RAY MICRODIFFRACTION OBSERVATION OF STRAIN EVOLUTION IN Cu DAMASCENE LINES UNDER THE INFLUENCE OF ELECTROMIGRATION ON A ONE MICRON SCALE. R. Spolenak[a], N. Tamura[b], B.C. Valek[c], D.L. Barr[a], M.D. Morris[a], J.F. Miner[a], W.L. Brown[a], A.A. MacDowell[b], R.S. Celestre[b], H.A. Padmore[b], J.C. Bravman[c], H. Fujimoto[e], B.W. Batterman[b,d] and J.R. Patel[b,d]; [a]Bell Laboratories, Lucent Technologies, Murray Hill, NJ; [b]ALS/LBNL, Berkeley, CA; [c]Dept. Materials Science & Engineering, Stanford University, Stanford, CA; [d]SSRL/SLAC, Stanford University, Stanford, CA; [e]Intel Corp., Santa Clara, CA.

In contrast to the knowledge base that has been acquired for Al interconnects over the past 30 years, the investigations of electromigration in Cu damascene interconnects are still relatively new. One of the major issues is, as it has been for Al interconnects, whether the local microstructure of Cu has a direct influence on electromigration. In this study we utilized the newly developed facility for microdiffraction at the Advanced Light Source (ALS) at Lawrence Berkeley National Labs. The complete 3D strain tensor of any single grain along a conducting line can be determined to an accuracy of 2e-4. The spatial resolution is better than 0.8 μm. This technique was applied to Blech type Cu damascene interconnects in-situ at 250°C at current densities between 0.5 and 2 MA/cm^2. The segment lengths ranged from 10 to 100 μm and the line widths from 0.8 to 2 μm. The lines were passivated with 200 nm of SiN_x and showed a critical product (current density * segment length) of between 3000 and 5000 A/cm. Voiding was observed to occur at the Cu/SiN_x interface, not only at the cathode end but also at specific locations along the entire length of the line. The correlation between the void sites, the local microstructure and the local strain/stress state will be demonstrated.

4:30 PM L6.9

ELECTROMIGRATION CHARACTERIZATION OF DAMASCENE COPPER INTERCONNECTS: COMPARISON BETWEEN CVD COPPER AND ECD COPPER. Thierry Berger, Roberto Gonella , ST Microelectronics, Crolles, FRANCE; Lucile Arnaud, Gérard Tartavel, CEA LETI, Grenoble, FRANCE; Gérard Lormand, GEMPPM, INSA, Villeurbanne, FRANCE.

We have characterized the electromigration performance of copper damascene interconnects using moderately accelerated tests at package level. Two metallizations have been studied:
CVD copper deposited on CVD TiN
ECD copper deposited on CVD TiN using 90 nm of CVD copper as a seed-layer. All metallizations were passivated using SiO_2. Two line widths have been characterized: 0.6 and 4 microns. Scanning Electron Microscope (SEM) observations provided qualitative information on the microstructure of the tested lines. The wide and narrow lines are respectively polycrystalline and quasi-bamboo for CVD copper, quasi-bamboo and bamboo for ECD copper. For wide lines, we obtained the same activation energy (Ea) for both metallizations (0.65 eV). For narrow lines, the Ea value is 0.78eV for CVD copper whereas it is as high as 1.29eV for ECD copper. For wide lines of both metallizations, failure analysis performed with a SEM gave clear evidences that microstructural gradients have a strong impact on voids and extrusions formation (i.e. that grain boundaries are the active diffusion paths in spite of the low Ea values). For the narrow lines, diffusion at the upper interface is believed to be the main diffusion path on the basis of SEM observations. From the reliability point of view, the extrapolated lifetimes of the metallization including ECD copper are much higher (1 to 2 orders of magnitude depending on the line width) than for CVD copper. This work has been carried out in the framework of the CCMC agreement between ST Microelectronics, CEA-LETI and France Telecom CNET.

4:45 PM L6.10

INVESTIGATION ON MASS TRANSPORT IN DUAL DAMASCENE COPPER INTERCONNECT. Hideki Matsuhashi, Anup Ramamurthi, Alex Bierwag, Ki-Don Lee, Patrick Justison, Ennis T. Ogawa and Paul S. Ho, Univ. of Texas, Microelectronics Research Center, Austin, TX; Volker A. Blaschke and Robert Havemann, International SEMATECH, Austin, TX.

Electromigration (EM) testing has been performed to investigate the mass transportation phenomenon in Cu/Oxide two level dual damascene interconnects. The test modules used in this EM testing consist of N number of identical line element connected in series. The numbers of N included in this study were 1, 10 and 100. The lengths of the element are 100 and 300 um. The line widths were 0.25 and 0.5um. Average drift velocity in dual damascene copper interconnects under various testing condition are estimated from the rate of resistance increase, assuming the voiding that causes the resistance increase proportional to depletion of copper at voiding site. The analysis of resistance change showed that the rate of resistance increase per unit time is mostly proportional to number of N. This result suggested that the mass transport caused by electromigration happened throughout the test module. The failure sites were found to distribute evenly. Focused ion beam of the failure sites analysis revealed that the mass transport occurs primarily at the interface between the capped layer and Cu. The detailed results on drift velocity in the copper line and its statistical characteristics will be presented.

SESSION L7: POSTER SESSION
LOW-k DIELECTRICS
Chairs: Robert F. Cook, Mihal E. Gross, Paul S. Ho,
Robert D. Miller and Masanori Murakami
Wednesday Evening, April 18, 2001
8:00 PM
Salon 1-7 (Marriott)

L7.1
CHARACTERIZATION OF PECVD CARBON-DOPED SiO_2 LOW-k THIN FILMS PREPARED FROM TETRAMETHYL-SILANE. Licheng M. Han, N. Balasubramaniana, P.D. Foo, Institute of Microelectronics, SINGAPORE; Ji-Sheng Pan, Institute of Materials Research & Engineering, SINGAPORE; Jianou Shi, Novellus Systems, Inc., San Jose, CA.

Carbon doped SiO_2 low k thin films were prepared by radio-frequency (RF) plasma enhanced chemical vapor deposition at 400°C from polymerization of tetramethylsilane (4MS) and copolymerization of tetramethylsilane and silane (SiH_4) precursor, with nitrous oxide (N_2O) as oxidant gas. It is found that copolymer thin films from 4MS and SiH_4 precursor show much higher deposition rate than polymer thin film from 4MS, while keeping all the other parameters same. The addition of SiH_4 can significantly promote the plasma polymerization of 4MS molecules. The chemical structure and composition of these films were characterised using Fourier transform infrared (FTIR) and X-ray photoelectron spectroscopy (XPS). The two kinds of films have similar chemical composition and structure. It is also found from FTIR spectra that chemical composition and structure of the films varied progressively with 4MS flow rate. The characteristic peak Si-CH_3, which is one mechanism giving lower dielectric constant, increased with 4MS flow rate. On the other hand, film porosity, which can be characterized by Si-O cage structure peak at higher wavenumber, decreased with 4MS flow rate. Five different SiOn (n=0 - 4) moieties were identified by XPS and it is found that the dominant Si moiety is SiO_2. The physical properties of the films, such as dielectric constant, refractive index and thermal stability, have been investigated and related to the Si-CH_3 and cage structure of the films. The higher the Si-CH_3 and Si-O cage structure content, the lower the dielectric constant. The above two mechanisms compete with each other resulting in a minimum for the variation of dielectric constant with 4MS flow rate. The film as prepared shows excellent thermal stability at temperature as high as 400°C and has a dielectric constant of about 3, indicating its potential as a low-k dielectric for advanced interconnect applications.

L7.2
RESIDUAL STRESS AND THERMAL EXPANSION BEHAVIORS IN DIELECTRIC THIN FILMS PREPARED FROM POLYALKYLSILSESQUIOXANE SPIN-ON GLASS MATERIALS. Moonhor Ree, Weontae Oh, Joerg Bolze, and Byeongdu Lee, Dept of Chemistry, Center for Integrated Molecular Systems, and BK-21 Functional Polymer Thin Film Group, POSTECH, Pohang, SOUTH KOREA.

Polyalkylsilsesquioxanes and their composites in thin films were prepared by various process protocols. Their curing process was in-situ examined by FT-IR spectroscopy, thermogravimetry, and residual stress analysis. And, thermal expansion coefficients were measured in the film plane as well as in the out-of-film plane. Optical and dielectric properties were measured by prism coupling and multifrequency ellipsometry. In addition, morphogical structure in thin films were characterized by synchrotron X-ray scattering and reflection techniques. Optical and dielectric properties were measured by prism coupling and multifrequency ellipsometry. Structures and properties will be discussed in detail with considering chemical structure, curing reaction kinetics, and pore. [This study was supported in part by the Ministry of Science & Technology and the Ministry of Industry & Resources (Korean Collaborative Project for Excellence in Basic System IC Technology (98-B4-C0-00-01-00) and by the KOSEF via the Center for Integrated Molecular Systems.]

L7.3
COPPER DIFFUSION INTO LOW DIELECTRIC CONSTANT PLASMA POLYMERIZED CYCLOHEXANE THIN FILMS DEPOSITED BY PLASMA ENHANCED CHEMICAL VAPOR DEPOSITION. Cheonman Shim, Jayoung Choi, and Donggeun Jung, Department of Physics, Brain Korea 21 Physics Research Division and Institute of Basic Science, Sungkyunkwan University, Suwon, SOUTH KOREA.

Copper (Cu) diffusion into low dielectric constant plasma polymerized cyclohexane (PPCHex) thin films deposited by plasma enhanced chemical vapor deposition upon annealing was investigated. Cu diffusion was analyzed by current- voltage (I-V) measurement, Rutherford backscattering spectroscopy (RBS), and transmission electron microscopy (TEM). From I-V measurement and TEM analysis, it was revealed that PPCHex thin films were resistant to Cu diffusion up to 400°C, while there was a notable amount of Cu diffused into the PPCHex thin films after 450°C annealing. RBS was not sensitive enough to detect a small amount of Cu diffused into the PPCHex films. Improved Cu diffusion resistance of our PPCHex thin films compared to thin films of chemically synthesized polymers is thought to be due to high cross-linking among film-forming species of plasma polymers.

L7.4
VAPOR PHASE DEPOSITED TOTAL X-RAY FLUORESCENCE AS A MEANS TO STUDY COPPER DRIFT DIFFUSION IN LOW-k DIELECTRICS. Filip Lanckmans[a], S. Arnauts, K. Maex[a], IMEC, Leuven, BELGIUM, [a]also at E.E. Dept., K.U.-Leuven, BELGIUM.

Reliable copper integration requires a study of the copper diffusion behavior in low-k dielectrics in order to assess the barrier requirements. For oxide it is found that copper drift diffusion -diffusion under the influence of an electrical field- is already severe at temperatures as low as 200°C. A common method to electrically investigate copper drift diffusion in dielectrics is by using bias thermal stressing in combination with capacitance voltage techniques [1]. An analytical determination of copper diffusion in dielectrics is difficult because most methods lack a high sensitivity. An exception is vapor phase deposited total X-ray fluorescence (VPD-TXRF). VPD-TXRF is primarily used to detect contaminants with a similar sensitivity as capacitance voltage measurements ($\approx 10^{10}$at/cm^2). The technique is applied to investigate copper diffusion through a low-k dielectric. Si/thermal oxide/low-k dielectric/copper capacitor structures are prepared and stressed under different fields at various times and temperatures. After stressing, both the metal and low-k dielectric are etched and the copper present in the thermal oxide is detected by VPD-TXRF. This technique involves evaporating the thermal oxide in HF vapor resulting in a deposition of the contaminants present in the oxide on the silicon surface. Subsequently these metals are collected in an aqueous drop. The drop is put on a Si wafer, evaporated and the copper concentration is measured with TXRF. Two types of low-k dielectrics are evaluated: organic ($k<2.9$) and porous inorganic ($k\approx 2.0$) materials. The effectiveness of a barrier between the copper and the dielectric is investigated in a similar way. Starting from the measured concentration of copper in the oxide, a model is presented to estimate the copper mobility in the low-k dielectric. A good agreement of the mobility is found between this analytical method and an electrical evaluation technique (capacitance voltage). [1] F. Lanckmans, W. Vandervorst, K. Maex, AMC '99, pp.409-415

L7.5
EFFECTS OF CURING TEMPERATURE AND THICKNESS ON THE THERMAL CONDUCTIVITY OF HYDROGEN SILSESQUIOXANE THIN FILMS. Hsin Wang, High Temperature Materials Laboratory, Oak Ridge National Laboratory, Oak Ridge, TN; Huey-Chiang Liou, Dow Corning Corporation, Semiconductor Fabrication Materials, Midland, MI.

As the minimum geometry in integrated circuits (ICs) continues to shrink to the 0.18-0.25 μm range, low k dielectric materials have to be implemented to reduce the delay due to the line-to-line cross talk, and to increase the signal propagation speed. Among the available low k materials, materials are either containing pores in the films or having less polar groups in their structure to achieve lower k. While implementing porous low k materials in the IC devices, one of the reliability concerns for these materials is thermal conductivity because porous films have lower thermal conductivity than those of non-porous films do. Hydrogen silsesquioxane (HSQ), which has $k > 2.9$ due to its porous structure, has been successfully integrated in manufacturing processes. The chemical structure of HSQ is (HSiO3/2)n before cured and the Si-H bond in HSQ disassociates and its cage-like structure is rearranged into a network structure when thermally processed. It has been reported that the HSQ film properties are strongly dependent on the cure environment and temperature. Therefore, it is very important to understand the correlation between structure and thermal conductivity to ensure the reliability of HSQ in IC manufacturing. In this study, 3-omega method was used to measure the thermal conductivity of HSQ films cured at different temperatures. The impact of HSQ structure change on thermal conductivity and other properties will be reported.

L7.6
LOW-k DIELECTRICS FROM PULSED-PLASMA CVD OF ORGANOSILICON PRECURSORS. Daniel D. Burkey, Karen K. Gleason, Massachusetts Institute of Technology, Dept. of Chemical Engineering, Cambridge, MA.

Thin films produced by pulsed-plasma CVD of organosilicon precursors are promising candidates for use as low-k dielectric materials. In this paper, we consider the use of a variety of precursors and mixtures for the production of low-k organosilicon (OSG,

Si:O:C:H) thin films. Specifically, we examine the effect of duty cycle (plasma on time/total time) and precursor identity on the final film structure and thermal stability. Pulsed-plasma CVD allows some control over the film composition as compared to continuous plasma CVD. We have deposited films under both pulsed-plasma conditions and continuous plasma conditions at the same equivalent power. Films deposited under continuous plasma conditions often exhibit a higher degree of powder formation as well as structural moieties, such as methylene groups, that are not present in films deposited under PP conditions. Pulsed-plasma CVD also allows the retention of some of the original precursor structure in the final film, as evidenced by Fourier Transform Infrared Spectroscopy (FTIR) and ^{29}Si Nuclear Magnetic Resonance (NMR) analysis. Additionally, it has been observed that the methyl concentration in the film varies linearly with the duty cycle for some precursors. Growth rates for the films varied linearly with duty cycle, up until the point at which powder formation became appreciable. Index of refraction of the films varied between 1.43 and 1.47, depending upon the nature of the precursor. Another aspect of this work focuses on the thermal stability of the deposited films. Thermal stability was tested in a custom-built apparatus that heated the films to approximately 400°C under nitrogen for one hour. Thickness changes were measured via interferometry. Film retention rates, as measured by ellipsometry pre-and post-anneal, ranged between 80% and 98%, and were strongly related to precursor identity.

L7.7
NOVEL METHOD OF ESTIMATING DIELECTRIC CONSTANT FOR LOW-k MATERIALS. Takuya Fukuda, Nobuo Aoi, Azuma Matsuura, Hironori Matsunaga Association of Super-advanced Electronics Technologies, Yokohama, JAPAN.

This study is part of a five-year Japanese national project to develop multi-level interconnect processes using ultralow-k materials. Before the material design is tackled, it is important to obtain an estimate of the dielectric constant. A novel method based on a theoretical treatment of dielectrics has been devised. The dielectric constant can be broken down into three components: electronic, ionic and orientational. For LSIs, the frequency of interest is less than a few GHz. So, all three components must be considered in estimating the dielectric constant. Here, the key point is to treat materials as collections of oscillators and atoms. The electronic component is described in terms of the molecular polarizabity. Since the ionic polarization is based on atomic oscillations, it must be described in terms of the sum of the oscillation strengths, Fj, which in turn are related to the derivative of the dipole moment with respect to a normal coordinate. Therefore, Fj must be related to the absolute IR intensity of the j-band. In order to treat the condensed phase, a correction is needed for the local electric field. Here we assume that: the component terms are independent; the temperature is high enough; the frequency of interest is ~1 GHz (~0.03 cm^{-1}) and is much lower than the angular frequency of the oscillators. To obtain the relationship between the absolute IR intensity and the oscillation strength, we take the imaginary part of the dielectric constant. The integral of the imaginary part is written in terms of the absolute intensity, Aj. On the other hand, the integral of the imaginary part can be written in terms of oscillation strength. Based on the above assumptions and procedures, a theoretical expression for the components can be obtained. The electronic component is obtained by sum of atomic or bond refractions, ionic component is obtained by IR intensities and orientational component is obtained by sum of dipole moments. The data are found in many places in the literature. The sum of the three components was found to agree well with the value determined by C-V measurement. This demonstrates the validity of our estimation method. Acknowledgments: This work was performed under the management of ASET in a MITI R&D program supported by NEDO.

L7.8
THE EFFECT OF POST PLASMA TREATMENT ON THE PROPERTIES OF FLUORINATED AMORPHOUS CARBON FILMS AND THE CRYSTALLINITY OF Cu AND Ta IN Cu/Ta/A-C:F/Si MULTILAYER. Sung-Hoon Yang, Seok Woo Hong, Hanyang University, Division of MS&E, Seoul, KOREA; Chang-Hee Shin, Hanyang University, Department of Nano-Structure Semiconductor Engineering, Seoul, KOREA; Jong-Wan Park, Hanyang University, Division of MS&E, Seoul, KOREA.

The effect of post plasma treatment on the properties of fluorinated amorphous carbon (a-C:F) films and the crystallinity of Cu and Ta in Cu/Ta/a-C:F/Si multilayer. In this study, a-C:F films were prepared by an electron cyclotron resonance chemical vapor deposition (ECRCVD) system using gas mixture of C_2F_6 and CH_4 on the pre-deposited 500Å thick hydrogenated amorphous carbon (a-C:H) film. The post-plasma treatment of the a-C:F films was carried out using H_2 plasma with various plasma treatment powers (150~700 W) and times (5~300 s) after deposition without vacuum breaking. During the plasma treatment, 20 sccm H_2 gas was introduced into a plasma chamber. Diffusion barrier of tantalum with a thickness 200Å and 300Å copper seed layer were sputtered on the a-C:H film. Copper was electrodeposited on copper seed layer. X-ray photoelectron spectroscopy (XPS) was taken to investigate changes in surface chemical composition. The leakage current density and the dielectric constant of the a-C:F films were investigated I-V and C-V characteristics using an MIS structure. The resistivity of Ta and Cu films were obtained using a four-point probe measurement. The crystallographic orientations of Ta and Cu films were measured using an X-ray diffractometer (XRD). The surface energy of a-C:F films was evaluated by contact angle measurements using water and diiodomethane. From this study, it was found that the plasma treatment of a-C:F films produce more reactive surfaces and affect the fluorine concentration of the surface, the structure of chemical bonding and electric properties.

L7.9
EFFECT OF STRESS STATE ON THE ADHESION OF A POROUS LOW-k DIELECTRIC. Michael W. Lane, Kenneth P. Rodbell and Kenneth Wu, IBM T.J. Watson Research Center, Yorktown Heights, NY; Willi Volksen and Robert D. Miller, IBM Almaden Research Center, San Jose, CA.

The drive for faster interconnects dictates that dielectric materials which separate the active metal lines must have a dielectric constant, k, approaching that of air (k ~ 1.0). To this end, dielectrics which contain embedded voids have been proposed. The net effect of these voids is to average the dielectric constant of air and the matrix material. An outstanding issue when considering these porous dielectrics is how they will behave under different stress conditions. Stress states arise in interconnect device structures due to mismatches in the coefficient of thermal expansion and elastic properties of the materials. These factors, along with the complex geometries employed in interconnects and the processing steps required to fabricate the devices (such as chemical mechanical polishing), may lead to complex stress states that vary from point to point in the device depending on the local geometry. Therefore, no single adhesion value will characterize the material as it is likely to experience stress states ranging from pure shear to pure tension. Accordingly, a fracture mechanics based test methodology has been implemented to measure the adhesion of porous MSSQ films from pure shear to pure normal loading. Changes in the delamination path were observed as the stress state was varied from pure tension to pure shear. Furthermore, the delamination path was found not only to depend on the type of stress (normal or shear) but also the sign of the shear stress (+ or -). Fracture paths were characterized by AFM and EDX.

L7.10
INVESTIGATION OF N_2 PLASMA EFFECTS ON THE DENSITY PROFILE OF HYDROGEN SILSESQUIOXANE THIN FILMS. H.J. Lee, E.K. Lin, W.L. Wu, B.M. Fanconi, National Institute of Standards and Technology, Polymers Division, Gaithersburg, MD; J.K. Lan, Y.L. Cheng, Y.L. Wang, Taiwan Semiconductor Manufacturing Co., Hsin-Chu, TAIWAN; H.C. Liou, Semiconductor Fabrication Materials KCI, Dow Corning, Midland, MI; M.S. Feng, C.G. Chao, National Chiao-Tung University, Hsin-Chu, TAIWAN.

Materials with low dielectric constant (low-k) have attracted much interest because they can reduce RC delay, which becomes a limiting factor in improving device performance. One of the low-k candidates is the commercially available siloxane-based hydrogen silsesquioxane (HSQ) resin because of its excellent planarization and gap fill capabilities. However, the integration of both copper lines and low-k dielectrics still has several technical problems such as reducing copper diffusion, decreasing the leakage current, suppressing water uptake, and avoiding damage during patterning in IC applications. Many of these problems can be addressed through processing modifications to increase the surface density of an HSQ film. Although this addresses some problems, a densified surface layer also increases the effective dielectric constant of film. To balance these two effects, the semiconductor industry would like to precisely control the thickness of the densified dielectric layer. To reach this goal, it is essential to develop an accurate analytic technique to measure the thickness of the densified dielectric layer. In this work, we demonstrate the use of specular X-ray reflectivity (SXR) as a powerful technique to measure the depth profile of HSQ films treated with N_2 plasma with varying power and exposure time. The influence of the N_2 plasma treatments on the chemical bonding structures is also investigated using Fourier transform infrared (FTIR) spectroscopy. The SXR data indicated that the density profile of an untreated HSQ film is not uniform. Plasma treatment results in a densified layer at the film/air interface and an increase in surface roughness. The thickness of the densified layer increased with both plasma power and plasma exposure time. The FTIR data show that the plasma converts the HSQ structure into a SiO_2-like structure and are consistent with the densification observed in the SXR measurements.

L7.11
CORRELATIONS BETWEEN STRUCTURAL CHARACTERISTICS AND PROCESS CONDITIONS OF HSQ BASED POROUS LOW-k THIN FILMS. Hae-Jeong Lee, Eric K. Lin, Howard Wang, Wen-li Wu, National Institute of Standards and Technology, Polymers Division, Gaithersburg, MD; Wei Chen, Thomas A. Deis, Semiconductor Fabrication Materials KCI, Dow Corning, Midland, MI.

One of the current challenges in semiconductor processing is to improve device performance while keeping the cost low. The main limiting factor in improving device performance is the signal delay through metal interconnects from the resistance, R, in the metal lines and the capacitance, C, between adjacent lines. Lowering the resistance of the metal line and the dielectric constant of the interlayer dielectric (ILD) material could reduce this RC delay. The National Technology Roadmap for Semiconductors indicates a need for materials with dielectric constants of 1.5 - 2.0 for dimensions below 0.13 um by the year 2003. Dielectric constants are effectively lowered to values below 2.2 by incorporating voids (dielectric constant of 1) in the material. Several types of porous materials are being developed to replace the current ILD, silicon dioxide. Among them, hydrogen silsesquioxane (HSQ) based porous materials have been evaluated extensively because of their potential compatibility with conventional Si technology and the high strength of the backbone siloxane network. The pore structure in porous thin films can seriously affect the thermo-mechanical and electrical properties of the thin film. Structural information such as the film porosity, pore size, wall density, and pore connectivity of thin films as a function of process conditions is important to improve and optimize the properties of low-k thin films. In this work, we provide results on the correlations between processing conditions of HSQ based porous low-k thin films and the resulting structural properties. Samples with different Si-H contents ranging 30% to 52% and different dielectric constant ranging from 1.5 to 2.2 were prepared. We performed the measurements of the structural properties such as porosity, average pore size, and wall density, average film density, and pore connectivity using small angle neutron scattering (SANS), high-resolution specular X-ray reflectivity (SXR), and ion scattering techniques.

L7.12
COMPOSITIONAL AND MECHANICAL STUDY ON THE LOW DIELECTRIC CONSTANT SiOC FILM. Yoon-Hae Kim, Moo Sung Hwang, Hyeong Joon Kim, Seoul National University, School of MS&E, KOREA; Young Lee, Jusung Engineering Ltd, KOREA.

As ultralarge scale integrated circuits (ULSIs) are reduced in size to deeper sub-micron dimension, there has been a strong demand for low dielectric constant inter-metal dielectric materials instead of SiO_2 that is conventionally used to improve the performance of devices, such as signal propagation delay, cross talk, and power consumption. Recently, SiOC, which is hybrid between organic and inorganic materials, is very promising inter-metal dielectric, since it has higher thermal and mechanical stabilities than organic materials as well as low dielectric constant. Despite many researches, the reasons for increasing dielectric constant upon carbon incorporation remain under debate. Generally, it is accepted that the carbon incorporation ($-CH_3$) in the Si-O network leads to the porous structure and the decrease of film density results in the decrease of dielectric constant. In this investigation we focused on the fundamental relationships among the film density, composition and dielectric constant. As carbon contents incorporated in film increased, the film density and dielectric constant decreased. Also, there was the shift of O-Si-O stretching mode peak in the infrared spectra of the SiOC film and we could see the similar phenomena in the fluorinated silicate glass (FSG) film. Spectroscopic ellipsometry, electronic balance, and elastic recoil detection (ERD) were used for calculation of film density. Compositions of the films were investigated by Fourier transform infrared (FTIR), x-ray photoelectron spectroscopy (XPS), and ERD. The microstructure of the SiOC film was examined by transmission electron microscopy (TEM) and the dielectric constant was calculated from capacitance-voltage (C-V) measurement.

L7.13
GAP FILLING AND DIELECTRIC STABILITY OF FLUORINATED SILICON DIOXIDE (FSG) IN ALUMINUM-FSG INTERCONNECTS. Young Way Teh, Terence K.S. Wong, Nanyang Technological University, School of Electrical and Electronic Engineering, SINGAPORE; John L. Sudijono, Alex See, Huang Liu, Technology Development Department, Chartered Semiconductor Manufacturing Ltd. Woodlands, SINGAPORE.

For each IC generation, the continuing reduction of the metal pitch requires taller aluminum conductors so as to mantain the same resistance. This makes dielectric gap filling very challenging as the aspect ratio becomes greater. FSG has been widely adopted as the first generation low-k dielectric. However, the extendibility of FSG to future generations depends not only on a reduction of the FSG k value but also its ability to fill gaps with increasingly high aspect ratios. In this paper, the gap filling capability of FSG deposited by HDP-CVD is studied by varying the ratio of source gas flow rates, RF bias power and the deposition pressure. Aluminum lines with different heights and pitch spacing are used to study the effect of aspect ratio for different plasma conditions. The quality of the gap fill is characterised by cross section SEM and analyzed by step coverage analysis. The HDP-CVD gap fill capability is closely related to the deposition to sputter (D/S) ratio. An optimum D/S ratio allows good bottom-up gap fill. For FSG deposition, the sputter component consists of sputtering by argon as well as chemical etching by fluorine in the plasma. Thus, the fluorine containing gas flow can affect the D/S ratio and hence the gap fill characteristics. The reduction of pressure is known to improve the gap fill capability but its effect on FSG film stability remains unknown. FTIR and SIMS are used to evaluate the stability of FSG films deposited at low pressures.

L7.14
ELECTRICAL PROPERTIES OF NANOPOROUS PMSSQ. H.-W. Rhee, B.-S. Kim, D.J. Lee, S.K. Min, Sogang Univ., Dept. of Chem. Eng., Seoul, KOREA; K. Char, Seoul National Univ., School of Chem. Eng., Seoul, KOREA; J.-K. Lee, D.Y. Yoon, Seoul National Univ., Dept. of Chem., Seoul, KOREA; M.Y. Jin, KRICT, Daejoen, KOREA.

Nanoporous inorganic materials have been extensively studied to develop the ultra low dielectric materials ($k < 2.0$) for the next generation logic chips. Poly(methylsilsesquioxane) (PMSSQ) has been one of the most promising matrices. Organic/inorganic nanohybrids were prepared by using star-shaped poly(caprolactone) as a nano-template. Nanoporous PMSSQ films were obtained by thermally decomposing the organic polymer (porogen) in the nanohybrids. Nanohybrids were prepared by spinning the solution of MSSQ and porogen in methyl isobutyl ketone (MIBK) or propylene glycol monomethyl ether methyl acetate. The compatibility between the porogen and inorganic materials is a key controlling factor to obtain the uniform size and distribution of pores in the nanoporous materials. Thus, MSSQ copolymers were synthesized and their interaction with the porogen was controlled. Dielectric properties and refractive indices (n) of the pure and nanoporous PMSSQ were measured by LCR meter and ellipsometer, respectively. Dielectric constants of nanoporous PMSSQ linearly decreased with increasing amount of PCL added and the calculated porosity also showed a good correlation with the amount of PCL added. The effect of MSSQ copolymer composition and surface treatment effect on the electrical properties will be presented.

L7.15
A NOVEL RECESSED GATE-LINE EMPLOYING AN AIR-GAP LINE CROSSOVER WITH DECREASED SIGNAL DELAY IN AMLCD PANEL. Jin-Woo Park, Woo-Jin Nam, Cheon-Hong Kim, Min-Cheol Lee and Min-Koo Han, Seoul National University, School of Electrical Engineering, Seoul, KOREA.

The large size AMLCD requires high speed driving circuits because the signal delay of the data line due to RC delay is increased and the quality of display image is degraded. In order to decrease the signal delay of the data line, a considerable effort has been to reduce signal delay in AMLCD panel as well as various FPDs (Flat Panel Display). Most of previous works are concentrated to reduce a resistance rather than capacitance. The purpose of our work is to report a new low-dielectric air-gap structure which decreases the capacitance between gate and data line considerably. Our new structure planarizes the air-bridge panel in order to sustain the mechanical durability of the structure without sacrificing the capacitance. The planarization is rather important in AMLCD because rubbing or spacer processes in AMLCD fabrication may induce the mechanical stress. The proposed structure was successfully fabricated. The key process steps are as follows. After trenching oxide on transparent quartz wafer, gate-metal was evaporated without photoresist stripping. The metal on photoresist was eliminated by the lift-off process in order to forming gate-lines on the bottom of the oxide trench. A new photoresist layer formed by the backside-exposure technique is the sacrificial layer for forming the air-gap. It enables align the sacrificial photoresist on the recessed gate-line exactly without any more photolithography mask. This sacrificial layer photoresist was treated by thermal curing for performing the high temperature plasma process such as a metal sputtering on the organic photoresist. The inter-layer oxide and the data-line metal was deposed on sacrificial photoresist and patterned. Finally, the sacrificial and data-line patterning photoresists were eliminated by oxygen plasma simultaneously. After fabricating, It was observed that recessed air-bridge was successfully formed in the oxide trench. The planarized panel surface prevents the air-bridge from collapsing due to the mechanical stress. Our experimental signal delay data shows that the proposed structure reduces the delay time by about 9 times compared with the conventional structured panel. The

proposed hollow air-gap structure in the oxide trench reduces the capacitance corresponding to the low-dielectric material. The proposed recessed structure that is almost planarized is immune to the mechanical stress.

L7.16
CORRELATION BETWEEN SURFACE MODIFICATION OF HSQ FILMS AND PHASE TRANSFORMATION OF Cu/W-N BILAYERS DEPOSITED ON THE NH_3 PLASMA TREATED HSQ FILMS.
Dong Joon Kim, Hyun Sang Sim, Jong-Wan Park, Hanyang University, Division of MS&E, Seoul, KOREA; Yong Tae Kim, Seong-Il Kim, Chun Keun Kim, Korea Institute of Science and Technology, Semiconductor Materials Laboratory, Seoul, KOREA.

After NH_3 plasma treatment of HSQ films, W-N and Cu thin films are deposited on the NH_3 plasma treated HSQ films. As a result, surface roughness of W-N film becomes smoother and adhesion of the W-N to the HSQ is also stronger than that of the W-N to the non-plasma treated HSQ film. From contact angle measurement, surface energy of the HSQ film increases 2 times from $\sim$ 23 to $\sim$ 61 mJ/m^2 after the NH_3 plasma treatment. Therefore, it is concluded that surface modification of HSQ film by the NH_3 plasma treatment causes the wet-ability on the surface of HSQ film, resulting in the improvement of surface morphology and adhesion of W-N thin film. Also, a texture of the Cu is preferred oriented to (111) when the Cu film is deposited on the W-N/the NH_3 plasma treated HSQ thin film. After annealing the Cu/W-N/HSQ interconnect structure at 400 $\sim$ 700°C, we have found that the Cu/W-N/non-plasma treated HSQ structure is agglomerated at 600°C and the phase transformation of W-N film is significantly occurred at 700°C. However, in the case of NH_3 plasma treated HSQ, the Cu film is not agglomerated at 600°C and the W-N phase is also remained at 700°C. These results suggest that the surface of HSQ thin film modified by the NH_3 plasma treatment forms a passive Si-N layer between W-N and HSQ. This passive Si-N layer act as a diffusion barrier against inter-diffusions of N and H atoms from the W-N and HSQ films, respectively.

L7.17
LOW DIELECTRIC CONSTANT FUNCTIONALIZED SILICA XEROGELS.
Rosa A. Orozco-Teran, Hanjiang Dong, Jodi A. Roepsch, Dennis W. Mueller, and Richard F. Reidy, Department of Materials Science, University of North Texas, Denton, TX.

Silica thin film xerogels have excellent potential as interlayer dielectric materials needed for the next generation of electronic devices. Silica xerogel films exhibit extremely low dielectric constants; however, thermal and chemical stabilities of these dielectric constants during semiconductor processing are of some concern. Effective low κ materials have hydrophobic surface groups that exhibit low polarizability. Adsorption of water can increase polarizability and removed low polarizable functional groups. Many silica-based xerogel systems require "capping" steps to create hydrophobic surfaces. To avoid these additional process steps in device fabrication, efforts have been made to identify "single step" xerogel precursors. The advantage of these systems is the relatively straightforward and inexpensive integration into current fabrication methods. Studies have been conducted on two systems: triethoxyfluorosilane (TEFS) and methyltrimethoxysilane (MTMS). TEFS is a potential precursor for low κ dielectric applications because of low polarizability of the fluorine surface atom and small particle size of polymerized FTES. However, TEFS gels very rapidly and traps unreacted hydrophillic hydroxyl groups thus presenting difficulties due to water adsorption and in spin coating processing. Another hydrophobic precursor, MTMS, gels at more controlled rates; consequently, offers some control of gel nanostructure. However, the particle size of MTMS can increase rapidly during the aging and drying periods; therefore, care must be taken to prevent particle sizes from approaching IC feature sizes. Hybrid systems of TEFS and MTMS provide a balance among gel time, hydrophobicity, and dielectric properties. In addition, samples have been reacted with surface modification agents to establish if further reductions in dielectric constant can be attained. To determine which systems are best suited for IC dielectric applications, gas adsorption, FTIR, SEM, ellipsometry, and impedance measurements have been employed to describe the structures, chemical and thermal stabilities, and dielectric constants of thin film hydrid xerogels.

L7.18
NANOINDENTATION OBSERVATIONS OF POROUS MATERIALS.
Eva E. Simonyi, K.P. Rodbell, J.C. Hedrick, IBM Research, Yorktown Heights, NY; A. Jain, Renssalaer Polytech Institute, NY.

Manufacturing of low dielectric constant thin insulating layers present a special challenge for the microelectronics industry. One of many approaches is to use porous materials. This paper discusses hardness and Young's modulus changes for porous materials covering a range from zero to 50% porosity. As an example metalsesquioxane (dendriglass) and tetraethylorthosilicate (TEOS) will be discussed. Correlations with pore size distributions will also be shown.

L7.19
EVALUATION AND COMPARISON OF TRIBOLOGICAL AND MECHANICAL PROPERTIES OF LOW-k DIELECTRIC MATERIALS.
A.K. Sikder, I.M. Irfan, Ashok Kumar, S. Ostapenko and J. Mark Anthony, Center for Microelectronics Research, College of Engineering, University of South Florida, Tampa, FL.

As the minimum geometry of microelectronic devices continues to shrink, new materials with low dielectric constant are demanded by the semiconductor industry. These are mainly used as an interlayer dielectric to improve the performance of ICs by reducing parasitic delays and power requirements. Mechanical characterization of low-K materials has shown that lower K typically also means lower elastic modulus and hardness. Also the major challenges involves in chemical mechanical polishing (CMP) of these films due to the reduced modulus and cohesive strength of many low-K materials. Parallel with the improvement of the lower dielectric constant it is utmost necessary to evaluate the mechanical and tribological properties in order to successful implementation of this materials. We have made a comparative study of mechanical and tribological properties of low-K dielectric materials (SiLK, Porous silica, Doped silicon oxides FLARE, and others). Mechanical properties were evaluated using MTS Nanoindenter$^{(R)}$ XP with a Berkovich indenter. Universal Micro-Tribometer was used to study the tribological properties of these films. Surface morphology and roughness of the films were also characterized by atomic force microscopy. Mechanical and tribological characterizations along with surface characterization are equally important along with the electrical performance testing to implement low-K materials in the device.

L7.20
A METHOD OF IMPROVING DIELECTRIC CONSTANT AND ADHESION STRENGTH OF METHYL SILSESQUIOXANE BY USING A NH_3 PLASMA TREATMENT.
Hyun Sang Sim, Yong Tae Kim, Semiconductor Materials Laboratory, Korea Institute of Science and Technology, Cheongryang, Seoul, KOREA; Dong Joon Kim, Hyeongtag Jeon, Division of Materials Science and Engineering, Hanyang Univ, Seongdong-ku, Seoul, KOREA; Sang-Hyon Chu, Kookheon Char, School of Chemical Engineering, Seoul National Univ, Seoul, KOREA.

Low dielectric and porous thin films, such as hydrogen silsesquioxane (HSQ) and methyl silsesquioxane (MSQ) thin films, have been intensively studied as an interlevel dielectric (ILD) material for multi-level interconnection since RC time delay can be reduced by low-k. In this work, we have synthesized a MSQ material that has relatively a low-k (k=2.7-3.0), an intrinsic hydrophobicity, good mechanical hardness and good thermal stability (up to 500°C). However, it is well known that generally the MSQ has poor adhesion to Cu metal and diffusion barrier thin films. Therefore, we have tried to modify the surface of MSQ films by NH_3 plasma treatment to improve the adhesion. As a result, the effects of NH_3 plasma treatment on electrical and physical properties of methyl silsesquioxane (MSQ) have been investigated. After the NH_3 plasma treatment, the dielectric constant of the MSQ was decreased by about 20%, and the adhesion of MSQ to W-N diffusion barrier thin film was also improved. However, leakage current density of the plasma treated MSQ films was increased depending on plasma treatment conditions and as increasing the plasma treatment temperature from 150 to 350°C, the leakage current density of the MSQ increased as high as a order of magnitude. In this work, we will discuss the effect of nitrogen atom bombardment to the MSQ films on reducing the dielectric constant and wet-ability on the surface of the MSQ film.

L7.21
EVALUATION OF SiN AND SiC AS COPPER DIFFUSION BARRIERS.
Xiaomei Bu, Licheng M. Han, Joseph Xie, Wei Qin, Zhiqiang Mo, Jielin Xie, Shuri Wang, Bo Yu, P.D. Foo, Institute of Microelectronics, SINGAPORE.

The dielectric barrier is needed to prevent copper diffusion in copper dual-damascene technology. Silicon nitride (SiN) is currently employed for this purpose. Amorphous silicon carbide (SiC:H), a new promising thin film, is being evaluated as a potential barrier to replace SiN due to its excellent barrier properties, high thermal stability and lower dielectric constant. In this study, both SiN and SiC thin films have been evaluated as copper diffusion barriers as related to barrier deposition and following high temperature annealing process. The amorphous SiC:H thin film has been prepared by plasma deposition of methylsilane precursor. RI, dielectric constant and FTIR of SiC:H films have been measured. Significant copper signals were detected by TXRF measurement for the surfaces of as-deposited SiN and SiC:H thin films on Cu substrates. It was confirmed that the copper contamination on the surface of as-deposited dielectric solely comes

from the copper substrate. The copper diffusion has been attributed to plasma sputtering and high temperature diffusion during dielectric barrier deposition. It was also observed that copper concentration on dielectric is highly dependent on the copper substrate with post CMP copper substrate showing much higher copper concentration than PVD copper substrate. These results highlight the importance of dielectric barrier deposition and surface condition of copper substrate for the copper contamination of as-deposited dielectric. High temperature (from 400 to 800°C) annealing followed by SIMS measurement was conducted to evaluate SiN and SiC:H thin films as a copper diffusion barrier. SiC:H is a better diffusion barrier than SiN in the process temperature (about 400°C) even though it completely failed with temperature above 500°C. The barrier failure and copper diffusion mechanisms have been discussed.

SESSION L8: POSTER SESSION
DIFFUSION BARRIER & METAL THIN FILMS

Chairs: Robert F. Cook, Mihal E. Gross, Paul S. Ho, Robert D. Miller and Masanori Murakami
Wednesday Evening, April 18, 2001
8:00 PM
Salon 1-7 (Marriott)

L8.1
COMPARATIVE ANALYSIS OF THE NUCLEATION AND GROWTH OF Cu ON DIFFERENT LOW-k POLYMERS.
V. Zaporojtchenko, J. Erichsen, T. Strunskus, K. Behnke, F. Faupel, Chair for Multicomponent Materials, Faculty of Engineering, University of Kiel, Kiel, GERMANY; M. Baklanov, K. Maex, IMEC, Leuven, BELGIUM.

In view of the great need for further miniaturization and reduction of propagation delay in future device generations aluminum will increasingly be replaced by the lower resistivity copper, and polymers are seen as potential low-permittivity (low-k) dielectrics even for on-chip interconnects. Therefore, the investigation of the growth of Cu on low-k polymers is of considerable technological interest. Copper was deposited by thermal evaporation onto fully cured spin-coated polymer films of PMDA-ODA polyimide (PI), Teflon-AF 1601 (TAF) and SiLK resin dielectric. The evolving interfaces were characterized using transmission electron microscopy (TEM), x-ray photoelectron spectroscopy (XPS) and atomic force microscopy (AFM). Due to their low reactivity copper atoms can diffuse into polymers at elevated temperatures, but due to their high cohesive energy in combination with the weak metal-polymer interaction they also show a very strong tendency to get immobilized by aggregation. The nucleation and growth of copper clusters on the polymers at different temperatures was investigated. Condensation coefficients as well as the adsorption energy E_a and the activation energy for surface diffusion E_d of copper on the different polymers were also determined. Complete condensation ($C = 1$) of Cu occurs on PI up to 523 K and on SiLK even up to 623 K. In contrast to these polymers extremely incomplete condensation with a C as low as 0.1 was observed for Cu deposition onto TAF already at RT. The cluster density of Cu on SiLK was by a factor of 10 - 100 higher compared to PI and several orders of magnitude higher compared to TAF. An estimate of the metal-polymer interaction from these results indicates that the interaction in the case of Cu - SiLK is relatively strong and diffusion of copper into this polymer is much less pronounced compared to the other polymers under investigation.

L8.2
LOW TEMPERATURE DIRECT-WRITE CHEMICAL DEPOSITION OF COPPER USING INKJET TECHNOLOGY.
Gregor Rozenberg, Joachim Steinke, Dept of Chemistry, Imperial College, London, UNITED KINGDOM; Stuart Speakman, Patterning Technologies Ltd, The Maltings, Royston, Herts., UNITED KINGDOM.

Currently the majority of integrated circuits (ICs) contain tungsten (W), aluminium (Al) and/or aluminium-copper alloys as the conductors in transistor devices. However the push towards smaller features and higher integration demand better materials. For this copper (Cu) appears to be the strongest contender. The main reasons are that copper exhibits excellent electrical conduction with a bulk resistivity of 1.68 micro omega per cm. This value is close to the resistivity of bulk silver (Ag) 1.59, the lowest value of any metal. By comparison currently used aluminium has a bulk resistivity of 2.65 and tungsten 5.4 micro omega per cm. In this paper we present a method and apparatus for the deposition of copper using drop-on-demand ink-jet printing of novel organo-metallic copper precursors. The ink-jet apparatus is a means of delivering appropriate chemical precursors as 'inks' in a controlled and placement accurate fashion that react to give the desired deposited material(s). The 'ink' is jetted using a piezo activated attenuator and the generated droplets then hit either a pre-activated surface, or the droplets themselves are activated at the surface. The subsequent chemical reaction yields the desired chemical composition of the deposited feature. The 'inks' that are either neat liquids of a precursor material or volatile solutions containing the precursor enable low temperature deposition and give off volatile byproducts during the conversion reaction. These are removed using vacuum or a constant flow of inert carrier gas. Feature sizes, material morphology, rheology, electrical performance, environmental and mechanical stability is controlled by the choice of material, inkjet delivery parameters and the chemistry involved in the conversion processes. Structural, chemical and electronic analyses of the printed deposits are also presented. Our findings represent an important step towards the manufacture of electronic devices by entirely non-lithographic means.

L8.3
ELECTROLESS COPPER DEPOSITION OF SEEDING LAYER FOR ULSI COPPER INTERCONNECT METALLIZATION.
Wang Ling Goh, Kee Tchuan Tan, Man Siu Tse, Kai Yu Liu, Nanyang Technological University, School of Electrical and Electronic Engineering, Microelectronics Center, Micro-Fabrication Laboratory, SINGAPORE.

PVD technologies are widely used for Cu seeding layer deposition but the step coverage on deep via/trench is questionable for sub-0.15um technology. CVD Cu deposition technology is thus in active research to replace the PVD methods for Cu seeding layer formation. We propose the Electroless (EL) copper technology as an alternative contending technology to CVD Cu for seeding layer formation. The resistivity, morphology, texture, grain size, roughness, microstructure and adhesion of the electroless Cu seeding layer was studied. Excellent step coverage is achieved with the EL-Cu technology. EL-Cu with very high (111) texture can be obtained using Cu flash layer. A comparative study was also performed to study the properties of Cu seeding layers deposited by the CVD and EL methods. CVD and EL Cu Seeding layers are quite comparable in term of physical properties like grain size (0.15-0.2um), roughness (<15nm) and resistivity (>2 uohm-cm). Unlike the CVD-Cu seeding layer which is known to have very poor adhesion to most substrate, we demonstrate that EL Cu film has good adhesion on barrier. Electroless copper deposition method has great potential as a copper seeding scheme for ULSI copper metallization due to its very low tool cost (much lower than CVD Cu) and excellent step coverage (comparable to CVD Cu process). Being a wet process, EL-Cu technology offers the advantage of easy integration with existing Cu plating process and allows both EL-Cu seeding and EP (electroplating)-Cu filling processes to be integrated on the same platform. Moreover, EL Cu is deposited at a much lower temperature of around 70 deg, compared to the typical CVD process temperature of 200-300 deg. The low temperature processing in EL-Cu technology ensures compatibility with most low-K dielectric.

L8.4
H-ASSISTED PLASMA CVD USING $Cu(HFAC)_2$ AND $Cu(EDMDD)_2$.
Masaharu Shiratani, Hong Jie Jin, Kousuke Takenaka, Kazunori Koga, Toshio Kinoshita, Yukio Watanabe, Kyushu University, Fukuoka, JAPAN.

Complete filling of high-purity copper in subquarter-micron trench structures is a key requirement in formation of metal interconnects carrying signals in ULSI. For this interconnect application, we have developed an H-assisted plasma CVD reactor (HAPCVD) which is equipped with an H atom source. This reactor can realize control of quality and conformality in Cu film deposition, since H irradiation is effective in purifying the Cu films, increasing the grain size, and reducing the surface roughness, while the decrease in dissociation degree of Cu source materials leads to realize conformal deposition in fine trenches. When using $Cu(hfac)_2$ as the source materials, Cu(hfac) is identified as the radical mainly contributing to the deposition. Based on a series of our results, we propose a model in which Cu(hfac) and H react on surfaces to deposit Cu films. We also have demonstrated conformal deposition of smooth high-purity Cu films (about 100%) of 30 nm in thickness and 1.9 $\mu\Omega$cm in resistivity in trenches using the HAPCVD.[1-3] Moreover, we use a new Cu source of $Cu(EDMDD)_2$, which does not contain undesirable element F for obtaining good adhesion to barrier metals such as TaN and WN. Films deposited using $Cu(EDMDD)_2$ shows better adhesion strength than those obtained using $Cu(hfac)_2$.

[1]H.J. Jin, *et al.*, J. Vac. Sci. & Tech. **A17** (1999) 726.
[2]H.J. Jin, *et al.*, Jpn. J. Appl. Phys. **38** (1999) 4492.
[3]M. Shiratani, *et al.*, Mater. Res. Soc. Proc. **612** (2000) D9.2.

L8.5
EFFECTS OF PLATING CURRENT PROFILE AND BARRIER LAYER ON SELF-ANNEALING BEHAVIOR OF ECP Cu FILM.
Zhang Yi, National University of Singapore, Singapore-MIT Alliance, SINGAPORE; Koh Leong Tee, Li Chaoyong, Institute of Microelectronics, Deep Submicron Integrated Circuit, SINGAPORE;

Liu Hengda, Rudolph Technologies, Inc., Flanders, NJ; Joseph Xie Zhifeng, Institute of Microelectronics, Deep Submicron Integrated Circuit, SINGAPORE.

The properties of electroplated copper films have been found to alter along the time after the plating. This phenomenon is called self-annealing, which is a relaxation process associated with microstructure changes and tensile stress release. Effects of DC and pulse current with the use of different barriers on the self-annealing behavior of the ECP Cu film have been investigated. Wafers with same Cu film thickness were deposited using different DC process with plating current density of 7, 18, 35, and $65mA/cm^2$, or using pulse current. They were also grown on different barriers (Ta, Ta(N), and Ta/Ta(N)/Ta) for a comparison. After the deposition, the properties of these Cu films were investigated with FSM, four-point probe, AFM, MetalPULSE and SEM for analyzing their stress, sheet resistance (R_S), surface topography, thickness, roughness and grain size. The results indicate that R_S had a most distinct change for all the wafers during the self-annealing, which decreased up to 25%, depending strongly on the employed plating current profile. When using DC current, applying higher current density lead to that R_S began to decrease earlier in a faster rate and to a larger percentage. When using pulse current, however, the measured R_S decreased much slower and only reduced its value about 3% in one week after the deposition. The effects of different barriers on the self-annealing, on the other hand, show that R_S decrease exhibited a similar trend as in the case of applying higher DC current density. These changes, based on SEM analysis, can be attributed to the increase of the Cu grain sizes.

L8.6
HIGHLY (111) ORIENTED Al THIN FILMS BY ION-PLATING METHOD USING DISCHARGE PLASMA. Shin Masui, Kimio Kinoshita, Susumu Sakuragi, Toshio Kudo, Sumitomo Heavy Industries Ltd, R&D Center, Hiratsuka, Kanagawa, JAPAN; Shinji Takayama, Hosei Univ, Dept of System and Control Engineering, Koganei, Tokyo, JAPAN.

Ion plating (IP) method using arc discharge plasma was applied to deposition of Al thin films for interconnects. The high energy electron beam in this discharge plasma lets Al metals melt, vaporize and highly ionize. The resultant Al ions are accelerated toward a glass substrate due to the plasma potential and Al thin films are deposited with energetically impinging of Al ions on the substrate. In this method highly oriented Al(111) films were obtained. The characteristics of IP-Al films are shown comparing with those obtained by magnetron sputtering (MS). According to X-ray diffraction (XRD), the (111) peak intensity of IP-Al films is 10 times higher than that of MS-Al films at least, and except for the (111) peak, no other peaks were observed in the XRD pattern of IP-Al films. Ar ion bombardment as a pre-treatment was found to be effective for narrowing the half-width (down to 2.4 deg.) of rocking curve at the (111) peak. Whereas, the MS-Al films have several weak XRD peaks and broad rocking curves. Furthermore it was found that the surface roughness of IP-Al films (Ra=1.3nm) is smaller than that of MS-Al films (Ra=2.9nm) under AFM observation and the IP-Al films have much more resistance to abnormal grain growth with the post-treatment of the furnace annealing up to 623K. In order to prevent the electromigration and abnormal grain growth in Al interconnects, the advantages of the (111) preferred orientation have been reported by many authors. IP-Al films have vast potential for this purpose but the mechanism of the growing film has not cleared yet. We will discuss the cause of the highly (111) oriented IP-Al films in terms of the ion energy and plasma irradiation during deposition.

L8.7
INDEPENDENT MEASUREMENT OF COPPER FILM THICKNESS AND RESISTIVITY BY OPTO-ACOUSTIC TRANSIENT GRATING TECHNIQUE. A.A. Maznev, Michael Gostein, Philips Analytical, Natick, MA; John A. Rogers, Glen Kowach, Bell Laboratories, Lucent Technologies, Murray Hill, NJ.

Conventional techniques for electrical resistivity measurements such as four-point probe determine not the resistivity itself but rather the sheet resistance i.e. the product of the resistivity and film thickness. In this presentation, we show that a non-contact and nondestructive optical technique called Impulsive Stimulated Thermal Scattering (ISTS) is capable of measuring film thickness and resistivity independently. In this technique, lasers are used to impulsively generate and detect both surface acoustic waves and a thermally-induced displacement pattern at the sample surface. The measured acoustic frequency is determined by the film's thickness and mechanical properties while the decay time of the "thermal grating" is dependent on the film's thermal diffusivity. The latter is well correlated with the electrical conductivity in good conductors such as copper. Thus by measuring the acoustic frequency and thermal grating decay time one can extract both thickness and resistivity of a copper film. The concept has been demonstrated on a set of physical vapor deposited (PVD) Cu samples fabricated under different deposition conditions. The results obtained with the optoacoustic technique correlated well with resistivity and thickness data obtained by a combination of four-point probe and grazing-incidence X-ray reflectivity measurements.

L8.8
SPUTTERED Ta-Si DIFFUSION BARIER IN Cu/LOW k METALLIZATION. Shih-Chan Huang[a], Yu-Jen Chen[a], Xing-Jian Guo[b], and Fon-Shan Huang[a], [a]Institute of Electronics Engineering, National Tsing-Hua University, Hsin-Chu, TAIWAN; [b]Materials Science Center, National Tsing-Hua University, Hsin-Chu, TAIWAN.

As the low k dielectrics will be used in ULSI process, the fabrication temperature will reduced, so dose the requirement of the thermal stable temperature of diffusion barrier. In this report, sputtered Ta-Si amorphous film was investigated as a barrier material. The TaSi film was deposited by sputtering of $TaSi_2$ target in Ar gas. The resistivity of the film is about 200 $\mu\Omega$-cm. XRD, TEM, XPS, and AES were employed to understand the crystalline structure, chemical structure, and atomic composition. The thermal stability can be studied from C-V test. The MOS capacitors of sputtered Cu or electroplating Cu/Ta-Si(30 nm)/methylsilsesquioxane (MSQ), porous SiO_2 or SiO_2/p-Si structure were annealed at the temperature from 350°C to 500°C for 30 min in nitrogen ambient. The MSQ and porous SiO_2 films with thickness 200 nm were spin-coated on the Si wafer. The dielectric constant of these films was about 2.6. From the flat band shift and the variation of inversion capacitance, the diffusion performance can be evaluated. The thermal stable temperature can be up to 450°C. We also compare the barrier properties of amorphous Ta-Si film with that of poly-TaSi film. Finally, SIMS profiles of the above MOS capacitors are correlated to the electrical test.

L8.9
BEHAVIOUR OF ELECTROPLATED COPPER FILM IN THE EPCu/IMPCu/IMPTaN/SiO_2/Si MULTILAYER STRUCTURE. Khin Maung Latt [a], Y. K. Lee[a], H.L. Seng, T. Osipowicz. [a]School of Materials Engineering, Nanyang Technological University, SINGAPORE; Department of Physics, National University of Singapore, SINGAPORE.

Electroplated Cu film on a thin seed layer of IMP deposited Cu has been investigated in the EPCu (1μm)/IMPCu (150nm)/TaN (25nm)/SiO_2 (500nm)/Si multi-layer structure before and after annealing in nitrogen ambient for 35 min. The AFM results showed that the as-deposited IMP-TaN diffusion barrier was an amorphous phase with the roughness (RMS) of ∼0.369nm and the seed IMP-Cu layer had a grain size of around 30nm and the roughness (RMS) of ∼1.4nm. Consequently, the growth morphology of EP-Cu film on IMP-Cu seed layer was found to be more uniform and gave lower RMS values, resulting in a lower resistivity of EP-Cu film. The blanket EP-Cu film deposited on IMP-Cu seed layer had a predominantly (111) texture while IMP-Cu film deposited on IMP-TaN had a strong (220). After annealing at 750°C, the sheet resistance of the sample underwent an abrupt rise (∼ 200%) and several new peaks, Cu_2O and Ta_2O_5, were found. By annealing at 850^{circ}C, a new peak of $Cu_7Ta_{15}O_{41}$ appeared due to the reaction among Cu_2O, Ta_2O_5, Ta and Cu at the interface of Cu/TaN. No evidence of the diffusion of Cu through the barrier was detected even after annealing at 950°C. AFM measurement revealed that the average grain size of the as-deposited EP-Cu was around 1.0μm and it grew normally as annealing temperature increased. Average grain size after annealing at 750 and 850°C was 5 times larger than the film thickness as observed by SEM. Annealing temperatures higher than 850°C, Cu film starts to agglomerate due to the accelerated grain growth in EP-Cu film. At 950°C, Cu grains agglomerated each other disclosing part of Ta to the ambient. RBS results indicate the intermixing and/or reactions occurred in the structure after annealing at 750°C. However, a strong (111) preferred orientation of EP-Cu was maintained through out the annealing process.

L8.10
CHEMICAL VAPOR DEPOSITION (CVD) OF TUNGSTEN NITRIDE FOR DIFFUSION BARRIERS. Roy G. Gordon, Jeffrey T. Barton and Seigi Suh, Harvard Univ, Dept of Chemistry and Chemical Biology, Cambridge, MA.

A new process was developed for CVD of highly conformal, electrically conductive tungsten nitride (WN_x) films at low temperatures. The process uses the reaction of vapors of a tungsten amide and ammonia at a typical pressure of 100 Torr and temperatures from about 300-400°C. The tungsten precursor was vaporized by dissolving the solid in anhydrous liquid decane and nebulizing the solution into a flow of nitrogen carrier gas preheated to 150°C. The tungsten precursor vapor and ammonia were fed into separate manifolds of holes in the showerhead of a Novellus CVD reactor for 8 inch wafers. The composition, determined by Rutherford

backscattering spectroscopy (RBS) from films deposited on glassy carbon, was around $WN_{1.5}O_{0.2}$. The oxygen arises from impurities in the deposition chamber; its concentration is being reduced by the addition of purifiers and a load-lock. The growth rate (number of atoms deposited per unit area and unit time), also found from RBS, increased with the flow rate of ammonia. In the absence of ammonia, no film was detected. The thicknesses and step coverage were determined by scanning electron microscopy. The step coverage was essentially 100% in vias with aspect ratio of 5:1. The films are amorphous by X-ray diffraction. Electrical resistivity measurements and copper diffusion barrier properties will be reported.

L8.11
Transferred to L4.6

L8.12
ELECTRICAL CHARACTERIZATION OF COPPER PENETRATION EFFECTS IN THE GATE OXIDE OF MOS DEVICES. Francois Mondon, Jacques Cluzel, Denis Blachier, Gilles Reimbold and Lucile Arnaud, LETI-DMEL, CEA-Grenoble, FRANCE.

This paper addresses copper contamination in integrated devices through carrier generation lifetime killing and leakage current increase induced by copper penetration in device layers. MOS capacitors with thermal oxide (25 and 150 nm) and copper gate, with or without TiN barrier, were obtained by the damascene process. Thermal dry oxide provides good quality capacitors, allowing reliable electrical characterization. Copper penetration was tested by annealing at 450°C and bias-temperature stress BTS (250°C, 1 MV/cm, positive gate). Electrical characterization used C-V , generation lifetime derivation, i-V plots and mobile charge detection by TVS. Devices using a 10nm TiN barrier on 25nm oxide displayed a good stability. After annealing 10h at 450°C, generation lifetime, flat-bands voltage (Vfb) and leakage current remained unaffected. BTS caused only a slight lifetime reduction. Capacitors using Cu without barrier displayed a gradual lifetime decay (from ca. 150μs to 5μs) upon annealing, but no Vfb and leakage current variation. After BTS (10 min to 2h), the generation lifetime was too short to be measured. During stress, the leakage current increased by 3 decades, the same increase appearing on i-V plots. TVS plots displayed a broad peak, yielding charge densities from 10^{12} to 10^{14} cm^{-2}. In contrast, no significant Vfb shift appeared on the C-V plots. Moreover, a short negative stress restored the leakage current close to its initial value, cancelling also the TVS peak, but the lifetime remained nil. Despite copper reached the Si surface, less than 10^{10} cm^{-2} ionised copper is present in the oxide after BTS (according to the small Vfb shifts). That is yet enough to trigger electron conduction in oxide, which decays when Cu ions are removed from the oxide by negative gate bias. The TVS peak is then nothing but the electron current rise with voltage and gradual decay when Cu ions are driven back to the gate.

L8.13
Abstract Withdrawn.

L8.14
THREE-DIMENSIONAL COMPUTER SIMULATION OF MICROSTRUCTURE EVOLUTION IN TRENCHED STRUCTURE USED FOR DAMASCENE PROCESS. Jung-Kyu Jung, Young-Chang Joo, Seoul National University, School of Materials Science & Engineering, Seoul, KOREA; Young-Joon Park, Korea Institute of Science and Technology, Seoul, KOREA; Nong-Moon Hwang, Center for Microstructure Science of Materials, Seoul National University, Seoul and Korea Research Institute of Science and Standards, Taejon, KOREA.

Grain growth characteristics of a trench structure for a Damascene process, e.g. for fabrication of Cu interconnects, is studied by means of three-dimensional grain growth simulation. The microstructure of trench is complicated because abnormal grain growth as well as simultaneous growth from bottom and from sidewalls of the trench occurs. To investigate the mechanism of microstructure evolution in such a structure, a Monte Carlo method is used for the three-dimensional computer simulation in which abnormal grain growth is induced by anisotropy in grain boundary, free surface and interface energies. Various parameters like geometric aspect ratio of trench, ratio relationship between energy anisotropy factors, etc. are considered in the simulation. In order to examine the effect of a strongly oriented seed layer, the behaviors of grain growth on random or strongly oriented trench interface between seed layer and diffusion barrier are compared. The relative growth velocity of large grains to averaged ones is also analyzed to determine whether grain growth is characteristic of being abnormal or not. The results indicate that the anisotropy of free surface energy and interface energy are critical to microstructure evolution characteristics driven by abnormal grain growth. The anisotropy of grain boundary energy is less significant, but it affects the growth kinetics. These relationships would provide a clue on the origin of abnormal grain growth as well as help to realize bamboo-type grain structures, which are pursued for optimized reliability of trenched interconnects.

L8.15
COMPARITIVE GRAIN SIZE DISTRIBUTION AND GRAIN ORIENTATION DISTRIBUTION MEASUREMENTS FROM EBSD AND A NEW XRD TECHNIQUE ON COPPER FILMS AND INTERCONNECT LINES. Kris Kozaczek, Dave Kurtz, Roger Martin, HyperNex, Inc., State College, PA.

In recent years electron backscatter diffraction (EBSD) has emerged as a highly useful technique for quantitative analysis of grain orientation distribution and grain size distribution in thin films. However, the sequential grain-by-grain analysis protocol, combined with the requirement for carefully polished, uncapped samples places some limits on large-scale analysis with EBSD. An XRD technique has been developed which can simultaneously monitor grain size distributions and grain orientation distributions in thin films on a macro scale (20 to 300 micron diameter beam) compared to EBSD (sub-micron beam diameter) without the need for over-layer removal. The technique relies on the fact that continuous Debye rings transition to discontinuous spots as a smaller beam size is used to illuminate fewer grains. Multiple partial Debye rings that are discontinuous (spotty) are collected from an area detector and used to generate an orientation distribution function from which texture volume fractions can be redisplayed. The grain size distribution is determined from the intensity distribution of the diffraction spots, each spot representing one grain. Comparative measurement examples for EBSD and the XRD technique for blanket and variable line width Cu films will be shown. Good correlation for both grain size and grain orientation has been demonstrated between the two techniques.

L8.16
X-RAY POLE FIGURE ANALYSIS OF PREFERRED IN-PLANE ORIENTATION IN INLAID COPPER INTERCONNECT LINES. Paul R. Besser, Technology Development Group, Advanced Micro Devices, Inc., Austin, TX; Delrose Winter, Richard Ortega, AMIA Laboratories-Rigaku, The Woodlands, TX; and Ehrenfried Zschech, Werner Blum, Advanced Micro Devices Saxony Manufacturing GmbH, Dresden, GERMANY.

The crystallographic texture of inlaid Cu lines has been quantified by (111), (110) and (100) pole figure analysis using X-Ray diffraction as a function of anneal temperature (pre and post-CMP). Cu lines 0.45 μm deep and 0.35, 0.7 and 1.06 μm wide were produced using conventional fabrication techniques for inlaid Cu lines. The crystallographic texture is predominantly (111) out-of-plane with sidewall-nucleated grains in narrow lines. It will be shown that the (111) grains nucleated from the trench bottom have a preferred in-plane orientation with the aa0 direction parallel to the sidewall, and that the sidewall-nucleated grains have a preferred in-plane orientation as well, with the aa0 direction parallel to the trench bottom. The preferred in-plane orientation results from minimization of the surface energy by the Cu grains. A 5 degree splitting of the X-Ray diffraction peaks from sidewall-nucleated grains will be shown, suggesting that the sidewall-nucleated (111) grains are tilted by 5 degree with respect to normal to the trench bottom. It will be shown that the 5 degree tilt results of the non-vertical trench sidewalls. Also, the texture will be shown to be independent of when the anneal is done (pre or post CMP) and the anneal temperature.

L8.17
A ROLE OF INTERFACE IMPURITIES ON ADHESION BEHAVIOR OF CVD COPPER FILMS. Young Suk Kim and Yukihiro Shimogaki, Department of Materials Engineering, University of Tokyo, Tokyo, JAPAN.

Chemical Vapor Deposition (CVD) is considered an important technology for the deposition of copper (Cu) thin films during the fabrication of future ULSI devices primarily due to excellent step coverage. In the near future, Cu-CVD process will be combined as seed or filling layer fabrication with electroplating. However, CVD Cu films deposited on common barrier layers has a poor adhesion, which influences chemical mechanical polishing (CMP) process, reliability problem and contact resistance. Thus, reliable interfacial bonding of Cu seed layer deposited by CVD is a critical factor for future application. We describe the adhesion characteristics of CVD Cu films deposited on various barrier layers depending on the type of substrate, the barrier preparation process, the interface residuals and the surface roughness. Adhesion strength of the Cu films on CVD TiN prepared by in-situ exhibited better adhesion due to formation of $Cu(OH)_2$ at the interface. The X-ray photoelectron spectroscopy (XPS) results revealed that the formation of $Cu(OH)_2$ was considered to improve the adhesion strength and to be facilitated by unstable intermediate components of substrate such as $Ti(OH)_x$ and sub-oxide. Increased surface roughness of CVD TiN films were considered to

contribute the improved adhesion due to mechanical anchoring and large surface areas to contact. A significant accumulation of fluorine and Ta-F bonding on Ta surface were observed, which is one of factor reducing adhesion strength. Among the factors affecting the adhesion, interface impurities such as F from Cu precursor and Cl from $TiCl_4$ were mainly studied to reveal the adhesion behavior with introducing F and Cl source intentionally. PVD Cu as well as CVD Cu was deposited to examine the effect of impurities more clearly. The adhesion characteristic will be discussed with using XPS in detail.

SESSION L9: POSTER SESSION
ELECTROMIGRATION & RELIABILITY
Chairs: Robert F. Cook, Mihal E. Gross, Paul S. Ho,
Robert D. Miller and Masanori Murakami
Wednesday Evening, April 18, 2001
8:00 PM
Salon 1-7 (Marriott)

L9.1
ANALYSIS OF ELECTROMIGRATION EXTRUSION FAILURE MODE IN DAMASCENE COPPER INTERCONNECTS.
Lucile Arnaud, Gerard Tartavel, Francois Mondon, Robert Truche, CEA LETI, Grenoble, FRANCE; Thierry Berger, ST Microelectronics, Crolles, FRANCE.

Cu hillocks have often been observed as a consequence of electromigration in Cu damascene interconnects passivated with SiO_2. In this study, we have compared, for the first time, lifetimes deduced from hillocks formation with lifetimes associated to voids generation. The Cu damascene lines are fabricated with CVD copper deposited on CVD TiN (10 nm), encapsulated with SiN (40 nm) and passivated with SiO_2 (1μm). The test structure used a straight stripe (test line, length 800 μm), with voltage and current contact pads at both ends. Two line widths (3 μm and 0.5 μm) provided respectively polygrain or quasi-bamboo Cu microstructure. The test line was surrounded on both sides, at the same and at upper metal levels, by other metal lines acting as extrusion detectors. The failure criterion for void formation was set to 10 % test line resistance increase while failure criterion for hillock formation was the occurrence of a 0.1 mA current flowing in the extrusion detector circuit subjected to 2 V bias. For all test conditions (oven temperatures set to 250, 300 and 350°C and current densities set to 4 and 6 MA/cm^2), extrusion failure mode always occurred significantly before void failure. The time to failure of each mode was computed separately with Blacks equation using a global analysis. Activation energy of void formation was 0.82 eV (resp 1.03 eV) for wide lines (resp narrow lines). These values are consistent with SEM observations showing grain boundary diffusion in polygrain microstructure and interface diffusion in quasi-bamboo microstructure. Moreover, for both linewidths, activation energy of hillocks formation was lower than the value obtained for voids formation. FIB cross-section showed the typical shape of hillocks and help us to propose hypothesis to explain this failure mechanism It is concluded that hillocks failure mode should be taken into account in electromigration design rules because it provided extrapolated lifetimes 10 times lower than the value calculated with void failure mode. This work has been carried out within the CCMC consortium between CEA-LETI and STMicroelectronics.

L9.2
THE EFFECT OF INITIAL VOID CONFIGURATION ON THE MORPHOLOGICAL EVOLUTION UNDER THE ACTION OF NORMALIZED ELECTRON WIND FORCES.
Ersin Emre Oren, Tarik Omer Ogurtani, Middle East Technical Univ, Dept of Metallurgical and Materials Engineering, Ankara, TURKEY.

In these studies a comprehensive picture of void shape evolution dynamics and its strong dependence on the initial configuration has been thoroughly investigated by utilizing hypocycloid algebra to generate four different shapes of main interest. Our mathematical model on the isotropic diffusion and mass accumulation on void surfaces, under the action of applied electrostatic potential and capillary effects, follows a novel irreversible but discrete thermodynamic formalism of interphases and surfaces. As a result during the intragranual motion, in addition to the crescent-like slit formation, very rich and also unusual void morphological variations such as fragmentations into the daughter voids or inner island generation have been observed under the severe (normalized) electron wind intensities or very long exposure times. In these numerical experiments, the Euler's method of finite differences with an automatic time step self-adjustment has been utilized in combination with a rather powerful and fast boundary element method (BEM) for the solution of the Laplace equation.

L9.3
COMPARATIVE STUDY ON WAFER-LEVEL AND PACKAGE-LEVEL ELECTROMIGRATION RELIABILITY FOR SUB-QUARTER MICRON LOGIC DEVICES.
Young-Bae Park, H.H. Ryu, W.G. Lee, Hyundai Electronics Industries Co., Ltd., SYSTEM IC R&D Center, Cheongju, KOREA.

Dependence of the microstructures, electrical resistance and electromigration reliability of aluminum interconnections on the wide range variations of aluminum deposition conditions and metal stack structure are investigated. Effects of several Ti and TiN composite layers under Aluminum are compared for the conventional, collimated, and IMP (Ionized Metal Plasma) sputtering deposition methods. And the effects of aluminum deposition thickness, power and temperature variations are also investigated. Structural characterizations are performed using XRD, FIB, AFM and cross-sectional TEM. And electrical characterizations are performed by the measurements of sheet resistance from blanket films and Kelvin resistance from multi-level metallization test pattern structures. Also, electromigration lifetimes of metal line pattern are compared using both package-level and wafer-level electromigration testing method which uses highly accelerated test conditions over conventional package-level electromigration test. And the correlation between the two methods is investigated. Effects of variable metal stack structures on electromigration reliability and electrical resistance of interconnections can be well explained from aluminum (111) texture analysis and interfacial reaction results. Finally, optimum metal stack structure is developed for sub-quarter micron logic devices.

L9.4
INVESTIGATING THE MICROSTRUCTURE-RELIABILITY RELATIONSHIP IN Cu DAMASCENE LINES.
David P. Field, Washington State Univ, School of Mechanical and Materials Engineering, Pullman, WA; Dieter Dornisch, Huayu (Jonathan) H. Tong, Conexant Systems, Inc., Newport Beach, CA.

The continuing performance increase of integrated circuit structures has necessitated the implementation of Cu as an interconnect material. The present work focuses upon characterizing the microstructure of Cu damascene lines and investigating the reliability of the test structures as a function of microstructural characteristics. The lines were fabricated using various processing paths including self-annealing and high temperature annealing. The microstructures were characterized using focused ion beam imaging, transmission electron microscopy and orientation imaging microscopy techniques. The differences in microstructure were correlated with reliability of the test structures as determined from accelerated electromigration tests. It is apparent that the microstructure of Cu damascene lines can be altered substantially by changing the fabrication process. The grain morphology is of primary importance in predicting reliability from the microstructure. This will be discussed in connection with defining microstructural parameters for use in modeling the electromigration behavior of Cu damascene structures.

L9.5
FORMATION OF A STRONG (001) TEXTURE IN THERMALLY CYCLED COPPER THIN FILMS.
M. Wada, J. Koike, K. Maruyama, Tohoku University, Dept. of Materials Science, Sendai, JAPAN.

Cu is a new interconnect material for semiconductor devices. Electromigration (EM) has been known to be a major reliability problem during device operation. In the case of Al interconnects, sharply textured films are more resistant against EM because of the possible formation of special grain boundaries with slow atomic diffusivity. However, in Cu thin films, little information is available for texture and grain-boundary structure. Our aim is to investigate texture variation by various heat treatments. Samples were composed of the layers of Cu 500nm / Ta 20nm / Si(110) wafer. The Ta and Cu layers were deposited by RF magnetron sputtering. Some samples were heated to 723 K immediately after deposition, while others were kept at room temperature for one month before thermal cycling was performed. Texture information and grain-boundary structure type were obtained by EBSP. Microstructure was observed by SEM and TEM. The as-deposited films had a strong $< 111 >$ texture. When thermal cycling was performed immediately after deposition, large grains of the $< 100 >$ orientation were formed in the most part of the film. Thermally processed voids were very few to be observed. In addition, approximately 95% of all grain boundaries of this film was either small-angle boudnaries or special boundaries of a low atomic diffusivity. The nucleation of the $< 100 >$ grains were found to occur by twinning of the $< 221 >$ grains. The subsequent selected growth of the $< 100 >$ grains was attributed to much smaller biaxial elastic strain energy for the $< 100 >$ grains than for other low-index grains. In contrast, the $< 111 >$ texture was stabilized in the samples kept at room-temperature. Only small portion of the film had turned to the $< 100 >$ grains by subsequent thermal cycling. The present work offers a possibility of producing new Cu interconnects with excellent EM and SM resistance.

L9.6
EFFECTS OF CONTACT RESISTANCE ON CURRENT

CROWDING AND CRITICAL PRODUCT OF ELECTROMIGRATION IN BLECH STRUCTURES. Everett C.C. Yeh, K.N. Tu, Dept. of Materials Science and Engineering, UCLA, Los Angeles, CA.

In using Blech structures to study electromigration, current density has been assumed to be the same in the similar sets of short strips deposited on an under-layer. But this is not true owing to the existence of contact resistance between the strips and the under-layer. It has been shown experimentally that the contact resistance between strips and under-layer is very sensitive to fabrication processes. A high contact resistance reduces the maximum current in the strip. Also, it diffuses the current detouring between the strip/under-layer interface from a narrow crowding to a wide spreading window. In other words, it suppresses or even eliminates current crowding in Blech structures. In this work, we simulate these phenomena of current reduction and spreading in terms of contact resistance and film thickness, both are key factors in controlling current distribution in a Blech structure. We explore their effects on back stress and incubation time of void formation in short strips. We demonstrate these effects by the discrepancy in critical product measurements found in experiments using similar Blech structures.

L9.7
INTEGRATION AND ELECTROMIGRATION RELIABILITY OF CVD-PVD ALUMINUM INTERONNECTS. Won-Jun Lee, Jung Joo Kim, Suk Jae Lee, Jong Yoon Yoon, Heung Lak Park, Hyundai Electronics, Memory R&D Div, Kyonggi-do, KOREA; Sa-Kyun Rha, Taejon National Univ of Technology, Dept of Materials Engineering, Taejon, KOREA.

CVD-PVD Al process is promising as the metallization method in low-cost dynamic random access memory (DRAM) manufacturing, because it forms plugs and wires simultaneously. In this work, a CVD-PVD Al process was successfully integrated into a 4-giga-bit DRAM process flow, and its electromigration reliability was compared with that of the conventional W plug process. The multilayer film of MOCVD TiN/ionized PVD Ti was used as the underlayer of CVD Al from dimethylaluminum hydride (DMAH), and thin CVD Al film functioned as an effective wetting layer for the subsequent PVD Al reflow. Sub-quarter-micron vias with high aspect ratio (up to 10) was completely filled with Al at the wafer temperature below 400°C. The CVD-PVD Al plug process exhibited via resistance lower than that of the conventional W plug process. The effect of process parameters on via resistance was examined. The CVD-PVD Al plug process showed different electromigration behavior than that of the W plug process. Most electromigration failures were catastrophic and they occurred at the Al plugs for the CVD-PVD Al samples, whereas the resistance of the electromigration test structure increased gradually until the failure time and voids were observed at the Al wires over/under the W studs for the W-plug samples. The difference in the electromigration behavior of the Al-plug samples and the W-plug samples was explained by the structural and geometrical difference between them. Finally, the application of CVD-PVD Al process to the dual damascene Al process flow will be also presented.

L9.8
COMPARISON OF GRAIN BOUNDARY DIHEDRAL ANGLE DISTRIBUTIONS IN Cu AND Al THIN FILMS FABRICATED BY VARIOUS DEPOSITION METHODS. Jong-Min Paik, Min-Seung Yoon, Young-Chang Joo, Seoul National University, School of Materials Science & Engineering, Seoul, KOREA; Young-Joon Park, Korea Institute of Science and Technology, Seoul, KOREA.

In electroplated copper films used in ULSI interconnects, the evolution of microstructure at room temperature known as self-annealing has been observed. Since self-annealing is not observed in the metal films fabricated by CVD or PVD methods, self-annealing seems to be related to the inherent characteristics of electroplated copper. In order to investigate microstructural characteristics of electroplated copper, we compared the distribution of dihedral angles at the grain boundary triple junctions of electroplated copper films with those of sputtered copper and aluminum films. Textures and grain size distributions were analyzed as well. For electroplated copper films, FWHM(Full Width at Half Maximum) of dihedral angle distribution was significantly larger (67.3°) than those of annealed electroplated copper (41.9°), sputtered copper (42.6°) and aluminum (35.5°). Simulation on dihedral angle distribution shows that the exceptionally large FWHM of electroplated copper films is due to the large deviation in the grain boundary energies, and this may suggest grain boundaries of electroplated Cu films are in the singular states. In a system where singular grain boundaries exist, abnormal grain growth has been observed as in the case of self-annealing. The detailed observation of grain boundaries of electroplated Cu films and the possible origin for singularity in grain boundaries are discussed.

L9.9
EFFECTS OF BOUNDARY CONDITIONS AND ANISOTROPY ON SAMPLES LOADED IN FOUR-POINT BENDING. S.K. Kaldor, Columbia University, Department of Applied Physics and Applied Mathematics, Program in Materials Science, New York, NY; I.C. Noyan, IBM Research Division, Yorktown Heights, NY.

Four-point bending, a technique often employed for loading specimens to known stress levels, is especially appropriate for testing brittle samples which are difficult to pull in uniaxial tension. This method has found application in the microelectronics area where it is used in the testing of single crystal specimens for VLSI. Typically, in these problems, 1-D bending solutions which assume material isotropy are employed [1]. Semiconductor test samples, however, are generally anisotropic and possess dimensions that make it difficult to determine whether beam or plate solutions are more appropriate [2]. We describe a finite element model of Si single crystal substrates loaded in a four-point configuration and report the effects of boundary conditions, sample dimensions, and anisotropic material constants on the model. Finally, we compare our modeling results to experimental data. [1] P. Scardi, Y.H. Dong, S. Setti, and V. Fontanari. Proceedings of the Sixth International Conference on Residual Stress. Oxford, UK. Vol. 1, pp. 67-73 (2000). [2] S.K. Kaldor and I.C. Noyan. Proceedings of the SEM IX International Congress on Experimental Mechanics. Orlando, FL. pp. 808-811 (2000).

SESSION L10/N6: JOINT SESSION METAL/POLYMER ADHESION IN CHIP PASSIVATION AND PACKAGING

Chairs: F. Patrick McCluskey and Reinhold H. Dauskardt
Thursday Morning, April 19, 2001
Golden Gate B2 (Marriott)

8:30 AM *L10.1/N6.1
CHEMISTRY AT METAL/POLYMER INTERFACES FOR ELECTRONICS. R.L. Opila, Bell Labs, Lucent Technologies, Murray Hill, NJ.

Interfaces between metals and polymers are of increasing importance in electronics. Applications that use polymers include electronics packaging, Cu and low-k dielectrics, and displays that utilize semiconducting polymers. We have used electron spectroscopy to study chemical reactions between a variety of metals (Cu, Ti, Ta, Cr, Al) and polymers (polyimide, PPV, and various low-k dielectrics). While greater metal reactivity with the polymer may yield greater initial adhesion, often the reliability degrades with time. In addition, adhesion is only one of the factors that must be considered-the role of barrier layers as conductors and/or diffusion barriers must also be considered. Great insight into the chemistry of these systems has been gained by studying the adsorption of metals onto thiol-based self-assembled monolayers on Au. We have used novel applications of photoelectron spectroscopy and x-ray absorption spectroscopy to study evolution of the buried interfaces, and thus the long-term performance of the system. Extensions of these studies to contacts with semiconducting polymers will be discussed.

9:00 AM L10.2/N6.2
ESTIMATION OF THE INTERFACIAL FRACTURE ENERGY OF METAL/POLYMER SYSTEM IN MICROELECTRONIC PACKAGING. J.Y. Song, S.I. Cho, Jin Yu, Center for Electronic Packaging Materials, Korea Advanced Institute of Science and Technology, Taejon, KOREA.

In the microelectronic packaging, reliability of the metal/polymer interfaces is an important issue and many test methods have been used to measure the adhesion strength of the interfaces. In the present work, we measured the adhesion strength of flexible two layer tapes made of Cu/Cr/Polyimide(PI) using the T peel test. The steady state peel strengths(P) were measured along with the peel angle and maximum root curvatures(K_B) behind the peel front, which were directly measured by using an optical camera. Then, effects of the biased rf plasma pretreatment and the metal layer thickness on the T peel strength were investigated, and the energy dissipated by plastic bending(Ψ) were deduced based on the elastic/plastic analysis and measured root curvatures. The interfacial fracture energy(Γ) was the subtraction of Ψ from P. It was found that the peel strength and the plastic bending work increased with the rf plasma power density(ρ) and then saturated. And the same was true of Γ. With the metal layer thickness, P and Ψ showed maximum due to the balance between crystal volume effect and compliance effect, however, interfacial fracture energy, Γ= P - Ψ, was more or less independent of the metal layer thickness, suggesting it to be an interface material parameter. The interfacial fracture toughnesses of the Cu/Cr/PI interface were measured using fracture mechanics specimens and compared to the

interfacial fracture energies deduced from the T peel test. Another method used to measure the interfacial fracture toughness of the Cu/Cr/PI interface was the nanoindentation test using the W superlayer sputter-deposited on Cu film, which induced the interfacial delamination. Effects of the W superlayer thickness and residual stresses in the Cu and W films on the interfacial fracture toughness were also investigated.

9:15 AM L10.3/N6.3

FINITE ELEMENT ANALYSIS OF COPPER ADHESION TO POLYMER ENCAPSULANT. Flordivino Basco, ON Semiconductor Philippines, Inc., Technical Operations Department, Carmona, Cavite, PHILIPPINES.

Finite element analysis is used to analyze the button shear test. Through the use of experimental data the adhesion strength of interfaces involved in test are characterized. It was found that adhesion strength of each interface could be characterized by dimensionless parameter. The parameter is used to understand the delamination occurring in the interface of the encapsulating molding compound (EMC) and the back of the die flag (BDF), which is made of copper. Through this adhesion strength of the EMC-BDF interface is identified and compared with saturated vapor pressure to see if the interface will delaminate at a given reflow temperature. Furthermore, the adhesion strength of the intervening layer of oxide is identified, which is very difficult to do in actual experiment.

9:30 AM L10.4/N6.4

ADHESION MECHANISMS OF SILANE ADHESION PROMOTERS IN MICROELECTRONIC PACKAGING. Maura Jenkins, Jeffrey Snodgrass, Gretchen DeVries, Reinhold H. Dauskardt, John C. Bravman, Stanford University, Dept of Materials Science and Engineering, Stanford, CA.

Silane adhesion promoters are seeing increasing use in microelectronic packaging interfaces. For example, they are currently used to adhere the passivating polymer overlayer to oxide, and these materials are being investigated as surface treatments for silica particles in underfill epoxies. Until recently, the exact mechanism of adhesion promotion was postulated. In this paper, we present detailed studies of silane adhesion promoters on the silicon oxide surface. Two common promoters (aminopropyltriethoxysilane and vinyltriethoxysilane) as well as non-functional silanes are investigated. It was found that without a functional end group, long carbon chain silanes can severely degrade adhesion, resulting in interfaces weaker than if no silane is used. Several spin coat solution formulations are used in depositing these films. Resulting surface coverage is examined and quantified with the help of AFM and XPS. Then, the adhesion behavior of various promoter films are tested in sandwich structures using a fracture mechanics approach. Finally, spin-coat solution concentration, surface coverage, and interface fracture energy are compared for the amine functional promoter.

9:45 AM L10.5/N6.5

METAL/POLYMER INTERFACE AND SOLDER JOINT RELIABILITY OF A WAFER LEVEL CSP. H. Han, Jin Yu, K.O. Lee and I.S. Park, Dept. MS&E, Center for Electronic Packaging Materials, Korea Advanced Institute of Science and Technology, Taejon, KOREA.

As microelectronic devices get smaller and higher I/O densities are required, various chip scale packages (CSP) are adopted, and wafer-level chip scale package (WLCSP) combined with flip chip technology has the highest potential. In doing so, it is necessary to redistribute peripheral bond pads and relax the thermal stress in the WLCSP. Here, we use a low modulus polymers as the stress buffer layer (SBL) to relax the thermal stress generated at the solder joint and studied the reliabilities of the metal/SBL interface and solder joint using peel tests and ball shear tests, and effects of the polymer surface pretreatments by the RF plasma and runner metal structure were investigated. Results showed that the adhesion strength of the metal/SBL interface depended on the RF power density (ρ) and runner metal structure. The peel strength (P) was very low for $\rho < 0.27 W/cm^2$ but increased up to $\rho = 0.3 W/cm^2$ and tended to saturate around 1000g/cm. Then failure locus analyses were conducted using AFM, AES, and XPS. The peeling locus of peel test and the failure locus of solder ball shear test were dependent on the Ni layer in the under bump metallurgy (UBM) and also on the thickness of the runner metal, particularly the thickness of Cu layer. Depending on the metal deposition condition, metal films over SBL were delaminated or buckled due to the residual stress in the metal film, which was measured using the laser curvature method. Additionally, stress strain fields and crack initiation and propagation behaviors around the solder joint were analyzed using micro-Moire pattern and the correlated to the process parameters and package structures. Then, implications to the package processes and designs were discussed

10:30 AM L10.6/N6.6

HIGH Tg, LOW DIELECTRIC CONSTANT AROMATIC BENZOXAZOLES CONTAINING ALLYLETHER PENDENT GROUPS FOR USE IN MICROELECTRONIC PACKAGING. Max D. Alexander, Jr., Thuy D. Dang, Christina E. Specker, Marlene Houtz, R.J. Spry, and Fred E. Arnold, Air Force Research Laboratory, Materials and Manufacturing Directorate, Polymer Core Technology Area, Wright-Patterson Air Force Base, OH.

Next generation microelectronic packaging requirements are driving the need to produce increasingly lower dielectric constant materials while maintaining high thermal stability and ease of processing. Polymer candidates with low dielectric constant (2.0-2.4), high thermal stability (degradation temperature $> 400°C$), high glass transition temperature ($> 350°C$), low water uptake ($< 1\%$), solubility in selected organic solvents, low thermal expansion coefficient and the capability for undergoing post-polymerization chemistry to impart insolubility after processing have been successfully synthesized and characterized by our research group. Highly fused ring structures, formed via intramolecular hydrogen bonding, were utilized for the enhancement of the glass transition temperature. Lowering of the dielectric constants of these polymeric structures was accomplished by the incorporation of perfluoroisopropyl groups along the polymer backbone. The design of post-polymer reactions to impart insolubility to select polymer candidates was based on the methodology of attachment of crosslinking sites to the polymer backbone. Aromatic benzoxazoles containing pendant allylether groups were synthesized from the parent structures. Upon heating, the polymer would undergo an intramolecular rearrangement reaction (Claisen rearrangement), resulting in a Tg enhancement by increasing the number of fused rings via intramolecular hydrogen bonding between the in situ-formed hydroyl groups and the nitrogen atom of the adjacent benzoxazole group. At elevated temperature (250-300°C), crosslinking of the allyl groups would occur, thus providing a mechanism for insolubility and dimensional stability of the polymer system. Efforts are underway to control the crosslinking density of the polymer system by partial allylation of the hydroxyl groups attached to the aromatic benzoxazoles. We will address several issues relating to integration of these polymeric materials into current processes and how we have tailored our systems, to address issues such as back etching, adhesion, dimensional stability, and conformal coating of small feature sizes.

10:45 AM *L10.7/N6.7

MOLECULAR INTERACTIONS AND ADHESION FOR INTERFACES RELEVANT TO FLIP-CHIP ASSEMBLIES Raymond A. Pearson, Lehigh University, Dept of Materials Sci. & Eng., Bethlehem, PA.

Debonding is a common wear-out mechanism in flip-chip assemblies that utilize organic substrates. The large mismatch of the thermal expansion coefficients of the silicon chip and the organic substrate generates significant stresses during thermal cycling. These thermally induced stresses promote debonding at several interfaces and debonding at the underfill-passivation interface can occur. This paper focuses on developing an understanding between interfacial molecular interactions and adhesive strength in an effort to 'engineer' reliable interfaces. The experimental approach consists of studying the adsorption of model epoxy systems onto polyimide and borosilicate surfaces using a flow microcalorimeter and separating these interfaces using double cantilever beam specimens. Acid-base theory is utilized to explain the trends in adhesion strength.

11:15 AM *L10.8/N6.8

THERMOMECHANICAL RATCHETING IN INTERCONNECTS. Z. Suo, M. Huang, Mechanical and Aerospace Engineering Department and Materials Institute, Princeton University, Princeton, NJ; Q. Ma and H. Fujimoto, Intel Corporation, Santa Clara, CA; J. He, Intel Corporation, Components Research, Hillsboro, OR.

Temperature cycling has long been used as an accelerated reliability test to qualify new electronic products. Many commonly observed failure modes, however, are so poorly understood that the extrapolation of the test results to service lifetime is empirical, loosely based on historical records of similar products. This lack of mechanistic understanding is particularly disconcerting when new interconnect materials are being explored. We have initiated a program to study mechanisms of failure modes under temperature cycling. In this talk, we present our recent study on cracking in the SiN film. The SiN film has been widely used as a passivation layer in microelectronic devices. It has been known for over a decade that the SiN film cracks after packaged devices are thermally cycled. While engineering solutions have been proposed on the basis of trial and error, no basic understanding of the cause of the cracking has been identified before. In this talk, we show that the cyclic temperature, coupled with the shear stress at the die corner, causes the

interconnect pads underneath the SIN films to undergo plastic ratcheting. Consequently, in the SiN films the stress builds up as the temperature cycles, leading to cracks. We compare the effects of copper and aluminum interconnects. Implications for design rules and qualification tests are discussed.

11:45 AM L10.9/N6.9
DIELECTRIC PROPERTIES OF FERROELECTRIC CERAMICS-POLYMER COMPOSITE FILMS. C.K. Chiang, L.P. Sung and J. Obrzut, National Institute of Standards and Technology, Gaithersburg, MD.

The ferroelectric ceramic-polymer composite thin-film is one of important electronic packaging materials. The dielectric constant of a ceramic-polymer composite thin film follows an empirical logarithmic mixing rule when the powder is dispersed uniformly. The low dielectric polymer matrix usually dominates the dielectric constant of the composite. For example, a composite containing 30 volume percent of barium titanate powder in an acrylic polymer shows the dielectric constant about 21 at 1 kHz. This value is much less than that of ceramic powder in the composite. Further increasing the concentration of the filler has only limited effect on the increase of the dielectric constants. We used laser scanning confocal microscopy and optical microscopy to examine the distribution of particles. The thin-slice images of the thickness of the order of one micron and re-constructed 3D image from them allowed us to visualize the relation of micron-size particles and the polymer interface between them nondestructively. These data may correlate to the dielectric constant of composite thin-films from different processing conditions.

SESSION L11: LOW-k DIELECTRICS - INTEGRATION AND MECHANICAL PROPERTIES
Chairs: Robert F. Cook and Michael W. Lane
Thursday Afternoon, April 19, 2001
Golden Gate B2 (Marriott)

1:30 PM *L11.1
Pe-CVD LOW DIELECTRIC CONSTANT MATERIALS. Andrew J. McKerrow, J.S. Martin, K.J. Taylor, A.K.R. Ralston, T. Tsui, D. Morris, G. Xing, H. Hong, and J.D. Luttmer, Silicon Technology Research, Texas Instruments Inc., Dallas, TX.

Improvements in transistor performance with scaling place increasing demands on interconnect performance and thereby necessitate fundamental changes in its architecture. This includes replacing aluminum metalization with copper metalization, thereby reducing the interconnect resistance delay. At the same or a subsequent technology node most SC manufacturers are also replacing the tradition silicon dioxide, SiO_2, insulator with materials that are characterized by a lower dielectric constant. The introduction of these low dielectric constant materials, or low-k materials, is intended to improve the interconnect capacitance delay. Pe-CVD deposited SiO_2 is characterized by a dielectric constant of 4.1-4.2. There are a number of materials that are deposited by Pe-CVD, or similarly, that are characterized by a lower dielectric constant and could potentially replace SiO_2 in high performance interconnects. Candidate materials include fluorine-doped SiO_2 or FSG, k = 3.5-3.8, organosilicate glasses or OGSs, k = 3.0-2.7, and even lower dielectric constant teflon-like materials, k = 2.2-2.0. In the $k < 3$ regime there are a number of candidate materials that are deposited via spin coating, i.e. spin-on low-k materials. This presentation will focus on those materials deposited by plasma methods, HDP or PECVD, and that likely to be integrated at the 0.18 or 0.13 μm technology nodes. Process technology improvements and material characterization of HDP-FSG films that led to the development of production worthy FSG films will be discussed (based on Martin et. al., American Vacuum Society, 47th International Symposium, Oct. 2000). This presentation will include a discussion of the materials properties of OSG films that affect their integration in high performance interconnects including stress corrosion cracking and patterning using chemically-amplified resists.

2:00 PM L11.2
THE EFFECT OF CARBON ON THE ADHESION AND DEBONDING OF LOW-k DIELECTRIC ORGANOSILICON FILMS (Si:O:H:C) IN MULTI-LAYER THIN-FILM STRUCTURES. Jee Eun Rim, Frank Shi, Reinhold Dauskardt, Stanford Univ, Dept of MS&E, Stanford, CA.

Incorporating organic carbon groups such as methyl groups into the Si-O network of silicon dioxide is one way of lowering the dielectric constants of ILDs in integrated circuits. However, in general, this has a detrimental effect on the mechanical properties of the dielectric film. Of particular interest in terms of device reliability is the interface adhesion between the dielectric and adjoining films in the multi-layer stack. In this study, the effect of increasing carbon content on the adhesion to adjacent materials and the intrinsic fracture resistance is adressed. Thin film fracture mechanics techniques were employed to test these multi-layer thin film structures containing organosilicon films (Si:O:H:C) prepared by both spin-on glass (SOG) and CVD methods. XPS scans at the resulting fracture surfaces were used to characterize the weak microstructural paths to failure. Adhesion and fracture mechanisms will be discussed in terms of the organosilicon glass network structure.

2:15 PM L11.3
PREDICTION ON LOWER LIMITS OF DIELECTRIC CONSTANT FOR LOW k DIELECTRICS RESTRICTED BY A MECHANICAL STRENGTH. Nobuo Aoi, Takuya Fukuda and Hironori Matsunaga, Environmental Process Technology Laboratory, Semiconductor Technology Research Department, Association of Super-Advanced Electronics Technologies, Yokohama, JAPAN.

By decreasing film density, dielectric constant can be reduced. However, simultaneously mechanical strength of the films drastically becomes weaker. Therefore, there may exist some restrictions of lowering dielectric constant of dielectric films arising from degradation of mechanical strength. Some estimations of such limitation are our major concern. We evaluated elastic modulus of various inorganic low k films and inorganic porous ones and that of various organic low k by means of a nano-indentation. Relations of modulus vs. density for various low k films exhibited linear dependencies having positive slopes with negative intercepts for inorganic, porous inorganic, and organic low k groups, respectively. This fact indicates that reduction of dielectric constant of low k films realized by lowering film density will be confronted with a physical limitation caused by a degradation of mechanical strength. According to the relation, which bases on the assumption that density reduction of films is caused by a homogeneous dispersion of fine spherical pores in films, dependencies of dielectric constants of various low k films upon film density can be described. From the relations between modulus versus film density, and between dielectric constant versus film density, new relations between modulus and dielectric constant can be obtained. From the relations, it is concluded that modulus of inorganic low k films decreases abruptly with decreasing of dielectric constant in comparison with moderate decrease of organic low k ones. The values of modulus for organic low k films becomes larger than those of inorganic ones in the region of dielectric constant lower than c.a. 2.5, and in the region of dielectric constants lower than 2.0, modulus of inorganic porous low k films become larger. This work was performed under the management of ASET in Ministry of International Trade and Industry (MITI) and New Energy and Industrial Technology Development Organization (NEDO).

2:30 PM L11.4
COMPARATIVE STUDY OF MECHANICAL PROPERTIES AND INTERCONNECT PROCESS PERFORMANCE FOR NANOPOROUS SILICA FILMS OF VARIOUS POROSITY. Hui-Jung Wu, Fan Zhang, Jessie Chen, Teresa Ramos, Rob Roth, Doug Smith, Lisa Brungardt, Steve Wallace, Anh Duong, Victor Lu, Ha Le, Allan Nguyen, Jude Dunne, and Jim Drage, Honeywell International, Honeywell Electronic Materials, Sunnyvale, CA.

Successful development of ultra low dielectric constant (k) insulating films is a critical part of the semiconductor industry technical roadmap. This industry is considering the use of insulating films with a k value in the 2.5 to 1.5 range for the 0.13 um to 0.07 um device generations; in these device generations the insulating film would be part of a damascene interconnect structure with Cu as the conductor metal. Nanoglass^{TM} E films, a form of nanoporous silica, can be made with k values that cover this k range. In this paper we describe the experimental results using Nanoglass^{TM} E films which cover a range of porosity values. For these films we report general physical and chemical properties and results from interconnect module tests. Key physical properties of the films (such as k, refractive index, average pore size, pore size distribution, surface area, elastic modulus, harness) are reported. The films are also compared for their performance in various module processes which are used in fabricating Cu damascene structures. These processes include CMP performance (polish rate, defect density). The work shows that Nanoglass^{TM} E films can tolerate the typical CMP conditions which are used for removal of excess Cu in damascene structures.

2:45 PM L11.5
PROCESSING OF XLK^{TM} SPIN ON DIELECTRIC MATERIALS FOR NEXT GENERATION INTERCONNECT TECHNOLOGY. Jeffrey N. Bremmer, Eric Moyer, Tom Deis, Les Carpenter, Todd Bridgewater, Wei Chen, Akihiko Kobayashi, Mike Bourbina, Dow Corning Corporation, Auburn, MI.

A new dielectric material has been developed to meet the emerging needs of advanced interconnects beyond the 0.18 μm technology node. Dow Corning XLK dielectric is a porous spin on material based on

silsesquioxane resin chemistry and offers a tunable dielectric constant of k = 2.0-2.5. Films processed from XLK offer a good balance of electrical and mechanical properties. Discussed in this paper are various options of processing XLK and the influence of processing on structure and properties of XLK thin films.

3:30 PM L11.6
POROSITY EFFECT ON THERMAL CONDUCTIVITY OF ORGANOSILICATE GLASS FILMS. Junjun Liu, Chuan Hu, Michael Kiene, Paul S. Ho, Microelectronic Research Center, University of Texas, Austin, TX; W. Volksen and R.D. Miller, IBM Almaden Research Center, San Jose, CA.

The introduction of porous materials as intra-layer ultra-low K dielectrics faces the trade off between enhanced dielectric property and degraded thermal and thermo-mechanical properties. The formation of network of open pores at high porosity is thought to cause reliability problems. Closed-cell low porosity OrganoSilicate Glass (OSG) films become very interesting because it avoids the formation of network of pores. More rigid structure and better thermal conductivity and thermo-mechanical properties are expected of this material. We have characterized the thermal and dielectric properties of low porosity OSG films prepared by incorporation of macromolecular "porogens"[1]. Using 3ω technique[2], the dependence of thermal conductivity on porosity has been determined. Correlated study on dielectric constants was performed with C-V measurement. The results have been compared with those obtained for high porosity xerogel silica films[2]. Low porosity OSG films were found to follow a better scaling rule of thermal conductivity as a function of porosity. Possible mechanisms of the effects of pore morphology on properties will be discussed. [1] R.D. Miller et al., Mat. Res. Soc., Symposium Proceeding, Vol. 565, p.3 (1999) [2] C. Hu et al., Mat. Res. Soc. Symposium Proceeding, Vol. 565, p. 87(1999)

3:45 PM L11.7
ENVIRONMENTAL EFFECTS ON STRESS-CORROSION CRACKING OF ORGANOSILICATE GLASS (OSG) LOW-k DIELECTRIC FILMS. Dylan Morris[a], Ting Tsui[b], Andrew McKerrow[b]. [a]Department of Chemical Engineering and Materials Science, University of Minnesota, Minneapolis, MN; [b]Silicon Technology Research (SiTR), Texas Instruments Inc., Dallas, TX.

Low dielectric constant materials of a wide variety are currently being evaluated as replacements for silicon dioxide, SiO_2, in high performance interconnects. In all cases the mechanical properties (modulus, hardness, and fracture toughness) of such low-k materials differ considerably from those of SiO_2 . Another significant difference between standard Pe-CVD SiO_2 films and most low-k materials is that films of the former are characterized by compressive residual stress at room temperature, while films of the latter are typically tensile. One of the challenges associated with interconnect fabrication using such low-k materials is the potential for stress-corrosion cracking in the presence of an aqueous environment; a process that requires a tensile driving force and chemical bonding in the film that can be hydrolyzed at the crack tip. One class of low-k films, organosilicate glasses (OSG), are integrated with tensile stress, contain Si-O bonds that are susceptible to chemical hydrolysis, and are therefore candidates for stress corrosion cracking. To better understand the fracture properties of OSG materials the steady-state crack velocity under different aqueous environments were measured. It was observed that moisture absorption reduces the film residual stress and crack velocity significantly. The pH of the reactive environment is shown to have a discernable effect on the steady-state cracking velocity. The relationship between the chemical makeup of the films and the corresponding resistance to stress-corrosion cracking will be discussed.

4:00 PM L11.8
EFFECTS OF MICROSTRUCTURE AND MOLECULAR WEIGHT OF POLYSILSESQUIOXANES ON MECHANICAL AND DIELECTRIC PROPERTIES OF THIN FILMS. J.-K. Lee, H.-J. Kim, H.W. Ro, E.S. Park, D.Y. Yoo, D.Y. Yoon, School of Chemisty; K. Char, School of Chemical Enginering, Seoul National University, Seoul, KOREA; H.W. Rhee, Dept of Chemical Engineering, Sogang University, Seoul, KOREA.

We have prepared polysilsesquioxanes with systematically varying organic moieties (methyl, ethyl, propyl, and phenyl, for example) and molecular weights of the polymer structures, and investigated their microstructures and physical properties of thin films. The local microstrucres as determined from the MALDI-TOF and FT-IR data as function of the polymerization time change markedly with the nature of organic moieties, forming ladderlike, cagelike or highly branched structures, through the varying degree of intramolecular versus intermolecular condensation reactions. The local microstructures in turn are found to strongly influence the mechanical properties (hardness and crack resistance) while only a small effect is seen for the dielectric properties.

4:15 PM L11.9
ADHESION AND RELIABILITY IN METHYLSILSESQUIOXANE DIELECTRICS. Dan Maidenberg, Stanford Univ, Dept of Materials Science and Engineering, Stanford, CA; Willi Volksen, Robert Miller, IBM Almaden Research Center, San Jose, CA; Reinhold Dauskardt, Stanford Univ, Dept of Materials Science and Engineering, Stanford, CA.

Methylsilsesquioxane (MSSQ) is an important new interlayer dielectric. It is an attractive candidate for the replacement of silica due to its low base dielectric constant and the relative ease of creating porous morphologies. However, it is necessary to understand the adhesion and inherent crack growth resistance of the material before full-scale integration. This study investigates the inherent toughness of MSSQ as well as its adhesion to a variety of layers. The measurements were made using fracture mechanics techniques that eliminate the effects of residual stress. This is crucial, because CMP and thermal mismatch with other layers in the structure create stresses in addition to any residual stresses in the film. The effect of salient compositional and microstructural factors such as porosity, connectivity, and porogen remnants was examined. In addition, the effect of adhesion promoters and surface modification via UV-Ozone and electron beam techniques will be described. The implications of such microstructural and surface modifications on fracture and adhesion mechanisms is discussed. Of special interest is the discovery that some of the porogen does not fully decompose in the porous material. In some instances, however, this effect is helpful rather than detrimental to the interfacial adhesion.

4:30 PM L11.10
THE EFFECT OF PLASTICITY IN POLYMER LOW-k FILMS ON INTERFACIAL ADHESION. Christopher S. Litteken, Reinhold H. Dauskardt, Department of Materials Science and Engineering, Stanford University, Stanford, CA.

The development of new organic low-k materials has provided an opportunity to examine plastic energy dissipation in thin polymer films. Unlike most brittle oxides and organic hybrids, polymer low-k thermosets have been observed to be ductile and more resistant to interfacial debonding. Macroscopic adhesion was determined by measuring the critical strain energy release rate (Gc) of a stable debond located within a thin film structure comprised of the polymer, metal, and barrier layers. The plastic energy dissipated in the polymer layer was controlled by varying the thickness of the layer and the distance between the layer and debond. The benefit of such plastic energy dissipation is often not observed for thin metal layers such as Al and Cu due to strengthening mechanisms. Alternatively, polymer yield properties are not sensitive to layer thickness over similar length scales and offer the possibility of being controlled with chemistry and curing cycles. Finally, the yield properties and plastic energy dissipation can also be manipulated by changing the stress state of the ductile layer. Interfacial adhesion was measured for thin film structures that included patterned channels with selected aspect ratios and dimensions of the order of the ductile layer thickness. Results will be discussed in terms of the prevailing mechanism of deformation in the polymer channels.

SESSION L12: POROUS LOW-k DIELECTRICS - CHARACTERIZATION

Chairs: Shu Yang and Kenneth P. Rodbell
Friday Morning, April 20, 2001
Golden Gate B2 (Marriott)

8:30 AM L12.1
LOW-k, POROUS METHYLSILSESQUIOXANE FOR INTERLEVEL DIELECTRIC APPLICATIONS. Agnes M. Padovani, Hyun-dam Jeong, Sue Ann Bidstrup Allen, Paul A. Kohl, School of Chemical Engineering, Georgia Institute of Technology, Atlanta, GA.

This project focuses on the development, characterization, and optimization of the properties of silsesquioxane-based, porous, low dielectric constant materials for use as interlevel dielectrics. The goal is to modify a commercially available spin-on-glass (methylsilsesquioxane), and introduce porosity into the films to lower the effective dielectric constant of the silsesquioxane by the incorporation of air. The pores are created by adding a sacrificial polymer (substituted norbornene polymer) to the silsesquioxane matrix. The sacrificial polymer is then thermally decomposed to form nano-size pores ($\sim$ 5 nm) within the films. Studies to evaluate the pore size and distribution, chemical bonding of the sacrificial polymer to the spin-on-glass, mechanical and optical properties, and the permeation of decomposition products through the silsesquioxane matrix will be reported. Transmission electron microscopy and small angle X-ray scattering experiments were performed to investigate the pore size distribution as a function of polymer molecular weight, concentration and type of functional groups within the polymer, and

polymer loading level. NMR and FT-IR spectroscopies were used to probe the bonding of the polymer to the glass prior to curing and pore formation. The mechanical properties were investigated by nano-indentation techniques. In general, it was shown that the porous films had superior fracture toughness (resistance to cracking) compared to those without pores. The moisture absorption and optical properties of the porous silsesquioxane films were characterized.

8:45 AM L12.2
NANOPOROUS, LOW DIELECTRIC CONSTANT ORGANOSILICATES PREPARED FROM ORGANIC/INORGANIC NANOCOMPOSITES: EFFECT OF MACRMOLECULAR ARCHITECTURE ON STRUCTURE DEVELOPMENT.
James L. Hedrick, Robert D. Miller, Craig J. Hawker, Willi Volksen, IBM Research, Almaden Research Center, San Jose, CA.

A general route to organic-inorganic hybrids with nanophase morphologies has been elaborated with the objective of ultimately templating nanoporosity in organosilicates (SSQ). The compatablization of the organic template and the SSQ on the nanoscopic size scale is critical and was accomplished using polymers containing significant functionality and multiple chain ends. Poly(caprolactone) is ideally suited for such applications since functionality in the main chanin and the end groups interact significantly with the SSQ to facilitate the compatiblization of the dissimilar materials, and because it thermally decomposes quantitatively into monomer. Novel synthetic routes allowed dendritic, hyperbranched and denritic-linear hybrid architectures to be prepared. These polymers were readily soluble initially in the organosilicate prepolymer (methyl silsesquioxane, MSSQ), however, upon the onset of crosslinking, both the solubility parameters and molecular weight of the organosilicate (PMSSQ) change causing the polymer template to phase separate by a nucleation and growth process. The organic polymer was selectively removed by thermolysis, producing a nanoporous inorganic structure. The size and shape of the pores are identical to those of the initial hybrid morphology (< 100A), and the effect of the macromolecular architeture on the morphology is significant. A reduction in the dielectric constant was achieved by simply replacing a portion of the glass matrix with air which has a dielectric constant of 1.0.

9:00 AM L12.3
CHARACTERIZATION AND Cu METALLIZATION OF MOLECULARLY TEMPLATED NANOPOROUS SILICA DIELECTRICS. F.M. Pan, T.G. Tsai, B.W. Wu, National Nano Device Laboratories, Hsinchu, TAIWAN; A.T. Cho, C.M. Yang, K.J. Chao, Department of Chemistry, National Tsinghua University, Hsinchu, TAIWAN; L.D. Chao, Department of Materials Science and Engineering, National Tsinghua University, Hsinchu, TAIWAN.

Molecularly templated nanoporous silica films have an ordered pore structure and uniform size distribution. The dielectric constant and mechanical strength of the nanoporous silica films can be well controlled by their porosity, hydrophobicity and pore structure, and, therefore, they have a great advantage over aerogel and zerogel silica films in terms of being a potential intermetal dielectric material for sub-130 nm technology nodes. In the study, we have prepared nanoporous films by spinning on the silica sol-gel, with which various organic template molecules were mixed, on silicon wafers. The nanoporous silica films have a porosity of ~70%, and the pore size is estimated to be about 4.5 nm according to krypton adsorption and desorption isotherms. XRD and TEM results clearly show that the porous films have an ordered microstructure. MIS capacitor structure was fabricated to measure the electrical characteristics of the nanoporous silica films. The nanoporous silica films exhibit an ultra low k value over a range of 1.5-2.0 depending on film modification methods, such as hexamethyldisilazane (HMDS) vapor exposure or plasma treatments. A leakage current density in the order of 10^{-7}A/cm^2 can be readily obtained for the silica films under a stress of 2MV/cm. Combining with TDS, FTIR and the electrical characterization, the nanoporous films demonstrate very good thermal and dielectric stabilities. Copper and tantalum nitride films have been PVD deposited on a bare or a Si_3N_4 capped nanoporous silica film. The TaN film behaves as a very good diffusion barrier for Cu diffusion up to an anneal temperature above 400°C. The Cu/TaN deposited nanoporous silica film was subjected to the chemical-mechanical polishing process, and collapse of the silica film due to mechanical stress during CMP was not observed. The study shows that molecularly templated nanoporous films are very compatible with contemporary IC processing technology.

9:15 AM L12.4
STRUCTURE AND MICROMECHANICAL CHARACTERIZATION OF NANOPOROUS ORGANOSILICATE THIN FILMS. K. Char, S.-H. Chu, D. Kim and J.-G. Lee, School of Chemical Engineering, Seoul National University, Seoul, KOREA; J.-K. Lee, H.W. Ro, D.Y. Yoo, and D.Y. Yoon, Department of Chemistry, Seoul National University, Seoul, KOREA; M.Y. Jin, Advanced Materials Division, Korea Research Institute of Chemical Technology, Taejon, KOREA; S.Y. Kim, Department of Chemistry, Korea Advanced Institute of Science and Technology, Taejon, KOREA; J.-H. Hahn, Korea Research Institute of Standards and Science, Taejon, KOREA.

As the feature size in advanced ULSI microelectronic devices shrinks continuously, it is expected that low-k interlayer dielectric materials with k lower than 2.5 would be needed around 2003. A continuous reduction of the dielectric constant k is also believed to be possible only by incorporating nanometer-sized pores filled with air ($k = 1.0$) into the electrically insulating matrices such as poly(methyl silsesquioxane) (PMSSQ). Micromechanical properties of the nanoporous ultralow-k thin films becomes more important than ever since the films are required to withstand severe mechanical stress conditions imposed by the chemical mechanical planarization (CMP) processes and the thermal expansion mismatch of multilevel BEOL films. Whenever air is incorporated into ultrathin films for lowering k, the mechanical strength of the films is sacrificed. To minimize this effect, the pores should exist in the film as closed cells in nanometer scale. In this study, nanoporous ultra low-k films were prepared with PMSSQ and star-shaped poly(caprolactone) (PCL), both of which were synthesized to control molecular weight and functionality. Nanoporous structures including shape, size, and distribution of pores across the film were investigated using field emission scanning electron microscopy, cross-sectional transmission electron microscopy, atomic force microscopy and high-resolution X-ray reflectivity. Micromechanical characterizations were also carried out, using a nanoindentor and a microvickers, to measure hardness, modulus and crack-propagation velocity of the nanoporous thin films, showing a strong correlation between structure and micromechanical properties.

9:30 AM L12.5
NOVEL METHOD FOR PRODUCING NANOPOROUS DIELECTRIC FILMS. Bashar I. Lahlouh, Xupeng Chen, Xuejun Wang, Shubhra Gangopadhyay, Department of Physics, Texas Tech Univeristy, Lubbock, TX; Juan Sun, Prathamesh Doshi, and Sindee L. Simon, Department of Chemical Engineering, Texas Tech Univeristy, Lubbock, TX.

We have prepared amorphous silicon carbide (a-SiC:H) films using a liquid source in a plasma enhanced chemical vapor deposition(PECVD)system. The dielectric constant of the films ranges from 3 to 5 and depends strongly on process parameters. We are working on a novel method for introducing porosity in a-SiC:H films. In this method, nanopores are introduced by swelling the film with inert supercritical CO_2 and subsequently depressurizing the gas to form nanoporous structures. The film thickness and refractive index were measured using a prism coupler and the dielectric constant was measured using mercury probe technique. Our preliminary work shows that when a-SiC:H film with dielectric constant of 3.0 was swelled at 1500 psi CO_2 pressure for two hours followed by rapid depressurization, the film thickness increased by 2.1 ±0.1% and the refractive index decreased by 2.7 ±0.1%. The dielectric constant reduced by 6.0 ±0.2% (from 3.0 to 2.8). Increasing CO_2 pressure is anticipated to increase the CO_2 absorption in the films, thereby further reducing the dielectric constant. The effect of CO_2 processing temperature and pressure on the porosity and dielectric constant of films prepared under various PECVD conditions will be discussed.

10:15 AM *L12.6
POROSITY CHARACTERIZATION OF MESOPOROUS DIELECTRIC THIN FILMS USING POSITRON ANNIHILATION SPECTROSCOPY. M.P. Petkov, M.H. Weber, K.G. Lynn, Dept. of Physics, Washington State University, Pullman, WA; K.P. Rodbell, IBM T.J. Watson Research Center, Yorktown Heights, NY; W. Volksen, R.D. Miller, IBM Almaden Research Center, San Jose, CA.

Beam based Positron Annihilation Spectroscopy (PAS) is a recent addition to the spectrum of diagnostic tools useful for the characterization of low-dielectric constant (low-k) thin films. Using the annihilation signatures of positronium (Ps: H-like positron-electron atom), PAS provides information on total porosity, pore size, pore size distribution and void interconnectivity (percolation) as a function of film depth. In this paper, we show examples of the utility of various PAS techniques to characterize porous MSSQ films as a function of porogen load (5-50 wt.%). PALS, 3g-Ps annihilation, and Doppler Broadening were used to obtain a global picture of film porosity. We report results from measurements of mesoporous MSSQ spin-on films (0.6 um thick), in which the porosity was created using a sacrificial porogen approach. The PAS results are subsequently compared to more traditional characterization techniques including CV, AC-conductivity, FE-SEM, FTIR, TGA, elipsometry, and hardness measurements.

10:45 AM L12.7
POROSITY AND STIFFNESS OF AEROGEL FILMS

CHARACTERISED BY WIDEBAND ULTRASONIC SURFACE WAVES. Colm M. Flannery, Paul Drude Institute for Solid State Electronics, Berlin, GERMANY; C. Murray, I. Streiter, S.E. Schulz, Centre for Microtechnologies, TU Chemnitz, GERMANY.

Density/porosity is the most important parameter determining properties of porous films, however it is difficult to measure. This work reports characterization of density/porosity and Young's modulus values of a range of nanoporous silica aerogel films via dispersion of laser-generated wideband surface acoustic waves. The technique shows clear relations between dielectric constant, porosity and Young's modulus. Density and Young's modulus of submicron thickness aerogel thin films have been measured from dispersion of laser-generated wideband surface acoustic waves. The films had porosities of 60–70% and Young's moduli of ≈ 1-2 GPa. Both density/porosity and Young's modulus show a strong correlation with film dielectric constant. Young's modulus is shown to reduce drastically with porosity, providing valuable information about material stiffness which is of vital importance with respect to ability to withstand chemical-mechanical polishing. The technique provides absolute values of density and Young's modulus, rather than relative. Porosity can be measured to better than 1%. The technique is rapid, relatively cheap and nondestructive, and has the potential to provide density measurements quicker and more accurately than other techniques. The additional ability to assess stiffness is a further advantage. Use of the method can provide valuable process control to develop and standardise nanoporous silica film properties, the lack of such a technique has severely hindered development of such films.

11:00 AM L12.8
POROSITY IN LOW-k DIELECTRICS: EFFECTS OF THE TRANSITION FROM CLOSED TO OPEN CELL POROSITY. Michael W. Lane and Kenneth P. Rodbell, IBM T.J. Watson Research Center, Yorktown Heights, NY; Willi Volksen and Robert D. Miller, IBM Almaden Research Center, San Jose, CA.

The drive for faster interconnects dictates that materials with a dielectric constant, k, lower than that of SiO_2 (k ∼ 3.9) must be incorporated into future device technologies. A number of candidates ranging from organic to inorganic films have emerged. However, the general consensus is that solid films will not be able to provide the ultra low dielectric constant (k < 2.0) needed for future applications. To this end, dielectrics which contain embedded voids have been proposed to lower the dielectric constant towards that of air (k ∼ 1.0). While inserting voids into a material may produce favorable results in regards to electrical properties, it may have deleterious effects on the mechanical properties of the material. Accordingly, this work focuses on characterizing the effects of porosity on the electrical and adhesive properties of porous MSSQ. Positron annihilation studies are used to quantify the porosity in the films and identify the transition from closed cell to open cell porosity. Four-point flexure adhesion measurements were made and the fracture path was characterized by AFM and EDX. The adhesive properties of the porous MSSQ were found to depend strongly on the transition from closed to open celled porosity.

11:15 AM *L12.9
PROBING BARRIER INTEGRITY ON POROUS LOW-K THIN FILMS USING POSITRONIUM ANNIHILATION LIFETIME SPECTROSCOPY. Jianing Sun, Terry L. Dull, Albert F. Yee, MS&E Dept., Univ. of Michigan, Ann Arbor, MI; David W. Gidley, William E. Frieze, Dept. of Physics, Univ. of Michigan, Ann Arbor, MI; E. Todd Ryan, Simon Lin and Jeff Wetzel, SEMATECH, Austin, TX.

Positronium annihilation lifetime spectroscopy (PALS) has been used to investigate the continuity and thermal stability of thin barrier layers designed to prevent Cu diffusion into porous silica low dielectric constant (k) films. Honeywell Nanoglass^{TM} K2.2-A10C, a porous organosilicate film, is determined to have interconnected pores with an average diameter of 6.9±0.4 nm, assuming the pores are tubular in shape. Cu deposited directly on the A10C films is observed to diffuse into the porous structure. The minimum necessary barrier thickness for stable continuity of Ta and TaN deposited on A10C is determined by detecting the signal of positronium (Ps) escaping into vacuum. It is found that the 25 nm thick layers do not form continuous barriers. This is confirmed by the presence of holes observed in such films using a transmission electronic microscope (TEM). Although 35 nm and 45 nm Ta and TaN layers perform effectively at room temperature as Ps barriers, only the Ta-capped samples are able to withstand heat treatments up to 500C without breakdown or penetration into the porous film. TaN interdiffusion into the silica pores is indicated by the reduction of the Ps lifetime after high annealing temperatures. The procedures to standardize the testing of barrier layer integrity and thermal stability using PALS are proposed. Progress in extending this method to probe barrier integrity in realistic trenches or vias will be presented.

11:45 AM L12.10
A NEW X-RAY SCATTERING METHOD FOR DETERMINING PORE-SIZE DISTRIBUTION IN LOW-k THIN FILMS. Kazuhiko Omote, X-Ray Research Laboratory, Rigaku Corp, Tokyo, JAPAN; Shigeru Kawamura, Technology Development Center, Tokyo Electron Ltd, Yamanashi, JAPAN.

Low-k dielectrics are extensively interested for producing ultra-high density integrated circuits. Nanometer-sized pores are introduced into thin silica, polymer or their hybrid thin films for reducing the dielectric constant of the materials. The structure of the pore and its size distribution are very closely related with physical properties of the materials. Thus, a rapid and simple method is important for determining the pore size distribution in submicron films on thick substrates. The use of gas adsorption analysis, neutron scattering, and positron annihilation lifetime spectroscopy has been reported previously. In our laboratory, we tried to use x-ray scattering, which is a very common and simple technique for determining nanometer-size structures. However, the transmission geometry used in x-ray small angle scattering is not applicable since x-ray photons can not transmit the substrate material. Furthermore, the conventional specular reflection geometry can not be used because of strong x-ray reflection from the substrate. We, therefore, have developed a new method for avoiding specular reflected x-rays in measuring small angle scattering patterns only from the porous thin films. It is important to correct for refraction and reflection at the surface because it interferes with the small angle scattering data. The pore size distribution of a film is determined by a comparison of a simulated x-ray small-angle scattering pattern with that of the observed data. We also compared the results of our method with that from the gas adsorption analysis. A good agreement has been obtained, even though the analytical models of both methods are different.