SYMPOSIUM M

Chemical-Mechanical Polishing Advances and Future Challenges

April 18 – 20, 2001

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* Invited paper

SESSION M1: CMP: RECENT DEVELOPMENTS / PADS AND RELATED ISSUES
Chairs: Suryadevara Babu and Manabu Tsujimura
Wednesday Morning, April 18, 2001
Golden Gate A1 (Marriott)

8:30 AM *M1.1
RECENT ADVANCES IN CMP TECHNOLOGY. Malcolm Grief, Randy Harwood, Eric Woods, Sanjay Basak, Fadi Elkhodr, Jim Schlueter, Mark Ferra, Dan Trojan and Saket Chadda, Speedfam-IPEC, Chandler, AZ.

Chemical Mechanical Planarization (CMP) has become an essential unit process for fabricating state of the art devices. CMP started primarily for dielectric applications. The purpose of dielectric CMP was to increase planarization length, such that steppers could print without exceeding the depth of focus budget. Dielectric CMP continues to evolve with With-in-wafer Non-Uniformity (WIWNU) as the primary metric for improvement. Dielectric CMP was followed by W CMP applications for definition of plugs (contact and via). Primary motivation for W CMP was defect density reduction. Development efforts in W CMP are focussed towards improving oxide erosion and plug recess. Shallow Trench Isolation (STI) was adopted as a CMP application starting at the 0.35-0.25 micron technology nodes. STI reduced real estate usage while defining effective isolation of devices. Development efforts are primarily focussed on direct STI and therefore in reducing overall variation (WTWNU, WIWNU, & WIDNU). Next, CMP enabled copper interconnects. Copper CMP challenges are well known and primary drivers for development are oxide erosion, oxide loss, dishing, and defectivity. Finally, there are an increasing number of integration schemes for definition of High K gates requiring multiple CMP steps. This paper will discuss advances in CMP technology that address key drivers of different CMP applications. These advances include better In-situ End point detection, superior carrier technology, and the combination of advantages of rotary platforms (rigid platen) with those of orbital platform (kinematics and through the pad slurry delivery). State of the art results from Speedfam-IPECs new MomentumTM platform for copper, Tungsten and oxide/STI will also be shown. There are three basic types of tools available in the marketplace: Rotary, Linear, and Orbital. This paper will discuss key differences and the ramifications on the total variation: With-In-Wafer Non-Uniformity (WIWNU) and With-in-Die Non-Uniformity (WIDNU).

9:00 AM M1.2
A NOVEL OXIDE CMP FOR DAMASCENE GATE FORMATION. Hyung-Hwan Kim, Sang-Ick Lee, Hyungjun Kim, Se-Aug Jang, Tae-Kyun Kim, Yong-Joo Noh, Jae-Hong Kim, Jae-Hong Lee, Chul-Woo Nam, Memory R&D Division, Hyundai Electronics Industries Co. Ltd., Ichon, KOREA.

A damascene or replacement gate process has been drawing an intensive interest due to its capability to avoid thermal or plasma-damage occurred during conventional RIE process. This replacement gate process normally adapts poly-silicon dummy gate. Source/drain implantation is performed self-aligned to the dummy gate, followed by replacing the dummy gates with W or Al metal gates. To replace dummy gates with metal gates, the top surface of the dummy gate needs to be exposed by removing the overlaying inter-level dielectric (ILD) oxide using conventional CMP process. Exposed dummy gates are removed by wet-etching. In this study, ceria-based slurry was used for ILD CMP and compared with conventional silica-based slurry. Since the ceria slurry shows high polishing selectivity of oxide to poly-silicon as well as oxide to nitride, poly-silicon dummy gates could be successfully acted as a stopping layer during ILD CMP process. As a result, process window could be significantly enlarged and final gate height could be maintained very uniformly compared with the case using conventional silica base slurry. However, TEM analysis showed that very thin layer was formed on top of poly-silicon dummy gate after polishing with ceria base slurry. It was found that this thin layer made subsequent wet-etching of dummy gate impossible. In order to avoid this issue, we developed a new process and possible mechanism on the formation of this blocking layers was proposed.

9:15 AM *M1.3
WHY ABRASIVE FREE Cu SLURRY IS PROMISING? Yasuo Kamigata, Yasushi Kurata, Katsuyuki Masuda, Jin Amanokura, Masato Yoshida, Hitachi Chemical Co., Ltd., Research & Development Center, Tsukuba, JAPAN; Masanobu Hanazono, Hitachi Chemical Co., Ltd., Electronic Devices Materials Operations Division, Tokyo JAPAN.

To obtain reduced number of micro-scratches and reduced remaining polishing particles in the fabrication of Copper interconnection circuites, we developed "Abrasive Free Polishing slurry". By applying this newly developed slurry, we were able to achieve improved values of Dishing and Erosion for circuit patterns. Using "Abrasive Free Slurry" in the damascene CMP process, excellent properties of multi-layerd Copper circuits were fabricated. Details of this slurry and the topography and electrical characteristics obtained using this slurry will be discussed.

9:45 AM *M1.4
ROTATIONAL AVERAGING OF MATERIAL REMOVAL DURING CMP. David R. Evans, SHARP Laboratories of America, Camas, WA; Michael R. Oliver, Rodel Inc, Newark, DE.

At present, several different competing mechanical configurations are used in chemical mechanical polishing. These range from classical rotary designs to orbital and linear systems as well as the more recent web format. Invariably, wafer rotation is used in all of these systems to average out gross material removal rates. To the uninitiated, this would perhaps seem to be so obvious that no further investigation is necessary. However, the interaction of polishing pad microstructure, along with whatever abrasive particles and chemical agents that might be present is in reality quite complex. In addition, fluid transport between wafer and pad surfaces is strongly affected by pad macrostructure and relative motion of the two surfaces. In the present work it has been found that in the absence of rotational averaging correlated variations in material removal rate can be observed "downstream" from patterned features on the wafer surface. Furthermore, the correlation length is quite long and can be related to micro and macrostructural viscoelastic properties of the polishing pad material. Specifically, relaxation time for decompression of pad asperities is a major determinant of the correlation length. It should be emphasized that this is an entirely separate issue from "planarization length" as commonly defined. Also, in the absence of rotational averaging, very strong "leading edge effect" is often observed. This is characterized by very high material removal rates at the leading edge of the wafer. In contrast, at the trailing edge removal rates are very low and may even vanish altogether. In addition to the usual process variables (down force, slurry flow, etc.), this behavior is governed by the angle of attack of the wafer relative to the pad. Obviously, rotation of the wafer during polishing converts any leading to trailing edge gradient in material removal rate to radial non-uniformity. In normal operation, this will be confounded with additional sources of radial non-uniformity due to slurry distribution, back pressure, etc. In the present work these effects can be separated and quantified.

10:45 AM M1.5
DE-PUZZLING THE ORIGIN OF A CMP-ASSOCIATED "CENTER SPIKE" YIELD/RELIABILITY ISSUE. IS CMP TO BE BLAMED FOR ITS APPEARANCE? Yehiel Gotkis, David Wei, John Boyd and Rodney Kistler, Lam Research Corporation, CMP/Clean Division, Fremont, CA.

A long-lasting CMP related yield/reliability puzzle - thickness spike, frequently appearing at the wafer center after CMP operation, was studied. Optical film thickness measurements for pre- and post-CMP film were combined with surface topography profiling. Wafer surface profile was also studied after the oxide film was HF-etched out. It was found that the post-CMP thickness spike is not caused by CMP malfunctioning however originates to a specific bare silicon defect type and occurs when the bare silicon wafer has a narrow dip-like defect in its center. The scenario of the "anti-spike" formation could be portrayed as: 1. Bare silicon wafer comes with a dip-like defect in its center. 2. Oxide deposition, having high step coverage properties, follows the profile of the bare silicon wafer and fills the dip. Optical thickness measurements tools, being not sensitive to the height variations, are not capable to detect the dip. 3. CMP, doing its planarization job and flattening the surface, creates a local thickness bulge, actually an "anti-spike" pattern filling the bare silicon dip in the wafer center. The higher is the CMP planarization efficiency and the narrower and deeper is the bare silicon dip, the more pronounced is the spike pattern. An uniformly thick but topographically non-flat underlying topography copying film is transformed by CMP into a planarized flat-top film with inevitable thickness variations (thin elevated sections and thick elevated sections), which is exactly what planarization technique is supposed to produce. The center spike generation scenario explaining the appearance of the film thickness spike in the wafer center reveals the root cause of this phenomenon- bare silicon dip-like defect located exactly in the wafer center, which most probably is originated to the specificity of the silicon crystal growth. This scenario also indicates that yield failures related to the center spike problem supposed to be associated with under-etched plug holes and, as a result, electrical opens. It also explains why the photolithography operation also experiences problems in these cases and what is the nature of the problems. Surface non-flatness obviously causes so-called "Focus depth" problems in this case, which finally result in numerous electrical and functional failures. The size of the dip normally is about 4 mm in diameter, which may affect either 1 or 4 dies depending on wafer layout approach. The origin of the dip in

the bare silicon wafer center is under investigation. Up to this point it was found that the dip is not originated to the thermal shrinkage of the silicon in the wafer center. The center-spike phenomenon could be considered as an example of extremely long-range CMP related integration interaction of a narrow dip-like microdefect at the bare silicon wafer surface and high planarization efficiency of the CMP process.

11:00 AM M1.6
EFFECTS OF NANO-SCALE ABRASIVE SIZE ON THE CHEMICAL MECHANICAL POLISHING OF SiO_2. Chunhong Zhou, Lei Shan, Rob Hight, Steven Danyluk, the George W. Woodruff School of Mechanical Engineering, Georgia Institute of Technology, Atlanta, GA; S.H. Ng, Gintic Institute of Manufacturing Technology, Singapore, SINGAPORE; Andrew J. Paszkowski, Chemical Products Corporation, Cartersville, GA.

This paper addresses the influence of the size of the abrasive in a slurry while the polishing a thermally-grown silicon dioxide deposited on 100 mm diameter (100) p-type single crystal silicon wafers. The sizes of the abrasive particles (colloidal silica) were 10, 20, 80, 140 and a 1:1 mix of 80/140 nm. The slurries contained 30% by weight abrasive particles stabilized with KOH. Experimental results demonstrate that the polishing rate and surface roughness are sensitive to the particle size and there exists an optimum abrasive particle size in terms of removal rate. A "nano-film" theory based on the pad roughness is used to explain the phenomenon. Keywords: Abrasives; Material Removal Rate; Chemical Mechanical Polishing; Surface Finish.

11:15 AM M1.7
POLYURETHANE PAD DEGRADATION AND WEAR DUE TO TUNGSTEN AND OXIDE CMP. Amy L. Moy and Joseph Cecchi, University of New Mexico, Chemical and Nuclear Engineering Department, Albuquerque, NM; Dale Hetherington and David Stein, Sandia National Laboratories, Microelectronics Development Laboratory, Chemical Mechanical Polishing, Albuquerque, NM.

Chemical Mechanical Polishing (CMP) of both silicon dioxide and tungsten films utilizes Rodel IC1400 polyurethane polishing pads and alumina (tungsten) and silica (oxide) abrasives. The purpose of this research is to examine the structural, chemical, and mechanical property changes due to CMP of tungsten and oxide films. The physical and chemical properties of a polishing pad are not well understood. These property changes due to polishing will affect the removal rate, wafer uniformity, and pad life. The degradation of the pad has been examined using Electron Microprobe, Confocal, SEM, TEM, DMA, TMA, XRD, FTIR, and Raman analyses. Tungsten and oxide polishing mechanisms are very different. Tungsten polishing is more a combination of chemical and mechanical abrasion, whereas, oxide polishing is more mechanical than chemical. Based on the FTIR spectra, the oxide polishing resulted in only one detectable structural change in the polyurethane hard segment. Tungsten polishing, however, resulted in various structural chemical changesas well as the displacement of various elements such as Cl, Al, and I in the pad. The properties of the polyurethane are dependent on the ratio of the isocyanate hard and the polyol soft segment, which change due to CMP. The result of the reduction in the isocyanate hard segment and the formation of the carboxylic group may increase the pad hydrophilicity. The swelling of the polyurethane pad during polishing is due to the increase absorption of water from the slurry system into the pad. The presence of the slurry abrasive in the pad after polishing may affect the performance of the pad. Mesa or "flat top" formation occurs at a faster rate without conditioning for both oxide and tungsten polishing and affects polishing performance. Conditioning effectively roughens the surface of the polyurethane pad and increases the contact area between the pad, wafer, and slurry. Without conditioning, there are less pad areas for slurry transport and decreased rough areas for effective abrasion.

11:30 AM M1.8
EVALUATION OF MECHANICAL AND TRIBOLOGICAL BEHAVIOR, AND SURFACE CHARACTERISTICS OF CMP PADS. A.K. Sikder, I.M. Irfan, Ashok Kumar, S. Ostapenko and J. Mark Anthony Center for Microelectronics Research, College of Engineering, University of South Florida, Tampa, FL.

In spite of being a historically ancient technology, chemical mechanical planarization (CMP) has attracted enormous of attention recently because of its applicability in planarizing the dielectrics and metal films used in the silicon integrated circuit fabrication. Continued miniaturization of the device dimensions and the related need to interconnect an increasing number of devices on a chip have led to building multilevel interconnection on planarized levels. In CMP very thin materials ($\leq$5 μm) has to be removed very precisely maintaining the precise control on the remaining thickness. Because CMP occurs at an atomic level at the slurry/wafer interface, slurries and pads play a critical role in the successful implementation of this process. Surface roughness, elastic and viscoelastic properties, thickness, pore sizes play important role in this process. Unfortunately mechanical properties of polyurethane polishing pads used in CMP are poorly understood. In this study we have studied the mechanical properties and surface morphology of CMP pads using the state-of-the-art nano-indentation technique along with tapping mode atomic force microscopy. Elastic, viscoelastic, modulus and hardness, and surface roughness have been evaluated. Tribological properties of the pad has been evaluated using Universal Micro-Tribometer. Direct correlation between pad properties and polish performance is not yet clear. Attempt has been made to correlate the properties and performance of the pads.

11:45 AM M1.9
A TECHNIQUE FOR ENGINEERING THE PLANARIZATION PROPERTIES OF A CMP POLISHING PAD. Peter Renteln, Lam Research Corp., Fremont CA; Brian Lombardo, Madison CMP, Wilmington, DE.

In CMP, long-range planarization - planarization occurring over a lateral distance of greater than, say, 400 microns - is controlled primarily by the mechanical properties of the polishing pad, i.e. thickness and stiffness. One measurement of long range planarization can be made by polishing structures of graded lateral dimension and fixed step height. When the wafer is polished, the remaining normalized step height can be plotted as a function of feature size. Doing so results in a sigmoidal shaped curve transitioning from zero (perfect planarity) to unity (zero planarity). We describe the planarization length "L" as the distance at which the curve crosses 0.5 and "S" as the standard deviation of the gaussian which is the derivative of the sigmoid. While longer planarization length is generally desirable and easily achievable, a large S often results in too much planarization, where the ultimate planarity of the silicon substrate is challenged, and an undesirable effect known as "cottage cheese" occurs as the polisher planarizes the silicon substrate itself. Decreasing L can eliminate this effect, but only at the expense of long range planarity, a desirable output. The challenge, therefore, is to engineer a polishing pad with a long L but a very short S. This can be achieved by cutting grooves into the surface of the polishing pads, effectively decoupling L from S. By cutting the grooves in such a way so as to create islands on the pad surface, these features serve to create a planarization length on the order of and limited to the island size, i.e. causing S to be very small. By changing the size of the islands, L and S can be engineered to achieve optimal planarization for the given structure to be planarized and quality of silicon substrate available. Planarization results are presented to show the effect of actively engineered planarization pads, and how the groove pattern can be optimized for a given planarity requirement and substrate quality. The results are followed by a discussion of the expected vs. the achieved results.

SESSION M2: CMP ABRASIVES I / CMP ABRASIVES II

Chairs: Kenneth C. Cadien and Rajeev Bajaj
Wednesday Afternoon, April 18, 2001
Golden Gate A1 (Marriott)

1:30 PM *M2.1
PREPARATION AND EVALUATION OF CHEMICALLY MODIFIED ABRASIVES FOR CMP. R. Partch, N. Barney, H-Y. Wang, K. Griffiths and A. Babel, Clarkson University, Dept of Chemistry, Center for Advanced Materials Processing, Potsdam, NY.

Abrasive particle size, shape and composition in CMP slurries are known to be among several variables that control polishing rate and generation of defects during wafer planarization. In order to meet next generation standards, particle sizes are being reduced and composition used to control abrasive hardness and provide selectivity in polishing different wafer surfaces. In recent years advances have been made in technologies for surface functionalization and coating of many types of particulate matter. That expertise is now being applied to the preparation of powders for use in CMP. Presented in this paper will be methods developed by the authors to selectively improve for use in CMP slurries the surface of several micro and nano sized metal oxide particles. The treatments include coating individual cores with a continuous shell of inorganic or organic material; or, covalent attachment of chemical functionalities on the core surfaces capable of imparting chemistry at the point of contact between the particle and the wafer. Preliminary polishing data using the described treated abrasives will be discussed.

2:00 PM *M2.2
AN EVALUATION ON THE EFFECTS OF NEWLY DESIGNED ABRASIVES IN CMP SLURRY. Nobuo Kawahashi and Masayuki Hattori, JSR Corporation, Fine Electronic Research Laboratory, Yokkaichi, JAPAN.

Newly designed abrasives with various particle morphology and components have been prepared and evaluated in terms of CMP polish efficiency. Polymer spheres with uniformed particle size and special functional groups were prepared by soap-free emulsion polymerization. CMP slurries with these polymer abrasives indicated characteristics such as dishing, erosion and low defectivety for metal and dielectric surfaces. This study has also been conducted with a preparation of composite particles consisting of a polymer core covered with inorganic composition such as zirconium compound, titanium compound, SiO_2, Al_2O_3, etc. The controlled hydrolysis and hetero-coagulation systems were proposed as preparation methods of composite particles. The thickness, morphology and state of the deposited layer could be altered by adjusting concentrations of the reactant and nucleus of metal compounds, pH of the aqueous solution, aging temperature, silane coupling agents, etc. These composite particles were particularly useful in preventing scratching of low-k dielectric material surfaces during a CMP process.

2:30 PM M2.3
CMP OF COPPER: EVOLUTION OF A SLURRY. Witold Paw, Jon Wolk, George Emond, Intersurface Dynamics, Inc., Bethel, CT.

The presentation describes the evolutionary steps taken in the development of a single step Cu CMP slurry/oxidizer formulation. Descriptions range from procedures for screening chemical components to analysis used in final optimization of a commercial product to process simulation on a CMP polisher. Emphasis is on the relatively complex interplay of slurry/oxidizer/metal components. This is studied using instrumental methods of chemical analysis including UV/Vis and FTIR spectrophotometry, pH/conductivity measurements, ICP-OES elemental analysis, ion exchange chromatography and DC electrochemistry. Information includes insights on surface chemistry of metal oxide abrasives and how it effects metal removal, complexation of metal ions in aqueous mixtures, issues of galvanic interaction between Cu and barrier materials and to what extent pattern density becomes a factor. A comparison of laboratory results with process simulation on a CMP polisher is shown with data including performance metrics such as removal rates, dishing, erosion, and thinning.

2:45 PM M2.4
HIGH PERFORMANCE CMP SLURRY WITH INORGANIC/RESIN ABRASIVE FOR Al/LOW k DAMASCENE. Hiroyuki Yano, Yukiteru Matsui, Gaku Minamihaba, Toshiba Corporation, Semiconductor Company, Yokohama, JAPAN; Nobuo Kawahashi, Masayuki Hattori, JSR Corporation, Fine Electronic Research Laboratories, Yokkaichi, JAPAN.

Damascene is an attractive wiring method for process simplification and yield enhancement. But CMP still has many issues like scratch, planarity and corrosion. Meanwhile low dielectric constant (low k) material is going to be introduced as the interlayer dielectrics (ILD) to improve device performance. However, the lack of the mechanical strength of low k material increases concerns like scratch and planarity. So, a new concept is introduced to the CMP slurry abrasive. The new abrasive is composed of resin particle coated with inorganic particles. The unique characteristics of Inorganic/Resin abrasive mainly come from the elasticity of the resin. The soft resin particle behaves as a cushion and prevents the scratch caused by agglomerated inorganic particles and foreign material. The springy feature of the resin particle increases the selectivity of removal rate at convex portions and concave portions. Furthermore, the pressure is loaded to the Al film surface effectively through the resin particle and higher CMP rate can be achieved even without chemicals like oxidizers. This chemical free polishing would be the advantageous in preventing the corrosion of Al.
In this paper, the polishing mechanism of Inorganic/Resin abrasive and the results of Al/Low k Damascene will be presented.

3:30 PM M2.5
OXIDE POWDERS FOR CMP PRODUCED BY CHEMICAL VAPOR SYNTHESIS. Hermann Sieger, Markus Winterer, Horst Hahn, Darmstadt University of Technology, Materials Science Department, Thin Films Division, Darmstadt, GERMANY.

Ultra-fine, non-agglomerated oxide powders are produced by chemical vapor synthesis (CVS). In the CVS process volatile metalorganic precursors are decomposed in a hot wall reactor with a well defined reaction zone at reduced pressures forming nano-sized powders with a narrow size distribution. An inherent advantage is the modular design of the gas flow reactor which enables the production of mixed, doped and coated silica powders with improved volume and surface properties, e.g. isoelectric point, zeta potential, hardness, chemical reactivity or dispersability. In order to correlate CVS product characteristics with CMP performance, powders are investigated by nitrogen adsorption, TEM, XRD, aqueous dispersions by zeta potential and size measurements and polished surfaces by HRSEM and AFM.

3:45 PM M2.6
SILICA ABRASIVES IN POLISHING APPLICATIONS. S.D. Hellring, C.P. McCann, PPG Industries, Inc., Pittsburgh, PA; S.V. Babu, S. Narayanan, Clarkson University, Department of Chemical Engineering and Center for Advanced Material Processing, Potsdam, NY.

Slurries containing silica abrasive produced by varying processes are compared for polishing performance. The relationship between the physical and chemical character of silica and polishing performance with copper, tantalum, and oxide were examined. The effects of morphological parameters and surface chemistry on removal rates, selectivity, stability, and post-polishing cleaning will be discussed.

4:00 PM *M2.7
SYNTHESIS OF ALUMINA SLURRIES FOR DAMASCENE PATTERNING OF COPPER. Byung-Chan Lee, David J. Duquette, Ronald J. Gutmann, Rensselaer Polytechnic Institute, Center for Integrated Electronics and Electronics Manufacturing, Troy, NY.

Model alumina slurries have been synthesized using fundamental electrochemical concepts and surfactant additives, along with characterization of blanket copper wafers after chemical-mechanical planarization (CMP) processing. A model slurry was established containing 3 wt% alumina (50 nm nominal size), 2 wt% potassium dichromate and 1 vol% DOWFAX 2AO, as abrasive, oxidizer and anionic surfactant, respectively, which resulted in copper removal rates of 120 nm/min with smooth, low-particulate defect density surfaces without aggressive post-CMP cleaning. When used with a model silica-abrasive to remove the Ta liner, well-defined damascene-patterned structures were achieved with low-particulate defect densities. The principal techniques used in developing the model alumina slurry include the following: open circuit potential measurement, potentiodynamic polarization, capillary hydrodynamic fractionation (CHDF) particle size analysis, surface tension measurement, and zeta-potential measurement. The paper will include variations obtained with alternative alumina abrasives, alternative oxidizers and alternative surfactants to illustrate the synthesizing principles. The use of this approach in developing a slurry for the Ta liner will also be described.

4:30 PM M2.8
THE EFFECTS OF ADDITIVES IN IODINE BASED SLURRY ON COPPER CHEMICAL MECHANICAL POLISHING. Seung-Mahn Lee, Zhan Chen, and Rajiv K. Singh, Department of MS&E and Engineering Research Center for Particle Science and Technology, University of Florida, Gainesville, FL.

Copper CMP has now been recognized and accepted as the process that is capable of providing the planarity to build multilevel interconnects schemes with below quarter-micron lines. One of the key issues in copper CMP is the development of slurries which can provide high removal rates, good planarity and high selectivity. In our previous presentation, the possibility of the use of iodine slurry for copper CMP was introduced. Iodine slurry showed the highest removal rate and relatively good surface quality. In this presentation, we have investigated the effects of additives in iodine slurry in order to control the removal rate of copper and surface quality. Since BTA and SAS-60 are well known inhibitor and surfactant for copper, respectively, both additives can be used to retard the surface reaction rate and dissolution rate of copper and to enhance the surface quality. From the results, it is observed that CuI-BTA layer is formed uniformly on the surface, which protect the further corrosion of copper. In addition, surfactants were very effective to control the removal rate and surface quality. Then, for better understanding of the high removal rate of copper in iodine based slurry, friction force measurements and nano-scratch tests in solutions were conducted. These results were compared to hydrogen peroxide based slurry.

4:45 PM M2.9
SELF-ASSEMBLED SURFACTANT MEDIATED DISPERSION OF NANOPARTICULATE SYSTEMS FOR CHEMICAL MECHANICAL POLISHING (CMP). Pankaj K. Singh, Joshua J. Adler, Bahar Basim, Yakov I. Rabinovich, and Brij M. Moudgil, Department of Materials Science and Engineering and Engineering Research Center for Particle Science and Technology, University of Florida, Gainesville, FL.

The current interest in using different types of ultrafine (nanosized) powders for Chemical mechanical Polishing (CMP) under severe conditions such as high salt, chemical additives, and high pressure, puts a high demand on suspension processing. Traditional dispersing methods such as electrostatics and polymeric dispersants may not perform adequately under the conditions encountered in CMP. Surfactant solutions can provide a feasible alternative for stabilization

of ultrafine particles. The barrier to aggregation in presence of surfactants was measured using atomic force microscopy and the barrier heights were correlated to suspension stability. It was found that the barrier was several orders of magnitude higher in presence of micelle-like self-assembled surfactant aggregates, as compared to barrier expected from electrostatic interactions. The results indicate the presence of steric barrier due to the adsorbed micelles on the surface, the strength of the barrier increasing with increasing strength or compactness of the adsorbed micelle. The origin of these forces was explored through techniques such as adsorption, contact angle, zeta potential, and polarized Attenuated Total Reflection Fourier-Transform Infra-Red Spectroscopy (ATR-FTIR). In previous studies, unstable slurries were observed to create significant surface deformation during silica CMP. Polishing was carried out using cationic surfactant stabilized silica slurries to enhance the surface quality while maintaining a reasonable material removal rate. The effect of particle size and polishing pressure was also examined.

SESSION M3: COPPER CMP / STI AND PLANARIZATION I

Chairs: James G. Ryan and Ronald J. Gutmann
Thursday Morning, April 19, 2001
Golden Gate A1 (Marriott)

8:30 AM *M3.1

INTERPLAY BETWEEN COPPER ELECTROPLATING AND CHEMICAL MECHANICAL PLANARIZATION. Akihisa Hongo, Yusuke Chikamori, Tatsuya Kohama, Koji Mishima, Norio Kimura, Ebara Corporation, Fujisawa, JAPAN; David K. Watts, Ebara Technologies, Inc., San Jose, CA.

The introduction of Chemical Mechanical Polishing (CMP) into semiconductor device processing brought a significant need for wet chemistry research and development in this industry. With the transition from aluminum to copper for advanced interconnect metallization came a tremendous amount of electrochemical research towards developing a production worthy copper CMP process capable of meeting the stringent specifications of dual damascene integration. In addition, the dual damascene integration scheme introduced copper deposition challenges that brought significant activity in developing another wet chemistry process, electroplating. These two sequential, chemical processes have been shown to have significant interaction that has created significant challenges in process integration. We present here some of the copper electroplating and copper CMP results from development efforts at Ebara that highlight the process integration challenges between these two processes. For example, a non-uniform copper clearing pattern observed during copper CMP can be compensated for in the CMP process but may be indicative of non-uniform deposition, or demonstrate the need for a post deposition anneal that gives a more uniform distribution of copper microstructure across the wafer. Compositional changes to copper electroplating bath chemistry can achieve high aspect ratio, 'bottom-up' trench fill, but can present local, pattern dependant, challenges for copper CMP. Critical issues between these two processes, such as global uniformity, local morphology variation, post CMP voids or pits, or transient changes in copper structural and compositional properties, will be presented and discussed.

9:00 AM M3.2

EFFECT OF COPPER FILM SURFACE PROPERTIES ON CMP REMOVAL RATE. Yuchun Wang, Rajeev Bajaj, Gary Lam, Yezdi Dordo, Doyle Bennet, Fritz Redeker, Applied Materials, CMP Division, Cu KPU, Santa Clara, CA.

It has been observed that CMP (chemical mechanical polishing) removal rate of copper varies for films from different sources. While the film hardness and their wet static etch rate in absence of inhibitor are similar, the static etch rate in presence of inhibitor are significantly different. Analysis by AFM, XPS, and ion beam sputtering showed the film roughness and surface composition are different within the range of 160 angstroms deep. The different CMP removal rates are synergistic effect of copper film roughness (grain size), surface composition, and effective adsorption of inhibitor. Once polishing is initiated by an aggressive polishing step, removal rate of the remaining copper films becomes less different. Based on these findings, the polishing slurry and process were further optimized.

9:15 AM M3.3

COPPER CMP FOR DUAL DAMASCENE TECHNOLOGY: SOME CONSIDERATIONS ON THE MECHANISM OF Cu REMOVAL. David Wei, John M. Boyd, Hugh Li, Yehiel Gotkis, Stephen Jew, Joseph Li, K.Y. Ramanujam, and Rodney Kistler, Lam Research Corporation, Fremont, CA.

Copper Dual Damascene (Cu2D) technology becomes the process of choice in semiconductor manufacturing. The Cu2D sequence includes multiple use of CMP both for dielectric planarization and for shaping plugs and wires. The Cu-CMP function is to remove the overburden materials leaving the wafer surface as flat as possible. The planarization task in Cu-CMP is more challenging than in other CMP processes due to larger topography variations, and it has to be accomplished twice: while dealing with incoming topography, and while polishing heterogeneous surface during barrier removal. Electroplating additives adsorbed at the grain surface affect the intergrain binding forces, layer properties and CMP response, causing coordinate, pattern and feature size sensitivity. Typically Cu-CMP process is multi-step/multi-consumable. High planarization efficiency and absence of the intergrain boundary damage is a critical requirement and it is directly linked to the Cu/slurry interaction mechanism. Fast formation of passivating surface films prevents Cu from direct chemical dissolution, converting a chemically driven process into a pseudo-mechanical one with high planarization capability and self-inhibiting action, minimizing the intergrain boundary damage. Normally, H2O2 is added as oxidizer to the Cu-CMP slurries. The H2O2 concentration determines the mechanical and chemical properties of surface oxide species and as a result the all aspects of the CMP-process. In this study the effect of H2O2 concentration on Cu removal rate and the types of surface films formed were investigated and Cu removal mechanisms discussed. It was found that Cu removal rate is extremely low in the absence of H2O2, it increases up to 4800 A/min with the increase of H2O2, and then decreases again. The values of open circuit potential plotted in the Eh-pH diagram clearly show that the surface Cu2O is formed at lower H2O2 concentration and CuO at higher ones. The formation of different Cu-oxides was confirmed by XPS analyses.

9:30 AM M3.4

SURFACE PASSIVATION DURING CHEMICAL-MECHANICAL POLISHING OF COPPER USING XPS. Sudipta Seal[a], Vimal Desaia, Ying Lia and S.V. Babua. [a]Advanced Materials Processing and Analysis Center and Mechanical, Materials and Aerospace Engineering University of Central Florida, Departments of Mechanical and Chemical Engineering Center for Advanced Materials Processing Clarkson University, Potsdam, NY.

Chemical-mechanical polishing (CMP) has become an essential step in semiconductor manufacturing. Copper CMP is complicated by the changing nature of Cu surface in different chemical environments. Understanding of the dissolution-passivation behavior is especially important in identifying the polishing mechanism and minimizing polishing defects in Cu CMP, Depending on the chemical environment, Cu is either directly dissolved or passivated. The formation of a passive layer on the Cu surface is desirable since it can protect the recessed features from being chemically etched while the passive film formed on the protruding features is removed during polishing. Our previous work proposed different mechanisms for Cu polishing in the presence of different oxidizers, namely, Fe(NO3)3, H2O2, H2O2/glycine, and KIO3. Except for the polishing in Fe(NO3)3 based slurry, the removal of Cu is presumably due to the removal of the passive layer formed, such as Cu2O, CuO, and Cu(IO3)2. However, knowledge of these passive layers is very poor. In this work, X-ray photoelectron spectroscopy (XPS) and Auger Photoelectron Spectroscopy (AES) is used to identify the structure, chemistry and composition of the surface passive layer formed in the presence of H2O2, H2O2/glycine, and KIO3, etc. The effect of the chemical concentration and pH on the surface passivation of Cu will be investigated and the results will be related to the polishing mechanism.

9:45 AM M3.5

ANALYSIS OF COPPER TO TANTALUM TRANSITION IN COPPER CMP. J.M. Kang, Shaoyu Wu, T. Selvaraj, and P.D. Foo, Institute of Microelectronics, DSIC-MD Department, SINGAPORE.

The evolution from Cu to Ta surface during Cu CMP has been investigated. As a first step of Cu CMP, removing excess Cu on field area to Ta often gives rise to topography issues such as dishing or erosion. The exposure of Ta is detected by in-situ reflectance measurement, where the downward slope-start signifies the start of Ta exposure. For blanket wafers, the maximum remaining Cu thickness at slope-start increases with initial Cu thickness. Applying lower polishing pressure and table speed, so-called soft landing, near the Cu-Ta transition stage results in thicker remaining Cu. In patterned wafers, Ta exposure starts near high pattern density areas such as wide lines. By this, contrary to blanket wafers, remaining Cu thickness at slope-start cannot be correlated simply with initial Cu thickness. In this experiment, with increasing initial Cu thickness, remaining Cu thickness at slope-start decreased. The amount of dishing is largely proportional to the initial Cu thickness. Applying soft landing results in thicker remaining Cu than polishing without soft landing as in blanket wafers. However, polishing without soft landing gives more dishing. Total-indicated-range (maximum remaining Cu thickness

maximum dishing on 100 μm trench) after first step ranges from 826 to 1457 Å according to the initial Cu thickness, over polishing and whether soft landing has been applied or not.

10:30 AM *M3.6

ANALYSIS OF CMP PLANALIZATION PERFORMANCE FOR STI PROCESS. Manabu Tsujimura, Ebara Corporation, Tokyo, JAPAN; Masanori Matsuo, Hirokuni Hiyama, Ebara Resarch Co., Tokyo, JAPAN; Masahiro Ota, Tokyo Metropolitan University, Tokyo, JAPAN.

CMP has now been adopted not only for ILD and W-plug, but also for Cu metal and STI. In the STI CMP process, the wafer has some defined waviness, and it has recently been reported that this waviness may affect the STI CMP yield. The principle purpose of CMP is to planarize relatively large rather than relatively small topography. Therefore, there may be a range of wafer topography in which the STI pattern may be overpolished, depending on its peak-to-valley and frequency. The range and dishing performance of STI are calculated based on step height performance, which is in turn calculated by FEM. In this analysis, CMP is defined as four types of regions. The first is known as the "step height region." In this region, the planarization performance of step height reduction is required. The second is referred to as the "uniform material region." In this region, uniform polish is requied. The third region is known as the "non-uniform material region." In this region, the planarization perfomance of dishing and erosion reduction is required. The fourth region is known as the "substrate region." In this region, defect reduction is required. The allowable peak-to-valley value and its frequency are calculated by determining whether the difference in polish quantites between the peak and vallay is less than allowable values such as 10 nm, 20 nm, and 30 nm. It has also been reported that slurry selectivity can decrease this effect, together with disadvantage.

11:00 AM M3.7

A STUDY ON STI AND DAMASCENE CMP USING CHIP LEVEL SIMULATION. Kyung-Hyun Kim, Yoo-Hyun Kim, Chang-Ki Hong, Moon-Hyun Yoo, Jeong-Lim Nam, Jeong-Taek Kong and Sang-In Lee, Semiconductor R&D Center, Samsung Electronics Co. Ltd., Kiheung-Eup, Yongin-Si, Kyungki-Do, KOREA.

Modeling and simulation of Chemical Mechanical Polishing (CMP) are essential not also for understanding the physical mechanisms, but also for optimizing the process integration. Notwithstanding the prevalence of data regarding the pattern dependency of the CMP rate for a single material, e.g., an oxide film, that for dual type of materials can be more complicated. The dearth of knowledge of the the effective polish rate in patterned regions and the effect of slurry selectivity on pattern erosion in a CMP of STI/damascene structure, for instance, raises the level of complexity in both the modeling and the numerical analysis based - chip level simulation. In this work, we present a methodology that describes the effective polish rate of pattern area in STI/W-Damascene CMP process, and show that the above method can be used to predict the pattern erosion under various process related factors, such as slurry selectivity, pattern density, and over-CMP Using the model above, we have developed a CMP simulator to calculate the chip planarity after STI and Damascene CMP in chip level. The simulator can automatically calculate the local pattern density of unit cell of size about $10\times10\mu$m from the mask e-beam file, and generate the effective pattern density distribution of chip level using a pattern bias factor and a planarization length. The pattern bias factor was introduced to represent the effects of gap-filled materials on planarity, and the planarization length was introduced to represent the effects of CMP process conditions and consumables on planarity. Using the above simulator, the effect of reverse etchback, gapfill oxide, deposition thickness, slurry selectivity, and over-CMP on chip planarity can be sucessfully predicted. We have verified the developed simulator on STI / Damascene layer of DRAM, SRAM and logic devices. The calculated data are in good agreement with experimental data less than 5% error range.

11:15 AM *M3.8

CONTINUING INVESTIGATIONS INTO THE PECULIARITIES OF CMP USING CERIA-BASED SLURRIES. David J. Stein and Dale L. Hetherington, Sandia National Laboratories, Albuquerque, NM; Michael R. Oliver, Rodel, Inc., Newark, DE.

Previous work has discussed a novel ILD deposition technique which, when used with an experimental ceria-based slurry, produces a self-stopping CMP process that minimizes pattern density effects. Specifically, the ILD deposition process involves varying the silicon content of the film as a function of film thickness. The ILD polish rate using the experimental slurry is an inverse function of the silicon content of the film. Thus, if a low silicon content film is deposited on top of a high silicon content film (which is deposited directly on the metal), the high silicon content film will act as a stop layer for the CMP process. Specific data that was presented included the polish rate of these films using both an the experimental ceria-based slurry and a standard fumed silica CMP slurry. Other data showed the chemical differences between the various ILD films, the wettability of the films before and after CMP, and nano-indentation studies of the ILD films. Ceria particles of various sizes and iso-electric points were investigated using both the silicon-rich films described above and thermally grown silicon dioxide films. The drastic differences in polish rate were found to be not only a function of the silicon content of the oxide but also the iso-electric point of the ceria particles and the pH of the slurry. The secondary particle size was also found to have an effect. Polish rate data will be presented. Friction and adhesion measurements between ceria and silica particles and various oxide surfaces and pad materials obtained from in-situ lateral and adhesive atomic force microscopy experiments will also be presented and discussed.

11:45 AM M3.9

CHARACTERIZATION AND CONTROL OF COPPER CMP WITH OPTOACOUSTIC METROLOGY. Michael Gostein, Michael Joffe, Alex A. Maznev, Philips Analytical, Natick, MA; Paul Lefevre, International SEMATECH, Austin, TX.

The silicon IC industry is rapidly moving to adopt copper as the material of choice for circuit interconnects. Because of the lack of etching processes to remove copper, these interconnects must be patterned with a Damascene process, in which copper is deposited over a film with trenches etched in an insulator material and the excess copper is then removed with chemical-mechanical polishing (CMP). The challenge for developers of copper CMP processes is to obtain a process that polishes uniformly across 200-300 mm silicon wafers, minimizes copper dishing and dielectric erosion, and polishes uniformly on structures with widely varying density of copper-filled trenches. Optoacoustic metrology provides a valuable tool for CMP process development and control, by enabling rapid, non-destructive measurement of copper film thickness on both blanket and patterned films. Unlike profilometry, which measures only surface topography, the optoacoustic technique measures metal thickness. It can be used at all stages of polishing, from measuring the uniformity of wafers prior to polish, measuring removal rates at intermediate polishing stages, and measuring final post-polish thickness of test pads and arrays of submicron trenches. In this presentation, we will demonstrate that optoacoustic measurements provide unique process characterization data, e.g. determination of planarization length and measurement of remaining film at intermediate stages of polishing. The rapid ($\sim$1 second per site), non-contact measurement is also ideally suited for in-line control of within-wafer and wafer-to-wafer uniformity of the CMP process.

SESSION M4: STI AND PLANARIZATION II / WEAR RATE MODELS

Chairs: Hiroyuki Yano and Nobuo Kawahashi
Thursday Afternoon, April 19, 2001
Golden Gate A1 (Marriott)

1:30 PM *M4.1

FIXED ABRASIVE TECHNOLOGY FOR STI CMP ON A WEB FORMAT TOOL. Laertis Economikos, IBM Microelectronics, Semiconductor R&D Center, Hopewell Junction, NY; Alexander Simpson, Infineon Technologies, Hopewell Junction, NY.

Shallow trench isolation (STI), requires a high quality oxide with superior fill capability provided by High Density Plasma (HDP). Unfortunately, HDP creates large topographies within a die that are difficult to polish directly using conventional silica slurries. Therefore, etch back integration schemes have been employed for STI polish. Fixed abrasive pads allow direct STI polish with outstanding planarization efficiency and process stability without prior etch-back. The planarization efficiency is also highly dependent on the shape of the pad's small composites that hold the mineral. Fixed abrasive pads with pyramid and pole shapes were tested. The pad with adequately spaced pole shaped composites, provided better planarity compared to pyramid composites that were spaced very closely. The basic polishing characteristics of 3M's fixed abrasive pad such as: planarization length and the effect of the subpad to planarity, selectivity to topography, dishing and nitride erosion are presented. Fixed abrasive polish has high selectivity to topography and very low dishing of the down areas. These characteristics allow one to fill the STI with very little overfill which in turn reduces the HDP fill cost. Furthermore, it allows polishing of structures with very large topography steps. Its self-stopping characteristic upon planarization can be used to develop processes with no stopping layer (blind stop). However, it defines the limitation of the fixed abrasive process to combinations of designs and fill techniques that result in less than 200A of overfill.

2:00 PM M4.2

MODELING OF FEATURE-SCALE PLANARIZATION IN STI

CMP USING MESA^{TM}. Thomas Laursen, Inki Kim, Jim Schlueter, SpeedFam-IPEC Incorporated, Chandler, AZ; Scott Runnels, Scott Runnels Consulting, San Antonio, TX.

MESA is a feature-scale planarization model developed by SpeedFam-IPEC (SFI), in conjunction with Southwest Research Institute, for describing the chemical mechanical polishing (CMP) process used in IC manufacturing. This model has previously been applied to the polish of inter-level dielectrics and copper CMP. The present study is part of an experimental validation for shallow trench isolation (STI). This study was carried out on the SFI Auriga polisher, using SKW Associates 200-mm wafers (SKW3 MIT-STI-mask), Rodel IC 1000/1400 pads and Cabot SS-12 slurry. MESA accounts for observed differences in planarization using Rodel IC1000 with and without foam backing as well as the pattern-density (PD) dependence within each die. The data were obtained and plotted in such a way that the active-area (AA) and trench-oxide (TO) levels are displayed throughout the whole polish, including the points where the AA clears to nitride and silicon as well as where the TO dishes below the silicon level. The PD effect is evident in both cases, and a comparison between the two pads shows less PD effect and improved planarization with the single IC 1000 pad. MESA has been shown to predict the details of the topographical evolution for STI CMP on the feature scale. When validated by fitting the pad constants, k1 and k2, to describe the planarization, MESA is expected to provide accurate predictions for the polish of any oxide pattern structure as long as the same CMP process is used.

2:15 PM M4.3
MODELING OF PATTERN DEPENDENCIES IN MULTI-LEVEL COPPER CHEMICAL-MECHANICAL POLISHING PROCESSES. Tamba E. Tugbawa, Tae H. Park, Duane S. Boning, Microsystems Technology Laboratories, MIT, Cambridge, MA; Paul Lefevre, SEMATECH, Austin, TX; Lawrence Camilletti, Conexant Systems, Newport Beach, CA.

Chemical mechanical polishing (CMP) has become a necessary processing step in fabricating multi-level copper interconnects. Copper CMP is recognized to suffer from pattern dependent problems such as dishing and erosion, which cause increased line resistance and non-uniformity within the die, for a given metal level. The non-uniformity on metal level one that is caused by the post CMP dishing and erosion on that level, manifests itself as non-uniformity in the electroplated copper thickness on metal level two. In addition, the typical plating process also causes wafer-scale, array-scale and feature-scale copper thickness non-uniformity. The combined non-uniformity on metal level two can thus be considerable and could lead to complicated dishing and erosion after CMP on metal level two. This will degrade the attainable planarity on higher metal levels, and will certainly cause integration and manufacturing problems. Predictive pattern dependent models of copper CMP processes are therefore highly desirable for use in optimization of a manufacturing flow, as well as for developing interconnect design rules, among other things. We have developed a mathematical model that predicts the post CMP pattern dependent thickness in multi-level copper CMP. The model is an extension of our earlier model for single level copper CMP processes [1]. It is built on the premise that copper CMP processes are chemically- enhanced mechanical processes, and it views copper CMP processes as comprising of three intrinsic stages: bulk copper removal, barrier removal, and overpolish stage. The model takes into account the initial long-range electroplated copper topography, the effective pattern density, and the initial local step-heights within the arrays. [1]. T. Tugbawa et al., CMP Symposium, Electrochemical Society Meeting, Honolulu, HA, October 1999.

2:30 PM M4.4
DIRECT MEASUREMENT OF PLANARIZATION LENGTH FOR COPPER CHEMICAL-MECHANICAL POLISHING PROCESSES USING A LARGE PATTERN TEST MASK. Tamba Tugbawa, Tae Park, Duane Boning, Microsystems Technology Laboratories, MIT, Cambridge, MA; Paul Lefevre, Albert Gonzales, Tom Brown, SEMATECH, Austin, TX; Michael Gostein, Philips Analytical, Natick, MA; John Nguyen, Speedfam-IPEC, Phoenix, AZ.

Planarization length is a very important parameter in CMP, as it succintly summarizes the planarization capability of a given polishing process. In copper CMP, the planarization length tells us the extent to which a CMP process can planarize the electroplated copper topography during the overburden copper polishing stage. The larger the planarization length, the better the planarization capability of the process in question, and the more uniform will be the polishing across different densities within the die. There is currently no simple formula which one can use to determine the planarization length for a given process. Instead one must resort to experimentation with the use of specially designed patterned wafers, followed by extraction of the planarization length through numerical fitting of measured data to a pattern density based CMP model. In this work, we describe a simplified methodology for direct measurement of the planarization length. This methodology is an extension of that used by Steve Hymes [1], and it includes a model that explains the polishing behavior. A new test mask that contains square trenches of dimensions ranging from 1 micron to 25 millimeters has been designed for this work. The design takes into account the wafer-scale non-uniform nature of the CMP process. The mask also contains isolated lines and arrays of lines intended to provide information about the feature-scale dishing and erosion performance of a given copper CMP process. We have used the mask to perform several experiments that show the dependence of planarization length on CMP consumables such as slurry and pad, and on process settings such as down force and relative speed. [1]. S. Hymes et al., CMP Symposium, MRS Spring Meeting, April 1999.

3:15 PM M4.5
A MECHANICAL WEAR MODEL FOR CHEMICAL-MECHANICAL POLISHING PROCESS. Goodarz Ahmadi, Alireza Mazaheri and Xun Xia Department of Mechanical and Aeronautical Engineering Clarkson University, Potsdam, NY.

Abrasive particle-surfaces interactions are studied and the surface removal process by adhesive and abrasive wear mechanisms during chemical-mechanical polishing (CMP) are analyzed. The mechanical contact theory is used and a model for interactions of pad asperities with abrasive particles and wafer is developed. The cases of hard and soft pads and dilute and dense slurries are analyzed. A model for particle-scale surface removal process in the chemical-mechanical polishing is developed. The influence of abrasive particle adhesion to the surface is included in the analysis. Variations of polishing rate with pressure, abrasive particle size, and concentration, as well as pad characteristics (including asperity distribution, and asperity elastic and plastic deformation) are studied. The functional dependence of the polishing rate on pressure and velocity was found to be related to the distribution of pad asperities. The results also show that the abrasive particle adhesion affects the CMP process. The effect of non-sphericity of slurry particles on the CMP performance is also studied.

3:30 PM M4.6
A CONTACT-MECHANICS BASED MODEL FOR DISHING AND EROSION IN CHEMICAL-MECHANICAL POLISHING. Joost J. Vlassak, Harvard University, Division of Engineering and Applied Sciences, Cambridge, MA.

In this presentation, we describe a new model for dishing and erosion during chemical-mechanical polishing. According to the model, dishing and erosion is controlled by the local pressure distribution between features on the wafer and the polishing pad. The model uses a contact mechanics analysis based on the work by Greenwood to evaluate this pressure distribution and it allows us to take the compliance of the pad as well as its roughness into account. Using the model, it is straightforward to evaluate the effect of pattern density, line width, applied down force, selectivity, pad properties etc. on both dishing and erosion. The model can be applied to CMP used for oxide planarization, metal damascene or shallow trench isolation. The model is implemented as an algorithm that quickly calculates the evolution of the profile of a set of features on the wafer during the polishing process. With proper calibration of the selectivities, it can be used as a tool in optimizing the CMP process and implementing CMP design rules.

3:45 PM *M4.7
APPLICATIONS OF THE MODELING BASED ON THE CONTACT PRESSURE ANALYSES FOR CMP PROCESS. Takeshi Nishioka, Toshiba Corp., Corporate R&D Center, Kawasaki, JAPAN; Yoshikuni Tateyama, Naoto Miyashita, Hiroyuki Yano, Toshiba Corp., Semiconductor Company, Yokohama, JAPAN.

Chemical mechanical polishing is an essential process for achieving a high degree of planarization. The planarity after CMP sensitively depends on the pattern scales, the pattern densities, the mechanical properties of polishing pads and the polishing process properties. In order to simulate the topography after CMP, a numerical model with the pad surface soft layer had been proposed. The model should be very useful not only for the topography simulation, but also for the development and the evaluation of new process, i.e. new slurry and new polishing pads. Based on the good agreement between the numerical model and the physical model, its applications for oxide CMP and metal CMP will be presented in this paper. Application for the ceria based slurry process, which has a non-linear pressure dependence of the polishing rate and a self-stopping property, and application for the metal CMP with high selectivity will be discussed.

4:15 PM M4.8
MODELING THE EFFECTS OF POLISHING PRESSURE AND SPEED ON CMP RATES. Ed Paul, Stockton College, Pomona, NJ.

In a previous CMP model, the effects of both chemical and abrasive slurry concentrations on the polishing rate were quantitatively explained, for constant polishing pressure and velocity. That model is extended here to consider specific descriptions of mechanical abrasion, including Preston and non-Preston expressions. Predictions of behavior are compared to literature data, leading to an improved understanding of the abrasive process in CMP.

4:30 PM M4.9
WAFER NANOTOPOGRAPHY EFFECTS ON CMP: EXPERIMENTAL VALIDATION OF MODELING METHODS. Brian Lee, Duane Boning, Massachusetts Institute of Technology, Dept of Electrical Engineering, Cambridge, MA; Winthrop Baylies, BayTech Group, Weston, MA; Noel Poduje, Pat Hester, ADE Corporation, Westwood, MA; John Valley, Chris Koliopoulos, ADE Phase-Shift, Tucson, AZ; Dale Hetherington, Sandia National Laboratories, Albuquerque, NM; HongJiang Sun, Philips Semiconductor, Albuquerque, NM; Michael Lacy, Lam Research, Fremont, CA.

Nanotopography refers to 10-100nm surface height variations that exist on a lateral millimeter length scale on unpatterned silicon wafers. Chemical mechanical polishing (CMP) of deposited or grown films (e.g. oxide or nitride) on such wafers can generate undesirable film thinning which can be of substantial concern in shallow trench isolation manufacturability. Proper simulation of the effect of nanotopography on post-CMP film thickness is needed to help in the measurement, analysis, diagnosis, and correction of potential problems. Our previous work has focused on modeling approaches that seek to capture the thinning and post-CMP film thickness variation that results from nanotopography. Analysis has been performed using a density and step-height based CMP model, as well as a contact mechanics CMP model. The importance of relative length scale of the CMP process used (planarization length) to the length scale of the nanotopography on the wafer (nanotopography length) has been suggested. In this paper, we report on extensive experiments using sets of 200mm epi wafers with a variety of nanotopography signatures (i.e., different nanotopography lengths). Sets include single-sided and double-sided polished wafers, upon which a 1 micron oxide film is thermally grown. These wafer sets have been polishing using different CMP pads and processes with varying planarization lengths. Additional patterned CMP characterization wafers were included in each wafer set; extracted planarization lengths using these wafers ranged from 1.9mm to nearly 10mm. Experimental results indicate a clear relationship between the relative scales of planarization length vs. nanotopography length: when the planarization length is less than the nanotopography length little thinning occurs; when the CMP process has a larger planarization length, surface height variations are transferred into thin film thickness variations. In addition to presenting these experimental results, modeling of the nanotopography effect on dielectric CMP processes will be reviewed, and measurement data from the experiments will be compared to model predictions.

4:45 PM M4.10
SLURRY RETENTION AND TRANSPORT DURING CHEMICAL-MECHANICAL POLISHING OF COPPER. Ying Li, Satish Narayananb, S.V. Babu, Depts of Mechanical and Chemical Engineering, Center For Advanced Materials Processing, Clarkson University, Potsdam, NY.

Although significant progress has been made in slurry development and process optimization, one important issue, i.e., the slurry transport between the wafer and the pad during polishing, still needs in-depth investigation. The slurry transport not only affects directly the chemical reactivity of the slurry by influencing the steady state concentration of the various chemicals and abrasives between the pad and the wafer, but also the efficiency of mechanical abrasion of the particles. This work investigates the retention and transport of chemical species and abrasive particles during copper CMP. "Slurry step-flow" experiments, in which the concentration of the chemicals and abrasives in the slurry are altered in a step change during polishing, are conducted with slurries containing different chemicals, such as ferric nitrate, hydrogen peroxide and potassium iodate. Results from these experiments that shed light on the role of abrasives and chemicals during the polishing will be presented.

SESSION M5: POSTER SESSION
Thursday Evening, April 19, 2001
8:00 PM
Salon 1-7 (Marriott)

M5.1
IN SITU LATERAL FORCE MEASUREMENT DURING CHEMICAL MECHANICAL POLISHING. Wonseop Choi, Seung-Mahn Lee, Rajiv K. Singh, Department of MS&E and Engineering Research Center for Particle Science and Technology, University of Florida, Gainesville, FL.

A variety of in-situ measurement techniques were developed in metal and dielectric CMP. However, until now, no in situ technique has been developed to monitor mechanical effects in CMP environment under solid loading conditions and the need to understand the fundamental aspects of the process is also important. In our previous work, the friction force of stationary wafer without solid loading has been studied. In this talk, frictional forces under real CMP conditions with solid loading and rotational wafer have been investigated. An in-situ lateral force measurement apparatus was modified to be suitable for real CMP condition. This technique measures friction force between the surface of the wafer sample and the polishing pad under different solid loading condition. Experiments were done in polishing of silica wafer using silica slurry and polishing of copper wafers using alumina slurry. The friction force measurements, which were conducted as a function of time and process parameters, were correlated with the change in surface characteristics of the polished wafers. Atomic Force Microscopy (AFM), Ellipsometry, and Four-point probe were used to characterize the samples before and after the experiments. The results showed the better understanding of the frictional force mechanism occurring at the wafer-pad interface under different solid loading conditions during CMP.

M5.2
CMP RELATED AND CMP REVEALED SHORT- AND LONG-RANGE INTEGRATION INTERACTIONS IN COPPER DUAL DAMASCENE TECHNOLOGY. Yehiel Gotkis and Rodney Kistler Lam Research Corporation, CMP/CLN Technology Division, Fremont, CA.

More than 3 years passed since IBM made their official announcement on Copper Dual Damascene (Cu2D) technology, drawing the semiconductor world in the Cu2D rush. Nowadays, after more than 3 years of extensive R&D work, the EOL yields are still too low, and a lot of process integration work still has to be done to make it FAB ready. At this phase the key to success is to link the problem to its root cause, which is frequently located at remote operation and it takes more efforts to discover the link than to fix the problem. CMP is one of the most, if not the most, critical yield affecting operation in Cu2D technology. Going through all metal deposits and touching the dielectric, CMP is performing a kind of reversed processing. In this sense it could be considered also as a quality control procedure, capable to reveal problems related to other process steps. Additionally to the known Cu/oxide losses and formal particulate defectivity, other CMP-related or CMP-revealed yield affecting issues are discussed in details: scratching; micro-cracking; corrosion; non-removed residuals; voids and pits; barrier integrity damage; oxide depressions/discolorations. Cu is a very soft material. In addition to slurry agglomerates and tool debris, two new classes of scratchiers, in-situ created flakes and "rolling stones", leading in some cases to extremely repeatable regularly shaped effects, and so-called shallow "chemical" scratches, are discussed. Copper is a polycrystalline material, that is a new challenge for CMP, and micro cracking at the intergrain boundaries is discussed particularly in details. Rough estimation of the number of intergrain separations in a chip per one Cu level leads to a number as high as about one billion. Inter-grain boundaries are extremely mechanically and chemically vulnerable. Shier forces and chemically aggressive CMP media provoke chemistry-assisted inter-grain cracking and stress-induced intergrain corrosion. Inevitably exposure of processed layers to corrosive conditions is inherent part of the CMP game. There are some specific spots of the Cu layer (pin-holes, micro-cracks, true- and pseudo-scratches, inter-grain boundaries, hidden stressed spots, voids, galvanically active spots etc.), demonstrating enhanced vulnerability to corrosion. What should be done to prevent corrosion damage in such conditions? In summary it is concluded that extensive work still has to be done to tune design rules, deposition, annealing and CMP to make the whole Cu2D back-end cluster self-consistent.

M5.3
A PLANARIZATION MODEL IN CHEMICAL MECHANICAL POLISHING OF SILICON OXIDE USING HIGH SELECTIVE CeO_2 SLURRY. JongWon Lee, BoUn Yoon, SangRok Hah and JooTae Moon, Semiconductor R&D Center, Samsung Electronics Co. Ltd., Kyungki-Do, KOREA.

As the design rule of IC device decreases high selective chemical mechanical polishing process for shallow trench isolation formation is becoming important. One of the most promising slurry for high selective CMP is ceria based slurry. However, in the high selective STI CMP process on the real pattern wafer, unexpected increase in polishing time results due to the removal rate drop in patterned area. In this study, mechanism of planarization for the CMP of silicon oxide

using high selective ceria slurry was explored. A comparison study on silica, ceria, and high selective ceria CMP processes was carried out. At the onset of polishing with silica slurry, the removal rate of high active areas are higher than the bulk removal rate. As the surface of oxide becomes planarized, removal rate exponentially decrease and converges to the bulk removal rate. However in the high selective CMP case, the removal rate of silicon oxide in high area is constant and does not dependent on the polishing time. This implies that the oxide polishing rate does not increase on the raised areas for high selective CMP. Polishing behaviors as a function of the solid content of ceria and chemical additive for high selectivity were investigated. Although the removal rate increases with increase in solid content similar removal rate drop phenomena was observed. In the case of non-selective ceria slurry without the chemical additive, the reduction of removal rate in patterned areas was not observed. Therefore it is proposed that the ceria abrasive which is coated by chemical additive passivates the oxide of recessed areas that reduces the removal rate drop. On the basis of the result, it is known that the removal rate drop phenomena in patterned areas is not caused by solid content but caused by chemical additive.

M5.4
LAYOUT PATTERN DENSITY AND OXIDE DEPOSITION PROFILE EFFECTS ON DIELECTRICS CHEMICAL-MECHANICAL POLISHING. Young-Bae Park, I.Y. Yoon, J.Y. Kim, W.G. Lee, Hyundai Electronics Industries Co., Ltd., SYSTEM IC R&D Center, Cheongju, KOREA.

Based on experimentally obtained interaction distance, new test masks for characterizing and modeling pattern dependent variation of the remained thickness after chemical-mechanical polishing (CMP) are designed. Using these masks, we characterize polishing behavior with layout pattern density and pitch variations. Also deposition profile effects are compared between PETEOS (Plasma Enhanced Tetra Ethyl Ortho Silicate) and HDP (High Density Plasma) oxide in STI (Shallow Trench Isolation) CMP. Both remained silicon nitride thickness and expected oxide pattern density considering deposition profile effects show a good correlation with respect to pitch variation for a constant layout pattern density. And the relation between the remained silicon nitride thickness and the true layout pattern density are deduced. Also, the remained thickness increases nearly linearly with the layout pattern density for a constant layout pitch, which can be explained from the simple pattern density model.

M5.5
A CMP NUMERICAL MODEL COMBINING DIE SCALE AND FEATURE SCALE POLISHING CHARACTERISTICS.
Stephanie Delage, Frank Meyer, Goetz Springer, Infineon Technologies, Munich, GERMANY.

Chemical Mechanical Polishing (CMP) has emerged as the leading process for global and local planarization in silicon integrated circuits fabrication. However, there remains a large number of variation and effects due to layout pattern, equipment, and process dependencies that are still poorly understood. An effective characterization and modeling methodology is needed to facilitate the assessment and reduction of such variations. Several works have proposed models for Chemical Mechanical Polishing that provide various benefits. But most of them relate to a one-scale process description (wafer/die/feature) and a lack of multiscale models remains. In this paper, a new numerical model combining die scale and feature scale polishing characteristics for oxide CMP is proposed. This work is based on the analytical effective density model proposed by D.Boning and al. [1], that takes into account a die scale pad deformation. We expand this model to include the description of the removal at the feature scale. A topography discretization allows us to describe the polishing in down areas more accurately, depending on the down area width. The physical parameters considered include the deformation of the polishing pad (die scale and feature scale), the removal rate of a blanket wafer polished in the same process conditions, and the removal rate in down areas for small polishing times. Comparison of simulated results with MIT Testreticles experiments is performed and evaluated. [1] D. Boning at al., "Pattern dependent modeling for CMP optimization and control", MRS Spring Meeting, Proc. Symposium P: Chemical Mechanical Polishing, San Francisco, CA, Apr. 1999

M5.6
LINKING BLANKET TO PATTERNED WAFER PERFORMANCE IN COPPER CMP. S. Hymes, D. Tamboli, S. Chang, I. Butcher, B. Bayer, S. Storch, Ashland Specialty Chemicals, Dublin, OH.

A basic connection between blanket and patterned wafer performance is presented using a single fundamental assumption on the role of step height. Using idealized rate responses to downforce, the blanket wafer response of idealized slurries (both Prestonian and non-Prestonian) is used to develop expressions for planarization efficiency and dishing susceptibility of patterned films directly applicable to traditional and Damascene CMP. Results for real Cu CMP slurries are then compared to the model in order to demonstrate the link between composition, blanket and patterned wafer performance.

M5.7
CHARACTERIZATION OF A NEW CLEANING METHOD USING ELECTROLYTIC IONIZED WATER FOR POLY Si CMP PROCESS. Naoto Miyashita, Meiji Univ., Dept of Electrical and Electronic Engineering, Kawasaki, JAPAN; Toshiba Co, Semiconductor Company, Yokohama, JAPAN; Shin-ichiro Uekusa, Meiji Univ., Dept of Electrical and Electronic Engineering, Kawasaki, JAPAN; Masako Kodera, Yoshitaka Matsui, Toshiba Co, Semiconductor Company, Yokohama, JAPAN; Satoko Iseta, Takeshi Nishioka, Mechanical Systems Laboratory, Toshiba Corporation, Saiwai-ku, Kawasaki, JAPAN.

Recently, trench isolation technology has been developed and applied to bipolar LSI production. Especially, ploy-Si Chemical-Mechanical-Polishing (CMP) technique has made much improvement on deep trench isolation. Major issues of the process integration for that purpose have been the post CMP cleaning process. In general, the wafer surface after a conventional CMP is contaminated with silica particles and chemical impurities. These contaminations produce some unexpected patterns and crystal defects in the wafer surface layer after oxidation. It is difficult to remove them by the conventional cleaning technique. Therefore, we have established the new post CMP cleaning method, using the electrolytic ionized water containing chemical additive of a small quantity. The anode water has the cleaning effect for the metal and organic contamination, and the cathode water has the removing effect for the particles and the etching effect for the poly-Si surface. For this new cleaning process, it is important to avoid the chemical mechanical damages on the surface and control the surface roughness. Our experimental work has been focused on the numbers of the remaining particles, the contamination concentration and the surface roughness using AFM, VPD-ICP/MS. We herein report the properties of the electrolyzed water and the examined results of poly-Si surface after CMP process. It was found that the electrolyzed water is effective for surface control, and the new cleaning process is useful for CMP process.

M5.8
ENGINEERED POROUS AND COATED SILICA PARTICULATES FOR CMP APPLICATIONS. K.S. Choi, R. Vacassy, J. Grey, N. Bassim and R.K. Singh Department of Materials Science and Engineering and Engineering Research Center for Particle Science and Technology, University of Florida, Gainesville, FL.

The aim of this study has been to synthesize the microporous silica spheres and to coat as-synthesized SiO_2 with CeO_2 for CMP applications. First, spherical microporous silica powders with a narrow size distribution have been prepared by a precipitation technique involving the hydrolysis reaction of a silicon alkoxide in ethanol. The interparticle microporosity has been created by adsorption of an organic compound (glycerol) as the porogen. The presence of glycerol during the synthesis affect considerably the precipitation mechanism and its effect on the particle size will be discussed. The synthesis of silica microporous spheres of narrow size distribution yielded the preparation, by varying particle size and porosity, of a wide range of aqueous silica slurries. The influence of particle size, particle size distribution, porosity and particle concentration will be discussed in chemical mechanical polishing applications. Although silica particles show large plastic deformation than the bulk material, very good glass polishing rate are obtained due to the plastic deformation of the silica layer during CMP. Silica particles are suitable candidates for application in CMP because silica can be directly precipitated as monodispersed spheres, their narrow size distribution being an important requirement in CMP applications. Secondly, as-synthesized silica particles were coated with the cerium dioxide particles having hexagonal shape, which were precipitated by decomposition from the cerium precursors. For this study, three coating processes were introduced to investigate the best coating parameters. Improvements in CMP of glass were also obtained by coating silica particles with cerium oxide nanoparticles.

SESSION M6: LOW-k AND INTEGRATION ISSUES / PARTICLE AND PROCESS EFFECTS IN CMP
Chairs: Michael R. Oliver and David R. Evans
Friday Morning, April 20, 2001
Golden Gate A1 (Marriott)

8:30 AM *M6.1
ADVANCES IN THE CMP OF LOW k INTERLAYER DIELECTRIC MATERIALS. Sean Smith, Melanie Carasso, M. Krishnan, IBM T.J. Watson Research Center, Silicon Science and Process Technology, Yorktown Heights, NY.

While the minimization of device size in integrated circuits promises greater device speed and packing density, it has also led to problems with increased resistance-capacitance delays due to the high resistance of the small dimension metal lines, and the increased interline capacitance. Efforts to reduce the delay have resulted in the move to copper interconnects, as well as the development of new low k dielectric materials to reduce line to line capacitance and cross talk noise. The novel properties of the latter materials have resulted in significant challenges in their integration into these smaller interconnects. This paper will report on the challenges and advances in the chemical mechanical polishing of low k organic and inorganic interlayer dielectric materials. Particular emphasis will be placed on the dependence of the polishing behavior of these materials on the chemical parameters of the slurry, such as the type and size of the abrasive particles.

9:00 AM M6.2
CHALLENGES IN DEVELOPMENT OF MANUFACTURABLE COPPER AND LOW-k DIELECTRIC CMP PROCESS. Yongsik Moon, David Mai, Kapila Wijekoon, Fritz Redeker, Rajeev Bajaj, Applied Materials, CMP Product Business Group, Santa Clara, CA.

As the feature size of microelectronic devices shrinks down to sub-0.18 micrometer, the clock speed delay caused by resistance (R) and capacitance (C) of the interconnection is higher than the gate delay. This interconnection crisis requires new materials for metal and dielectrics to reduce RC delay and Copper (Cu) and low-k dielectrics became the possible candidates to meet this demand. This study focuses on the development of manufacturable and robust CMP process for Cu and low-k material needed in Cu damascene process. There have been three major problems in implementing Cu and low-k CMP for manufacturing advanced microelectronic devices; high dishing and erosion of Cu, surface damage, and absence of post-CMP cleaning process of low-k materials. The main cause of high dishing and erosion of Cu and low-k integrated devices is the high dielectrics loss during CMP due to the weak material property of low-k dielectrics. In this study, different copper and barrier removal slurries were evaluated. Each slurry combination was evaluated for topography and defectivity. Cu and barrier removal slurries were tested in Cu and low-k integrated pattern wafer polishing. Both processes offer different trade-offs wrt topography and metal loss. Due to the weak material property of low-k dielectrics, substantial amount of surface damage is created during CMP. This surface damage, causes bonding failure of the following deposited layer and eventually results in the unreliability of microelectronic devices. The surface damage appears mostly along the edges of the wafer due to the high friction force by the direct wafer-pad contact. By using differentiated pressure distribution on and around the wafer surface, the surface damage along the wafer edges has been dramatically decreased. This is the result of the reduced solid contact between the wafer edges and the polishing pad surface. Post CMP cleaning of low k dielectric materials is challenging because of the hydrophobic nature. A proprietary cleaning agent was used to completely wet the low k dielectric material after CMP and keep the surface hydrophilic. The solution cleans both the dielectric and copper surface without leaving any residue or damage to copper surface. This study details the development challenges associated wit development of a multi-level capable Cu-Low K process. Future areas of development and improvement are identified.

9:15 AM M6.3
DEVELOPMENT OF MANUFACTURABLE COPPER AND LOW-k DIELECTRIC CMP PROCESS. Yongsik Moon, Kapila Wijekoon, Yuchun Wang, Rajeev Bajaj, and Fritz Redeker, Cu CMP Technolgy Group, Applied Materials, Santa Clara, CA.

As the feature size of microelectronic devices shrinks down to sub-0.18 micrometer, the clock speed delay caused by resistance (R) and capacitance (C) of the interconnection is higher than the gate delay. This interconnection crisis requires new materials for metal and dielectrics to reduce RC delay and Copper (Cu) and low-k dielectrics became the possible candidates to meet this demand. This study focuses on the development of manufacturable and robust CMP process for Cu and low-k material needed in Cu damascene process. There have been three major problems in implementing Cu and low-k CMP for manufacturing advanced microelectronic devices; high dishing and erosion of Cu, surface damage, and absence of post-CMP cleaning process of low-k materials. The main cause of high dishing and erosion of Cu and low-k integrated devices is the high dielectrics loss during CMP due to the 'weak' material property of low-k dielectrics. In this study, nonselective-selective and selective-selective Cu and barrier removal slurries are tested in Cu and low-k integrated pattern wafer polishing and it is found that the dishing and erosion can be improved by abrasive-free selective-selective Cu and barrier slurries. Due to the weak material property of low-k dielectrics, substantial amount of surface damage can be created during CMP. The surface damage appears mostly along the edges of the wafer due to the high friction force by the direct wafer-pad contact. By using differentiated pressure distribution of the polishing head, the surface damage along the wafer edges has been dramatically decreased. Post CMP cleaning of low k dielectric materials is challenging because of the hydrophobic nature. A proprietary sheeting reagent completely wets the low k dielectric material after CMP and keeps the surface hydrophilic. The solution cleans both the dielectric and copper surface without leaving any residue or damage to copper surface.

9:30 AM M6.4
CHEMICAL-MECHANICAL POLISHING OF STEEL BY CARBON-CONTAINING THIN FILMS. Stephen J. Harris, Gordon G. Krauss, Ford Research Labs, Chemistry Dept., Dearborn, MI.

The material removal rate during polishing of steel by diamondlike carbon (DLC) and boron carbide (B4C) films falls by as much as four orders of magnitude during the course of several thousand polishing cycles. We provide quantitative scaling relationships which describe the abrasion kinetics. Not only the steel but also the DLC and B4C films are polished in the process, even though the films are at least 2-3 times harder than the steel. AFM analysis shows that the B4C coating becomes atomically smooth over regions of 100 nm by 100 nm as it polishes the steel. The polishing ability of the films is closely related to their nanoscale morphology but not to their microscale morphology. We provide evidence that the polishing of the films by the steel is primarily a chemical process, while the polishing of the steel by the film is primarily a mechanical process.

9:45 AM M6.5
CONTROL OF PATTERN SPECIFIC CORROSION DURING ALUMINUM CHEMICAL MECHANICAL POLISHING. Hyungjun Kim, Panki Kwon, Sukjae Lee, Hyung-Hwan Kim, Sang-Ick Lee, Chul-Woo Nam, Seo-Young Song, Memory R&D Division, Hyundai Electronics Industries Co. Ltd., Ichon, KOREA.

A pattern specific corrosion of aluminum wires was found during aluminum chemical mechanical polishing process. This paper presents and discusses the particular pattern dependency of the corrosion behavior and effective control methods in order to reduce the corrosion. An aluminum single damascene structure on silicon dioxide thin film was prepared and the effects of process variables and pattern configuration on corrosion behavior were extensively explored. It was demonstrated that corrosion of aluminum wire was associated with cleaning media and pattern configuration. Two approaches were made for preventing the pattern specific aluminum corrosion: by changing CMP consumables and post polish treatments, and by modifying pattern configurations. An optimized process condition was successfully evolved from such approaches and resulted in corrosion-free aluminum damascene structure. Electrical data were also collected and correlated with corrosion phenomena.

10:30 AM M6.6
DIRECT VISUALIZATION OF PARTICLE DYNAMICS IN MODEL CMP GEOMETRIES. Claudia Zettner and Minami Yoda, Georgia Institute of Technology, School of Mechanical Engineering, Atlanta, GA.

Chemical-mechanical polishing (CMP), used to planarize silicon wafers, involves shearing an abrasive particle-laden slurry between a rough rotating polyurethane pad and the wafer. The chemical and mechanical properties of the slurry, which consists of sub-micron colloidal particles suspended in a liquid lubricant, can greatly affect wear rates and material selectivity in CMP. The particle dynamics in a model CMP geometry were studied experimentally in this work. A technique for directly measuring the particle concentration next to the wafer surface was developed and used to evaluate how various particle properties affect this concentration. We hypothesize that increasing this particle concentration by manipulating both chemical and mechanical particle properties will increase their interaction with the wafer surface and hence CMP material removal rates. Evanescent waves were used to illuminate a roughly 300 nm thick region next to a solid glass surface. The surface, simulating the wafer is fully flooded with an aqueous dilute suspension of 200-300 nm diameter fluorescent particles. The suspension is sheared between the stationary glass surface and a rotating silicon surface textured with periodic micron-scale asperities, simulating the pad. Since the evanescent waves only illuminate a layer about one particle diameter thick next to the glass surface, the abrasive particle concentration next to the glass surface can be measured simply by counting particles. The effect of process properties such as particle size (diameters of 200 vs. 300 nm) and hardness (polystyrene vs. silica particles), the presence or absence of van der Waals forces and shear rate on particle concentration will be investigated. The effect of pad roughness on the particle dynamics will also be studied by comparing results for smooth and periodically textured rotating silicon surfaces.

10:45 AM M6.7
MODELING OF CHEMICAL-MECHANICAL PLANARIZATION. Rajiv K. Singh, Zhan Chen, and Seung-Mahn Lee, MS&E, University of Florida, Gainesville, FL.

Although chemical-mechanical planarization (CMP) has successfully been employed in semiconductor device fabrication, the lack of comprehensive and quantitative understanding on CMP mechanism continuously command researches to establish CMP models. The existing CMP models have help people in understanding and developing CMP process, but issues such as pad-slurry-wafer interaction mechanism and decoupling of chemical and mechanical effects still need to be resolved for the advance of CMP process. In this paper, we present a new model on CMP process, in which we emphasize on the key role of the chemically modified layers on the wafers. We realize that the remove rate is a function of the formation and removal of the chemically modified layer. The chemistry in the slurry defines the formation rate of the chemically modified layer, while the removal of this layer is caused by pad-particle-wafer interaction. The observed removal rate is thus the balance of formation and removal of the chemically modified layer under certain chemical and mechanical conditions. We categorized the real CMP process into three categories: mechanically controlled, chemically controlled, and intermediate CMPs. The effects of chemistry, pressure, particle loading and particle size in different categories are discussed. The application of this model on tungsten CMP and copper CMP are also discussed in this paper.

11:00 AM M6.8
EFFECT OF pH ON CHEMICAL-MECHANICAL POLISHING OF COPPER AND TANTALUM. Anurag Jindal, Ying Li, S.V. Babu, Depts of Chemical and Mechanical Engineering, Center For Advanced Materials Processing, Clarkson University, Potsdam, NY.

During chemical-mechanical polishing (CMP), pH not only has a great impact on the stability of the slurry, but may also determine the surface reactions that occurs during polishing. Our previous work found that the slurry pH has a very strong influence on the removal rate of Cu and Ta in DI water. Even the η-phase (low density) alumina powders polish Ta film at relatively high rates at high pH values in contrast to the near zero rates observed at near neutral pH values. This is consistent with our earlier observation that the magnitude of electrostatic interactions is an important parameter in determining the material removal rates of Cu and Ta films. This work is now extended to Cu and Ta polishing in the presence of different chemicals, namely, H_2O_2, H_2O_2/glycine, and KIO_3, using fumed silica powders and alumina particles with different crystalline structures. Microhardness measurements by nanoindentation in the presence of chemicals, along with in situ electrochemical measurements, are performed to investigate the surface modification of Cu and Ta at different pH values in different chemical environments, and the results will be related to the material removal rate.

11:15 AM M6.9
A MODEL FOR EFFECT OF COLLOIDAL FORCES ON CHEMICAL-MECHANICAL POLISHING. Ali R. Mazaheri and Goodarz Ahmadi, Department of Mechanical and Aeronautical Engineering, Clarkson University, Potsdam, NY.

It is well known that the variation of slurry PH could significantly affect the Chemical-Mechanical polishing Process. In this study, the mechanical model for the effect of abrasive on surface removal rate is extended by including the double layer forces. It is shown that the double layer attraction and repulsion could overwhelm the other surface forces such as the Van der Waals force, and thus, plays a major role in Chemical-Mechanical-Polishing (CMP) processes. It is found that the magnitude and sign of the zeta potentials of the surface and the abrasive particles significantly affect the removal rates. The results show that the removal rate increases sharply in for the cases that the zeta potentials of the surface and abrasive have opposite sign. On the other hand the removal rate decreases the zeta potentials have the same sign. The finding are compared with the available data and qualitative agreement was observed.

11:30 AM M6.10
EFFECT OF ELECTROCHEMICAL INTERACTIONS ON REMOVAL RATES AND PLANARITY IN COPPER CMP. Dnyanesh Tamboli, Stephen Hymes, Song Chang, Ben Bayer, Ionica Butcher and Steven Storch.

Copper CMP involves complex interplay between chemical and mechanical components. In this study we evaluate the CMP performance of a number of slurry chemistries using a DOE approach and correlate the CMP performance to the chemical and mechanical interactions between the slurry and copper surface. The chemical interations between the copper surface and the slurry are evaluated by static etch rate measurements and electrochemical measurements. Parameters such as temperatures generated in the polishing, the ratio of removal rate to static etch rates and the slope of removal rates vs, polishing pressure are used to characterize the chemical and mechanical interactions between CMP. The results obtained on the blanket wafers are subsequently applied to understanding the planarization performance of patterned wafers.

11:45 AM M6.11
TRANSIENT ELECTROCHEMICAL STUDIES ON CHEMICAL EFFECTS IN METAL CHEMICAL-MECHANICAL PLANARIZATION PROCESS. Zhan Chen, Seung-Mahn Lee, Rajiv K. Singh, MS&E Dept, University of Florida, Gainesville, FL.

The formation of the chemically modified layer on the wafer surface is one of the key aspects to understand chemical-mechanical planarization (CMP) mechanism. In order to decouple chemical and mechanical effects in a CMP process, the formation rate of the chemically modified layer should be quantitatively understood. The CMP process is a non-equilibrium process in which the steady state is reached by the balance of transient formation and removal of the chemically modified layer. The time interval between the chemical modification and mechanical removal of the surface layer is typically within a fraction of a second. Thus, only in this short time domain that the chemically modified layer formation is relevant to real CMP conditions. Chronoamperometry provides an appropriate method to investigate the mechanism and the rate of the surface layer modification in very short time on conducting wafers. In this study, the chemical effects on tungsten and copper CMPs with different slurry chemistries have been studied with this technique, together with impedance analysis. The formation rates of surface layer modification on tungsten and copper surface are obtained and compared with CMP removal rates. The insights to the overall metal CMP mechanism obtained from the formation rate of the chemical modification layer are also discussed in this paper.

SESSION M7: ISSUES IN CMP CLEANING
Chairs: Rajesh Tiwari and Suryadevara Babu
Friday Afternoon, April 20, 2001
Golden Gate A1 (Marriott)

1:30 PM M7.1
CHEMISTRY AND TREATMENT OF CMP WASTEWATER. Josh H. Golden, Microbar Incorporated, Sunnyvale, CA; Robert Small, Louis Pagan, Cass Shang, EKC Technology, Inc., Hayward, CA; Srini Ragavan, University of Arizona, Department of Materials Science and Engineering, Tucson, AZ.

Integrated circuit fabrication at 180 nm and beyond relies on chemical-mechanical polishing (CMP) to reduce wafer surface imperfections, and thus improve the depth of focus of lithography processes through better planarity. As a result, the CMP market is growing faster than other equipment sector, and is expected to reach $1.7 billion by the year 2003 and $5 billion by 2010. The growing use of CMP slurry also drives the consumption of ultrapure water (UPW) for slurry dilution, cleaning and rinsing wafers and production equipment. Until recently, the CMP process accounted for only about 5% of the total UPW used in IC manufacturing, but estimates at leading-edge fabs put the usage in 2001 at 30-40% of the water consumed. Consequently, CMP wastewater generation is expected to reach 450 million gallons by the year 2006, and this effluent will contain increasing amounts of copper. However, this increased use of UPW by CMP processes conflicts with the National Technology Roadmap for Semiconductors target of decreasing overall water consumption five-fold, from today's approximately 1500 gal/200 mm wafer to 300 gal/200 mm wafer in 2003, based on increased adoption of recycling and conservation. Before the recent introduction of CMP, the CMP waste stream was not a major issue. Silica and fluoride contaminants were typically diluted with other fab process water or treated by the fab acid waste neutralization system (AWNS). However, because the AWNS is not equipped to handle high levels of suspended solids or especially, heavy metals such as copper, fabs are beginning to run the risk of violating local regulations for these contaminants in discharged wastewater. To effectively meet regulatory challenges and safely treat CMP wastewater, it is useful to become familiar with the CMP wastewater chemistry, treatment options and regulatory issues regarding copper in CMP effluent.

1:45 PM M7.2
ENVIRONMENTALLY-BENIGN CLEANING FOR GIGA DRAM USING ELECTROLYZED WATER. Hyoseob Yoon and Kunkul Ryoo, Soonchunhyang Univ., Dept of Advanced Materials Engr, Asan, KOREA.

Cleaning process takes an important role technically and commercially in semiconductor manufacturing processes. As

semiconductor devices are scaled down, the number of manufacturing processes increases and the number of cleaning processes increases as well. The conventional RCA cleaning process consumes very large amount of chemicals and ultra pure water (UPW). From environmental and commercial view points, it is clear that the cleaning process must reduce consumption of chemicals, UPW, and production costs. In this study, Si wafers contaminated with particles and metallic impurities were cleaned using the electrolyzed water (EW). Properties of generated EW such as oxidation-reduction potential (ORP), pH, and lifetime were measured. In order to compare characteristics of anode water (AW) with those of cathode water (CW) of EW on DHF treated Si wafer surface, contact angles were also measured. pH and ORP of AW and CW measured to be 4.7 and +1050 mV, and 9.8 and 750 mV, respectively. AW and CW were deteriorated after electrolyzing, but maintained their characteristics for more than 40 minutes. Contact angles of UPW, AW, and CW on DHF treated Si wafer surfaces were measured to be 65.9°, 66.5° and 56.8°, respectively. Therefore, it was understood that CW was prone to wetting on hydrogen-terminated surface. AW was effective for Cu removal, while CW was more effective for Fe removal. The particle distribution after AW and CW cleaning showed the applicability for 0.1 μm particle removal. It is hence promising that this cleaning technology will be very effective for promoting environment, safety, and health (ESH) issues in semiconductor manufacturing.

2:00 PM M7.3
POLISHING AND CLEANING OF LOW k DIELECTRIC MATERIAL FOR ILD AND DAMASCENE. Yuchun Wang, Rajeev Bajaj, Yongsik Moon, David Mai, Kapila Wijekoon, Yufei Chen, Fritz Redeker, CMP Division, Applied Materials, Santa Clara, CA; Dian Sugiarto, Li-Qun Xia, CVD Low K Division, Applied Materials, Santa Clara, CA.

This paper describes CMP challenges in development of Cu-low K process technology. As copper-Teos/FSG schemes are being implemented successfully in early manufacturing, development focus has shifted to Cu-OSG integration development. Cu-OSG presents unique challenges with CMP integration, as these films tend to have much lower hardness than silicon dioxide. Significant process challenges have to be overcome prior to successfully implementing CMP process which does not mechanically damage the softer films and at the same time can achieve planarization requirements expected from CMP process. In addition, the OSG films tend to be hydrophobic leading to a need for developing improved cleaning processes/consumables. It was determined that AMAT ElectrapolishTM barrier slurry is extendable to OSG films. Good removal rate and removal profile can be achieved with ElectrapolishTM. A proprietary cleaning solution reduced defect counts by 2 orders of the magnitude on SurfScan SS6200 on blanket hydrophobic wafers. The same cleaning solution can be applied to copper-low k damascene patterned wafers to clean both copper and dielectric surface. Polished Black Diamond films have RMS roughness less than 2 angstroms and copper surface roughness about 5 angstroms with good surface finish. Process performance using the Cu-FSG process was used to highlight capability gaps in the process. Process enhancements were then integrated into the new process. Blanket and patterned wafer results are presented to demonstrate final capability. Future directions for process enhancement are identified.

2:15 PM M7.4
MECHANISMS OF POST-CMP CLEANING. Emmanuel Estragnat, Hong Liang, Dept of Mechanical Engineering, Univ of Alaska Fairbanks, Fairbanks, AK; Kristan Bahten, Dan McMullen, Rippey Corporation, El Dorado Hills, CA.

There has been a great interest in understanding post-CMP cleaning mechanisms. From the view point of CMP engineers, this means to know the relationship between applied load, relative surface speed, resulting friction, and effectiveness of particle removal. Inevitably, this leads to maintaining the optimum water film thickness between a brush and the wafer/disk. This work simulates the cleaning conditions using a laboratory model system. Comparing with the classic lubricating concept as presented in a measured Stribeck curve, we have concluded that the cleaning process is a boundary to elastohydrodynamic process that involves a constant contact between a brush and wafer/disk.

2:30 PM M7.5
A STUDY OF CMP MULTI HEAD CMP TOOL EFFECT ON BPSG FILM FOR ADVANCED DRAM APPLICATIONS. David A. Hansen, Gerry Moloney, Cybeq Nano Technologies, San Jose, CA; David Watts, Ebara Technologies, San Jose, CA.

With the maturity of CMP processes and consumables most of the major IC fabrication companies are now investigating CMP tool designs that will help increase throughput without loss of process control with a corresponding reduction in CoO. In the past most of the attention was directed at multi-head polishing tools as a means of attaining these goals. However most of the early multi-head polishing tools produced severe Head-To-Head Thickness Variation (HTHTV) and resulting Wafer-To-Wafer Thickness Variation (WTWTV). In fact some of the reported WIWNU measurements were as high as 7%, which could be tolerated by some earlier products. However for all new advanced device products this high WIWNU could not be tolerated and hence the drive toward multi-head polishing tools faded. With new advanced CMP consumables and techniques it might be a good idea to revisit a multi-head polishing tool to see if the above issues my be addressed. In this work we have carried out a study of CMP multi-head CMP tool and its effect on BPSG film for advanced DRAM applications by using the Cybeq Nano Technologies IP-8000 Dry-In/Dry-Out multi-head CMP tool. Once the process recipe was optimized on blanket BPSG wafers, 84 BPSG device wafers were run. Analysis of planarized wafers was carried out and the WTWTV (1σ) and HTHTV (1σ) of 0.99% and 0.88%, respectively, were obtained. Furthermore the average measured WIWNU and average post-step height was 2.43% and 45 Å, respectively. These results demonstrate the vast improvement that has been made by using advanced consumables and process techniques compared to early work using multi-head CMP tools. In this paper we will detail how the use of the advanced consumable, i.e. tighter manufacturing specifications, and process techniques, i.e. novel pad dressing methods, have dramatically improved the viability of the multi-head CMP tool.

2:45 PM M7.6
MULTIPROBE ENDPOINT DETECTION FOR PRECISION CONTROL OF THE COPPER CMP PROCESS. Thomas Laursen, Malcolm Grief, SpeedFam-IPEC Incorporated, Chandler, AZ.

A reliable end-point detection (EPD) system is critical for maintaining optimized CMP processes. EPD controls the delicate point in process optimization ensuring that the overburden being polished is removed everywhere across the wafer, while minimizing overpolish. A multiprobe EPD system has been developed based on monitoring a broad spectrum of reflected light. Light is reflected off the wafer surface during polish. While polishing on SpeedFam-IPEC's 200-mm and 300-mm orbital polishers, large representative areas of the wafer are monitored from multiple locations in the pad continuously throughout the polish process. Spectra of reflected light from cleared and uncleared copper on a pattern wafer demonstrates a clear transition. The normalized copper spectrum is approximately a straight line while the normalized spectrum of a cleared region is oscillating due to thickness interference fringes of the underlying dielectric. Basing the EPD on this pronounced shape change is a direct result of using a broadband probe and spectrograph, making it robust and insensitive to intensity changes. Another essential feature of this robust EPD is the use of a flash lamp, making high-frequency discrete measurements instead of averaging. The wafer is probed at optimized multiple locations at all times by small-diameter light spots. The coverage of the monitoring is extensive and the radial coverage is close to 100% on a real-time basis. The EPD call is made based on the EPD trace, which displays the fractional copper coverage as a function of polish time. The detection of copper clearing is very reliable and predictable and not sensitive to process changes. Multiprobe EPD has been demonstrated to be a robust system for copper CMP on the orbital polisher, constantly monitoring the entire wafer. The same system will be an important component in closed-loop process control.