SYMPOSIUM N

Microelectronics and Microsystem Packaging

April 16 – 19, 2001

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TUTORIAL

ST L/N/EE: ADVANCED TECHNIQUES FOR MATERIALS CHARACTERIZATION AND RELIABILITY TESTING

Monday, April 16, 2001
1:30 p.m. - 5:00 p.m.
Salon 10/11 (Marriott)

Advanced microelectronic interconnection structures make use of high-conductivity copper conductors with low dielectric-constant insulators at extremely small dimensions. As a consequence, issues arise in the characterization and reliability of these structures that are not found in the well-used aluminum-silica system. Differences appear in: the microstructure of the copper metallization and the changes induced in it by processing, thermal loading and electromigration; the mechanical characteristics of the surrounding dielectric; and, the resulting interdependence of the reliability of the interconnection structure and the changes in the metal microstructure as constrained by the dielectric. This tutorial will cover these topics, introducing participants to the issues involved and the fundamental reliability concerns for both the metallization and its supporting dielectric encapsulant. Advanced methods for characterizing electromigration behavior (especially that of copper), mechanical properties of dielectrics (especially those of low-k materials), and metallization microstructure (by X-Ray diffraction) will be described.

Instructors:
Du Nguyen, IBM Microelectronics
Hari Rathore, IBM Microelectronics
Robert F. Cook, University of Minnesota
Stuart R. Stock, Georgia Institute of Technology

SESSION N1: PLASTIC ENCAPSULATION AND UNDERFILL

Chair: Anthony A. Gallo
Tuesday Morning, April 17, 2001
Golden Gate A3 (Marriott)

8:30 AM *N1.1
GREEN MOLDING COMPOUNDS. Anthony A. Gallo, Dexter Electronic Materials, Olean, NY.

New molding compounds for encapsulation of integrated circuits are required in the future because the bromine-containing flame retardants and antimony oxide flame retardant synergists, which are commonly used in most present day molding compounds, are thought to be potentially unsafe to the environment. Phosphorus-containing compounds, have been proposed as flame retardants. Although they are less hazardous, molding compounds containing these compounds generally possess undesirable properties such as high moisture absorption. New molding compounds have been developed that are substantially free of bromine, antimony and phosphorus and yet pass UL94V-O at 3.2 mm bar thickness. These molding compounds contain either two transition metal oxides with either standand epoxy cresol novolac or biphenyl resins or a combination of a single transition metal oxide with highly aromatic epoxy resins or hardeners. Both molding compound types were found to give good moiture and high temperature electrical reliability for ICs encapsulated with these materials. Molding compounds with transition metal oxides have the potential for less health and environmental concern since these metal oxides are suggested by the American Conference of Governmental Industrial Hygienists to be less hazardous than antimony trioxide.

9:00 AM N1.2
EVALUATION OF THERMOMECHANICAL PROPERTIES OF GREEN MOLDING COMPOUNDS. Leonorina G. Cada, Rasmia Lalanto and Noel Lipat, On Semiconductor Philippines Inc., Carmona, PHILIPPINES.

In an attempt to reduce and eventually eliminate the use of potentially hazardous halogenated compounds, On Semiconductor Philippines Inc., has evaluated the thermomechanical properties of select non-halogenated molding compounds (common name: green molding compounds or GMCs). The study included evaluation of thermal stability, adhesion properties, manufacturability and reliability of GMCs as compared to conventional halogenated molding compounds. The data obtained from thermogravimetric analysis (TGA) revealed higher decomposition temperatures for GMCs containing magnesium hydroxide or phosphorous compounds as flame-retardants, relative to the decomposition temperatures for existing halogenated molding compounds. A preliminary study on the decomposition products of culls and runners, considered as waste products from the molding process, was conducted using TGA coupled with Fourier Transform Infrared (FTIR) spectroscopy and using Gas Chromatography-Mass Spectroscopy (GC-MS). Identified spectra of decomposition products for GMCs based on orthocresol novolac resins were predominantly acetone, cresols and phenols. Culls and runners from existing biphenyl-based molding compounds yielded methanol, phenols and acrylic esters upon thermal decomposition. No significant and simple trend in adhesion property was observed as the resin type and flame-retardant vary in the different molding compounds. Thermomechanical FE model showed lower internal stress level for the GMCs. Their manufacturability and reliability were found comparable to the conventional molding compounds. This paper discusses the relative thermomechanical stability of the green molding compounds and its potential impact on package robustness and on environmental concerns of the industry.

9:15 AM N1.3
PACKAGE CHARACTERIZATION AND FINITE ELEMENT ANALYSIS. Flordivino L. Basco and Doris M. Asis, ON Semiconductor Philippines Inc., Carmona, Cavite, PHILIPPINES.

The direction towards environment friendly manufacturing has triggered the semiconductor companies to source out materials and processes that eliminate the use of lead, antimony, bromine and other toxic packaging and process materials. On Semiconductor has initiated a corporate wide strategy to make our manufacturing meet or converge to a lead-free and green mold compound environment. Study showed that lead-free solder requires 260°C-reflow temperature to optimize mounting of the surface mounted package on PCB's. In this direction, characterization is done on the NiPdAu preplated 20L(ead) TSSOP at 260°C. Triple IR reflow pass and oil immersion tests at same moisture sensitivity level 1 (MSL1) are done on this. Degree of delamination is measured each test, before and after preconditioning. Results are compared with the 235°C reflow response. Furthermore, finite element study was formulated to analyze package robustness on both 235°C and 260°C reflow temperatures.

9:30 AM N1.4
HYGROSCOPIC SWELLING AND SORPTION CHARACTERISTICS OF EPOXY MOLDING COMPOUNDS USED IN ELECTRONIC PACKAGING. Haleh Ardebili, General Electric Company at Corporate Research and Development, Schenectady, NY; Ee Hua Wong, Institute of Micro-Electronics, SINGAPORE; Michael Pecht, CALCE Electronic Products and Systems Center, University of Maryland at College Park, College Park, MD.

Moisture induced swelling mismatches between different materials in a microelectronic package can cause stresses that lead to underestimated failure driving force. In this study, the swelling coefficients of four types of epoxy molding compounds used in electronic packaging were measured. The samples were subjected to isothermal desorption and dimensional changes were measured using a Thermo-Mechanical Analyzer. The moisture sorption characteristics of the four different types of molding compounds at 85°C/85%RH were also determined from weight gain measurements. The effect of desorption temperature on the swelling coefficients was then investigated by comparing swelling coefficients at 85C, Tg, and 230C. The molding compound characteristics including percentage fillers, Tg and crosslinking density were considered in explaining the swelling coefficients and the moisture sorption behavior of the four different types of epoxy molding compounds. The significance of swelling from reliability perspective for the four types of molding compounds was also determined.

9:45 AM N1.5
EFFECTS OF HYDRO-THERMAL AGING ON THE DIELECTRIC PROPERTIES OF EPOXY MOLDING COMPOUNDS. Patrice Gonon, Alain Sylvestre, Lab for Electrostatics and Dielectric Materials, University of Grenoble, FRANCE; Jerome Teysseyre, Christophe Prior, STMicroelectronics, Corporate Package Development, Grenoble, FRANCE.

During service IC packages are subjected to the combined effects of moisture (ambient) and thermal aging (soldering processes, high-temperature applications). Such hydro-thermal aging is well know to be at the origin of some mechanical failures (delamination, popcorn cracking...). These effects have been well characterized in the past years. On the other hand, less data are available regarding the effects of hydro-thermal aging on the dielectric properties of packaging materials. Since dielectric characteristics -dielectric constant and dissipation factor- are key parameters for package design and modeling, it is important to understand the influence of humidity and temperature on these characteristics. In the present work we studied industrial epoxy molding compounds currently used for microelectronic packaging (polyfunctional epoxies loaded with 90 wt.% silica). We measured the dielectric constant and the loss factor, between 100 Hz and 100 kHz, as a function of hydro-thermal aging. Long term aging was simulated using Joint Electron Device

Engineering Council (JEDEC) standard procedures. In order to distinguish between the effects of moisture and temperature the humidity exposure and thermal stress times were varied separately. In addition, to study the influence of cross-linking density on aging, the study was performed for resins having different initial levels of curing. We observed important variations in the dielectric properties as a function of aging procedure and degree of curing. These variations are discussed in relation with material inner structural changes.

10:30 AM *N1.6

FUNDAMENTAL STUDY ON ADHESION OF EPOXY UNDERFILL MATERIALS WITH PASSIVATION LAYER IN FLIP-CHIP PACKAGING. Shijian Luo, C.P. Wong, Packaging Research Center, School of Materials Science and Engineering, Georgia Institute of Technology, Atlanta, GA.

Underfill is used to fill the gap between integrated circuit (IC) chip and substrate in flip chip package. This paper systematically discusses the environmental influence (temperature and humidity) on the adhesion performance of underfill material. The adhesion strength (measured by die shear test on 2 mm by 2mm die) between the underfill and passivation does not show significantly after thermal cycling test (-55°C for 10 min, 125°C for 10 min per cycle) for 1000 cycles. The adhesion strength of underfill material decreases with the increase of test temperature above room temperature. The sharp decrease occurs at a temperature below the glass transition temperature of underfill material, as the decrease in adhesion strength versus temperature is due to the decrease in modulus of underfill and decrease of interfacial interaction with the increase of temperature. Adhesion strength of underfill with different passivation materials decreases after aging in a high temperature and high humidity environment (pressure cooker test at 121 C, 2 atm, 100% relative humidity for 24 hours, or 85 C 85% relative humidity for 500 hours). The adhesion degradation after aging in a high temperature and high humidity environment is strongly dependent on the hydrophilicity of passivation material, which is characterized by contact angle of water on the surface. Hydrophilic passivation such SiO2 and SiN shows much more severe adhesion degradation than the hydrophobic passivation such as benzocyclobutene (BCB) and polyimide (PI). Kinetics of moisture diffusion into die shear sample is studied by monitoring moisture pickup of a 2 mm by 2 mm long orthogonal underfill sample. Although the degradation of adhesion strength is due to the moisture diffusion into the underfill, the rate of adhesion degradation of die shear sample during aging in an 85 C 85% relative humidity environment is not controlled by moisture diffusion. The model on adhesion degradation will be described. It will be demonstrated that the adhesion stability for hydrophilic passivation can be successfully improved by use of coupling agent such as organofunctional silane that introduces stable chemical bond at interface.

11:00 AM N1.7

EFFECT OF COMPOSITION AND BEAD SETTLING ON DEBONDING OF UNDERFILL LAYERS. Lorraine C. Wang and Reinhold H. Dauskardt, Stanford University, Department of Materials Science & Engineering, Stanford, CA.

With the increased complexity of microelectronic devices and a general trend towards making chip packages smaller, the need for reliable high-density flip-chip packaging is increasingly important. In these packages, epoxy underfills are often used to surround a solder ball grid array in order to help support both mechanical and thermal stresses in the system. One of the most critical issues that arise in these systems involves the adhesion between the underfill and chip passivation. Factors such as the incorporation of inorganic particles within the epoxies and exposure to moisture can greatly affect this adhesion. This research focuses on determining the mechanisms that cause debonding between underfill systems and Si_3N_4 passivation. A fracture mechanics approach was used to test two model underfills, one based on an aliphatic epoxy, and the other based on a bisphenol F epoxy. The layers in question were sandwiched between silicon substrates and constructed in a double cantilever beam (DCB) configuration. Interestingly, these two underfills, which are similar mechanically, appear to show very different critical and subcritical behavior. The aliphatic underfill exhibits subcritical debond growth under constant displacements, behavior typically seen in interface systems, while the bisphenol F underfill surprisingly shows little susceptibility to stress corrosion. Although both underfills show evidence of filler settling, the addition of filler has opposing effects on their critical adhesion values. The effects of varying filler content in these underfills as well as environmental effects on the critical and subcritical behavior of these systems will be examined.

11:15 AM N1.8

INVESTIGATIONS OF UNDERFILL FLOW OF MODEL SUSPENSIONS AND INDUSTRIAL ENCAPSULANTS. Thomas Driscoll, Qing Peng, Eric Cotts, Binghamton University, Dept of Physics, Binghamton, NY; Drew Davidson, Gary Lehmann, Binghamton University, Dept of Mechanical Engineering, Binghamton, NY.

In Direct Chip Attach (DCA), a critical step in manufacturing is the underfill process. This procedure is necessary for minimizing stresses that result from the mismatch between the coefficient of thermal expansion (CTE) of the different materials (board, chip, solder interconnects, etc.) involved. The underfill process involves the capillary flow of solid/fluid mixtures into flow passages that are typically smaller than 127 microns. The underfill material consists of solid spheres (generally silica) suspended in a liquid carrier material (epoxy resin). Modeling this underfill flow process is difficult and further complicated by the presence of the filler particles necessary to achieve the desired CTE, particularly since the particles can be comparable in size to the underfill gap spacing. Our modeling of the underfill process, however, treats the material as a homogeneous fluid (i.e. no particles) with measured fluid properties (ex. surface tension, viscosity, etc.). Our research has concentrated primarily on a parameter study and flow of model suspensions and an industrial encapsulant. Wetting and rheological properties were measured for purposes of modeling the flow behavior. The average flow front position of the model suspensions and/or industrial encapsulants is calculated from the change in capacitance as the underfill material flows into the flow cell. Comparisons of flow distances and dynamics contact angle measurements between model calculations and experiments are made.

SESSION N2: LEAD-FREE SOLDER AND CONDUCTIVE ADHESIVES

Chair: Abhijit Dasgupta
Tuesday Afternoon, April 17, 2001
Golden Gate A3 (Marriott)

1:30 PM *N2.1

MICROTHERMOMECHANICAL ANALYSIS OF LEAD FREE SOLDER JOINTS. Abhijit Dasgupta, Peter Haswell, CALCE Electronic Products and Systems Consortium Mechanical Engineering Department, University of Maryland, College Park, MD.

This paper presents a micro-mechanistic approach for modeling fatigue damage initiation due to cyclic plasticity and cyclic creep in a Pb-free solder. Such loading arises due to vibraton and thermal cycling of electronic assemblies. Experimental measurement of cyclic fatigue behavior is reported in this paper, under different temperature and strain rates. Fatigue damage due to cyclic plasticity is modeled with dislocation mechanics. A conceptual framework is provided to quantify the influence of temperature on fatigue damage due to cyclic plasticity. Damage mechanics due to cyclic creep is modeled with a void nucleation model based on micro-structural stress fields. Micro-structural stress states are estimated under viscoplastic phenomena like grain boundary sliding and its blocking at 2nd phase particles, and diffusional creep relaxation. A conceptual framework is provided to quantify the creep-fatigue damage due to thermo-mechanical cycling.

2:00 PM N2.2

ELECTROMIGRATION OF FLIP CHIP SOLDER BUMPS ON Cu/Ni(V)/Al THIN FILM UNDER-BUMP-METALLIZATION. Woojin Choi, Everett C.C. Yeh, and K.N. Tu, Dept. of Materials Science and Engineering, UCLA, Los Angeles, CA; Peter Elenius, and Haluk Balkan, FlipChip Technologies, Phoenix, AZ.

The electromigration of flip chip solder bump (eutetic SnPb) has been studied at temperatures of 100, 125 and 150°C and current densities of 1.9 to 2.75 x 10^4 A/cm^2. The under-bump-metallization on the chip side is thin film Al/Ni(V)/Cu and on the board side is thick electroless Ni coated with 30 nm of Au. Stressed at the higher current density, the Mean-Time-To-Failure (MTTF) was found to decrease much faster than what we expect from the published Blacks equation. At the cathode where voids formed, the thin Ni(V) layer was not found. We note that this Ni(V) layer has been found to be very stable under multipe reflows, but it disappeared in electromigration after a high current stressing. In addition, the Cu-Sn intermetallic compounds formed during the reflow is known to adhere well to the thin film UBM, but they also detached from the UBM after current stressing. Therefore, the UBM itself could be part of the reliability problem of the flip chip solder joint under electromigration. By simulating the current distribution in the sample, we found that current crowding occurs at the chip side where the current enters the solder ball. We are able to match this simulation to the real electromigration damage in the sample. The experimental result showed that voids initiated from the position of current crowding and propagated outward. This phenomenon of current crowding in flip chip solder joints can decrease MTTF.

2:15 PM N2.3
ELECTROMIGRATION OF EUTECTIC TIN-LEAD AND TIN-SILVER-COPPER SOLDERS ON ELECTROLESS NICKEL.
T.Y. Lee, K.N. Tu, Univ of California-Los Angeles, Dept. of MS&E, Los Angeles, CA; D.R. Frear, Motorola, Interconnect System Laboratory, Tempe, AZ.

The electromigration of eutectic SnPb and $SnAg_{3.8}Cu_{0.7}$ solder bumps on electroless Ni Under Bump Metallurgy (UBM) were characterized after current stressing at 120°C for several days at 10^4 to 10^5 A/cm^2. The solders were cross-sectioned before current stressing. The marker motion on the cross-sectioned surface was used to calculate the rate of electromigration and the effective charge number of the solders. For eutectic SnPb, the effective charge number was between 36 and 100 after 39.5 hrs of electromigration. For $SnAg_{3.8}Cu_{0.7}$, the marker movement was negligible so it was not possible to measure the effective charge number even after 200 hrs current stressing. The atomic flux of current stressing in $SnAg_{3.8}Cu_{0.7}$ is much smaller than that in eutectic SnPb. Voids were observed in both solders on the cathode side of the joint. The growth of the intermetallic compound (IMC) between the Ni and the solders during current stressing is 10 to 100 times faster than the growth during solid state annealing. Dissolution of electroless Ni was observed. The dissolution of electroless Ni was affected by the Ni-Cu-Sn compound formation adjacent to the electroless Ni UBM. In Cu UBM on PCB side, no Cu dissolution was observed and there was no enhanced growth of Cu-Sn compounds during electromigration.

3:00 PM N2.4
TEXTURED GROWTH OF Cu-Sn INTERMETALLIC COMPOUNDS.
Kithva Prakash Hariram, Thirumany Sritharan, Nanyang Technological University, School of Materials Engineering, SINGAPORE.

Rectangular sections of an extruded rod of Cu were reacted with molten Sn-Pb solder alloys of different composition over a range of temperatures above their liquidus temperatures to study the growth behaviour of Cu-Sn intermetallic compounds (IMC) at the Cu/solder interface. X-ray diffraction studies were carried out on the IMC layers in the reacted samples after selectively etching away the excess solder. The resulting diffractograms consisted of very strong $(10\bar{1}1)$ $(10\bar{1}2)$ peaks of η-phase (Cu_6Sn_5) when the Sn content was high, at all temperatures. In the low Sn solder (27Sn-73Pb), the η-phase peaks were absent at the two highest temperatures in the present study, but the (2 12 0) ϵ-phase (Cu_3Sn) peak was prominent. Since many major peaks of these compounds listed in JCPDS cards were either absent or small, a crystallographic texture was suspected in the IMC layers. Hence, pole figures were constructed using the conventional texture goniometer. For the η-phase $(10\bar{1}1)$ pole figures, and for the ϵ-phase (002) pole figures were constructed. They confirm a strong texture in these phases normal to the surface of substrate Cu. The growth directions were identified to be $< 101 >$ and $< 102 >$ for η-phase and $< 102 >$ and $< 031 >$ for ϵ-phase. The growth directions do not change with exposure time and temperature although, the layer thickness and morphology undergo substantial changes. The morphology of the η-phase layer varies gradually from a cellular film with rugged interface to a dense film with scalloped interface as the Pb content and temperature increase. The ϵ-phase was dense and planar. It is expected that the textured growth of the IMC layer would give rise to anisotropy in properties such as electrical resistivity and mechanical properties of the joint.

3:15 PM N2.5
COMPARISON OF SOLID STATE AGING AND WETTING REACTION OF EUTECTIC TIN-LEAD AND LEAD-FREE SOLDERS ON COPPER.
T.Y. Lee, W.J. Choi and K.N. Tu, Univ of California-Los Angeles, Dept. of MS&E, Los Angeles, CA; J.W. Jang, S.M. Kuo, J.K. Lin and D.R. Frear, Motorola, Interconnect System Laboratory, Tempe, AZ.

The intermetallic compound (IMC) growth of four different solders - eutectic SnPb, $SnAg_{3.5}$, $SnAg_{3.8}Cu_{0.7}$, and $SnCu_{0.7}$ - on Cu Under Bump Metallurgy (UBM) during solid state aging and wetting reaction was studied. The four solders were reflowed twice on Cu at 240°C for 2 min and followed by solid state aging at 125°C, 150°C and 170°C for 500 hrs, 1000 hrs and 1500 hrs. The morphology and the growth mechanism of the IMC during solid state aging were layer-type and diffusion-controlled growth, respectively. The activation energy was 0.94 (eV) for eutectic SnPb, 1.03 (eV) for $SnAg_{3.5}$, 1.01 (eV) for $SnAg_{3.8}Cu_{0.7}$, and 1.05 (eV) for $SnCu_{0.7}$. However, the activation energy during the wetting reaction was between 0.2 and 0.3 (eV) and the morphology was scallop-type. The growth mechanism was ripening-controlled. The rate of IMC growth is 10^4 times different between the reactions, i.e. 1 μm/min for wetting reaction and 10^{-4} μm/min for solid state reaction. Even though the Gibbs free energy changes per mole at 240°C and 170°C are not significantly different; the rate of Gibbs free energy change is significantly different. Therefore, the scallop morphology during the wetting reaction is stable due to the high rate of Gibbs free energy change, even though the scallop type has much higher surface energy than the layer type. During the solid state reaction, the slow change in Gibbs free energy causes the IMC to change from the scallop type to the layer type.

3:30 PM N2.6
INTERFACIAL PHASE FORMATION IN Sn-Ag-Cu SOLDER JOINTS ON Ni/Au COATED BOARDS.
Kejun Zeng, Vesa Vuorinen, Jorma K. Kivilahti, Helsinki University of Technology, Dept of Electrical and Communications Engineering, Espoo, FINLAND.

Ni(P)/Au coatings have been extensively used as a finish system on PCB pads because Ni coating provides flat and uniform surface and also serves as a diffusion barrier between solder and copper. However, complicated interfacial phenomena between this finish layers and Sn-Pb solder have caused a problem of joint reliability. AuSn4 re-deposits at interface after thermal cycling or aging. Phosphorous is accumulated between Ni-Sn compounds and nickel phosphide. This interfacial structure greatly degrades the mechanical properties of the joints. Pb will be eventually eliminated from electronic products and Sn-Ag-Cu alloy has been considered as the most promising substitute for the Sn-Pb solder. Interfacial reaction of the Sn-Ag-Cu solder with Ni(P)/Au finish on board has been investigated in this work. Transmission electron microscopy and scanning electron microscopy were employed to analyze the interfacial microstructure. The intermetallic compound Cu6Sn5, containing a small amount of Ni, was found to preferentially form on the Ni coating. This compound layer served as a barrier for the reaction of Sn with the Ni coating. On the Ni(P) side, a nickel phosphide was identified. Thermodynamic modeling of the Cu-Ni-Sn system was carried out to rationalize the segregation of Cu at the solder/finish interface. Effects of the interfacial reaction on joint reliability are discussed.

3:45 PM N2.7
FATIGUE AND INTERMETALLIC FORMATION IN LEAD FREE SOLDER DIE ATTACH.
Patrick McCluskey, Craig Hillman, and Zheng Yunqi, University of Maryland, College Park, MD.

With the advent of many new lead-free solder materials, it is important to understand their reliability as die attaches. However, little information is available in the literature on the fatigue properties of thin films of these materials. Such information is critically needed to evaluate the lifetime of power electronic modules. In this paper, we will discuss analytical, semi-analytical, and numerical methods for assessing the fatigue behavior of large area solder die, the use of mechanical testing as a way of determining the fatigue coefficients and the validation of these methods against thermal cycle testing. Furthermore, most of the Pb free solder candidates being considered for moderate to high temperature applications, such as Sn95.5Ag3.8Cu0.7, consist of small amounts of alloying elements added to tin. The abundance of tin assists in surface wetting by promoting intermetallic reaction with the underlying plating materials. However, it is this same tendency of tin to form intermetallics that raises a long term reliability concern with high tin solders. The brittle intermetallic is prone to fracture, especially in the presence of voids created by asymmetric interdiffusion. We will discuss experiments developed to model and address intermetallic reliability concerns.

4:00 PM N2.8
CHARACTERIZATION AND SOLDERING OF ORGANIC SOLUTION MODIFIED ALUMINUM THIN FILMS AND BOND PADS.
Rui Fang, Eric Dahlgren, Matt O'Keefe, Tom O'Keefe, University of Missouri-Rolla, Dept of Metallurgical Engineering and Materials Research Center, Rolla, MO; Wu-Sheng Shih, Brewer Science, Rolla, MO; Dan Gamota, Motorola, Schaumburg, IL.

The use of solder connections on integrated circuits with aluminum bond pads for applications such as direct chip attach, micro ball grid arrays and chip scale packages is increasing. In order to have a wettable surface and reliable solder joint, under bump metallization (UBM) is deposited onto the aluminum bond pad prior to solder deposition. The UBM is usually deposited by blanket film deposition, photolithography and etching, as is the case for copper, or by electroless plating directly onto the bond pads, as is done for Ni/Au. In this study an immersion plating process using organic solutions containing copper and palladium ions were used to deposit a seed layer and activate the surface of thin film aluminum surfaces and bond pads for subsequent electroless copper deposition and solderability tests. It was demonstrated that the copper and palladium particles deposited from the organic solution onto sputter deposited aluminum thin films were able to act as nucleation sites for the subsequent build up of adherent, continuous copper films from formaldehyde and hypophosphite electroless plating baths. In addition, the metal deposition from organic solution process was found to be very selective on patterned test vehicles and integrated circuits as metal deposition

occurred only on the exposed aluminum bond pads and not on passivation layers. Tests were conducted to determine the solderability of the samples after the both organic solution and electroless copper deposition. Results from the studies demonstrate that an adherent solder joint to the aluminum was possible after only organic solution processing and that the solder shear strength of flip chip test die with the selective Cu or Pd organic seed layers and electroless copper UBM could be comparable to standard sputter deposited and etched UBM.

4:15 PM *N2.9
FUNDAMENTAL ISSUES IN ELECTRICALLY CONDUCTIVE ADHESIVES. James E. Morris, State Univ of New York at Binghamton, Dept of Electrical Engineering, Binghamton, NY.

Electrically Conductive Adhesives (ECAs) offer significant advantages over solders for both surface mount and flip-chip interconnect, including no-lead content, improved fine pitch performance, greater compliance, and lower process temperatures leading to lower thermomechanical stress and better reliability. Nevertheless, adoption has been slow, other than for niche applications, with impact resistance remaining the primary obstacle. This paper will review the status of Isotropic Conductive Adhesive (ICA) technology, concentrating on recent research results, and on the new directions they suggest.

4:45 PM N2.10
SIMULTANEOUS MEASUREMENTS OF ELECTRICAL RESISTIVITY AND RAMAN SCATTERING FROM CONDUCTIVE DIE ATTACH ADHESIVES. J. Miragliotta, R.C. Benson, and T.E. Phillips, Johns Hopkins Univ, Laurel, MD; J.A. Emerson, Sandia National Laboratories, Albuquerque, NM.

Silver (Ag)-filled conductive polymer adhesives have been widely used in microelectronic packages due to their lower temperature processing relative to inorganic eutectics. It is known that the development of electrical conductivity in Ag-loaded adhesives is dependent on the thermal profile of the curing process. The chemical reactions at the interfaces of the silver particles during the cure determine the subsequent performance of the conductive adhesive system. The interaction between the Ag particle and its lubricant layer affects the subsequent particle interaction with the polymer adhesive system, other particles, and the electrical contacts on the component or substrate. Therefore, a key to understanding the interfacial properties of the particle, and hence the electrical performance of the conductive polymer, lies in the ability to probe the chemical nature of the Ag surface in an in-situ environment. Despite the importance of the lubricant-coated Ag particle, little attention has been focused on the behavior of the Ag interface under conditions that are consistent with polymer curing. In an attempt to correlate the behavior of adhesive electrical conductivity with the chemical nature of the Ag particle interface, we have simultaneously performed four-point electrical resistivity and surface enhanced Raman scattering (SERS) measurements on commercial conductive adhesives. For SERS, studies have shown that it provides chemical specificity and surface sensitivity to interfacial processes such as adsorption and decomposition. In this study, the SERS investigation focused on the interaction between the lubricant layer and the Ag surface under thermal processing conditions that are employed during the cure of adhesives. Variations in the chemical structure of the lubricant layer and decreases in the resistivity of the adhesive were observed at specific points in the curing, suggesting a correlation between macroscopic electrical conductivity and the chemical composition of the particle interface.

SESSION N3: POSTER SESSION MICROELECTRONICS AND MICROSYSTEMS PACKAGING

Tuesday Evening, April 17, 2001
8:00 PM
Salon 1-7 (Marriott)

N3.1
WETTING AND THERMAL FATIGUE BEHAVIORS OF SnCuAg SOLDER. Flordivino L. Basco and Doris M. Asis, ON Semiconductor Philippines Inc., Carmona, Cavite, PHILIPPINES.

A worldwide demand of eliminating lead in the solder prompted the semiconductor community to look for alternative for SnPb solder and SnCuAg is the best candidate as replacement. Using SnPb as a control, the wetting and thermal fatigue behaviors of SnCuAg is studied. The effectiveness of intermetallic formation of SnCuAg in preplated NiPdAu 20L TSSOP is investigated as a function of time. Impact of increasing the lead counts, comparison of 20L and 48L TSSOP, to thermal yield cycle will be reported also.

N3.2
SYNTHESIS OF DIAMOND COPPER COMPOSITES AS A POTENTIAL CANDIDIATE OF ELECTRONIC PACKAGING MATERIALS. Hui Ma, Michael Ollinger, Rajiv K. Singh, University of Florida, Dept of MS&E, Gainesville, FL.

Thermal dissipation requirements increase as power density is growing. The failure in power electronics is usually caused by temperature increase on the chip and CTE (Coefficient of Thermal Expansion) mismatch between the board and chip. Diamond copper composites were developed to meet the increasing need of fast thermal dissipation because of their high thermal conductivity and good matched CTE to semiconductor devices. The uniform metallic copper coating was carried out on micron diamond particles with electroless deposition technique. Morphology of copper coating was observed by Scanning Electron Microscopy (SEM). The copper coating was confirmed by Energy Dispersive X-Ray (EDX). XRD analysis provides the orientation phase of copper coating on diamond particles. The distribution of copper coating on the diamond particles was characterized with X-Ray mapping. The thickness of copper coating can be obtained by observing the cross section of coated particles with SEM or deriving from results of Inductively Coupled Plasma-Atomic Emission Spectroscope (ICP-AES). Based on the results, ICP is good alternative for estimating coating thickness. Especially for fine particles, weight gain is not practical for investigating coating thickness. The ideal composite composition with CTE matched to Si was calculated in terms of different theoretical models. The cross section of composite pellet was observed by SEM. XRD results show that no impurity has been formed on composite during sintering.

N3.3
DETERMINATION OF A SUBSOLIDUS ISOTHERM IN THE Cu-Sn-Zn SYSTEM. APPLICATION TO Cu/Sn-Zn SOLDER INTERFACE. Alicia Alcaraz, Inst de Tecnologia, Univ Nac de San Martin, Buenos Aires, ARGENTINA; Eduardo Vicente, Luis Gribaudo, Dept Materiales, Com Nac de Energia Atomica, Buenos Aires, ARGENTINA.

Due to health and environmental concerns, new Pb-free solders are being developed for microelectronic packaging applications. In addition, continuing miniaturization of electronic components demands solders with improved properties to substitute commonly used Sn-Pb eutectic alloys. Tin-zinc eutectic alloys are an economic alternative. Copper is the typical substrate metal in electronic technologies, and it can also be added in small quantities to the binary Sn-Zn system to reduce the melting temperature. However, the Cu-Sn-Zn ternary phase is not entirely known. In this work the 180°C isothermal section of the Cu-Sn-Zn system was experimentally determined. Twenty-two alloys were prepared from pure elements. Most compositions lie on the 80 at % Sn isopleth. They were annealed at 180°C for 45 days in an argon atmosphere and then ice-quenched. The samples were examined by optical and scanning electron microscopy, and analyzed by electron-probe microanalysis and X-ray diffraction techniques. No ternary phases were observed in the system. A new subsolidus isothermal section at 180°C is proposed, which is in disagreement with the isotherms calculated at both 160 and 250°C by other authors. These results allow to understand the formation of intermetallic phases at the substrate/solder interface during the soldering process and post-soldering anneals.

N3.4
MECHANICAL PROPERTIES AND FRACTURE BEHAVIOR OF THE Cu AND Cu_6Sn_5-DISPERSED Sn-Pb SOLDER BUMPS PROCESSED BY SCREEN PRINTING. Ho-Seob Cha, Kwang-Eung Lee, Tae-Sung Oh, Hong Ik Univ, Dept of Metallurgical Engineering and Materials Science, Seoul, KOREA; Jin-Won Choi, Package R&D ChipPAC, Ichon, KOREA.

Cu and Cu_6Sn_5-dispersed 63Sn-37Pb solder bump of 760 μm size were fabricated on Au(0.5 μm)/Ni(5 μm)/Cu(27 $\pm$ 20 μm) BGA substrates by screen printing process, and their microstructure and shear strength were characterized with variation of dwell time at reflow peak temperature (220°C) and aging time at 150°C. With the dwell time of 30 seconds at reflow peak temperature, the Cu_6Sn_5-dispersed solder bumps exhibited higher shear strength than the value of the Cu-dispersed ones. With increasing the dwell time longer than 60 seconds, however, shear strength of the Cu_6Sn_5-dispersed solder bumps became lower than that of the Cu-dispersed ones. Shear strength of both Cu and Cu_6Sn_5-dispersed solder bumps was lowered with increasing the aging time at 150°C. The failure surface of the solder bumps could be divided into two regions of slow crack propagation and critical crack propagation, and the shear strength of solder bumps was inversely proportional to the slow crack propagation length.

N3.5
MICROSTRUCTURE AND MECHANICAL PROPERTIES OF THE Sn-Ag SOLDER ALLOY WITH ADDITION OF Bi AND Cu. Kwang-Eung Lee, Ho-Seob Cha, Kwang-Yong Lee, Tae-Sung Oh,

Hong Ik Univ, Dept of Metallurgical Engineering and Materials Science, Seoul, KOREA; Jin-Won Choi, Package R&D ChipPAC, Ichon, KOREA.

Microstructure and mechanical properties of the Sn-Ag solder alloys were characterized with addition of Bi and Cu up to 9 wt% to Sn-3.5Ag composition. Compared to the Bi-added Sn-Ag solder alloys, large amount of second phase and fast growth of second phase were observed in the Cu-added alloys. The Bi-added Sn-Ag solder alloys exhibited higher yield strength and higher ultimate tensile strength than those of the Cu-added alloys. With addition of 1∼9 wt% Bi and Cu, the yield strength of the Sn-3.5Ag solder alloy increased from 20 MPa to 50 MPa and to 36 MPa, respectively. The melting temperature of the Sn-3.5Ag solder alloy decreased from 221°C to 210°C and to 217°C with addition of 9 wt% Bi and Cu, respectively. In this study, Bi and Cu-added Sn-Ag solder bumps of 760μm size were also fabricated on the Au(0.5 μm)/Ni(5 μm)/Cu(27 $\pm$ 20 μm) BGA substrates, and their microstructure and shear strength were characterized with variation of the dwell time at reflow peak temperature (220°C).

N3.6
NEW STEPPED PROCESS AND MATERIALS FOR CHIP BONDING TECHNOLOGY OF NONRIGID AND FLEXIBLE SUBSTRATES. Sung Kyu Park, Jeong In Han, Won Keun Kim and Min Gi Kwak, Electronics Devices Research Center, Korea Electronics Tech. Inst., Pyungtaek Kyunggi, KOREA.

Reliable interconnection of electrodes to the plastic-based display with anisotropic conductive films (ACFs), of which the conductive particles were similar in elasticity to the substrates, was accomplished. The contact resistance value was maintained even while the junction was stressed under sudden changes in temperature and pressure. It was found that the conduction failure was caused by the action of a complex mechanism on the changes of a joint structure from investigation of scanning electron microscope (SEM) images and other experiments. The major driving factor seems likely to be defects in the transparent electrodes due to the thermal strain of substrates and penetration of conductive particles. Conductive particles with elasticity similar to that of the plastic substrates did little damage to the transparent electrodes on the substrates, and low temperature and pressure under a stepped process did not bring about their deformation either. As a result, a highly reliable interconnect with a very low contact resistance (20-25Ω) was realized. In addition to these reliable interconnect, we analyzed the relationship of conductive particle size and bump area on contact resistance for these substrates. Finally, a prototype plastic film LCD module was fabricated using a driver IC chip and a polycarbonate-based super twisted nematic (STN) LCD panel to confirm whether the module could be realized in accordance with our experimental results.

N3.7
USING THE SURFACE POTENTIAL DECAY METHOD TO PROBE ELECTRICAL CONDUCTION IN EPOXY RESINS USED FOR PACKAGING. Alain Sylvestre, Patrice Gonon, Lab for Electrostatics and Dielectric Materials, University of Grenoble, FRANCE.

Transverse and longitudinal conductivities quantify the aptitude of materials to neutralize an electric charge deposited on their surface. The method which is usually used to determine these conductivities consists in contacting electrodes on the material, applying a voltage and measuring the resulting current. This method presents some difficulties related to the contact of electrodes with the insulator. Moreover, the voltage cannot be very weak if one wants to obtain a measurable current and, if the voltage is high, electric discharges can be occur at the edges of the electrodes. Another difficulty is to separate the capacitive current from the conduction current corresponding to the flow of the charges in the electric field. Another way to reach these characteristics is the Surface Potential Decay (SPD) method. An electric charge is deposited on the surface by corona discharge. The surface takes a potential which will change in time, the charge flowing out either through the surface or the volume. The SPD is measured by an induction probe. The interest of this method lies in the absence of electrode on the upper face of the sample, as well as in the absence of high voltage source. In this work, we present the potentialities of this method to investigate insulating materials, in particular epoxy resins used for packaging. We emphasize the influence of electrical and thermal stresses on the conductivities in these materials and we investigate the importance of relative humidity on these properties.

N3.8
Abstract Withdrawn.

N3.9
PACKAGING FOR A SENSOR EMBEDDED IN CONCRETE. Russell Paul Cain, Bliss G. Carkhuff, Kenneth R. Grossman, Rengaswamy Srinivasan, Frank B. Weiskopf Jr., Johns Hopkins University, Applied Physics Laboratory, Laurel, MD.

The Johns Hopkins University Applied Physics Laboratory is developing packaging for a sensor platform to be embedded in the harsh environment of concrete structures for monitoring corrosion-related degradations over extended periods of 25 years or more. The United States is replacing aging infrastructure and simultaneously developing the tools and techniques to monitor new infrastructure as it ages. JHU/APL has analyzed the sensing requirements for infrastructure monitoring, especially bridge deck monitoring, and developed a concept based on distributed, embedded sensors. The Wireless, Embedded Sensor Platform (WESP) will implement the concept of a low-cost, customizable, sensor platform suitable for long-term performance in the field. The WESP is designed to be powered and queried remotely as often as required and can be used to map the time evolution of the structural degradation The objective of this research and development is to design, implement, and demonstrate packaging techniques for embedded sensor suites commensurate with a 50-year lifetime embedded in concrete that is at a pH >13, and exposed to harsh environments of salt, moisture, mechanical, and thermal stress. The sensor and communications design for such a system is being developed in parallel with the packaging and reliability efforts. To meet this objective, the WESP construction will use a commercial ceramic IC packaging and unique manufacturing and assembly techniques. The prototype is expected to provide sensor identification, temperature, pressure, and conductivity data within a package volume less than 2 cm^3 (0.2 in^3). Reliability tests will be conducted to evaluate the performance of the packaging design. These include such tests as freeze/thaw cycling, thermal shock, thermal cycling, HASP, 85/85, and accelerated life testing. Future developments will implement additional sensor types to fully characterize the concrete environment.

N3.10
ELECTROMIGRATION IN LEAD FREE AND EUTECTIC TIN-LEAD SOLDER POWER FLIP CHIPS. Patrick McCluskey, Dhiraj Bansal, University of Maryland, College Park, MD.

The automotive industry has used flip chip for many years as a high density interconnection method in hybrid power modules. With the advent of lead free solder, there is considerable interest in determining the relative electromigration resistance of lead free solder flip chip bumps with respect to tin-lead eutectic bumps, especially at the high current densities needed to supply the levels of power required for automotive applications. This study focused on the relative susceptibilities and underlying material processes leading to electromigration failure of 63Sn37Pb eutectic solder and a lead free solder. To conduct the study, sample boards were constructed consisting of daisy chained flip chip die, 0.25 inches on a side, attached with one of the two materials. Half of the samples of each solder material were powered so a current density of 6100 A/cm^2 was maintained through each sample and the other half were left unpowered. All the samples were subjected to a high temperature lifetime test so that a junction temperature of 150°C was achieved, and any change of resistance of the samples was monitored in situ. The lead free solder investigated was found to have a longer mean time to failure than its eutectic tin-lead counterpart. However, the mode of failure for eutectic tin-lead solder was found to be a slow and steady increase in resistance as opposed to a sudden and complete electrical open for lead-free solder. The presence and size of initial voids in the solder bumps did not have a substantial effect on the rate of failures in both the solders. This presentation will discuss these findings and provide detailed information on the mechanism of failure.

SESSION N4: MICROSYSTEM PACKAGING
Chairs: J. C. Boudreaux and Howard R. Last
Wednesday Morning, April 18, 2001
Golden Gate A3 (Marriott)

8:30 AM *N4.1
MEMS PACKAGING: OPPORTUNITIES AND CHALLENGES. Aicha Elshabini, Univ. of Arkansas, Electrical Engineering Dept., Fayetteville, AR.

MicroElectroMechanical Systems (MEMS) are rapidly evolving into an important and promising technology. The ability to fabricate switches, micro pumps, sensors, and an array of actuators that can perform unique and complex functions in very compact form factors is an exciting prospect. Potential target electrical applications include; T/R switches in wireless and microwave products, phase shifters, tunable filters, and tunable oscillators. However, a key challenge is the packaging of these devices. Conventional packaging techniques such as plastic encapsulation are generally not suitable for these devices, since

the encapsulant would restrict the movement of the internal mechanical components. In addition, a wide range of new problems, that had not previously been faced, arise due to the novel nature of these devices. Some of these problems include; the dicing of MEMS in a manner that does not damage the structures, creating less heat and stress on the wafer, and generating less particles, manipulation of the diced components without damaging the fragile mechanical structures, mechanical and fluidic feed through to the outside world, as well as the lubrication of moving parts, in order to facilitate the production of a more durable and reliable product. This paper will provide a brief overview of MEMS devices as well as a detailed evaluation of the state of the art MEMS packaging techniques. In addition, key problems in MEMS packaging will be highlighted and potential solution will be discussed.

9:00 AM N4.2
INNOVATIVE MEMS AND MOEMS PACKAGING CONCEPTS.
Ken Gilleo, Cookson Electronics, Foxboro, MA.

More than 2-decades old, Micro-Electro-Mechanical Systems (MEMS) paradoxically began to generate tremendous interest just as we entered the new millenium. Traditional MEMS is widely deployed in airbag triggering accelerometers and made-by-the millions ink jet printer cartridges. But it is the emerging advanced MEMS that piques interest. This is because MEMS represents the single point of technology convergence where electronics, mechanics, physics, chemistry and biology can all be merged on a single slice of silicon. Now add optics and we move up to MOEMS; micro-opto-electro-mechanical systems where "magic mirrors" beam the digital cinema onto theater screens or route a rainbow of data-rich photons for the new, glass Internet super-highway. But the all-important package has been left behind relegated to an insignificant afterthought. Yet failure to invent a cost-effect MEMS/MOEMS packaging system will surely limit the advance of these wonderful 21st century technologies. The cost-burdened classical hermetic package is only a short-term solution for many of the applications. New and innovative packages have been proposed and several have already been built. Some propose to enable photonics using glass caps while others use minimal chips on glass chip carrier platforms. Some are near hermetic, but use "getters" to extend life even for critical optical mirror products. This paper will describe the newest design concepts for MEMS/MOEMS and provide a status report on specific packages already built for this technology. Several newer package-enabling materials will also be discussed that include getters and vacuum-deposited anti-stiction agents. Tune in and participate in the Grand Convergence of Technologies.

9:15 AM *N4.3
MATERIAL SYSTEM FOR PACKAGING 500°C SiC MICRO-SYSTEM. Liang-Yu Chen, AYT Research Corp./NASA Glenn Research Center, Cleveland, OH; Robert S. Okojie, Philip G. Neudeck, Gary W. Hunter, NASA Glenn Research Center, Cleveland, OH.

A systematic packaging technology for high temperature microsystems is essential for both in situ testing and commercialization of high temperature microsystems. Core technologies needed for high temperature electronic packaging are electrical interconnections and die-attach. Aluminum nitride and aluminum oxide were selected as packaging substrates and precious metal thick-film materials were selected for electrical interconnection system (thick film printed wires and thick film metallization based wire-bond) and conductive die-attach interlayer for high temperature application. This approach has shown promise. During a 2000-hour test in atmospheric oxygen with and without electrical bias, the electrical resistance of thick-film based interconnection system demonstrated both low and stable electrical resistance at 500°C. A silicon carbide (SiC) Schottky diode was attached to ceramic substrate using gold thick-film material as the conductive bonding layer and was successfully tested at 500°C in air for more than 1000 hours. These results indicate that the ceramic substrates and thick-film metallization based interconnection system and die-attach scheme provide a material framework for packaging 500°C operable SiC microsystems. In addition to a general packaging design for SiC electronics and sensors, robust hermetic and non-hermetic packaging for absolute and differential SiC pressure sensors will be discussed with specific packaging requirements. Engine performance parameter monitoring sensors such as pressure sensors must be thermally stable and functionally reliable during their operational life which heightens the demands on the reliability of their packaging. These requirements include reliable contact metallization (on the SiC chip) and the ability to reduce thermomechanically induced stress. High temperature, high power device and gas sensor packaging will also be discussed in parallel. Progress in this area will be presented.

10:15 AM *N4.4
CARRIER-LEVEL PACKAGING AND RELIABILITY OF A MEMS BASED SAFETY AND ARMING DEVICE. Rajesh Swaminathan, Peter Sandborn, CALCE Electronic Products and Systems Center, University of Maryland, College Park, MD; Michael Deeds, Naval Surface Warefare Center, Indian Head, MD.

The carrier-level packaging for a MEMS based Safety and Arming (S&A) system has been considered. The package houses the S&A chip, initiator chip, and a deflection delimiter. The carrier-level package provides traditional electrical, fiber optic, pressure, and explosive interconnects. The S&A chip contains a moving "slider" that either exposes a hole through the chip or blocks the hole, as well as various environmental sensors and actuators that lock the slider into a safe position. The initiator chip converts electrical energy to mechanical energy upon demand to initiate the explosive train. The delimiter is placed between the S&A chip and the initiator chip to restrict out of plane movement of the MEMS structures. Various delimiter technologies and carrier approaches/materials have been assessed. The carrier designs include hermetic, non-hermetic, and breathable packages. The impact of moisture ingress and egress from the carrier packaging have been studied as a function of the performance of MEMS parts.

10:45 AM *N4.5
AMBIENT GAS ANALYSIS OF HERMETIC ENCLOSURES.
Robert K. Lowry, Intersil Corporation, Analytical Services Laboratory, Melbourne, FL.

Hermetically sealed enclosures for microelectronic, MEMS, and optoelectronics devices and associated components may contain gaseous species that can ultimately endanger the functionality of the system. Condensates of moisture and/or ammonia, especially in conjunction with ionic impurities, can cause metals to corrode, resulting in electrical opens in conductor lines or contacts. Atomic oxygen can oxidize and cause mechanical failure of solders or damage to other oxidation-prone materials within the enclosure. Military specifications impose concentration maxima for these two species in sealed package cavities of 5000 ppmv and 2000 ppmv, respectively. While there are no specified maximum limits for other volatile species, condensates of organic substances that volatilize from adhesives or other hydrocarbons may form residual deposits that interfere with proper mechanical operation of gears or other moving parts. In optoelectronic systems, condensates of moisture or volatile organics may cloud mirrors and degrade performance. Hydrogen is a rapid diffuser that can degrade MOS device function. Argon has been reported to cause arcing in high-power RF hybrid packages. Otherwise, argon and other gases such as carbon dioxide and helium, are not known to adversely affect mechanical or electrical device operation, but their detection can provide clues to packaging materials behavior and overall physical and mechanical integrity of the enclosure. Knowing the ambient gas composition of hermetic device enclosures assists in selecting high quality package materials and enables hermetic sealing process control to assure reliable products. This paper describes the analysis method for hermetic enclosures, known as Residual Gas Analysis (RGA). It discusses materials and sealing practices that are possible sources for the gaseous species which may endanger sealed product reliability. It gives material selection and process improvement guidelines to reduce and control volatile species in hermetic enclosures.

11:15 AM N4.6
IMPLEMENTATION OF A LOW TEMPERATURE WAFER BONDING PROCESS FOR ACCELERATION SENSORS.
M. Wiemer, T. Gessner, Fraunhofer Institute Reliability and Microintegration, Department Micro Devices and Equipment, Chemnitz, GERMANY; K. Hiller, Chemnitz Univ of Technology, Center of Microtechnologies, Chemnitz, GERMANY; K. Kapser, H. Seidel, TEMIC TELEFUNKEN microelectronic GmbH, Munich, GERMANY; J. Bagdahn, M. Petzold, Fraunhofer Institute for Mechanics of Materials, Halle, GERMANY.

Waferbonding technologies are used for the fabrication and packaging of micro mechanical devices in bulk and surface micro machining. A special low temperature bond process was integrated into the technological process flow to produce an acceleration sensor fabricated by TEMIC TELEFUNKEN microelectronics GmbH. Detailed investigations should show to which extent the low temperature bonding process is able to replace an anodic bonding process between pyrex and silicon. The reason for this wafer substitution was the measured offset sensor values caused by the different expansion coefficient of the glass bottom wafer and the silicon middle wafer. The implementation of the low temperature wafer bonding process which should be used requires special surfaces quality of the process wafers. It was found that the most important parameters are the surface silicon or silicon oxide roughness as well as the surface contamination caused by the technology process steps before the bonding step. In the paper a low temperature bonding process used with an oxygen plasma pre-treatment followed by 400°C anneal will be explained and the results of infrared transmission as well as the measured bond

strengths of the prepared test wafers will be plotted. First dicing tests have shown that the new bonding process has the potential to replace the glass wafers. During the development of this bonding process it was shown that it is possible to reach a bond strength between 1.8 J/m^2 and 2.4 m^2 depending on the annealing time. To optimize the necessary size of the bond frame and the bond strength a test pattern was designed with different sizes of bond frames, mesa structures and chevron notch structures. These structures are used to qualify the bond results concerning the bond strength and bond reproducibility depending on the process technology and sensor design. The results of these investigations are represented in the paper.

11:30 AM N4.7
COMPARISON OF YIELD STRENGTH OF AMORPHOUS DIAMOND FILMS MEASURED BY TENSILE TESTING AND NANOINDENTATION. T.A. Friedmann, D.A. Lavan, T.M. Alam, P.G. Kotula, J.P. Sullivan, R.J. Hohlfelder, M.P. de Boer, C.I.H. Ashby, M. Mitchell, Sandia National Laboratories, Albuquerque, NM.

Amorphous-Diamond (a-D) thin films deposited by pulsed-laser deposition typically have high levels (6-10 GPa) of residual stress. This stress is thought to be intrinsic to the deposition process, but is not intrinsic to hard (> 85 GPa) a-D films, since thermal annealing to moderate temperatures (600°C) can completely remove the stress without significantly changing the 4-fold carbon content. We have taken advantage of these low stress a-D films to create true surface micromechanical structures (MEMS). We have fabricated cantilever beams, tensile pull tabs, notched beam pull tabs, and friction test structures to evaluate the micromechanical properties of these films. Tensile test results were obtained by using a nanoindentor to pull laterally on the samples till fracture occurred. The a-D fracture strength was found to be > 8 GPa, much higher than CVD diamond films (~1 GPa), but lower than the yield strength (75 GPa) derived from traditional nanoindentation measurements. The reason for the difference in strength is presumably due to defects that serve as stress concentrators for crack initiation. Obvious candidates for defects in this system are particulates inherent in the deposition process and imperfections introduced due to imperfect device processing. In this amorphous material, defect characterization is difficult but results of SEM, TEM, cross-section EELS, and 13C NMR experiments will be employed to attempt to relate defects and nanostructure with the observed fracture strength. *This work was supported by the U.S. DOE under contract DE-AC04-94AL85000 through the Laboratory Directed Research and Development Program, Sandia National Laboratories.

11:45 AM N4.8
FATIGUE EFFECTS IN SINGLE CRYSTAL SILICON FOR MEMS APPLICATIONS. E.D. Renuart, Stanford Univ, Dept of Materials Science and Engineering, Stanford, CA; A.M. Fitzgerald, Sensant Corporation, San Jose, CA; T.W. Kenny, Stanford Univ, Dept of Mechanical Engineering, Stanford, CA; R.H. Dauskardt, Stanford Univ, Dept of Materials Science and Engineering, Stanford, CA.

MEMS devices may experience significant alternating loads during service, associated with both applied and vibrational loading. Long-term reliability and lifetime predictions require a careful study of possible fatigue mechanisms in these structures. Although silicon is not generally considered susceptible to fatigue crack growth, recent studies suggest that there may be fatigue processes in silicon MEMS structures. The effect, however, has still not been extensively studied. In this work, we used a micro-machined compressive double cantilever beam specimen geometry to examine stable crack growth. Crack growth tests were performed under displacement control under both static and cyclically varying loads. Due to the high compliance of the sample structure, the loads changed only minimally with crack growth. Fatigue crack-growth tests were performed at an applied loading frequency of 20 Hz. A titanium thin film was sputtered onto the side face of the sample to accurately measure crack growth from changes in electrical resistance. The crack length and loads were monitored throughout the test in order to distinguish between the role of possible environmentally assisted crack-growth (stress corrosion) processes and mechanically induced fatigue mechanisms. Implications for devices reliability will be discussed.

SESSION N5: HIGH TEMPERATURE, HIGH POWER PACKAGING

Chair: F. Patrick McCluskey
Wednesday Afternoon, April 18, 2001
Golden Gate A3 (Marriott)

1:30 PM *N5.1
NOVEL MATERIALS AND JOININGS FOR POWER ELECTRONICS MODULE PACKAGING. Eckhard Wolfgang, Gerhard Mitic, Guy Lefranc, Herbert Schwarzbauer, Siemens AG, Corporate Technology, Munich, GERMANY.

Power module packages consist of several layers of different materials according to their function. A base plate is necessary for mounting the module to the cooling unit, an insulating layer is needed for protection against high voltages, the power semiconductor chips having metal electrodes on both sides are used for switching currents, and finally passivation layers have to protect chips against high electric fields and environmental impacts. The combination of semiconductors, metals and insulators and their different coefficients of thermal expansion leads to stresses and fatigues during temperature excursions. There are some major trends which require the use of new materials and joinings: Higher voltages (up to 6.5 kV), higher currents (above 2000 A), and higher operating temperatures, e.g. in automotive applications (up to 200°C). To reduce the influence of the thermal mismatch between the base plate and the insulator (Alumina, AlN) metal matrix composites like AlSiC are used since a few years in power modules. To realise a higher thermal conductivity and a easier joining technique CuSiC samples were prepared and investigated. First results will be presented. To minimise the partial discharge of the substrate several passivation materials like amorphous Si and Ba titanate in epoxy resins were tested at high voltages up to 15 kV. For joining the MMC base plate and the Si chips to the ceramic substrate a low temperature joining technique - using Ag powder under high pressure - can be used which turns out to be reliable at temperatures up to 200°C.

2:00 PM *N5.2
A NOVEL PACKAGING CONCEPT FOR HIGH POWER PRESSPAK IGBT MODULES. E. Herr, S. Kaufmann, T. Lang, R. Schlegel, ABB Semiconductors AG, Lenzburg, SWITZERLAND.

Ceramic packaging has been the standard technology for bipolar high power devices such as diodes, thyristors and GTOs. High power IGBTs (Insulated Gate Bipolar Transistor) are more and more replacing thyristors and GTOs for high power applications. They are commercially available as multi-chip modules in plastic packages and as PressPak devices in ceramic packages. A novel packaging concept for high power IGBTs will be presented in this paper, using plastic packaging for PressPak devices, thus combining the advantages of the two available packaging technologies. It will be demonstrated that a considerable number of requirements and constraints severely narrow the choice of materials that can be used. High power devices are mostly used in harsh environments. At the same time, the useful life of the components is required to be 20 - 30 years. Most critical for proper device performance and good reliability are housing materials, molding compound, and contact materials. It will be explained how these materials were selected and qualified for the use in IGBT high power devices.

2:30 PM N5.3
A DIMPLE-ARRAY INTERCONNECT TECHNIQUE FOR POWER SEMICONDUCTOR DEVICES. Simon S. Wen, Dan Huff, Guo-Quan Lu, Virginia Polytechnic Institute & State Univ, Center for Power Electronics Systems and Dept of MS&E, Blacksburg, VA.

This paper describes a wireless-bond interconnect technique, termed Dimple-Array Interconnect (DAI) technique for packaging power devices. Electrical connections onto the devices are established by soldering arrays of dimples pre-formed on a metal sheet. Preliminary experimental and analytical results demonstrated potential advantages of this technique such as reduced parasitic noises, improved heat dissipation, as well as lowered processing complexity, compared to the conventional wire bonding technology in power module manufacturing. Thermo-mechanical analysis using thermal cycling test and FEM were also performed to evaluate the reliability characteristics of this interconnect technique for power devices.

2:45 PM N5.4
AN INVESTIGATION OF LEAD FREE AND BROMINE FREE TECHNOLOGIES FOR MEDIUM POWER SEMICONDUCTOR PACKAGING. Pamela Dugdale and Arthur Woodworth, Assembly R&D, International Rectifier GB, Surrey, UNITED KINGDOM.

Over recent years there has been a growing interest in the removal or substitution of Lead, Bromine and other hazardous chemicals from electronic and electrical equipment. This relates primarily to products whose end of life disposal relies on the use of landfill sites or increasingly on recycling. The driving forces for these changes come from both legislation, such as that proposed by the European Union, and also from consumer awareness. The implications of the move towards more environmentally friendly electronics extend right down the level of discrete component packages including those produced in large numbers by the Power Semiconductor Industry. In the present paper the technical challenges associated with the development of a lead and bromine free Medium Power Packaging are discussed and the results of ongoing investigations are presented. The major challenges in this area relate not only to the substitution of key elements but also to ensuring compatibility with the higher reflow temperatures

which may be associated with Pb-free surface mount processing. This raises particular issues with respect to the die attach material, which is often a high Pb soft solder; the encapsulation compounds which tend to rely on Bromine and Antimony compounds for their flame retardant properties; and the device plating which must be compatible with Pb-free board attach solders.

3:30 PM *N5.5
PACKAGING ISSUES OF ELECTRONIC DEVICES FOR HIGH-TEMPERATURE APPLICATIONS. W. Wondrak, A. Boos, K. Merkel, and W. Schaper, Daimler-Benz AG, Power Semiconductor Devices, Frankfurt/Main, GERMANY.

In automotive industry, many innovations are enabled by electronic control. Mechatronic applications like in transmission or combustion control will require increased junction temperatures up to 200°C. Temperature has a strong impact on device performance and reliability. In addition to temperature-accelerated sensitivity of electronic devices to electrical stresses, thermo-mechanical stress and humidity are major damage sources. Due to the high cost pressure in car production, reliable device operation has to be fulfilled with cost-effective technologies. Therefore, the availability of organic molding compounds suited for harsh environments is a real need.
In this paper, different molding compounds and die attach systems were evaluated for high-temperature use. Comparison with commercial components was performed as a reference.
The test vehicles were plastic packaged power MOSFETs. Measurements after thermal shock tests and after pressure cooker tests (PCT) were conducted to give informations on the failure modes and reliability at accelerated temperatures.
Failure investigations were made by optical inspection, electrical measurements, scanning acoustic microscopy (SAM) and cross-sectioning. Two types of delamination could be observed. The first type of delamination is between the metal plane and the plastic and is present on all devices tested. The second type of delamination is associated with the die attach.
Commercial power MOSFETs in plastic packages off-the-shelf can be operated at temperature levels of 200°C. They withstand a number of thermal cycles without severe electrical degradation, but the lifetime is not sufficient for automotive applications.
The different types of molding materials (ECN, biphenyle, MfR, silicone) used for device encapsulation in this work have glass transition temperatures Tg ranging from 120 to 180°C. The occurrence of delaminations was correlated with Tg and thermal expansion coefficients. In contrast to expectation, it was found, that a higher Tg does not necessarily mean better high-temperature capability.
In order to meet future automotive demands, new molding materials and/or adhesion-promoting layers are strongly requested. For materials developments, thermomechanical stress taking into account the leadframe material must be reduced and improvements in adhesion strength are necessary.

4:00 PM N5.6
MECHANICAL BENDING FATIGUE RELIABILITY AND ITS APPLICATION TO AREA ARRAY PACKAGING.
Andrew F. Skipor, Motorola, Motorola Lab's Advanced Technology Center, Schaumburg, IL; Larry Leicht, Motorola, Personal Communications Sector, Component Interconnect Technology Center, Libertyville, IL.

The means to model and characterize the thermal cycling reliability of area array packaging is fairly well understood. Thermal cycling reliability of an electronic package is for the most part driven by mismatch in the thermal coefficients of expansion and change in temperature. However as portable products become smaller and lighter, the micro-electronic assemblies within these products can become more compliant, in part due to decreased laminate thickness, therefore the greater potential of bending the printed circuit boards (PCB). In addition, smaller products necessitate the need for greater packaging density such as plastic ball grid array and chip scale packaging. Assemblies comprising of more compliant PCB's and smaller interconnects have been found to be sensitive to low frequency isothermal mechanical flexural fatigue. For example, when a keypad is depressed, the PCB bends resulting in stressing the interconnect. The modes of failure for mechanical flexural fatigue were found to be different than those of thermal fatigue. A methodology to assess and the means to model the interconnect reliability of isothermal mechanical bending fatigue of area array package interconnects has been developed. The methodology has been applied to 1.0 mm pitch plastic ball grid array and 0.8 mm pitch chip scale packages assembled to PCB's. The fatigue fracture morphology, its relation to solder joint location and crack propagation will be discussed at length. Finite element analysis of ball grid array and chip scale packages subjected to mechanical bending was found to correlate to experimental results. The experimental modes of failure have been correlated to field failure data. All in all, the details of the mechanical bend fatigue methodology, fatigue fracture morphology, and theoretical finite element analysis prediction results of area array packaging will be presented.

4:15 PM N5.7
INVESTIGATION OF MECHANICAL STRESSES IN UNDERLYING SILICON DUE TO LEAD-TIN SOLDER BUMPS VIA SYNCHROTRON X-RAY TOPOGRAPHY AND FINITE ELEMENT ANALYSIS. J. Kanatharana, Research Institute for Network and Communications Engineering (RINCE), School of Electronic Engineering, Dublin City University, Dublin, IRELAND; J.J. Pérez-Camacho, T. Buckley, Intel Ireland Ltd., Leixlip, Co. Kildare, IRELAND; P.J. McNally, RINCE, School of Electronic Engineering, Dublin City University, Dublin, IRELAND; T. Tuomi, Optoelectronics Laboratory, Helsinki University of Technology, FINLAND; A.N. Danilewsky, Freiburg, GERMANY; M. O'Hare, D. Lowney, W. Chen, RINCE, School of Electronic Engineering, Dublin City University, Dublin, IRELAND.

Solder based flip-chip packaging has prompted interest in many integrated circuit (IC) packaging applications due to its many advantages in terms of cost, package size, electrical performance, input/output density, etc. The ball grid array (BGA) is one of the most common flip-chip packaging techniques used for microprocessor applications. However, mechanical stresses induced by the flip-chip process can adversely impact on the reliability of production. White beam synchrotron x-ray topography (SXRT), a non-destructive technique has been employed to investigate the spatial extent of strain fields imposed on the underlying silicon substrate for Intel Pentium III microprocessors due to the elevated temperature fabrication steps in a lead-tin solder bump process for BGA packaging. Large area and section back-reflection SXRT images were taken before and after a simulation of the reflow process at 350°C in atmosphere. The presence of induced strain fields in the Si substrate due to the overlying bump structures has been observed via the extinction contrast effect in these x-ray topographs. In addition, orientational contrast effects have also been found after the reflow process due to the severe stresses in the underlying silicon beneath the lead bumps. The estimated magnitudes of stress perpendicular to the Si surface imposed on the underlying silicon were calculated to be in the range 43-97 MPa. The spatial strains in the underlying silicon were relieved dramatically after the lead bumps were removed from the wafer, which confirms that the bumps are indeed a major source of strain in the underlying Si. Finite element analysis (FEA) has also been performed in 2-D plane stress mode. The magnitudes and spatial distribution of the stresses after the reflow process are in good agreement with the SXRT results.

4:30 PM N5.8
PREDICTION OF LATERAL AND NORMAL FORCE-DISPLACEMENT CURVES FOR FLIP CHIP SOLDER JOINTS.
Daniel Wheeler, Daniel Josell, James A. Warren, William E. Wallace, Materials, NIST, Gaithersburg, MD; Adam C. Powell, Department of MS&E, MIT, Cambridge, MA.

We present the results of experiments and modeling of flip-chip geometry solder joint shapes under shear loading. Modeling, using Surface Evolver, included development of techniques that use an applied vector force (normal and shear loading) as input to determine a vector displacement of the pads connected by the solder joint (standoff height and misalignment). Previous solutions solved the converse problem: fixed displacements used to determine required applied force. Such solutions were inconvenient for applications, where the applied force (chip weight) is known. Also, for geometric and materials studies of solder joint shapes involving multiple parameters, determining the equilibrium displacement from applied force by bracketing solutions could become computationally expensive. Using force as the input, the code developed here eliminates these difficulties. It also models wetting beyond the pad onto the surrounding substrate. Measurements of solder joint standoff height and misalignment as functions of the applied force (normal and shear), solder volume and pad diameter are presented. Experiments were carried out for solder ball diameters from 15 mil (0.029 mm^3 volume) to 6 mil (0.0019 mm^3 volume) on pads of diameter 0.64 mm and 0.35 mm. Conditions studied include where the solder remained fully on the pad, extruded beyond the pad under no shear force, and extruded beyond the pad only for sufficiently large values of applied shear force. Measured standoff heights were as small as 20 microns and shear displacements (misalignments) in some of the experiments approached the pad diameter. Fitting of simulation to experimental results gave optimised values for the contact angle and surface tension of the solder. Consistency of the optimal value of the contact angle with the independently measured value as well as the optimal surface tension with literature values confirm the usefulness of capillary based codes at these length scales under these experimental conditions.

SESSION N6/L10: JOINT SESSION
METAL/POLYMER ADHESION IN
CHIP PASSIVATION AND PACKAGING
Chairs: F. Patrick McCluskey and Reinhold H. Dauskardt
Thursday Morning, April 19, 2001
Golden Gate B2 (Marriott)

8:30 AM *N6.1/L10.1

CHEMISTRY AT METAL/POLYMER INTERFACES FOR ELECTRONICS. R.L. Opila, Bell Labs, Lucent Technologies, Murray Hill, NJ.

Interfaces between metals and polymers are of increasing importance in electronics. Applications that use polymers include electronics packaging, Cu and low-k dielectrics, and displays that utilize semiconducting polymers. We have used electron spectroscopy to study chemical reactions between a variety of metals (Cu, Ti, Ta, Cr, Al) and polymers (polyimide, PPV, and various low-k dielectrics). While greater metal reactivity with the polymer may yield greater initial adhesion, often the reliability degrades with time. In addition, adhesion is only one of the factors that must be considered-the role of barrier layers as conductors and/or diffusion barriers must also be considered. Great insight into the chemistry of these systems has been gained by studying the adsorption of metals onto thiol-based self-assembled monolayers on Au. We have used novel applications of photoelectron spectroscopy and x-ray absorption spectroscopy to study evolution of the buried interfaces, and thus the long-term performance of the system. Extensions of these studies to contacts with semiconducting polymers will be discussed.

9:00 AM N6.2/L10.2

ESTIMATION OF THE INTERFACIAL FRACTURE ENERGY OF METAL/POLYMER SYSTEM IN MICROELECTRONIC PACKAGING. J.Y. Song, S.I. Cho, Jin Yu, Center for Electronic Packaging Materials, Korea Advanced Institute of Science and Technology, Taejon, KOREA.

In the microelectronic packaging, reliability of the metal/polymer interfaces is an important issue and many test methods have been used to measure the adhesion strength of the interfaces. In the present work, we measured the adhesion strength of flexible two layer tapes made of Cu/Cr/Polyimide(PI) using the T peel test. The steady state peel strengths(P) were measured along with the peel angle and maximum root curvatures(K_B) behind the peel front, which were directly measured by using an optical camera. Then, effects of the biased rf plasma pretreatment and the metal layer thickness on the T peel strength were investigated, and the energy dissipated by plastic bending(Ψ) were deduced based on the elastic/plastic analysis and measured root curvatures. The interfacial fracture energy(Γ) was the subtraction of Ψ from P. It was found that the peel strength and the plastic bending work increased with the rf plasma power density(ρ) and then saturated. And the same was true of Γ. With the metal layer thickness, P and Ψ showed maximum due to the balance between crystal volume effect and compliance effect, however, interfacial fracture energy, Γ= P - Ψ, was more or less independent of the metal layer thickness, suggesting it to be an interface material parameter. The interfacial fracture toughnesses of the Cu/Cr/PI interface were measured using fracture mechanics specimens and compared to the interfacial fracture energies deduced from the T peel test. Another method used to measure the interfacial fracture toughness of the Cu/Cr/PI interface was the nanoindentation test using the W superlayer sputter-deposited on Cu film, which induced the interfacial delamination. Effects of the W superlayer thickness and residual stresses in the Cu and W films on the interfacial fracture toughness were also investigated.

9:15 AM N6.3/L10.3

FINITE ELEMENT ANALYSIS OF COPPER ADHESION TO POLYMER ENCAPSULANT. Flordivino Basco, ON Semiconductor Philippines, Inc., Technical Operations Department, Carmona, Cavite, PHILIPPINES.

Finite element analysis is used to analyze the button shear test. Through the use of experimental data the adhesion strength of interfaces involved in test are characterized. It was found that adhesion strength of each interface could be characterized by dimensionless parameter. The parameter is used to understand the delamination occurring in the interface of the encapsulating molding compound (EMC) and the back of the die flag (BDF), which is made of copper. Through this adhesion strength of the EMC-BDF interface is identified and compared with saturated vapor pressure to see if the interface will delaminate at a given reflow temperature. Furthermore, the adhesion strength of the intervening layer of oxide is identified, which is very difficult to do in actual experiment.

9:30 AM N6.4/L10.4

ADHESION MECHANISMS OF SILANE ADHESION PROMOTERS IN MICROELECTRONIC PACKAGING. Maura Jenkins, Jeffrey Snodgrass, Gretchen DeVries, Reinhold H. Dauskardt, John C. Bravman, Stanford University, Dept of Materials Science and Engineering, Stanford, CA.

Silane adhesion promoters are seeing increasing use in microelectronic packaging interfaces. For example, they are currently used to adhere the passivating polymer overlayer to oxide, and these materials are being investigated as surface treatments for silica particles in underfill epoxies. Until recently, the exact mechanism of adhesion promotion was postulated. In this paper, we present detailed studies of silane adhesion promoters on the silicon oxide surface. Two common promoters (aminopropyltriethoxysilane and vinyltriethoxysilane) as well as non-functional silanes are investigated. It was found that without a functional end group, long carbon chain silanes can severely degrade adhesion, resulting in interfaces weaker than if no silane is used. Several spin coat solution formulations are used in depositing these films. Resulting surface coverage is examined and quantified with the help of AFM and XPS. Then, the adhesion behavior of various promoter films are tested in sandwich structures using a fracture mechanics approach. Finally, spin-coat solution concentration, surface coverage, and interface fracture energy are compared for the amine functional promoter.

9:45 AM N6.5/L10.5

METAL/POLYMER INTERFACE AND SOLDER JOINT RELIABILITY OF A WAFER LEVEL CSP. H. Han, Jin Yu, K.O. Lee and I.S. Park, Dept. MS&E, Center for Electronic Packaging Materials, Korea Advanced Institute of Science and Technology, Taejon, KOREA.

As microelectronic devices get smaller and higher I/O densities are required, various chip scale packages (CSP) are adopted, and wafer-level chip scale package (WLCSP) combined with flip chip technology has the highest potential. In doing so, it is necessary to redistribute peripheral bond pads and relax the thermal stress in the WLCSP. Here, we use a low modulus polymers as the stress buffer layer (SBL) to relax the thermal stress generated at the solder joint and studied the reliabilities of the metal/SBL interface and solder joint using peel tests and ball shear tests, and effects of the polymer surface pretreatments by the RF plasma and runner metal structure were investigated. Results showed that the adhesion strength of the metal/SBL interface depended on the RF power density (ρ) and runner metal structure. The peel strength (P) was very low for $\rho <$ 0.27W/cm^2 but increased up to ρ = 0.3W/cm^2 and tended to saturate around 1000g/cm. Then failure locus analyses were conducted using AFM, AES, and XPS. The peeling locus of peel test and the failure locus of solder ball shear test were dependent on the Ni layer in the under bump metallurgy (UBM) and also on the thickness of the runner metal, particularly the thickness of Cu layer. Depending on the metal deposition condition, metal films over SBL were delaminated or buckled due to the residual stress in the metal film, which was measured using the laser curvature method. Additionally, stress strain fields and crack initiation and propagation behaviors around the solder joint were analyzed using micro-Moire pattern and the correlated to the process parameters and package structures. Then, implications to the package processes and designs were discussed

10:30 AM N6.6/L10.6

HIGH Tg, LOW DIELECTRIC CONSTANT AROMATIC BENZOXAZOLES CONTAINING ALLYLETHER PENDENT GROUPS FOR USE IN MICROELECTRONIC PACKAGING. Max D. Alexander, Jr., Thuy D. Dang, Christina E. Specker, Marlene Houtz, R.J. Spry, and Fred E. Arnold, Air Force Research Laboratory, Materials and Manufacturing Directorate, Polymer Core Technology Area, Wright-Patterson Air Force Base, OH.

Next generation microelectronic packaging requirements are driving the need to produce increasingly lower dielectric constant materials while maintaining high thermal stability and ease of processing. Polymer candidates with low dielectric constant (2.0-2.4), high thermal stability (degradation temperature > 400°C), high glass transition temperature (> 350°C), low water uptake (< 1%), solubility in selected organic solvents, low thermal expansion coefficient and the capability for undergoing post-polymerization chemistry to impart insolubility after processing have been successfully synthesized and characterized by our research group. Highly fused ring structures, formed via intramolecular hydrogen bonding, were utilized for the enhancement of the glass transition temperature. Lowering of the dielectric constants of these polymeric structures was accomplished by the incorporation of perfluoroisopropyl groups along the polymer backbone. The design of post-polymer reactions to impart insolubility to select polymer candidates was based on the methodology of attachment of crosslinking sites to the polymer backbone. Aromatic benzoxazoles

containing pendant allylether groups were synthesized from the parent structures. Upon heating, the polymer would undergo an intramolecular rearrangement reaction (Claisen rearrangement), resulting in a Tg enhancement by increasing the number of fused rings via intramolecular hydrogen bonding between the in situ-formed hydroyl groups and the nitrogen atom of the adjacent benzoxazole group. At elevated temperature (250-300°C), crosslinking of the allyl groups would occur, thus providing a mechanism for insolubility and dimensional stability of the polymer system. Efforts are underway to control the crosslinking density of the polymer system by partial allylation of the hydroxyl groups attached to the aromatic benzoxazoles. We will address several issues relating to integration of these polymeric materials into current processes and how we have tailored our systems, to address issues such as back etching, adhesion, dimensional stability, and conformal coating of small feature sizes.

10:45 AM *N6.7/L10.7

MOLECULAR INTERACTIONS AND ADHESION FOR INTERFACES RELEVANT TO FLIP-CHIP ASSEMBLIES

Raymond A. Pearson, Lehigh University, Dept of Materials Sci. & Eng., Bethlehem, PA.

Debonding is a common wear-out mechanism in flip-chip assemblies that utilize organic substrates. The large mismatch of the thermal expansion coefficients of the silicon chip and the organic substrate generates significant stresses during thermal cycling. These thermally induced stresses promote debonding at several interfaces and debonding at the underfill-passivation interface can occur. This paper focuses on developing an understanding between interfacial molecular interactions and adhesive strength in an effort to 'engineer' reliable interfaces. The experimental approach consists of studying the adsorption of model epoxy systems onto polyimide and borosilicate surfaces using a flow microcalorimeter and separating these interfaces using double cantilever beam specimens. Acid-base theory is utilized to explain the trends in adhesion strength.

11:15 AM *N6.8/L10.8

THERMOMECHANICAL RATCHETING IN INTERCONNECTS.

Z. Suo, M. Huang, Mechanical and Aerospace Engineering Department and Materials Institute, Princeton University, Princeton, NJ; Q. Ma and H. Fujimoto, Intel Corporation, Santa Clara, CA; J. He, Intel Corporation, Components Research, Hillsboro, OR.

Temperature cycling has long been used as an accelerated reliability test to qualify new electronic products. Many commonly observed failure modes, however, are so poorly understood that the extrapolation of the test results to service lifetime is empirical, loosely based on historical records of similar products. This lack of mechanistic understanding is particularly disconcerting when new interconnect materials are being explored. We have initiated a program to study mechanisms of failure modes under temperature cycling. In this talk, we present our recent study on cracking in the SiN film. The SiN film has been widely used as a passivation layer in microelectronic devices. It has been known for over a decade that the SiN film cracks after packaged devices are thermally cycled. While engineering solutions have been proposed on the basis of trial and error, no basic understanding of the cause of the cracking has been identified before. In this talk, we show that the cyclic temperature, coupled with the shear stress at the die corner, causes the interconnect pads underneath the SIN films to undergo plastic ratcheting. Consequently, in the SiN films the stress builds up as the temperature cycles, leading to cracks. We compare the effects of copper and aluminum interconnects. Implications for design rules and qualification tests are discussed.

11:45 AM N6.9/L10.9

DIELECTRIC PROPERTIES OF FERROELECTRIC CERAMICS-POLYMER COMPOSITE FILMS.

C.K. Chiang, L.P. Sung and J. Obrzut, National Institute of Standards and Technology, Gaithersburg, MD.

The ferroelectric ceramic-polymer composite thin-film is one of important electronic packaging materials. The dielectric constant of a ceramic-polymer composite thin film follows an empirical logarithmic mixing rule when the powder is dispersed uniformly. The low dielectric polymer matrix usually dominates the dielectric constant of the composite. For example, a composite containing 30 volume percent of barium titanate powder in an acrylic polymer shows the dielectric constant about 21 at 1 kHz. This value is much less than that of ceramic powder in the composite. Further increasing the concentration of the filler has only limited effect on the increase of the dielectric constants. We used laser scanning confocal microscopy and optical microscopy to examine the distribution of particles. The thin-slice images of the thickness of the order of one micron and re-constructed 3D image from them allowed us to visualize the relation of micron-size particles and the polymer interface between them nondestructively. These data may correlate to the dielectric constant of composite thin-films from different processing conditions.