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SESSION D1: ADVANCED MATERIALS AND STRUCTURES
Chair: Tsu-Jae King
Tuesday Morning, April 22, 2003
Golden Gate C2 (Marriott)

NOTE EARLY START

8:00 AM *D1.1
SCALING CHALLENGES FOR SUB-50-NM CMOS TECHNOLOGY. Tohru Mogami, Silicon Systems Research Laboratories, NEC Corporation, Sagamihara, Kanagawa, JAPAN.

Scaling challenges are discussed for sub-50-nm CMOS technology to improve the gate delay of CV/I. The basic scaling challenges must be a small channel-length formation, an equivalent oxide thickness (EOT) thinning of silicon oxynitride (SiON) film, and a suppression of series resistance. 24-nm MOSFETs are precisely formed by shallow source/drain extensions (SDE) and a steep halo using a high-ramp-rate spike annealing (HRR-SA) and a reverse-order source/drain (R-S/D) formation. The steep halo is useful to suppress parasitic resistances. For gate-dielectric, a radical oxynitridation process achieves a low-leakage SiON film with high reliabilities including negative bias temperature instability (NBTI), because of its higher dielectric constant and well-controlled nitrogen profile. The aggressive scaling challenges should include a high-k gate dielectric film and a small-depletion gate electrode. The high-k dielectric film with a small EOT of 1.1 nm is achieved by zirconium silicate with a compositional gradation and a post deposition annealing (PDA). For a gate electrode, the gate depletion of poly-SiGe is remarkably suppressed by the control of grain size of poly-SiGe. Furthermore, a thin amorphous-Si layer between poly-SiGe and gate-dielectric films is able to improve a break down charge (QBD). The metal gate electrode using W/TiN systems suppresses the gate depletion. Furthermore, dual-metal gated CMOS devices with a threshold voltage difference of 0.1 V are demonstrated by a nitride concentration controlled TiN film using a nitride-ion implantation. In sub-50-nm CMOS devices formed by challenging technologies, the integration technology must be strongly studied, especially for SoC applications.

8:30 AM *D1.2
PROSPECTS AND CHALLENGES FOR ADVANCED GATE-STACK MATERIALS IN SUB-65 NM CMOS TECHNOLOGY. Hiroshi Iwai, Tokyo Institute of Technology, Frontier Collaborative Research Center, Yokohama, JAPAN.

Progress of MOS LSI has been accomplished by the downscaling of its components such as MOSFETs. Now, the gate insulator thinning becomes the most critical issue for the downscaling of MOSFETs. Already 1.4 nm thick oxynitride films have been used for the gate insulator of high-speed microprocessor products. However, the huge direct-tunneling leakage current through the gate oxides is a big problem and will limit further downsizing after a few more generations in near future. The leakage through the gate insulator is a more serious problem for low standby power devices such as cellular phone and thus, introduction of high dielectric constant (or high-k) gate insulator is strongly demanded. Among the high-k dielectrics, HfO2 and ZrO2 have been thought to be the most promising candidates because of their predicted good thermal stability and high dielectric constant values. In reality, however, these materials have, at this moment, several serious problems, such as i) interfacial later growth and micro-crystal formation during the thermal process, ii) lower carrier mobility at the high-k and silicon interface, iii) higher densities of fixed charge and interface state, iv) boron penetration from the gate electrode during the thermal process, v) contamination of the film from precursor of CVD. Solutions for the above problems are seriously being developed in the world, and some good results have been reported. Investigation on other materials such as rare earth oxides is also being done and some good results of La2O3, Pr2O3, Gd2O3 have been also reported. In this paper, current status of the development of the high-k gate dielectrics for advanced CMOS gate insulator is reviewed.

9:00 AM *D1.3
ISSUES IN SELECTING METAL GATE ELECTRODES FOR CMOS APPLICATIONS. Veena Misra, Bei Chen, You-Seok Suh, Jaehoon Lee and Jason Gurganos Department of Electrical and Computer Engineering North Carolina State University, Raleigh, NC.

This papers will focus on the material and electrical properties of candidate metal electrodes on SiO2 and high-K dielectrics. In the gate electrode selection process, work function, thermal stability and gate depletion are all critical parameters that need to be satisfied. Although, elemental metals have found to exhibit a wide range of work function values (3eV to 6eV), obtaining their thermal stability is problematic. The challenge especially lies in finding low work function metals (for NMOS devices), which also offer thermal stability. One option to achieve this is to introduce N and/or Si in metals with low work functions. Another approach is to use metal alloys of low and high work functions. Both these approaches will discussed in terms of having of appropriate work functions on high-K dielectrics, thermal stability of EOT and VFB and feasible integration schemes including composition control, dual gate integration and dopant diffusion. Candidate metals for PMOS applications will also be discussed.

9:30 AM D1.4
STACKED METAL LAYERS AS GATE FOR MOSFET THRESHOLD VOLTAGE CONTROL. Wei Gao and Yoshi Ono, Sharp Labs of America, Camas, WA.

The transition to metal gates and high-k materials for future MOSFETs requires the right choice of materials for achieving the proper threshold voltages for both p and n type FETs. This report describes a study on two layer metal gate stacks that allows the effective work function to be tuned by varying the thickness of the first metal layer. MOS capacitors were fabricated by using Al on TaN and Pt on TiN metal stacks on thermal oxide and on HfAlO gate dielectric where the TaN and TiN layer thickness is varied over a range from 0 to 100nm. Electrical and thermal stability measurements were performed and are reported. The effective workfunction is seen to transition from the value of one metal to the other rapidly as the thickness of the first metal layer is varied from 0 to around 10nm. The Vfb transition matches the workfunction difference of the two metals in the stack. Both the first and second metal must be stable in contact with gate dielectric and throughout the remainder of the fabrication process. The advantage of this approach is that it allows the effective workfunction of the metal stack, and the Vth of the device to be fine tuned. It also allows for eventual CMOS fabrication where two different work function metal stacks are necessary, without processing directly on the gate dielectric.

10:15 AM *D1.5
KEY FEOL TECHNOLOGIES IN 65 NM NODE SOI-MOSFETS FOR WIDE RANGE OF APPLICATION. T. Sugii, Y. Momiyama, K. Goto, T. Yamamoto, S. Pidin, T. Kubo, M. Kase, Fujitsu Ltd., Tokyo, JAPAN; T. Hirose, Y. Watanabe, T. Aoyama, Fujitsu Laboratories Ltd., Atsugi, JAPAN.

In this paper, we first review recent trends of MOSFET development, which are an aggressive scaling of gate length, decrease in on-current with scaling, and an increased variety of transistors for a wide range of target products. To satisfy the requirement for the wide range of target products such as high-end MPU, digital AV, mobile, RF application, and so on, transistors used for them must have variations in their characteristics by optional technologies. The variation is classified to speed performance, power consumption (dynamic, standby), RF performance, and so on. In the 65 nm node, both overcoming issues on aggressive scaling and satisfying requirements of variety of transistors have to be realized by introduction of a new material, a new structure, and a new process in a short development time. In this paper, we show our approach for the 65 nm node such as SOI-MOSFETs, a dynamic threshold operation, a metal over-gate structure, a high-k gate insulator, and a laser annealing process. These new technologies should be properly used from the point of required performance and cost. For example, we developed SOI-DTMOS with a metallic overlay-gate for one-chip integration of RF/digital ICs for wireless systems and high-speed data communication systems. The transistor has an fmax of 185 GHz, which is forecasted by ITRS as a 2016′ technology. In addition, a very low noise properties have also been obtained. The minimum noise figure is less than 1dB. This value is competitive to GaAs low-noise HEMT one.

10:45 AM *D1.6
EVOLUTION OF THE SOI MOSFET: FROM SINGLE GATE TO MULTIPLE GATES. Jean-Pierre Colinge, Dept. of Electrical and Computer Engineering, University of California, Davis, CA.

During the last 20 years Silicon-on-Insulator (SOI) MOSFETs have evolved from the partially depleted structure inherited from SOS technology into fully depleted devices which are more adapted to high-performance, low-voltage applications. Standard SOI MOSFETs essentially mimic bulk devices and suffer from similar problems when decananometer gate lengths are reached. These problems are usually referred to as "short-channel" effects and include DIBL subthreshold slope degradation. These effects are caused by the two-dimensional encroachment of drain electric field lines on the channel region. Classically these effects are minimized using engineered doping profiles in the channel region, such as the formation of HALOs. Fully depleted SOI MOSFETs offer another way of restoring the control of the channel region by the gate and reduce the influence of drain field lines from the drain: the use of double and triple gate device structures. The scaling benefits of the double-gate device have been explored as early as 1984, and volume inversion was first reported in 1987. Despite of several proposed embodiments and the fabrication of

medium-scale (10k transistors) ICs, the fabrication of double-gate SOI MOSFETs remains somewhat exotic and unpractical. Triple-gate devices, on the other hand, are much easier to fabricate. They offer much higher current drive than single-gate transistors, along with superior short-channel effect reduction capability and are likely candidates for decananometer, low-voltage CMOS applications.

11:15 AM D1.7
A TECHNIQUE FOR SOURCE/DRAIN ELEVATION USING IMPLANTATION MEDIATED SELECTIVE ETCHING. M.Q. Huda and K. Sakamoto, Nanoelectronics Research Institute, National Institute of Advanced Industrial Science and Technology, Tsukuba, JAPAN.

A process involving implantation mediated selective etching has been developed for Source/Drain elevation of CMOS devices. Our approach relies on the formation of elevated Source/Drain by non-selective growth of silicon through conventional Low Pressure Chemical Vapor Deposition (LPCVD). Poly-silicon layers deposited on SiO_2 or Si_3N_4 sidewalls would then be removed by selective etching in a solution of HF: HNO_3: CH_3COOH. A silicon layer of 100 nm thickness was formed on a sample with Si/SiO_2 structure by LPCVD at 700°C. As grown poly-silicon layer formed on the oxide region showed a small rate of etching similar to that of the elevated epitaxial silicon. Samples were then implanted with Argon at 140 keV with a dose of $2x10^{14}/cm^2$. Implantation orientation was aligned in the vertical $< 100 >$ channeling direction to keep damage in the elevated silicon region in a minimum level. A short annealing at 420°C was sufficient for damage recovery of the epitaxial silicon. The damage in poly-silicon layer, on the other hand, showed only a small recovery by the same annealing. The implanted and annealed layers of poly-silicon and silicon showed etching rates of 20 nm/min and 1 nm/min respectively. The selectivity over an order of magnitude was used to etch the poly-silicon layers, leaving the elevated silicon region unaffected. Pattern edges, representing the gate sidewalls in actual devices, showed no sign of residual poly-silicon. The sidewall material SiO_2 subjected to the implantation and annealing step, was found to work as an etch-stop with etching rate of 6 nm/min. Much smaller etching rate of 0.5 nm/min was observed for Si_3N_4 under similar processing conditions. Our approach of silicon elevation does not depend on isolation/sidewall materials, and is not bound by thickness limits, or faceting effects.

11:30 AM D1.8
STUDY OF USING ELEMENTS FROM GROUP II AS BARRIERS FOR DOPANT PENETRATION INTO GATE DIELECTRICS AND GETTERS FOR METALLIC ION CONTAMINATION. Grace Sun, Vladimir Zubkov, Sheldon Aronowitz, LSI Logic Corp., Milpitas, CA; Margaret A. Gabriel, Department of Chemistry, University of Washington, Seattle, WA.

Various mechanical and chemical processes may introduce contamination, such as metallic ions, during the creation of an integrated circuit. This can cause device degradation and current leakage. In addition to externally introduced charged species, during anneal cycles dopants such as boron can penetrate the silicon substrate from a highly doped polysilicon gate; this penetration also will cause problems. We performed extensive first principles calculations using periodic boundary conditions and cluster approximations to search for a novel material that can attract or trap ions and fast diffusing dopant species to reduce or eliminate such problems. Examination of calcium and strontium interactions with other ions in silicon dioxide was conducted. Strong metal ion attractions to calcium are calculated. Ion attractions to strontium are also found, but the magnitudes are less and, in several cases, even repulsive. Both calcium and strontium attract neutral boron with the stronger attraction found with calcium. Calcium interaction with boron in other dielectric materials was also studied. Attraction was predicted to occur between calcium and boron whether they were distributed in silicon dioxide, hafnium or zirconium orthosilicate, for example. This study leads us to propose incorporation of calcium into critical dielectric layers as a promising material to trap ions and reduce boron penetration through the gate oxide. Compared to existing boron penetration barriers, calcium has several advantages. In this talk, results of our theoretical investigation along with experimental work will be presented.

11:45 AM D1.9
CREATION OF A NEW CLASS OF SEMICONDUCTOR MEMORY DEVICES GUIDED BY QUANTUM MECHANICAL MODELING. Sheldon Aronowitz, Vladimir Zubkov, Grace Sun, LSI Logic, Milpitas, CA; Mehmet C. Ozturk, Yanxia Lin, Department of Electrical and Computer Engineering, North Carolina State University, Raleigh, NC.

A new class of semiconductor memory devices is proposed. The class is a product of quantum mechanical calculations that predicted non-zero electron affinities when zirconium was inserted into a representative structure of silicon dioxide. The zirconium rich region exhibited an electron affinity between 1.7 and 1.9 eV in the simple silicon dioxide models first used. That is, the regions where excess zirconium is incorporated into silicon dioxide will function as charge storage centers. More elaborate calculations were performed on cristabolite using periodic boundary conditions with density functional theory. Transition metal or non-transition metal elements were inserted into the center of a ring and the entire structure then was allowed to relax. It was found that the inserted elements tended to remain in their original positions. Interestingly, the depth of the electron trapping well, if formed, was found to be unique to each element. An existing memory device class, which utilizes states created at the interface between two different dielectric materials such as silicon nitride and silicon dioxide, superficially resembles this new one. However, these two classes are fundamentally different. The properties of the new class result from intrinsic electronic interactions between the transition metal with its immediate silicon dioxide environment, for example, and not because of mismatched or dangling bonds at the boundary of two materials. The talk will include extensions to other systems, such as amorphous hafnium oxide by itself, and to experimental investigations.

SESSION D2: HIGH-k DIELECTRICS
Chair: Tohru Mogami
Tuesday Afternoon, April 22, 2003
Golden Gate C2 (Marriott)

1:30 PM *D2.1
IMPACT OF NEW MATERIALS AND TRANSISTOR ARCHITECTURES ON SCALED CMOS FOR MIXED-SIGNAL APPLICATIONS. Youri Ponomarev, Philips Research Leuven, BELGIUM.

The introduction of both new materials (high-k gate dielectrics, metal gate electrodes, mobility-enhancing materials in the channel, such as strained Si or SiGe) and alternative transistor architectures, such as FD-SOI and multi-gate transistors (FinFET, Double Gate, SON, etc.) into 45nm and smaller CMOS nodes is inevitable. It is quite clear that historical trend of yearly improvement of transistor performance by 17% will be impossible to sustain without it. The driving force of these changes is naturally coming from the necessity to aggressively scale CMOS for digital applications (both logic and memories). However, this will entail significant consequences to the operation of non-digital parts of the IC, which might be either beneficial or detrimental, depending on the application block. In this paper we will review these effects, with special emphasis on analogue/RF parts of the circuitry used for mixed-signal applications. We will show that early feedback loop between new materials and transistor architectures on one side and application domains on the other is of vital importance to ensure future SOC success.

2:00 PM D2.2
IMPACT OF GATE PROCESS TECHNOLOGY ON EOT OF HfO_2 GATE DIELECTRIC. Daewon Ha, Qiang Lu, Hideki Takeuchi, Tsu-Jae King, Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA; Katsunori Onishi, Young-Hee Kim, Jack C. Lee, Department of Electrical and Computer Engineering, University of Texas, Austin, TX.

HfO_2 is one of the most promising candidates to replace SiO_2 as the gate dielectric because of its high permittivity, thermodynamic stability, and large energy-bandgap offset to Si. For simplicity of process integration, polycrystalline silicon (poly-Si) is preferred as a gate electrode material. However, the growth of an interfacial layer at the surface of the silicon upon high-temperature annealing (e.g. used for source/drain formation) increases the equivalent oxide thickness (EOT) and gate leakage current [1]. Polycrystalline silicon-germanium (poly-SiGe) has been received much attention as an alternative gate-electrode material, because it alleviates gate depletion and boron penetration issues [2]. Recently, it was reported that the use of poly-SiGe results in thinner EOT for HfO_2 gate dielectric [3]. In this paper, we investigate the mechanism responsible for this effect. Using MOS capacitors, the effect of the gate material and gate deposition rate on interfacial layer formation is studied. A conventional LPCVD furnace was used to deposit the gate materials (poly-Si and poly-$Si_{0.8}Ge_{0.2}$) at 550°C onto PVD HfO_2 gate dielectric. The effect of gate deposition rate was studied by comparing the results for poly-Si deposited using SiH_4 against those for poly-Si deposited using Si_2H_6. (The deposition rate for poly-Si using Si_2H_6 is about 8 times faster than that for poly-Si using SiH_4; the deposition rate for $Si_{0.8}Ge_{0.2}$ is about 7 times faster than that for poly-Si using SiH_4.) Interfacial layer thicknesses are evaluated by cross-section transmission electron microscopy (TEM) and capacitance measurements. Initial results indicate that poly-$Si_{0.8}Ge_{0.2}$ gate provides the highest inversion capacitance (F/cm^2), while the Si_2H_6-deposited poly-Si gate provides the lowest inversion capacitance. TEM analysis elucidates differences in the thickness of

the interfacial layer between the HfO_2 and silicon substrate. The dependence of interfacial layer thickness and gate leakage current on annealing temperature for each gate electrode material will be presented. [1] L. Kang et al., IEDM Technical Digest, pp. 35-38, 2000. [2] W.C. Lee et al., Symposium on VLSI Technology, Technical Digest, pp. 190-191, 1998. [3] Q. Lu et al., Symposium on VLSI Technology, Technical Digest, pp. 86-87, 2002.

2:15 PM D2.3
ANALYSIS OF INTERFACIAL DIFFUSION BETWEEN HIGH-k GATE DIELECTRICS AND SILICON SUBSTRATE USING MOLECULAR-DYNAMICS TECHNIQUE. Tomio Iwasaki and Hideo Miura, Mechanical Engineering Research Laboratory, Hitachi, Ltd., Tsuchiura, JAPAN.

The problem of interfacial-layer formation between high-k gate dielectrics and a Si substrate is one of the major problems to be solved in order to obtain future devices that have gates with sub-nm equivalent oxide thickness (EOT). Interfacial oxygen diffusion from high-k gate dielectrics into a Si substrate at high temperatures is considered to be a dominant factor in the interfacial-layer formation. To find effective methods for suppressing the interfacial diffusion, we have developed a molecular-dynamics technique for analyzing the atomic diffusion at different-material interfaces. Because this technique uses the extended Tersoff potential that can cope with charge transfer between different elements, we can analyze the atomic diffusion at dielectric/semiconductor interfaces as well as at metal/metal, semiconductor/semiconductor, dielectric/dielectric interfaces. To suppress the formation of a lower-k interfacial layer, this technique was applied to the analysis of interfacial oxygen diffusion from high-k gate dielectrics (ZrO_2 and HfO_2) into a Si substrate. The analysis results showed that the interfacial oxygen diffusion is suppressed when Ti atoms are positioned in the ZrO_2 and HfO_2 films. They also showed that the oxygen diffusion at the ZrO_2/Si(111) and HfO_2/Si(111) interfaces is much more suppressed than that at the ZrO_2/Si(001) and HfO_2/Si(001) interfaces. Thus it was found that the addition of Ti and the use of Si(111) substrates instead of Si(001) substrates are effective methods for suppressing the interfacial-layer formation. The effectiveness of these methods was confirmed by transmission electron microscopy (TEM). We thus conclude that the molecular dynamics technique is useful in finding effective methods for suppressing the interfacial-layer formation between high-k gate dielectrics and a Si substrate.

2:30 PM D2.4
INTERFACE ATOMIC STRUCTURE AND BAND OFFSETS AT HIGH K OXIDE:Si INTERFACES. J. Robertson, P.W. Peacock, Engineering Dept, Cambridge University, Cambridge, UNITED KINGDOM.

High dielectric constant oxides are needed to replace silicon dioxide as the gate oxide in future CMOS devices. The band offsets should exceed 1V to inhibit leakage currents. The atomic structure and bonding across the interface between representative high K oxides, ZrO_2 and $SrTiO_3$, and Si have been modeled, and their electronic structure and band offsets have been calculated. Atomic models of the epitaxial interfaces Si:ZrO_2(100), Si:ZrO_2(111), Si:SrO(100), Si:$SrTiO_3$(100) are used as examples. Because the bonding in the oxides is ionic, the bonds across the interface must satisfy more conditions to give charge neutrality and an absence of interface states, than for the simpler case of the SiO_2:Si interface. The total energy of the interfaces is found to compare their stabilities. It is found that changing the termination oxide can vary the band offset by 0.5 eV, compared to those values previously determined by matching bulk charge neutrality levels [1]. [1] J. Robertson, J Vac Sci Technol B 18 1785 (2000).

2:45 PM D2.5
LAYERED TUNNEL BARRIERS USING HIGH DIELECTRIC CONSTANT MATERIALS. Julie D. Casperson[a], L. Douglas Bell[b], Brett W. Busch[c], Mun Yee Ho[c], Martin L. Green[c], Harry A. Atwater[a]; [a]California Institute of Technology, Watson Laboratory of Applied Physics, Pasadena, CA; [b]Jet Propulsion Laboratory, Pasadena, CA; [c]Agere Systems, Murray Hill, NJ.

We have modeled and fabricated the layered dielectric barrier structures that address the main performance limitations of floating gate nonvolatile memory devices, such as flash memories and nanocrystal memories, namely the long program time ($\sim$1 μs) and erase time ($\sim$1 ms) achievable via a Fowler-Nordheim tunneling mechanism for charging of the floating gate through a homogeneous tunnel barrier. Silicon compatible layered barrier heterostructures that enable a large drop in the barrier height with applied voltage are an alternative to homogeneous dielectric films as the tunnel barriers for nonvolatile memories. Such voltage-dependent barrier lowering in layered tunneling barrier heterostructures may also form the operating principle for a new class of electrically-tunable photodetectors. Using a numerical effective-mass model, we have been able to optimize and analyze possible layered structures with real materials parameters. Based on literature values for conduction band offsets, we find from simulation that some of the most promising structures for layered tunnel barriers consist of Al_2O_3 with Si_3N_4 or HfO_2 and we have fabricated such structures. The Si_3N_4 was made by low-pressure chemical vapor deposition, while the Al_2O_3 and HfO_2 were made by atomic layer deposition. We have fabricated the layered barrier structures Si_3N_4 / Al_2O_3 / Si_3N_4 and HfO_2 / Al_2O_3 / HfO_2 as well as single- and double-layered structures using these materials. One of the important results is in the comparison of the I-V characteristics of n-Si / Si_3N_4 / Al_2O_3 / Si_3N_4 and n-Si / Si_3N_4 / Al_2O_3. We find significant asymmetry in the two-layer measurement, an indication of barrier lowering in a Si-based layered tunneling barrier structure. Experiments involving metal-insulator-semiconductor diodes with semi-transparent gates are underway in order to directly measure the band offsets of our dielectric materials, using a chopped tunable arc-lamp source for illumination. These measurements give us a better understanding of the electrical properties of the heterostructures.

3:15 PM *D2.6
HIGH-k MATERIALS FOR ADVANCED GATE STACK DIELECTRICS: A COMPARISON OF ALCVD AND MOCVD AS DEPOSITION TECHNOLOGIES. Matty Caymax, H. Bender, B. Brijs, R. Carter, M. Claes, T. Conard, S. De Gendt, A. Delabie, M. Heyns, O. Richard, W. Vandervorst, and S. Van Elshocht, IMEC vzw, Leuven, BELGIUM; J.W. Maes, ASM Belgium, Leuven, BELGIUM; L. Date and D. Picque, Applied Materials France, Meylan, FRANCE; M. Green, V. Kaushik, J. Kluth, and W. Tsai, International Sematech residents at IMEC.

Among the metal oxides with high electrical permittivity (high-k) that are currently considered as candidates to replace SiO2 as gate dielectric, the oxides based on Hf are the most favored ones. Two of the most important deposition techniques to fabricate thin layers of these materials are Atomic Layer Chemical Vapor Deposition (ALCVD) and Metal-organic CVD (MOCVD). In this presentation, we will compare several aspects of these techniques and of the materials deposited as a function of their suitability for gate dielectrics for both low power and high performance applications. First, we will briefly describe the two deposition techniques and the most important differences/similarities. We will discuss some typical growth characteristics, and the importance of these characteristics for the resulting quality of the film. The success of both techniques for this application is heavily depending on the starting surface; this will be illustrated for a number of different surface pre-treatments. The resulting interfacial layer (IL) behaves quite differently for both techniques, as will be shown. Also the stability of this IL during further thermal processing can become an issue. Next, the characteristics of the bulk of both types of films can be very different, such as the density of the films, the surface roughness and the presence of defects. On the other hand, there are also striking similarities such as the k values as they are evaluated from CV measurements on capacitors. The interaction of the HfO2 films with electrode layers is strongly dependent on the type of electrode layer, and needs special attention. Whereas the principle of the approach to cope with this interaction is very similar in both cases, still the practical way to solve the problem can be quite different. Finally, we will compare some of the pros and cons for low power and for high performance applications.

3:45 PM D2.7
SCALABILITY OF MOCVD-DEPOSITED HAFNIUM OXIDE. S. Van Elshocht[a], R. Carter[a], M. Caymax[a], M. Claes[a], T. Conard[a], L. Date[b], S. De Gendt[a], V. Kaushik, A. Kerber, J. Kluth, G. Lujan[a], J. Petry[a], D. Pique[b], O. Richard[a], E. Rohr[a], Y. Shimamoto[c], W. Tsai , and M.M. Heyns[a]. [a]IMEC vzw, Heverlee, BELGIUM; ISMT, Austin, TX; [b]Applied Materials, Meylan, FRANCE; [c]Hitachi, Kokubunji, Tokyo, JAPAN.

Because of aggressive downscaling to increase device performance, the physical thickness of the SiO_2 gate dielectric is rapidly approaching the limit where it will only consist out of a few atomic layers resulting in very high leakage currents due to direct tunneling. To allow further scaling, materials with a k-value higher than SiO_2 are explored, the so-called high-k materials, such that the thickness of the dielectric can be increased without degrading performance. For the moment, the most likely candidates are the Hf-based materials such as HfO_2, HfSilicates, and the HfAluminates. The present work discusses the potential of MOCVD-deposited HfO_2 to scale to 1- and sub-1-nm EOTs, where we will focus on the issues that complicate downscaling the gate stack and try to suggest possible solutions. It can be suspected that aberrations from the ideal gate stack Si/HfO_2/polySi will result in an increased EOT. Hence, a primary concern is the interfacial layer that is formed during the MOCVD deposition process between the Si and the HfO_2 for both H-passivated and SiO_2-like starting surfaces. This interface will contribute to the EOT reducing

the benefit of the high-k material, but at the same time seems to have a positive effect on the mobility. In addition, we have observed, for example by TEM, that interactions occur between the HfO_2 and the polySi gate electrode at the top interface. Furthermore, we have determined, based on a thickness series, the k-value for HfO_2 deposited at various temperatures and found that the k-value of the HfO_2 depends upon the gate electrode deposited on top (polySi or TiN). We propose a hypothesis to explain this dependency and discuss the impact on EOT scalability. Finally, we demonstrate that also the thermal stability of the gate stack forms a potential problem for scaling EOT values.

4:00 PM D2.8
SCALING LIMITS OF ATOMIC LAYER DEPOSITED HfO_2 GATE DIELECTRICS. M.L. Green and G.D. Wilk, Agere Systems, Berkeley Heights, NJ; M.-Y. Ho, National University of Singapore, SINGAPORE; B. Busch, Micron, Boise, ID; T. Sorsch, Lucent Technologies, Murray Hill, NJ.

The international semiconductor roadmap calls for gate dielectrics with equivalent oxide thickness (EOT) < 1.0 nm by about 2007. Therefore, it is important to understand to what extent one of the most promising high-k candidate materials, HfO_2, can be scaled. In this capacitor study, the parameters studied were HfO_2 layer thickness (3 - 6 nm), type of underlayer (SiO_2, Si-O-N or Si-O-H (chemical oxide)), and post-deposition anneal PDA) temperature (600 - 1000C), time (spike anneal - 600 seconds), and ambient (N_2, O_2 or NO). Chemical oxide underlayers were favored in this study, as they gave rise to the smoothest, most two-dimensional films. Using them leads to the thinnest "sealed" (i.e., pinhole-free) films. These results were compared to HfO_2 growth on thermal oxide or oxynitride underlayers. Electrical measurements reported in this study are EOT, leakage current and $Delta V_{fb}$. Regardless of the PDA ambient, high temperature anneals (>700C) are required to lower $Delta V_{fb}$, as is some interfacial regrowth. For 3 nm HfO_2 layers, the thinnest practical from a growth and gate current leakage standpoint, even if the PDA resulted in no regrowth at the interface, the minimum achievable EOT would be about 1.2 nm. Therefore, to achieve sub-nanometer EOT gates with HfO_2, the intentionally grown underlayers should be eliminated. Schemes for accomplishing this, while achieving satisfactory growth morphology, will be discussed. The alternative is to identify suitable high-k films with dielectric constants greater than that of HfO_2 (18-20).

4:15 PM D2.9
ENHANCEMENT OF THE THERMAL STABILITY OF Hf-SILICATES WITH NITROGEN INCORPORATION AND ITS INFLUENCE ON THE ELECTRICAL PROPERTIES.
Akira Nishiyama, Masahiro Koike, Tsunehiro Ino, Masato Koyama, Ryosuke Iijima, Takeshi Yamaguchi and Mizuki Ono, Toshiba Corp., Advanced LSI Technology Laboratory, Corporate R&D Center, Yokohama, JAPAN.

Hf-silicate is one of the prospective materials for the first high-k gate dielectrics applied to real LSIs due to its modest dielectric constant and relatively good interface properties with silicon substrate. However, the major drawback of this material has been its poor thermal stability. Experiments with Hf-silicate, sputter-deposited on Si substrate have clearly revealed that the phase separation from the uniform silicate structure to HfO_2 and the remaining matrix during high-temperature annealing, which is required in the conventional CMOS process, resulted in the reduction of the average dielectric constant of the film. It could lead to significant degradation in the speed of CMOS circuits. To enhance the thermal stability, nitrogen was incorporated in Hf-silicate by adding N_2 in the ambient of the sputtering system. The result indicated that the nitrogen as well as hafnium in the material could increase the dielectric constant of the material. Moreover, nitrogen can retain its high dielectric constant by suppressing the phase separation phenomenon.
Poly-Si/Hf-silicate/p-Si capacitors with the same physical dielectric thickness revealed that the equivalent oxide thickness decreased as the nitrogen concentration increased, while the reduction in leakage current relative to that of SiO_2 remained almost the same. The dependence of other electrical parameters such as fixed charge and charge trapping on the nitrogen concentration will be also discussed at the presentation.

4:30 PM D2.10
PHYSICAL-CHEMICAL EVOLUTION OF Hf-ALUMINATES UPON THERMAL TREATMENTS. Barbara Crivelli, Mauro Alessandri, Stefano Alberici, Daniela Brazzelli, Alice Camille Elbaz, Gabriella Ghidini, Giuseppe Pavia, STMicroelectronics, Agrate Brianza, ITALY; Jan Willem Maes, ASMI, Leuven, BELGIUM; Giampiero Ottaviani, University of Modena, Department of Physics and Unitaí INFM, Modena, ITALY; Claudia Wiemer, Laboratorio MDM-INFM, Agrate Brianza, ITALY.

The continuous scaling down of transistor and memory devices toward 65 nm technology node demands for the replacing of ultra thin SiO_2 based dielectrics with high-k materials. In this study, the investigation of physical-chemical stability of Al_2O_3-HfO_2 alloys upon prolonged post-deposition annealings (PDA) is presented. Two different Hf-aluminates were analyzed, containing 35% and 75% Al_2O_3 mol% respectively. Amorphous films were deposited on RCA treated p-type silicon by ALCVD™. Post-deposition annealings were carried out in O_2 or N_2 atmosphere, at 850°C and 900°C for 30 minutes. Interfacial layer (IL) increase after PDA was detected on all the samples. No impact of annealing temperature was observed on Al-rich alloy, while sensible effect was noticed on Hf-rich material. N_2 and O_2 annealings resulted in limited IL differences, suggesting that these films were not completely permeable to oxygen diffusion. XRD and planar TEM-ESI analysis evidenced first phase separation and then, in the case of Hf-rich samples, crystallization phenomena occurring at HfO_2 cluster sites. Differently from HfO_2, this alloy crystallized mainly in tetragonal phase with some specific features depending on annealing ambient. Stack composition was characterized by means of TOF-SIMS, XRR, EELS, standard and microprobe XRF. Growth of interface layer was justified by limited oxygen incorporation from external ambient. Silicon diffusion from the substrate into high-k material and aluminium/hafnium redistribution were observed and associated to annealing temperature. Finally, Hf-aluminates were electrically characterized by means of C-V and I-V measurements on basic capacitors. Variations in material electrical properties were found consistent with change in physical-chemical film structure. Overall, Hf-aluminates were found to remain amorphous during high temperature prolonged treatments up to 900°C for 75% and 850°C for 35% alloys respectively. Oxygen, silicon and metals inter-diffusion was observed at these conditions, but with no relevant physical differences and lower impact on electrical properties compared to Al_2O_3 and HfO_2.

4:45 PM D2.11
ATOMIC LAYER DEPOSITION OF ZrO2 ON Si AND Ge SUBSTRATE. Hyoungsub Kim, Paul C. McIntyre, Stanford Univ., Dept of Materials Science & Engineering, Stanford, CA; Chi-On Chui, Krishna Saraswat, Stanford Univ., Dept of Electrical Engineering, Stanford, CA.

As the continued scaling of Si CMOS devices approaches its fundamental limits, alternative semiconductor materials, such as Ge, with high intrinsic carrier mobility are increasingly promising for use in the channel region of field effect transistors. However, in the case of a Ge substrate, the lack of a sufficiently stable native oxide (GeO_x) can hinder the formation of a good quality gate dielectric. Recently, deposited high-k dielectric materials prepared on Si by methods such as ALD (Atomic Layer Deposition) have demonstrated excellent film quality and dielectric characteristics. In this presentation, we compare the microstructural and electrical properties of ZrO_2 films grown by the ALD technique on Si and Ge substrates with different surface cleaning/passivation methods. A cold wall ALD system with $ZrCl_4/H_2O$ precursors was used and the deposition was carried out at 300°C. ZrO_2 microstructures on different substrates were investigated using HR-TEM imaging and electron diffraction. Several compositional analyses were performed using AR-XPS and the electrical properties such as C-V and I-V characteristics were compared using Pt gate capacitor structures fabricated through a shadow mask process. High-k dielectric deposition by ALD often occurs readily on hydroxylated surfaces such as chemical SiO_2 or a hydroxylated oxynitride passivation. Deposition processes for gate dielectric preparation on Si surfaces usually result in the unavoidable and uncontrolled formation of a thin interfacial oxide layer if the Si is not already passivated by such a layer prior to deposition. However, in contrast to results on Si substrates, ALD deposition of ZrO_2 film on a Ge (100) substrate showed locally epitaxial growth without a distinct interfacial layer unlike ZrO_2 on SiO_2/Si. Due to the large lattice mismatch (~10%) between ZrO_2 and Ge, a significant areal density of interfacial dislocations was observed. The effects of interface traps, possibly the result of these interfacial dislocations, on the CV hysteresis and frequency dispersion will be presented.

SESSION D3: POSTER SESSION
ADVANCED GATE STACK MATERIALS
Chairs: Hiroshi Kitajima and Robert J.P. Lander
Tuesday Evening, April 22, 2003
8:00 PM
Salon 1-7 (Marriott)

D3.1
A NEW PARAMETER OF PREDICATING GM FOR ULTRA THIN NITRIDED GATE OXIDE. Mitsuaki Hori[a], Naoyoshi Tamura[a], Masataka Kase[a], Hiroko Sakuma[b], Hiroyuki Ohota[b], Mayumi Shigeno[b], Yuuzi Kataoka[b]; [a]Fujitsu, [b]Fujitsu Lab., Tokyo, JAPAN.

The application of nitrided oxide gate dielectric continuously has been used, because the high performance CMOSFET requires high transconductance of channel carrier, i.e., Gm. Also the understanding of Si/dielectric interface for improving the characteristics of base layer of high-k material is highly demanded. Many methods of nitridation technique were proposed and influenced Gm strongly. Previous works indicated that Gm may depend on the nitrogen concentration at the Si/dielectric interface analyzed by SIMS or XPS in the thickness range up to 2.0 nm. Presently the physical thickness is scaled down below 1.1 nm for developing 90 nm generation high-performance transistors, then to solve relationship of Gm and nitridation require immediate attention. We proposed new parameter of predicating Gm for ultra thin nitrided gate oxide. We made MOSFET with some variant ultra thin nitrided gate oxide about the physical thickness of 1.1 nm with the base oxide thickness of 0.85 nm, using the Fujitsu state-of-art 90 nm generation CMOS technology of Lg=40nm transistor, and we investigated these Gm. Also, we analyzed the dielectrics by XPS, and estimated amount of Si3N4 structure by separate N1s peak. Then we observed a good correlation that the ratio of Si3N4 structure in NSi3 and Gm rather than the amount of nitrogen at Si/dielectric interface.

D3.2
TRISILYLAMINE: A C & Cl-FREE SOLUTION FOR LOW TEMPERATURE SILICON NITRIDE CHEMICAL VAPOR DEPOSITION. Christian Dussarrat, Jean-Marc Girard, Takako Kimura, Air Liquide Laboratories, Tsukuba, Ibaraki, JAPAN; Naoki Tamaoki and Yuusuke Sato, Corporate Research & Development Center, Toshiba Corporation, Kawasaki, JAPAN.

With the shrinkage of the critical dimension in semiconductor devices towards 100 nm in a near future, the need to maintain sharp dopant concentration profiles throughout the complete chip manufacturing creates a strong constraint on the allowed thermal budget for the post-implantation process steps. When performed with a dichlorosilane-ammonia (DCS-NH3) chemistry, the low pressure chemical vapor deposition (LPCVD) of Si3N4 is one of the most budget-hungry process since a temperature in the 720-800C range is required to achieve a sufficient deposition rate. Recently, two new low temperature silicon nitride precursors have been proposed to address this issue, namely hexachlorodisilane (HCD) and BTBAS. On one hand, HCD yields high quality Si3N4 films at low temperature, but its results, as for DCS, is the generation of solid byproducts depositing in the exhaust line. Moreover, up to percent level chlorine is incorporated as the deposition temperature is reduced. On the other hand, if BTBAS has the advantage of being chlorine-free, it tends to incorporates high carbon and hydrogen levels. Trisilylamine (TSA, (SiH3)3N) has been evaluated to optimize the film properties and deposition kinetics, taking into account several advantages of this precursor: chlorine and carbon-free; direct Si-N bonds in the molecule; stable, and therefore convenient to use; very volatile. The LPCVD of silicon nitride was achieved at low temperature (between 550 and 780C) using TSA. Silicon nitride films deposited with TSA and ammonia below 600C gave excellent conformal step coverage. As a result of the chemical composition of TSA, these films were also free of chlorine and carbon contamination. The hydrogen concentration in the films, a critical feature related to boron diffusion from the substrate, is as low as the standard silicon nitride processes.

D3.3
MODELING INHERENT ELECTRON TRAPPING PROPERTIES OF HIGH-k DIELECTRIC MATERIALS. Vladimir Zubkov, Grace Sun, Sheldon Aronowitz, LSI Logic, Milpitas, CA; Margaret A. Gabriel, Department of Chemistry, University of Washington, Seattle, WA.

It has been reported that the well-known high-k dielectrics aluminum oxide and hafnium oxide exhibit trapping probabilities that are orders of magnitude higher than that of silicon oxide. This trapping behavior will reduce the acceptable lifetime operation of devices constructed with these dielectric materials or might lead to catastrophic threshold shifts for very sensitive applications. There are at least three possible reasons for electron trapping in these dielectrics: grain boundaries intrinsic to polycrystalline materials, defects in the bulk and at the surface, and inherent bulk electronic properties of these dielectrics. The inherent bulk properties are especially important as other factors can be decreased to some degree, e.g., by amorphization and appropriate surface treatment. Understanding and evaluating intrinsic trapping properties is important as it may be used for predicting trapping properties of currently considered high-k dielectrics as well as of those that might be generated in future. In this work electron affinity (EA) is employed as a measure of electron trapping capability of considered dielectrics. Values of electron affinity have been estimated for two kinds of dielectric bulk models: models with periodic boundary conditions (PBC) and clusters. Both models have been considered within the framework of density functional theory. In agreement with experiment, calculations reveal no EA for both crystalline and amorphous silicon oxide. In the case of hafnium oxide noticeable EA has been calculated for the amorphous phase; some EA also has been calculated for the crystalline phase of hafnium oxide. Estimated EA values are also reported for various metal silicates and some dielectrics containing oxynitrides in combination with transition metals. The relationship between the electronic structure of dielectrics and their inherent electron affinity has been explored.

D3.4
KINETICS of CHARGE GENERATION DURING FORMATION of Hf and Zr SILICATE DIELECTRICS. Theodosia Gougousi and G.N. Parsons, Dept of Chemical Engineering, NC State University, Raleigh, NC.

Understanding charged defects in high dielectric constant insulators is a critical challenge for advanced devices. We have formed thin Zr and Hf silicates by sputtering and examined the effect of formation time and temperature on the flatband voltage from capacitance vs. voltage. Films are formed by depositing a thin metal on clean silicon, and oxidizing in N_2O at 600 or 900°C, and the resulting equivalent oxide thickness (EOT) ranges from 12 to 30Å. We find that the thermal budget during oxidation and the type of oxidizing agent significantly affect the amount of fixed charge in the film. Oxidation of 8Å of Zr metal on Si at 600°C in N_2O for 15s results in EOT=12Å and a shifts in the flatband voltage by ~-0.2V indicating generation of positive fixed charge. For Zr and Hf films longer oxidations in N_2O (up to 300s, with an increase in EOT) show an increase in fixed charge. Direct comparison of Si oxidized in the same environment does not show this extent of flatband voltage shift. A significantly reduced charge generation rate is observed for Hf oxidation under low O_2 partial pressure. Extended oxidations (up to 300s) showed minimal increase in EOT (14Å increased to ~15Å) with a slight decrease in the charged defect state density. X-ray photoelectron spectroscopy indicates formation of Hf-silicate. However, the low O_2 oxidation process results in less silicon incorporation in the film as compared to films oxidized in N_2O. Post metal anneal (PMA) results in partial neutralization of the charge. PMA after the Al gate deposition also leads significant decrease of the EOT (from 27 to 21Å) indicating significant reaction of the film with the gate metal. Results suggest that understanding oxidation mechanisms will be important in isolating and controlling fixed charge in high-k dielectrics.

D3.5
ATOMISTIC SIMULATIONS OF SURFACE CHEMICAL REACTIONS FOR GROWING HIGH-k GATE STACKS. Charles Musgrave, Yuniarto Widjaja, Joseph Han, Dept of Chemical Engineering, Stanford Unviersity, Stanford, CA.

We have used density functional theory to predict the atomistic mechanisms and associated kinetics of atomic layer deposition processes to deposit several materials (ZrO_2, HfO_2, and Hf and Zr silicates) for high-k gate stacks. These processes had not previously been investigated theoretically and our results lead to insight into the details of the process and an explanation of several unanswered questions regarding the deposition of these materials, including an explanation for submonolayer growth which is often observed.

D3.6
PREVENTION OF NATIVE OXIDE REGROWTH FOR HIGH-k GATE DIELECTRICS. K. Choi, H. Harris, S. Gangopadhyay, H. Temkin, NanoTECH Research Center, Texas Tech University, Lubbock, TX.

The existence of sub-monolayer (0.1~0.3 nm) silicon oxide becomes more crucial as the required equivalent oxide thickness goes below 1.5~2 nm, the limit of conventional silicon dioxide gate devices. Controlled interface formation will not only reduce the capacitance of the gate dielectrics, but also the non-uniform nature of the native oxide, which can vary transistor properties such as threshold voltage from cell to cell. Robust hydrogen-termination and an atomically smooth surface are required to prevent the silicon substrate from native silicon oxide formation due to oxidants in the environment. Various cleaning methods are tested in terms of resistance to native oxide formation. Native oxide re-growth behavior versus exposure time to the atmosphere is observed by using ellipsometry. Hafnium dioxide film (k ~20) is deposited on the as-cleaned substrates by electron beam evaporation and subsequently annealed in hydrogen. MOS-Capacitor devices are fabricated by depositing metal electrodes on the specimens. Two important parameters that depend on the combination of the cleaning schemes are defined; residual thickness after etching and re-growth rate. From the monitoring of residual oxide after final etching and subsequent re-growth, we found that the maximum difference between conventional RCA cleaning and the new cleaning method after 1 hour is more than 0.16 nm, which is significant for devices demanding equivalent oxide thickness of <2 nm. Degree of hydrogen passivation, surface micro-roughness and organic removal capability are considered to be the main factors that explain

the differences between the cleaning methods. Data derived from C-V analysis verify the trends resulted by the native oxide thickness measurements. An increase of more than 10% in accumulation capacitance is observed in the samples treated by the new cleaning method.

D3.7
HIGH QUALITY THIN HfO_2 FILMS DEPOSITED VIA ALTERNATING PULSES OF $Hf(NO_3)_4$ AND $HfCl_4$. J.F. Conley, Jr. and Y. Ono, Sharp Labs of America, Camas, WA; R. Solanki, Oregon Graduate Institute, Department of Electrical and Computer Engineering, Beaverton, OR.

The most widely used precursor for ALD of HfO_2 is $HfCl_4$ with H_2O as the oxidant. A major drawback of $HfCl_4$ is that it does not allow uniform initiation of deposition directly on H-terminated Si. Because several initial monolayers of SiO_2 are required to achieve deposition of uniform HfO_2 films, it will be difficult to achieve equivalent oxide thicknesses less than 1.0 nm using $HfCl_4$. We present a novel technique for deposition of HfO_2 that consists of alternating pulses using a combination of two hafnium containing precursors ($Hf(NO_3)_4$ and $HfCl_4$) with N_2 purges between the pulses. An in-situ 400C post deposition anneal densifies and improves the film. H_2O is not used, instead, $Hf(NO_3)_4$ serves as the oxidant. It was found that this method allows deposition of high quality HfO_2 films directly on H-terminated Si, without any "incubation" cycles. The thickness of the resulting films is linearly dependent on the number of cycles (each cycle consists of $Hf(NO_3)_4/N_2/HfCl_4/N_2$). A high deposition rate of approximately ~0.7 nm / cycle was obtained, greater than that for either precursor used individually with H_2O. The deposition rate is independent of temperature over the range of ~150°C-185°C. HfO_2 films were also characterized using spectroscopic ellipsometry (SE), x-ray diffraction (XRD), and x-ray reflectivity. Electrical measurements capacitors on with sputtered TiN gates indicate promising electrical characteristics.

D3.8
ALD OF HrO_2 FROM TETRAKIS(ETHYLMETHYLAMINO) HAFNIUM (TEMAH) AND TETRAKIS(DIMETHYLAMINO) HAFNIUM (TDMAH) AND OZONE. Xinye Liu, Ana Londergan, Anuranjan Srivastava, Stefano Rassiga, Jerry Winkler, Sasangan Ramanathan, Eddie Lee, and Tom Seidel, Genus, Inc., Sunnyvale, CA.

Hafnium oxide (HfO_2) thin films were synthesized from tetrakis(ethylmethylamino) hafnium (TEMAH) and ozone (O_3) by atomic layer deposition (ALD) on 200 mm silicon wafers. Non-ideal saturation was observed for TEMAH. However O_3 showed very good saturation behavior within the range that was studied, which indicates that O_3 is a good ALD reactant in combination with TEMAH. Within wafer non-uniformity (WIWNU) of less than 1% was achieved. 100% step coverage was achieved for ~100nm trenches with aspect ratio of 34 to 44. Film thickness increased linearly as number of cycles increased. Temperature dependence of deposition rate was studied at susceptor temperature from 160°C to 420°C. Lowest deposition rate and highest refractive index was observed at 320°C. Carbon and hydrogen content decreased as susceptor temperature increased from 200°C to 320°C. Films made with H_2O had lower carbon and hydrogen level than that of films made with O_3. The difference of impurity level between O_3 based films and H_2O based ALD films decreased as temperature increased. Mercury probe measured dielectric constant increased from 16 to 20 as susceptor temperature increased from 200°C to 320°C. Mechanism of O_3 based ALD process was discussed. Selected comparisons with tetrakis (dimethylamino) hafnium (TDMAH) were also made. Our experiments show that O_3 based ALD HfO_2 deposition with these precursors are very promising for advanced capacitor mass production.

D3.9
ATOMIC LAYER DEPOSITION OF HAFNIUM OXIDE USING METAL-ORGANIC PRECURSORS AND OZONE.
Yoshihide Senzaki, S.G. Park, Randall Higuchi, Eugene S. Lopata, S.I. Lee, and Aubrey Helms Jr., ASML Thermal Division, Scotts Valley, CA.

The need for high-k gate dielectrics with CMOS integration was identified in the International Technology Roadmap for Semiconductors (ITRS). Conventional SiO_2 gate dielectrics are limited below 20$\AA$ due to the increase of quantum tunneling as integrated circuits are reduced in size. For low power consumption applications where the gate leakage current is below $10^{-7}A/cm^2$, high-k dielectrics having stability with Si gate are needed at the 65nm node. HfO2 has been extensively studied as a promising high-k gate dielectric candidate due to its high permittivity, good thermal stability and large band offset to Si. Charge trapping related to Vt (threshold voltage) instability, and electron mobility degradation in MOSFET performance are the most serious concerns for the integration of HfO_2 as a high-k dielectrics. One of the sources for the fixed and trapped charge is OH-, a prevailing impurity in H_2O-based high-k dielectric, which can be eliminated by using ozone as an oxidant in lieu of H_2O. We have developed processes to deposit hafnium oxide film using atomic layer deposition (ALD) with metal-organic precursors and using ozone as an oxygen source. The hafnium precursors used in this study are volatile liquids. A comparison was made in film quality and deposition performance among the precursors. The use of ozone allows ALD processes at temperatures below 300°C and provides HfO_2 thin films with good electrical properties.

D3.10
EVALUATION OF TETRAKIS(DIETHYLAMINO)HAFNIUM PRECURSOR IN THE FORMATION OF HAFNIUM OXIDE FILMS USING ATOMIC LAYER DEPOSITION. Ronald Inman, Anand Deshpande, and Gregory Jursich, American Air Liquide, Countryside, IL.

Due to their thermodynamic compatibility with Silicon interface and high dielectric constant, films containing hafnium oxide are becoming strong candidates in replacing Silicon oxynitride as the gate dielectric layer in CMOS devices. To achieve ultimate conformality and thickness control, atomic layer deposition is receiving much more attention in recent years for nanometer size film applications. For hafnium oxide deposition by ALD, metal chlorides have traditionally been used as precursors with moisture being the co-reactant; however for gate oxide applications, metal chlorides are not considered suitable due to the corrosive nature of these compounds and the risks of film contamination. Hence, researchers are exploring alternate organometallic precursors in a CVD process with oxygen being the co-reactant. In this work, tetrakis diethylamino hafnium precursor is used in an ALD process with moisture co-reactant to deposit Hafnium oxide films onto H-terminated Si substrate in a temperature regime of 200 to 350 C. Film composition is determined by x-ray analysis and is found to be stoichiometric without residue from ligand decomposition. Film thickness and uniformity is measured by reflectometry. Film growth rate is measured as a function of substrate temperature and reagent pulsing characteristics. These results will be presented and compared with that obtained with the more conventional hafnium chloride precursor.

D3.11
CHARACTERISTICS OF HfO_2 GATE DIELECTRIC DEPOSITED BY REMOTE PLASMA ENHANCED ATOMIC LAYER DEPOSITION METHOD. Ju Youn Kim, Do Youl Kim, Yangdo Kim, and Hyeongtag Jeon, Division of Materials Science & Engineering, Hanyang Univ., Seoul, KOREA.

As the metal oxide semiconductor device continues scale down, the high-k gate dielectrics become one of the solutions in providing increased capacitance and reduced leakage currents without significantly increasing the actual equivalent oxide thickness (EOT) of gate dielectrics. Among the high-k materials, hafnium oxide (HfO_2) is considered to be one of the potential replacements of SiO_2 gate oxide due to its high dielectric constant and good thermal stability in contact with silicon. In this study, we investigated the HfO2 gate dielectric deposited by remote plasma enhanced atomic layer deposition (PEALD) method using metal organic source. HfO2 films were deposited at 200~350°C using tetrakis-dimethyl-amido- hafnium (TDEAH) as Hf precursor and oxygen plasma as reactant gas at the various process pressures. The electrical properties of MOS capacitor were measured after post metal annealing. The physical and chemical characteristics of HfO_2 film were analyzed by cross-sectional transmission electron microscope (XTEM), Auger electron spectroscopy (AES), X-ray photoelectron spectroscopy (XPS) and Rutherford backscattering spectroscopy (RBS). The electrical properties and reliability characteristics including EOT, hysteresis, leakage current and capacitance were evaluated by I-V and C-V measurements. This paper will present the characteristics of HfO_2 gate dielectric deposited by remote PEALD using metal organic precursor.

D3.12
INVESTIGATION OF W/HfO_2 METAL OXIDE SEMICONDUCTOR CAPACITORS. V. Narayanan, P. Jamison, A. Callegari, S. Zafar, F.R. McFeely, D. Neumayer, P. Ranade[a], C. Cabral Jr., M. Copel and M.A. Gribelyuk[b], Semiconductor Research and Development Corporation (SRDC), IBM T.J. Watson Research Center, Yorktown Heights, NY. [a]Department of Electrical Engineering & Computer Science, University of California, Berkeley, CA; [b]IBM Microelectronics Division, Hopewell Junction, NY.

W has a midgap workfunction and has been studied in combination with HfO_2 as a possible candidate for metal gate/high k CMOS devices. In this work, we have investigated the effect of post metal anneals on W gated HfO_2 capacitors with respect to the thermal stability of the gate stack, shifts from the ideal flatband condition, changes in capacitance equivalent thickness (CET, no quantum mechanical correction) and charge trapping. Capacitance-Voltage

(C-V) measurements on as deposited W/HfO_2 films result in a CET $\sim$15.5$\AA$, low C-V hysterisis, and low leakage ($6x10^{-4}$A/cm^2). However, high frequency CVs clearly show the presence of a high density of interface states. Post metal anneals are required to eliminate these interface states and result in an increase of the CET. Structural analysis of the as deposited gate stack by high resolution transmission electron microscopy (HRTEM) shows a well defined W/HfO_2 interface in contrast to as deposited Al/HfO_2 interfaces which clearly show a reacted layer and also a higher CET for the same thickness of stack. Upon post metal annealing, HRTEM images of W/HfO_2 indicate a thickening of the interfacial layer between the HfO_2 and Si, corroborating the increase in CET. Annealed W/HfO_2 films have a CET $\sim$16.5 $\AA$, low C-V hysterisis $<$ 15 mV, leakage 5 orders of magnitude better than an equivalent SiO_2 film and minimum flatband shift (extracted workfunction of W $\sim$4.7 eV) indicating little fixed charge in the gate stack. In addition, charge trapping has been monitored in these films as a function of different rapid thermal anneals.

D3.13
YTTRIUM STABILIZED HfO2 EPITAXIAL THIN FILMS - A NEW APPROACH FOR HIGH-k GATE DIELECTRIC. P.F. Lee, J.Y. Dai, H.L.W. Chan and C.L. Choy, Department of Applied Physics, Hong Kong Polytechnic University, Hung Hom, Kowloon, Hong Kong, CHINA.

HfO2 is an attractive candidate for high-k gate dielectric due to its thermodynamic stability on Si under high temperature annealing. Epitaxial growth of HfO2 thin films on Si is of significant fundamental and technological interest, even though the amorphous structure has been commonly accepted as the approach to select high-k gate dielectric candidates. We report successful epitaxial growth of yttrium stabilized HfO2 thin films on p-type (100) Si substrates by pulsed laser deposition at relatively lower substrate temperature of 550°C. Transmission electron microscopy observation illustrated a fixed orientation relationship between the epitaxial films and Si substrates, i.e. (100)Si||(100)HfO2 and [001]Si//[001]HfO2. However, the rough film/Si interface suggests that interdiffusion and interfacial reaction at the interface may happen. High-resolution deep profile X-ray photoelectron spectroscopy analysis (XPS) revealed Hf silicate formation at the interface area. Very next to Si surface, XPS spectra also show the presence of Hf-Si bonding. Capacitance-voltage measurement revealed that the an equivalent SiO2 thickness of about 10Å has been achieved by a 40Å-thick epitaxial yttrium stabilized HfO2 film with a leakage current density of 1x10-2A/cm2 at 1 V gate bias voltage. The growth mechanism of the yttrium stabilized HfO2 thin films on Si has been studied and it was found that substrate temperature is a critical parameter for the epitaxy of yttrium stabilized HfO2 films. Substrate temperature higher than 600°C causes SiO2 formation on Si surface before film deposition and therefore prevents the intended epitaxial growth. On the other hand, the films grown at substrate temperature lower than 450°C also resulted in polycrystalline structure even the interface is free from SiO2 layer. This can be interpreted by relatively lower kinetic energy of Hf and O atoms arrived at the Si surface at lower substrate temperature leading to island growth of the films.

D3.14
MICROSTRUCTURAL EVOLUTION OF ZrO_2/HfO_2 NANO-LAMINATE GATE STACKS GROWN BY ATOMIC LAYER DEPOSITION. Hyoungsub Kim, Man-Ho Cho[a], Paul C. McIntyre, Stanford Univ., Dept of Materials Science & Engineering, Stanford, CA; Krishna Saraswat, Stanford Univ., Dept of Electrical Engineering, Stanford, CA; [a]currently at Korea Research Institute of Standards and Science, Daejon, KOREA.

Among many possible high-k dielectric candidates for the future sub-nanometer MOSFET devices, ZrO_2 and HfO_2 are attractive because of their relatively high dielectric constant and large bandgap. Although ZrO_2 and HfO_2 have similar electrical properties, including their dielectric constants, ZrO_2 is typically deposited as a polycrystalline (tetragonal) phase and HfO_2 as amorphous, especially using low thermal budget processes such as atomic layer deposition (ALD). In this presentation, microstructural evolution and electrical properties of nanolaminate structures composed of alternating ZrO_2 and HfO_2 layers will be investigated. In order to obtain extremely precise thickness and interface control without breaking vacuum, ALD was used because excellent film quality can be achieved owing to its surface adsorption-controlled deposition mechanism. A cold wall ALD system with $ZrCl_4/H_2O$ and $HfCl_4/H_2O$ precursors for ZrO_2 and HfO_2, respectively, were used and the deposition was carried out at 300°C on a p-type Si substrate having $\sim$15$\AA$ chemical or thermally grown SiO_2 surface passivation. Alloy and nanolaminate structures having different layer sequences with different numbers of layers were grown and their film microstructures were investigated using HR-TEM imaging and electron diffraction. Nanolaminate structures composed of ZrO_2 layers larger than a characteristic thickness had a polycrystalline structure with both tetragonal and monoclinic phases, and their surface roughness and final film grain size strongly depended on the identity of the initial layer deposited. Electrical properties such as C-V and I-V characteristics were evaluated using Pt gate capacitors fabricated through a shadow mask process.

D3.15
COMPARISON OF UV-OZONE PROCESSED HfO_2 AND ZrO_2 HIGH-κ GATE DIELECTRICS. David Chi, Shriram Ramanathan, and Paul C. McIntyre, Department of Materials Science and Engineering, Stanford University, Stanford, CA.

Oxidation of thin metal films in the presence of ultraviolet light has been shown to produce high quality metal oxide gate dielectric layers. The oxides of hafnium and zirconium are both considered potential high-κ replacements for SiO_2 in future MOS devices. Growth kinetics for these two metal oxides under UV-ozone conditions is compared using imaging (HRTEM) and ion scattering (NRA) techniques. The primary advantage of nuclear reaction analysis (NRA) is its high sensitivity to oxygen. Accurate measurements of oxygen areal density were used to calculate effective metal oxide thicknesses. Results from NRA were corroborated using HRTEM. Our results show that the UV-ozone process can be used to fabricate gate oxides of the thickness required for the gate dielectric application. Electrical measurements (CV, IV) on MOSCAP structures demonstrate the promise of UV-ozone grown HfO_2 and ZrO_2 as gate dielectrics on Si substrates passivated by an ultrathin SiO_2 layer. Capacitance-derived EOT values of 1.5-2.0 nm (without quantum mechanical corrections) were obtained for starting metal precursor thicknesses of 2.0 nm, corresponding to 2.5-3.5 nm final metal oxide layer thickness. Leakage current densities were on the order 10^{-4} A/cm^2 at 1 V bias. Electrical results obtained were highly dependent upon the surface passivation of the silicon substrate. Several passivation methods will be discussed. The procedure yielding the optimum electrical results entailed an HF strip followed by a low P_{O2} UV-ozone re-oxidation of the Si surface.

D3.16
EFFECTS OF Ge ON THE ELECTRICAL PROPERTIES OF MOS CAPACITOR WITH POLY Si/HfO_2 AND POLY $Si_{0.4}Ge_{0.6}$/HfO_2 GATES STACK AFTER VARIOUS ANNEALING VARIOUS ANNEALING CONDITION. B.G. Min, S.K. Kang, S. Nam, S.W. Nam, D.-H. Ko, Department of Ceramic Engineering, Yonsei University, Seoul, KOREA; H.B. Kang, C.W. Yang, School of Metallurgy and Material Engineering, Sung Kyun, Kwan University, Suwon, Kyounggi-do, KOREA; K.Y. Lim, Memory Research and Development Division, Hynix Semiconductor Inc, Ichon, Kyounggi-do, KOREA.

Recently, high K dielectric films have been suggested as alternatives to the currently employed SiO_2 gate dielectric for CMOS-FET technology since high k dielectric films reduce the leakage current and improve the reliability without decreasing oxide capacitance. Among the suggested materials, HfO_2 films have received attention due to the high k value, wide band gap, and low heat of formation. In addition, HfO_2 films are compatible with conventional CMOS processes including a poly silicon gate electrode without any barrier layer. In spite of previous studies, long time and high temperature annealing is expected to bring about the silicidation in the poly Si/ HfO_2 system, as like poly Si/ZrO_2 system, due to the similar chemical properties. Furthermore, as the gate depletion effect and boron penetration becomes more prominent for the sub-10A oxide regime, it is importantly considered that other gate material, such as a metal gate and poly $Si_{1-x}Ge_x$ films, have to replace poly Si. In our experiments, poly $Si_{0.4}Ge_{0.6}$ films were deposited on HfO_2 films as a gate electrode to compare with the electrical results of the poly Si/ HfO_2 gates stack after annealing. It is well known that the Ge in the epi $Si_{1-x}Ge_x$ films retarded the silicidation in the Ti, Co, Zr/ $Si_{1-x}Ge_x$ system as compared to the Co, Ti, Zr/Si system. From these previous results, compared with poly Si/ HfO_2 system, the silicidation will be retarded in poly $Si_{1-x}Ge_x$/ HfO_2 system after annealing and then, the retardation of silicidation is expected to bring about other reaction, silicate formation, in poly $Si_{1-x}Ge_x$/ HfO_2. HfO_2 films and poly $Si_{1-x}Ge_x$ (x=0, 0.6) films were deposited by using a DC magnetron sputtering and a low pressure chemical vapor deposition (LPCVD) system. After the formation of the MOS structure, the specimens were annealed from 700°C to 900°C in N_2 ambient for 5min and the electrical properties were measured by using C-V and I-V measured.

D3.17
HIGH-κ METAL OXIDES DIELECTRICS ON Ge (100) SUBSTRATES. David Chi, Baylor B. Triplett, and Paul C. McIntyre, Department of Materials Science and Engineering, Stanford University, Stanford, CA; Chi On Chiu and Krishna C. Saraswat, Department of Electrical Engineering, Stanford University, Stanford, CA; Eric Garfunkel and Torgny Gustafsson, Departments of Chemistry and Physics, Rutgers University, Piscataway, NJ.

As a semiconductor channel material for use in future scaled MOS transistors, Ge has the advantage of enhanced low-field mobility compared to Si. However, a primary drawback that has limited use of Ge surface channel devices is the absence of a stable Ge oxide that can serve as a dielectric and a surface passivation. With the expected introduction of deposited high-κ dielectrics in MOS technology, the poor quality and stability of GeO_2 may no longer be a significant obstacle to development of Ge-channel field effect transistors. Growth of ZrO_2-based gate dielectrics on Ge (100) substrates is reported in this presentation. UV-ozone oxidation is used to fabricate ultrathin metal oxide dielectrics. ARXPS, MEIS, and HRTEM have been used to characterize the gate stack structure with atomic resolution. A comparison of the gate stack structure of ZrO_2/Si and ZrO_2/Ge will be presented. Promising electrical results obtained from MOSCAP and MOSFET structures will also be presented, demonstrating important functional characteristics of high-κ/Ge gate stacks.

D3.18
Abstract Withdrawn.

D3.19
Abstract Withdrawn.

D3.20
HfO2, Al2O3 AND HfAlOx HIGH-k DIELECTRICS CHARACTERIZED BY VUV SPECTROSCOPIC ELLIPSOMETRY. Pierre Boher and Christophe Defranoux, SOPRA, Bois-Colombes, FRANCE; Hugo Bender, IMEC, Leuven, BELGIUM.

New high k dielectric materials are intensively investigated to replace the silicon dioxide as gate dielectric in the next generations of electronic devices. Several candidate materials and deposition processes are currently under investigation but the technological problem is difficult due to the specifications of these new materials not only in terms of electrical properties but also for the compatibility with the fabrication process of the devices. In any case, the layer thickness which will be used in the future devices is of the order of some nanometers and a precise control of this critical stage of the process will be mandatory. In this respect, spectroscopic ellipsometry has long been recognized as a powerful technique for thin film characterization and is now used routinely to control thin films and multilayers at different stages of the device fabrication process. For very thin layers like high k dielectrics, the situation is complicated by the fact that the interface properties play a key role in the device. A precise physical model is then needed to extract accurate information from ellipsometry. In addition, since these layers are completely transparent in the visible and UV range, the correlation between thickness and refractive index is very high and so, structural and thickness information cannot be extracted independently. In this paper, we use vacuum UV (VUV) spectroscopic ellipsometry to characterize such layers. Indeed, all the candidates for high k dielectrics become absorbent when the wavelength is reduced down to 190nm. So, the correlation between thickness and refractive index is reduced in the VUV range and more precise structural information can be deduced. HfO2, Al2O3 and mixed HfAlOx layers have been deposited by Atomic Layer Deposition (ALD) on a 1 nm oxide grown in-situ by rapid thermal oxidation (RTO) on 200 mm (100) silicon wafers. The thickness and the composition of the layers has been changed and some wafers have been annealed in a nitrogen ambient at 700°C after the deposition. X-ray reflectometry (XRR) has been used to measure precisely the layer thickness and transmission electron microscopy (TEM) was used to get information on the crystallinity and on the interface properties. In particular, it will be shown that VUV spectroscopic ellipsometry can detect the crystalline character of the HfO2 layers thanks to the absorption peaks detected in the VUV range. The composition of HfAlOx layers can also be deduced in addition to the layer thickness from the optical absorption in the same wavelength range.

D3.21
FLAT-BAND VOLTAGE STUDY OF ATOMIC-LAYER-DEPOSITED ALUMINUN-OXIDE SUBJECTED TO SPIKE THERMAL ANNEALING. A.T. Fiory, V.R. Mehta, and N.M. Ravindra, New Jersey Institute of Technology, Newark, NJ; Mun Yee Ho and G.D. Wilk, Agere Systems, Berkeley Heights, NJ; T.W. Sorsch, Bell Laboratories, Lucent Technologies, Murray Hill, NJ.

High-K dielectrics based the oxide of Al were prepared by atomic layer deposition (ALD) on 200-mm diameter Si wafers in an ASM Pulsar ALCVD system. Films were deposited directly on clean Si or on ~0.5-nm underlayers of chemical oxide, rapid thermal oxide, and rapid thermal oxynitrides grown in NO and a mixture of O_2 and NO. The purpose of the underlayer films is to provide a barrier for atomic diffusion from the crystalline Si to the high-K dielectric film. Deposited Al-oxide films varied in thickness from 2 to 6 nm. Post deposition anneals were used to stabilize the ALD oxides. Equivalent oxide thickness varied from 1.5 to 3.5 nm. In situ P-doped 160-nm amorphous-Si films were deposited over the oxides to prepare heavily-doped gate electrodes in the MOS structures. Samples were rapid thermal annealed in N_2 ambient at 800°C for 30 s, or spike annealed at 950, 1000, and 1050°C (nominally zero time at peak temperature). Heating and cooling rates are approximately 50°C /s. Flat band voltages (V_{FB}) were determined from C-V measurements on dot patterns. The 800°C anneals were used as a baseline, at which the poly-Si electrodes are crystallized and acquire electrical activation while subjecting the high-K dielectrics to a low thermal budget. Positive shifts in V_{FB} were observed, relative to a pure SiO_2 control, ranging from 0.2 to 0.8V. Spike annealing changes V_{FB} towards that for SiO_2 for ALD films deposited over underlayer films. The V_{FB} shift and the changes with annealing temperature show systematic dependence on the nitridation of the underlayer.

D3.22
LS-MOCVD OF BARIUM STRONTIUM TITANATE THIN FILMS USING NOVEL PRECURSORS. Hyun Goo Kwon, Young Woo Oh, Jung Woo Park, Young Kuk Lee, Chang Gyoun Kim, Yunsoo Kim, Thin Film Materials Laboratory, Advanced Materials Division, Korea Research Institute of Chemical Technology, Daejeon, KOREA; Do Jin Kim, Department of Materials Engineering, Chungnam National University, Daejeon, KOREA.

BST have attracted much attention in memory devices due to their high dielectric constants. However, low volatility of the Ba or Sr precursors with only thd ligands has limitations in obtaining high quality thin films by liquid source metal organic chemical vapor deposition (LS-MOCVD) processes. To improve the volatility of these precursors, many attempts have been made such as adding polyether ligands to satisfy the coordinative saturation. We report the synthesis of new precursors $Ba(thd)_2$(tmeea) and $Sr(thd)_2$(tmeea), where tmeea = tris[2-(2-methoxyethoxy)ethyl]amine, and LS-MOCVD of barium strontium titanate (BSTO) thin films using these precursors. Due to increased basicity of amines compared with ethers, it is expected that the nitrogen-donor ligand will make a strong bond to a metal than an analogous oxygen-donor ligand, consequently improving the volatility and thermal behavior of these precursors. Thin films of BSTO were grown by LS-MOCVD using a cocktail source consisting of the conventional Ti precursor $Ti(thd)_2(OiPr)_2$ and these new Ba and Sr precursors. As-grown films were characterized by XPS, SEM, XRD, XRF, and C-V and I-V measurements. BSTO films grown at 420°C were stoichiometric BST with very smooth surface morphology and their dielectric constants were found to be as large as 450. Dependence of the composition and the electrical properties of the BSTO films on the growth temperature, working pressure, and the composition of the cocktail source will be discussed.

D3.23
METAL-ORGANIC CHEMICAL VAPOR DEPOSITION OF Pr_2O_3 FILMS ON SILICON SUBSTRATES. Raffaella Lo Nigro and Vito Raineri, Consiglio Nazionale delle Ricerche, IMM-sezione di Catania; Roberta Toro, Graziella Malandrino, Ignazio Fragala, Univ of Catania, Dept. of Chemistry, Catania, ITALY.

In recent years, Pr_2O_3 has received much attention because of the possible use as alternative gate dielectrics in CMOS devices. Physical vapor deposition methods have been successfully used to grow Pr_2O_3 films on silicon substrates, while, to date, there are no studies on chemical vapor deposition methods. We report on the results of a recent study on the deposition of praseodymium oxides thin films on silicon substrates by metal-organic chemical vapor deposition (MOCVD). Suited Pr(III) b-(diketonate) precursor has been used as the metal source and the deposition conditions have been carefully selected because of a large variety of possible PrO_{2-x} (x= 0-0.5) phases. Pr_2O_3 films have been obtained in a non oxidizing ambient in an hot-wall MOCVD reactor, using 750°C deposition temperature, while Pr_6O_{11} films were formed using 50-100 sccm oxygen flow as reaction gas. The structural and morphological characteristics of Pr_2O_3 films were carried out by X-ray diffraction (XRD), high resolution transmission electron microscopy (TEM) and atomic force microscopy (AFM). Chemical compositional studies have been performed by energy filtered transmission electron microscopy (EFTEM) analysis and a fully understanding of the MOCVD process has been achieved. Preliminary electrical measurements point to MOCVD as a reliable growth technique to obtain good quality Pr_2O_3 films.

D3.24
INTERFACE CHARACTERIZATION OF THE HIGH-k GATE DIELECTRIC Pr_2O_3. Hans-Joachim Müssig and Jarek Dąbrowski, IHP, Frankfurt (Oder), GERMANY; Dieter Schmeisser, Angewandte Physik-Sensorik, BTU Cottbus, Cottbus, GERMANY.

Pr_2O_3 is currently under consideration as a potential alternative gate dielectric candidate for sub-0.1 μm Complementary Metal Oxide Semiconductor (CMOS) technology [1-3]. For all thin gate dielectrics,

the interface with silicon plays a key role, and in most cases is a dominant factor in determining overall electrical properties. Most of the high-k metal oxide systems investigated so far have unstable interfaces with Si. In order to maintain a high-quality interface and channel mobility, it will be important to have no metal oxide or silicide phases present at or near the channel interface. We studied the Pr_2O_3/Si(001) interface by a non-destructive depth profiling using synchrotron radiation photo-electron spectroscopy and *ab initio* calculations. Our results provide evidence that a chemical reactive interface exists consisting of a mixed Si-Pr oxide such as $(Pr_2O_3)_x(SiO_2)_{1-x}$, typically in non-stoichiometric composition. There is no formation of neither an interfacial SiO_2 nor interfacial silicide: all Si-Pr bonds are oxidized and all SiO_4 units dissolve in the Pr oxide. Interfacial silicates like $(Pr_2O_3)_x(SiO_2)_{1-x}$ are promising high-k dielectric materials because they represent incremental modification of SiO_2 films by Pr ions so that the interface characteristics can be similar to Si-SiO_2 interface properties. The ternary phase diagram, determined experimentally for the first time, indicates that this non-stoichiometric pseudobinary alloy remains amorphous and stable on Si up to high temperatures, without phase separating into crystalline Pr_2O_3 and SiO_2. Under ultrahigh vacuum conditions, silicide formation is observed when the silicate film is heated above 800°C. The praseodymium silicate system observed at the interface between Si(001)and Pr_2O_3 offers greater flexibility towards integration of Pr_2O_3 into future CMOS technologies. [1] H. J. Osten et al., IEDM Technical Digest (2000) 653. [2] H.-J. Müssig et al., 2001 IEEE International IRW - Final Report (USA), 1. [3] H.-J. Müssig et al., Surf. Sci. 504C (2002) 159.

D3.25
SEARCHING NEW HIGH-κ DIELECTRICS BY COMBINATORIAL CVD. Bin Xia, Department of Chemistry; Jeffery T. Robberts, Department of Chemistry; Stephen A. Campbell; Department of Electronic Engineering; Wayne L. Gladfelter; Department of Chemistry; University of Minnesota, Minneapolis, MN.

To develop a high-κ gate dielectric for replacing SiO_2 in MOSFETs, multicomponent metal oxides could have advantages over single metal oxides because they may have higher dielectric constants (κ's) and other favorable properties. However, to find the optimum elemental ratio for obtaining a good dielectric from the given component oxides is a time-consuming and costly work, especially when three or more oxides are involved. Recently, we invented a combinatorial CVD technique to deposit compositional spreads of ternary metal-oxides for searching new high-κ dielectrics. In the current work, we use this to study compositional spreads of ZrO_2, SnO_2 and HfO_2 deposited using anhydrous metal nitrates. Extending three vertical precursor injectors in a low-pressure CVD reactor so that their exits are close (H = 5-10 mm) to the surface of the horizontal substrate allows each symmetrically distributed precursor flux to spread on the substrate, mix with the other two components and form a compositional spread. The chemical composition and the film thickness primarily depend on the distances between the spot and each of the three injectors, as well as experimental parameters such as the substrate temperature, precursor fluxes, and gas flow rates. By measuring chemical composition, film thickness, and electrical properties, we are able to map the κ (and other electrical properties) and establish its dependence on chemical composition. This high-throughput deposition technique allows us to screen film electrical properties rapidly and reliably. In addition to the electrical properties, this technique also offers us an excellent chance to explore the formation of new crystalline phases due to numerous possible reactions among the component oxides in a compositional spread. A crystalline phase, α-PbO2, which does not exist in any of the three pure oxides was observed along with monoclinic ZrO_2, HfO_2, and rutile SnO_2.

D3.26
$Si_{0.85}Ge_{0.15}$ OXYNITRIDATION IN WET-NITRIC OXIDE AMBIENTS. Anindya Dasgupta, Christos G. Takoudis, University of Illinois at Chicago, Dept of Chemical Engineering, Chicago, IL; Yuanyuan Lei, Nigel D. Browning, University of Illinois at Chicago, Dept of Physics, Chicago, IL.

Nitric oxide (NO) aided $Si_{0.85}Ge_{0.15}$ wet-oxynitridation has been performed at 400°C, 500°C, 600°C, and 700°C, while the wet-NO feed gas was preheated to higher temperatures before entering the reaction zone. X-Ray photoelectron spectroscopy (XPS) and secondary ion mass spectroscopy (SIMS) data suggests that both nitrogen and oxygen incorporation increases within the dielectric bulk with increasing wet-oxynitridation temperature, while there is no germanium segregation towards the dielectric/substrate interface at all temperatures studied. Moreover, angle-resolved XPS analysis suggests that increase in wet-oxynitridation temperature above 600°C volatilizes some germanium oxide from the surface region, while silicon monoxide is found to outgas from the dielectric bulk and accumulate near the surface. Nitrogen incorporation is found to stop germanium segregation, since, wet or dry oxidation at the above-specified temperatures is known to cause germanium segregation. Z-contrast imaging with scanning transmission electron microscopy (STEM) shows that the oxynitride grown in wet-NO at 600°C has a sharp interface with the bulk $Si_{0.85}Ge_{0.15}$, while the roughness of the dielectric/$Si_{0.85}Ge_{0.15}$ substrate interface is less than 2 Å. These results are discussed in the context of an overall mechanism of SiGe wet-oxynitridation.

D3.27
ORGANOMETALLIC RUTHENIUM MOCVD PRECURSORS. David M. Thompson, Cynthia Hoover, John Peck, David Peters, Praxair, Inc. Tonawanda, NY.

Films of ruthenium are currently receiving considerable attention as potential candidates for capacitor electrodes due to their low resistivities, good susceptibilities to dry etching, and the conductivity of the RuO_2 oxide phase. Most recently, 1,1′-diethylruthenocene has been described in the literature as a promising candidate for this application. As the substituents on the ruthenium metal center are varied the physical properties of the precursor can change significantly. Novel ruthenium compounds have been synthesized and will be compared to 1,1′-diethylruthenocene. Precursor properties, such as thermal stability, vapor pressures, and viscosities will be presented. Furthermore, results from ruthenium films deposited on an SiO_2/Si substrate using the most promising candidate precursor(s) will be discussed and compared to films generated from 1,1′-diethylruthenocene. XPS and Auger results will be used to analyze film composition, crystallinity and the degree of film orientation as determined by XRD. The results from SEM and AFM measurements will be shown to compare the thickness and morphology of deposited films from different precursors. Resistivities and thermal stabilities of the films will be presented.

D3.28
ATOMIC LAYER DEPOSITION OF Ti-Al-N THIN FILMS AS AN OXYGEN DIFFUSION BARRIER FOR FUTURE HIGH-DENSITY VOLATILE MEMORY CAPACITORS. Yong Ju Lee, Ja-Yong Kim, Sang-Won Kang, Korea Advanced Institute of Science and Technology (KAIST), Department of Materials Science and Engineering, Daejeon, REP. OF KOREA.

Ferroelectric random access memory (FRAM) has been touted as a possible future memory device. Since ferroelectric films are typically prepared at annealing temperatures ranging from 600 to 700°C in a strong oxygen environment, the polysilicon plug is easily oxidized, and forms an insulating layer of SiO_2, which severely degrades the device performance. Therefore, it is necessary to develop a high-temperature diffusion barrier to prevent oxidation of the polysilicon plug. TiN has been extensively studied as a diffusion barrier in advanced integrated circuit devices, suggesting that TiN can be introduced without any difficulties into existing or future ultra-large-scale processes. However, TiN films oxidize noticeably at temperatures above 500°C forming TiO_2 (rutile structure). In this study we have investigated the Ti-Al-N films deposited by plasma-enhanced atomic layer deposition (PEALD). Ti-Al-N films were synthesized from tetrakisdimethylamino-titanium (TDMAT), NH_3, and trimethylaluminum (TMA) at a low temperature (180°C) using PEALD. A hydrogen plasma was used as a reducing agent for TMA and to improve film quality. One cycle of Ti-Al-N deposition consisted of TiN and Al steps, and the Ti-Al-N cycles were then repeated until the desired thickness was obtained. The growth rate was saturated at 0.35 nm/cycle, which made it easy to control the film thickness concisely. Ti-Al-N films had excellent surface morphology and good step coverage on a patterned structure, which resulted from the self-limiting surface reactions. Ti-Al-N films are polycrystalline with a hexagonal $Ti_3Al_2N_2$ structure and good oxidation resistance when O_2 annealed at 700°C for 30 min.

SESSION D4/G1: JOINT SESSION
HETEROGENEOUS INTEGRATION AND STRAINED Si TECHNOLOGIES
Chairs: Tsu-Jae King and Timothy D. Sands
Wednesday Morning, April 23, 2003
Golden Gate C1/C2 (Marriott)

8:30 AM *D4.1/G1.1
HETEROGENEOUS INTEGRATION OF SiGe, Ge, AND GaAs WITH Si. E.A. Fitzgerald, Department of Materials Science and Engineering, Cambridge, MA.

A long sought after goal has been to expand the product offerings in semiconductors through the use of new materials. Traditionally, new materials required new and sometimes novel infrastructure to process and manufacture materials and devices. One of the barriers to utilizing incumbent manufacturing infrastructure has been the

dissimilarity in semiconductor materials. For example, lattice mismatch between semiconductor materials has prevented most novel materials from being monolithically integrated on a common substrate. In this talk, we show that relaxed SiGe is a pathway for introducing novel semiconductor materials in Si CMOS infrastructure. Although strained Si is now attracting much interest, strained SiGe and Ge heterostructures integrated on Si may offer even greater performance enhancements. In addition, we have demonstrated continuous wave, room temperature GaAs and InGaAs lasers on Si using this materials technology. As the use of relaxed SiGe increases, increased Ge concentration allows the introduction of more complex heterostructures for electronics and optoelectronics. We also show that relaxed SiGe on Si creates a new path for wafer bonding, in which relaxed SiGe, Ge, and GaAs across entire Si substrates can be transferred to Si wafers and SiO_2/Si wafers. These integrated materials structures are promising for the monolithic integration of advanced electronics and optoelectronics with Si CMOS.

9:00 AM *D4.2/G1.2
CHALLENGES AND OPPORTUNITIES FOR HIGH PERFORMANCE MOSFETS WITH STRAINED Si/RELAXED SiGe CHANNEL. Ken Rim, IBM SRDC, T.J. Watson Research Center, Yorktown Heights, NY.

Strained Si/relaxed SiGe MOSFETs have received considerable amount of attention as the device structure that can provide performance boost to silicon CMOS technology. The enhancement is the result of change in electronic properties of Si under strain, and therefore is largely in addition to the benefits provided by continued geometric scaling of devices. Analysis shows that strain-induced mobility/current increase can be used to improve trade-offs in scaling scenarios for high performance CMOS technology. Electrical characterizations on fabricated MOSFETs have quantified the strain dependence of electron and hole mobility as well as the impacts due to strain-induced band offsets. The results help define the challenges for obtaining enhancements for both NFET and PFETs in a cost-effective manner with minimal disturbance to device and circuit design. On the other hand, dislocation defect formation in strained heterolayers is critical to the layer design and process windows in device integration. The impact of strain on the performance is not as readily quantified in aggressively scaled devices since many factors contribute to the characteristics and performance of scaled MOSFETs. Interactions between lattice mismatch-induced strain and fabrication process-induced stress can make analysis very complicated. Material analysis and novel electrical measurements were used to probe the impact of strain in very small devices, showing that strain-induced mobility enhancement can be retained even in sub-100 nm channel lengths. Si/SiGe heterostructures allow novel device structures and process techniques suitable for ultra-thin body devices. Such devices can combine the advantages of enhanced transport in strained layers and extreme device scaling enabled by ultra-thin body and double gate structures. Some of the progresses in materials and device structures will be presented.

9:30 AM D4.3/G1.3
RELAXATION OF A COMPRESSED FILM ON A COMPLIANT SUBSTRATE: EXPANSION, WRINKLING, AND FRACTURE. Rui Huang, The University of Texas at Austin, Dept of Aerospace Engineering and Engineering Mechanics, Austin, TX; J. Liang and Z. Suo, Princeton University, Dept of Mechanical and Aerospace Engineering, Princeton, NJ; H. Yin and J.C. Sturm, Princeton University, Dept of Electrical Engineering, Princeton, NJ; K.D. Hobart, Naval Research Laboratory, Washington, DC.

A compressively strained, epitaxial SiGe film was transferred to a Si wafer coated with a glass layer, and then patterned into islands of various sizes. Upon annealing, the glass flows and the SiGe relaxes. The initial relaxation process includes both lateral expansion and wrinkling. The competition sets a critical island size. For small islands, expansion dominates, resulting in flat and relaxed SiGe islands. For large islands, wrinkling is significant. After a long annealing, the wrinkles either disappear or cause the film to fracture. We model the relaxation process using a nonlinear plate theory for the film and a lubrication theory for the glass and simulate the evolution of the displacements (in both lateral and vertical directions) and stresses in the film. The results are compared to experiments. By comparing the time scales of expansion and wrinkling, an explicit formula is obtained to estimate the critical island size. For large islands, we show that a tensile stress builds up as the wrinkle grows and fracture occurs at a stress level depending on the flaw size in the film. We demonstrate that a cap layer suppresses wrinkling, relaxing a large island crack-free.

9:45 AM D4.4/G1.4
RELAXATION OF SiGe FILMS FOR FABRICATION OF STRAINED Si DEVICES. J.S. Maa, D.J. Tweet, J.J. Lee, and S.T. Hsu, Sharp Labs of America, IC Process Technology Lab, Camas, WA; K. Fujii, T. Naka, T. Ueda, T. Baba, N. Awaya, and K. Sakiyama, Sharp Corporation, IC Group, Process Development Center, Tenri, JAPAN.

In the fabrication of SiGe/Si heterostructure devices, the biaxially-strained Si layers are usually deposited on a virtual substrate formed from a several micron thick compositionally graded SiGe layer[1]. Recently a simpler approach utilizing H or He implantation to enhance relaxation of thinner SiGe films was reported[2]. SiGe with up to 20 at.% Ge was effectively relaxed after implantation with 2-3E16 cm-2 of H and subsequently annealed at a temperature higher than 700C. For SiGe with up to 30 at.% Ge, He implantation was needed. Since the SiGe film thickness was limited to about 100 nm, subsequent growth of a second SiGe layer required further surface cleaning, which was likely to cause an increase in defect density. In this current work, a similar implantation approach is used to enhance the relaxation of SiGe films. However, relaxation beyond the previously reported limit is demonstrated. Experiments are performed on CVD deposited SiGe films with Ge fractions ranging from 20% to 40% and thickness in the range of 100nm to about 500nm. After annealing in the temperature range of 700C to 900C, relaxation of more than 80% is achieved. PMOS and NMOS devices are successfully fabricated and much enhanced hole and electron mobilities are demonstrated. [1] K. Rim, et al., Symp. on VLSI Tech., 98 (2002). [2] H. Trinkaus, et al., Appl. Phys. Lett., 76, 3552 (2000); M. Luysberg, et al., J. Appl. Phys., 92, 4290 (2002).

10:30 AM D4.5/G1.5
SURFACE TOPOLOGY OF IN-SITU STEP-GRADED Si_x Ge_{1-x} BUFFER ON Si SUBSTRATE. Kevin K. Chan, Ray Sicina, Erin C. Jones, Patricia M. Mooney, Inna Babich, IBM Semiconductor Research and Development Center (SRDC), Research Division, Yorktown Heights, NY.

Strained Silicon layers grown on <001> relaxed SiGe buffer layers on Si are promising materials for CMOS devices because the in-plane tensile strain in the layers enhances the electrical carrier mobility in both hole and electron inversion layers. Generally, FET devices made with low germanium concentration relaxed SiGe material show significant electron mobility enhancement, but low increase in hole mobility. As the germanium concentration increases above 30% in the SiGe layer, hole mobility begins to rise. Therefore, high germanium content silicon materials are expected to be important in future microelectric device technologies, and their materials properties require increasing study. One well known problem in high germanium concentration relaxed SiGe heterostructures is poor surface roughness and high etch pit density. In this work, stepwise graded Si_xGe_{1-x} buffers with various germanium concentrations are grown in an 8 inches wafer-size CVD system. Low germanium content films, 15%, are found to have significant surface roughness, 1n RMS value of $\sim$10nm and Z-range of $\sim$90nm, and optical pit density by microscope as high as $\sim$300 pits/mm^2. As the germanium concentration in the buffer layer increases, surface roughness and pit density both increase monotonically. Yet over wider range of Ge content, 15% to 60%, this Si_xGe_{1-x} buffer layer was subjected to in-situ RT annealing, it surface roughness as measured by AFM can be reduced a factor of two and the pit density reduced by a factor of four. The SiGe buffer relaxation, however, as measured by triple axis X-ray diffraction, is unchanged after in-situ annealing.

10:45 AM D4.6/G1.6
FREE STANDING SILICON AS A COMPLIANT SUBSTRATE FOR SiGe. G.M. Cohen, P.M. Mooney and J.O. Chu, IBM T.J. Watson Research Center, Yorktown Heights, NY.

We show that SiGe grown on free-standing silicon is elastically relaxed. The free-standing Si structure consists of a 20 nm-thick, 5 μm-square silicon slab supported by a SiO_2 pedestal at a single contact point at the center of the square (the cross-section resembles a mushroom). A matrix of free-standing structures was made by patterning a bonded silicon-on-insulator (SOI) wafer and undercutting the SiO_2 to form the pedestal. Un-patterned areas of the SOI wafer and the exposed bulk Si substrate were included as reference (control) regions. A UHVCVD $Si_{0.8}Ge_{0.2}$ film was grown epitaxially on both sides of the free-standing silicon and simultaneously on the blanket SOI and bulk substrate control areas. The SiGe layer thickness was about 200 nm, which is 10 times thicker than the free-standing silicon film. Scanning electron microscope (SEM) images show faceting at the edge of the free-standing silicon squares indicating single crystal growth, and thin poly-SiGe is seen on the SiO_2 pedestal. The strain, layer thickness, and composition of the SiGe and the strain in the free-standing Si slab were determined by high-resolution x-ray diffraction (HRXRD) measurements.
The SiGe film grown on both SOI and bulk silicon was found to be fully strained. In contrast, the SiGe layer grown on free-standing silicon is $\sim$90% strain-relaxed, and the free-standing silicon film was measured to be under tensile strain. Since the same lattice mismatch

was found between the SiGe layer and the Si on the free-standing silicon and on the SOI and bulk Si control regions, we conclude that the strain relaxation of the SiGe film on free-standing Si is elastic with the strain accommodated entirely by the free-standing silicon film under tensile strain. This was further confirmed by AFM measurements. The SiGe film on the control regions showed a very smooth SiGe surface with only a few surface steps from misfit dislocations. No surface steps from misfit dislocations were observed on the surface of the SiGe film on free-standing Si. These results show that free-standing silicon serves as an ideal compliant substrate for SiGe.

11:00 AM D4.7/G1.7

HIGH Ge CONTENT (~0.6) RELAXED SiGe LAYERS AND SiGe/Ge STRUCTURES BY COMPLIANT SUBSTRATE APPROACHES. Haizhou Yin, Rebecca L. Peterson, Center for Photonics and Optoelectronic Materials, Princeton University, Princeton, NJ; K.D. Hobart, Naval Research Lab, Washington, DC; Sean R. Shieh, Thomas S. Duffy, Department of Geosciences, Princeton University, Princeton, NJ; J.C. Sturm, Center for Photonics and Optoelectronic Materials, Princeton University, Princeton, NJ.

There has been increasing interest in compliant substrates for integration of heterogeneous epitaxial materials. In our experiments, borophosphorosilicate glass (BPSG) on silicon is used as a compliant substrate to allow the relaxation of a strained silicon-germanium (SiGe) layer initially grown pseudomorphically on Si(100) substrate and then transferred to the BPSG by a bond and etch process[1]. The compressed SiGe can then relax outward by BPSG flow during a 800C anneal to soften the BPSG. This process in principle allows the formation of relaxed SiGe for subsequent devices without requiring any misfit or threading dislocations, unlike conventional relaxed buffer technology. We have previously reported how capping layers and patterning the SiGe into islands can prevent a parasitic buckling during the relaxation, to give layers with only ~1 nm roughness, but the layers were limited in Ge fraction to ~0.3. [2,3] In this talk, we first use the relaxed SiGe layer as a substrate for additional SiGe growth with higher Ge content. After anneal, strain partition between the SiGe layers is observed and consequently, the equivalent Ge percentage of fully relaxed SiGe based on lattice constant is increased. Secondly, strain partition for different thickness of the initial relaxed SiGe layer is investigated and we observe that a thinner initial layer allows more relaxation of the subsequent SiGe layer, so that an relaxed layer of x~0.6 is achieved. To further increase the lattice constant, commensurately strained (compressive) 30 nm of $Si_{0.4}Ge_{0.6}$ is deposited on pre-relaxed $Si_{0.7}Ge_{0.3}$ islands of varying thickness by CVD at 500C. Upon anneal at 800C, we observe by micro-Raman spectroscopy that the $Si_{0.7}Ge_{0.3}$ film gets stretched by the same amount as that which the $Si_{0.4}Ge_{0.6}$ film expands, indicating strain partition between the two layers, consistent with no relaxation by misfit dislocations. By varying the relative thicknesses of the layers, final relaxed layers with equivalent Ge percentages from 0.45 to as high as 0.57 are obtained. These are the highest Ge fractions known to date by compliant substrate. Finally, the strain qualities of epitaxial Ge layers on top of these structures will be described. This work is supported by DARPA. 1. K.D. Hobart, F.J. Kub, M. Fatemi, M.E. Twigg, P.E. Thompson, T.S. Kuan and C.K. Inoki, J. Electron. Mater. 29, 897 (2000) 2. H. Yin, R. Huang, K.D. Hobart, Z. Suo, T.S. Kuan, C.K. Inoki, S.R. Shieh, T.S. Duffy, F.J. Kub and J.C. Sturm, J. Appl. Phys. 91, 9716 (2002) 3. H.Yin, R. Huang, K.D. Hobart, Z. Suo, S.R. Shieh, T. Duffy, J.C. Sturm, "Prevention of Buckling during SiGe Relaxation on Compliant Substrates", MRS Spring Meeting, San Francisco, CA, 2002.

11:15 AM D4.8/G1.8

HELIUM IMPLANTATION AND ANNEALING USED FOR THE FABRICATION OF STRAINED Si ON THIN RELAXED Si-Ge LAYERS. S. Mantl, B. Hollaender, St. Lenk, D.M. Buca, S. Hogg, M. Luysberg, N. Hueging, H. Trinkaus, ISG/IFF Forschungszentrum Juelich GmbH, Juelich, GERMANY; Th. Hackbarth, H.-J. Herzog, DaimlerChrysler Forschungszentrum Ulm, Ulm, GERMANY; R. Loo, IMEC, Leuven, BELGIUM; P.F.P. Fichtner, Dept. de Metalurgia, UFRGS, Porto Alegre, BRAZIL.

Strained silicon has superior electronic properties and will be used in mainstream technology in the near future. The key problem of the implementation of strained silicon in MOSFET or MODFET devices is the fabrication of high quality strain relaxed SiGe layers on Si(100) which serve as virtual substrates for the growth of strained Si. Our approach using He or H implantation and annealing to fabricate very thin, high quality buffer layers has gained considerable interest. We will report results on the strain relaxation of epitaxial SiGe layers on Si(100) wafers with Ge contents varying between 15 and 30at%. The pseudomorphic SiGe layers were grown either by chemical vapor deposition (CVD) or by molecular beam epitaxy (MBE). In addition, results of thin buffer layers on SOI wafers will be presented. The He implantation was performed with energies between 10 keV and 20 keV and doses between 1×10^{16} cm^{-2} and 3×10^{16} cm^{-2} depending on the Ge content and the epilayer thickness. The thickness was varied between 70 and 170 nm. Annealing at a moderate temperature, typically around 850°C, was used to relax the strain. The resulting layers were investigated with numerous analytical techniques, e.g. transmission electron microscopy, AFM, He ion channeling and X-ray diffraction. The relaxed samples are very smooth (rms roughness = 0.3 nm) which allows immediate overgrowth or wafer bonding without polishing. No misorientations or inclinations are observed. Residual strain and threading dislocation density will be discussed as a function of the Ge concentration, the layer thickness, the implantation conditions and the thermal treatment. We will also show that MODFETs produced on such thin buffer layers show higher drive currents and the same RF response as devices processed on thick, step graded SiGe-buffer layers indicating the high layer quality. A model for the implantation induced strain relaxation mechanism will be discussed, which assumes the formation of misfit dislocation segments from dislocation loops punched out by gas filled platelets.

11:30 AM D4.9/G1.9

REAL-TIME OBSERVATION OF STRAIN RELAXATION IN SiGe FILMS ON ULTRA-THIN SOI VIA LOW-ENERGY ELECTRON MICROSCOPY. B. Yang, A.R. Woll[a], M.M. Roberts, D.E. Savage and M.G. Lagally, University of Wisconsin-Madison; [a]Current address: CHESS, Cornell University.

We have used low-energy electron microscopy (LEEM) to study the initial stage of strain relaxation in $Si_{0.96}Ge_{0.04}$ thin films grown on silicon-on-insulator (SOI) and bulk Si substrates. Dislocation glide, cross-slip, and reconnection interactions have been observed in real time. In general, strain relaxation is difficult to see and follow dynamically. Because of its sensitivity to the dislocation-induced strain field, LEEM is able to detect single, buried misfit dislocations. In contrast to TEM, LEEM is nondestructive and can observe dynamic events during growth. On SOI substrates, we observe dislocation glide in SiGe films that are below the critical thickness for dislocation motion on bulk Si. These results provide direct experimental evidence for a decrease in line tension of a buried misfit segment at the Si/SiGe interface caused by the finite Si layer thickness. We will discuss our data in the context of recent models of SiGe film relaxation on SOI [1, 2]. Videos of real-time observations, such as dislocation interactions, cooperative motion, and reversal of glide direction with temperature, will be presented to support the discussion of the models. Our observations have direct implications for the fabrication of strained layer devices on SOI substrates. [1] E.M. Rehder, Ph.D Thesis, University of Wisconsin-Madison, 2002; E.M. Rehder, T.F. Kuech, to be published [2] L.B. Freund, W.D. Nix, Appl. Phys. Lett. 69 173 (1996).
Supported by ONR, DARPA, and NSF.

11:45 AM D4.10/G1.10

HYBRID VALENCE BANDS IN STRAINED LAYER HETEROSTRUCTURES GROWN ON RELAXED SiGe VIRTUAL SUBSTRATES. Minjoo Lee, Eugene A. Fitzgerald, Massachusetts Institute of Technology, Dept of Materials Science and Engineering, Cambridge, MA.

Strained Si, $Si_{1-y}Ge_y$, and Ge layers grown on $Si_{1-x}Ge_x$ virtual substrates (y>x) provide a path for future high performance CMOS devices. Surface strained Si devices exhibit peak hole mobility enhancements of 2 times over bulk Si, while dual channel devices, which combine a strained Si cap with a buried compressive layer, exhibit enhancements of 3 to 8 times. When the strained layer or layers are grown to nanometer-scale dimensions, the wave function of the hole occupies a hybrid valence band where the relaxed substrate, compressive buried layer, and tensile surface layer each make strong contributions to transport. The hybridization of the valence band results from the low effective mass of holes in the out-of-plane direction, and the relative weighting factor of each layer is determined by the vertical effective field and layer thickness. For example, we demonstrate a p-MOSFET consisting of a single 45Å strained Si layer grown on a $Si_{0.3}Ge_{0.7}$ virtual substrate with mobility enhancements comparable to those seen in many dual channel heterostructures. At high E_{eff}, the hole hybridizes the Ge-like effective mass in the relaxed buffer with the valence band splitting in the Si cap, creating a band structure which resembles a compressively strained $Si_{1-x}Ge_x$ alloy. We also demonstrate a high mobility digital alloy consisting of ~1nm alternating layers of strained Si and relaxed SiGe. In this device, the hybrid valence band allows hole mobility enhancement to remain nearly constant with E_{eff}. The high mobility of the digital alloy proves that the hole can intermix the properties of many layers at once- even when the layers are only several monolayers thick- instead of undergoing random alloy scattering. We also apply the concept of hybrid valence bands to demonstrate nearly symmetric mobility p- and n-MOSFETs utilizing strained Si and strained Ge grown on a $Si_{0.5}Ge_{0.5}$ virtual substrate.

SESSION D5: ULTRA-SHALLOW JUNCTION TECHNOLOGY
Chair: Robert J.P. Lander
Wednesday Afternoon, April 23, 2003
Golden Gate C2 (Marriott)

1:30 PM *D5.1
CHALLENGES AND PROSPECTIVES IN USJ TECHNOLOGY FOR ADVANCED CMOS. Hiroshi Kitajima, NEC Electronics Corporation, Advanced Process Development Division, Kanagawa, JAPAN.

The elimination of the transient enhanced diffusion(TED) of dopants is very important to fabricate sub-100nm CMOS devices. The gentle dopant profile caused by TED degrades the transistor performance. For 90-100nm technology node CMOS devices, as-implanted damage decreasing, spike annealing, and the utilization of high-diffusivity dopants can be solutions to suppress TED. Thermal process optimization also can be an solution, since there's an enough margin of the thermal budget. Advanced RTP equipment can realize surface independent annealing with high frequency (>100Hz) feedback, and fabrication of shallow and low-resistivity layer by utilizing the fast ramp-up/ramp-down recipe. Channeling implantation is also effectiveto suppress TED. The annealing at the medium temperature range is effective to decrease the damage especially for heavy ion implantation. For p+ SD-extension profile, Xj of as-implanted B is 15-20nm and final Xj is 25-30nm, which meets the ITRS2001. If Xj of 65nm CMOS devices must be shallower than 20nm as prospected in ITRS2001, we must maintain implanted dopant profile in SD-extension regions. This implies that thermal process, especially temperature, may be restricted after SD-extension implantation. One candidate is very short time annealing, such as flash lamp annealing(FLA) and laser annealing(LA). The annealing time is ms. range, even for FLA, and this means that feedback control by monitoring wafer temperature is not available. As a result, wide process (temperature) margin must be necessary as compared with spike annealing. The other candidate is low temperature annealing, which is more controllable as compared with FLA and LA. But the most critical issue is the junction leakage current. On the assumption of conventional CMOS fabrication process, deep-SD formation will be most critical issue. Elevated SD structure can be an solution, if pre-heating and process temperatures decrease down to 600-650C range.

2:00 PM *D5.2
OVERVIEW OF THE PROSPECTS AND CHALLENGES FOR LAMP ANNEALING IN 45-65nm TECHNOLOGY NODE CMOS. Kyoichi Suguro, Takayuki Ito, Takaharu Itani, and Toshihiko Iinuma, Process and Manufacturing Engineering Center, Toshiba Corporation, Yokohama, JAPAN.

Ultra shallow junction with low resistance is required to improve short channel effects in 45-65nm technology node. Since the gate length for high performance MOSFETs shrinks to 20-30nm, the extension depth (pn junction depth near the gate edge) is required to be shallower than 20nm. However, current RTA tool is confronted with the trade-off problems of thermal diffusion of dopant atoms and electrical activation which is limited by solid solubility. Rapid thermal annealing is also required to reduce dislocation density so that the pn junction leakage specification of high performance MOSFETs can be satisfied. In order to minimize the annealing time at high temperatures, we investigated various lamp annealing methods and newly developed flash lamp annealing (FLA) technology. By optimizing FLA conditions and implantation conditions, p+/n junction depth of 14 nm at 1E18cm-3 and 11nm at 1E19cm-3 were realized with the sheet resistivity of 770ohm/sq. and good junction leakage. As well as p+/n junction, ultra-shallow n+/p junction was successfully formed. Since the impurity diffusion is drastically suppressed, the higher acceleration energy for ion implantation can be applied. The use of higher acceleration energy results in the reduction in the process time of ion implantation, especially in ultra-low energy regime. Shorter length ion implantation leads to higher through-put and reduces process cost of shallow junction formation process. In this paper, we overview prospects and challenges for rapid thermal annealing in 45-65nm technology node.

2:30 PM D5.3
EFFECT OF SIDEWALL NITRIDE SPACER ON ULTRA SHALLOW JUNCTIONS. P. Kohli[a,b], Amitabh Jain[b], H. Bu*b*, S. Chakravarthi[b], C. Machala[b], S.T. Dunham[c] and S.K. Banerjee[a]. [a]Microelectronics Research Center, University of Texas, Austin, TX; [b]Silicon Technology Development, Texas Instruments, Dallas, TX; [c]Electrical Engineering, University of Washington, Seattle, WA.

In the last decade, in order to continue conventional junction scaling, the semiconductor industry has relied heavily on changing the implant energy and dose, and also the activation anneal. Reducing the implant energy and increasing the ramp rate of anneal has greatly reduced transient enhanced diffusion (TED) effects. With TED less pronounced at low implant energies, surface reactions and related processes emerge to dominate the formation of ultra shallow junctions. A nitride spacer with an underlying deposited TEOS oxide that behaves as a convenient etch stop layer, is a popular choice for sidewall spacer in modern CMOS process flow. In this work we have investigated the effect of the nitride spacer process on the boron profile in silicon and the related dose loss of B from the silicon into the oxide. We find that the nitride influences the concentration of hydrogen in the oxide at the final source and drain anneal. The presence of hydrogen enhances the diffusivity of B in the oxide and thereby results in a significant dose loss from the silicon into the oxide. A model calibrated to this data shows 1000 times enhancement of B diffusivity in the oxide due to the nitride. In this work we have shown that by altering the nitride stoichiometry we can affect the oxide so as to reduce the dose loss into the oxide. Thus, we find that optimizing the spacer process results in desirable B diffusion profiles for ultra shallow junctions.

2:45 PM D5.4
IMPACT OF RAPID THERMAL ANNEALING ON B DIFFUSION IN LOW ENERGY IMPLANT WITH PRE-AMORPHIZATION OF DIFFERENT SPECIES. Hong-Jyh Li, Peter Zeitzoff, Larry Larson, International SEMATECH, Austin, TX; Sanjay Banerjee, University of Texas-Austin, Austin, TX.

The formation of an amorphous layer is needed to prevent channeling effect of B in the subsequent implant and hence, shallower as-implanted and annealed profiles could be expected. B diffusion in the pre-amorphization (PAI) Si has been studied extensively by many research groups [1] and the diffusion has been explained by the interaction of B and defects generated by the PAI and B implant processes. In our previous study [2], we theoretically found that B diffusion can be affected by the incorporated species and therefore, B diffusion in the PAI Si should be expected to be different with different PAI species. Experimentally, we have seen different B diffusion behavior in the PAI samples of different species [3]. We found that B clustering plays an important role in the PAI treatment samples [4]. B forms immobile clusters at the surface where most of the PAI species reside and hence, B diffusion can be reduced. However, the immobile B clustering also makes higher sheet resistance, which is a disadvantage of this technique. Increasing annealing temperature can dissolve B clusters but it inevitably makes B diffuse deeper. Therefore, the response of B diffusion in the presence of different PAI species to different annealing conditions need to be explored in order to understand the detail mechanism and make the co-implant technique more useful. In this paper, we studied different B diffusion behavior with respective to different annealing conditions in bulk Si of different PAI species. The species include GeF2, Ge, F, BF2, In and some combinations of those above. References: [1]. Jones, K.S., et. al., Appl. Phys. Lett., 1996. 68(19) p. 2672. [2]. H.-J. Li, P. Kohli, S. Ganguly, T. A. Kirichenko, P. Zeitzoff, K. Torres and S. K. Banerjee, IEDM 2000 Technical Digest pp.515-518. [3] Hong-Jyh Li, Peter Zeitzoff, Robin Tichy, Larry Larson and Sanjay Banerjee, submitted to USJ 2003. [4]. Hong-Jyh Li, Taras A. Kirichenko, Puneet Kohli, Sanjay Banerjee, Eric Graetz, Robin Tichy and Peter Zeitzoff, will be appeared in Nov. issue of IEEE EDL, 2002.

3:30 PM D5.5
Sb SEGREGATION AND ENHANCED DIFFUSION ANALYSIS DURING ULTRA-SHALLOW JUNCTION FORMATION IN SILICON. Dietmar Krueger, Victor Melnik, Peter Zaumseil, Peter Formanek, Rainer Kurps, and Detlef Bolze, IHP, Frankfurt (Oder), GERMANY.

Antimony has been suggested as an alternative to As for shallow source-drain extensions in nMOSFETs. Transient enhanced diffusion (TED) effects due to implantation damage and due to As clustering make it difficult to maintain the steepness of as-implanted As profiles in ultra-shallow junctions and steep wells for CMOS and BiCMOS applications. Here we investigate segregation and diffusion of Sb after low energy implantation (5 and 10 keV) and annealing, both RTP and furnace annealing. We apply X-Ray reflectometry, Transmission electron microscopy (TEM), X-Ray induced photoelectron spectroscopy (XPS), and low energy SIMS depth profiling for the analysis and compare the results with As segregation and diffusion under same conditions. Using primary beam energies below 500 eV in ToF-SIMS we demonstrate strong Sb and As segregation above 1E21 cm^{-3} in an interfacial layer of about 1 - 2 nm. We determine conditions where shallow Sb implantation reveal less dose loss and lower sheet resistance than As implantation. Sb allows to eliminate enhanced diffusion effects typical for As due to injection of Si self-interstitials during electrical deactivation of high As concentrations. As a consequence, the junction depth could be reduced by about 20 nm substituting As implants with Sb. However, for very low implantation energies (below 5 keV) we observe enhanced

Sb segregation with very high dose loss. The observed reduction of enhanced diffusion makes Sb an outstanding candidate for replacing As in S/D extensions for sub - 100 nm CMOS and BiCMOS technologies.

3:45 PM *D5.6
MAXIMUM ACTIVATION AND MINIMUM DIFFUSION BY MILLISECOND ANNEALING - THE KEY TO SHALLOW JUNCTION FORMATION. Peter B. Griffin, Center for Integrated Systems, Stanford University, CA.

The key to ultra shallow junction formation is to maximize dopant activation while minimizing dopant diffusion. In a CMOS process flow, forming shallow PMOS junctions is more difficult than forming shallow NMOS junctions, because the p-type boron diffusion is more rapid than n-type arsenic or antimony diffusion. Fortunately, for the same thermal budget, boron activates more rapidly than arsenic or antimony. It is therefore possible to reduce the diffusion thermal budget for boron by using millisecond annealing while achieving acceptable activation levels. The reason this occurs for boron in particular is related to the atomistic details of its activation mechanism. The activation of boron proceeds by boron cluster dissolution, a process that is mediated by silicon self interstitials. Because the supply of self interstitials is limited by the silicon self diffusion rate, going to higher temperatures enhances the dissolution process while minimizing the diffusion process. This occurs because of the higher activation energy for self compared with dopant diffusion. In the case of the n-type dopants, the activation process is not controlled or limited by the native silicon point defects, so going to higher tempertures contributes only a second order enhancement to the activation level based on increased solubility. We will discuss the role of point defects in the activation and diffusion processes and indicate how millisecond annealing at high temperatures provides the optimum path for achieving ultra shallow, highly active junctions.

4:15 PM D5.7
ATOMISTIC SIMULATIONS OF EFFECT OF COULOMBIC INTERACTIONS ON CARRIER FLUCTUATIONS IN DOPED SILICON. Zudian Qin, Scott T. Dunham, Univ of Washington, Dept of Electrical Engineering, Seattle, WA.

Fluctuations in carrier density associated with discrete dopant atoms have been identified as a critical issue in controlling threshold voltage (V_{th}) in nanoscale MOSFETs. To date, analysis of this phenomenon has largely assumed that the dopants are distributed randomly within the active region. However, interactions between dopants during device fabrication can lead to correlations in dopant locations, modifying the resulting V_{th} variations. One source of these correlations is the Coulombic interactions between ionized dopants, screened by nearby free carriers. In this work, we examine the effect of these interactions on variations in electrical potential within doped regions via kinetic lattice Monte Carlo (KLMC) simulations which simultaneously solve for free carrier distributions and include the effect of associated potential variations on the diffusion of charged dopants and point defects. Our simulation results clearly show that over a broad range of doping concentrations Coulombic repulsion between like dopants leads to ordering, resulting in a more uniform electrical potential distribution (and therefore reduced V_{th} variations) than arises from random doping, with lower temperature annealing giving stronger ordering. In all cases the thermal budget required for ordering is small ($\sqrt{Dt} < 2$ nm) compared to projected junction depths (4-6 nm for the 22 nm technology node based on ITRS).

4:30 PM D5.8
DOPANT DIFFUSION SIMULATION IN THIN-SOI. Hong-Jyh Li, Robin Tichy, Jonathon Ross, Jeff Gelpey, Vortek Industries Ltd, Vancouver, BC, CANADA; Ben Stotts, Heather Galloway, Southwest Texas State University, San Marcos, TX; and Larry Larson, International SEMATECH, Austin, TX.

As the technology of semiconductor devices evolves, the scaling of traditional CMOS devices might approach barriers that make the scaling economically or physically infeasible. New starting materials such as SOI have been attracting attention recently as approaches to overcome these barriers. To further improve the device characteristics using SOI, it is necessary to optimize the top Si layer thickness [1]. As the top Si layer is thinned, the dopants diffusion in the confined Si layer with respect to different thermal treatments needs to be better understood. Recently, dopant diffusion using more advanced annealing technologies like spike and Flash anneals in bulk Si have been studied extensively [2]. The motivation of these annealing techniques is to reduce to junction depth and increase the activation by optimizing the thermal budget. Therefore, it is interesting to study the dopant diffusion and activation in the ultra-thin SOI wafers using the spike/Flash anneals. Boron, BF2 and Arsenic were implanted into bulk Si and SOI wafers with 530 Å Si and 1475A BOX. Samples were annealed using both spike (Impulse) anneal and Flash anneal. Simulations of dopant diffusion and heat conduction analysis are used to resolve apparent differences in dopant profiles that resulted for SOI in contrast with bulk Si samples. References: [1]. H. Park, et. al. p.14.2.1, IEDM 1999; H. Uchida, et. al., p. 33, IEEE SOI Conference, 2001. [2]. D. Camm, et. al., in RTP Conference 2002.

4:45 PM D5.9
MODELING AND SIMULATION OF DOPANT DIFFUSION IN SiGe. Chun-Li Liu, Marius Orlowski, Aaron Thean, Alex Barr, Ted White, Bich-Yen Nguyen, Hernan Rueda; Advanced Products Research and Development Laboratory, Motorola Inc., Tempe, AZ.

Understanding of dopant behavior in SiGe during implantation and activation anneals is critical to development of strained Si technology. We have developed a lattice expansion theory to explain dopant diffusion behavior in SiGe. The theory establishes the relationship between Ge concentration and the changes in dopant activation energies compared to crystalline Si. Quantitative predictions of dopant enhancement and retardation for As, P, and B in SiGe with 20%Ge are in good agreement with experiment. Diffusion equations based on the theory were implemented in the FLOOPS process simulator. Simulated profiles are consistent with experiment under equilibrium conditions without the use of fitting parameters. Implementation of this new tool will help us to speed up the development of novel devices involving strained Si layers.

SESSION D6: POSTER SESSION
STRAINED Si AND SOURCE/DRAIN TECHNOLOGY
Chairs: Bin Yu and Tsu-Jae King
Wednesday Evening, April 23, 2003
8:00 PM
Salon 1-7 (Marriott)

D6.1
A NEW TYPE OF TEXTURE IN THIN FILMS: NiSi, $CoSi_2$ AND α-$FeSi_2$ ON Si(100). Christophe Detavernier, IBM T.J. Watson Research, Yorktown Heights, NY; Ahmet Özcan, Boston University, Dept. of Physics, Boston, MA; J.L. Jordan-Sweet, Christian Lavoie, IBM T.J. Watson Research, Yorktown Heights, NY.

We observed a new type of texturing for a thin film upon reaction with a single crystal substrate. The types of texture reported so far in thin films are either (1) random, (2) in-plane texture, resulting in distinct spots on a pole figure or (3) fiber texture, with the fiber axis normal to the substrate, creating a ring on a pole figure. For NiSi, $CoSi_2$ and α-$FeSi_2$ on Si(100), we observed an off-normal fiber texture with a fiber axis perpendicular to Si(110) facets in the substrate. NiSi, $CoSi_2$ and α-$FeSi_2$ were formed by depositing Ni, Co or Fe on a Si(100) substrate and annealing at 500, 900 and 950°C, respectively. Synchrotron-radiation was used to measure pole figures for the different silicide films. Standard Bragg-Brentano $\theta/2\theta$ scans for the silicide phases did not reveal any clear evidence of a strongly textured film. However, full pole figures consist of complicated line patterns, with very narrow width ($\Delta\chi$ and $\Delta\phi < 1°$). Unlike with standard fiber texture, these lines are not circles centered in the middle of the pole figure. Especially for the orthorhombic NiSi, very complex patterns were observed, at first sight reminding of Kikuchi-type patterns known from electron diffraction. Calculations show that the lines are related to a fiber-type alignment of certain lattice planes parallel to Si(110) planes in the substrate.

D6.2
SHORT-PERIOD $(Si_{14}/Si_{0.75}Ge_{0.25})_{20}$ SUPERLATTICES FOR THE GROWTH OF HIGH-QUALITY $Si_{0.75}Ge-0.25$ ALLOY LAYERS. M.M. Rahman, T. Tambo, and C. Tatsuyama, Department of Electrical and Electronic Engineering, Faculty of Engineering, Toyama University, JAPAN.

Despite of low cost, abundant in nature, process simplicity and prospect of bandgap engineering, SiGe is still away from its full-fledged usages. To realize the proper utilization of SiGe, strain relaxed and smooth alloy layers is required. In the present experiment, we have grown 2500-Å thick $Si_{0.75}Ge_{0.25}$ alloy layers on Si(001) substrate by MBE process using a short-period $(Si_{14}/Si_{0.75}Ge_{0.25})_{20}$ superlattice (SL) as a buffer. In the SL layers, first a layer of 14 monolayers (MLs) of Si (thickness about 20Å) then a thin layer of $Si_{0.75}Ge_{0.25}$ (thickness 5-6Å)were grown. These Si and $Si_{0.75}Ge_{0.25}$ layers were repeated for 20 times. The alloy layers were grown at 500°C and the buffer layers were grown at different temperatures from 300-400°C. Introduction of the buffer layers dramatically changes the surface morphology of the top alloy layers. The alloy layer showed low residual strain (about -0.16%) and smooth surface (rms rougness ~12Å) with 300°C grown SL buffer. Low temperature growth of Si in SL layer introduces point defects and low temperature growth of

$Si_{0.75}Ge_{0.25}$ in SL layer reduces the Ge segregation length, which leads to strained SL layer formation. Strained layers are capable to make barrier for the propagation of threading dislocations and point defect sites can trap the dislocations. This type of buffer is easier to grow and reveals high quality top alloy surface, so this buffer can be considered for the growth of bandgap engineered heterostructures.

D6.3
MATERIAL CHARACTERIZATION FOR STRAINED Si CMOS. Qianghua Xie, Ran Liu, Xiang-Dong Wang, Michael Canonico, Erika Duda, Jim Christiansen, Stefan Zollner, Advanced Products Research and Development Laboratory, DigitalDNA Laboratories, Motorola, Tempe, AZ; Shawn Thomas, Si RF/IF Technologies, DigitalDNA Laboratories, Motorola, Tempe, AZ; Ted White, Alex Barr, Bich-Yen Nguyen, Advanced Products Research and Development Laboratory, DigitalDNA Laboratories, Motorola, Austin, TX.

Strained Si CMOS devices are moving from the research and development phase into manufacturing. The greatest hope for this technology is that compatibility with standard CMOS processing could be achieved with minimum process change, Thus, it could become economically competitive in comparison to pushing the lithography limit. The challenges are residing in the area of appropriately engineering strained Si on a relaxed SiGe buffer to achieve sufficient strain in the Si channel, low threading dislocation density, small surface roughness, good uniformity of strain/stress, and good stability with thermal annealing during subsequent CMOS processing. We will present data on our recent effort in establishing a set of analytical techniques to address the needs in these aspects for strained Si material evaluation using Si/SiGe on bulk Si as an example. Transmission electron microscopy (TEM) is used to reveal the defects formation and propagation in the material. Atomic force microscopy (AFM) reveals the cross hatch patterns, surface roughness, and etch pitch density. Raman scattering equipped with mapping capability can measure the strain in Si as well as the spatial distribution of the strain. A stress of $\sim$1.2 GPa was observed in Si with a standard deviation of 0.2 GPa and the stress non-uniformity can generally be correlated to the cross hatch patterns. TEM and secondary ion mass spectrometry (SIMS) reveals significant intermixing between Si and Ge at the Si channel and SiGe buffer interface upon standard annealing around 900-1000°C used for routine CMOS process.

D6.4
EVALUATION OF STRAIN RELAXATION OF STRAINED-Si LAYERS SELECTIVELY GROWN ON MESA-ISOLATED SiGe-ON-INSULATOR (SGOI) USING RAMAN SPECTROSCOPY AND NANO ELECTRON DIFFRACTION METHODS. Koji Usuda, Tomohisa Mizuno, Tsutomu Tezuka, Naoharu Sugiyama, Yoshihiko Moriyama, Shu Nakaharai, and Shin-ichi Takagi, MIRAI Project, ASET, Kawasaki, JAPAN.

Strained-Si MOSFETs are one of the most promising device structures for high speed CMOS. We have developed the strained-Si MOSFETs on the thin relaxed SiGe-On-Insulator (SGOI) structures[1] for combining strained-Si with SOI structures. Since fabrication of the strained-Si MOS with small size is indispensable in the strained-Si MOS LSIs, the investigation of strain relaxation during integration processes is an important issue. Here, we have investigated the relaxation of strained-Si layers which were selectively grown on the mesa-isolated SGOI layers thinking of the device isolation process of mesa etching of SGOI substrates and successive epitaxial growth of strained-Si. The mesa isolation process was carried out using Chemical-Dry-Etching. The Rapid-Thermal-Annealing (RTA) procedure was performed in N2 atmosphere. As a result, it was confirmed using Raman spectroscopy with resolution of $>$ 1 micrometer square that the strained-Si layers with the size of 5 micrometer square had resistance to relaxation against the RTA processes. Meanwhile, to overcome a limit of lateral resolution in the Raman measurement, the nano-Electron Diffraction (ED) with resolution of 10nm was employed and the distribution of lattice constant within the strained-Si and SiGe layers was evaluated. It was clearly confirmed that the relaxed-SiGe layer induced tensile strain into the strained-Si layer and the strain was almost maintained to the edge part of the isolated strained-Si layer. In conclusion, it was found that the relaxation of strained-Si layers selectively grown on the mesa-isolated SGOI layer was negligible down to 5 micrometer in size, and the nano-ED was effective to evaluate very thin strained-Si layers isolated into sub-micrometer size. This work was partly supported by NEDO. [1] T. Mizuno et al., EDL-21, 230 (2000).

D6.5
X-RAY SCATTERING AS A PROBE OF INTERDIFFUSION AT Si/SiGe INTERFACES. Daniel B. Aubertine, Nevran Ozguven, Paul C. McIntyre, Stanford Univ, Dept of Materials Science and Engineering, Stanford, CA.

We present a thorough analysis of X-ray diffraction as a probe of the interdiffusivity at Si/SiGe interfaces. The majority of Si/SiGe interdiffusivity measurements involve fitting diffusion simulations to depth dependent measurements of Ge concentration. This strategy is limited both by the depth resolution of the experimental techniques employed and by the need to assume a functional form for the interdiffusivitys concentration and strain dependence when performing the diffusion simulations. In principle, X-ray diffraction from Si/SiGe superlattices largely overcomes these limitations by providing sensitivity to sub-nanometer diffusion lengths and a direct measurement of the interdiffusivity that is independent of any preformed assumptions.
To study the use of X-ray diffraction as a probe of interdiffusion, we incorporate both dynamical X-ray diffraction simulations and numerical solutions to Ficks second law into a package for performing virtual interdiffusion experiments. This approach allows the characterization of the techniques robustness with respect to non-idealities in the annealing conditions, imperfect knowledge of the rate of strain relaxation, and uncertainties in the structural characterization of samples. We further show that although direct extraction of the Si-Ge interdiffusivity from superlattice satellite peak intensity attenuation data is only rigorously valid for superlattices with sinusoidal concentration profiles, in practice it serves equally well for square wave concentration profiles that are common in as-grown samples. Finally, we illustrate the difficulty of extracting a single, meaningful value for interdiffusivity in a system where the interdiffusivity varies considerably as a function of Ge concentration and time.

D6.6
DIRECT MEASUREMENT OF THE CONCENTRATION DEPENDENT ACTIVATION ETHALPY FOR INTERDIFFUSION AT Si/SiGe INTERFACES. Daniel B. Aubertine, Nevran Ozguven, Paul C. McIntyre, Stanford Univ, Dept of Materials Science and Engineering, Stanford, CA.

The activation enthalpy for interdiffusion at Si/SiGe interfaces is believed to be both concentration and strain dependent. An accurate characterization of this quantity as a function of Ge concentration is important both for refining process simulations involving the thermal stability of Si/SiGe interfaces and for understanding the physics of the interdiffusion process. To date, reported measurements of this activation enthalpy are based on unconfirmed assumptions about the functional form of the Si/SiGe interdiffusivity with respect to Ge concentration and film strain. We demonstrate the use x-ray diffraction from Si/SiGe superlattices possessing a specially designed concentration profile to directly probe the activation enthalpy as a function of Ge concentration.
Measuring interdiffusivity via x-ray diffraction involves monitoring the decay of x-ray (000) or (004) superlattice satellites as a function of annealing time. In a model system, where the interdiffusivity is concentration independent, the logarithm of the superlattice satellite decay rate is linearly proportional to the interdiffusivity. Typically, a straightforward analysis of this type is not possible with SiGe because the interdiffusivity is a strong function of Ge concentration. We show that by using $Si_{1-x}Ge_x/Si_{1-y}Ge_y$ superlattices with an as-grown composition amplitude of less than 2% Ge we are able to extract the interdiffusivity at the film's mean composition. The activation enthalpy is determined by performing these experiments by inert gas annealing at several different temperatures.

D6.7
INVESTIGATING THE CHANNEL LENGTH NON-UNIFORMITY AND VARIOUS IMPLANT STRUCTURES OF SEMICONDUCTOR DEVICES USING AFM/SCM. Kuo-Jen Chao, Hoainam Ho, & Ian Ward Charles Evans & Associates, Sunnyvale, CA.

Atomic force microscopy and scanning capacitance microscopy (AFM/SCM) have been applied to study various implant structures of semiconductor devices. In this work, two types of semiconductor devices, Si based and GaAs based, were studied. Many researchers have used AFM/SCM to study cross-sectional semiconductor devices to delineate the dopant profiles in the source and drain regions and further determine the channel length. While the width of the gate has been shrinking to below 0.13um, the length of the gate has not. Therefore, channel length determined from a cross-sectional study may not be representative. AFM/SCM has been applied to study a Si device directly from the top, and the channel length of this device was found to be non-uniform in the SCM image. A similar direct top-down AFM/SCM study has also been applied to a GaAs device. In this case, the lateral diffusion length of dopants after a thermal annealing process is evaluated. A GaAs substrate is masked and patterned by a layer of Si3N4, then Zn dopants are thermally diffused through a line-opening in the nitride layer into the substrate. By overlaying the AFM image on top of the SCM image, the lateral diffusion length of the Zn dopants is found to be about 2.2 um from the edges of the exposed GaAs region. Another important application of AFM/SCM is

in device failure analysis by directly comparing a failed device with a properly functioning one in order to identify the cause of failure. AFM/SCM has been applied to study the same N-well structures in two devices, one good and the other failed, and the depth of the N-well for the failed device is found to be about 0.4um shorter than in the good device.

D6.8
PHYSICS-BASED SIMULATION OF PROCESSING OPTIONS FOR PRE-AMORPHIZED ULTRASHALLOW JUNCTIONS.
N.E.B. Cowern and B. Colombeau, Advanced Technology Institute, Surrey Univ, Guildford, UNITED KINGDOM; R. Duffy, V. Venezia, C. Dachs, Philips Research, Leuven, BELGIUM; R. Lindsay, IMEC, Leuven, BELGIUM; F. Cristiano, LAAS-CNRS, Toulouse, FRANCE; A. Claverie, CEMES-CNRS, Toulouse, FRANCE.

The last three years have seen rapid advances in understanding of the energetics, Ostwald ripening and structural transformations between various types of extended defects (clusters, {113} defects and dislocation loops) in ion-implanted silicon. This opens the possibility of simulating end-of-range (EOR) defects, transient enhanced diffusion (TED) and dopant deactivation in preamorphized ion-implanted ultrashallow junctions. As a result, parameters such as junction depth, junction steepness and sheet resistance will be predictable over a wide range of implant and thermal annealing conditions. Given the difficulty in reaching projected targets for these parameters in future CMOS generations, such a capability will be of enormous value.
In this work we use a physically based two-step approach to model defect evolution, TED and deactivation in ultrashallow preamorphized and B-implanted junctions. First, a quasi-zero-dimensional multi-equation solver is used to calculate EOR defect evolution and interstitial transport between the defect layer and the surface. The evolution accounts for the detailed energetics of clusters, {113} defects and dislocation loops, including a simplified model for the transformation between {113} defects and loops. Calculations are performed across a wide range of thermal ramp rates from conventional RTP to arc annealing, and results are compared with quantitative TEM measurements on EOR defects in correspondingly processed samples. From these results we calculate the depth and time dependence of the interstitial supersaturation, $S_I(x,t)$, during annealing. Second, the established behaviour of $S_I(x,t)$ is used as input to numerical simulations of diffusion including substitutional and interstitial B as separate species. The simulations account for some counter-intuitive, and previously unexplained, trends in experimentally observed junction profiles.

D6.9
SHALLOW JUNCTION FORMATION BY ARSENIC OUTDIFFUSION FROM IMPLANTED OXIDE.
Omer Dokumaci, Paul Ronsheim, Suri Hegde, IBM SRDC, Hopewell Junction, NY.

As the devices are scaled down, shallower junctions are needed to prevent short channel effects in sub-0.1 um devices. We investigated arsenic outdiffusion from thin implanted oxide to form ultra-shallow junctions. A layer of oxide was grown on silicon with an RTO process. The oxide thicknesses were 15A, 35A and 75A. 15A oxide thickness served as a control. After preamorphization with Ge, arsenic was implanted with energies between 1 and 5 keV at a dose of 1.5e15 cm^{-2}. The samples were then annealed in an RTA system between 950C and 1050C for various times. Implanted and annealed arsenic profiles were obtained by SIMS. For the 1 keV implant, more than half of the implanted arsenic was found to be in the oxide for the 35A oxide sample. When this sample was annealed, nearly all of the arsenic came out of the oxide into silicon. This is the first time such an enhanced diffusion of arsenic through the oxide is observed. We believe that the enhanced diffusion is caused by the implant damage created in the oxide. For the 1 keV implant into 75A oxide, only a small amount of arsenic actually diffused out into silicon. In this case, arsenic peak was further away from the oxide/silicon interface so that even the enhanced diffusivity in the oxide was not enough to diffuse out the arsenic into silicon. All the results will be discussed in light of simulations which take into account the enhanced diffusivity in the oxide.

D6.10
VACANCY-ARSENIC COMPLEXES IN HIGHLY n-TYPE Si: IDENTIFICATION, FORMATION MECHANISMS, AND ROLE IN THE DEACTIVATION OF DOPING.
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The detailed atomic structure of vacancy-impurity complexes present in highly n-type Si can be experimentally determined by combining positron lifetime and electron momentum distribution measurements [1]. The monovacancy surrounded by three As atoms is the dominant vacancy-impurity complex in Czochralski Si doped with As up to $10^{20}cm^{-3}$ [1]. By studying the annealing of $V-As$ pairs formed by electron irradiation, we can show that the of $V-As_3$ complexes are formed as a result of the subsequent migrations of $V-As$ and $V-As_2$ [2]. The $V-As_3$ complexes are dominant defects also in highly As-doped MBE grown Si, where they exist at concentrations relevant to the electrical deactivation of doping. Larger complexes, tentatively identified as V_2-As_5, are also present at high concentrations. The $V-As_3$ and V_2-As_5 defects are removed by annealings at 800 and 900 C, respectively. However, they are likely to reconstruct during the cooling down by migrations of $V-As$ and $V-As_2$, as demonstrated in electron irradiated material [2]. The rapid thermal annealing is shown to lead to smallest concentrations of $V-As_3$ and V_2-As_5, most likely due to the limited time available for the migration processes. [1] K. Saarinen et al., Phys. Rev. Lett. 82, 1883 (1999). [2] V. Ranki et al., Phys. Rev. Lett. 88, 105506 (2002).

D6.11
EVIDENCE FOR A NEW DEFECT IN HIGHLY n-TYPE Si FROM ATOMIC-RESOLUTION CHANNELING EXPERIMENTS ON INDIVIDUAL DOPANT ATOMS.
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Channeling experiments performed in a scanning transmission electron microscope with single dopant atom sensitivity and resolution show that neither a vacancy-centered cluster nor a donor pair can be the primary defect responsible for the saturation of the carrier density as a function of dopant concentration in n-type Si. We propose a new defect, DP(N)V-I, which consists of a donor pair and a Si vacancy-interstitial pair. This defect is consistent with our measurements, has enough free volume to reconcile recent positron-annihilation measurements, and explains the observed behavior of the carrier density versus dopant concentration.

D6.12
IMPURITY AND SELF-DIFFUSION IN EXTRINSIC PHOSPHORUS DOPED SILICON ISOTOPICALLY CONTROLLED HETEROSTRUCTURES.
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Studies of dopant and self-diffusion in isotopically controlled silicon heterostructures involving extrinsic boron and arsenic doping have yielded new, quantitative information on the contributions of native point defects to self-diffusion in silicon.[1,2] As a result of the Fermi level shift under extrinsic conditions, these studies have yielded information on the roles of singly positively charged self-interstitials (I^+) and negatively charged vacancies (V^-) in diffusion. We present experimental results of dopant and self-diffusion in an isotopically controlled silicon heterostructure extrinsically doped with phosphorus. As a consequence of extrinsic n-type doping, the concentration of singly negatively charged native point defects is enhanced. However, indiffusion of phosphorus is known to cause a supersaturation of self-interstitials and thereby an undersaturation of vacancies. This suppresses the impact of vacancies in the simultaneous diffusion of phosphorus and self-atoms. As a consequence the charge states of self-interstitials in the diffusion process can be determined. Multilayers of isotopically controlled ^{28}Si and natural silicon enable simultaneous analysis of ^{30}Si self-diffusion into the ^{28}Si enriched layers and dopant diffusion throughout the multilayer structure. An amorphous 260 nm thick Si cap layer was deposited on top of the Si isotope heterostructure. Phosphorus ions were implanted to a depth such that all the radiation damage resided inside the amorphous cap layer. These samples were annealed for different times and temperatures. After diffusion the dopant- and self-atom diffusion profiles were recorded by means of secondary ions mass spectrometry. Modeling of the diffusion profiles provides information about the point defects mediating phosphorus diffusion and about their diffusion properties for various extrinsic n-type conditions.
[1]Silvestri H.H., et al., (2002) Mat. Res. Soc. Symp. Proc. 719 F13.10.1-F13.10.6
[2]Sharp I.D., et al., (2002) Mat. Res. Soc. Symp. Proc. 719 F13.11.1-F13.11.6

D6.13
DIFFUSION AND ELECTRICAL ACTIVATION OF INDIUM IN SILICON.
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ITC-irst, Povo (Trento), ITALY; S. Solmi CNR-IMM Sezione Bologna, ITALY; P. Pichler, Fraunhofer-Institute fuer Integrierte Schaltungen, Bauelementetechnologie, Erlangen, GERMANY.

In this work we investigate the diffusion and the electrical activation of In atoms implanted in silicon with different energies, in the range 40-360 keV, with doses between 5×10^{12} In/cm^2 and 5×10^{13} cm^2, after rapid thermal processing. Our investigation shows a clear dependence of In out-diffusion and electrical activation on the implant depth, being the electrically active fraction higher with increasing the implant energy for a fixed dose. We propose that the data can be explained considering the balance between the local In concentration and the C background. The occurrence of coupling between the C present in the substrate and the implanted In, depending on the C/In ratio, may in fact give rise to a significant formation of C-In complexes. Such complexes play a role in the enhanced electrical activation due to the shallower level they introduce into the Si band gap (E_v+0.111 eV), with respect to the rather deep level (E_v+0.156 eV) of In alone. The interaction of In atoms with the C background inside the silicon substrate has been therefore identified as the most likely origin of this behaviour. In and C co-implantation has also been studied within this work, in order to further investigate the key role of C in the increase of the electrical activation. A large increase of the electrical activation has been detected in the co-implanted samples, up to a factor of about 8 after annealing at moderate temperatures. However, C precipitation occurs at 1100°C, with dramatic effects on the carrier concentration that falls down by orders of magnitude. This gives a limitation to the maximum thermal budget to be used for In activation in C co-implanted material.

D6.14
THE EFFECTS OF FLUORINE ON BORON MOTION IN SILICON DURING ION IMPLANTATION AND POST-IMPLANTATION ANNEALING. L.S. Robertson, Texas Instruments Inc, Dallas, TX; J.M. Jacques, K.A. Gable, K.S. Jones, Univ of Florida, Dept of Materials Science and Engineering, Gainesville, FL; Amitabh Jain, Texas Instruments Inc, Dallas, TX.

Fluorine co-implantation with boron in silicon has garnered interest due to its demonstrated ability to reduce the transient enhanced diffusion of boron during post-implantation annealing. In addition to significantly reducing the diffusion of boron in silicon during post-implantation rapid thermal annealing (RTA), the presence of fluorine is observed to change the behavior of boron both in the as-implanted state and during low temperature annealing for solid phase epitaxial regrowth. The diffusion behavior of boron in each case is characterized by secondary ion mass spectrometry (SIMS). The presence of fluorine is observed to induce room temperature diffusion of boron during ion implantation. Correlation of the effects of fluorine and hydrogen in silicon are investigated by direct comparison of co-implantation of each species into pre-amorphized silicon with low energy boron implants. It is shown that the demonstrated fluorine effects are each consistent with the hypothesis that fluorine interacts with silicon lattice damage by passivating unbonded silicon orbitals both in crystalline and amorphous silicon. The evolution of the amorphous layer thickness of samples after implantation and subsequent annealing is monitored by variable angle spectroscopic ellipsometry (VASE) and cross-sectional transmission electron microscopy (XTEM). Application of the findings to the challenges encountered in the formation of ultra-shallow junctions, particularly reduction of junction depth without degradation of junction abruptness, will also be discussed.

D6.15
MODELING THE EFFECT OF FLUORINE ON BORON AND PHOSPHORUS. Milan Diebel, Univ of Washington, Dept of Physics, Seattle, WA; Srinivasan Chakravarthi, Charkes F. Machala, Shashank Ekbote, Amitabh Jain, Silicon Technology Development, Texas Instruments, Dallas, TX; Scott T. Dunham, Univ of Washington, Dept of Electrical Engineering, Seattle, WA.

Implanted fluorine (F) has been observed to behave unusually in silicon, manifesting an apparent uphill diffusion. Experiments also show that F can enhance as well as retard boron (B) and phoshorus (P) diffusion depending on the implant conditions. Based on previous presented ab-initio calculations (M. Diebel and S.T. Dunham, Mat. Res. Soc. Symp. Proc. 717), which explain the anomalous fluorine diffusion behavior, a comprehensive model is developed which explains the different effects of fluorine on B and P under sub-amorphizing and amorphizing conditions. Ab-initio calculations find no significant binding energies between B-F and P-F. Instead, the different effects of fluorine on dopants are primarily due to fluorine point-defect interactions. The formation and dissolution of fluorine vacancy clusters alters the local point-defect concentrations and therefore can enhance or retard B and P depending on the implant condition. A comprehensive continuum model was implemented and compared to experimental data. Fluorine enhances B and P diffusion under sub-amorphizing conditions and retards in amorphized environments. The model is also capable of predicting the fluorine effect on B and P in case where the dopant concentration is divided by amorphous-crystalline interface in a sub-amorphous and amorphous portion.

D6.16
DIFFUSION OF BORON AND SILICON IN GERMANIUM AND $Si_{1-x}Ge_x$ (x>50%)ALLOYS. Suresh Uppal, Arthur F.W. Willoughby, Materials Research Group, University of Southampton, Janet M. Bonar, Department of Electronics and Computer Science, University of Southampton, Southampton, UNITED KINGDOM.

Channel engineering in combination with ultra shallow junctions using ion implantation has shown potential for improvement in performance of existing MOSFET devices. On material front, strained Si, $Si_{1-y}Ge_y$, and Ge layers grown on $Si_{1-x}Ge_x$ (y>x) virtual substrates are prospective candidates especially for p-type MOSFET [1]. Utilizing B implanted Germanium intermixed with Si to form elevated source/drain p-MOSFET has also been suggested [2]. In this work, boron diffusion has been studied in germanium and $Si_{1-x}Ge_x$ (x>50%) alloys using ion implantation and high resolution secondary ion mass spectroscopy(SIMS). Effect of variation in implantation dose and energy has been investigated. A significantly low diffusivity of boron in Ge contrary to previously reported values has been observed. Si diffusion studies have also been carried out in Ge utilizing ion implantation, furnace annealing and SIMS. The results are discussed from the viewpoint of mechanism responsible for B and Si diffusion in Ge, $Si_{1-x}Ge_x$ alloys. Boron diffusion studies are being carried out using epitaxial growth in order to avoid implantation damage effects.
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[2] P. Ranade, H. Takeuchi, V. Subramanian, Tsu-Jae King, *IEEE Electron Device Letters*, **23**, 218, (2002).

D6.17
MULTISCALE COMPUTATIONS OF B DIFFUSION IN SiGe. Liguo Wang, Cheruvu S. Murthy†, and Paulette Clancy, School of Chemical and Biomolecular Engineering, Cornell University, Ithaca, NY; †IBM Semiconductor Res. & Dev. Center (SRDC), Microelectronics Division, Hopewell Jct., NY.

Device scaling has been driving the integrated circuit (IC) microelectronics revolution for around three decades. One of the critical elements in device scaling is the junction depth (and, now, the extension junction depth), pushed to 25 nm in the 2001 International Technology Roadmap for Semiconductors (ITRS). The scaling is not straightforward since the anomalous boron diffusion in the post-implantation heating processes poses severe challenges to the formation of ultra-shallow junctions. To reduce the diffusion of boron, other species, e.g. Ge, N, are incorporated into the Si substrate, dramatically reducing the diffusivity of boron (e.g. a factor of 6 in $Si_{0.80}Ge_{0.20}$ relative to Si). Experimental evidence tends to be indirect, hence the atomic-scale migration mechanisms and paths of the boron diffusion in SiGe alloys are not understood yet. The energetics of boron diffusion in SiGe can be investigated quantitatively with ab initio calculations. Using the linear, basis-independent Density Functional Theory LDA code, DFT++, developed by T. Arias at Cornell University, we are investigating the mechanism that retards boron diffusion in SiGe. Initial results show that stress compensation plays a minor role in the boron diffusion in SiGe, contrary to some expectations. Placing a neutral B atom and a Ge atom in close proximity does not lead to an energetically favorable configuration. The energetics of defects involving B and Ge atoms suggest that substitutional boron atoms find it difficult to be "kicked out" by an interstitial Ge atom or to diffuse past a nearby Ge. Larger-scale empirical Stillinger-Weber models show that the preferred interstitial positions and trapping mechanisms of B are different in Si and SiGe. In Si, an initially interstitial boron quickly displaces a lattice Si atom and occupies a substitutional site for "long" periods. In contrast, in SiGe an initially interstitial boron in $Si_{0.90}Ge_{0.10}$ becomes "trapped" for "long" periods in an interstitial position between two substitutional Ge atoms.

D6.18
BORON SEGREGATION AND OUT-DIFFUSION IN SINGLE-CRYSTAL $Si_{1-y}C_y$. Eric Stewart, James Sturm.

Boron and carbon diffusion in $Si_{1-x-y}Ge_xC_y$ and $Si_{1-y}C_y$ alloys is important to understand for integrating these materials into modern MOSFET and HBT devices. Previously, it has been shown that boron segregates into single-crystal $Si_{1-x}Ge_x$ [1] and even more strongly into polycrystalline $Si_{1-x-y}Ge_xC_y$ [2]. In this work, we report that boron also segregates into single-crystal $Si_{1-y}C_y$. We also find that, when most of the carbon is removed from the thin $Si_{1-y}C_y$ layer by

oxidation-enhanced out-diffusion, boron that had previously segregated to the layer can diffuse away as well. Models to explain these effects will be presented, as well as the effect of boron on carbon diffusion. All structures were grown by RTCVD at 625°C and 750°C, using $SiCl_2H_2$ and Si_2H_6 as silicon sources and $SiCH_6$ and B_2H_6 as carbon and boron sources, respectively. The test structure used for this study consisted of an undoped, 20 nm $Si_{0.996}C_{0.004}$ layer sandwiched between thicker boron-doped ([B] = $2x10^{19}$ cm^{-3}) Si layers, on an n-type substrate. The $Si_{0.996}C_{0.004}$ layer was positioned 50 nm below the surface of the sample. A two-step anneal was performed: the first step was an 850°C, 2 hour N_2 anneal to allow boron to move into the $Si_{0.996}C_{0.004}$ layer. SIMS profiles taken after this anneal show that boron segregates into the $Si_{0.996}C_{0.004}$, with a segregation coefficient of 1.8. The second step was an 850°C, 2 hour oxidation. A previous study has shown that, for a similar structure and anneal time, oxidation-enhanced diffusion allows all of the carbon to diffuse out of the $Si_{1-y}C_y$ layer [3]. SIMS profiles of our samples show the same effect - most of the carbon is removed from the $Si_{1-y}C_y$ layer. As this happens, most of the boron that had previously segregated to the layer diffuses away as well. Models to explain the initial boron segregation include (i) B-C or B-SiC defect complex formation, or (ii) point defect gradients caused by the local interstitial undersaturation in the $Si_{1-y}C_y$. The ability of both carbon and boron to out-diffuse during the oxidation indicates that immobile B-C defects are not responsible for the boron segregation, favoring the point defect gradient model. This work was supported by DARPA and ARO. 1. S.M. Hu, D.C. Ahlgren, P.A. Ronsheim, and J.O. Chu, Physical Review Letters, vol. 67 (11), p. 1450-1453 (1991). 2. E.J. Stewart, M.S. Carroll, and J.C. Sturm, MRS Symposium Proceedings, vol. 669, paper J6.9 (2001). 3. M.S. Carroll, J.C. Sturm, E. Napolitani, D. De Salvador, M. Berti, J. Stangl, G. Bauer, and D.J. Tweet, Physical Review B, vol. 64, 073308 (2001).

D6.19

PROCESS OPTIMIZATION FOR MULTIPLE-PULSE LASER ANNEALING OF BORON IMPLANTED SILICON WITH GERMANIUM PRE-AMORPHIZATION. Debora Poon, Byung Jin Cho, Yong Feng Lu, Silicon Nano Device Laboratory and Laser Micro-Processing Laboratory, National University of Singapore, SINGAPORE; Mousumi Bhat, Alex See, Technology Development Department, Chartered Semiconductor Manufacturing, SINGAPORE.

One of the major advantages of multiple-pulse Laser Thermal Annealing (LTA) with moderate-energy fluence is that good dopant activation can be achieved without further increases in junction depth by successive pulses. This paper presents the ability to predict the number of laser pulses required to anneal an initially amorphous layer to obtain a defect-free single crystal for different preamorphized layer depths. In addition, a method to separate the reason behind sheet resistance reduction upon multiple laser pulses, into either increased dopant activation, defect annealing or both without the need for further High Resolution Transmission Electron Microscopy (HR-TEM) analysis is also proposed. Wafers are implanted with germanium to form amorphous layers of varying depths, close to the surface. This is followed by a 0.5 keV boron implantation. The samples are then LTA processed with varying number of pulses and energies ranging from below to above the energy density required to fully melt the Preamorphization Implantion (PAI) layer. It is demonstrated that when the laser fluence is adjusted to a value that can melt the PAI layer but not the underlying silicon substrate, PAI layer depths control the junction depths. Hence, it is desirable to operate LTA in this regime since this allows for a tighter process control as opposed to when the junction depth is controlled solely by the laser fluence. HR-TEM micrographs show that with single-pulse LTA at such a energy fluence, although damage in thin amorphous layers can be repaired, the defects in thick amorphous layers are not annealed out effectively, giving rise to micro-twins and polycrystalline formation. Our study allows for the prediction, from four-point probe measurements, the maximum allowable PAI depth for a given number of pulses in order to fully remove the damage caused by the PAI.

D6.20

Abstract Withdrawn.

D6.21

FORMATION OF NiSi-SILICIDED P^+N SHALLOW JUNCTIONS USING IMPLANT THROUGH SILICIDE AND LOW TEMPERATURE FURNACE ANNEALING. Chao-Chun Wang, Chiao-Ju Lin, and Mao-Chieh Chen, Department of Electronics Engineering, National Chiao-Tung University.

NiSi-silicided p^+n shallow junctions are fabricated using $BF_2{}^+$ implantation into/through thin NiSi silicide layer (ITS technology) followed by low temperature furnace annealing (from 550 to 800°C). The NiSi film agglomerates following a thermal annealing at 600°C, and may result in the formation of discontinuous islands at a higher temperature. The incorporation of fluorine atoms in the NiSi film can retard the formation of film agglomeration and thus improving the film's thermal stability. The forward ideality factor of about 1.02 and the reverse current density of about $1nA/cm^2$ can be attained for the NiSi(310Å)/p^+n junctions fabricated by $BF_2{}^+$ implantation at 35 keV to a dose of 5×10^{15} cm^{-2} followed by a 650°C thermal annealing; the junction formed is about 60nm measured from the NiSi/Si interface. Activation energy measurement indicates that the reverse bias junction currents are dominated by the diffusion current, indicating that most of the implanted damages can be recovered after annealing at a temperature as low as 650°C.

D6.22

Abstract Withdrawn.

D6.23

THE IMPROVED THERMAL STABILITY OF NICKEL SILICIDE FILMS BY NICKEL AND TANTALUM ALLOY. Dongwon Lee, Kihoon Do, Dong Chan Suh, Dae-Hong Ko, Yonsei Univ., Dept. of Ceramic Engineering, Seoul, KOREA; Ja-Hum Ku, Siyoung Choi, Process Development Team, Semiconductor R&D Division, Samsung Electronics Ltd., KOREA; Cheol-Woong Yang, Sungkyunkwan Univ., School of Metallurgical and Materials Engineering, Suwon, KOREA.

The formation and the thermal stability of Nickel silicide film with pure Ni and Ni-Ta alloy has been investigated for the application to the ULSI device. A comparative study of the silicide formation with Ni film and Ni-Ta alloy films deposited on the single crystal Si(100) substrate has been performed by using Rapid Thermal Process (RTP). After silicidation process with different RTP temperature, we measured the sheet resistance of Ni/Si and $Ni_{1-x}Ta_x$/Si system with different composition of Ta. With addition of Ta system, the sheet resistance became more stable than pure Ni silicide in high RTP temperature range. Moreover, we analyzed the microstructure of the interface by using TEM and phase transition with XRD. Corresponding to the results of sheet resistance, Ni-Ta/Si system shows an improved thermal stability and microstructure than Ni/Si system in higher RTP temperature. These results show the improvement in the thermal and morphological stability of nickel silicide in case of Ni-Ta/Si systems. After first annealing by RTP at 500°C, post anneal were performed at the different temperature, considering post thermal budget after salicide process. In case of Ni-Ta/Si system, the silicide layer has a stable sheet resistance of about 5Ω/sq. and maintained for 120min long time annealing at 600°C. But, the sheet resistance increase with increasing of annealing time due to formation of $NiSi_2$ in Ni/Si system. After annealing of $Ni_{0.95}Ta_{0.05}/SiO_2$/Si and $Ni_{0.95}Ta_{0.05}/Si_3N_4$/Si systems at 500°C, wet etching at 85°C was done by H_2SO_4+H_2O_2 solution. There is no formation of silicide and the unreacted metal alloy films on dielectric materials after annealing. Through SEM image, there is no residue left on the dielectric materials. Therefore silicide is expected to be selectively grown on poly-Si lines and bulk Si.

SESSION D7: LASER ANNEALING AND SILICIDE PROCESSES

Chair: Bin Yu
Thursday Morning, April 24, 2003
Golden Gate C2 (Marriott)

8:30 AM *D7.1

ULTRA-SHALLOW JUNCTION FORMATION BY EXCIMER LASER ANNEALING OF ULTRA-LOW ENERGY B IMPLANTED IN Si. G. Fortunato and L. Mariucci, CNR-IFN, Rome, ITALY; V. Privitera, S. Whelan, A. La Magna, G. Mannino, M. Italia and C. Bongiorno, CNR-IMM, Catania, ITALY.

Formation of ultra-shallow junctions by excimer laser annealing (ELA) of ultra-low energy (1keV -200 eV) B implanted in Si has been investigated. High resolution TEM has been used to assess the as-implanted damage and the crystal recovery following ELA. The electrical activation and redistribution of B in Si during ELA has been studied as a function of the laser energy density (melt depth), the implant dose and the number of laser pulses (melt duration). Under appropriate ELA conditions, ultra-shallow profiles, extending to a depth as low as 35 nm with an abrupt profile (2.5 nm/dec), have been achieved. The activated and retained dose has been evaluated with spreading resistance profiling and SIMS. A significant amount of the implanted dopant was lost from the sample following ELA. However, the dopant that was retained in crystal material was fully activated following rapid re-solidification. The electrical activation was increased for high laser energy density annealing, when the dopant was redistributed over a deeper range. We developed a theoretical model, that considers the dopant redistribution during melting and regrowth, showing that the fraction of the implanted dopant not activated during ELA was lost from the sample through out diffusion. The lateral distribution of the implanted B following

laser annealing has been studied with 2-D measurements, using selective etching and cross-section TEM on samples where the implanted dopant was confined within an oxide mask. The results show that there is substantial lateral diffusion of B under the oxide mask when melting occurs in this region while, if melting under the oxide mask is prevented, the implanted B close to the oxide mask edge was not activated by ELA. The results have been explained by numerical heat-flow calculations and it is concluded that lateral diffusion can be controlled by the oxide mask thickness.

9:00 AM *D7.2
LASER ANNEALING FOR JUNCTION FABRICATION IN CMOS DEVICES. Somit Talwar, Yun Wang, Verdant Technologies, San Jose, CA; Mike Thompson, Cornell University, Department of Material Science, Ithaca, NY.

Conventional rapid thermal annealing has evolved to shorter times and higher temperatures to limit transient enhanced diffusion and improve dopant activation. Current spike annealing technologies achieve sub-100 millisecond exposures near the peak temperature. On the other extreme, laser thermal processing achieves activation in the nanosecond timescale, but requires surface melting and additional layers to address geometry issues. Ion implantation damage annealing and dopant activation for ultra shallow junctions using laser annealing has been explored in the well known melt and a new solid-phase regime. We report here on the intermediate regime - solid-phase annealing with total heating times of microseconds. Low energy boron, phosphorus and arsenic implanted samples were cycled with peak temperatures up to the single crystal melting point using either a single cycle, or multiple cycles for increased time at temperature. Activation of all three dopants was achieved with minimal diffusion. Defect evolution and annealing time limitations and mechanisms have been investigated by SIMS, TEM, and in-situ probes. Preliminary results suggest that this type of annealing can readily achieve the 20 nm ultra shallow junctions required for the 65 nm NTRS node.

9:30 AM D7.3
EXPERIMENT AND MODELISATION RESULTS ON LASER THERMAL PROCESSING FOR ULTRA-SHALLOW JUNCTION FORMATION: INFLUENCE OF LASER PULSE DURATION. M. Hernandez, J. Venturini, D. Zahorski SOPRA, Bois Colombes, FRANCE; G. Kerrien, T. Sarnet, D. Dé barre, J. Boulmer Institut d'Electronique Fondamentale, UMR CNRS 8622 Université Paris-Sud, Orsay, FRANCE; C. Laviron, M.-N. Semeria CEA-DRT - LETI/DTS - CEA/GRE, Grenoble, FRANCE; D. Camel, J.-L. Santailler CEA-DRT - DTEN/LESA - CEA/GRE. Grenoble, FRANCE.

According to the International Technology Roadmap for Semiconductors (ITRS), the doping technology requirements for the MOSFET source and drain regions of the future CMOS generations lead to a major challenge. A critical point of this evolution is the formation of ultra-shallow junctions(USJ) for which present technologies, based on ion implantation and rapid thermal annealing, will hardly meet the ITRS specifications. Laser Thermal Processing (LTP) has been shown to be a potential candidate to solve this fundamental problem. In the present paper, LTP experiments have been performed with two XeCl excimer lasers (λ = 308 nm) with different pulse characteristics. The first laser (Lambda Physics, Compex 102) delivers 200 mJ laser pulses with a duration of $\approx$ 25 ns. The second laser is an industrial tool (SOPRA, VEL 15) that delivers 16 J laser pulses with a duration of $\approx$ 200 ns and allows to anneal a few cm^2 die in a single laser shot. Here we examine the influence of the pulse duration on LTP of B^+ (with and without Ge^+ pre-amorphization) and $BF(2)^+$ implanted silicon samples on the basis of real-time optical monitoring of the laser induced melting / recrystallisation process, four-point probe resistivity measurements, secondary ion mass spectrometry (SIMS) depth profiles. Experimental results are compared to model calculations developed in the framework of an industrial software (FIDAP) with pulse characteristics of both laser pulses. The activated dopant dose, junction depth and sheet resistance, as a function of the laser fluence and shot number for both lasers, confirm the efficiency of laser processing to realize ultra-shallow and highly doped junctions required for the future CMOS generations. Influence of the pulse duration on the USJ formation process is also discussed.

9:45 AM D7.4
A COMPARISON OF SPIKE, FLASH, SPER AND LASER ANNEALING FOR 45nm CMOS. Richard Lindsay, K. Henson, Wilfried Vandervorst, Karen Maex, IMEC, Leuven, BELGIUM; Bartek J. Pawlak, Radu Surdeanu, Peter Stolk, Philips Research Leuven, BELGIUM; Jorge Kittl, Affiliate Researcher at IMEC from Texas Instruments; Cristina Torregiani, Simone Giangrandi, Master's Stage at IMEC from University of Pavia, ITALY; Abhilash Mayur, Applied Materials, Santa Clara, CA; Jonathon Ross, Steve McCoy, Jeff Gelpey, Kiefer Elliot, Vortek Technologies, Vancouver, CANADA; Xavier Pages, ASM Belgium, Leuven, BELGIUM.

Due to integration concerns, the use of meta-stable junction formation approaches like laser thermal annealing (LTA), solid phase epitaxial regrowth (SPER), and flash annealing has largely been avoided for the 65nm CMOS node. Instead fast-ramp spike annealing has been optimised along with co-implantation to satisfy the device requirements, often with the help from thin offset spacers. However for the 45nm CMOS node it is widely accepted that this conventional approach will not provide the required pMOS junctions, even with changes in the transistor architecture. In this work, we will compare junction performance and integratablity of fast-ramp spike, flash, SPER and laser annealing for 45nm CMOS. The junction depth, abruptness and resistance offered by each approach are balanced against device uniformity, deactivation and leakage. Results show that the main contenders for the 45nm CMOS are SPER and flash annealing - but both have to be rigorously optimised for regrowth rates, amorphous positioning and dopant and co-implant profiles. From the two, SPER offers the best junction abruptness (<2nm/dec) with leakage at the limit of the 45nm requirements (1E-3A/cm2), while the flash anneal has the benefit of higher solid solubility (5E20at/cm3) and less transistor modifications. As expected, Ge and F co-implanted spike annealed junctions do not reach the 45nm node requirements. For full-melt LTA, poly deformation on isolation can be reduced but geometry effects result in unacceptable junction non-uniformity. The merits of SPER and flash annealing are discussed.

10:15 AM *D7.5
SILICIDES FOR 65 NM CMOS AND BEYOND. Jorge A. Kittl[a], Anne Lauwers, Oxana Chamirian[b], Mark Van Dal[c], Amal Akheyar[d], Muriel de Potter, Richard Lindsay and Karen Maex[b], IMEC, Leuven, BELGIUM. [a]Texas Instruments (affiliate researcher at IMEC); [b]IMEC and EE Department, KU Leuven; [c]Philips Research Leuven; [d]Infineon Technologies (affiliate researcher at IMEC).

As CMOS scaling ventures into the 65 nm node and beyond, with gate lengths decreasing from 40 to 25 nm and below and junction depths well below 100 nm, the constraints for silicidation processes result in new and harder challenges. As Co silicide, the industry's choice for previous nodes, suffers from linewidth scaling issues, the emphasis in development has switched to alternative materials. This paper presents an overview of silicide development activities at IMEC for the 65 nm node and beyond, with emphasis on Ni silicide as well as in Co based and Ni based alloy silicides (such as Co-Ni and Ni-Pt). Fundamental aspects of the silicidation reactions are reviewed, such as the reaction kinetics, mechanism of thermal degradation, effect of alloying elements and thickness scaling as well as their implications for implementation into advanced CMOS flows. The effects of substrate crystallinity, dopants and alloying elements (such as Ge) are also addressed as well as the impact of processing variables and device geometry on parameters such as narrow line sheet resistance, diode leakage and contact resistivity.

10:45 AM D7.6
NEW METHOD OF $CoSi_2$ FORMATION USING Co/Co-Ti ALLOY/TiN-CAP PROCESS. Masanori Uchida and Tatsuya Inoue, Fujitsu VLSI Ltd., Mie, JAPAN; Takaki Kurita and Akira Takenaka, Fujitsu Ltd., Mie, JAPAN; Shigeo Kodama, Fujitsu Laboratory Ltd., Kanagawa, JAPAN.

In the fabrication of ultra large-scale integrated (ULSI) circuits, cobalt silicide has been used for reducing the parasitic resistance of polysilicon-gate and source/drain area. As the conventional co-silicide process, Co/TiN-cap deposition is used at recently process. However, the conventional process makes bad morphology of $CoSi_2$ due to agglomeration, result in the increasing of junction leakage current. In order to improve these problems, we studied the new cobalt-silicide process using Co/Co-Ti-alloy stack deposition with TiN-cap. This Co/Co-Ti-alloy stack process obtains better uniformity, lower resistance and lower Junction Leakage Current at thickness ratio=1 (50% Co and 50% Co-Ti alloy stack) compare with conventional Co/TiN-cap or Co-Ti/TiN-Cap Process. As the results depth profiles of Co and Ti, the $CoSi_2$ using Co-Ti/TiN-cap process is confirmed to exist highly Ti Concentration at the $CoSi_2$ surface. On the other hand, Co/TiN-cap and Co/Co-Ti/TiN-cap process are good uniformity of Ti concentration, and Co/Co-Ti/TiN-cap process is fifty times higher concentration compare with Co/TiN-cap process. We conclude that the difference in the Ti concentration can affect the morphology, and the high concentration of Ti is effective for suppressing the agglomeration of $CoSi_2$ and the junction leakage current. According to improve the uniformity of Ti concentration in $CoSi_2$, Ti uniformly diffuses into $CoSi_2$ grain boundary. We proposed that the relationship between the Ti behavior in $CoSi_2$ and the junction leakage current due to agglomeration.

11:00 AM D7.7
LOW RESISTIVITY NICKEL AND PLATINUM GERMANO-SILICIDE CONTACTS TO ULTRA-SHALLOW JUNCTIONS

FORMED BY SELECTIVE CVD SiGi TECHNOLOGY FOR NANOSCALE CMOS. Jing Liu, Hongxiang Mo, Mehmet C. Ozturk, North Carolina State University, Department of Electrical and Computer Engineering, Raleigh, NC.

One of the key challenges for future CMOS technology nodes is to form source/drain junctions with very small parasitic series resistance. This requires fundamentally new junction and contact formation technologies to produce ultra-shallow junctions with super-abrupt doping profiles, above solid solubility dopant activation and contact resistivity values near 10^{-8}ohm-cm^2. Recently, this laboratory reported a new technology based on selective deposition of heavily doped SiGe alloys in source/drain regions isotropically etched to the desired depth. Of particular interest to this paper is the smaller bandgap of SiGe resulting in a smaller metal-semiconductor barrier height, which is a key advantage in reducing the contact resistivity. In this paper, we present our recent results on Pt and Ni germanosilicide contacts formed on boron and phosphorus doped SiGe alloys. The contacts were formed by sputter deposition of 10 - 30 nm thick Ni and Pt layers followed by rapid thermal annealing in nitrogen. Our results show that both Ni and Pt germanosilicide contacts can provide contact resistivity near 10^{-8}ohm-cm^2 on boron doped SiGe. On phosphorus doped SiGe, Ni germanosilicide can yield a low contact resistivity near 10^{-8}ohm-cm^2. However, the contact resistivity obtained with Pt germanosilicide is substantially higher possibly due to Pt germanosilicide Fermi-level being closer to the valence band. The thermal stability of Ni germanosilcide was found to be limited to approximately 500°C for a Ge concentration around 50%. On the other hand, Pt germanosilicide is stable up to 800°C. We have also shown that the thermal stability and film morphology of Ni germanosilicide could be improved using a thin Pt interlayer without sacrificing the sheet or contact resistance values. Using this approach, we have shown that high quality germanosilicide contacts that satisfy the requirements of future CMOS technology nodes can be formed on boron and phosphorus doped SiGe alloys.

11:15 AM D7.8
NiSi FORMATION IN THE Ni(Ti5%)/SiO_2/Si SYSTEM. R.T.P. Lee, D.Z. Chi, and S.J. Chua, Institute of Materials Research and Engineering, SINGAPORE.

NiSi formation in Ni(5%Ti)/SiO_2/Si system was investigated. p-type 10-15 Ω·cm(100) Si wafers were used in this study. A thin layer of silicon oxide ~12Å was grown on some of the wafers using Shiraki cleaning process. Pure Ni and Ni(5%Ti)-alloy films of thickness ~300Å were then deposited on all wafers by sputter deposition (co-sputtering of Ni and Ti was used for Ni(5%Ti) alloy film deposition). The concentration of Ti in the Ni(5%Ti) films was measured by Rutherford back scattering (RBS). Rapid thermal annealing (RTA) silicidation was performed in N_2 ambient for 60s at different temperatures. Four points probe, X-ray diffraction (XRD), secondary ion mass spectroscopy (SIMS) and cross-sectional transmission electron microscopy (XTEM) were used for monitoring silicidation reaction process as well as silicide film analyses. It was found that the thin interfacial oxide (Shiraki oxide) is an effective diffusion barrier for Ni as no silicide formed in the Ni/SiO_2/Si system up to 700°C. However, a drastic reduction in the ability of the interfacial oxide in blocking Ni diffusion was observed in the Ni(5%Ti)/SiO_2/Si system. For example, in Ni(5%Ti)/SiO_2/Si system, it was found that NiSi forms at temperatures as low as 400°C. The observation of NiSi formation at much lower temperatures in the Ni(5%Ti)/SiO_2/Si system, compared to the Ni/SiO_2/Si system, is attributed to the formation of $Si_xO_yTi_z$ diffusion membrane by the reaction of Ti and interfacial oxide and resultant diffusion of Ni into underlying Si substrate. It is thought that NiSi may directly form in the Ni(5%Ti)/SiO_2/Si system, bypassing the Ni-rich Ni_2Si phase, due to the much reduced Ni supply for silicidation reaction. It was also found that the NiSi/Si interface in the Ni(5%Ti)SiO_2/Si system is more planar than that observed in NiSi/Si and Ni(5%Ti)/SiO_2/Si systems.

11:30 AM D7.9
PERFORMANCE OF PLATINUM SILICIDE FOR LOW BARRIER SCHOTTKY CONTACTS P-MOSFETS. Guilhem Larrieu, Emmanuel Dubois, IEMN/ISEN UMR CNRS 8520, Villeneuve d'Ascq, FRANCE.

One of the grand challenge imposed by CMOS down-scaling is the optimisation of the source/drain (S/D) architecture, e.g., dopant activation above solid solubility, steep dopant profiling, low silicide specific contact resistivity. Recently, the concept of very low Schottky barrier S/D MOSFET has emerged as a possible alternative to the conventional architecture using highly doped S/D and midgap silicide ohmic contacts. For p-MOSFETs integration, platinum silicide is an excellent candidate because of its very low barrier to holes. This paper proposes a detailed study of the platinum silicidation reaction obtained by rapid thermal annealing (RTA) based on X-ray photoemission spectroscopy (XPS), transmission electron miscrocopy (TEM) and low temperature-dependent current-voltage measurements. Using XPS analysis, it is shown that: i) an initial silicide layer is formed at room temperature, ii) three stable phases Pt, Pt_2Si, PtSi can not coexist providing to iii) the annealing ambience is strictly controlled to avoid the formation of a SiO_2 barrier due to oxygen penetration through few nanometers thick platinum layers. Starting from an initial 15 nm thick Pt layer subsequently annealing at 400°C, TEM cross-sections reveal that homogeneous 30 nm PtSi layers with a uniform grain size distribution are formed. Finally, current-voltage characteristics have been measured on a special test structure that accounts for the lateral disposition of S/D regions in a typical MOSFET architecture. It consists in two back-to-back Schottky contacts separated by a narrow silicon gap both on bulk silicon and silicon-on-insulator substrates. Based on temperature-dependent electrical measurements (Arrhenius plot), it is shown that in addition to thermionic emission, field emission is also involved in the current transport mechanism. An excellent current drive performance of 220 μA per micron width has been obtained for a 45 nm silicon gap on a 10 nm thick SOI substrate.

11:45 AM D7.10
LOW SCHOTTKY BARRIER ON n-TYPE Si FOR n-CHANNEL SCHOTTKY SOURCE/DRAIN MOSFETS. Meng Tao, Darshak Udeshi, Shruddha Agarwal, Nasir Basit, Eduardo Maldonado, and Wiley P. Kirk, NanoFAB and Dept of Electrical Engineering, Univ of Texas, Arlington, TX.

Schottky source/drains in Si MOSFETs provide very shallow junctions, small series resistance, immunity to latchup, and simplified fabrication. They also have the potential to outperform bipolar-junction MOSFETs with their small internal capacitance and resistance. In fact, Schottky diodes have shown performance comparable to tunneling diodes and oscillation diodes with cutoff frequency well into the terahertz regime. The p-channel Si Schottky S/D MOSFET has been demonstrated at a number of university and industrial labs. The bottleneck for the n-channel Schottky device is the fact that none of the common metals or metal silicides has a low enough barrier height (~0.2 eV) on n-type Si for a large drive current. Exotic materials, therefore, have to be used to obtain the right barrier height, such as erbium silicide that is readily oxidized in air, or titanium germanide-silicide that introduces many more process parameters. A method to produce low Schottky barrier on n-type Si with common metals such as Al, Cr, and possibly Ti will be reported in this talk. The interface between metal and Si is engineered at the atomic scale to reduce interface states, and the engineered interface shows inertness to chemical and electronic processes at the interface. One consequence of this electronic inertness is that the Schottky barrier height is now more dependent on metal work function. Al, Cr, and Ti all have work function very close to the conduction band of Si. It has been found that the Schottky barrier of Al on engineered n-type Si(001) is 0.1 eV, and that of Cr is 0.25 eV. These numbers are significantly different from the decades-old data on Schottky barrier height. Mg contacts on engineered Si(001) demonstrate that the interface is thermally stable up to at least 375°C. These results bring new hope for the n-channel Si Schottky S/D MOSFET with a metal commonly used in the semiconductor industry.