SYMPOSIUM G

Integration of Heterogeneous Thin-Film Materials and Devices

April 23 – 24, 2003

Chairs

Harry A. Atwater
Applied Physics Department
Harvard Univ
Pierce Hall
Cambridge, MA 02138
617-496-9489

Michael Current
Current Scientific
San Jose, CA 95124-1700
408-265-6192

Miguel Levy
Physics Department
Michigan Technological Univ
Houghton, MI 49931
906-487-2084

Timothy D. Sands
School of Materials Engr
Purdue Univ
1289 MSEE Bldg
West Lafayette, IN 47907-1289
765-496-6105

Proceedings to be published in both book form and online
(see *ONLINE PUBLICATIONS* at www.mrs.org)
as Volume 768
of the Materials Research Society
Symposium Proceedings Series

* Invited paper

SESSION G1/D4: JOINT SESSION HETEROGENEOUS INTEGRATION AND STRAINED Si TECHNOLOGIES

Chairs: Tsu-Jae King and Timothy D. Sands
Wednesday Morning, April 23, 2003
Golden Gate C1/C2 (Marriott)

8:30 AM *G1.1/D4.1

HETEROGENEOUS INTEGRATION OF SiGe, Ge, AND GaAs WITH Si. E.A. Fitzgerald, Department of Materials Science and Engineering, Cambridge, MA.

A long sought after goal has been to expand the product offerings in semiconductors through the use of new materials. Traditionally, new materials required new and sometimes novel infrastructure to process and manufacture materials and devices. One of the barriers to utilizing incumbent manufacturing infrastructure has been the dissimilarity in semiconductor materials. For example, lattice mismatch between semiconductor materials has prevented most novel materials from being monolithically integrated on a common substrate. In this talk, we show that relaxed SiGe is a pathway for introducing novel semiconductor materials in Si CMOS infrastructure. Although strained Si is now attracting much interest, strained SiGe and Ge heterostructures integrated on Si may offer even greater performance enhancements. In addition, we have demonstrated continuous wave, room temperature GaAs and InGaAs lasers on Si using this materials technology. As the use of relaxed SiGe increases, increased Ge concentration allows the introduction of more complex heterostructures for electronics and optoelectronics. We also show that relaxed SiGe on Si creates a new path for wafer bonding, in which relaxed SiGe, Ge, and GaAs across entire Si substrates can be transferred to Si wafers and SiO_2/Si wafers. These integrated materials structures are promising for the monolithic integration of advanced electronics and optoelectronics with Si CMOS.

9:00 AM *G1.2/D4.2

CHALLENGES AND OPPORTUNITIES FOR HIGH PERFORMANCE MOSFETS WITH STRAINED Si/RELAXED SiGe CHANNEL. Ken Rim, IBM SRDC, T.J. Watson Research Center, Yorktown Heights, NY.

Strained Si/relaxed SiGe MOSFETs have received considerable amount of attention as the device structure that can provide performance boost to silicon CMOS technology. The enhancement is the result of change in electronic properties of Si under strain, and therefore is largely in addition to the benefits provided by continued geometric scaling of devices. Analysis shows that strain-induced mobility/current increase can be used to improve trade-offs in scaling scenarios for high performance CMOS technology. Electrical characterizations on fabricated MOSFETs have quantified the strain dependence of electron and hole mobility as well as the impacts due to strain-induced band offsets. The results help define the challenges for obtaining enhancements for both NFET and PFETs in a cost-effective manner with minimal disturbance to device and circuit design. On the other hand, dislocation defect formation in strained heterolayers is critical to the layer design and process windows in device integration. The impact of strain on the performance is not as readily quantified in aggressively scaled devices since many factors contribute to the characteristics and performance of scaled MOSFETs. Interactions between lattice mismatch-induced strain and fabrication process-induced stress can make analysis very complicated. Material analysis and novel electrical measurements were used to probe the impact of strain in very small devices, showing that strain-induced mobility enhancement can be retained even in sub-100 nm channel lengths. Si/SiGe heterostructures allow novel device structures and process techniques suitable for ultra-thin body devices. Such devices can combine the advantages of enhanced transport in strained layers and extreme device scaling enabled by ultra-thin body and double gate structures. Some of the progresses in materials and device structures will be presented.

9:30 AM G1.3/D4.3

RELAXATION OF A COMPRESSED FILM ON A COMPLIANT SUBSTRATE: EXPANSION, WRINKLING, AND FRACTURE. Rui Huang, The University of Texas at Austin, Dept of Aerospace Engineering and Engineering Mechanics, Austin, TX; J. Liang and Z. Suo, Princeton University, Dept of Mechanical and Aerospace Engineering, Princeton, NJ; H. Yin and J.C. Sturm, Princeton University, Dept of Electrical Engineering, Princeton, NJ; K.D. Hobart, Naval Research Laboratory, Washington, DC.

A compressively strained, epitaxial SiGe film was transferred to a Si wafer coated with a glass layer, and then patterned into islands of various sizes. Upon annealing, the glass flows and the SiGe relaxes. The initial relaxation process includes both lateral expansion and wrinkling. The competition sets a critical island size. For small islands, expansion dominates, resulting in flat and relaxed SiGe islands. For large islands, wrinkling is significant. After a long annealing, the wrinkles either disappear or cause the film to fracture. We model the relaxation process using a nonlinear plate theory for the film and a lubrication theory for the glass and simulate the evolution of the displacements (in both lateral and vertical directions) and stresses in the film. The results are compared to experiments. By comparing the time scales of expansion and wrinkling, an explicit formula is obtained to estimate the critical island size. For large islands, we show that a tensile stress builds up as the wrinkle grows and fracture occurs at a stress level depending on the flaw size in the film. We demonstrate that a cap layer suppresses wrinkling, relaxing a large island crack-free.

9:45 AM G1.4/D4.4

RELAXATION OF SiGe FILMS FOR FABRICATION OF STRAINED Si DEVICES. J.S. Maa, D.J. Tweet, J.J. Lee, and S.T. Hsu, Sharp Labs of America, IC Process Technology Lab, Camas, WA; K. Fujii, T. Naka, T. Ueda, T. Baba, N. Awaya, and K. Sakiyama, Sharp Corporation, IC Group, Process Development Center, Tenri, JAPAN.

In the fabrication of SiGe/Si heterostructure devices, the biaxially-strained Si layers are usually deposited on a virtual substrate formed from a several micron thick compositionally graded SiGe layer[1]. Recently a simpler approach utilizing H or He implantation to enhance relaxation of thinner SiGe films was reported[2]. SiGe with up to 20 at.% Ge was effectively relaxed after implantation with 2-3E16 cm-2 of H and subsequently annealed at a temperature higher than 700C. For SiGe with up to 30 at.% Ge, He implantation was needed. Since the SiGe film thickness was limited to about 100 nm, subsequent growth of a second SiGe layer required further surface cleaning, which was likely to cause an increase in defect density. In this current work, a similar implantation approach is used to enhance the relaxation of SiGe films. However, relaxation beyond the previously reported limit is demonstrated. Experiments are performed on CVD deposited SiGe films with Ge fractions ranging from 20% to 40% and thickness in the range of 100nm to about 500nm. After annealing in the temperature range of 700C to 900C, relaxation of more than 80% is achieved. PMOS and NMOS devices are successfully fabricated and much enhanced hole and electron mobilities are demonstrated. [1] K. Rim, et al., Symp. on VLSI Tech., 98 (2002). [2] H. Trinkaus, et al., Appl. Phys. Lett., 76, 3552 (2000); M. Luysberg, et al., J. Appl. Phys., 92, 4290 (2002).

10:30 AM G1.5/D4.5

SURFACE TOPOLOGY OF IN-SITU STEP-GRADED Si_x Ge_{1-x} BUFFER ON Si SUBSTRATE. Kevin K. Chan, Ray Sicina, Erin C. Jones, Patricia M. Mooney, Inna Babich, IBM Semiconductor Research and Development Center (SRDC), Research Division, Yorktown Heights, NY.

Strained Silicon layers grown on <001> relaxed SiGe buffer layers on Si are promising materials for CMOS devices because the in-plane tensile strain in the layers enhances the electrical carrier mobility in both hole and electron inversion layers. Generally, FET devices made with low germanium concentration relaxed SiGe material show significant electron mobility enhancement, but low increase in hole mobility. As the germanium concentration increases above 30% in the SiGe layer, hole mobility begins to rise. Therefore, high germanium content silicon materials are expected to be important in future microelectric device technologies, and their materials properties require increasing study. One well known problem in high germanium concentration relaxed SiGe heterostructures is poor surface roughness and high etch pit density. In this work, stepwise graded Si_xGe_{1-x} buffers with various germanium concentrations are grown in an 8 inches wafer-size CVD system. Low germanium content films, 15%, are found to have significant surface roughness, 1n RMS value of ~10nm and Z-range of ~90nm, and optical pit density by microscope as high as ~300 pits/mm^2. As the germanium concentration in the buffer layer increases, surface roughness and pit density both increase monotonically. Yet over wider range of Ge content, 15% to 60%, this Si_xGe_{1-x} buffer layer was subjected to in-situ RT annealing, it surface roughness as measured by AFM can be reduced a factor of two and the pit density reduced by a factor of four. The SiGe buffer relaxation, however, as measured by triple axis X-ray diffraction, is unchanged after in-situ annealing.

10:45 AM G1.6/D4.6

FREE STANDING SILICON AS A COMPLIANT SUBSTRATE FOR SiGe. G.M. Cohen, P.M. Mooney and J.O. Chu, IBM T.J. Watson Research Center, Yorktown Heights, NY.

We show that SiGe grown on free-standing silicon is elastically relaxed. The free-standing Si structure consists of a 20 nm-thick, 5 μm-square silicon slab supported by a SiO_2 pedestal at a single contact point at the center of the square (the cross-section resembles a mushroom). A matrix of free-standing structures was made by

patterning a bonded silicon-on-insulator (SOI) wafer and undercutting the SiO_2 to form the pedestal. Un-patterned areas of the SOI wafer and the exposed bulk Si substrate were included as reference (control) regions. A UHVCVD $Si_{0.8}Ge_{0.2}$ film was grown epitaxially on both sides of the free-standing silicon and simultaneously on the blanket SOI and bulk substrate control areas. The SiGe layer thickness was about 200 nm, which is 10 times thicker than the free-standing silicon film. Scanning electron microscope (SEM) images show faceting at the edge of the free-standing silicon squares indicating single crystal growth, and thin poly-SiGe is seen on the SiO_2 pedestal. The strain, layer thickness, and composition of the SiGe and the strain in the free-standing Si slab were determined by high-resolution x-ray diffraction (HRXRD) measurements.
The SiGe film grown on both SOI and bulk silicon was found to be fully strained. In contrast, the SiGe layer grown on free-standing silicon is ~90% strain-relaxed, and the free-standing silicon film was measured to be under tensile strain. Since the same lattice mismatch was found between the SiGe layer and the Si on the free-standing silicon and on the SOI and bulk Si control regions, we conclude that the strain relaxation of the SiGe film on free-standing Si is elastic with the strain accommodated entirely by the free-standing silicon film under tensile strain. This was further confirmed by AFM measurements. The SiGe film on the control regions showed a very smooth SiGe surface with only a few surface steps from misfit dislocations. No surface steps from misfit dislocations were observed on the surface of the SiGe film on free-standing Si. These results show that free-standing silicon serves as an ideal compliant substrate for SiGe.

11:00 AM G1.7/D4.7
HIGH Ge CONTENT (~0.6) RELAXED SiGe LAYERS AND SiGe/Ge STRUCTURES BY COMPLIANT SUBSTRATE APPROACHES. Haizhou Yin, Rebecca L. Peterson, Center for Photonics and Optoelectronic Materials, Princeton University, Princeton, NJ; K.D. Hobart, Naval Research Lab, Washington, DC; Sean R. Shieh, Thomas S. Duffy, Department of Geosciences, Princeton University, Princeton, NJ; J.C. Sturm, Center for Photonics and Optoelectronic Materials, Princeton University, Princeton, NJ.

There has been increasing interest in compliant substrates for integration of heterogeneous epitaxial materials. In our experiments, borophosphorosilicate glass (BPSG) on silicon is used as a compliant substrate to allow the relaxation of a strained silicon-germanium (SiGe) layer initially grown pseudomorphically on Si(100) substrate and then transferred to the BPSG by a bond and etch process[1]. The compressed SiGe can then relax outward by BPSG flow during a 800C anneal to soften the BPSG. This process in principle allows the formation of relaxed SiGe for subsequent devices without requiring any misfit or threading dislocations, unlike conventional relaxed buffer technology. We have previously reported how capping layers and patterning the SiGe into islands can prevent a parasitic buckling during the relaxation, to give layers with only ~1 nm roughness, but the layers were limited in Ge fraction to ~0.3. [2,3] In this talk, we first use the relaxed SiGe layer as a substrate for additional SiGe growth with higher Ge content. After anneal, strain partition between the SiGe layers is observed and consequently, the equivalent Ge percentage of fully relaxed SiGe based on lattice constant is increased. Secondly, strain partition for different thickness of the initial relaxed SiGe layer is investigated and we observe that a thinner initial layer allows more relaxation of the subsequent SiGe layer, so that an relaxed layer of x~0.6 is achieved. To further increase the lattice constant, commensurately strained (compressive) 30 nm of $Si_{0.4}Ge_{0.6}$ is deposited on pre-relaxed $Si_{0.7}Ge_{0.3}$ islands of varying thickness by CVD at 500C. Upon anneal at 800C, we observe by micro-Raman spectroscopy that the $Si_{0.7}Ge_{0.3}$ film gets stretched by the same amount as that which the $Si_{0.4}Ge_{0.6}$ film expands, indicating strain partition between the two layers, consistent with no relaxation by misfit dislocations. By varying the relative thicknesses of the layers, final relaxed layers with equivalent Ge percentages from 0.45 to as high as 0.57 are obtained. These are the highest Ge fractions known to date by compliant substrate. Finally, the strain qualities of epitaxial Ge layers on top of these structures will be described. This work is supported by DARPA. 1. K.D. Hobart, F.J. Kub, M. Fatemi, M.E. Twigg, P.E. Thompson, T.S. Kuan and C.K. Inoki, J. Electron. Mater. 29, 897 (2000) 2. H. Yin, R. Huang, K.D. Hobart, Z. Suo, T.S. Kuan, C.K. Inoki, S.R. Shieh, T.S. Duffy, F.J. Kub and J.C. Sturm, J. Appl. Phys. 91, 9716 (2002) 3. H.Yin, R. Huang, K.D. Hobart, Z. Suo, S.R. Shieh, T. Duffy, J.C. Sturm, "Prevention of Buckling during SiGe Relaxation on Compliant Substrates", MRS Spring Meeting, San Francisco, CA, 2002.

11:15 AM G1.8/D4.8
HELIUM IMPLANTATION AND ANNEALING USED FOR THE FABRICATION OF STRAINED Si ON THIN RELAXED Si-Ge LAYERS. S. Mantl, B. Hollaender, St. Lenk, D.M. Buca, S. Hogg, M. Luysberg, N. Hueging, H. Trinkaus, ISG/IFF Forschungszentrum Juelich GmbH, Juelich, GERMANY; Th. Hackbarth, H.-J. Herzog, DaimlerChrysler Forschungszentrum Ulm, Ulm, GERMANY; R. Loo, IMEC, Leuven, BELGIUM; P.F.P. Fichtner, Dept. de Metalurgia, UFRGS, Porto Alegre, BRAZIL.

Strained silicon has superior electronic properties and will be used in mainstream technology in the near future. The key problem of the implementation of strained silicon in MOSFET or MODFET devices is the fabrication of high quality strain relaxed SiGe layers on Si(100) which serve as virtual substrates for the growth of strained Si. Our approach using He or H implantation and annealing to fabricate very thin, high quality buffer layers has gained considerable interest. We will report results on the strain relaxation of epitaxial SiGe layers on Si(100) wafers with Ge contents varying between 15 and 30at%. The pseudomorphic SiGe layers were grown either by chemical vapor deposition (CVD) or by molecular beam epitaxy (MBE). In addition, results of thin buffer layers on SOI wafers will be presented. The He implantation was performed with energies between 10 keV and 20 keV and doses between 1×10^{16} cm^{-2} and 3×10^{16} cm^{-2} depending on the Ge content and the epilayer thickness. The thickness was varied between 70 and 170 nm. Annealing at a moderate temperature, typically around 850°C, was used to relax the strain. The resulting layers were investigated with numerous analytical techniques, e.g. transmission electron microscopy, AFM, He ion channeling and X-ray diffraction. The relaxed samples are very smooth (rms roughness = 0.3 nm) which allows immediate overgrowth or wafer bonding without polishing. No misorientations or inclinations are observed. Residual strain and threading dislocation density will be discussed as a function of the Ge concentration, the layer thickness, the implantation conditions and the thermal treatment. We will also show that MODFETs produced on such thin buffer layers show higher drive currents and the same RF response as devices processed on thick, step graded SiGe-buffer layers indicating the high layer quality. A model for the implantation induced strain relaxation mechanism will be discussed, which assumes the formation of misfit dislocation segments from dislocation loops punched out by gas filled platelets.

11:30 AM G1.9/D4.9
REAL-TIME OBSERVATION OF STRAIN RELAXATION IN SiGe FILMS ON ULTRA-THIN SOI VIA LOW-ENERGY ELECTRON MICROSCOPY. B. Yang, A.R. Woll[a], M.M. Roberts, D.E. Savage and M.G. Lagally, University of Wisconsin-Madison; [a]Current address: CHESS, Cornell University.

We have used low-energy electron microscopy (LEEM) to study the initial stage of strain relaxation in $Si_{0.96}Ge_{0.04}$ thin films grown on silicon-on-insulator (SOI) and bulk Si substrates. Dislocation glide, cross-slip, and reconnection interactions have been observed in real time. In general, strain relaxation is difficult to see and follow dynamically. Because of its sensitivity to the dislocation-induced strain field, LEEM is able to detect single, buried misfit dislocations. In contrast to TEM, LEEM is nondestructive and can observe dynamic events during growth. On SOI substrates, we observe dislocation glide in SiGe films that are below the critical thickness for dislocation motion on bulk Si. These results provide direct experimental evidence for a decrease in line tension of a buried misfit segment at the Si/SiGe interface caused by the finite Si layer thickness. We will discuss our data in the context of recent models of SiGe film relaxation on SOI [1, 2]. Videos of real-time observations, such as dislocation interactions, cooperative motion, and reversal of glide direction with temperature, will be presented to support the discussion of the models. Our observations have direct implications for the fabrication of strained layer devices on SOI substrates. [1] E.M. Rehder, Ph.D Thesis, University of Wisconsin-Madison, 2002; E.M. Rehder, T.F. Kuech, to be published [2] L.B. Freund, W.D. Nix, Appl. Phys. Lett. 69 173 (1996).
Supported by ONR, DARPA, and NSF.

11:45 AM G1.10/D4.10
HYBRID VALENCE BANDS IN STRAINED LAYER HETEROSTRUCTURES GROWN ON RELAXED SiGe VIRTUAL SUBSTRATES. Minjoo Lee, Eugene A. Fitzgerald, Massachusetts Institute of Technology, Dept of Materials Science and Engineering, Cambridge, MA.

Strained Si, $Si_{1-y}Ge_y$, and Ge layers grown on $Si_{1-x}Ge_x$ virtual substrates (y>x) provide a path for future high performance CMOS devices. Surface strained Si devices exhibit peak hole mobility enhancements of 2 times over bulk Si, while dual channel devices, which combine a strained Si cap with a buried compressive layer, exhibit enhancements of 3 to 8 times. When the strained layer or layers are grown to nanometer-scale dimensions, the wave function of the hole occupies a hybrid valence band where the relaxed substrate, compressive buried layer, and tensile surface layer each make strong contributions to transport. The hybridization of the valence band results from the low effective mass of holes in the out-of-plane direction, and the relative weighting factor of each layer is determined by the vertical effective field and layer thickness. For example, we

demonstrate a p-MOSFET consisting of a single 45Å strained Si layer grown on a $Si_{0.3}Ge_{0.7}$ virtual substrate with mobility enhancements comparable to those seen in many dual channel heterostructures. At high E_{eff}, the hole hybridizes the Ge-like effective mass in the relaxed buffer with the valence band splitting in the Si cap, creating a band structure which resembles a compressively strained $Si_{1-x}Ge_x$ alloy. We also demonstrate a high mobility digital alloy consisting of ~1nm alternating layers of strained Si and relaxed SiGe. In this device, the hybrid valence band allows hole mobility enhancement to remain nearly constant with E_{eff}. The high mobility of the digital alloy proves that the hole can intermix the properties of many layers at once- even when the layers are only several monolayers thick- instead of undergoing random alloy scattering. We also apply the concept of hybrid valence bands to demonstrate nearly symmetric mobility p- and n-MOSFETs utilizing strained Si and strained Ge grown on a $Si_{0.5}Ge_{0.5}$ virtual substrate.

SESSION G2: WAFER BONDING

Chairs: Nathan W. Cheung and Peter D. Moran
Wednesday Afternoon, April 23, 2003
Golden Gate C1 (Marriott)

1:30 PM *G2.1

WAFER BONDING FOR MATERIALS INTEGRATION. U. Goesele, M. Alexe, S. Christiansen, G. Kaestner, I. Radu, M. Reiche, A. Reznicek, R. Scholz, S. Senz, I. Szafraniak, Max Planck Institute of Microstructure Physics, Halle, GERMANY.

The talk will cover the status of materials integration by wafer bonding approaches involving bonding in ambient atmosphere, hydrogen or forming gas at elevated temperatures, or in ultra-high vacuum. The present understanding of layer transfer of single crystalline semiconducting materials or complex oxides by smart-cut related techniques will be reviewed with special emphasis on GaAs. A formation mechanism for nano-voids at the bonding interface will be suggested. We will comment on the requirements for exfoliating thin foils from a single crystalline material. In the area of of compliant substrates by twist wafer bonding the concept of a reduced (in contrast to the usual increased) critical thickness for dislocation generation will be introduced. We will also discuss basic questions concerning the role of wafer bonding in fabricating strained silicon layers. The talk will end with a list of open questions which should be addressed in future research on materials integration involving wafer bonding.

2:00 PM G2.2

HETEROSTRUCTURALLY INTEGRATED III-V SEMICONDUCTORS THROUGH WAFER-BONDING: INTERFACE ADHESION AND RELIABILITY. F. Shi, C.F. Xu, K.L. Chang, J. Epple, K.Y. Cheng, and K.C. Hsieh, Micro & Nano-Technology Lab Department of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign, Urbana, IL; W. Hoke, Raytheon RF Components, Andover, MA.

Wafer-level integration of various advanced high-speed/high-frequency photonic and electronic devices on a single chip requires technologies to integrate different types of semiconductors in the lateral plane of the wafers. Over the past a few years, wafer-bonding has received considerable attention for integrating mismatched materials where heteroepitaxial growth would compromise device properties through a high density of misfit and threading dislocations, and it has been reported to be an enable technology responsible for many state-of -the-art photonic devices. In this study, the material-compatibility and wafer-bondability of a few different III-V semiconductors, such as GaAs/InP, GaN/GaN, and Al0.25Ga0.75N/GaN, were reported. The surface morphologies of pre-bonding and de-bonded wafers were characterized by using Atomic Force Microscope (AFM). Scanning Electron Microscope (SEM) and Transmission Electron Microscope (TEM) were employed to study the epi-layer structures and the wafer-bonded interface microstructures. The interface adhesion (bonding strength) and reliability were characterized based upon the interface fracture energy Go from double cantilever beam (DCB) and shear strength Eo from lap shear test. By comparing the calculated atomic chemical bond strength with the measured interface fracture energy, the bondability of these different III-V semiconductors were analyzed. The potential effects from surface/interface nano-scale structures on the wafer bondability and interfacial adhesion were discussed.

2:15 PM G2.3

WAFER BONDED EPITAXIAL TEMPLATES FOR GaAs/Si HETEROSTRUCTURES. James M. Zahler, Chang-Geun Ahn, Anna Fontcuberta i Morral, Harry A. Atwater, Caltech, Dept. of Applied Physics, Pasadena, CA.

Wafer bonding and layer processes offer the promise of low-cost integration of non-lattice-matched materials. Specifically, we are interested in transferring thin films of single crystal Ge to Si support substrates to serve as epitaxial templates for optically active III-V compound semiconductors with ohmic film/substrate interfaces. We have successfully used direct wafer bonding along with hydrogen-induced layer splitting of Ge to bond and transfer single crystal Ge (100) films to Si (100) substrates without using a metallic bonding layer. Triple junction GaInP/GaAs/Ge solar cell structures have been grown on Ge/Si heterostructures. These devices exhibit photoluminescence intensity and photoluminescence decay lifetime in the GaAs top contact region and photoluminescence intensity in the GaInP active region that are comparable to devices grown on bulk Ge substrates. Ge substrates with $1x10^{17}$ cm^{-2} H^+ at 80 keV were used to transfer 600-700 nm thick films on the order of ~1cm2 for Ge/Si. Hydrophobic surface passivation and less than 0.5nm rms surface roughness as measured by contact mode AFM along with slight bond initiation pressure are suitable surface conditions for reversible room temperature bonding of Ge/Si to occur. Layer splitting is induced by a thermal cycle up to 250°C under ~0.5 MPa normal pressure leaving a transferred layer with 10-20 nm surface roughness. Electrical measurements indicate ohmic I-V characteristics for p^+/p^+ and p^+/n^+ Ge/Si wafer bonded heterojunctions with an interfacial specific resistance of less than 0.1 Ω-cm^2 for both structures giving a bonded interface allowing current injection or extraction through the bonded interface in an optical device fabricated on these templates. Additionally, p^+/p Ge/Si wafer bonded isotype heterojunctions show double Schottky barrier I-V behavior. The anneal dependence of the barrier height in these p^+/p wafer bonded heterojunctions has been studied as a means of observing the evolution of the chemical state of the bonded interface. Initial results indicate that room temperature bonded structures have a heterojunction barrier height of ~0.8eV dominated by the presence of a thin insulating interfacial layer. Upon annealing the barrier height is reduced to <0.5eV. Work in progress to be presented at the meeting focuses on characterization of the heteroepitaxial growth by fabrication of GaInP/GaAs/GaInP double heterostructures on Ge/Si epitaxial templates, and characterization of the minority carrier lifetime of the GaAs and the surface recombination velocity of the GaAs/GaInP interface.

2:30 PM G2.4

ELECTRICAL AND STRUCTURAL CHARACTERIZATION OF THE INTERFACE OF WAFER BONDED InP/Si.
A. Fontcuberta i Morral, J.M. Zahler, H.A. Atwater, Thomas J. Watson Laboratory of Applied Physics, California Institute of Technology, Pasadena, CA; M.M. Frank, Y.J. Chabal, Department of Chemistry and Chemical Biology, Rutgers University, Piscataway, NJ; P. Ahrenkiel, M. Wanlass, National Renewable Energy Laboratory, Golden, CO.

Integration of InP-based materials on Si are important to monolithically integrated $In_{1-x}Ga_xAs_yP_{1-y}$ device applications in high-speed electronics and optoelectronic devices covering minimum dispersion loss wavelengths of optical fibers at 1.3 and 1.5 microns. In this paper we study the interfacial properties of wafer bonded InP/Si. First, the electrical properties of InP/Si interface were studied by bonding InP/Si with different doping concentrations. Al contacts were deposited by evaporation on both sides of the bonded structure, and current-voltage characteristics measured as a function of the annealing time of the bonded pairs. Three different kinds of structures were studied: 1) n+InP doped to 3×10^{18} cm^{-3} bonded with n+Si doped to 1×10^{19} cm^{-3} 2) n+InP doped to 3×10^{18} cm^{-3} bonded with p-Si doped to 6×10^{14} cm^{-3} 3) p+InP doped to 3×10^{18} cm^{-3} bonded with p-Si doped to 6×10^{14} cm^{-3}. After 30 minutes of annealing at 350°C, structure 1 showed ohmic interfacial electrical properties with interfacial specific resistance of < 0.1 $\Omega \cdot cm^2$, which indicates that a tunnel junction contact is possible for the bonded InP/Si interface. When the silicon wafer is lightly doped in structures 2 and 3, the Schottky barrier current-voltage characteristics are sensitive to the InP/Si interface properties. Indeed, both the reverse and forward current are reduced during the annealing at 350°C in structure 2 and 3. This suggests the formation of a barrier at the interface during the annealing, and high-resolution transmission electron microscopy combined with electron energy loss spectroscopy, indicates the presence of an amorphous interfacial oxide. In order to understand the formation of this oxide, results of infrared absorption spectroscopy measurements of the bonded InP/Si interfaces as a function of anneal conditions will be discussed.

2:45 PM G2.5

STRAIN IN GaN FILMS BONDED TO C-FACE AND Si FACE SiC.
Jaeseob Lee, J. Park, Z.J. Reitmeier, J.J. Huening, B.T. Adekore, R.F. Davis, and R.J. Nemanich, Dept. of Mat. Sci. & Eng and Dept. of Physics, North Carolina State Univ, Raleigh, NC.

The method of direct bonding enables thin film layer transfer for heterojunction formation and the approach may overcome many of the constraints of epitaxial growth of heterogeneous materials. For

compact power applications, GaN-SiC junctions would be important to form a HBT. However, the growth of GaN on SiC requires a buffer layer which inhibits the electronic performance of the junction. Recently, we have succeeded in layer transfer of GaN film to C-face and Si-face SiC substrates. In this talk we investigate the strain in the GaN film before and after layer transfer using a combination of vibrational, structural and optical characterization methods. Epitaxial GaN layers are grown on Si(111) substrates. The layer transfer of the GaN film from Si substrate to SiC substrate was done using UHV direct bonding at 900°C for 30∼120min and HNA etching to remove the Si substrate. The samples were characterized by RT photoluminescense using the 325nm radiation, RT Raman scattering with 514.5nm excitation, and X-ray diffraction ω-2Θ scans using Cu Kα1. All three measurements indicated in-plane tensile strain for the GaN film on Si (0.34±0.03%, 0.19±0.02%, 0.26±0.01% : Raman, XRD(0002), PL). After layer transfer, a decrease of the in-plane tensile strain of the GaN film was observed for both GaN-SiC(Si-face) and GaN-SiC(C-face) (Si-face: 0.14±0.03%, 0.15±0.02%, 0.21±0.03% and C-face: 0.12±0.01%, 0.09±0.01%, 0.17±0.01% : Raman, XRD(0002), PL). The strain in both cases is attributed to the thermal misfit between the GaN and Si and the GaN and SiC (0.36% for GaN on Si and 0.17% for GaN on SiC after cooling from 900°C to RT). The GaN/C-face interface exhibits stronger mechanical bonding and a slightly increased ω-2Θ FWHM. Electrical measurements of bonding to p-type SiC demonstrate heterojunction character.

3:30 PM *G2.6
MECHANISTIC STUDIES OF SEMICONDUCTOR WAFER BONDING AND LAYER EXFOLIATION BY H IMPLANTATION.
Martin Frank, and Yves J. Chabal, Rutgers University, Dept of Chemistry, Piscataway, NJ; Anna Fontcuberta i Morral and James Zahler, California Institute of Technology, Department of Applied Physics and Materials Science, Pasadena, CA.

Wafer bonding is attractive to integrate different semiconductors to silicon, particularly when epitaxy is not possible. Moreover, using H-implantation/annealing (SmartCut technique) makes it possible to deposit thin crystalline films of most semiconductors onto a Si substrate. Methods have been developed to work with compound semiconductors. However, the mechanism for both bonding and exfoliation is not as well characterized for III-V semiconductors for lack of physical measurements, such as vibrational spectroscopy. We summarize in this talk the current understanding of silicon direct wafer bonding and exfoliation, and present new infrared absorption data on bonding of InP and Ge to silicon, and InP and Ge exfoliation by H-implantation and annealing. In general, an interface layer is formed between III-V semiconductors and silicon, incorporating some contamination (e.g. hydrocarbons) due to the poor stability of HF-etched III-V surfaces and resulting in poorer bonding. Upon H implantation in the relevant thermal window for exfoliation, H-terminated surfaces of InP can clearly be seen as precursor to exfoliation, similarly to what was observed for silicon. This observation contrast the lack of any measurable vibrational features in H-implanted SiC, and makes it possible to develop a mechanistic pathway for exfoliation.

4:00 PM G2.7
ION-CUT LAYER TRANSFER IN TERMS OF STRENGTHS OF MULTIPLE INTERFACES.
Yonah Cho, University of California, Berkeley, Dept. of Materials Science and Engineering, Berkeley, CA; Nathan Cheung, University of California, Berkeley, Dept. of Electrical Engineering and Computer Sciences, Berkeley, CA.

Recent development in layer transfer processes for multi-material integration relies greatly on the "paste-and-cut" approach. Exemplified in ion-cut processes for SOI wafers and laser liftoff transfer of GaN onto Si and copper substrates, the "paste-and-cut" approach consists of (1) bonding of two materials units and (2) separating the bonded system along a prescribed layer other than the bonded interface. In this paper, a general concept for layer transfer is presented in terms of mechanical strength of the bonding interface (γbond) and the cutting interface (γcut). We demonstrate the concept of γbond > γcut as a requirement for successful layer transfer using specific materials systems based on the ion-cut process consisting of direct wafer bonding and crack-initiated separation at the ion implantation region. γbond and γcut are measured at bonded Si/Si and Si/SiO_2 interfaces and at the hydrogen-implanted cut layer, respectively, after post-bonding annealing. By initiating a crack from one side of double-cantilever beam (DCB) shaped samples, measured equilibrium crack extension at the bonded interface or the implanted layer is directly related to γbond or γcut, representing resistance to mechanical separation or interface strength. Three modes of separation were observed in the Si/Si and Si/SiO_2 systems depending on post-bond annealing temperature. Without sufficient annealing where gbond < gcut, crack propagated along the bonded interface, and no transfer (mode I) was observed. After annealing above 200°C to achieve gbond > gcut, crack propagated fully along the implanted layer, yielding full transfer (mode III). Partial transfer (mode II) was observed between the temperature range (100-200°C) between mode I and mode III, where local variations in the bonding strength rendered alternating crack propagation between the bonding interface and the implanted layer.

4:15 PM G2.8
THE EFFECT OF SURFACE NANO-TEXTURES ON SILICON WAFER BONDING.
Z.X. Liu, Y.Cho, X.F. Meng, and N.W. Cheung, Plasma Assisted Materials Processing Laboratory, University of California-Berkeley, Berkeley, CA.

Wafer bonding is an enabling technology for materials integration in microelectronics, optoelectronics, and MEM systems. Although most published work focus on forming a permanent bond between two wafers, a growing aspect of bonding involves the use of temporary or controlled bonding, so called "Post-It" style of bonding. Surface nano-texturing could be a way to engineer the bond to a prescribed strength. In this paper, we describe the surface textures produced by low energy Ar ion sputtering under various experimental conditions. A important feature is that nanometer scale ripples can be formed, with wave vector either parallel or perpendicular to the projected direction of ion beam. The surface topography is characterized by atomic force microscopy (AFM), and topography parameters are extracted as functions of incidence angle, ion energy, and dose. Correlation of the delamination energy (measured by the crack opening method) with the topography parameters will be presented.

4:30 PM G2.9
TEM STUDY OF THE WAFER-FUSED SILICON/DIAMOND INTERFACE.
G.N. Yushin, S.D. Wolter, A.V. Kvit, F. Okuzumi, R. Collazo, Z. Sitar, North Carolina State Univ, Dept of Materials Science and Engineering, Raleigh, NC; J.T. Prater, Army Research Office, Research Triangle Park, NC.

Integration of diamond with other electronic materials is of considerable technological interest. Silicon-on-diamond (SOD) technology would significantly enhance power characteristics of devices fabricated on silicon due to diamond's thermal characteristics. Wafer bonding is a promising way to create SOD. The interface obtained during bonding will determine the properties of SOD substrates. This work focuses on transmission electron microscopy (TEM) studies of the bonded Si/diamond interfaces formed in the temperature range between 850°C and 1100°C. Bonding of both polished highly oriented diamond films and polished polycrystalline diamond films to silicon was performed in ultra high vacuum at 32 MPa of applied uniaxial pressure. The TEM investigation revealed that the interface of all the bonded samples was non-uniform. Mechanically abrupt boundary between wafers existed only in some parts of the interface, while other parts contained an up to 40 nm thick amorphous interlayer. Electron energy loss spectroscopy (EELS) revealed that this interlayer consisted of oxygen, carbon and silicon. Based on the comparison of the microstructure and chemical composition of the interface fabricated at different temperatures, we propose a model of the Si/diamond wafer fusion process.

SESSION G3: POSTER SESSION HETEROGENEOUS INTEGRATION BY FILM DEPOSITION

Chair: Michael Current
Wednesday Evening, April 23, 2003
8:00 PM
Salon 1-7 (Marriott)

G3.1
DETERMINATION OF SPACE SHIFT OF Si/SiGe/Si HETEROJUNCTION'S CAP LAYER BY GRAZING-ANGLE INCIDENCE X-RAY BACK DIFFRACTION TECHNIQUE.
Siranush E. Bezirganyan, Hakob (Akop) P. Bezirganyan, Yerevan State Univ, Faculty of Physics, Yerevan, ARMENIA; Hayk H. Bezirganyan Jr, Yerevan State Univ, Faculty of Informatics and Applied Mathematics, Yerevan, ARMENIA; Petros H. Bezirganyan Jr, State Engineering Univ of Armenia, Dept of Computer Science, Yerevan, ARMENIA.

The well established Si complementary metal-oxide-semiconductor (CMOS) or Si/SiGe heterojunction bipolar technology can be extended to high frequency applications by adding heterojunction bipolar transistors (HBTs). Presented theoretical paper concerns the application of the non-destructive and extremely sensitive Grazing-Angle Incidence X-ray Backdiffraction (GIXB, see [1]) technique for structure investigations of the Si/SiGe/Si heterojunction bipolar devices with a thick SiGe layer. Typical epitaxial layer stacks are consisting of Si-low doped emitter, SiGe layer grown as the base of a bipolar transistor on a Si wafer (the collector). A transistor design

with a low-doped emitter and a high Ge concentration in the base allows one to increase the base doping level significantly, but requires processing with a very low thermal budget to minimize dopant outdiffusion. The incorporation of C into the SiGe base of the HBT opens a new possibility in the usage of planar silicon process technology, since C is found to hamper B outdiffusion. The investigations of SiGeC/Si strain-compensated heterojunction by the grazing-angle incidence x-rays are given e.g. in [2, 3]. The lattice mismatch between Si and Ge constrains the design of Si/SiGe/Si heterojunction bipolar devices because of the limited thickness for pseudomorphic SiGe epilayers on a Si platform, i.e. there exists a maximum thickness called the critical thickness above which is necessary too much energy to strain additional layers of material into coherence with the substrate. If one grows a thick SiGe layer, which is well above the critical thickness, it relaxes to the bulk SiGe lattice constant but a large number of defects rise exponentially with temperature. Such strained layer can relax e.g. by the formation of misfit dislocations (e.g. see [3]). A thin Si cap layer and the Si wafer have the same value of the spacing period d equal to bulk Si lattice constant along the growth surface according the proposed model of Si/SiGe/Si heterostructure. At the same time a thick relaxed SiGe layer has the lattice constant equal to bulk Ge lattice constant along the growth surface. Thus, a phase shift exists between lattice space periods of the thin Si cap layer and of the bulk Si wafer (also see [3]) stipulated by misfit dislocations. GIXB is considered to be dependent on the value of phase shift between the lattice space periods and of the Bragg angle. The modern high-resolution non-destructive investigation methods are in the focus of fundamental aspects of materials research, crystal engineering, electronics etc, so the aim of our paper is the development of the GIXB theory to stimulate the non-destructive experimental investigations sensitive to space phase shift. References: [1]. A.P. Bezirganyan and P.A. Bezirganyan, Solution of the Two-dimensional Stationary Schroedinger Equation with Cosine-Like Coefficient (in View of X-ray Diffraction), Phys. Stat. Sol. (a), 105 (1988) 345-355. [2]. H.A. Bezirganyan Jr, S.E. Bezirganyan, A.P. Bezirganyan and P.A. Bezirganyan Jr, Grazing-Angle Incidence X-ray Diffraction by the Si(1-a(x)-b(x))Ge(a(x))C(b(x))/Si Heterojunction where the Germanium and the Carbon Concentrations are Periodically Varying along the Flat Layer Surface, eds. J. Veteran, D.L. O'Meara, V. Misra, P. Ho, Proc. Materials Research Society (MRS) 2002 Spring Meeting, v.716, San Francisco, CA (USA), 2002, pp. B4.31.1 - B4.31.6. [3]. A.P. Bezirganyan, S.E. Bezirganyan, H.A. Bezirganyan Jr and P.A. Bezirganyan Jr, Investigation of Si(1-a-b)Ge(a)C(b)/Si Strain-Compensated Heterojunction by the X-rays Backdiffraction Method, the Book of Abstracts of EDXRS 2002 Conference, Berlin, Germany, 2002, p.16.

G3.2
Ge DIFFUSION STUDY IN OXYGEN-IMPLANTED SiGe/Si HETEROSTRUCTURE. Zhenghua An, Ricky K.Y. Fu, Peng Chen, Dept of Physics & Materials Science, City University of Hong Kong, Kowloon, HONG KONG; Weili Liu, State Key Laboratory of Functional Materials for Informatics, Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences, Shanghai, CHINA; Paul K. Chu, Dept of Physics & Materials Science, City University of Hong Kong, Kowloon, HONG KONG; C.L. Lin, State Key Laboratory of Functional Materials for Informatics, Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences, Shanghai, CHINA.

Relaxed Silicon Germanium alloy (SiGe) layers without dislocations are important as "virtual" substrates for the subsequent fabrication of devices such as quantum wells and two-dimensional electron and hole structures. For this purpose, compositionally graded SiGe layers are widely used as buffer layers to reduce threading dislocations in SiGe alloy layers. Furthermore, it has recently been reported that a thin Si layer grown at a low temperature is effective as a buffer layer. Nevertheless, another competing choice is to form SiGe on Insulator (SiGe-OI) structure that is similar to SOI (silicon-on-insulator). This approach integrates the advantages of SiGe virtual substrate with those of SOI. In previous work, separation by implantation of oxygen (SIMOX) and ion-cut have been employed to fabricate this novel structure. In these studies, a thick and compositionally graded SiGe buffer layer was grown prior to the high quality SiGe growth, but a buffer layer that is too thick makes it difficult to get a smooth surface. Moreover, a thick buffer layer is costlier and definitely affects the device properties due to the high defect density. A graded SiGe buffer layer is not necessary for the formed SiGe-OI structure if high quality SiGe film can be fabricated prior to implantation. Thus, SIMOX can be employed to produce pseudomorphic SiGe samples within the limit of critical thickness. In addition, if the implanted oxygen peaks at the SiGe/Si interface, the high misfit defects in the interfacial region will be offset by the amorphous silicon dioxide after high temperature annealing. Therefore, this approach is quite promising for SiGe-OI fabrication. In the work reported here, a 115 nm SiGe expitaxial film with uniform germanium composition was fabricated on Si (100) substrate without a buffer layer and subsequently an 8nm Si layer was grown. Both steps were performed in an ultra-high vacuum chemical vapor deposition system at 500°C with Si2H6 and GeH4 precursors. The samples were subsequently implanted with oxygen at 60keV and a dose of 3x1017cm-2 at 550°C, followed by annealing at high temperature in flowing Ar ambient. Rutherford backscattering spectroscopy/channeling (RBS/C) measurement was preformed to study the crystal quality and Ge diffusion punching through the oxygen-rich region into the substrate. High-resolution X-ray diffraction (HRXRD), atomic force microscopy (AFM) and Fourier Transform Infrared Spectroscopy (FTIR) were also used to characterize the samples.

G3.3
SPONTANEOUS GENERATION OF FREE-STANDING Ge QUANTUM DOTS ON SILICON-ON-INSULATOR. Eli Sutter, Peter Sutter, Percy Zahl, Department of Physics, Colorado School of Mines, Golden, CO.

The growth of heteroepitaxial materials on engineered composite substrates such as silicon-on-insulator (SOI) opens a new route for controlling the structural and electronic properties of materials at the nanoscale. Local lattice strain induced by Ge quantum dots grown coherently on SOI - a composite of an ultrathin monocrystalline Si template supported by amorphous SiO_2 on a conventional Si wafer, causes significant local distortion in the Si template and can be used as a tool for nanoscale band structure engineering of the Si substrate. The Ge islands themselves form on SOI initially as huts and then transform into domes, similar to the sequence of epitaxially constrained shapes they assume on bulk Si (100). While the shape sequence of epitaxial Ge islands on bulk Si ends here, we observe further dramatic morphological changes on ultrathin SOI: a spontaneous transformation to free-standing Ge islands accompanied by a breakup of the thin Si slab. We use a combination of atomic force microscopy (AFM) and transmission electron microscopy (TEM) to document the sequence of shape transformations of Ge islands on SOI. We investigate in detail the island shape evolution and redistribution of the substrate material between the islands both before and after the breakup of the ultrathin Si slab of the SOI substrate.

G3.4
IN-SITU STRESS ANALYSIS OF SOL-GEL DEPOSITED PZT THIN FILM ON $Pt/Ti/SiO_2/Si$ SUBSTRATE. Santiranjan Shannigrahi, Francis Eng Hock Tay, Tang Xiaosong, Cheryl Liew Kuan Pong, Yao Kui, Institute of Materials Research and Engineering, SINGAPORE.

Sol-gel processed films involve repeated cycles of spin coating followed by heat treatment for required thickness. In this process, films generate significant stress to the substrate, especially during the heat treatment. The understanding of such in-situ stress and their effects is very important for MEMS applications as the performance of the MEMS devices can be adversely affected. In this paper a ferroelectric thin film was successfully integrated with a micro fabricated device. The stress values are derived using a method of curvature measurements. This is done in each layer of film fabrication. The initial curvature of the $Pt/Ti/SiO_2/Si$ substrate is first pre-scanned by a laser-scanning machine with heating capability. The substrate, after coating with a thin layer of PZT green gel, is again transferred into the laser-scanning machine. The process of sintering the PZT films is performed with preprogrammed temperature and process times, which includes heating up the sample, holding at different set temperatures, and cooling down. The values of the substrate curvature are obtained using Laser scanning at each step. The PZT film quality is analyzed by X-ray diffractometer (XRD), and the mechanical stiffness is obtained by the nano-indention technique. Five to six layers of coating and sintering steps are required to obtain a working PZT films for micro actuations. The stress value in each measurement is then calculated based on the change of substrate curvature. The stress profile is analyzed during the whole process. The stress versus temperature profile is further interpreted based on the model of polycrystalline thin films and grain growth effects. It was found that in-situ stress changes are not only important to investigate the degrees of film shrinkage during the heat treatment, but is also essential to estimate the stress effects for PZT-MEMS integration.

G3.5
STRUCTURAL AND ELECTRICAL CHARACTERIZATION OF MANGANITE BASED METAL-FERROELECTRIC-SILICON STRUCTURES. T.S. Kalkur and Ali Mahmud, Microelectronics Research Laboratories, Dept. of Electrical and Computer Engineering, University of Colorado, Colorado Springs, CO; Klaus Dimmler, Greg Huebner, David Klingensmith and Fred Gnadinger, COVA Technologies, Colorado Springs, CO.

Metal-Ferroelectric-Silicon(MFS) structures are important in the fabrication of high density single transistor non-volatile memory cell.

Ferroelectrics based on the manganate family have low dielectric constant, high Curie temperature and therefore are ideal for integration on silicon. In this paper, we will present structural and electrical characteristics of MOCVD deposited manganite family based ferroelectrics on silicon. The structural properties were investigated by scanning electron microscopy(SEM), x-ray photoelectron spectroscopy, x-ray diffraction, transmission microscopy and Rutherford backscattering. The electrical characterization of the MFS structures were performed by capacitance-voltage(C-V) and current-voltage(I-V) measurements. The C-V characteristics show a memory window and the direction of memory window corresponds to ferroelectric polarization. We will also present preliminary results on MFSFETs(Metal Ferroelectric Silicon Field Effect Transistors) fabricated with manganite based ferroelectric gate dielectrics.

G3.6
LEAKAGE CURRENT AND DIELECTRIC PROPERTIES OF $Ba_{0.5}Sr_{0.5}TiO_3$ FILMS DEPOSITED BY RF SPUTTERING AT LOW SUBSTRATE TEMPERATURE. N. Cramer, T.S. Kalkur, ECE Dept., University of Colorado at Colorado Springs, Colrado Springs, CO; E. Philofsky and L. Kammerdiner, Applied Ceramics Research, Colorado Springs, CO.

Most studies of $Ba_{0.5}Sr_{0.5}TiO_3$ (BST) thin-film deposition have focused on chemical vapor deposition or spin-on techniques. Both these techniques require high substrate temperature (greater than 600°C), either during the deposition or during an anneal after deposition. A few groups have reported on sputtered films, but most of these studies also used high-temperature processes. While such temperatures are compatible with poly-Si plug DRAM and related technologies, they are far above the limits for technologies that require the deposition of non-refractory metals before the deposition of the ceramic film. For example, the use of Al metalization before the deposition of BST would limit the BST processing temperature to about 450°C. A process compatible with such a temperature limit is reported. Such a process makes fabrication of high-quality BST thin-films difficult, primarily due to the need for oxidation of the ceramic. The leakage current and dielectric properties of BST films deposited in such a process are reported and are shown to be sufficient for practical device applications.

G3.7
INTEGRATION OF SOL-GEL CERAMIC FILMS WITH POROUS SILICON. Sara Stolyarova, Roni El-Bahar, Yael Nemirovsky, Technion-Israel Institute of Technology, Haifa, ISRAEL; Barbara Malic, Sasha Javoric, Maria Kosec, Josef Stefan Institute, Ljubljana, SLOVENIA.

The aim of this work is integration of sol-gel derived ceramic films with porous silicon (PS). The interaction of these films with standard polished silicon wafer is found very weak, and the deposition of intermediate adhesion layers (such as platinum, for example) is usually needed. The effects of ceramic type, solvent type, solution concentration, as well as, porous silicon layer thickness, porosity and preparation conditions, on the quality and microstructure of sol-gel films/porous silicon integrated systems have been studied. The following ceramic compositions have been applied to porous silicon as protecting coatings: PZT ($PbZr_{0.53}Ti_{0.47}O_3$ and $PbZr_{0.3}Ti_{0.7}O_3$), PLZT ($Pb_{0.925}La_{0.075}Zr_{0.3}Ti_{0.7}O_3$), ZrO_2, TiO_2, $RuCl_2$ with 2-methoxyethanol and 2-ethoxyethanol solvents, 0.5 and 0.1 M concentrations. The LSC ($La_{0.5}Sr_{0.5}CoO_3$) water based sol-gels have been deposited for electroconductive purposes. The obtained composites were characterized by optical and scanning electron microscope (SEM), atomic force microscope (AFM) and x-ray diffraction. The best compositions for integration, giving mirror-like, homogenous films with fine morphology and strong adhesion, were found to be the TiO_2 and ZrO_2 sol-gels as well as, the diluted (0.1M)PZT($PbZr_{0.3}Ti_{0.7}O_3$) sol-gels. Conductive LSC sol-gel films showed improved wetting,enhanced crystallization and stronger adhesive interaction with porous silicon, as compared to polished silicon wafers. The results can be explained in terms of nano-scale fractal roughness of PS as well as different chemical composition of porous silicon surface. Thus, porous modification of silicon surface is shown to allow a direct integration of sol-gel films with silicon wafers, without intermediate layers. The obtained experimental results provide good basis for fabrication of sol-gel ceramic films/porous silicon composites for optoelectronics application.

G3.8
CONTROL OF CRYSTAL ORIENTATIONS AND ITS ELECTRICAL PROPERTIES OF PZT/Ru AND PZT/RuO_2 THIN FILMS BY MOCVD. Kazuo Shinozaki, Akinori Iwasaki, Naoki Wakiya, Nobuyasu Mizutani, Tokyo Institute of Technology, Dept of Metallurgy & Ceramic Science, Tokyo, JAPAN.

Ru and RuO_2 thin films were deposited on $LaAlO_3$, MgO and Pt/Ir/SiO_2/Si substrates by MOCVD. The crystal orientations and electrical properties of the PZT thin films deposited on the Ru and RuO_2 thin films were strongly affected by the crystal orientations and microstructure of the Ru and the RuO_2 films. : RuO_2 thin films with (100) orientation were deposited both on $LaAlO_3$ and Pt/Ir/SiO_2/Si substrates. (110)-oriented RuO_2 thin film was deposited on MgO substrate. RuO_2 thin films deposited on $LaAlO_3$ and MgO substrates at 400°C showed the high crystallinity and were epitaxially grown. RuO_2 films deposited at 400°C had most smooth surfaces and showed lowest room-temperature electrical resistivities of 110 $\mu\Omega$·cm. RuO_2 films deposited at 350°C or lower showed polycrystalline peaks by XRD. On the other hand, Ru thin films deposited at 350-500°C on $LaAlO_3$, MgO and Pt/Ir/SiO_2/Si substrates showed (001) crystal orientation. Ru thin films deposited at 400°C showed the lowest room-temperature resistivity of 95 $\mu\Omega$·cm. $Pb(Zr_{0.6}Ti_{0.4})0_3$ (PZT) thin films with 200 nm in thickness were also deposited on RuO_2 and Ru thin films by MOCVD. PZT thin films deposited at 550°C on RuO_2 substrates showed (110) orientation. PZT thin films deposited at 550°C on Ru thin film showed (001) orientation. The remanent polarization value (Pr) for (001) PZT thin film was ~70 $\mu C/cm^2$. PZT thin film with (110) orientation showed lower Pr (~30 $\mu C/cm^2$) than that with (001) orientation, but showed very low leakage current (10^{-9} A/cm^2 at 500kV/cm and 10^{-8} A/cm^2 at 700kV/cm). The good leakage characteristics were brought by the dense microstructures and very smooth surface structures. The effect of deposition rate on the structure of thin film and electrical properties were also discussed.

G3.9
CeO_2 THIN FILMS AS BUFFER LAYERS FOR Si/YBCO INTEGRATED MICROELECTRONICS. Elena Tresso, V. Ballarini, A. Chiodoni, R. Gerbaldo, G. Ghigo, L. Gozzelino E. Mezzetti, B. Minetti, C.F. Pirri, INFM-UdR ToPoli and Politecnico of Torino, ITALY; G. Tallarida, INFM-Laboratorio MDM, ITALY; G. Barucca, INFM UdR Ancona and Universita di Ancona, ITALY; C. Camerlingo, C.N.R., Istituto di Cibernetica, Pozzuoli, ITALY.

The unique properties of superconductors (such as as radiation hardness, highest microwave performances and availability to photonic applications) make the integration with semiconductor conventional electronics a stimulating challenge. Many attempts have been tried to obtain good YBa2Cu3O7-x (YBCO) films on Si substrates: yttria-stabilized zirconia (YSZ), Y2O3, MgO, SrTiO3, CeO2 and their combinations have been used as buffer layers. We present results concerning the study of Si/buffer layers/YBCO system. Goal of our work is the optimization of the multilayer deposition processes, in order to grow superconducting films (and in perspective also bi-epitaxial junctions) of quality suitable for applications in semiconductor-based electronics. We have deposited different sets of polycrystalline CeO2 films on Si(100) substrates, by RF magnetron sputtering of CeO2 targets in Ar (and O2) atmosphere. The samples have been characterized by X-ray diffraction, AFM, RBS and high resolution TEM. The preferential grain orientation, the crystals dimensions, the stoichiometry, the surface roughness and the interface Si/CeO2 have been studied. The deposition parameters (substrate temperature, RF power, O2 flow), the pre-deposition treatments and the assessment of the deposition chamber have been optimized in order to obtain repeatibility and good quality Si/CeO2 bilayers, suitable for YBCO growth. Different YBCO films have been grown at different temperatures, ranging from 690 to 720°C, on top of the CeO2/Si optimized bi-layer. The electrical, structural and morphological properties of the YBCO films have been studied and related to the properties of the substrate. Diffusion of oxygen through the multilayer has been discussed. The large transition widths in Resistance vs. Temperature dependence points toward a random in plane orientation of the films. The widths result to be too large for general-purpose applications as the envisaged Josephson Junctions layout, but it could present suitable characteristics for a cryogenic thermometer, integrated with HTSC bolometric stripes.

G3.10
CONDUCTION BEHAVIOR OF VANADIUM DOPED $Bi_{3.25}La_{0.75}Ti_3O_{12}$ THIN FILM GROWN BY PULSED LASER DEPOSITION. Jin Soo Kim, Ill Won Kim, Chang Won Ahn, Dae Su Lee, Department of Physics, University of Ulsan, Ulsan, KOREA; Jong Seong Bae, Jung Hyun Jeong, Department of Physics, Pukyong National University, Busan, KOREA; Soung Soo Yi, Department of Photonics, Silla University, Busan, KOREA.

Vanadium doped $Bi_{3.25}La_{0.75}Ti_3O_{12}$ (BLTV) thin films were prepared on Pt/Ti/SiO_2/Si substrate by pulsed laser deposition. The structural feature and surface morphology were characterized by X-ray diffraction and scanning electron microscope (SEM) studies. The ferroelectricity was confirmed by polarization-electric field (P-E) hysteresis loops. The measured value of remanent polarization ($2P_r$) of vanadium-doped BLT film was 32 $\mu C/cm^2$ with a coercive field ($2E_c$) of 150 kV/cm at the applied field of 200 kV/cm. The remanent polarization of BLTV was higher than that of BLT thin film. Almost the same hysteresis loops were observed before and after 10^{10}

switching cycles, it indicates good fatigue endurance. The dielectric constant and the ac conductivity of the Pt/BLTV/Pt capacitor were investigated in the low frequency range of 0.1 Hz - 100 kHz and the temperature range of 25°C - 400°C. The frequency dependent ac conductivity and current-voltage (I-V) measurement were used to determine the conductuin mechanism related to vanadium doping. From the slope of ac conductivity vs. 1/T plot, the activation energy was calculated at the low frequency. Also leakage currents were investigated by I-V measurements as a function of applied electric field. For the BLT thin film, the low leakage current was slowly increased from 3×10^{-7} A/cm^2 to the 2×10^{-6} up to 110 kV/cm and then rapidly increased above the field. While BLTV thin film maintained a nearly constant leakage current of 3×10^{-7}A/cm^2 at the electric field of 160 kV/cm. To determine the influence of La and V concentrations on the BLTV/Pt junction, the ferroelectric properties and conduction behavior of BLTV thin films are discussed.

G3.11
GROWTH OF YBCO ON TEXTURED COPPER TAPES.
Amit Chugh, Ashutosh Tiwari, A. Kvit, H. Wang, and J. Narayan, Department of Materials Science and Engineering, North Carolina State University, Raleigh, NC.

We have grown single crystal YBCO on passivated copper strips using Pulsed Laser Deposition technique. To passivate the copper, it is doped with different concentrations of Mg by ion implantation followed by annealing in controlled oxygen ambient. A thin layer of MgO is formed upon annealing on Cu, which prevents it from getting oxidized at high deposition temperatures. This MgO layer can be used as a template for the growth of Strontium Titanate layer (STO) and LMO based ($LaMnO_3$, $La_{0.7}Ba_{0.3}MnO_3$, $La_{0.7}Ca_{0.3}MnO_3$) perovskite layers on which YBCO can be grown epitaxially. We have also grown epitaxial TiN on copper using domain epitaxy to form Cu/TiN/MgO/STO/YBCO heterostructures. YBCO is grown on copper with MgO and STO as a buffer layer for lattice matching. The epitaxial behavior of the films is confirmed by making use of different characterization techniques like X ray diffraction, high-resolution transmission electron microscopy, z-contrast imaging and Rutherford backscattering (RBS)/channeling. T_c and J_c measurements were performed in the temperature range of 12-300 K by a DC four-probe method in a close cycle refrigerator.

G3.12
GROWTH OF C60 FULLERENE FILMS ON SEMICONDUCTOR SURFACES. Elena V. Basiuk (Golovataya Dzhymbeeva), Jose G. Banuelos, Alejandro Esparza, Jose M. Saniger, Universidad Nacional Autonoma de Mexico, Centro de Ciencias Aplicadas y Desarrollo Tecnologico, Mexico D.F., MEXICO.

There has been considerable interest in studies on film deposition techniques and physical and structural characterization of high quality fullerenes films. New interesting phenomena associated with substrate/C60 interactions can be expected. In the present study we have obtained fullerene films on such semiconductor surfaces as Ge(100), Si(100) and InP(100). Morphology and properties of the films obtained were investigated by using infrared spectroscopy, X-rays and atomic force microscopy (AFM). For film deposition we used two kinds of semiconductor surfaces: polished and patterned ones (by chemical anisotroping etching). We found that the strongest interractions are those between C60 molecules and Si surface. In this case the fullerene molecules formed a film, which is composed of tightly arrayed grains, with sizes of 80-100 nm. Furthemore, the grain shape was regular, and it can be seen from the AFM images that many grains consisted of twins, and secondary nucleation was also observed. In comparison with the Si surface, the interaction of C60 molecules with InP surface is not so strong, and the fullerene film formed has grains of bigger sizes, of 200-300 nm. In other words, the interractions between fullerene molecules in this case are stronger than those between C60 molecules on Si surfaces. Also, very interesting results were obtained for the patterned InP surface with regular microrelief (a system of parallel U-grooves, oriented in [011] direction) produced by chemical anisotroping etching in HCl acid. C60 films on such surfaces grow above the groove walls, and they are composed of grains arrayed in perpendicular direction to the groove axis. The growth mechanism of the C60 films obtained is discussed.

G3.13
EXCHANGE BIAS IN MnPd/Fe BILAYERS. Peter Blomqvist and Kannan M. Krishnan, University of Washington, Materials Science and Engineering Department, Seattle, WA.

We present here a study of the MnPd/Fe exchange bias system. The growth as well as the magnetic properties of MnPd/Fe bilayers have been investigated by means of X-Ray Diffraction (XRD), Transmission Electron Microscopy (TEM) and Vibrating Sample Magnetometry (VSM). MnPd/Fe/MgO bilayers with high crystalline quality have been deposited at different temperatures on MgO (001) substrates using the ion-beam sputtering technique. The bias field was applied along the in-plane magnetic easy axis ([100]) of Fe and along the hard ([110]) during deposition. The composition of the MnPd alloy used is 52 at% Mn and 48 at% Pd which gives a tetragonally distorted cubic unit cell. Our results indicate that there exists a narrow temperature window in which it is possible to grow c-axis oriented MnPd/Fe bilayers with limited interdiffusion. A c-axis oriented film means that the distorted axis is out-of-plane and the two a-axes are in-plane. If the temperature is lower than 400°C then a twinned a-axis oriented MnPd film is obtained [1,2]. On the other hand if the temperature is higher than 700°C interdiffusion between the antiferromagnetic and the ferromagnetic layers is initiated. The onset of interdiffusion is clearly seen as a dramatic increase of the coercivity and a change in the appearance of the hysteresis loop while the exchange bias is only slightly affected. It should be pointed out that the given temperatures are of the heater and not the actual film temperatures. When the magnetic field is applied along the bias field direction there is a sharp transition between the two saturated magnetic states whereas the transition has an intermediate state when the field is applied perpendicular to the bias direction. This behaviour is currently not fully understood but planned neutron reflectivity measurements will aid in explaining it [3].
[1] N. Cheng, J.P. Ahn, K.M. Krishnan, Journal of Applied Physics 89, 6597, (2001) [2] R.F.C. Farrow et al., Applied Physics Letters 80, 808, (2002) [3] This work is supported in part by the US-DoE under contract number DE-FG03-02ER45987 and by the Campbell Endowment at UW.

G3.14
DIRECT GROWTH OF LOW TEMPERATURE GaAs ON SILICON SUBSTRATES FOR PHOTOCONDUCTIVE SWITCHES APPLICATION. Kai Ma, Ryohei Urata, James S. Harris, Jr., and David A.B. Miller, Solid State and Photonics Laboratory, Stanford University, Stanford, CA.

GaAs was grown directly on silicon substrates by molecular beam epitaxy (MBE) at low substrate temperatures. The uniqueness of our work is that the whole growth process, including silicon wafer surface cleaning, was done at temperatures lower than Si-Al eutectic temperature. Our ultimate goal is to monolithically integrate low-temperature-GaAs (LT-GaAs) photoconductive switches with completely fabricated CMOS circuits. This approach is simple and has minimum fabrication perturbation so that problems associated with finishing the final level metallization of Si circuits after growing GaAs devices could be avoided. MSM photoconductive switches were fabricated on the LT-GaAs epilayers by depositing a titanium/gold Schottky contact and using a standard lift-off process. Time-resolved electro-optic sampling technique was used to characterize the responsivity and carrier lifetime of LT-GaAs. 1-2 picosecond lifetime was achieved and the responsivity was reasonably high. Refractive High Energy Electron Diffraction (RHEED) and Transmission Electron Microscopy (TEM) study will also be presented.

G3.15
ELECTRICAL PROPERTIES OF $Bi_{3.25}La_{0.75}Ti_3O_{12}$ THIN FILMS WITH VARIOUS GRAIN ORIENTATIONS PREPARED BY R.F. MAGNETRON SPUTTERING. Ju Hyung Suh, Sang Ho Oh, Chan Gyung Park, Dept of Materials Science & Engineering, Pohang University of Science & Technology (POSTECH), Pohang, KOREA.

Ferroelectric random access memory (FRAM) is a memory device with many advantages, such as the high density of dynamic random access memory, the fast access time of synchronous DRAM and the non-volatile property of flash memory. Among the various candidate ferroelectric oxides for FRAM, La substituted bismuth titanate ($Bi_{4-x}La_xTi_3O_{12}$, BLT) is a promising material since BLT thin films can have fatigue-free property as well as the high value of remanent polarization. Bismuth-layered perovskite has generally orthorhombic crystal lattice and is characterized by strong anisotropy of crystal structure and ferroelectric properties. So the crystal orientation of grain determines the allowed polarization direction and at microstructural range, grain orientation with optimum electrical properties can be evaluated experimentally. To evaluate the relationship between grain orientation and electrical properties of BLT thin film, comparative study of various grain orientations and orientation-dependent electrical properties of thin films deposited on various electrode system and with heat-treatment was performed. The films were deposited on epitaxial $SrRuO_3/SrTiO_3$, $SrRuO_3$/Si and Pt/Ti/SiO_2/Si substrates by using r.f. magnetron sputtering. Structure and morphology of the films were studied by X-ray diffraction, cross-sectional transmission electron microscopy, and atomic force microscopy. The BLT film grown on $SrRuO_3/SrTiO_3$ substrate revealed cube-on-cube epitaxial relationship with $SrRuO_3$ epitaxial film: $(001)_{BLT}\|(110)_{SRO}\|(100)_{STO}$, $[110]_{BLT}\|[110]_{SRO}\|[100]_{STO}$ and the resulting remanent polarization revealed nearly paraelectric property. As the degree of c-axis off-alignment to the substrate normal was increased, the spontaneous

polarization also increased but the surface roughness of films was deteriorated. And as the surface roughness was increased, leakage current density was increased from 10^{-7} up to 10^{-4} A/cm^2. In conclusion, the optimum orientation of BLT film in view of both the electrical polarization and the leakage current characteristic was found to be near (117) random orientation.

G3.16
LASER ASSISTED MOLECULAR BEAM DEPOSITION OF THIN FILMS FOR GATE DIELECTRICS APPLICATIONS.
James F. Garvey, Robert L. DeLeon, and Gary S. Tompa, AMBP Tech Corporation, Amherst, NY; Harry Efstathiadis and Richard Moore, School of NanoSciences and NanoEngineering, The University at Albany-SUNY, Albany, NY.

High dielectric constants (k), the thermal stability and the chemical stability with respect to reaction with silicon of Hafnium oxide (HfO_2), and zirconium oxide (ZrO_2) places them among the leading candidates for an alternative gate dielectric material. High dielectric constant (k) hafnium oxide (HfO_2), and zirconium oxide (ZrO_2) thin films have successfully been deposited on silicon substrates by Laser Assisted Molecular Beam Deposition (LAMBD). The films were grown at substrate temperature in the range of 30°C - 400°C and at process pressures less than 1 Torr. The LAMBD process is related to conventional Pulsed Laser Deposition (PLD). In the PLD process, the ablation plume impinges directly upon the substrate to deposit the thin film, whereas in the LAMBD process, the ablation plume is directed within a concurrently pulsed stream of a carrier gas. The carrier gas pulse serves to transport the ablated material to the substrate for deposition of the thin film. One advantage of the LAMBD process is that a chemically reactive carrier gas can be selected to produce desired chemical products. Depositions on silicon and patterned silicon substrates yielded 5 nm to 100 nm of stoichiometric HfO_2, and ZrO_2 films. Structural and chemical characterization of the films were performed by Auger electron spectroscopy (AES), cross section transmission electron microscopy (TEM), Rutherford Back-scattering (RBS) and Fourier transform infrared reflectometry (FTIR). Optical characterization was also performed by means of spectroscopic ellipsometry (SE) and infrared spectroscopic ellipsometry (IRSE), x-ray reflectivity (XRR) and focus ion beam (FIB) measurements. The films were amorphous as deposited at the lower substrate temperature. The use of the deposited films as gate dielectrics is investigated.

SESSION G4: INTEGRATION OPTOELECTRONICS
Chairs: Harry A. Atwater and April S. Brown
Thursday Morning, April 24, 2003
Golden Gate C1 (Marriott)

8:30 AM *G4.1
HETEROGENEOUS MATERIALS AND DEVICES INTEGRATION: FROM SUBSTRATE TECHNOLOGY TO ACTIVE PACKAGING.
April S. Brown, Duke University, Dept of Electrical and Computer Engineering; Nan Marie Jokerst, Georgia Institute of Technology, School of Electrical and Computer Engineering; Thomas F. Kuech, University of Wisconsin-Madison, Dept of Chemical Engineering.

Active packaging [S. Luryi, IEEE Transactions on Electron Devices, vol. 41, p. 2241, Dec. 1994] describes a generalized approach to concurrent package and device design. In our approach, the processing required for integration, such as substrate removal and bonding, is coupled with pre- and post-processing to enable new device and materials configurations not achieved in standard fabrication sequences. Specific materials processes, such as epitaxial growth sequences; and resultant material characteristics, such as the total strain, must be considered differently in the context of integration. We will focus on such materials issues for InP- and GaN-based heterojunction electronic and optoelectronic device integration processes. Both wafer bonding and device/circuit scale integration approaches are used and impact materials requirements differently. Regrowth during the integration process will also be covered. Materials characteristics, device performance, and integration yield will be discussed for both materials systems. System-level integration of an array of materials will be discussed using a planar photonic circuit demonstration. The integration of optoelectronic passives and actives into standard microelectronic packages for System on a Package (SOP), and directly onto integrated circuits for System on a Chip (SOC), involves the integration of materials which include compound semiconductors, silicon, silicon integrated circuits (such as Si CMOS), polymers, metals, and inorganic materials such as silicon dioxide and silicon nitride. Recent SOP implementations focus upon chip to chip optical interconnections using polymer waveguides and planar waveguide circuits with embedded thin film active optoelectronic devices such as photodetectors and edge emitters embedded in the waveguide/cladding structure. Embedding the thin film devices in the waveguide structure eliminates the need for beam turning elements for optical coupling in and out of the waveguide to and from the active optoelectronic devices. Such system demonstrations show the ultimate impact of heterogeneous integration technology.

9:00 AM G4.2
FABRICATION AND CHARACTERIZATION OF WAFER-BONDED GaAs- AND InP-BASED III-V SEMICONDUCTORS FOR OPTOELECTRONIC DEVICES.
Frank Shi, Kuo-Lih Chang, John Epple, Chao-Feng Xu, K.Y. Cheng, and K.C. Hsieh, Micro & Nano-Technology Lab, Department of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign, Urbana, IL.

If the last century is remembered for the birth of transistor and the development of silicon-based very-large-scale integrated circuits (VLSI), then the fabrication and integration of III-V semiconductor-based microelectronic and photonic devices with even higher operating speed and varied optical wavelength into the low-cost, mass-produced, portable system-on-chips will certainly leave its mark on this century. Typically, chip-scale integration of various advanced high-speed/high-frequency photonic and electronic devices requires technologies to heterogeneously integrate different types of semiconductors in the lateral plane of the wafers. Wafer-bonding, as one of the promising device integration approaches, has received tremendous attention and the previous researches have shown that this technique has the capabilities to yield a robust, atomically smooth, electrically conductive, and optically transparent junction interface. During the past a few years, wafer-bonding has been reported to become an enabling technology responsible for a variety of sate-of-the-art photonic devices, including visible LED's, 1.3- and 1.55-um edge emitting and vertical-cavity-surface-emitting lasers (VCSEL's), resonant-cavity photodetectors (APDs), 2-D or 3-D photonic crystals, and also other advanced optoelectronic devices. In this work, wafer-bonded GaAs/GaAs and InP/GaAs systems have been used as model material systems to characterize and fundamentally understand the transport behaviors of both n-typed and p-typed majority and minority carriers at different bonded interface junctions with emphasis on the temporal correlations of I-V electrical properties and interface microstructures caused by varied annealing conditions. Primarily based on the interface I-V characteristics, the effects of the wafer rotation alignments on both n-n and p-n interface junctions under different processing conditions will be systematically studied, quantitative relations of interface conductivity of n-n junctions and ideality factor n of p-n junctions at different alignment with varied annealing conditions will also be determined. In addition, a kinetic and thermodynamic analysis of the annealing-resulted interfacial transformation process will be performed based upon the temporal measurements of interface electrical conductivity from I-V characterization and micromorphologies from transmission electron microcopy (TEM).

9:15 AM G4.3
GaSb/GaAs WAFER FUSION FOR GaInAsSb INTEGRATED OPTOELECTRONICS. C.A. Wang, Z.L. Liau, P.M. Nitishin, Lincoln Laboratory, Massachusetts Institute of Technology, Lexington, MA.

Low-temperature fusion of GaSb-based epitaxial layers (lattice matched to GaSb substrates) to semi-insulating GaAs wafers has been demonstrated for the first time for potential monolithic integration of GaSb-based mid-infrared optoelectronics and high-speed electronics. To investigate conditions for wafer fusion, GaSb and GaAs wafers were first bonded via methanol liquid capillarity and then annealed either with or without pressure application at temperatures ranging between 350 and 600°C. Varying degrees of mass transport and covalent-bond formation (i.e., "fusion") between wafers were observed by examining cleaved cross sections using a high-resolution scanning electron microscope. A GaSb/GaInAsSb/InAsSb/GaSb heterostructure simulating a thermophotovoltaic device, was successfully fused to a semi-insulating GaAs substrate without pressure at temperatures between 350 and 450°C. Lapping and selective chemical etching was subsequently used to remove the GaSb substrate, leaving the GaInAsSb/GaSb epitaxial layers on GaAs. The GaInAsSb layer showed strong photoluminescence (PL) comparable to that of a control sample without wafer fusion. Similar wafer fusion was achieved at temperatures as low as 350°C by pressure application using differential thermal expansion in a graphite/quartz container. These samples, however, showed considerable degradation in PL intensity, indicative of defect generation due to pressure application.

10:00 AM *G4.4
SEMICONDUCTOR PHOTONIC CRYSTALS. Susumu Noda, Kyoto University, Dept. of Electronic Science and Engineering, Kyoto, JAPAN.

Recent progresses in 3D and 2D semiconductor photonic crystals

based on wafer-bonding and thin-film layer transfer techniques are described. On 3D photonic crystals, we already developed GaAs-based crystals with complete photonic bandgap [1, 2] and have recently succeeded in introduction of InGaAsP/InP-based light-emitter with artificial point defects into the crystals. Low temperature and long time heat treatment with thinning process of substrate is a key for the success. It has been observed that the strong light-emission occurs only at the artificial defects, and the suppression of light-emission occurs for the other parts. This is an important step to achieve a threshold-less laser. On 2D photonic crystals, we have utilized a SOI substrate and formed a thin slab structure with 2D triangular-lattice air hole structure to manipulate photons based on the idea which we proposed previously [3]. A line-defect waveguide and a donor-type point defect cavity with three-missing holes have been introduced into the structure. Photons propagating through the waveguide are trapped by the point defect cavity and emitted to the vertical direction. The phenomenon can be applied to, for example, ultrasmall channel add/drop filtering devices, nonlinear optical devices, and even trapping of atoms. It is shown that the Q factor as high as 3800 (which corresponds to the wavelength resolution of 0.4nm) has been realized, and photon manipulation efficiency over 45% by a single defect has been successfully obtained. A new concept of "In-plane Proportional Hetero Photonic Crystals (IPHPCs)" will be also described for the multi-wavelengths operation. [1] S. Noda, et al, Science, 289, 604 (2000). [2] S. Noda, et al, IEEE J. Quantum Electron., 38, 726 (2002). [3] S. Noda, et al, Nature 407, 608 (2000).

10:30 AM G4.5
OPTICAL AND CRYSTALLOGRAPHIC STUDIES OF ION IMPLANTED RELAXOR FERROELECTRIC LEAD ZINC NIOBATE FOR SINGLE-CRYSTAL LAYER TRANSFER. M. Levy, P.D. Moran, Michigan Technological University, Dept. of Materials Sciences, Houghton, MI; H. Bakhru, SUNY at Albany, Dept. of Physics, Albany, NY.

Single-crystal lead zinc niobate-lead titanate (PZN-PT) has been found to exhibit extremely large electro-optic and piezoelectric coefficients near the morphotropic phase boundary, with r_{33} = 500 pm/V and d_{33} = 2,500 pC/N.[1,2] As such it is an excellent candidate for highly efficient optical modulators, piezo-actuators and hybrid opto-mechanical devices. In the past we have reported on the layer transfer of PZN-PT films by crystal ion slicing.[3] Singly charged 3.8MeV helium ions are implanted nearly normal to the surface. A dose of 5 X 10^{16} ions/cm^2 yields a sacrificial layer buried several microns beneath the surface. Subsequent wet etching removes the damage layer to detach 7μm-thick rectangular films off the bulk. In this talk we examine the characteristics of the film and sacrificial layer by optical and crystallographic analysis. The implantation is found to lower the sacrificial layer refractive index for TE and TM modes at He-Ne wavelengths, thus forming an optical waveguide in the film prior to separation. Rapid thermal processing, which activates the selective etching of the sacrificial layer, modifies the refractive index profile, yielding a sharply peaked optical barrier region. Ion implantation damage and thermal processing are responsible for the changes in index of refraction. Triple-crystal X-ray diffraction analysis shows that the guiding layer maintains its single-crystal structure, but is severely strained (1.8%) by the implantation. Most of the lattice dilation and damage in the film are removed upon RTA, while sharpening up the stress in the sacrificial layer underneath. [1] Y. Barad, U. Lu, Z.Y. Cheng, S.E. Park, and Q.M. Zhang, Appl. Phys. Lett. Vol 77, 1247-1249 (2000). [2] S.E. Park and T.R. Shrout, J. Appl. Phys. Vol 82, 1804-1811 (1997). [3] M. Levy, S. Ghimire, A.K. Bandyopadhyay, Y.K. Hong, K. Moon, S. Bakhru and H. Bakhru, Ferroelectrics Lett. Vol 29(3-4), 29-40 (2002).

10:45 AM G4.6
MAGNETO-OPTIC MATERIALS FOR INTEGRATED APPLICATIONS. Sang-Yeob Sung, Na hyoung Kim, Bethanie J.H. Stadler, University of Minnesota, Dept of Electrical and Computer Engineering, Minneapolis, MN.

Bulk isolators are very important components in fiber optic systems because they protect light sources from back-reflected light. Integrating isolators with optical source platforms promises to reduce the size and cost of the total source module. Such integration is also critical to the realization of photonics integrated circuits. All of the materials necessary for integrated isolators were grown and the application of 2D photonic crystal structures to isolators has been explored. Magneto-optical garnets were grown monolithically by several methods, including metallorganic chemical vapor deposition (MOCVD), sputtering, and metallorganic chemical liquid deposition (MOCLD). A variety of substrates were used, including MgO and SiO2 which are useful buffer layers and optical claddings. The chemical, structural, and optical properties of the resulting films will be discussed, including the effects of Ce and Bi doping. One of the most interesting results is the 10% increase in refractive index of Ce-YIG with Faraday rotations as high as 0.6 deg/um at 1.3um. In order to incorporate photonic crystal structures into the magneto-optic integration scheme, we have calculated a range of radii and spacings necessary to fabricate YIG with 2D photonic bandgaps using an advanced plane-wave expansion technique. Self-assembled alumina nanostructures have been grown with these calculated dimensions, namely hexagonal close-packed pores with radii of 0.18-0.22um and center-to-center periods of 0.7-0.85um. These nanostructures were grown onto semiconductor and oxide substrates in order to demonstrate their use as RIE masks in fabricating photonic crystals. For biasing the magneto-optical elements, a variety of sputtering techniques were used to monolithically integrate permanent SmCo magnet films with coercivities as high as 1000 Oe using semiconductor-friendly processing. These magnets are sufficient for biasing our magneto-optical waveguides and photonic crystals. The chemical, structural and magnetic properties of these materials, as well as total integration with SiO2 cladding layers will be discussed.

11:00 AM G4.7
WAFER-SCALE LASER LIFT-OFF OF INDIUM GALLIUM NITRIDE LIGHT-EMITTING DIODES. J.L. Schroeder, Univ of CA, Berkeley, Dept of Materials Science & Engineering, Berkeley, CA; M.C. Yoo, Oriol, Inc., Santa Clara, CA; N.W. Cheung, Univ of CA, Berkeley, Dept of Electrical Engineering & Computer Sciences, Berkeley, CA; and T. Sands, Purdue University, School of Materials Engineering and School of Electrical & Computer Engineering, West Lafayette, IN.

The transfer of GaN-based heterostructure devices from their sapphire growth substrate to another substrate offers significant advantages in increasing device yield during packaging, improving device performance, and enabling heterogeneously integrated microsystems. The excimer laser lift-off (LLO) process, utilizing a 20-40 nanosecond uv laser pulse directed through the sapphire substrate, has been shown to be suitable for the delamination of thick (~100 micron) GaN films from 50 mm diameter sapphire substrates, as well as for the transfer of thin-film (<10 microns) LED heterostructures over smaller areas. In this presentation, a process for the complete transfer of LED devices from entire 50 mm sapphire wafers to silicon is described. An important feature of this process is the preservation of the LED orientation, necessitating a two-step process beginning with the transfer to a temporary handle substrate. Thermomechanical issues associated with pulse edge effects, pulse overlap, adhesion and bonding layer stiffness have been addressed in the design of the transfer process. Compared to conventional top-side-contacted LEDs on sapphire, the transferred LEDs with backside n-contacts show a 30% increase in front-side light output, a 400 mV reduction in forward voltage at 20 mA, a red shift of 6-7 nm associated with the relief of residual stress, and improved device lifetime at high current injection (>180 mA).

11:15 AM G4.8
INTEGRATION OF GaN LIGHT-EMITTING DIODES INTO BIOPHOTONIC CHIPS BY PIXEL-TO-POINT TRANSFER USING LASER LIFT-OFF AND Pd-In BONDING. Z.S. Luo, Department of Materials Science & Engineering, University of California, Berkeley, Berkeley, CA; T. Sands, School of Materials Engineering and School of Electrical & Computer Engineering, Purdue University, W. Lafayette, IN; N.W. Cheung, Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, Berkeley, CA.

One of the major challenges in realizing fluorescence-based lab-on-a-chip or micro-total analysis systems (u-TAS) by heterogeneous integration of the necessary components such as light sources, microfluidic channels, optical filters, and photodetectors is the direct integration of the light source into the system. The ability to integrate multi-color narrow-band sources that are spatially distributed so as to operate in the near field would provide functionality on a chip that is currently only possible on the benchtop. Recently, large-area transfer of GaN light-emitting diodes (LED) and wafer-scale transfer of GaN film have been demonstrated using "double-transfer" process. However, in order to integrate the GaN light-emitting diodes of multiple emission wavelengths with the existing Si-based electronic systems, problems of pixel pick-up from the source wafer and pixel registration to the target system need to be solved. In the present paper, a novel pixel-to-point transfer process based on the excimer laser lift-off and Pd-In transient-liquid-phase bonding scheme was developed to integrate GaN light-emitting diodes with photodetector chips and thin-film bandedge filters. The transfer was accomplished by (1) temporarily bonding the LED pixel to a specially designed pick-up rod with sapphire substrates facing up using Super Glue (2) removing the sapphire substrates using laser lift-off, and (3) permanently bonding the LED pixel to the designated area in the pre-fabricated silicon photodiodes using Pd-In transient-liquid-phase bonding. An oxygen plasma was employed to clean the Super Glue residue before further microfabrication and system integration was performed. A GaN LED with peak emission at 463 nm was used to excite 515nm fluorescence from FluoSpheres^{TM}

carboxylate-modified yellow-green fluorescent microspheres (40nm in diamters). The performance of these integrated light sources has been assessed by evaluating the fluorescence intensity as a function of LED current and dye concentration.

11:30 AM G4.9
INTEGRATION OF InGAaN-BASED OPTOELECTRONICS WITH MICROFLUIDIC CHANNELS. William S. Wong, Michael L. Chabinyc, Steven E. Ready, Michael Kneissl, and Mark Teepe.

Fabrication of microsystems frequently requires electronic and optoelectronic components fabricated from dissimilar materials. In many cases, integration of dissimilar thin-film materials by direct deposition involves substantial sacrifices in the thin-film quality and performance. For example, combining III-V nitride-based optoelectronic devices onto glass- or polymeric-based microfluidic channels by direct growth would be impossible. Direct integration through bonding and layer transfer of dissimilar materials systems can enable the desired microsystem functionality. Such a process would allow combining III-nitride-based thin-film devices with dissimilar materials selected and pre-fabricated exclusively for optimal performance and functionality rather than for growth compatibility. We have developed a method for combining InGaN-based optoelectronics with microfluidic channels fabricated on glass and polymeric substrates. A process for allowing accurate light source placement and alignment to the microfluidic channels will be presented. We will discuss the fabrication and functionality of the integrated optoelectronic/microfluidic device for bio-analytical applications.

SESSION G5: LAYER TRANSFER
Chair: Miguel Levy
Thursday Afternoon, April 24, 2003
Golden Gate C1 (Marriott)

1:30 PM *G5.1
FABRICATION OF 3-DIMENSIONAL INTEGRATED CIRCUITS BY LAYER TRANSFER OF FULLY DEPLETED SOI CIRCUITS. James A. Burns, C. Keast, K. Warner, P. Wyatt, and D. Yost, Advanced Silicon Technology, Massachusetts Institute of Technology, Lexington, MA.

Three-dimensional (3-D) integrated circuits composed of active circuit layers that are vertically stacked are expected to lead to improved logic devices, memories, CPUs, and photosensors [1]. These circuits will utilize high-density vertical interconnections, approaching the pitch of present multilevel metal vias, to achieve shorter interconnect paths. We have developed a 3-D integrated circuit technology that uses thin-film processes to bond and transfer conventional (2-D) silicon on insulator (SOI) integrated circuits to achieve stacking of multiple circuit layers and unrestricted placement of dense vertical interconnections [2].

The 2-D circuits are fabricated using a fully depleted SOI (FDSOI) CMOS technology to maximize circuit speed, to minimize power consumption, and to aid the 3-D fabrication process. Initially, a 3-D circuit is constructed from two wafers after FDSOI fabrication and test by transferring and interconnecting one FDSOI circuit layer, defined as a tier, to the tier of the second wafer. The tier to be transferred is inverted, aligned, and bonded to the bottom tier using a low-temperature oxide bonding process, and its handle silicon is then etched to the buried oxide. The buried oxide is used as an etch stop for the silicon etch to produce a thin, uniform insulating layer and is an essential factor in the 3-D assembly process. The inter-tier vias are formed by dry etching through the buried and deposited oxides to expose metal pads in the transferred and bottom tiers, after which the electrical connections are formed with tungsten plugs. Additional tiers can be bonded and interconnected by repeating the process to form 3-D circuits of three or more tiers, as demonstrated by the fabrication of three-tier 3-D via chains [3]. Since only the tiers to be transferred are fabricated on SOI wafers, this technology permits the heterogeneous integration of multiple materials and technologies to construct 3-D circuits.

[1] Y. Akasaka, Proc. IEEE, Vol. 74, No. 12, December 1986.
[2] J. Burns, et al., ISSCC Digest of Technical Papers, pp. 268-269, 2001.
[3] K. Warner et al., Proceedings of IEEE International SOI Conference, pp. 123-125, 2002.

This work was sponsored by the United States Army under U.S. Air Force contract F19628-00-C-0002. Opinions, interpretations, conclusions, and recommendations are those of the authors and are not necessarily endorsed by the United States Government.

2:00 PM G5.2
THE INFLUENCE OF THE SILICON WAFER ORIENTATION ON THE FORMATION OF H-PLATELETS IN H-ION IMPLANTED SILICON. T. Hoechbauer[a], A. Misra[a], M. Nastasi[a], M. Ridgway[b], T. Lafford[c]; [a]Los Alamos National Laboratory, Los Alamos, NM; [b]Australian National University, Canberra ACT 0200, AUSTRALIA; [c]Bede Scientific Instruments Ltd., Durham, UNITED KINGDOM.

Hydrogen implanted silicon has been shown to cleave upon annealing, thus facilitating the transfer of thin silicon slices to other substrates, a process known as "ion-cut". For the practical application of the ion-cut process it is crucial to understand the underlying mechanisms behind the formation of sub-surface H-platelet and H_2-gas bubbles, which ultimately lead to the cleavage of the silicon crystal. We investigated the effect the orientation of the silicon wafer has on the formation and arrangement of the sub-surface H-platelets. We implanted $< 100 >$, $< 111 >$, and $< 110 >$ silicon wafers with 40 keV H-ions to a dose of 2e16 H/cm^{-2} at cryogenic temperatures. The samples were either left in their as-implanted state or vacuum annealed at 380°C for 30 minutes. Following the sample preparation, all samples were examined by a combination of Rutherford backscattering spectroscopy (RBS) in channeling mode, elastic recoil detection (ERD) analysis, and transmission electron microscopy (TEM). Mechanical stresses in the material, caused by the proton irradiation, were determined by measuring curvature changes of the silicon samples utilizing a laser scanning setup. Double crystal X-ray diffraction (DCXRD) measurements provided information about the out-of-plane strain buildup in the material during the H-ion implantation. The obtained results will be discussed in terms of strain buildup in the implantation zone due to mechanical stresses, introduced into the substrates by the H-ion implantation and their enhancing effect on H-platelet formation.

2:15 PM G5.3
ORIGIN OF BORON ENHANCED ION-CUT IN HYDROGEN IMPLANTED Si. Jungkun Lee, Richard Averitt, Michael Natasi, Materials Science and Technology Division, Los Alamos National Laboratory, Los Alamos, NM.

The mechanism underlying the exfoliation phenomenon in B+H co-implanted Si is presented. Though boron is known to enhance the hydrogen induced transfer of a silicon layer, the origin of B+H co-implantation effect is still controversial. N-type Si substrates with the conductivity of 1 - 10 ohm-cm were implanted with B; half of these samples were given an activation anneal at 900°C and the other half were left in as-implanted state. The B implanted samples were implanted with 40 keV H^+ at a depth of 475 nm and then annealed at several temperature. The lattice damage and the hydrogen concentration were analyzed with Rutherford back scattering (RBS) in channeling mode and the elastic recoil detection (ERD), respectively. Also, the chemical bonding in the implanted Si substrates was monitored by Infrared Spectroscopy (IR). Compared with only H implantation, B+H co-implantation decreased the lattice damage in spite of the enhanced blistering, which was more pronounced in non-activated case. IR showed that this inconsistent behavior originated from the change in the internal defect structure. Boron reduced the stability of interactions between H and Si, and controlled the type and the content of Si-H multi-vacancy defects in Si substrates. This change in the defect structure of B+H co-implanted samples is attributed to B enhanced Si-defect annihilation, which in turn promotes the formation of H^2 and the enhanced exfoliation in Si.

3:00 PM G5.4
LOW TEMPERATURE FABRICATION OF SEALED Si CAVITIES BY DIRECT WAFER BONDING AND MECHANICAL ION CUT. Yonah Cho, University of California, Berkeley, Dept. of Materials Science and Engineering, Berkeley, CA; Nathan Cheung, University of California, Berkeley, Dept. of Electrical Engineering and Computer Sciences, Berkeley, CA; Tim Sands, Purdue University, School of Materials Engineering and School of Electrical & Computer Engineering, West Lafayette, IN.

Single crystalline silicon membranes on top of buried cavities and channels have many applications in micro-electromechanical systems and biosensors. The conventional approach to fabricate these structures is silicon direct wafer bonding at high temperature (~1000°C) followed by etch-back which lacks precise control of membrane thickness and lateral uniformity. Our recent work showed thermal ion-cut in combination with direct bonding can bypass the uniformity limitation, especially for membranes below thickness of microns. To accommodate a wider class of material systems for encapsulation inside such cavities, a low processing temperature is always desired. We have demonstrated mechanical ion-cut is a lower-temperature alternative to attaining sealed cavities, with the maximum processing temperature as low as 105°C required for the bonding step. Both the thermal ion-cut and mechanical ion-cut employ hydrogen ion implantation into a silicon donor wafer and

direct bonding to a handle wafer. Instead of annealing at 400-600°C to thermally initiate separation, a mechanical force is applied at room temperature to propagate a crack across the region of the peak ion concentration for the mechanical cut. Our study will compare layer transfer/failure mechanisms over cavities by the two cutting methods. Both cut methods yielded mirror finish as-cut surfaces with RMS roughness below 4 nm across a 5 μm by 5 μm area. Using the room temperature mechanical cut method, 0.3 μm-thick membranes were successfully transferred over 5 μm x 5 μm square cavities and 2 μm x 100 μm channels. SEM and optical images have revealed an anisotropic failure mode over larger cavities by the mechanical-cut method. Critical factors (e.g. transfer thickness, cavity dimensions, orientation of the cavity for the mechanical cut, and bonding-to-cavity area ratio) affecting thermal and mechanical layer transfer over cavities will be discussed.

3:15 PM G5.5
INTEGRATION OF ZnO AND Si NANOWIRE ARRAYS BY CUT-AND-PASTE TECHNIQUES. Z.S. Luo, Department of Materials Science & Engineering, University of California, Berkeley, Berkeley, CA; H. Yan, R. Fan, P. Yang, Department of Chemistry, University of California, Berkeley, Berkeley, CA; T. Sands, School of Materials Engineering and School of Electrical & Computer Engineering, Purdue University, W. Lafayette, IN; N.W. Cheung, Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, Berkeley, CA.

The integration of nanowire building blocks into complex functional electronic and photonic microsystems represents a major scientific and engineering challenge. In most cases functional nanowire devices or device arrays cannot be fabricated directly via nanowire growth processes. The special requirements for the growth substrates (e.g. (110) sapphire substrates for ZnO nanowires grown by the vapor-liquid-solid mechanism) and the severe growth conditions for the nanowires (e.g. high temperature and the presence of Au) usually prevent the direct growth of nanowire device structures within a microsystem platform. Suitable hierarchical assembly techniques therefore are required to realize nanowire-based electronic and photonic microsystems. In this paper, we will present the demonstration of the transfer of ZnO nanowire arrays and Si nanowire arrays to virtually any substrate using two different cut-and-paste techniques. The wide bandgap (3.37eV) of the ZnO nanowire makes it a promising candidate as an ultraviolet nanolaser. Recently, optically pumped ultraviolet lasing of ZnO nanowires has been demonstrated, stimulating great interest in seeking electrically pumped ZnO nanowire lasers and in applying ZnO nanowires as laser sources in optoelectronics and photonics. ZnO nanowire arrays embedded in epoxy were successfully separated from the sapphire growth substrates by 248nm KrF excimer laser lift-off at fluences from 500mJ/cm2 to 800mJ/cm2. SEM examinations show that the nanowire arrays maintain their as-grown configuration after transfer. Since the laser lift-off process heats only the nanowire/substrate interface, this process can, in principle, be used to integrate ZnO nanowire arrays with any platform. Using the ion-cut technique, we are also able to transfer Si nanowire arrays onto various substrates by hydrogen implantation and consequent separation. Both Monte Carlo simulation and preliminary experimental results will be presented.

3:30 PM G5.6
PHOTO-POLYMER WAFER BONDING FOR TRANSFER OF GaN HETEROSTRUCTURES AND DEVICES FROM SAPPHIRE TO DISSIMILAR SUBSTRATES. V. Loryuenyong, T. Sands, and N.W. Cheung, Department of Materials Science & Engineering, University of California-Berkeley, Berkeley, CA; School of Materials Engineering and School of Electrical & Computer Engineering, Purdue University, W. Lafayette, IN; Department of Electrical Engineering and Computer Sciences, University of California-Berkeley, Berkley, CA.

A polymer wafer bonding and laser lift-off process has been developed and implemented to integrate GaN heterostructures and functional devices with dissimilar substrates. The integration process takes advantage of the high quality of GaN growth on sapphire and the complementary functionality of the receptor substrates. The process developed in this study uses an SU-8 photo-polymer both as a bonding material and as a delamination material for layer transfer. For the single-transfer experiments, SU-8 was spun onto an optically transparent handle wafer (e.g. quartz or glass) and then bonded to the GaN-on-sapphire donor wafer. UV curing of the SU-8 through the backside of the handle wafer yielded an increase in the bonding strength between the donor and the handle wafer to 0.9 J/m2. Laser lift-off of the GaN from the sapphire substrate was then performed with a 38 ns-KrF laser pulse (248 nm wavelength) transmitted through the backside of the sapphire with a fluence of 500-600 mJ/cm2, yielding a GaN/SU-8/silica glass final structure. For the double-transfer experiments, the GaN/SU-8/silica glass structure obtained was then bonded to a Si substrate using the Pd/In transient-liquid-phase method. Laser separation of the silica-glass substrate was achieved by irradiating the SU-8/quartz interface through the quartz substrate at a fluence of 50 mJ/cm2, yielding a final SU-8/GaN/Pd-In/Si structure. Detailed results on device transfer and large-area transfer will be presented.

3:45 PM G5.7
ASSEMBLY OF AlN BIMORPH THIN-FILM ACTUATORS BY PULSED LASER LIFT-OFF WITH AN INDIUM TIN OXIDE SACRIFICIAL LAYER. J.L. Schroeder, Univ of CA, Berkeley, Dept of Materials Science and Engineering, Berkeley, CA; J.R. Donnelly, Univ of CA, Berkeley, The Electronics Research Laboratory, Berkeley, CA; and T. Sands, Purdue University, School of Materials Engineering and School of Electrical & Computer Engineering, West Lafayette, IN.

Textured aluminum nitride (AlN) thin films deposited by reactive sputtering at low substrate temperatures offer uniaxial piezoelectric and pyroelectric functionality comparable to that of single crystals. Furthermore, AlN films are thermally robust with excellent chemical stability, high breakdown strength and low losses. In this presentation, the assembly of an AlN bimorph actuator by laser lift-off is described. The bimorph structure is fabricated by first depositing textured AlN films by reactive magnetron sputtering onto indium tin oxide (ITO) coated fused silica substrates. Two identical AlN/ITO/silica heterostructures are then bonded face-to-face, thereby ensuring that the spontaneous polarization vectors in the AlN films are antiparallel. The silica substrates are then removed, one at a time, by pulsed excimer laser lift-off using a 38 ns pulse at 248 nm (KrF) directed through the transparent substrate. A fluence of 250 mJ/cm2 is sufficient to selectively decompose the absorbing ITO layer at the interface, thereby separating the silica substrate from the bimorph without damaging the AlN layer. The exposed ITO films can be used as transparent electrodes, or they may be removed by etching prior to electrode deposition. The use of ITO electrodes and optically transparent adhesives enables the design of optically transparent piezoelectric actuating membranes for active micro-optical devices.

4:00 PM G5.8
POLYMER/EPITAXIAL (Pb,La)(Zr,Ti)O_3 THIN FILM COMPOSITES BY EXCIMER LASER LIFTOFF. Eric J. Carleton, Univ of California, Berkeley, CA; Tim Sands, School of Materials Engineering and School of Electrical & Computer Engineering, Purdue University, West Lafayette, IN.

In recent years a wide variety of (Pb,La)(Zr,Ti)O_3 (PLZT) based MEMS sensors and actuators have been demonstrated. Typical conditions required for PLZT thin film growth (600°C, 200mtorr O_2) prohibit direct integration with Al-metallized Si or polymer substrates and drastically limit direct integration with bare Si or metal substrates. We have recently shown successful transfer of epitaxial PLZT thin films from their UV transparent MgO growth substrate to a variety of receptor substrates including; stainless steel, Si, and polymer. The PLZT films, while on their growth substrate, are bonded to a receptor substrate and then are subsequently separated from their growth substrate by application of a single excimer laser pulse though the backside of the growth substrate. We have found that the laser induced acoustic shock wave greatly affects both crack creation in the film and success of substrate removal. To mitigate the effect of the acoustic wave, the PLZT film is first bonded to UV transparent fused silica with SU8 photopolymer and then separated from the MgO growth substrate by irradiation through the backside of the MgO. The PLZT film is then bonded to a receptor substrate of choice and is subsequently released from the quartz by irradiation of the SU8 through the backside of the fused silica substrate. By choosing a temporary bond for the PLZT/receptor interface, the PLZT/SU8 can be released to produce a unimorph. In this talk the materials and processing issues involved in fabricating free standing PLZT/polymer unimorphs and other MEMS devices will be discussed. Other topics to be discussed include characterization of PLZT/polymer composites, patterned PLZT/polymer composites, effect of bonding uniformity and laser fluence, and future directions and applications of excimer laser liftoff for heterogeneous integration of epitaxial PLZT with polymers.