SYMPOSIUM H

Flexible Electronics–Materials and Device Technology

April 22 – 25, 2003

Chairs

Babu R. Chalamala
Research & Development Inst
MCNC
Res Triangle Park, NC 27709-2889
919-248-1417

Norbert Fruehauf
Inst for Network & Systems Theory
Univ of Stuttgart
Stuttart, 70569 GERMANY
49-685-6922

Bruce E. Gnade
Dept of Materials Science
Univ of North Texas
Science Research Building
Denton, TX 76203
940-565-3333

Jin Jang
Kyunghee Univ
1 Hoegi-dong
Seoul, 130-701 SOUTH KOREA
82-2-961-0270

Symposium Support
DARPA Microsystems Technology Office

Proceedings to be published in both book form and online
(see *ONLINE PUBLICATIONS* at www.mrs.org)
as Volume 769
of the Materials Research Society
Symposium Proceedings Series

* Invited paper

SESSION H1: FLEXIBLE ELECTRONICS
Chair: Babu R. Chalamala
Tuesday Morning, April 22, 2003
Salon 14/15 (Marriott)

8:30 AM *H1.1
THE ALLURE OF "FLEXIBLE". Dalen E. Keys, DuPont Displays, Research Triangle Park, NC.

Our desires as consumers are driving technologies to enable the integration of more features with lower cost with increased performance. The are tremendous revolutions in technologies occurring. It appears that flexible is going to become an increassingly significant factor in our lives. Why now? Flexible electronics and devices are already having an impact on the design of smaller devices. We might be surprised at the impact these devices are having on our lives today. Can we build from our current knowledge base to meet the demands that we are placing on the marketplace for state-of-the-art devices that are flexible? There are significant efforts underway to create transitor arrays on flexible substrates. Exciting concepts for roll-up or conformed displays are being pursued. And, if printing of flexible electronic and displays can be implemented, new vistas can be achieved in manufacturing and hence the cost of the component and device. In the OLED displays world, we have pursued a model to support our exploration of technologies and their shortcomings in a roll-to-roll manufacturing process. There are many technology challenges remaining in the flexible electronics and display world. The most significant of these will be discussed. Why is flexible so important? Why do we want it so much? Let's explore the need again and then speculate on what is to come for "flexible."

9:00 AM *H1.2
LIGHT EMITTING POLYMER MATERIALS: THE WORKING BASE FOR FLEXIBLE FULL COLOR DISPLAYS. Heinrich Becker, Esther Breuning, Arne Büsing, Aurelie Falcou, Susanne Heun, Amir Parham, Hubert Spreitzer, Jürgen Steiger, Philipp Stössel, Covion Organic Semiconductors GmbH; Frankfurt am Main; GERMANY.

In the last few years, industrial research into materials fulfilling the needs of the maturing OLED display industry has intensified considerably. A first generation of polymers (phenyl–PPVs) is now being commercially exploited in first monochrome polymer LED display applications. Based on these materials, non-planar displays have already been demonstrated. However, those proof of concept devices have been monochrome. Especially the RGB materials need considerable improvement to be suitable for flexible full color displays. We will therefore report on the progress in the development of polymers for red, green, and blue emission. Our main focus here is on improving the properties of various polymers derived from the spiro-bifluorene core. Depending on the color, the main issues vary strongly: For BLUE polymers, efficiency, color coordinates, and processibility are already at a commercial level while operational lifetime still needs strong improvement. RED materials are in an almost contrary situation: here, the operational lifetime is excellent, whereas the efficiency and the driving current are requiring further improvement. For GREEN, achieving saturated emission, whilst maintaining the other properties (high efficiency, long operational lifetime), is still challenging. We will demonstrate the current status of material development within Covion. In addition, we will report on advances in full-color patterning, especially techniques based on Ink-Jet printing. This technology potentially allows the efficient manufacturing of high resolution RGB devices on a variety of substrates, including flexible layers.

9:30 AM *H1.3
LARGE AREA, FLEXIBLE MACROELECTRONICS. Robert Reuss, Defense Advanced Research Projects Agency, Microsystems Technology Office, Arlington, VA.

Based on the success of amorphous silicon TFTs in both solar cells and AMLCDs, and with the imminent penetration of OLEDs into display applications, macroelectronics has now become a standalone field of electronics research. The emphasis in this paper will be on materials and material related issues in the development of large area and/or flexible electronics. Emphasis will be placed on areas that are important for the successful implementation of electronics whose utility stems not from small dimensions, but from other physical attributes such as form factor and cost. Materials of interest include both Si based and organic FET technologies. While displays are perhaps the best-known example of applications for such materials, the focus will be on other potential applications such as smart cards, RF tags, and sensor array networks. Successful implementation of such systems will require innovations at the material, device, circuit, and architecture levels. The potential of flexible electronics ranges from lightweight, rugged, and bendable electronics to the ultimate in low-cost manufacturing through roll-to-roll fabrication. This paper will assess the state of the art with regard to achievement of the goals of flexible electronics for specific systems that offer novel operational capabilities. At the extreme, one can envision a future where macroelectronics plays a major role in the electronic systems landscape. While the disparity in performance between existing (and future) Si technology would seem to make this unlikely, the extreme cost pressure being experienced by the worldwide IC industry at least raises the question of alternative approaches. If TFT device performance can improve significantly at the same time the promise of low cost manufacturing can be realized, then perhaps "macroelectronics" can find a role beyond displays.

10:30 AM *H1.4
MATERIALS FOR FLEXIBLE PLED DISPLAYS. G. Nisato, Philips Electronics, Eindhoven, THE NETHERLANDS; Y. Leterrier, Ecole Polytechnique Federale de Lausanne, Lausanne, SWITZERLAND.

Flexible, free shape displays are the enabling technology for new robust, lightweight, extremely thin, portable electronic devices (e.g. portable audio players). Polymer Light Emitting Diodes (PLED) are especially suited for these applications, due to their fast response time, low voltage, high luminous efficiency and viewing angle performance. On the other hand, PLED displays are extremely sensitive to moisture and oxygen. Substrate materials provided with high performance hermetic and conducting layers are therefore an essential component for manufacturing these flexible devices. Polymer based substrates provide the necessary mechanical flexibility; they also require several thin, brittle, functional inorganic layers such diffusion barriers and transparent electrodes. The structural integrity, dimensional stability and thermal properties of the substrate stack are crucial to insure processability, device functionality and reliability. The mechanical properties of the thin functional layers, such as the transparent electrodes, limit the bending radii achievable for a given substrate and, ultimately, of the display. The fracture mechanics of diffusion barrier and conducting layers is therefore of particular importance and is studied by a combination of mechanical, optical and electrical measurements. Effective permeation rates of the diffusion barriers are measured using an optical method based on the oxidation of thin calcium layers; this calcium test also allows a direct visualization of barrier defects such as cracks and pinholes. These tools are applied to characterize and improve the performance of new high performance substrate materials based on transparent polymers withstanding temperatures above 300C which are suitable for flexible PLED displays.

11:00 AM *H1.5
THIN-FILM SILICON DEVICES ON FLEXIBLE AND DEFORMABLE SUBSTRATES. Sigurd Wagner, Helena Gleskova, James C. Sturm, Princeton Univ, Dept of Electrical Engineering and POEM, Princeton, NJ; Zhigang Suo, Princeton Univ, Dept of Mechanical and Aerospace Engineering, Princeton, NJ.

Amorphous and microcrystalline silicon thin-film transistors, which dominate active matrices and thin-film solar panels, are now being made on flexible and deformable substrates. While flexible solar panels on steel and plastic have been made for some time, flexible TFT arrays are more recent, and deformable circuits are altogether new. Flexible and deformable electronics could enable conformal displays and detector arrays, shrink-wrap sensor skin, electro-mechanical actuator and tactile arrays, e-textiles, and shaped solar panels. Amorphous silicon transistors and solar cells respond to increasing mechanical strain in three steps: (1) Elastic deformation causes small, reversible changes in electrical performance; (2) The most brittle device material fractures close to its failure strain; the device becomes unstable but may remain functional. (3) Even larger strain causes definitive fracture and thus electrical failure. The devices fail more easily in tensile than compressive strain because of different mechanisms for crack formation. Thin-film transistors, which rely on in-plane carrier transport, appear to be more sensitive to deformation than solar cells, which function by top-to-bottom transport. We will discuss research issues in high-performance transistors for plastic substrates; 3-D shaped electronic surfaces; electronic fibers; and elastic circuits.

11:30 AM *H1.6
CRITICAL PROCESS ISSUES IN ROLL-TO-ROLL MANUFACTURING OF MICROELECTRONIC DEVICES. James R. Sheats, Rolltronics Corp., Menlo Park, CA.

There is a great deal of interest currently in a variety of technologies related to the production of flexible electronic devices, which have advantages for the user of light weight, compactness, and convenience; in principle devices that are currently powerful but rather cumbersome to use could be much more like familiar "information appliances" such as paper. Fabricating electronics on plastic, however, is likely to be more expensive than the market will bear unless roll-to-roll substrate handling systems are used, and these in turn pose challenges for microelectronic processing: dimensional control,

defects, thermal and mechanical characteristics are all new territory compared to familiar silicon and glass substrates. I will explore some of these issues from the perspective of what is currently practiced in commercial web processing and how this knowledge can be brought to bear on microelectronics.

SESSION H2: FLEXIBLE Si TFTs
Chair: Jin Jang
Tuesday Afternoon, April 22, 2003
Salon 14/15 (Marriott)

1:30 PM *H2.1
LOW TEMPERATURE POLY-Si ON FLEXIBLE POLYMER SUBSTRATES FOR ACTIVE MATRIX DISPLAYS AND OTHER APPLICATIONS. Nigel Young, Michael Trainor, Soo-Young Yoon, David McCulloch, Richard Wilks, Andy Pearson, Peter Green, Philips Research, Redhill, UNITED KINGDOM; Sander Roosendaal, Philips Research, Eindhoven, THE NETHERLANDS; and Elizabeth Hallworth, Philips Research, Redhill, UNITED KINGDOM.

For a number of years we have been developing LTPS technology on a range of polymer substrates for active-matrix LCD and LED displays and other applications. Our current vehicle for this technology is a 2.1 220x(176x3) transflective mobile phone display with integrated CMOS drivers, and this will be discussed in detail. Important issues include the choice of substrate material, the film deposition method, the processing temperature, and device hydrogenation. Our substrate studies have included PES (Sumitomo Bakelite), PI (UBE and Dupont), FPE (Ferrania) and PNB (Promerus) and particular consideration has been given to shrinkage, alignment, adhesion and laser crystallisation issues. The relative merits of TFTs formed on these substrates using either a simple gate-overlapped structure, or a self-aligned structure will be demonstrated. In this work, particular attention has been given to the choice of gate insulator (silicon dioxide or silicon nitride) and the method of deposition. Over and above the basic TFT properties, the dielectric defect density and its dependence on the deposition temperature has to be considered. Several other layers are required above the TFT in order to make a complete AMLCD. We will show that polymer dielectrics are suitable for the formation of cross-over dielectrics, in-cell scatterers, and the cell spacers required to make a transfllective display.

2:00 PM H2.2
LOW TEMPERATURE a-Si:H PIXEL CIRCUITS FOR MECHANICALLY FLEXIBLE AMOLED DISPLAYS.
Arokia Nathan, Kapil Sakariya, Anil Kumar, Peyman Servati, Karim S. Karim, and Denis Striakhilev, Univ of Waterloo, Dept of Electrical and Computer Engineering, Waterloo, ON, CANADA.

In this paper, we present amorphous silicon (a-Si:H) thin film transistor circuits fabricated at low (~100°C) temperature that compensate for material shortcomings such as metastable threshold voltage (Vt) shift and low mobility, and supply stable and predictable currents to drive mechanically flexible active matrix organic light emitting diode (AMOLED) displays. We use a vertically stacked pixel architecture that enables high aperture ratio and high on-pixel integration with low parasitic capacitance and leakage current. The simplest pixel driver circuit possible is the two TFT voltage-programmed circuit. Since the current through the OLED depends on the gate voltage of the drive TFT, this circuit is very susceptible to any Vt increase in the TFT. Due to this, the OLED brightness with the 2-TFT pixel circuit will gradually decrease and the pixel will eventually turn off. To overcome this problem, we have developed current-programmed pixel circuits based on the current mirror circuit family. The OLED current in these circuits is virtually independent of any threshold voltage or mobility variation in the drive TFT. We examine the effects of Vt-mismatch in the current mirror TFTs on the stability of the output drive current. Results show that the circuits provide higher linearity and dynamic range than currently available pixel circuits while minimizing the pixel area. Charge injection effects at the gate of the drive TFT have been reduced by using smaller switching TFTs with circuit topologies that provide in-pixel current gain. All circuits meet the speed requirements of a QVGA 60 Hz refresh rate display, and occupy less than 300um x 300um area.

2:15 PM H2.3
ULTRA-LOW TEMPERATURE POLY-Si THIN FILM BY EXCIMER LASER RECRYSTALLIZATION FOR FLEXIBLE SUBSTRATES. Sang-Myeon Han, Min-Cheol Lee, Kook-Chul Moon and Min-Koo Han.

TFTs on flexible substrate has attracted for flat panel display application. However, process temperature of TFT fabrication on flexible substrate should be less 200°C. The purpose of our work is to report a ultra-low temperature (150°C) poly-Si (ULTPS) active layer for TFTs on flexible substrate. It has been reported that a-Si film deposited by plasma enhanced chemical vapor deposition (PECVD) at 200°C has a large hydrogen content (~10%) which requires a troublesome dehydrogen process. We developed a low hydrogenated (less than 3%) μc-Si film utilizing inductively coupled plasma chemical vapor deposition (ICP-CVD) at substrate tempertature of 150°C. It is well known that μc-crystal silicon is obtained in the condition of high plasma power density and high H_2 /SiH_4 flow ratio. ICP-CVD has rather high plasma density so that a density of μc-Si film increases and hydrogen content decreases. The μc-Si film was crystallized by XeCl (308nm) excimer laser annealing (ELA) and no ablation of crystallized film was obtained. FTIR mesurement exhibited that the hydrogen content was decreased as the laser beam was irradiated. Our experimetal result shows that μc-Si film deposited by ICP-CVD maybe suitable for active layer of TFTs on flexible substrate.

2:30 PM H2.4
THIN FILM TRANSISTORS ON PLASTIC SUBSTRATES USING SILICON DEPOSITED BY MICROWAVE ECR PLASMA CVD.
Lihong Teng and Wayne A. Anderson, University at Buffalo, The State University of New York, Dept of Electrical Engineering, Buffalo, NY.

Thin film silicon transistors fabricated on plastic substrates at low temperatures are promising candidates for low-cost, large-area, unbreakable, lightweight and flexible flat panel displays. High-quality channel materials with fewer defects are important to realize TFT's with good performance, such as high mobility and low leakage current. We fabricated bottom-gated TFT's on polyimide foil at below 200°C with active channel layers deposited by microwave plasma electron cyclotron resonance chemical vapor deposition (MECR-CVD). The ECR condition enables the electrons to effectively absorb the microwave energy and, thus, a high-density plasma ($>10^{11}$ cm^{-3}) at a low temperature and low gas pressure is produced, which enhances the generation efficiency of SiH_3 radicals and is favorable to the formation of a better quality Si film. Hydrogen was introduced during the Si film deposition. The as-deposited Si film showed a high photoconductivity of 5×10^{-5} S/cm. The TFT fabrication processes that are compatible with the plastic substrates were optimized. The gate oxide quality was examined by the high frequency C-V characteristics of the MOS capacitors. The high frequency C-V curves showed small flat-band voltage (<1V) and stretch-out, which implied high-quality oxide with little fixed charge and small Si/SiO_2 interface trap density. The MOS capacitor J-E curve showed a high oxide breakdown field of 9 MV/cm. The TFT on polyimide foil with an active Si layer deposited at 190°C and 8 mTorr hydrogen had a field effect mobility of 3.9 cm^2/V-s, a threshold voltage of 4.1 V, a subthreshold swing of 0.73 V/decade and an ON/OFF current ratio of 5.1×10^6. The role of the incorporated hydrogen during the silicon film formation and the TFT fabrication will be discussed. The TFT transfer curves (I_D vs V_G) at different hydrogen pressures and substrate temperatures (150-200°C) will be presented and discussed. This process produces TFT's on plastic which are as good as those produced on SiO_2/Si under the same conditions.

2:45 PM H2.5
HIGH PERFORMANCE POLYSILICON THIN FILM TRANSISTOR CIRCUITS ON FLEXIBLE STAINLESS STEEL FOILS.
Themis Afentakis and Miltiadis K. Hatalis, Display Research Laboratory, Department of Electrical & Computer Engineering, Lehigh University, Bethlehem, PA; Apostolos T. Voutsas and John W.Hartzell, Sharp Labs of America Camas, WA.

In recent years, there has been an increased interest in the use of flexible substrates in microelectronic fabrication. Flexible substrates, such as polymers and metals have the potential to be utilized in roll-to-roll processing, resulting in low cost, rugged systems. Thin flexible stainless steel foils offer a number of advantages over polymers for device and circuit fabrication, most significantly in the increased thermal budget tolerance that they provide. This enables the utilization of high temperature processes in fabrication and the production of high performance devices and circuits. Thin film transistors have been fabricated on thin stainless steel foils using a variety of crystallization and gate dielectric approaches. N-channel devices with average mobility values of 250cm^2/Vs and p-channel devices with mobilities in the region of 90cm^2/Vs were successfully fabricated. Both digital and analog circuits, such as operational amplifiers, digital-to-analog converters, ring oscillators and a variety of shift register designs were also fabricated, and their basic performance characteristics will be presented in this paper. The characteristics of ring oscillators having 19 inverter stages operating with speeds of 10MHz or higher, along with the characteristics of shift registers, digital to analog converters and operational amplifiers will be reported. The impact of process and design parameters on their operation was evaluated and will be addressed in this paper. The results that are presented in this paper constitute the first successful

implementation of high performance circuitry having a high degree of scalability and complexity on thin metal foils, thus making the fabrication of efficient, inexpensive and versatile systems on flexible foils for a large variety of applications a realistic prospect.

3:30 PM *H2.6
LOW-TEMPERATURE POLYCRYSTALLINE-SILICON THIN FILM TRANSISTORS TRANSFERRED ON PLASTIC SUBSTRATES FOR FLEXIBLE DISPLAYS. Akihiko Asano, Mobile Display Division, Core Technology & Network Company, Sony Corporation, Atsugi, JAPAN.

A new technique has been developed which realizes a low-temperature polycrystalline silicon (LTPS) thin film transistor (TFT) arrays and CMOS circuits on plastic substrates. In the newly developed transfer process, a several-micron-thick device layer which was prepared on a 350mm x 300mm size glass substrate can be transferred onto a plastic substrate without any significant damage to the device layer. As an example, an all-plastic, full-color LTPS TFT LCD has been fabricated with practical image quality. This technology will lead to astonishingly lightweight, thin, and shock-resistant, or flexible displays which are suitable to mobile applications.

4:00 PM H2.7
FLEXIBLE MONOCRYSTALLINE Si FILMS FOR THIN FILM DEVICES FROM TRANSFER PROCESSES. Christopher Berge, Thomas A. Wagner, Markus B. Schubert, Juergen H. Werner, Institute of Physical Electronics, University of Stuttgart, GERMANY.

Transfer of monocrystalline silicon films to nearly arbitrary foreign substrates has proven to be a promising alternative to the direct deposition of thin silicon films on foreign substrates. Transfer technologies combine the high electronic quality of monocrystalline material with the advantages of thin films. Our transfer approach using *quasi-monocrystalline silicon (QMS)* is based on the formation of a separation layer on a host wafer with a monocrystalline Si film deposited on top. All high temperature device processes are performed while the monocrystalline film is still attached to the host wafer. Only at the end of the process, the monocrystalline films or devices are detached from the host wafer and transferred to a foreign substrate. Thus, thermal oxidation and diffusion at high temperatures as well as lithography, wet chemical or plasma chemical processes are carried out as in conventional technology. Typical light-point defect densities of silicon films transferred from virgin host wafers range from 10 to 100 cm^{-2}, while stacking fault and dislocation densities obtained from Secco etching are $\leq$ 100 cm^{-2}. The charge carrier diffusion length in the films is around 50 μm, thus allowing for the fabrication of CMOS and standard bipolar devices. Solar cells manufactured on thin silicon films obtained from our QMS process and transferred to glass substrates demonstrate record efficiencies up to 16.6 %. We will present systematic investigations on the formation and characterization of the separation layer which is essential for the successful transfer of the epitaxial layer. The transfer of films up to 150 mm in diameter as well as the transfer of processed electronic devices to flexible substrates will be discussed.

4:15 PM H2.8
CURVED SILICON ELECTRONICS. Linlin Wang, Dieter G.Ast, Cornell Univ, Dept of Materials Science and Engineering, Ithaca, NY.

An electronic imaging system using a curved sensing array can use a faster lens, and cover a greater field of view, than that using a planar array. The simpler lens systems also weight less, a decisive advantage in portable applications. We investigated a method to fabricate a curved silicon substrate from a flat silicon wafer containing appropriate circuits in close spaced 1cm by 1cm tiles. The tiles are separated by 0.5mm gaps, which are bridged, in turn, by a dense array of $45x100\mu$m gold leads formed by electroplating using lithographically defined leads as seeds. To curve the substrate, it is diced, via dry etching from the backside, into 1cm by 1cm tiles, removing the inter-tile silicon but leaving the connecting leads in place. Two methods were used to curve the wafer. In the first one, the wafer was bonded with epoxy to a PMMA disk, and then curved by heating the sandwich, under a load of ~230gr, for 1.5 hours at 130°C in a concave metal mold with a radius of curvature of 7.8cm. In the second method, the wafer was put into a curved metal mold, radius 14cm, loaded with 230gr, and heated to 290°C for 2 hours. The normal and shear strains accommodated by the flexible interconnects were measured and compared with theoretical models.

4:30 PM *H2.9
200 dpi a-Si:H TFT ACTIVE-MATRIX ORGANIC POLYMER LIGHT-EMITTING DISPLAYS. Jerzy Kanicki and Yongtaek Hong, University of Michigan, Dept of Electrical Engineering and Computer Science, Ann Arbor, MI.

Today, active-matrix organic light-emitting displays are being considered for mobile flat panel display applications, where the poly-silicon thin-film transistor technology is dominant since it has an advantage of driver circuitry integration. However, for larger size and high-resolution display applications, hydrogenated amorphous silicon thin-film transistor (a-Si:H TFT) technology looks more competitive in terms of uniformity of TFT performance over large area and manufacturing cost (high manufacturing yield leads to low cost). Therefore, in our laboratory, we have focused our research on active-matrix (AM) pixel electrode circuits design based on three- and four-a-Si:H TFTs, combining with organic polymer light-emitting devices (PLEDs), during the last several years. Most recently, we have successfully fabricated voltage-driving 200 dpi AM-PLED based on three a-Si:H TFT structure. For this specific AM-PLED, we obtained up to $2x10^{-2}$ lumen at V_{data} = 30 V for our green light-emitting PLED. The estimated display luminance was about 120 cd/m^2. In this paper, we will focus our attention on current-driving 200 dpi AM-PLED based on four-a-Si:H TFTs, which can compensate for the threshold voltage shift of PLEDs and a-Si:H TFTs. The PLED lifetime and power consumption issues associated with the aperture ratio of AM-PLED will also be addressed during this presentation. Our preliminary study of our PLED opto-electrical characteristics indicates that higher brightness and less power are needed for certain PLEDs as the aperture ratio of AM-PLED decreases. However, since the PLED lifetime is also closely related to the display brightness and the power consumption of the device, more research is needed to find the optimum design conditions for long-lasting and low-power consuming AM-PLEDs. This work is being supported by NIH grant.

SESSION H3: ORGANIC ELECTRONICS - OFETs
Chair: Norbert Fruehauf
Wednesday Morning, April 23, 2003
Salon 14/15 (Marriott)

8:30 AM *H3.1
ORGANIC ELECTRONICS FOR LARGE AREA ELECTRONIC DEVICES. Marc Chason, Motorola, Inc., Motorola Labs, Schaumburg, IL.

With market opportunities continuing to drive electronic products to smaller size, significant research efforts continue to shrink semiconductor devices in accordance with Moore's Law. However, a new set of market opportunities is emerging for which the significant driver is not semiconductor complexity, but rather lower product cost arising from the novel integration of technologies making use of organic and flexible substrates. These new technologies present opportunities for research into new materials and fabrication processes. These new research opportunities extend from organic MEMS, microfluidics, and embedded passive devices to printed organic transistors and polymeric optical waveguides. This talk will discuss these new technologies and present some of the market forces driving these efforts.

9:00 AM H3.2
ALL-ORGANIC FIELD EFFECT TRANSISTORS. R. Parashkov, E. Becker, H.H. Johannes, D. Schneider, G. Ginev, D. Metzdorf, T. Dobbertin, and W. Kowalsky, Institut für Hochfrequenztechnik, Technische Universitaet Braunschweig, Braunschweig, GERMANY.

In this work we present fully patterned organic transistors based on selective electropolymerization of conducting polymers that enables simple fabrication of micron scale features. It involves fabrication of pentacene field effect transistors in which the conducting, insulating parts as well as the substrate are all made of polymers. We have fabricated drain and source electrodes by electropolymerization of 3,4-ethylenedioxythiophene and gate by spin coating of commercially available poly(3,4- ethylenedioxythiophene) (PEDOT:PSS) aqueous dispersion, polyvinylalcohol for the gate dielectric layer, and pentacene for the organic active layer. We have built a top-gate structure with gate dielectric layer and gate placed on the top of the pentacene layer, and in a such way obtained protection of the active layer could permit enhancement of the operating time of devices. Carrier mobility as large as 0,01 cm^2/Vs was measured. Functional all- organic transistors have been realised using a simple and potentially inexpensive technology.

9:15 AM H3.3
ALL PRINTED ELECTROCHEMICALLY TUNABLE RECTIFIERS AND AMBIPOLAR TRANSISTORS ON FLEXIBLE SUBSTRATES. Miaoxiang Chen, Magnus Berggren, Tommi Remonen, Thomas Kugler, Mats Robertsson, Dept of Science and Technology, Linköping University, SWEDEN.

The present paper reports on all-organic electrochemical rectifiers with tunable threshold voltage function and electrochemical ambipolar transistors fabricated by printing technique on flexible plastic films.

Solution based conducting polymer poly(3,4-ethylenedioxythiophene) poly(styrene sulfonate) (PEDOT:PSS) used here as active material, were spin-coated on flexible polyester substrates, baked for forming a solid thin film layer, and then patterned by means of plotter. Gelled electrolyte structures were realized across the top of PEDOT:PSS channel and gate regions by screen-printing technique. The electrolyte layers were finally encapsulated with a waterproof coating, such as plastic paint or foil. Both rectifiers and transistors had a lateral device configuration with a feature size about 400 mm. The areas where PEDOT:PSS film both in the channel and gate regions interface with electrolyte form an electrochemical cell. Upon external bias beyond the oxidation and reduction potentials, electrochemistry, that is reduction (dedoped) and oxidation (doped) process, takes place in the electrochemical cells. Thus a reversible switching function can be realized at the channel regions. In one single tunable rectifier the threshold voltage can be tuned from 0 V to 0.8 V. Both tunable rectifiers and ambipolar transistors exhibit on/off current ratio of 5000 at low voltage biasing. In an electrochemical transistors, ambipolar transistor operation, i.e. having both n- and p-channel functions, has been realized. The both n- and p-channel functions transistors have threshold voltage near to 0 V at gate voltage and drain-source voltage below ± 3 V. Furthermore, the ambipolar transistors have open circuit memory function. The tunable rectifiers can be further constituted multi-channel switch that is suitable for large area display application.

9:30 AM *H3.4
DISPLAY, MEMORY, AND SENSOR APPLICATIONS OF ORGANIC TRANSISTORS. H.E. Katz, M. Mushrush, M. Lefenfeld, T. Someya, A. Gelperin, Bell Laboratories-Lucent Technologies; A. Facchetti, T.J. Marks, Northwestern University, Evanston, IL.

Organic-based transistors are now routinely prepared with semiconductor mobilities of 0.1 cm2/Vs and on/off ratios above ten thousand. While these values approach the requirements for certain amorphous silicon-type devices, such as the transistors used to control electrophoretic display pixels, they are well below the performance levels exhibited by crystalline silicon. Rather than competing directly with silicon, newer applications of organic-based electronics focus instead on capabilities unique to organic materials, such as low-temperature and large-area fabrication, chemically tunable energy levels, charge storage, and chemical sensitivity. This talk will focus on the molecular design of organic semiconductors aimed specifically at plastic displays, nonvolatile memory elements, and vapor sensor arrays. Proof of concept and future research opportunities for each application will be discussed. Methods for all-printed fabrication processes and highly flexible substrates will be emphasized.

10:30 AM *H3.5
ORGANIC THIN-FILM TRANSISTORS FABRICATED ON FLEXIBLE SUBSTRATE FOR ALL-ORGANIC ELECTRONIC DEVICE. Seong Hyun Kim, Taehyoung Zyung, Basic Research Lab., ETRI, Daejon, KOREA.

In the organic thin-film transistors (OTFTs) study, the formation of good gate dielectrics is one of the most important processes when being fabricated on plastic substrates. We investigated the electrical porperties of the OTFTs fabricated on plastic substrates such as polyethylene naphthalate (PEN) film. We varied the dielectric materials such as organic and inorganic materials including polyvinyl alcohol (PVA), acrylate, Al_2O_3, and ferroelectric PZT. In the electrical measurements, the flexible field effect transistor (FET) devics showed the typical I-V chracteristics. The field effect mobility μ of our flexible OTFT to be greater than 1.4×10^{-1} $cm^2V^{-1}s^{-1}$. Several properties of OTFT on the plastic substrates will also be discussed.

11:00 AM H3.6
INTEGRATED MICROFLUIDICS FOR THE FABRICATION OF ARRAYS OF POLYMERIC THIN FILM TRANSISTORS. Michael L. Chabinyc, William S. Wong, Kateri E. Paul, Robert A. Street, Palo Alto Research Center, Electronic Materials Lab, Palo Alto, CA.

Organic semiconductors are an attractive transistor technology for inexpensive displays because of their low processing cost and their potentially superior mechanical properties for applications in flexible electronics. A key issue in the development of organic electronics is to devise simple, reliable and low-cost patterning techniques. We are developing a variety of non-lithographic methods to fabricate polymeric thin film transistors (TFTs). We will describe a novel method to integrate a network of microfluidic channels with an array of electrodes. These microfluidic channels are used to pattern solution-processible organic semiconductors over the electrode array to create TFTs suitable for active matrix addressing of display media. We have fabricated prototype arrays containing 64 x 64 pixels with an edge-dimension of 300 μm using microfluidic patterning. The technique has been demonstrated with regio-regular polythiophenes and co-polymers of thiophene and fluorine. The performance of the TFTs will be presented and compared to other deposition approaches.

11:15 AM H3.7
AMOLED TFT PIXEL CIRCUITRY FOR FLEXIBLE DISPLAYS ON METAL FOILS. Matias Troccoli, Themis Afentakis, Miltiadis K. Hatalis, Display Research Laboratory, Department of Electrical and Computer Engineering, Lehigh University, Bethlehem, PA; Apostolos T. Voutsas, Masahiro Adachi, John W. Hartzell, Sharp Laboratories of America, Camas, WA.

Active matrix organic light emitting diode displays based on thin, flexible metal foil substrates offer a novel approach to fabricate light, flexible and rugged displays. The higher thermal budget tolerance of metal foils allows devices to be fabricated at higher process temperatures yielding better device characteristics than glass or plastic substrates for superior display performance. Furthermore, the conductive nature of metal foil substrates compared to insulating substrates like glass or plastic, enables more efficient use of pixel area through the use of the conductive substrate as a global power electrode. We are implementing Active Matrix Organic Light Emitting Diode (AMOLED) displays on flexible stainless steel substrate using two different pixel circuit topologies and two different layout realizations. We will report on AMOLED array characteristics having either 2-TFT or 4-TFT pixel circuitry architectures. In the most simple scheme, a 2-TFT pixel circuitry utilizes two p-type transistors to establish the OLED driving current. This circuit is realized with two different pixel layouts. The more traditional layout uses separate data lines, address lines and power supply lines. When using metal foil substrates such as stainless steel, we can exploit the high conductivity of the substrate to eliminate the need for power supply lines. Power is brought in to each pixel through contact holes to the metal substrate. Due to the potential variation in TFT performance across a large area array, it is necessary to compensate for changes in threshold voltage or mobility. The 4-TFT circuit compensates for such changes in order to achieve higher intensity uniformity throughout the display. This circuit topology utilizes two n-type and two p-type devices. It behaves like a current copy circuit, that replicates the reference current in the data line through the OLED. As with the previous circuit, we are implementing two different pixel layouts. One with a power supply line, and a second one with contacts to the conductive substrate.

11:30 AM H3.8
LARGE AREA PLASTIC CIRCUITS FORMED BY THERMAL TRANSFER PRINTING. Michael Lefenfeld, John A. Rogers, Bell Laboratories-Lucent Technologies, Nanotechnology Division, Murray Hill, NJ; Graciela Blanchet, DuPont, Central Research & Development, Willmington, DE.

Organic materials and polymers have shown the ability to play vital roles in robust, bendable transistors that can be printed over large areas at very low cost. These features are difficult to achieve with conventional electronic systems, which use brittle inorganic materials and high cost processing tools. In this talk, we describe an additive printing method that is capable of patterning, with micron resolution, all conducting layers of polymer circuits. The approach uses a laser transfer method to pattern, in a sequential fashion, the gate and then the source/drain electrodes over areas of up to 6 square feet. The electrical characteristics of such organic devices depend on many variables, such as the intrinsic characteristics of the semiconductor, the dimensions of the electrodes, the dielectric thickness, and the various chemical and physical interactions that can occur between these elements. With printed polyaniline (PANI) source/drain electrodes doped with single wall carbon nanotubes, ohmic contacts with small resistances can be formed with a wide range of organic semiconductors, including pentacene, FCuPc, a-6T, a-4T. This property is important because it shows that these printed, bottom contact devices can avoid the strong contact effects that often limit the performance of organic transistors when operated in the linear regime. High mobilities of up to 0.3-0.5 square centimeters per volt second were achieved in these printed devices.

11:45 AM H3.9
FLEXIBLE ORGANIC FIELD-EFFECT TRANSISTORS FABRICATED BY THE ELECTRODE-PEELING TRANSFER. Takeshi Yasuda, Katsuhiko Fujita and Tetsuo Tsutsui, Department of Applied Science for Electronics and Materials, Graduate School of Engineering Sciences, Kyushu University, Kasuga, Fukuoka, JAPAN.

Much progress has been shown in the research and development in organic and polymeric field-effect transistors in recent years. They are potentially low-cost, lightweight and mechanically flexible devices, compared with the conventional silicon-based transistors. Especially, polymeric dielectric layer and plastic substrates have significant advantages over conventional glass or silicon substrates, to realize a flexible device. However, when such flexible materials are used for organic electronic devices, one problem arises, e.g. it is difficult to

pattern the detailed metal electrodes by employing a conventional photolithography and etching process to the flexible substrate including organic semiconductors or polymeric dielectric layers. In the present study, we propose a novel way to fabricate a flexible organic field-effect transistor using electrode-peeling transfer method. Firstly, fine patterns of source-drain metal electrodes were formed on a solid substrate, where a micro-patterning process such as photolithography is applicable. An organic dielectric layer (poly-chloro-para-xylylene) was deposited by a chemical vapor deposition. Then patterned gate electrode was deposited using a shadow mask. On the top surface of the gate electrode, another adhesive flexible substrate was fixed and the stack of the flexible substrate/ gate electrode/ dielectric layer/ source-drain electrode was peeled away from the solid substrate. The peeling-transfer was completed with a help of a self-assembled monolayer (n-decyl mercaptan) as a connecting buffer layer between the gold electrodes and the dielectric layer. Then an organic semiconductor material was deposited on the fresh peeled-off surface on the flexible substrate. In the present case, pentacene was used as the active semiconductor material. A good field-effect transistor characteristic was shown even after the substrate was bent.

SESSION H4: ORGANIC ELECTRONICS - OLEDs
Chair: Bruce E. Gnade
Wednesday Afternoon, April 23, 2003
Salon 14/15 (Marriott)

1:30 PM *H4.1
FLEXIBLE OLED DISPLAYS. Anna Chwang, Mark Rothman, Sokhanno Mao, Jeff Silvernail, Mike Weaver, Richard Hewitt, Kamala Rajan, Mike Hack, and Julie Brown, Universal Display Corporation, Ewing, NJ.

Organic light-emitting device (OLED) technology is rapidly gaining momentum as the technology of choice for future flat panel display applications where low power consumption, low cost, and superior viewing ability are desired. The flexibility of both polymeric and small molecule OLEDs further enables the use of these materials in flexible displays. OLED displays on flexible plastic substrates have been demonstrated; the principal limitation of OLED displays on plastic, however, is their lifetime. The materials currently used in OLEDs are very sensitive to moisture and oxygen, and plastic substrates are generally too highly permeable to both. We will describe recent advances in the packaging of our flexible OLED (FOLED^{TM}) displays, which are based on our highly efficient electrophosphorescent OLED (PHOLED^{TM}) technology. Various packaging approaches will be discussed along with their performance with respect to lifetime, flexibility, and manufacturability.

2:00 PM *H4.2
OLED MATRIX-DISPLAYS. W. Kowalsky, E. Becker, T. Dobbertin, H.-H. Johannes, D. Metzdorf, T. Riedl, Institut für Hochfrequenztechnik, Technische Universität Braunschweig, Braunschweig, GERMANY.

The field of organic light emitting diodes (OLEDs) has matured considerably within recent years and first products are commercially available. After a brief review on the improvement of individual OLEDs we will focus on research topics for the preparation of passive matrix (PMOLED), active matrix (AMOLED) and full color displays. Different PMOLED-Displays based on vacuum deposited organic compounds have been prepared by various fabrication techniques. We demonstrate a 2 inch organic display with 50×100 single pixels and 0.3×0,35 mm^2 pitch whereby cathode separation was achieved using photoresist barriers featuring a distinct undercut. In contrast to the widespread quasi-static evaporation in cluster-like deposition tools PMOLED-Displays originating from dynamic inline-process will be shown. The superior aspects of inline fabrication process concerning device characteristics such as cross-talk or contrast and fabrication parameters like material yield or throughput will be discussed. Due to the inherent limitations of multiplexing and in order to satisfy the need for large area, high resolution displays the basic concepts for an active matrix addressing scheme are dealt with. In this regard transparent and electrically inverted top-side emitting diodes will be demonstrated. The latter are advantageous for the incorporation of powerful n-channel thin film transistors in the AMOLED driver backplanes. An all-organic smart pixel device comprising a single Pentacene based organic field effect transistor (OFET) and a conventional OLED has successfully been prepared. Furthermore a new flash-sublimation technique for the spatial selective deposition of small organic molecules will be presented. We prepared OLEDs comprising flash-deposited Tris-(8-hydroxyquinoline)aluminium (Alq_3) and Alq_3 doped with DCM2 which demonstrate the suitability of this technique for the preparation of full-color displays based on small organic molecules.

2:30 PM H4.3
DEGRADATION IN A METHYL-PHENYL CO-POLYMERIC POLYSILANE FOR LED APPLICATIONS. A. Sharma, Deepak, M. Katiyar, Materials & Metallurgical Engg. & Samtel Centre for Display Technology, IIT Kanpur, INDIA; Satyendra Kumar, Dept. of Physics and Samtel Centre for Display Technology, IIT Kanpur, INDIA; V. Chandrasekhar, Dept. of Chemistry and Samtel Centre for Display Technology, IIT Kanpur, INDIA; A.K. Saxena, A. Ranjan R.K. Tiwari, DMSRDE, Kanpur, INDIA.

Whereas most of the focus on organic light emitting diodes (OLEDs) is focused on carbon based organics, we are exploring Si-Si chain polysilane polymers for light emission. The emission in carbon based oligomers is controlled by π-π^* bandgap, where this transition is used to produce visible light mostly in the higher wavelength region of the visible spectrum. In polysilanes, however, the emission is controlled by a larger σ-σ^* transition, which could potentially provide UV to blue emission. But, in spite of potential availability of emission in higher energy region, the issue of degradation of emission properties is much more serious in polysilanes because of σ-σ bonds. In order to understand this degradation, a new co-polymer based on methyl-phenyl silane and phenyl-phenyl silane was prepared by Wurtz condensation reaction of dichloromethyl phenylsilane and dichlorodiphenylsilane in appropriate ratio using a binary solvent system and phase transfer catalyst. Then the PL investigation was performed on spin cast films of thicknesses (measured by Spectroscopic Ellipsometry) varying between 20-100 nm. The degradation of luminescence from these films on various substrates, hydrophobic and hydrophilic surfaces (e.g. quartz and Si), is examined after excitation with light sources of several energies. The room temperature PL spectrum on these films shows a sharp emission at 365 nm when excited with a source of 325 nm. However, the PL intensity at 365 nm deteriorates exponentially with time. In addition, the peak of the PL spectra shows a red shift upon extended exposure to light. We have further examined the causes of this degradation by characterizing the material for its transmission behavior and changes occurring in it by GPC and NMR.

2:45 PM *H4.4
ORGANIC LIGHT EMITTING DIODES AND PHOTODETECTORS FABRICATED ON A POLYMERIC SUBSTRATE FOR FLEXIBLE OPTICAL INTEGRATED DEVICES. Yutaka Ohmori, Osaka Univ, Collaborative Research Center for Adv Sci Tech (CRCast), Osaka, JAPAN.

Organic light emitting diodes (OLED) and organic photo detectors (OPD) have been investigated for an optical integrated circuits. High-speed operation of the devices have been investigated and realized. OLEDs have been fabricated on an indium-tin oxide (ITO) coated polymeric substrate with silicon dioxide and silicone nitride buffer layers. The OLED consists of diamine derivative (α-NPD) layer as a hole-transporting layer, rubrene doped in 8-hydroxyquinoline aluminum (Alq_3) layer as an emissive layer, and Alq_3 layer as an electron-transporting layer terminated with silver containing magnesium cathode. The device emits yellow light centered at 560 nm, and the maximum emission intensity reaches as high as 50mW/cm^2. The optical pulse of more than 100 Mbps has been generated from the OLEDs, which are comparable to those of fabricated on a glass substrate. Using several emissive materials, such as α-NPD or porphin derivative, optical pulses as high as 100 Mbps have been generated. The OPDs, which consist of superlattice structure of titanyl phthalocyanine and fluorinated metal phthalocyanine as photo-absorbing layers, have been fabricated and investigated. As decreasing the individual layer thickness of the phthalocyanines, the response frequency increased to several Mbps under reverse bias conditions. Optical transmission experiments of moving picture signals have been performed utilizing the OLEDs. The details of the device characteristics have been discussed for both devices fabricated on a polymeric and a glass substrate, for comparison.

SESSION H5: LARGE AREA PRINTING AND DEPOSITION
Chair: Bruce E. Gnade
Wednesday Afternoon, April 23, 2003
Salon 14/15 (Marriott)

3:30 PM H5.1
LOW-TEMPERATURE PHOTOCHEMICAL DEPOSITION OF PATTERNED FILMS FOR FLEXIBLE ELECTRONICS. Michael A. Fury, Harold O. Madsen, Paul J. Roman Jr., Shyama P. Mukherjee, Seigi Suh, Leo G. Svendsen, EKC Technology, Inc., Hayward, CA.

The evolution of consumer electronics toward low-cost, low-power and even disposable devices creates new challenges for manufacturing on flexible, plastic substrates. Processing temperatures are often limited

to 300°C and below. Circuit patterning by plasma etch is constrained by cost objectives and compatibility with the substrate materials. The present work introduces an emerging method for the deposition of directly photopatterned metal oxide thin films from a metal-organic precursor. The method described, Photochemical Metal-Organic Deposition or PMOD, can be used in lieu of plasma etch to pattern device elements. Alternatively, PMOD can be used to deposit a patterned hard mask for high plasma etch selectivity to the substrate below. Our initial studies have focused on the patterning of TiO_2 as a model system for both hard mask applications and as a high-κ dielectric. Precursors chosen include a variety of hexanoate and acetylacetonate coordination complexes. In these studies, the precursors are deposited on silicon wafers by spin coating from a casting solvent. Patterns are formed using a contact printing mask with a broadband deep UV light source. Patterns can also be created using electron beam direct write. Results are shown for TiO_2 films patterned optically to generate features down to 0.5μm. Edge definition and pattern stability are optimum following a partial exposure conversion of the precursor, to the extent that differential solubility of the converted pattern allows the image to be developed. Full conversion of the pattern is completed in a subsequent step. The desired post-exposure processing is a function of the film application, and is different for a hard mask than for a high-κ dielectric, for example. The work presented here is intended to serve as a model system for the development of other deposition materials and processes targeted specifically for flexible electronics, including metal conductors, transparent conductors, and dielectric films.

3:45 PM H5.2
ELECTROCHEMICAL PATTERNING OF CONDUCTING POLYMER LAYERS: A NOVEL TECHNOLOGY FOR "PRINTING" POLYMER ELECTRONIC DEVICES. Payman Tehrani[a], Tommi Remonen[b], Lars-Olov Hennerdal[b], Anna Malmström[b], Jessica Häll[b], David Nilsson[a], Luc Leenders[c], Thomas Kugler[a,b], and Magnus Berggren[a]; [a]Dept of Science and Technology, Linköping University, Campus Norrköping, Norrköping, SWEDEN; [b]Acero AB, Norrköping, SWEDEN; [c]Agfa Gevaert N.V., Mortsel, BELGIEN.

Within the context of polymer electronics, a number of additive and subtractive schemes have been proposed for realizing conducting polymer patterns: In the additive methods, conducting polymers are deposited on the substrate with some printing technology. In contrary to that, subtractive methods are based on the selective removal or de-activation of certain areas of a uniform polymer layer, which results in the formation of the desired polymer pattern. Whereas subtractive patterning is usually based on photolithography, resulting in a high pattern resolution, additive processes based on printing technologies allow for inexpensive and high volume production processes for the patterning and assembling of polymer electronic devices. Here we present a novel, subtractive approach, which is based on the local deactivation of the electrical conductivity in layers of conducting polymers by an irreversible, electrochemical over-oxidation process. Experiments have been conducted with PEDOT-PSS, but the method is applicable on other conducting polymers as well. The deactivated areas can be defined by a photolithography mask, which allows for high pattern resolution (we have demonstrated deactivation line widths under 10 micrometers). Alternatively, the contact area between the conducting polymer layer and a plotter pen (containing the electrolyte and counter-electrode) can define the deactivation area: In combination with a PC-controlled large area plotter, this "digital printing technology" is a highly versatile and flexible laboratory tool for the rapid prototyping of polymer electronic devices. Conductivity ratios between pristine and over-oxidized PEDOT-PSS approach 10^7 and we will discuss the influence of process parameters, such as chemical composition and concentration of the electrolyte, applied voltage, patterning speed, etc ... on the patterning process.

4:00 PM H5.3
CAPILLARY DRIVEN SPREADING OF DIRECTLY PRINTED POLYMER PATTERNS USED FOR LARGE-AREA ELECTRONICS FABRICATION. Scott M. Miller and Sandra M. Troian, Department of Chemical Engineering, Princeton University, Princeton, NJ; Sigurd Wagner, Department of Electrical Engineering, Princeton University, Princeton, NJ.

A variety of printing techniques can be used to directly pattern thin films of etch resist polymers, or solutions or suspensions of functional device materials. Most of these techniques rely on fluidity of the "ink" to achieve good pattern transfer. The ink commonly remains liquid-like for some period of time before it is solidified. In this time, capillary driven spreading of the printed structures can occur, leading to a loss of pattern fidelity and spatial resolution, and possibly to off-design electrical performance. In general, circuit patterns are non-equilibrium structures, and so such distortion must always be anticipated. We compare experiments of spreading of liquid polymer mask material driven by capillary pressure and gradients in surface curvature to theoretical modeling and computer simulations. These comparisons lead to a general framework for analysis of printed structures that can be applied to a number of printing technologies that utilize fluid inks.

4:15 PM H5.4
EFFECTIVE JET PRINTING OF ORGANIC SEMICONDUCTING POLYMERS. Kateri E. Paul, William S. Wong, Steve Ready, Palo Alto Research Center (PARC), Palo Alto, CA.

Organic semiconductors are an attractive alternative to conventional inorganic materials because of the ability to process the organic materials from solution, apply them to flexible substrates using lower temperatures and at a lower cost. Direct writing of these materials has the potential to reduce processing steps and material waste. While printing of semiconductors for organic light emitting diodes (OLEDs) is well known, little has been reported on printing semiconductors for organic thin-film transistors (OTFTs). We have developed a process to fabricate TFTs and arrays, using jet-printing to eliminate all photolithographic patterning. Active layers of the polymeric semiconductor poly-9,9-dioctylfluorene-co-bithiophene (F8T2) are jet-printed to form the TFTs. Many factors are found to affect the characteristics of TFT devices having a jet-printed semiconductor layer, including the substrate temperature, surface energy, printing direction, device geometry, and drop size and overlap. We will discuss the printing conditions that lead to performance similar to that of devices fabricated by spin coating.

4:30 PM H5.5
INKJET PRINTING OF CONDUCTORS AND DIELECTRICS FOR SOFT ELECTRONICS. Yuka Yoshioka, Paul Calvert and Ghassan E. Jabbour, University of Arizona, Tucson, AZ.

Inkjet printing has been used for depositing materials in order to build devices or structures. For multilayer printing we need to be able to deposit inks such that the new liquid ink does not mix with previous layers. If a single solvent, or dispersing medium, such as water is to be used, we must be able to chemical solidify the early layers in order to print onto them. This might be done by thermal or photo-crosslinking or by codepositing two reactive inks. A necessary part of device building will be removal of unwanted reaction products by a washing step. This requires that the printed layers must also adhere to the substrate and each other. Printing has been carried out using both thermal and piezoelectric printheads attached to a computer-controlled 3-axis (xyz) stage. This paper will describe efforts to print and immobilize dielectrics, metallic conductors and electroactive polymer gels.

4:45 PM H5.6
NANOIMPRINT LITHOGRAPHY AND NANOWIRE ELECTRONICS ON FLEXIBLE PLASTIC SUBSTRATES. Michael C. McAlpine and Charles M. Lieber, Harvard Univ, Dept of Chemistry, Cambridge, MA.

The merger of nanoscale devices with the flexibility and low cost of plastics could enable a broad spectrum of electronic and photonic applications, although difficulties in lithographic processing of plastics at the nanoscale has limited exploration of this potential. Here we describe the use of nanoimprint lithography for the production of a wide range of nanoscale designs on flexible organic substrates using a simple, room-temperature approach. This involved the production by electron-beam lithography of an inorganic stamp with nanoscale oxide features, which was then fastened to a hand-held press and physically molded into a piece of plastic coated with our chosen imprint resist. We utilize this development to create pre-patterned features for use in bottom-up assembly of semiconductor nanowires, which are chosen to provide specific electronic and/or photonic function. The solution-based assembly of such wires allows for an additive hierarchy of devices on these inexpensive, lightweight materials. Specifically, we aligned doped silicon nanowires onto nanoimprint-patterned metal gates to create fast, flexible field-effect transistors. We have also employed direct-bandgap semiconductor nanowires to form crossed arrays of light-emitting diodes. These key functioning elements constitute a robust new catalog of high-performance, low-power 'plastic' devices. Potential applications and implications for the future will be discussed.

SESSION H6: POSTER SESSION
FLEXIBLE ELECTRONICS
Chair: Babu R. Chalamala
Wednesday Evening, April 23, 2003
8:00 PM
Salon 1-7 (Marriott)

H6.1
A STUDY OF THIN METAL FOILS FOR FLEXIBLE

ELECTRONIC APPLICATIONS. Sambit K. Saha, Themis Afentakis, and Miltiadis K. Hatalis, Display Research Laboratory, Department of Electrical and Computer Engineering, Lehigh University, Bethlehem, PA; Apostolos T. Voutsas, Sharp Laboratories of America, Camas, WA.

Thin metal foils are light-weight and non-brittle materials. They can also withstand high temperature processing under controlled atmospheres. Hence they are potentially attractive alternatives to quartz and polymers as flexible substrate materials in microelectronic device applications that demand a high degree of ruggedness. High temperature processing enables fabrication of thin film transistors with superior device characteristics. This paper discusses the viability of a variety of substrate materials in flexible thin film transistor fabrication where high process temperatures were used. Working transistors were fabricated on thin 304 stainless steel, Kovar, and Titanium substrates. Mobilities for n-channel and p-channel devices up to 250cm2/Vs and 80cm2/Vs, respectively, have been achieved. Surface roughness and surface cleanliness are important substrate parameters that have the potential of affecting device performance considerably; hence they have to be controlled prior to device fabrication. The feasibility of using a variety of polishing procedures on available substrate materials such as stainless steel, Kovar, Inconel alloy, Titanium and Molybdenum have been examined in the light of x-ray photoelectron spectroscopy, scanning electron and atomic force microscopy data.

H6.2
Abstract Withdrawn.

H6.3
TETRAHEDRAL AMORPHOUS CARBON FILMS FOR ENCAPSULATION OF FLEXIBLE NEURAL STIMULANT MICROELECTRONIC IMPLANTS. Renato P. Camata, Mevlut Bulut, University of Alabama at Birmingham, Dept of Physics, Birmingham, AL; Robyn Sweitzer, Carmen Scholz, University of Alabama in Huntsville, Dept of Chemistry, Huntsville, AL; Douglas B. Shire, Cornell University, School of Electrical Engineering, Ithaca, NY.

Implantable microelectronic devices capable of neural stimulation present a promising pathway to restore basic neural functions in humans where non-regenerative specialized tissue responsible for signal transduction has been permanently damaged. Device flexibility is essential because gap-free alignment within the host tissue is necessary and bending often occurs during implantation. Although molecular electronic devices are desirable for this application, their realization awaits significant advances in that field. Alternatively, generators of neuro-stimuli are within reach of current integrated circuit technology. Challenging performance and reliability issues arise, however, when these flexible prosthetic devices are implanted into soft tissue and exposed to bodily fluids. Polyimide, the well-established polymeric standard for encapsulation of microelectronic circuits, is hydrophilic enough to allow significant rates of water and ion penetration, which lead to corrosion and device failure. Tetrahedral amorphous carbon (ta-C) is an attractive candidate for protective encapsulating layers on polyimide-laden devices because of its excellent mechanical properties, chemical inertness, and biocompatibility. We have explored this encapsulation approach by creating 100-500-nm-thick ta-C films by pulsed laser deposition on polyimide substrates at room temperature. Pyrolytic graphite targets were ablated using a KrF excimer laser (248 nm) in high vacuum at fluences of 5-15 J/cm^2. Layers show excellent adhesion to the polyimide substrate and Raman measurements confirmed the tetrahedral-carbon nature of films. Atomic Force Microscopy indicates high-quality, dense, pinhole-free ta-C films at optimized 8 J/cm^2 laser fluence and 3.6 Angstrons/sec deposition rate. Nanoindentation measurements have yielded hardness of 29 GPa and Youngs Modulus of 250 GPa. We will show how we have used this approach to coat flexible tridimensional implant simulants and will report on their *in vivo* biocompatibility. We will also discuss other serious materials issues such as the possible negative effect of intrinsic stress present in ta-C on device performance and the stability of ta-C/polyimide interface.

H6.4
Abstract Withdrawn.

H6.5
ELECTRONIC CIRCUIT COMPOSITION AND STRUCTURE OF WARP AND WOOF FOR A NOVEL HYBRID OPTO-ELECTRONIC INTEGRATED SYSTEMS WITH TEXTILE STRUCTURES. Shigekazu Kuniyoshi and Kuniaki Tanaka, Chiba Univ, Dept of Electronics & Mechanical Engineering, Chiba, JAPAN.

A new integrated circuit concept that forms electronic equipment by the textile structure using the flexible fiber equipped with the field effect transistor, the light emitting diode, the wiring pattern, etc. is proposed. In this report, the structure of the filamentous body as a basic structure of the cloth with various electronic functions was examined. A plastic optical fiber, the glass fiber, and the insulation coating thin metal line which is enough flexible to weave the cloth are used as a base substance of the string for cloth. The warp and the woof are located up and down alternately in textile structure. The part where the warp crosses with the woof is used as an electric connection in the new integrated circuit. The connection pad adjoined each other on the warp or the woof becomes the relation of the front reverse side. The field effect transistor and the electrode pattern for wiring formed on a pillar-like fiber are arranged symmetrically with the front reverse side. In order to simplify circuit composition, an active element such as field effect transistors, the electrode pattern for wiring, and the pads for connection are formed on the warp, and the electrode pattern for wiring and the pads for connection are formed on the woof. The circuit composition and a concrete structure of the warp and the woof will be discussed, and it will be shown that all logic circuits and flip-flop circuits can be constituted using only five kinds of thread.

H6.6
LOW TEMPERATURE PECVD SILICON OXIDE FOR DEVICES AND CIRCUITS ON FLEXIBLE SUBSTRATES. Mark Meitine and Andrei Sazonov, Univ of Waterloo, Electrical and Computer Engineering Dept, Waterloo, Ontario, CANADA.

The aim of this research is to develop low temperature gate dielectric/passivation layer for μc-Si and poly-Si based devices and circuits compatible with plastic substrates. The PECVD silicon oxide films were fabricated from mixture of silane and nitrous oxide at 250°C, 120°C and 75°C. Helium, argon, and nitrogen were used as diluent gases to optimize density, mechanical stress, uniformity, and electronic properties. Chemical composition and bonding in the films were studied by FTIR spectroscopy. The absorption peak at 1075-1080 cm^{-1} observed in the spectra of all films corresponds to SiO_2 stretching mode. No presence of SiH stretching or NH-stretching vibrations was found in the FTIR spectra. Film uniformity was varied from 2% to 6% for 6"x6" area. The deposited films have compressive stress varied from 0.063 GPa to 0.117 GPa. Respective film density is in the range from 1.35 g/cm^3 to 1.69 g/cm^3. The electronic properties were studied on MOS capacitors with 200 nm thick SiO_x. The dielectric permittivity was in the range between 2.03 and 3.57. The dielectric breakdown at 9 MV/cm was observed for the films deposited at 120°C. The films deposited at higher temperatures are characterized by lower leakage current density, which was 3.7x10$^{(-10)}$ A/cm^2 for the sample deposited at 250°C, 9x10$^{(-9)}$ A/cm^2 for 120°C, and 2.2x10^{-8} A/cm^2 for 75°C at 5 MV/cm. The a-Si:H and μc-Si based TFTs were fabricated using low temperature oxide as gate dielectric. TFT performance will be presented and discussed.

H6.7
Abstract Withdrawn.

H6.8
DEVICE GEOMETRIES FOR THIN FILM TRANSISTORS OF NANOCRYSTALLINE SILICON. I-Chun Cheng and Sigurd Wagner, Department of Electrical Engineering, Princeton University, Princeton, NJ.

Nanocrystalline silicon can be deposited over large areas at low substrate temperature and is capable of p and n channel operation. Therefore it is a semiconductor for fully-integrated active matrices. To reach technology readiness the thin film transistors (TFTs) made of nanocrystalline silicon (nc-Si:H) need optimized materials and processes for the channel, the gate dielectric, and the source/drain contacts. They also need experimenting with unconventional device geometries. We describe our recent research of the effects of the peculiar properties of nc-Si:H on transistor geometries and on certain process steps. TFTs of nc-Si:H are made as top gate devices to take advantage of the crystalline portion of the nc-Si:H film. The channel film is grown to a thickness at which the crystalline columns just coalesce at the surface. The contiguous crystalline surface layer so formed hosts the ~10-nm thick TFT channel with high hole and electron mobilities and high ON currents. The OFF current is set by conduction through the entire cross section of the channel layer. High ON combined with low OFF currents are obtained from growing the thinnest possible nc-Si:H channel films with fully developed crystallinity in their surface. Either coplanar (top) or staggered (bottom) source/drain contacts are usable. The most critical step in making coplanar TFTs is etching through the doped contact layer to the surface of the channel film. Because in the staggered geometry the channel film in the gate region nucleates differently from the contact regions, growing a seed layer in the gate region improves TFT performance. The important mask alignment step also varies with each of these TFT geometries. Prospects are good for further enhancement of TFT performance coming from experiments with TFT geometry.

H6.9
Transferred to H10.10

H6.10
THERMAL VIBRATION IN nAgI-3Ag_2O-2V_2O_5. A.Thazin, Y. Fujishima, M. Arai, T. Sakuma, Department of Physics, Ibaraki University, Mito, JAPAN; H. Takahashi, Faculty of Engineering, Ibaraki University, Hitachi, JAPAN.

In recent decades, much attention has been paid to superionic conducting glasses because of their high ionic conduction and application to batteries and other electrochemical devices. Among these, AgI doped glasses are easy to form the glassy state and they possess high ionic conductivity near room temperature. In order to inspect the thermal vibration of atoms in superionic conducting glasses, X-ray diffraction measurement of superionic conducting glasses nAgI-3Ag_2O-2V_2O_5 has been performed at 12, 100, 200 and 290 K.
Appropriate amounts of AgI, Ag_2O and V_2O_5 were mixed and melted at 600°∼1000° C. The sample was poured on a stainless-steel block and pressed by another block. By the method, rapid quench and glass formation of a thin sample can be realized. X-ray intensity data were collected using MoKα radiation for 80 s per step at 0.1° intervals over the 2θ range of 5° to 115° by a step-scan mode.
The profiles of the X-ray scattering intensity for superionic conducting glasses are discussed with the theory including the thermal displacements of atoms. The temperature dependence of characteristic features of observed structure factor S(Q) of glasses has been obtained. It is clarified that the effective overall Debye-Waller temperature parameter B increases with the increase of temperature and also increases with AgI concentration.

H6.11
LOW TEMPERATURE COPPER-INDUCED CRYSTALLIZATION TECHNIQUE FOR GERMANIUM ON FLEXIBLE PET, BY MEANS OF MECHANICAL COMPRESSIVE STRESS. Bahman Hekmatshoar, Davood Shahrjerdi, Shams Mohajerzadeh, Ali Khakifirooz, Arash Akhavan,Tehran Univ, Dept of Electrical and Computer Engineering, Tehran, IRAN; Michael Robertson, University of Acadia, Wolfville, NS, CANADA.

Mechanical compressive stress has been exploited to devise a low temperature metal-induced crystallization technique. Stress-assisted copper-induced crystallization of amorphous germanium has been performed on flexible PET substrates at temperatures as low as 130°C. Sample preparation was performed by e-beam deposition of Ge and thermal evaporation of Cu at a base pressure of 1×10^{-6} torr and a substrate temperature of 100°C, forming a Ge-Cu-Ge structure with thickness of 500Å-10Å-500Å on 120μm thick PET. Compressive or tensile stress was applied by inward bending or stretching the flexible substrate, at temperatures ranging from 130 to 180°C. During thermal treatment at a temperature of 150°C and an equivalent 0.05% compressive strain, the sheet resistance of Ge layer was monitored, evidencing a three orders of magnitude drop after 90 minutes. A sheet resistance of 25 K$\Omega/\square$ and a hole mobility of 110cm^2/V-s were obtained for this sample, measured with Hall effect. XRD, TEM and SEM analyses were also used to verify the crystallinity of the samples. XRD reveals the $< 220 >$ and $< 400 >$ peaks of Ge in the partially crystalline PET background. TEM diffraction patterns corroborate the polycrystalline structure of the Ge layer. SEM shows a granular surface morphology with an average size of 0.2μm, indicating an enhanced nucleation at buckling sites, where compressive stress is more densely accumulated. These buckling sites are located in parallel lines with 50μm separations. Minimizing crack density was obtained by patterning the amorphous Ge layer before thermo-mechanical treatment. These polycrystalline Ge films were used to fabricate flexible depletion-mode Ge-TFTs on PET with polystyrene gate dielectric and chromium gate metal, showing an ON/OFF ratio of 10^4. Polystyrene was used to minimize gate leakage current caused by crack formation, induced from Ge into the dielectric layer. The resulting leakage current is still high and its minimization is under study.

H6.12
A NOVEL METHOD FOR CONSTRUCTING STRETCHABLE METALLIZATION. Joyelle Jones, Stephanie Perichon-Lacour, Sigurd Wagner, Princeton University, Department of Electrical Engineering and POEM, Princeton NJ; Zhigang Suo, Princeton University, Department of Mechanical and Aerospace Engineering, Princeton, NJ.

Stretchable metallization is a key to the fabrication of 3-D conformal circuits and electrotextiles. The basic concept for reversibly stretchable metallization is a corrugated stripe of thin-film metal that is expanded by stretching and relaxes back upon release. The maximum elongation is reached when the stripe is stretched flat. Very recently, three approaches have been demonstrated to fabricate such metallization by deposition of thin films on elastomeric substrates. (1) A film deposited with built-in stress on a flat substrate can be made to buckle to a wave, which then can be stretched. (2) When a film is deposited on a wavy substrate surface it becomes a wave. (3) The substrate is stretched prior to deposition of the film, which upon release relaxes to a wave. We have introduced techniques (1) and (3), and in this presentation will focus on the universally applicable technique (3). We carried out experiments with substrate width and elongation, gold metal line width and thickness, and measured the film structure, amplitude and wavelength, as well as electrical conductance in relaxed and various stretched states. So far we have strained the substrate by 8 percent while maintaining the initial conductance of the film, which is approximately 3 times that of an ideal gold conductor. We discovered a rich variety of macroscopic and microscopic film morphology. We will present the theory of wavy interconnects, their fabrication and electro-mechanical performance, and data on film structure.

H6.13
Abstract Withdrawn.

H6.14
LIGHT TRAPPING IN AMORPHOUS SILICON SOLAR CELLS. Vanessa Terrazzoni-Daudrix, Joelle Guillet, Marion Ferelloc, Arvind Shah, Institut of Microelectronics, University of Neuchâtel, SWITZERLAND; R. Morf, PSI (Paul Scherrer Institut), Villigen, SWITZERLAND; O. Parriaux, TSI (Traitement du Signal et Instrumentation), Jean Monnet University, Saint Etienne, FRANCE; F. Diego, VHF Technologies S.A., EICN, Le Locle, SWITZERLAND.

In order to simultaneously decrease the production costs of thin film silicon solar cells and obtain higher performances, the authors have studied the possibility to increase the light trapping effect within thin film silicon solar cells deposited on flexible plastic substrates. In this context, different nano-structure shapes useable for the back contacts of amorphous silicon solar cells on plastic substrats have been investigated: random textures and gratings:
Plasma etching has been used to produce randomly textured plastic surfaces. Varying the etching parameters changes the feature size of the texture. The optimisation of such back reflectors is so far empirical. Gratings constitute a well-known optical technique and their light trapping effect can be optimised by simulation. They are well adapted to mass production because they can be obtained by directly embossing the plastic substrate. Spectrometry, AFM and SEM measurements have been performed on many different types of back contacts and the most interesting ones have been tested in cells. A first conclusion is that neither the traditional "Haze factor" determined in air for a wavelength of 650nm nor the "rms roughness" of the surfaces are sufficient as criteria to optimise the back contact roughness for light trapping in cells. The shape of grains is a further essential criteria.
Experimentally, randomly textured back reflectors have a substantial effect on light trapping in amorphous thin film silicon solar cells. The authors have so far obtained a relative current enhancement of 16% for solar cells deposited on randomly textured polyethylene terephthalate (PET), and 10% for solar cells deposited on periodic grating structures (glass substrate), as compared to a corresponding conventional solar cell co-deposited on a flat mirror on glass. Solar cells on PET with 6% stabilized efficiency have until now been obtained.

H6.15
Ge NANOPARTICLE SIMULATIONS FOR EFFICIENT, FLEXIBLE, THIN-FILM PHOTOVOLTAICS. Sang H. Yang and Rajiv J. Berry, Air Force Research Laboratory, Materials and Manufacturing Directorate, AFRL/MLBP WPAFB, OH.

Nanoparticles are known to melt at temperatures well below the bulk melting point. This behavior is being exploited for the low temperature recrystallization of Germanium to form large-grain thin films. Bulk properties of Germanium structures (diamond, BC8 and ST12) were computed by a density functional pseudo-potential method using a local orbital basis set. The computed lattice constants, bulk moduli, and internal atomic positional parameters were found to agree well with experimental results and with other plane wave basis calculations. MD simulations using both empirical potentials and density functional pseudopotentials were conducted to study melting temperatures, coalescence, and energetics of Ge nanocrystals as a function of size and chemical termination. Results of these nanoparticle simulations will be utilized to guide experimental efforts aimed at the production of near-single crystal semiconductor thin films on flexible, low temperature substrates.

H6.16
Abstract Withdrawn.

H6.17
GROWTH AND IN-SITU CHARACTERIZATION OF HETERO-MOLECULAR THIN FILMS. L. Fornace, E. Suljovrujic, S. Demic, Lj. Damjanovic, and V.I. Srdanov, Center for Polymers and Organic Solids, University of California at Santa Barbara, Santa Barbara, CA.

Charge and/or energy transfer processes between two molecules, as well as luminescence self-quenching phenomena, are highly dependent on the concentration ratio of the two constituents. In order to reduce the exploration time for device optimization, we utilize a dual evaporator chamber coupled with a remote absorption spectrophotometer and a photoluminescence (PL) apparatus. The computer-controlled MBE set-up produces dynamical change in the concentration ratio of the molecules, starting from pure component A at the beginning of the growth cycle to pure component B at the end. The dynamical in-situ absorption and PL spectra of Eu(dbm)3phen/TPD and Eu(dbm)3phen/AlQ3 mixtures grown on quartz substrates will be presented. L.F. thanks INSET/CCIMR Intership Summer 2002 Program at UCSB for support. This work was supported by NSF-CHE0098240.

H6.18
OPTIMIZATION OF INDUCTIVELY COUPLED PLASMA CHEMICAL VAPOR DEPOSITION SiO_2 FOR ULTRA-LOW TEMPERATURE POLY-Si TFT GATE OXIDES. Su-Hyuk Kang, Kook-Chul Moon, Min-Cheol Lee, Min-Koo Han, Seoul National University, School of Electrical Engneering, Seoul, KOREA.

Poly-Si TFTs (Thin Film Transistors) on flexible plastic substrates have attracted considerable attentions. A high quality gate insulator such as oxide is critical for practical applications and it is well known that ultra-low temperature (below 200°C) process is required on the plastic substrate. The suitable gate insulator with high breakdown field and low fixed oxide charge density are required to get high performance TFTs. Recently, ultra-low temperature (150°C) PECVD (Plasma Enhanced Chemical Vapor Deposition) oxide has been reported. However, the characteristics of the oxide are rather poor and more than 100 times excimer laser irradiation is required to improve oxide quality. The purpose of our work is to report an ultra-low temperature gate oxide deposition method by employing ICP-CVD (Inductively Coupled Plasma Chemical Vapor Deposition) and improvement of gate oxide quality by excimer laser irradiation. The deposition condition of ICP-CVD oxides for high breakdown field has been optimized. High breakdown field SiO_2 was successfully deposited at 150°C by ICP-CVD using He as carrier gas and N_2O and SiH_4 as precursors. The SiO_2 film exhibited high breakdown electric field over 8MV/cm and the CV flat band voltage (V_{FB}) was about -6V. After XeCl (λ=308nm) excimer laser annealing on the oxide, remarkable positive shift of V_{FB} was observed. V_{FB} was about -2V, which was shifted by 0.7V$\sim$5.9V after 10$\sim$20 times excimer laser irradiation. Experimental results show that the ICP-CVD oxides may be suitable for gate oxides for ultra-low temperature poly-Si TFTs on flexible substrates, employing only 10$\sim$20 times excimer laser irradiation to improve oxide quality.

H6.19
THIN FILM MORPHOLOGY AND GROWTH MECHANISMS OF PENTACENE THIN FILM USING LOW-PRESSURE ORGANIC VAPOR DEPOSITION. Seong Deok Ahn, Seung Youl Kang, Yong Eui Lee, Meyoung Ju Joung, Chul Am Kim, Mi Kyung Kim, Kyung Soo Suh, Basic Research Laboratory, Electronics and Telecommunications Research Institute, Daejeon, KOREA.

We have investigated the growth mechanisms and thin film morphology of pentacene thin films by the process of low-pressure organic vapor deposition. Source temperature, inert gas flow rate, substrate temperature and chamber pressure during film deposition is used to vary the growth rate, thin film morphology and the crystalline grain size of pentacene thin films. The electrical properties of pentacene thin films for applications in organic thin film transistor and electrophoretic displays will be discussed.

SESSION H7: FLEXIBLE ELECTRONIC MATERIALS
Chair: Jin Jang
Thursday Morning, April 24, 2003
Salon 14/15 (Marriott)

8:30 AM H7.1
FLEXIBLE MAGNETICS: MAGNETIC LITHOGRAPHY AND FABRICATION OF MAGNETIC MASKS ON THIN PLASTIC SUBSTRATES. Z.Z. Bandić, H. Xu, T.R. Albrecht, IBM Almaden Research Center, San Jose, CA.

Flexible magnetic lithography is a process qualitatively analogous to contact optical lithography which transfers information from a patterned magnetic mask (analog of optical photomask) to magnetic media (analog of photoresist), and is interesting for applications in instantaneous parallel magnetic recording. The magnetic mask consists of patterned soft magnetic material (FeNiCo, FeCo) on a flexible plastic substrate, typically Polyethylene Teraphtalate (PET). When uniformly magnetized media is brought into intimate contact with the magnetic mask, an externally applied magnetic field selectively changes the magnetic orientation in the areas not covered with the soft magnetic material. Flexible substrate of the magnetic mask offers superior compliance to magnetic media which is likely to have imperfect flatness and surface particulate contamination. Although magnetic in physical nature, flexible magnetics draws interesting parallels to flexible electronics, especially in challenges of fabrication of sub-micron patterns on thin flexible plastic substrates. We fabricated samples of sub-micron patterned FeCo and FeNiCo magnetic masks on PET substrates by using combined lamination/release process of PET films. Rigid substrates, typically silicon or quartz were initially laminated with PET films and processed using standard fabrication procedures. After completing magnetic mask device fabrication, PET films were released from the rigid substrates. We successfully transferred patterns from magnetic masks to hard disk CrPtCo-based magnetic media. The details of the method, including physics of the magnetic lithography pattern transfer, fabrication of the magnetic mask on flexible PET substrates, lamination and release of PET films, and magnetic force microscopy (MFM) images of the magnetic transition patterns are reported.

8:45 AM H7.2
ZnO THIN FILM TRANSISTORS FOR FLEXIBLE ELECTRONICS. P.F. Carcia, R.S. McLean, M.H. Reilly, and G.Nunes Jr, DuPont Research and Development, Wilmington, DE.

One of the challenges for flexible electronics is finding a semiconductor compatible with low temperature processing required by plastic substrates. A common plastic, such as polyethylene terephthalate (e.g., Mylar-R), typically limits device processing to much less than 150°C. One consequence is that electronics based on Si, even amorphous Si, may be incompatible with plastic substrates. That, in part, has fueled a broad interest in organic semiconductors as an inexpensive, low-temperature class of alternative materials, especially for thin film transistors (TFTs). However, the electronic properties of most organic semiconductors are inferior to those of amorphous Si, and organic materials frequently degrade in normal atmospheric conditions, requiring protection strategies. In contrast, a stable inorganic semiconductor compatible with temperature sensitive substrates, and with electronic properties equivalent to amorphous Si would enable electronics on a variety of flexible substrates. We show that ZnO semiconductor can meet those requirements. We fabricated ZnO thin film transistors by rf magnetron sputtering on substrates held near room temperature. The resistivity of films depended on the oxygen partial pressure during sputtering and underwent an abrupt transition from semiconducting ($\sim 10^{-2}$ ohm cm) to semi-insulating ($\sim 10^{7}$ ohm cm). We investigated the properties of TFT devices made in the vicinity of this resistance transition. The best devices had field-effect mobility of more than 2 cm^2/V-s and on/off ratio $>10^6$. These ZnO films had resistivity $\sim 10^5$ ohm cm, with high optical transparency (>80% for wavelength > 400 nm), and compressive stress < 0.5 GPa. The combination of transparency in the visible, excellent transistor characteristics with low processing temperature, and the prospect of p-type ZnO TFTs for complementary structures, make ZnO thin film transistors attractive for flexible electronics on temperature-sensitive substrates.

9:00 AM H7.3
PULSED LASER DEPOSITION OF ZnO THIN FILMS AND NANOSTRUCTURES ON FLEXIBLE SUBSTRATES FOR UV APPLICATIONS. Masashi Matsumura and Renato P. Camata, University of Alabama at Birmingham, Dept of Physics, Birmingham, AL.

Zinc Oxide (ZnO) is a promising wide bandgap semiconductor for applications in UV light emitting devices and sensors. Although significant advances in bulk and epitaxial growth, p-type doping, and production of high quality contacts are still needed to enable ZnO as a competitor for large scale UV applications, some of its characteristics suggest it may be a suitable material for integration into flexible electronics platforms. Its compatibility with low temperature deposition, the success of ZnO nanostructure synthesis, its anticipated biocompatibility, and its relative ductility in thin film form indicate that ZnO may become an important route to deliver UV functionality in flexible electronic devices. In order to assess the potential of ZnO in flexible electronics applications we created continuous and nanostructured ZnO films on polymeric substrates for evaluation of structural and optical properties. Specifically, we have used pulsed laser deposition (PLD) to deposit ZnO films with

thickness between 100 nm and several microns on polyimide substrates at room temperature. A KrF excimer laser (248 nm) operated at fluences of 1-3 J/cm^2 was used and films were deposited under O_2 atmosphere at a pressure of 10^{-4} Bar. Good flexibility characterizes the obtained layers and x-ray diffraction measurements show that films present all reflections of hexagonal ZnO. Atomic force microscopy analysis on the films revealed highly textured surfaces with RMS roughness in the 200 nm range. Improvements in adhesion strength are sought, however, as most of the films adhered poorly to the polyimide substrates. We will discuss luminescence measurements on the films in relation to the complex interface phenomena expected in our samples. In addition, we will report on how we have used a novel PLD-inspired approach known as Nanoparticle Beam Pulsed Laser Deposition (NBPLD) to deposit ZnO nanoparticles on polyimide substrates for potential flexible UV-based biosensing applications. (Research funded by NSF-DMR-0116098).

9:15 AM H7.4
INORGANIC-ORGANIC HYBRID MATERIALS FOR POLYMER ELECTRONIC APPLICATIONS. R. Houbertz, J. Schulz, G. Domann, L. Froehlich, and M. Popall Institute for Silicate Research ISC, Wuerzburg, GERMANY.

During the last years, much attention has been attracted by organic polymer electronics. Particularly organic field effect transistors are a topic of intensive investigation. Due to the relatively high sensitivity of active polymer functional layers with respect to diffusion of, e.g., water, organic integrated circuits have to be protected using suitable barrier coatings. The diversity of possible applications and designs such as particular FET architectures, results in a need for photo-patternable passivation layers which simply can be introduced into the devices. Inorganic-organic hybrid polymers (ORMOCER^{TM}) of various composition have been synthesized by hydrolysis/polycondensation reactions, followed by an organic cross-linking of organic functional groups such as methacryl, styryl or epoxy. Thus, the materials can be patterned by UV lithography. The synthesis can be controlled such that the resulting materials show very low water vapor permeation values which is a key property for passivation applications. Dependent on the processing conditions, e.g., using UV and/or thermal initiators as well as thermal hardeners, typical water vapor permeation values range between approximately 1 and 5 $\frac{g}{m^2 d}$ for individual thin-film layers (calculated for 100 μm). Besides, these layers can be used as dielectric passivation where the dielectric strength can be as high as 400 $\frac{V}{\mu m}$. The permittivity typically ranges between 4 and 5.5 in the low frequency range (10 Hz to 1 MHz). The passivation properties will be discussed with respect to the inorganic-organic network which is build upon processing. Particular emphasis will be on the influence of inorganic-oxidic particle sizes (determined by SAXS measurements) and the inorganic content as well as on the degree of polymerization of the organic functional groups (FT-IR spectroscopy), both influencing the inorganic-organic network. In addition, impedance spectroscopy measurements are used to characterize the dielectric behavior of the inorganic-organic hybrid polymers. ^{TM}registered by the Fraunhofer-Gesellschaft für Angewandte Forschung e.V.

9:30 AM H7.5
ENHANCED EFFICIENCY OF PLASTIC PHOTOVOLTAIC DEVICES BY BLENDING WITH IONIC SOLID ELECTROLYTES. Fang-Chung Chen, Yang Yang, Univ. of California, Los Angeles, Dept. of Materials Science and Engineering, Los Angeles, CA.

Plastic photovoltaic cells are promising energy source for many unique applications. Unfortunately the efficiency of current solar cells is still low. One of the bottlenecks limiting the efficiency is the low carrier mobility and thin film conductivity. In this presentation, we present an approach to solve this problem by adding a small amount of electrolyte into our polymer system. The heterojunction polymer photovoltaic devices, consisting of poly[2-methoxy-5-(2′-ethyl-hexyoxy)-1,4-phenylene vinylene] (MEH-PPV) and methano-fullerene([6,6]-phenyl C61-butyric acid methyl ester) (PCBM) as the active materials, were fabricated. It has been found that the power efficiency of organic was enhanced by blending ionic solid electrolyte, such as polyethylene oxide (PEO) and polyethylene glycol(PEG) into the active layer. The device performance will be described and the mechanism will be discussed in this presentation.

SESSION H8: NOVEL DEVICES AND CONCEPTS
Chair: Jin Jang
Thursday Morning, April 24, 2003
Salon 14/15 (Marriott)

10:15 AM H8.1
NANOTECTONICS: DIRECT FABRICATION OF ALL-INORGANIC LOGIC ELEMENTS AND MICRO-ELECTRO-MECHANICAL SYSTEMS FROM NANOPARTICLE PRECURSORS. Eric J. Wilhelm, Joseph Jacobson Massachusetts Institute of Technology, Media Lab, Cambridge, MA.

The reduced melting point and high solubility of inorganic nanoparticles have been shown to be useful in the low-temperature solution-based fabrication of semiconductor devices. These inks have been patterned using various techniques to form inorganic logic elements, multi-layer structures, and MEMS. Here we report advances in the printing of such nanoparticle inks.

10:30 AM H8.2
Abstract Withdrawn.

10:45 AM H8.3
HIGH-QUALITY INKJET-PRINTED MULTILEVEL INTERCONNECTS AND INDUCTIVE COMPONENTS ON PLASTIC FOR ULTRA-LOW-COST RFID APPLICATIONS. Steven Molesa, David R. Redinger, Daniel C. Huang, and Vivek Subramanian, University of California, Berkeley, Department of Electrical Engineering and Computer Scienece, Berkeley, CA.

Printed electronics is widely considered to be a crucial step to achieving ultra-low-cost RFID circuits for use as barcode replacements in consumer products, since it eliminates the need for lithography, vacuum processing, and enables the use of low-cost reel-to-reel manufacturing. While there have been some demonstrations of printed organic transistors to date, there has been little work on the associated passive component and interconnection technologies required to enable the development of RFID circuits. In particular, low-resistance conductors are crucial to achieve the high-Q inductors necessary for RFID. Last year, we reported on the development of a plastic-compatible printable conductor technology using alkanethiol gold nanoclusters. Here, we report on a robust interconnect and inductive component technology we have developed making use of the above materials library. We demonstrate inkjetted conductors on plastic with sheet resistances as low as 0.03 ohms/square, with conductivity greater than 70% of bulk gold. This conductor technology therefore provides the lowest resistance printed conductors on plastic reported to date. This was achieved by study and optimization of the solvent and jetting parameters to control the resulting droplet size, droplet kinetics on the air and on the surface of the plastic, and final film morphology. We will report on the mechanisms for optimization and control of the same. We also demonstrate a bridging technology based on an inkjetted polyimide interlevel dielectric. Using this process, we demonstrate various complex multilevel interconnect structures including bridges, tapped planar spiral inductors and multilevel planar balun crossovers. We will demonstrate the use of this technology to demonstrate single-bit passive RF tags, high-Q inductors, and various other passive components.

11:00 AM H8.4
FLEXIBLE MECHATRONIC SYSTEM OF ELASTOMER ELECTRO-ACTUATOR ADDRESSED BY THIN FILM PHOTOCONDUCTOR SWITCH. Stephanie Perichon Lacour, Princeton Univ, Dept of Electrical Engineering, Princeton, NJ; Ron Pelrine, SRI International, Menlo Park, CA; Sigurd Wagner, Princeton Univ, Dept of Electrical Engineering, Princeton, NJ.

In macroelectronics, thin film integrated circuits drive displays, sensors and actuators on flexible and deformable substrates. We demonstrate the first mechatronic system made of an electro-active polymer (EAP) based actuators, driven by thin film photoconductive high voltage switches and fabricated on a plastic foil substrate. The actuators are made of a dielectric elastomer that deforms and expands under high voltage. Its geometry is designed so that a small rigid shaft can be linearly translated during the electrostrictive deformation of the elastomer to make a linear actuator. Such linear actuators can be used for a variety of applications such as relief maps and other novel displays. The EAP is connected to the power supply through a photoconductor switch of hydrogenated amorphous silicon (a-Si:H) which is addressed and closed by illumination. We made the thin-film switches on flexible and laser transparent polyimide (Kapton®) substrates. The amorphous silicon is made by Plasma Enhanced Chemical Vapor Deposition (PECVD) at 150C substrate temperature. Aluminum conductors and electrodes are deposited on top of the a-Si:H layer by thermal evaporation. Finally the a-Si:H photo-switches are integrated onto the elastomer membrane. We made a linear array of five switch/actuator cells. We drove the array with switching speeds up to 100 Hz and voltages up to 7kV across the actuator. We describe the fabrication of the thin film photoconductors, their integration into the EAP module as well as measured and modeled electrical parameters and responses of the EAP/photoconductor system.

11:15 AM H8.5
NONVOLATILE MEMORY EFFECT ON ORGANIC CELLS. Qianfei Xu, Liping Ma, and Yang Yang, Dept. Materials Science and Engineering, UCLA, Los Angeles, CA.

Electrical bistability is a phenomenon in which a device exhibits two states of different conductivities, at the same applied voltage. In this presentation, we report an novel organic electrical bistable device (OBD) comprising of a thin organic thin film between two metal electrodes. The performance of this device makes it attractive for memory-cell type of applications. The two states of the OBD differ in their conductivity by several orders in magnitude and show remarkable stability, i.e. once the device reaches either state, it tends to remain in that state for a prolonged period of time. More importantly, the high and low conductivity states of an OBD can be precisely controlled by the application of biases to write and erase. These discoveries pave the way for newer applications, such as low-cost, large-area, flexible, high-density, electrically addressable data storage devices.

11:30 AM H8.6
FABRICATION OF ACTIVE DEVICES AND LOGIC GATES ON FIBERS. YongWoo Choi, Ioannis Kymissis and Akintunde Ibitayo Akinwande, Massachusetts Institute of Technology (MIT), Microsystems Technology Laboratories, Cambridge, MA.

Textile fabric is flexible, mechanically durable and inexpensive. Hence, textile is a suitable substrate for large area, flexible and wearable electronics. The ability to fabricate active devices on fiber is a key step for achieving large area and flexible electronic structures. We present a fabrication approach for making devices and logic gates on fibers. Hydrogenated amorphous silicon (a-Si:H) thin-film transistors (TFTs) are fabricated on 127 μm thick polyimide film. The TFT has bottom-gate and back-channel etch structure. The gate and source-drain electrodes are made of Cr. The SiNx gate dielectric, a-Si:H channel layer and SiNx passivation layer are deposited with ECR-PECVD at 80°C to avoid the thermal shrinkage of the polyimide film. A-Si anti-fuse layer and n-doped a-Si contact layer are deposited with E-beam evaporation. After patterning the channel layer, the contact patterning is performed to contact the gate and source-drain electrodes. In this paper, we shall present logic gates such as an inverters, NAND and NOR gates and ring oscillators that will be fabricated with this process. The logic gates use enhancement load NMOS logic and only require four to five masking layers for fabrication. We shall also present electrical properties of the devices and contact reliability.

11:45 AM H8.7
A BASIC CONCEPT OF NOVEL HYBRID OPTO-ELECTRONIC INTEGRATED SYSTEMS WITH TEXTILE STRUCTURES. Kuniaki Tanaka, Chiba Univ, Dept of Electronics & Mechanical Engineering, Chiba, JAPAN.

Exponential expansion of electronics during past half a century was achieved on the base of sophisticated "surface and planar" technology of semiconductor crystal. It is now forecasted that we are faced with basic physical limits of Moor's Law within the several years and those are going to grow up to a huge wall. In a general situation view, we are now in groping for a new strategy. It is necessary to take our eyes off from all elemental planar technologies and concepts related with present semiconductor electronics, such as, design, processing technology, system configuration, development object, applied area, etc. We should produce an innovative situation in which uniting with different field is inevitably involved, and a lot of reformative models and methods must be proposed in the situation. According to the situation recognition of the above-mentioned, one proposal based on a new technical principle is done here. An opto-electronic hybrid integrated system with "textile structure" is proposed as a novel electronic system and compared with "plane structure" system in present semiconductor technology. The system of textile structure is composed of warp-fiber and woof-fiber on which electronic devices, photoelectric conversion devices and various components are mounted. These elements are designed and arranged so that they are connected each other to form partial circuits, functional blocks and the final system. Several concrete compositions and characteristics of the proposed system are compared with those of present technology to construct a new electronics system. This proposal is also discussed in flexible electronics concept.

SESSION H9: FLEXIBLE SUBSTRATE TECHNOLOGIES
Chair: Norbert Fruehauf
Thursday Afternoon, April 24, 2003
Salon 14/15 (Marriott)

1:30 PM *H9.1
ULTRA-THIN FLEXIBLE GLASS SUBSTRATES. Armin Plichta, Silke Knoche, Andreas Weber, SCHOTT Displayglas, Mainz, GERMANY; Andreas Habeck, SCHOTT Glas, Mainz, GERMANY.

New applications in the electronics market ranging from foldable displays in mobile phones to wearable displays in clothes generate a high demand for flexible materials especially for substrates. The upcoming OLED technology shows some advantages in comparison with conventional LCDs and enables real flexible or shaped displays. Moreover, the wearable displays have a badly need for flexible circuits. At a first glance polymer foils are the materials of choice for flexible substrates and circuits but in general they suffer from thermal instability as well as from high permeation rates for gases and water. In contrast, even ultra thin glass sheets have excellent barrier properties and show sufficient bending properties if they are thinner than 100μm. Flexible glass substrates down to a thickness of 50μm have been developed. The deposition of an organic coating helps to overcome a lack of mechanical stability. Therefore, our flexible glass substrates can be used in conventional display manufacturing processes which include several semiconductor process steps. Moreover, they are suited for production of flexible PCB's.

2:00 PM H9.2
FILM SUBSTRATES BASED ON SILICONE RESINS. Mishitaka Suto and Nobuo Kushibiki, Dow Corning Asia Ltd, Chiba, JAPAN; Dimitris Katsoulis, Dow Corning Corporation, Midland, MI.

Commercial silicone resins are three dimensional network structures that can be depicted with the empirical formula $[R_xSiO_{(4-x)/2}]_n$, where x = 0-4 and n denotes their polymeric nature. The organic substituent, R, on the silicon atom is commonly methyl or phenyl group, but often vinyl or hydrogen substitution is being used to enable hydrosilation cure. The materials are used in numerous applications as additives, coatings and matrices for composites due to their high temperature stability, excellent electrical properties (i.e., low dielectric constant and loss), fire resistance and weather-ability. We report here the preparation of transparent, flexible films from silicone resins by solvent casting techniques. The films exhibit no birefringence, higher than 90% transparency between 350 to 1700 nm and average surface roughness below 1 nm. Thermal analysis shows that the films are stable at temperatures greater than 200°C (depending upon the starting resin composition). The films are suitable substrates for deposition of various coatings including ITO. Transparent semi-conducting ITO electrodes have been prepared with ion plating and RF sputtering methods. The ITO-silicone resin films were characterized by microscopy, XPS, absorption spectroscopy and conductivity measurements. Applications of silicone resin films in the areas of displays, electronics and energy related applications will be discussed.

2:15 PM H9.3
NEW DEVELOPMENTS IN POLYESTER FILMS FOR FLEXIBLE ELECTRONICS. Bill MacDonald, DuPont Teijin Films, Wilton, UNITED KINGDOM; Keith Rollins, DuPont Teijin Films, UNITED KINGDOM; Bob Rustin, DuPont Teijin Films, Hopewell.

Polyester films are well-known substrates for a wide range of electronic applications such as membrane touch switches and flexible circuitry. Their use is increasingly being extended into more technical areas, with ITO-sputtered polyethylene terephthalate (PET) films being successfully used for electroluminescent lamp and touch screen applications due to the versatile properties and high quality of the available base films. One area of considerable interest for the future is display technologies using organic light emitting diodes (OLED's) which are currently mainly based on glass substrates due to the need for a very smooth surface with good dimensional stability and high barrier properties. However, glass has a number of disadvantages and a more robust flexible substrate is being sought that can be processed economically in high volumes using roll-to-roll techniques. This contribution will describe new developments in polyester film substrates for this application area. In particular the development of polyethylene naphthalate (PEN) films which offer a unique combination of excellent dimensional stability, low moisture pickup, high clarity and very good surface smoothness will be discussed. This combination makes PEN a promising substrate for subsequent vacuum and other coating processes, leading to the potential use of this material as a flexible substrate for device manufacture and flexible electronics in general.

2:30 PM H9.4
GZO COATED POLYMERIC SUBSTRATES FOR OPTOELECTRONIC APPLICATIONS. E. Fortunato, V. Assuncio, A. Marques, I. Ferreira, H. Iguas, R. Martins.

Zinc oxide doped thin films have generated much attention in recent years, because of their material low cost, relatively low deposition temperature, non-toxicity and stability in hydrogen plasma, compared with indium tin oxide (ITO) and tin oxide (SnO2). It has been recently obtained by the present authors the best optoelectronic result on zinc oxide gallium (GZO) doped thin films at room temperature by

rf magnetron sputtering on glass substrates. However, when flexible optoelectronic devices are required, a polymeric substrate must be used. Nevertheless these substrates present certain challenges such as considerably lower working temperature and rougher surfaces as compared to glass substrates. In order to overcame these limitations, we have optimised the rf magnetron sputtering process in order to be able to produce transparent high conductive, low resistivity, low film stress and with a smooth surface GZO films. The films were grown by rf magnetron sputtering at room temperature on two kinds of commercially available polymeric substrates (Melynex and PEN from DuPont) in order to investigate the relationship between the polymeric substrate and the surface morphology presented by the films. The GZO films deposited on Melynex substrates, at room temperature and without any post treatment, presents a very low sheet resistance of 8 ohm/sqr and an average transmittance in the visible region of 80% (including the substrate). In this paper a detailed description on the preparation as well as on the electrical (Hall effect and resistivity as a function of temperature), optical (transmittance/reflectance and spectroscopic ellipsometry), structural (X-ray diffraction) and morphological (FE SEM and AFM) characterization will be presented.

2:45 PM H9.5
CHARACTERIZING THE MECHANICAL PROPERTIES OF NEW PHOTOPATTERNABLE LOW MODULUS SILICONES BY DEPTH SENSING NANOINDENTAION. Brian Harkness and Satyen Sarmah, Dow Corning Corporation, Midland, MI; Richard Schalek and Lawrence Drzal, Department of Chemical Engineering and Materials Science, Michigan State University, East Lansing, MI.

The continued advancement of smaller, more complex electronics devices has spawned the development of new materials capable of achieving a high level of performance yet easily processable into complex material architectures. For example, in electronics packaging there is an increasing need for low modulus materials capable of functioning as stress buffer layers to absorb the stresses generated by mismatches in the thermal coefficients of expansion of the materials of construction. In response, new silicone based low modulus materials are being developed by Dow Corning for these applications. These materials have also been designed to be spin-coatable and photopatternable to facilitate their application into device architectures. It is known that integration processes involved in building complex device structures warrant physical and chemical treatments that can change the surface properties of silicone materials. Therefore a need was apparent for a method to directly measure the mechanical properties of silicone thin films deposited on a device surface. Depth sensing nanoindentation is a method for measuring the mechanical properties of materials on a substrate. Recent advances in this technology such as the development of a continuous stiffness module (CSM), and variable frequency testing have extended the technique to allow for modulus and hardness determinations of low modulus materials as a function of indenter displacement. The effectiveness of depth sensing nanoindentation has been evaluated for two photopatternable silicone materials of different moduli. Measurements have been conducted on supported 20 μm cured films and cured freestanding bulk samples. The results have been compared to the moduli measured on bulk samples by dynamic mechanical analysis. The close agreement of the DMA and depth sensing moduli provide confidence in using this method for thin film sample analysis.

3:30 PM H9.6
INVESTIGATION OF BARRIER COATINGS ON STAINLESS STEEL FOIL SUBSTRATES FOR HIGH TEMPERATURE POLYSILICON TFT PROCESSING. Sambit K. Saha, Themis Afentakis, Miltiadis K. Hatalis Display Research Laboratory, Department of Electrical and Computer Engineering Lehigh University, Bethlehem, PA; Apostolos Voutsas, Sharp Laboratories of America, Camas, WA.

Thin stainless steel foils present an excellent alternative to polymers substrates for the fabrication of devices and circuits for flexible electronics. A major advantage they offer results from the increased thermal budget tolerance that they provide which enables the utilization of high temperature processes in fabrication and the production of high performance devices and circuits. Commercially available stainless steel foils can be obtained in a variety of thicknesses, but owing to constraints arising from surface roughness and composition in available foils, some modification of the surface is necessary before devices can be fabricated on them. The method of substrate preparation assumes more importance when devices are fabricated at high temperatures, especially in the region of 1000 deg. C. High temperature fabrication processes can adversely affect the integrity of stainless steel-silicon dioxide interfaces and flatness of the substrate surface as well as promote increased diffusion of constituent species of the stainless steel substrate into the device and compromise its performance. Barrier metal layers that prevented constituent species from the surface from diffusing into the fabricated devices were systematically investigated and will be presented in this paper. The efficacy of using various single and multi-level barrier layer structures using metals such as Tungsten, Molybdenum, Tantalum, Titanium and Nickel in preventing diffusion of constituent species into fabricated thin film transistors was analyzed using scanning electron microscopy, energy dispersive spectroscopy and X-ray photoelectron spectroscopy analysis. It was determined that the diffusion of chromium and manganese from the stainless steel played a pivotal role in controlling the quality of the substrate-silicon oxide interface. Both n-channel and p-channel devices have been fabricated on flexible stainless steel foils with barrier coatings. High performance TFT data and characteristics will be presented. The approach presented in this paper constitutes an indispensable first step for the utilization of flexible stainless steel foils for microelectronic fabrication, and is suitable for both low and high temperature processing.

3:45 PM H9.7
FABRICATION OF SILICON OXY-NITRIDE FILM AS A FLEXIBLE DIFFUSION BARRIER LAYER FOR ORGANIC LIGHT-EMITTING DIODE BY RADIO-FREQUENCY MAGNETRON SPUTTERING DEPOSITION. Fu-Lung Wong, Wing-Kwong Wong, S.-Wan Tong, Chun-Sing Lee, Shuit-Tong Lee, Center of Super Diamond and Advanced Thin Films (COSDAF) and Department of Physics and Materials Science, City University of Hong Kong, Hong Kong SAR, CHINA.

Silicon oxy-nitride (SiOxNy) films were deposited on polyethylene terephthalate (PET) substrate by magnetron sputtering deposition. Silicon nitride (Si3N4) was used as the target material. By varying the argon and oxygen flow ratio during deposition, SiOxNy films with different properties were obtained. The optical, electrical, chemical and water barrier properties were evaluated and characterized. The optical transmission of the optimized films can be as high as 96% and the root mean square (r.m.s) surface roughness was 27.48Å. The SiOxNy film showed great potential as a water diffusion barrier for plastic substrates.

4:00 PM H9.8
OPTIMIZATION OF 75°C AMORPHOUS SILICON NITRIDE FOR TFTS ON PLASTICS. Christian McArthur, Mark Meytin, Andrei Sazonov, Univ of Waterloo, Electrical and Computer Engineering Dept, Waterloo, CANADA.

Amorphous silicon nitride (a-SiN_x:H) is widely used as the gate dielectric and passivation layer in a-Si:H based electronics. For devices on plastic substrates deposited at low temperature, the a-SiN_x:H quality seems to determine the device performance. This paper investigates the effects of hydrogen dilution, helium dilution, ammonia-silane gas flow ratio, and RF power on the properties of PECVD silicon nitrides deposited in large-area parallel-plate reactors at substrate temperatures of 75°C. The chemical composition and bonding of the SiN_x:H films was studied using FTIR spectroscopy. The physical properties were investigated, and the density, growth rate, and compressive stress of the films were determined. The electrical properties such as leakage current, breakdown, stability, trap density, and dielectric constant of the films were characterized by I-V and C-V measurements of metal-insulator semiconductor (MIS) structures. Analysis of Variance (ANOVA) was performed on the results, and the deposition conditions for the optimal film properties were determined. The optimum film had SiN_x:H stochiometry of x=1.62 with hydrogen concentrations of 24 at%, and exhibited compressive stress of σ_{comp}= 1.2 ±0.02 GPa. The film displayed good stability under electrical stress with ohmic leakage of R_{leak}= 6.5 ±0.3 $10^{15}\Omega$·cm. Strong relationships between the film properties and deposition conditions were observed, and are discussed within the paper. A-Si:H bottom gate TFTs were fabricated using the optimized nitrides for gate dielectrics and passivation layers, and the influence of a-SiN_x:H on TFT performance is discussed.

4:15 PM H9.9
MICROENCAPSULATION OF POLYMER COATED COLOR PIGMENTS FOR MULTI-COLOR ELECTROPHORETIC DISPLAY. Meyoung Ju Joung, Chul Am Kim, Seong Deok Ahn, Yong Eui Lee, Seung Youl Kang, Mi Kyung Kim, Kyung Soo Suh, Electronics and Telecommunications Research Institute, Daejeon, KOREA; Chul Hwan Kim, DPI Solution, Inc., Daejeon, KOREA.

In this study, we have investigated microencapsulation of red, green, and blue color polymer balls for multi-color electrophoretic display implementation. The charged color pigments have been prepared by physical coating of red, green or blue color balls with functionalized polymer, then surface charging with charge control agent. These color balls were microencapsulated in suspending fluid through in-situ polymerization.

4:30 PM H9.10
CONTROLLING THE CURVATURE OF FLAT FIBERS FOR

E-TEXTILE APPLICATIONS. Eitan Bonderover and Sigurd Wagner, Department of Electrical Engineering, Princeton University, Princeton, NJ; Zhigang Suo, Department of Mechanical and Aerospace Engineering, Princeton University, Princeton, NJ.

In the most fundamental approach, e-Textile circuits will be made by weaving component fibers into circuits. The weaving pattern will determine the circuit function. A key requirement of such e-Textile circuits is reliable electrical contact between fibers. Contacts which rely only on the pressure between fibers are preferred since they preserve the drapability of real fabrics. Since thin-film device fabrication technology is planar, the component fibers, made by the slit-film technique, are flat. Thus a slight edge-to-edge curvature (with a radius of curvature as large as 500mm) can either prevent or promote electrical contact. Using fibers with thin-film transistors of amorphous silicon, we study the processes that produce the desired fiber curvature. A layer of stressed silicon nitride is used to create the curvature. The stress in this layer can be controlled by the deposition parameters. We present a study of this stressed layer and its effect on fiber curvature as well as electrical evaluation of transistor function.

SESSION H10: FLEXIBLE INTERCONNECTS AND DIELECTRICS

Chair: Babu R. Chalamala
Friday Morning, April 25, 2003
Salon 14/15 (Marriott)

8:30 AM H10.1
LASER-CRYSTALLIZED HIGH QUALITY ITO ON PLASTIC SUBSTRATES FOR FLEXIBLE DISPLAYS. Wonsuk Chung, Paul Wickboldt, Dat Toet, Paul G. Carey, FlexICs, Milpitas, CA; Michael O. Thompson, Cornell Univ, Dept of Materials Science and Engineering, Ithaca, NY.

In the study presented here, we successfully demonstrated that high quality ITO films could be obtained on polymeric substrates using excimer laser crystallization. ITO films were first deposited at 10°C on PEN substrates by DC magnetron sputtering, and then irradiated by a homogenized pulsed XeCl excimer laser beam (308 nm, 35 ns pulse duration) in a vacuum chamber. It was possible to reliably attain ITO films with sheet resistances down to 15Ω/sq. combined with more than 80 % transmittance and good etching behavior. Extremely well defined 2 μm ITO lines could be obtained using simple HCl etchant at room temperature. With continued work, the possibility exists to improve these properties further, and we will report on our latest results.

8:45 AM H10.2
EFFECT OF UV IRRADIATION ON THE PHYSICAL/CHEMICAL PROPERTIES OF THE ITO/PES SYSTEM TOWARD OLED-BASED FLEXIBLE DISPLAYS. Byung-Soo So, Jin-Ha Hwang, Jae-Ho Lee, Tae-Sung Oh, and Young-Hwan Kim, Hongik Univ., Dept. of Materials Science and Engineering, Seoul, KOREA.

OLED (Organic Light-Emitting Diodes) have been extensively studied since efficient green emission was demonstrated in a three-layered structure (Indium-Tin-Oxide/organic materials/metal). Since the Indium-Tin-Oxide (ITO) film is in direct contact with organic electroluminescent materials, the physical/chemical properties of ITO are crucial to optimized OLED performance toward OLED-based flexible electronics. The physical properties of ITO thin films strongly depend on the deposition parameters which control microstructure, stoichiometry, and crystallinity, including additional post treatments. The application of ITO as electrodes in OLED devices requires low resistivity (below 1E-3 ohm-cm), low surface roughness (about 1nm) and high transmittance (above 80%). The current work has aimed at improving the physical/chemical features of the ITO/PES system, employing several post annealing processes. The post annealing processes incorporate conventional heating, excimer laser (308nm) annealing and UV (365nm) irradiation on the ITO thin film (100nm) deposited on PES films by low temperature DC magnetron sputtering. Furthermore the effect of oxygen radicals was investigated. The electrical/optical properties were performed using Hall effect, DC 4-point resistance measurement, UV spectrometry, and Ellipsometry. The chemical/microstructural features are characterized by FESEM, XRD, Raman spectroscopy, AFM, and AES/XPS, in terms of morphology, crystallinity, roughness, and stoichiometry. Optimized UV treatment exhibits the enhanced conductivity and smooth surface, compared to that of excimer laser annealing. The role of silicone oxide will be considered as barriers against unwanted impurities. The electrical/optical properties are combined with the chemical/microstructural characterization, which elucidate the underlying mechanism occurring in post treatment concerning UV-irradiation. The ramifications will be made discussed in conjunction with OELD-based materials toward flexible displays.

9:00 AM H10.3
STRETCHABLE GOLD CONDUCTORS ON ELASTOMERIC SUBSTRATES. Catriona Chambers, Stephanie Perichon-Lacour, Sigurd Wagner, Department of Electrical Engineering and POEM, Princeton University, Princeton, NJ; Zhigang Suo, Department of Mechanical and Aerospace Engineering, Princeton University, Princeton, NJ.

3-D displays, sensor skins, mechatronic structures, and e-textiles will rely on flexible and stretchable electronic circuits. It is likely that such circuits will be made of rigid semiconductor islands interconnected with stretchable metallization. However, free-standing metal films fracture at tensile strains in the order of one percent, well short of the ten-percent extension needed for deformable circuits. We have discovered that flat metal lines made on an elastomeric substrate can be stretched by ten percent without losing electrical conduction. A free-standing metal film fractures by localized plastic deformation, e.g., by forming a shear band. By suppressing this localization the elastomer substrate allows delocalized plastic deformation. We fabricated 1-mm thick poly-dimethylsiloxane (PDMS) membranes with up to 100-nm thick, 1-mm wide gold lines deposited by electron beam evaporation. Then we evaluated the structure of the gold films by optical and scanning electron microscopy, and measured the electro-mechanical characteristics in a strain tester, with contact electrodes applied to the film. We find that 50-nm thick lines retain their electrical conduction up to 10 percent strain. Also, when the tensile strain is cycled between 0 and 5 percent, the electrical resistance in the stressed and relaxed states are reproducible. We will describe substrate and conductor preparation, and their structural, mechanical, and electrical properties. Key words: elastic, stretchable, gold film, PDMS, electrical conduction.

9:15 AM H10.4
A COMPARATIVE STUDY OF ADHESION PROPERTIES OF METAL FILMS ON POLYIMIDE SUBSTRATES TREATED BY VARIOUS PLASMA TREATMENT TECHNIQUES. Soo Hong Kim, Young Sik Lee, Su Hyeon Cho, Nae-Eung Lee, and Hun Mo Kim[a], Dept of Materials Engineering, Center for Advanced Plasma Surface Technology, and Intelligent Micro-Systems, Sungkyunkwan University, Suwon, Kyunggi-do, KOREA. [a]Dept of Mechanical Engineering and Intelligent Micro-Systems, Sungkyunkwan University, Suwon, Kyunggi-do, KOREA.

With an increase in the use of polyimides(PI) for applications in the flexible electronics, the techniques of surface treatments to enhance polymer-to-metal adhesion are becoming more and more important. Especially, plasma surface treatments to improve the adhesion of metal/PI are very useful in realizing required flexibility of metallization lines formed on the flexible substrates in developing flexible electronic devices. In this study, we investigated adhesion properties of Cu/Cr/polyimide(PI) systems by varying surface treatment conditions using various plasma treatment techniques such as microwave, atmospheric plasma, and inductively coupled plasma (ICP). O_2 and Ar plasma treatments of PI substrates are followed by the sputter deposition of 150-nm-thick Cr. Cr is used as an adhesion layer between Cu seed layer and PI films. After the deposition of the Cu seed layer of 200 nm, Cu electroplating was performed on the Cu seed layer. The characterization of the PI film surfaces treated by O_2 and Ar plasmas was carried out by atomic force microscopy (AFM), contact angle measurements, and X-ray photoelectron spectroscopy (XPS). The chemical interaction between Cr and plasma-treated PI films was investigated by XPS. The adhesion properties in Cu/Cr/polyimide(PI) systems will be discussed.

9:30 AM H10.5
EDGE AND SLIP COVERAGE BY METAL INTERCONNECTS FOR THREE DIMENSIONAL CIRCUITS. Rabin Bhattacharya, Sigurd Wagner, Princeton University, Dept of Electrical Engineering, Princeton, NJ; Min Huang and Zhigang Suo, Princeton University, Dept of Mechanical and Aerospace Engineering, Princeton, NJ.

Three-dimensional integrated circuits is a new and exciting field that has been spurred on by the need for conformal displays and detector arrays. These circuits are fabricated by interconnecting rigid sub-circuit islands made on a flat, deformable substrate. To prepare for interconnects, we apply a patterned deformable sacrificial material over the flat substrate. We then deform the substrate, with the sub-circuit islands and sacrificial pattern on it, to a spherical surface. Following deformation, we evaporate interconnect metal and then lift-off the sacrificial material, leaving only the metal lines that interconnect the islands. The maximum size for a circuit island to remain intact increases with the islands thickness. The larger the island has to be, the thicker it must be made to prevent it from cracking. We have found that 40 micrometer square islands must be at least 0.5 micrometers thick. With such thick islands, edge coverage by interconnect metal becomes difficult because of the three-dimensional

nature of the substrate. Using planetary rotation evaporation, we have achieved a maximum yield of 73% for 10 micrometer wide aluminum lines going over 0.9 micrometer thick islands. The resistances of 4.7 millimeter long line sections varied from 67 ohms to 1280 ohms; the design requirement for this line resistance is 100 ohms. The primary cause of yield loss and excessive line resistance is island-substrate delamination that occurs by slip along the substrate-island interface during deformation. At the top of the hemisphere, which experiences a substrate strain of 5 to 6 percent, the substrate slips by 560 nanometers. We are developing metallization that covers both edge and slip, and will report experiments and results. Keywords: Kapton, Metal Interconnects, Edge Coverage, Deformable Electronics, Thin Film Delamination.

9:45 AM H10.6
FLEXIBLE ORGANIC LIGHT-EMITTING DEVICE BASED ON LOW TEMPERATURE MAGNETRON SPUTTERED INDIUM TIN OXIDE ON PLASTIC SUBSTRATES. Fu-Lung Wong, Man Keung Fung, Chun Sing Lee, Shuit Tong Lee.

A low temperature radio-frequency (R.F.) sputter deposition method was applied to prepare indium tin oxide (ITO) on a plastic substrate (Polyethylene terephthalate, PET). The deposited specimen was transferred to a vacuum chamber for fabricating flexible organic light-emitting device (FOLED). ITO films with an average transmittance of over 90% over the visible wavelength (400-700nm) and a resistivity of 5.0x10e-4ohm/sq.cm were obtained. alpha-napthylphenylbiphenyl diamine (NPB), tris-(8-hydroxyquinoline) aluminium (Alq) and magnesium-silver (MgAg) were sequentially and thermally deposited on the ITO-PET substrate for FOLEDs. Among the fabricated devices, the best one had a maximum current efficiency of 4.1cd/A and a luminance of 4100cd/m2 at 100mA/cm2. These results are comparable with that of conventional glass-based OLED devices with the same device configuration.

10:30 AM *H10.7
LOW TEMPERATURE MATERIALS AND DEVICES FOR a-Si:H BASED ELECTRONICS ON PLASTIC SUBSTRATES.
Andrei Sazonov, Mark Meytin, Christian McArthur, Denis Stryahilev, Arokia Nathan, Univ of Waterloo, Electrical and Computer Engineering Dept, Waterloo, CANADA.

Amorphous hydrogenated silicon (a-Si:H) technology is considered today as the most effective practical solution for electronics on plastics due to its low capital cost, availability, mature state of both materials and device physics and technology, large area capability and wide variety of materials and their properties that can be achieved. To combine the advantages of this technology with inexpensive, low thermal budget plastic substrates, the reduction of deposition temperature to about 100°C is required. In standard a-Si:H technology, such a decrease results in poor electronic properties of materials and devices. In this paper, we present our results on materials optimization and TFT fabrication at 120°C and 75°C, the temperatures compatible with polyethylene naphthalate (PEN) and polyester (PET) substrates, respectively. a-Si:H, a-SiN_x:H and a-SiO_x properties were optimized, and TFTs were fabricated on glass and plastic substrates at maximum processing temperatures of 120°C and 75°C, respectively. In all experiments, industrial parallel-plate PECVD deposition system (PlasmaTherm 780 series) with 14″ by 14″ electrode area was used to prove our deposition capability over large area. At 120°C, TFTs show effective field effect mobility of 0.5 cm^2/V's and 0.8 cm^2/V's for channel length of 25 μm and 100-200 μm, respectively, which complies with the OLED driving requirements. The dependence of TFT performance on the materials and deposition conditions is discussed.

11:00 AM H10.8
DIELECTRIC PROPERTIES OF LAYERED POLYMER FILMS.
C.K. Chiang, Polymers Division, National Institute of Standards and Technology, Gaithersburg, MD; W. Sakai and N. Tsutsumi, Department of Polymer Science and Engineering, Kyoto Institute of Technology, Kyoto, JAPAN.

The dielectric properties of polymer film are important parameters in the design of flexible electronics. In this study, we measured the thickness dependence of the dielectric constant of various polymer thin films using single layered films, and also using three-layer structured films. For the three-layer structured film, the two outer layers were about one microns and the thickness of middle layer was varied. The results were evaluated with a simple serial three-capacitance model. The results were compared with those expected from bulk data.

11:15 AM H10.9
MICRO-SCALE Cu METALLIZATION ON FLEXIBLE POLYIMIDE SUBSTRATE BY Cu ELECTROPLATING USING SU-8 PHOTO-RESIST. Su Hyeon Cho[a], Soo Hong Kim[a], Young Sik Lee[a], Nae-Eung Lee[a] and Hun Mo Kim[b]. [a]Dept. of Materials Engineering and Center for Advanced Plasma Surface Technology, Sungkyunkwan University, Suwon, Kyunggi-do,KOREA; [b]Dept. of Mechanical Engineering and Intelligent Micro-Systems, Sungkyunkwan University, Suwon, Kyunggi-do, KOREA.

Technologies for flexible electronics have been developed to make electronic or electro-mechanical devices on inexpensive and flexible organic substrates. In order to interconnect device elements or layers, metallization on the flexible substrate is required. In this case, the width and conductivity of metallization line is very important for minimizing the size of device. The realization of metallization process with a few micrometer scale on the flexible substrate is required. Compared to the conducting polymer lines with high electrical resistivity, the metal lines with low electrical resistivity are desirable for the realization of micro-scale devices. In this work, micro-scale metallization lines of Cu were fabricated on the flexible substrate by electroplating using the patterned mask of SU-8 2010. SU-8 is negative tone, chemically amplified near UV photo-resist. Cr is used as an adhesion layer between the Cu seed layer and the polyimide for the enhanced adhesion between Cu and polyimide films. Electroplating of copper line was carried out as a function of temperature in the bath and current density on the surface. Cu lines with the width of 2∼4μm and the aspect ratio of 2∼3 were fabricated. We used dry plasma processes to remove the SU-8 mask. The flexibility and adhesion property of Cu line (electroplated)/ Cu(seed)/Cr/Polyimide are evaluated and discussed.

11:30 AM H10.10
Abstract Withdrawn.

11:30 AM H10.10
DEVELOPMENT OF HIGH PERMEABILITY CORE MATERIAL FOR EMBEDDABLE SOLENOID INDUCTORS IN FLEXIBLE ORGANIC SUBSTRATES. C.K. Liu, P.L. Cheng, S.Y.Y. Leung, T.W. Law, I.T. Chong and D.C.C. Lam, Department of Mechanical Engineering, Hong Kong University of Science and Technology, Hong Kong SAR, CHINA.

Capacitors, resistors and inductors are surface mounted components on circuit boards, which occupy up to 70% of the board area. For selected applications, these passives are embedded inside green ceramic tape substrates and sintered at temperatures over 700 degC in co-fired process. These high temperature fabrication processes are incompatible with organic substrates, and low temperature processes are needed if passives are to be embedded into organic substrates. In this study, embedded cored 3-D solenoid inductors with high permeability core in flexible organic substrates were fabricated. A new high permeability dual-phase Nickel Zinc Ferrite (DP NZF) core fabricated using a low temperature sol-gel route was developed for insertion into solenoid inductors in organic substrates. Crystalline NZF powder was added to the sol-gel precursor of NZF. The solution was deposited onto the substrates as thin films and heat-treated at varied temperatures. The changes in the microstructure were characterized using XRD, TGA and DTA. Results showed that addition of NZF powder induced low temperature transformation of the sol-gel thin film NZF phase to high permeability phase at 250degC, which is approximately 350degC lower than transformation temperature for unseeded NZF thin films. Electrical measurement of DP NZF cored solenoid inductors indicated that the inductance increased by 30X - 100X compared to inductors without the DPNZF cores. The relation between the increase in inductance and connectivity in the microstructure is discussed and compared with composite electrical properties models.

11:45 AM H10.11
HIGHLY CONDUCTIVE AND TRANSPARENT Ti-DOPED ZINC OXIDE THIN FILMS. Yang-Ming Lu, Shu-I Tsai, Chen-Min Chang, Kun Shan University of Technology, Department of Electronic Engineering, TAIWAN, R.O.C.

Highly conductive and transparent impurties-doped zinc oxide thin films have recently gained much attention because they are composed of inexpensive, abundant materials. The Ti doped ZnO thin films were deposited by simultaneously magnetron co-sputtering from both Zn and Ti targets in a mixture of oxygen and argon gases onto heated Corning 7059 glass substrates.By adjusting the Ar/O2 ratio and other process parameters including RF power, and substrate temperature, the electrical property of ZnO thin films change from an isolation to a good conduction. The results show that deposition rate is an approximately linear function of DC power of Ti target except at 300 watts. At 300watts, the growth rate decreases may due to strong interference between zinc and titanium sputtered atomic fluxes.The incorporation of titanium atoms into zinc oxide films is not effective until the Ti target power increased to a value of 250watts.The atomic percents of titanium in the films are measured to be 1.33% and 2.51% correspond to 250watts and 300watts of Ti target power applied

respectively. The XRD patterns shown only a single ZnO phase existing and shifted to lower 2 theta values imply Ti atoms incorporated into the ZnO lattice and occupy the zinc atoms lattice sites.The reistivity of undoped ZnO films is extremely high and decrease to a value of 3.78 - 10-2 ohm-cm when 2.51% atomic percent of Ti is incorporated. All of the zinc oxide films show good transmittance in the range of 4000-7000 A.The average transmittance is 70-80% in this study. The optical energy gap increases with increasing the doping amount of Ti in the films. The maximum value of optical energy gap gained in this study is 3.18 eV when the doping amount of Ti is 2.5 atomic %.

SESSION H11/L12: JOINT SESSION
DEVICES
Chair: Jerome Cornil
Friday Afternoon, April 25, 2003
Salon 1-3 (Marriott)

1:30 PM *H11.1/L12.1
PRINTING APPROACHES TO ORGANIC OPTOELECTRONICS ON PLASTIC, TEXTILE AND PAPER SUBSTRATES. Y. Yoshioka and G.E. Jabbour, Optical Sciences Center, The University of Arizona, Tucson, AZ.

The latest developments in the use of inkjet printing as a tool to pattern a given electrode promises in a maskless non-contact approach to generate a specific pattern on given substrate. Many factors including surface tension of the printed solution, substrate surface properties, and moisture have direct effect on the final quality and performance of the organic based devices. Issues related to device fabrication on plastic, textile and paper substrates will be discussed and results of tested devices will be presented.

2:00 PM *H11.2/L12.2
FULLY PRINTABLE LIGHT EMITTING DISPLAYS. Sue A. Carter, M. Kreger, J. Leger, Y. Nakazawa, J.J. Breeden, M. Wilkinson, University of California, Dept. of Physics, Santa Cruz, CA and Add-vision, Incorporated, Scotts Valley, CA.

One of the main promises of semiconducting polymers is the ability to manufacture inexpensive optoelectronic components that will lead to the wide-scale use of new technologies, such as large area light-emissive displays and photovoltaics. This vision relies on being able to manufacture semiconducting polymers using very inexpensive manufacturing processes where the labor and processing costs can be considerably less than the materials cost. In this talk, I will give an overview of the technical and cost considerations for making polymer displays and detectors where all layers are deposited under atmospheric conditions using a liquid-based manufacturing technique, such as ink-jet, screen-printing or web-based processes. I will discuss our work on fully screen-printed light emitting polymer displays with focus on the technical challenges in printing the light emitting polymer layer, printing the top electrode (cathode), and obtaining sufficient lifetimes and power efficiency on plastic substrates under such manufacturing conditions. I will conclude by showing our most recent results and prototypes of fully printed light emitting polymer displays.

2:30 PM H11.3/L12.3
IN-SITU ELECTRICAL AND SPECTROSCOPICAL STUDY OF DEGRADATION MECHANISMS AND LIFE TIME PREDICTION OF ORGANIC BASED ELECTRONIC MATERIAL SYSTEMS. Jean Vittorio Manca, Els Kesters, Laurence Lutsen, Ludwig Goris, Dirk Vanderzande, Jan D'Haen, Marc D'Olieslager, Luc De Schepper, Limburg Universitair Centrum, Institute for Materials Research, Diepenbeek, Belgium, IMEC, Division IMOMEC, Diepenbeek, BELGIUM; Ornella Sanna, University of Cagliari, Cagliari, ITALY.

In order to tailor the synthesis of new robust organic materials for electronic applications it is of key importance to understand the underlying degradation mechanisms. The strategy used by our group to study these mechanisms is to monitor the behavior of the materials submitted to a given stress conditions with so-called in-situ electrical and spectroscopical techniques and to subsequently use analytical techniques to determine the failure mode, degree of degradation and nature of morphological changes. This approach will be illustrated for several new polymer conductors and semiconductors in films and in light emitting devices. The in-situ electrical measurement technique was developed by our institute for a high resolution study of the electrical characteristics and ageing behavior of a given material during thermal annealing, as a function of temperature, time, etc. With this technique, a test structure is submitted to a desired temperature profile and atmospheric conditions, and the electrical property of interest is measured continuously during the treatment, i.e. in-situ. For the in-situ spectroscopical studies (in-situ IR and UV/VIS), a thermoregulated oven is used in which polymers can be analyzed against temperature and under various atmospheres as free standing films by means of an appropriate measurement cell. Films are heated following the temperature profile of choice and data are collected with a high rate. It will be shown that with these techniques activation energies can be determined for the elimination/polymerization mechanisms and the degradation mechanisms can be monitored during linear heating experiments and during isothermal treatments. With the presented in-situ techniques, the degradation kinetics can be studied under a matrix of degradation stress parameters, allowing the construction of a kinetic degradation model. Such a model is required in order to make a correct prediction of the degradation under operational conditions, based on the degradation data obtained under accelerated ageing conditions.

2:45 PM H11.4/L12.4
FABRICATION OF ORGANIC LIGHT-EMITTING DEVICES BY LOW PRESSURE COLD WELDING. Changsoon Kim and Stephen R. Forrest, Dept of Electrical Engineering, Princeton Univ, Princeton, NJ.

We demonstrate a method for high resolution patterning of metal cathode contacts for organic electronic devices using low pressure cold welding. The contacts are formed by transferring a metal film from a patterned, soft elastomeric stamp onto unpatterned organic and metal layers predeposited onto a substrate. Use of an elastomeric stamp allows for a thousand-fold decrease in the pressure needed for a high-yield pattern transfer as compared to that required with rigid stamps[1].
In our demonstration, we fabricate an array of efficient organic light emitting devices (OLEDs) based on the green phosphor *fac* tris(2-phenylpyridine) iridium [Ir(ppy)$_3$] doped into a 4,4′-N,N′-dicarbazole-biphenyl (CBP) host. Here, the cathodes consist of ultrathin (< 1 nm) layers of LiF and Al capped by a 15-nm-thick layer of Au deposited across the entire organic layer surface. A 100-nm-thick layer of Au is transferred onto the Au layer by pressing a stamp onto the substrate using a conventional semiconductor flip-chip bonder. The cathode patterning is finished by removing the thin Au layer between the transferred patterns by gentle sputter etching. The 200-μm-diameter cathodes were uniformly obtained over the whole substrate area with a yield exceeding 97%, and the pattern edge resolution was approximately 1 μm. The stamping and Au layer removal processes do not adversely affect the performance of OLEDs fabricated by conventional shadow mask patterning. For example, the voltage corresponding to a current density of J = 10 mA/cm^2 was (9.2 $\pm$0.3) V, and the external quantum efficiency at J = 1 mA/cm^2 were (6.0 $\pm$0.3)% for both stamped and control devices. This technique is potentially suitable for roll-to-roll fabrication of a wide range of organic electronic devices including OLEDs, organic thin-film transistors, and photovoltaic cells.
[1] C. Kim, M. Shtein, and S.R. Forrest, Appl. Phys. Lett. 80, 4051 (2002).

3:30 PM *H11.5/L12.5
PROGRESS IN THE GROWTH OF PENTACENE THIN FILMS AND DEVICES. Ruud Tromp, IBM T.J. Watson Research Center, Yorktown Heights, NY.

Recently, the growth of pentacene thin films on a variety of substrates has become of interest to the surface and interface science community. For instance, careful preparation of the substrate allows the pentacene thin film grain size to be increased very significantly.
In this talk I review recent results on the growth of pentacene films on semiconductor, insulator, and metal surfaces.

4:00 PM H11.6/L12.6
SELF-ALIGNED VERTICAL CHANNEL POLYMER FIELD-EFFECT TRANSISTORS. Natalie Stutzmann, Richard H. Friend, Henning Sirringhaus, Cavendish Laboratory, University of Cambridge, Cambridge, UNITED KINGDOM.

Manufacturing of high-performance conjugated polymer transistor circuits on flexible, plastic substrates requires patterning techniques capable of defining critical features with submicrometer resolution. We demonstrate here the use of solid-state embossing to produce polymer field-effect transistors with submicrometer critical features in planar and vertical configurations. Embossing is used for the controlled microcutting of vertical sidewalls into polymer multilayer structures without smearing. High-mobility vertical-channel polymer field-effect transistors on flexible poly(ethylene terephthalate) substrates have been fabricated, in which the critical channel length of 0.7-0.9 mm is defined by the thickness of a spin-coated insulator layer. We demonstrate that gate electrodes can be self-aligned to minimize overlap capacitance by inkjet printing using the embossed grooves to define a surface-energy pattern.

4:15 PM H11.7/L12.7
INKJETTED ORGANIC TRANSISTORS USING A NOVEL PENTACENE PRECURSOR. Steven K. Volkman, Steven Molesa, Brian Mattis, Paul C. Chang, and Vivek Subramanian, University of California, Berkeley, Department of Electrical Engineering and Computer Sciences, Berkeley, CA.

Pentacene is one of the most promising organic materials for organic transistor fabrication, since it offers higher mobility, better on-off ratios, improved environmental stability, and better reliability than most other common organic semiconductors. However, its severe insolubility renders it useless for the solution-based fabrication of electronic devices. Solution-based processing of these devices is the key to enabling ultra-low-cost circuit fabrication, since it eliminates the need for lithography, subtractive processing, and vacuum-based film deposition. Because it allows the use of entirely additive printing techniques, it is expected to result in the development of low-cost reel-to-reel fabrication methodologies. Prompted by a recent paper from Afzali et al describing the synthesis of a novel pentacene precursor, we demonstrate the first inkjet-printed pentacene transistor fabricated to date. This is achieved using a substrate-gated transistor structure in conjunction with an inkjet-printed pentacene precursor active layer. A subsequent thermal cycle is used to convert the precursor into a high-quality pentacene film. Unoptimized conditions yield transistors with an on-off ratio of >1,000 and a field-effect mobility of 0.001cm2/V-s. Further improvement is expected with optimization, to approach the mobility of >0.5cm2/V-s reported by Afzali. We study the effect of annealing conditions on the pentacene precursor characteristics, and establish qualitative models describing the various effects. The precursor is converted to pentacene via heating, through the decomposition of the Diels-Alder product. As the anneal temperature increases above 120C, performance increases dramatically. The process is therefore compatible with numerous low-temperature plastics. As the anneal time is increased to several minutes, performance likewise increases through increased precursor decomposition. However, exposure to excess temperatures or times tends to degrade performance. This is caused by morphological and chemical changes in the pentacene film.

4:30 PM H11.8/L12.8
N- AND P-TYPE BUILDING BLOCKS FOR ORGANIC ELECTRONICS BASED ON OLIGOTHIOPHENE CORES. Antonio Facchetti, Melissa Mushrush, Howard E. Katz, and Tobin J. Marks.

Organic semiconductors exhibiting complementary-type carrier mobility are the key components for the development of the field of "plastic electronics". We present here a novel series of α,ω- and isomerically pure β,β'-diperfluorohexyl-substituted thiophene oligomers [DFH-nTs and isoDFH-nT, respectively; C_6F_{13}-(thiophene)$_n$-C_6F_{13}; n = 2 - 6] and study the impact of fluoroalkyl substitution and conjugation length vìs-à-vìs the corresponding fluorine-free analogues [DH-nTs and isoDH-nT; C_6H_{13}-(thiophene)$_n$-C_6H_{13}; n = 2 - 6]. Trends between the fluorinated and fluorine-free families in molecular packing, optical absorption, HOMO-LUMO gap, and p-p interactions are found to be strikingly similar. However, fluoroalkyl substitution substantially enhances thermal stability, volatility, and electron affinity. Thin film transistor (TFT) devices were fabricated employing both vacuum- and, for shorter and β,β'-substituted oligomers, solution-deposited semiconducting layer. Field-effect transistor measurements indicate that all the longer members of both DFH-nT and isoDFH-nT series are n-type semiconductors with unoptimized mobilities and I^{on}:I^{off} ratios approaching 0.05 $cm^2/(Vs)$ and 10^5, respectively. These families represent the first example of a homologous series of variable core π-conjugation length n-type OTFT components.

4:45 PM H11.9/L12.9
NON-CONVENTIONAL DEVICES USING HIGH-RESOLUTION RUBBER STAMPS. Jana Zaumseil, John A. Rogers, Vikram C. Sundar, Yueh-Lin Loo, Zhenan Bao, Bell Laboratories, Lucent Technologies, Murray Hill, NJ.

Recent interest in the science and emerging applications of electro-active organic and bio-organic materials motivates research into non-invasive methods for forming high resolution electrical contacts on these classes of "soft", molecular materials. Many of the lithographic techniques that were developed for traditional microelectronic systems require processing protocols that are too severe for these organics. We have developed a soft-contact lamination approach using metal-coated elastomeric stamps that provides a convenient and non-invasive way of probing organic materials. This method exploits the surface relief of elastomeric stamps to define, with nanometer resolution, the geometry and separation of electrodes that are formed by directional deposition of thin metal films onto the stamps. Soft contact of these metal-coated stamps with the organic non-invasively establishes multiple independent electrical connections. As proof of concept we demonstrate successful fabrication of top-contact thin film transistors with channel lengths between 250 microns and 150 nanometers on pentacene and FCuPC. Advantages of this approach include a reversible contact that can be established at room temperature without the application of pressure or adhesives etc. that are generally used with traditional lamination or wafer bonding methods. This procedure provides a powerful tool for studying the physics of charge transport in chemically fragile or ultrathin soft materials. We use this method to investigate fundamental interface and contact properties between metal electrodes and organic semiconductors. By comparing the laminated contacts to conventional ones formed by thermal evaporation, it is possible isolate the electrical effects of depositing hot metal onto organic semiconductors.