SYMPOSIUM B

High-Mobility Group-IV Materials and Devices

April 12 - 15, 2004

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TUTORIAL

Strain in SiGe/Si Heterostructures
Monday April 12, 2004
1:30 PM - 5:00 PM
Room 2004 (Moscone West)

The tutorial will cover the basics of strain and stress in lattice mismatched heterostructures, the influence of strain on the electronic band structure, the consequences on optical and transport properties and the directions and prospects of device realizations. The tutorial is composed of the following topics which for each include background information, model assumption, results and outlook.

- Lattice mismatch and stress / strain distribution
- Critical thickness and metastability of layers
- Morphology and island / quantum dot formation
- Strain adjustment methods with emphasis on integrated circuits application
- Electronic band ordering of tensile and compressive strained Si/SiGe.
- Mobility enhancement in strained quantum wells
- Hetero CMOS concepts: history, status, prospects

Instructors:
Klara Lyutovich, Universtat Stuttgart
Jim Sturn, Princeton University

SESSION B1: Strained Si and SRBs on Bulk Si
Chairs: Matty Caymax and Eugene Fitzgerald
Tuesday Morning, April 13, 2004
Room 2004 (Moscone West)

8:30 AM *B1.1
Improving MOS with Engineered Semiconductor Substrates. Eugene Arthur Fitzgerald, Materials Science and Engineering, MIT, Cambridge, Massachusetts.

As with any technology value chain, optimization of silicon-based microelectronics has occurred through a process of value migrating from initial materials breakthroughs, up through device engineering, to desgin tool and circuit design optimization. In the last 20 years or so, commoditization of particular levels in the value chain was critical to progress in the industry (e.g. Si substrates). However, for further progress, we need to find new advances in previously commoditized areas. Great progress in research and development of engineered semiconductor substrates has introduced an intriguing possibility that further gains in integrated circuit products can be accomplished by inserting engineered substrates into the current Si manufacturing infrastructure. In this talk, we will review the plethora of strained SiGe heterostructures we have fabricated, from material growth to evidence of greatly improved channel transport in experimental MOSFETs. In general, electron transport and hole transport are maximized on intermediate alloy concentrations (50% Ge), as tension in Si-rich materials increases electron mobility and compression in Ge-rich material increases hole mobility. Time permitting, we will review current commercialization trends and speculate about future absorption of these engineered substrates into the semiconductor industry.

9:00 AM *B1.2
Selective) Epitaxial Growth of Strained Si to Fabricate Low Cost and High Performance CMOS devices. Roger Loo[1], Romain Delhougne[1], Philippe Meunier-Beillard[2], Matty Caymax[1], Peter Verheyen[1,3], Geert Eneman[1,3], Ingrid De Wolf[1], Alessandro Benedetti[1], Kristin De Meyer[1,3], Wilfried Vandervorst[1,3] and Marc Heyns[1]; [1]IMEC, Leuven, Belgium; [2]Philips-Research Leuven affiliated to IMEC, Leuven, Belgium; [3]ESAT-INSYS, K.U. Leuven, Leuven, Belgium.

CMOS performance can be improved by introducing tensile strained Si in the active device areas. The saturation drive current is increased due to strain induced electron and/or hole mobility enhancement. One possible way to obtain strained Si is the use of a Strain Relaxed SiGe Buffer (SRB). However, important integration issues have to be solved before SRBs can be implemented in CMOS. First, current SRB fabrication techniques are mainly based on blanket wafers, which complicate current isolation techniques. Second, the material quality of SRBs with $\geq$30 % Ge has to be improved to avoid yield issues. Such high Ge contents are needed to improve pMOS performance by using strained Si. The lowest threading dislocation density has been reported for thick SRB layers. Nevertheless, a lot of effort has been invested to create thin SRBs, because thick SRB structures suffer from disadvantages like high cost, issues with STI formation in the thick SiGe structure and self-heating effects. After a short overview of existing SRB fabrication techniques, their benefits and drawbacks, a new type of thin SRBs (200 nm), prepared by means of Chemical Vapor Deposition epitaxy is presented. All processes are developed in ASM's Epsilon epitaxial reactor. The incorporation of a thin carbon containing layer into a constant composition SiGe layer decreases the energy barrier for dislocation nucleation and provides nucleation centers for dislocations. Beside fabrication of blanket substrates with strained Si, this process permits also selective epitaxial growth (SEG) of both the SRB layer and the strained Si cap-layer on the active areas of patterned wafers. The combination of in-situ Chemical Vapor Etch and epitaxial re-growth allows the implementation of SRB layers in CMOS flows, without the need of CMP and without modifications of the standard STI process. This simplifies the integration of strained Si into the standard CMOS technology. Our SRB exhibits a high degree of relaxation (up to 90%), a RMS roughness below 1 nm and a density of threading dislocations around $1x10^6$ cm^{-2}. The material quality is comparable for layers grown on blanket wafers or selectively grown on patterned wafers. Similar device characteristics have been observed for the two different routes, which do show improved device performance for strained Si layers. The 75% higher electron mobility leads to an enhancement of the transconductance, which is 75% for L_g=10 μm and 25% for L_g=0.3μm.

9:30 AM B1.3
Defect-Free Strained Si-on-Insulator Fabricated from Free-Standing Si/SiGe Structures. Patricia M Mooney[1], Guy M Cohen[1], Huajie Chen[2], Jack O Chu[1] and Nancy R Klymko[2]; [1]IBM TJ Watson Research Center, Yorktown Heights, New York; [2]IBM Microelectronics Division, Hopewell Junction, New York.

Several different blanket pseudomorphic $Si_{0.8}$ $Ge_{0.2}$/Si layer structures, grown either by RTCVD or UHVCVD, were etched to form 5μ m X 5μ m elastically strain-relaxed free-standing SiGe/Si structures, supported by a single pedestal at the center. Examples include SiGe layers on bulk Si substrates and SiGe or SiGe plus Si layers on SOI substrates. Free-standing SiGe layers supported by a crystalline Si pedestal were essentially flat and were shown by x-ray diffraction measurements to be 100% relaxed, except where supported, independent of the SiGe layer thickness. Bi-layer SiGe/Si structures supported by a SiO_2 pedestal showed a high degree of curvature, as predicted. Symmetric tri-layer structures, 20nm Si/236nm $Si_{0.8}$ $Ge_{0.2}$ 20nm Si supported by a SiO_2 pedestal, are essentially flat. X-ray diffraction measurements of the strain and the thickness of the layers confirmed that the strain is shared between the Si and SiGe layers according to a force balance model, as was found for $Si_{0.8}$ $Ge_{0.2}$ grown epitaxially on free-standing Si [1,2]. We thus have fabricated defect-free Si layers under biaxial tensile strain, ϵ = 0.0069. The tri-layer structures were then firmly attached to the substrate using various filling materials. For example, a thermal oxide layer was grown on the upper and lower surface of the free-standing structures and then polycrystalline Si was deposited so as to fill the space between the free-standing structure and the Si substrate, thus attaching the lower strained Si layer to the substrate. The polycrystalline Si lying on top of the structures was subsequently removed by reactive ion etching. The upper SiO_2 and Si layers as well as the SiGe layer were then removed selectively by wet etching. Raman spectroscopy measurements show that the strain in the attached strained Si-on-insulator layer is ϵ = 0.0072. 1. G.M. Cohen, P.M. Mooney, J.O. Chu, Mat. Res. Soc. Symp. Proc. **768**, 9 (2003). 2. P.M. Mooney, G.M. Cohen, J.O. Chu and C.E. Murray, submitted to Appl. Phys. Lett.

9:45 AM B1.4
Ultra-Thin Strain Relaxed SiGe Buffer Layers With 40 Percent Ge. K. Lyutovich, E. Kasper and M. Oehme; Institute of Semiconductor Engineering, University of Stuttgart, Stuttgart, Germany.

Carriers in Si channels under tensile strain are notable for high mobilities due to lower effective mass and reduced intervalley scattering. The consequently enhanced performance of strained-Si-based devices excites considerable interest in such systems (catchword: strained Si). To yield the necessary tensile strain in the Si channel, a virtual substrate consisting of a standard Si substrate with a strain relaxed SiGe buffer layer on top of it offers an appropriate solution. The ability of virtual substrates to adjust the strain between the Si substrate and the layers in heterostructures is now widely acknowledged but their quality and integration ability still do not meet all requirements. We report about ultra-thin SiGe layers with 40 percent Ge emphasizing their high degree of relaxation and surface smoothness. These parameters as well as ultra-low thickness are crucial for buffer-layer application in virtual substrates for the adjustment of high strain values (up to 1.7 percent strain) in integrated circuits on Si. A purposely developed method is employed for the growth of virtual substrates with ultra-thin strain relaxed buffers in a solid source MBE system with in situ growth monitoring.

The thickness of SiGe buffer layers is kept below 100nm and mainly chosen in the range between 40 and 80nm. The degree of relaxation of buffers grown by used method is tunable between the pseudomorphic growth (fully strained SiGe layer) and the full relaxation of them, causing tensile strain in the following Si channel. Characterization of the strain and of the degree of relaxation is performed by means of micro-Raman spectroscopy and confirmed by X-ray diffraction. Surface morphology is studied using optical, scanning electron and atomic force microscopy. High surface smoothness without cross-hatch pattern is demonstrated by high resolution atomic force microscopy. The particularly desired absence of cross-hatch pattern is related to the specific growth procedure utilizing the introduction of point defects. Test MODFET structures processed on these virtual substrates confirm their device quality and the great potential for high frequency application.

10:00 AM B1.5
Defects in strained-Si layers. Stephen W. Bedell[1], Devendra Sadana[1], Keith Fogel[1], Huajie Chen[2] and Anthony Domenicucci[2]; [1]Research, IBM, Yorktown Heights, New York; [2]Microelectronics Division, IBM, Hopewell Junction, New York.

Defects in strained-Si layers formed on relaxed SiGe alloy layers (on both bulk-Si and SGOI substrates) are investigated using a novel defect etching method. A population of isolated etch pits and planar defects is observed. The relative fraction of planar defects to isolated etch pits is found to increase with increasing Ge content in the SiGe alloy layer. The etching data combined with TEM analysis suggests that the formation of stacking faults during the relaxation of SiGe layers becomes favored at higher Ge concentrations.

10:30 AM *B1.6
The use of ion implantation and annealing for the fabrication of strained silicon on thin SiGe virtual substrates.
Siegfried Mantl, Institute of Thin Films and Interfaces (ISG) and cni-center of nanoelectronic systems for information technology, Forschungszentrum Juelich, Juelich, Germany.

Strained silicon will be used as a channel material in the next generations of CMOS devices. The enhancement of the carrier mobility of the tetragonally distorted silicon allows a considerable improvement of the device performance. In this contribution an overview will be given on the fabrication of strained silicon on thin strain relaxed SiGe buffer layers formed by ion implantation and annealing of pseudomorphic SiGe layers. For this purpose we preferably use H or He ions, but we will present also first results using heavier ions. The epitaxial SiGe layers were grown either by CVD or MBE. After ion implantation the samples are annealed at temperatures around 850 C for several minutes during which the strain relaxation occurs. The key issue of this process is the formation of internal dislocation sources, which promote the strain relaxation. By this way relaxed SiGe layers with a very small surface roughness (rms $<$ 0.6 nm) are achieved, which is an excellent precondition for wafer bonding of strained silicon on silicon dioxide. We will discuss the influence of the implantation conditions on the relaxation for various thicknesses and Ge concentrations ("30at%) of the SiGe layers. Results achieved with SOI wafers and patterned wafers will also be discussed. In addition, we will demonstrate the fabrication of strained silicon layers by only one epitaxial growth step, recently achieved by He implantation, which is highly attractive from the physical and technological point of view.

11:00 AM *B1.7
Growth of strain-relaxed SiGe buffer layers on Si(001) substrates with controlled generation and propagation of dislocations. Akira Sakai[1], Shigeaki Zaima[2] and Yukio Yasuda[1]; [1]Department of Crystalline Materials Science, Graduate School of Engineering, Nagoya University, Nagoya, Japan; [2]CCRAST, Nagoya University, Nagoya, Japan.

Strain and defect engineering of SiGe alloy layers on Si substrates is crucial for high performance MOS devices with strained layer materials. Especially, strain-relaxed SiGe buffer layers have attracted much attention which is recently driven by strained channel Si MOSFET technologies. Several sophisticated methods, such as epitaxial growth, ion implantation, and SOI-based fabrication technique, have been utilized so far to pursue the SiGe buffer layers with high crystalline quality and flat surfaces (with no cross-hatch patterns). Realization of much thinner buffer layers should be also considered for practical applications. In principle, introduction of "strain" into the device requires highly-controlled structure and morphology of defects in which dislocations play an essential role in relaxing or inducing strain. It is no doubt that dislocations in the channel layer act as a scattering center of carriers and inhomogeneous strain might also give rise to harmful effects on the carrier mobility. In general, 60° dislocations are predominantly introduced into the SiGe/Si substrate interface as a result of the <110>/{111} slip system operation. Considering a screw component and components non-parallel to the interface of their Burgers vector, crystallographic tilting and rotation of SiGe inevitably occurs due to the dislocation introduction. Thus a problem arises how the SiGe material can be deformed on the Si(001) substrate without or with possibly-reduced crystalline morphological degradation. In this talk, we present our recent experimental results on the epitaxial growth of high quality SiGe buffer layers on Si(001) substrates, in which dislocation generation and propagation is precisely controlled during strain relaxation of SiGe. Two step strain relaxation procedure [1] is shown to introduce 60° dislocations dispersively into the SiGe/Si interface and enhance their propagation, resulting in the dislocation morphology tightly confined at the interface with no piling up. Characteristic crystalline texture resulting from the strain relaxation by the 60° dislocations is clearly revealed by microscopic and macroscopic analyses using transmission electron microscopy and X-ray reciprocal space mapping for the strain-relaxed SiGe layers. Furthermore, we report a novel approach based on the strain relaxation predominantly caused by a 90° dislocation network buried at the SiGe/Si(001) interface. Employing pure-Ge thin film growth prior to SiGe formation effectively restrains the introduction of 60° dislocations and instead high density of 90° dislocations can be generated. Ability of this 90° dislocation network to apply the strain relaxation of SiGe buffer layers is also discussed. [1] A. Sakai et al., Appl. Phys. Lett. 79, 3398 (2001).

11:30 AM B1.8
Critical Thickness Enhancement of Epitaxial SiGe Films Grown on Small Structures. Yue Liang[1], William D Nix[2], Peter B Griffin[1] and James D Plummer[1]; [1]Center for Integrated Systems, Stanford University, Stanford, California; [2]Department of Materials Science and Engineering, Stanford University, Stanford, California.

The 4.2% lattice mismatch between Ge and Si causes defects to form during Ge film growth on Si and leads to problems in device fabrication. Current growth techniques usually involve the creation of a thick graded SiGe buffer layer to accommodate the misfit strain. Thin or elastically soft, compliant substrates, on the other hand, increase the equilibrium critical thickness for defect formation and provide a means for forming dislocation-free heterostructures. A number of different approaches to such substrates have been reported in the literature. This paper explores the stress management with two kinds of structures, namely epitaxial films on small pillars or fins. In addition to the compliant substrate effect in the film/fin structures, the geometric effect in the film/pillar structure plays another important role in critical thickness enhancement. The stress-strain states of these two systems are calculated and the equilibrium critical thicknesses are predicted, using the work method, for different fin thicknesses, pillar radii and Ge concentrations. Compared to conventional films grown on planar bulk substrates, the critical thicknesses for fin and pillar structures are increased significantly. For example, the equilibrium critical thickness of 25% SiGe films on 25nm fin structures is 15 times larger than Matthews and Blakeslee's prediction. Moreover, if the fin or pillar dimension is below the critical thickness, the films can be grown to an arbitrary thickness without the generation of dislocations, since the misfit strain can be accommodated by the compliant substrate completely in this case. 200nm thick 25% SiGe films were grown at 625C on both sides of Si vertical fins with thicknesses ranging from 26nm to 470nm to demonstrate these concepts. Cross-sectional TEM analysis showed that dislocation densities are much smaller than for bulk Si substrate samples. The dislocation density versus fin thickness also illustrated the expected trend.

11:45 AM B1.9
Reduced Pressure - Chemical Vapor Deposition of SiGe virtual substrates for high mobility devices. Yann Bogumilowicz[3,1], Jean-Michel Hartmann[1], Alexandra Abbadie[1], Philippe Holliger[1], Frederic Laugier[1], Robert Truche[1], Guy Rolland[1], Thierry Billon[1], Olivier Estibals[2], Vincent Renard[2], Jean-Claude Portal[2], Evgueni Olshanetsky[4,2] and Dimitri Kvon[4,2]; [1]DTS, CEA-LETI, GRENOBLE, 38054, France; [2]GHMFL, GRENOBLE, 38042, France; [3]STMicroelectronics, CROLLES, 38926, France; [4]RAS, ISP, NOVOSIBIRSK, 630 090, Russian Federation.

We have studied the growth by Reduced Pressure Chemical Vapor Deposition of high Ge content (from 20% up to 55%) SiGe virtual substrates, focusing on their surface and film morphologies. We have used such virtual substrates as starting materials for the formation of SiGe On Insulator or tensile-strained Silicon On Insulator substrates. In a bulk form, they can serve as templates for the growth of tensile-strained Si surface channels with both high electron and hole mobilities (for Ge contents $>$ 35%). We have first extracted the macroscopic strain relaxation and the Ge concentration inside our virtual substrates from (004) and (224) Omega / 2Theta scans in X-ray diffraction. Typically, linearly-graded Si0.45Ge0.55 virtual substrates 8 microns thick are 97% relaxed (8% Ge / micron linear

grade). The misfit dislocations introduced to plastically relax the lattice mismatch between Si and SiGe are mostly confined in the graded layer, as confirmed by cross-sectional transmission electron microscopy. The threading dislocations density obtained for Ge concentrations of 20% and 27% is indeed typically of the order of 7.5E5 / cm2. The expected surface root mean square roughness increase when the Ge content exceeds 30% is not that important : the rms is indeed only of 4 to 5 nm for Ge concentrations in-between 30% and 55% (versus 2 to 3 nm for Ge concentrations in-between 20% and 27%). The spatial wavelength of the cross-hatch undulations is in-between 1 and 2 microns, this whatever the Ge content. A chemical mechanical polishing step in conjunction with the appropriate wet cleaning and H2 bake (2 min., T = 800C or more) can however make the surface fit for some epitaxial Si or SiGe re-growth, with a smooth resulting morphology (rms = 0.4 nm). We have also studied the electronic quality of our RP-CVD grown SiGe virtual substrates. For this purpose, we have first of all studied the phosphorous n-type doping of SiGe in the 20% to 33% Ge concentration range. We have noticed that the P incorporation into SiGe is (i) linear with the PH3 flow in the 4E17 to 1E19 / cm3 concentration range and (ii) decreases significantly with the Ge concentration. We have then grown a MODFET-like heterostructure, with a buried tensile-strained Si channel 8 nm thick deposited on nearly fully relaxed SiGe 26%, an intrinsic SiGe 26% spacer layer 15 nm thick and a P-doped SiGe supply layer (2E18 cm-3, 30 nm thick). We have obtained a well-behaved 2-dimensional electron gas in the Si channel, with electron sheet densities and mobilities at 1.45K of 5.4E11 / cm2 and 210 000 cm2/V.s, respectively.

SESSION B2: Strained Si and SRBs on Insulator
Chair: Steven Koester
Tuesday Afternoon, April 13, 2004
Room 2004 (Moscone West)

1:30 PM *B2.1
SiGe-on-Insulator and Ge-on-Insulator Substrates Fabricated by Ge-Condensation Technique for High-Mobility Channel CMOS Devices. Tsutomu Tezuka[1], Tomohisa Mizuno[1], Naoharu Sugiyama[1], Shu Nakaharai[1], Yoshihiko Moriyama[1], Koji Usuda[1], Toshinori Numata[1], Norio Hirashita[1], Tatsuro Maeda[2], Shin-ichi Takagi[2], Yoshiji Miyamura[3] and Eiji Toyoda[4]; [1]MIRAI-ASET, Kawasaki, Japan; [2]MIRAI-AIST, Tsukuba, Japan; [3]Komatsu Electronic Metals, Hiratsuka, Japan; [4]Toshiba Ceramics, Tokyo, Japan.

This paper presents a review of fabrication of SiGe-on-Insulator (SGOI) structures by Ge condensation technique [1] and its application to high-mobility channel CMOS devices. Strained Si, strained SiGe and strained/relaxed Ge are attractive channel materials for future scaled CMOS devices because of high current drive due to their high carrier mobilities. This advantage can be maximized by combining these materials and SOI structures, since these device structures allow low impurity concentration in the channels while the short channel effect is suppressed by thinning the bodies sufficiently. However, the biggest challenge in developing these devices is that the wafer supply of such kinds of substrates is currently very limited. In order to overcome this situation, we have developed a simple fabrication technique called Ge condensation for relaxed/strained SiGe- and Ge-on-Insulator substrate. This technique consists of epitaxial growth of a SiGe layer with a low Ge fraction on an SOI substrate and successive oxidation at high temperatures, which can be incorporated in a conventional CMOS process. During the oxidation, Ge atoms are pushed out from the oxide layer and condensed in the remaining SiGe layer. Eventually, an SGOI layer with a higher Ge fraction is formed on the buried oxide layer. The Ge fraction in the SGOI layer can be strictly controlled by the oxidation time because total amount of Ge atoms in the SGOI layer is conserved throughout the oxidation process. We have successfully fabricated both strained and relaxed SGOI layers by selecting the initial SiGe thickness and the Ge fraction appropriately. Fully depleted and partially depleted strained SOI MOSFETs were fabricated on strained Si layers grown on relaxed SGOI substrates formed by this technique [2, 3]. Electron and hole mobility in these devices exhibited enhancement of up to 80% and 50%, respectively. CMOS ring oscillators comprised of these devices also exhibited reduction in propagation delay of 70%-30% compared to conventional SOI-CMOS devices [2]. Ultrathin-body strained SGOI pMOSFETs with high Ge fraction and surface channels were also fabricated [4]. These devices exhibited much larger hole mobility enhancement (>100%). Recently, we have succeeded in fabrication of Ge-on-Insulator (GOI) structures with thicknesses less than 10 nm using the Ge-condensation technique [5]. This result implies that the Ge-condensation technique can be applicable to fabrication of ultrathin body GOI-CMOS devices. In conclusion, the Ge-condensation technique is promising for fabrication of high-mobility channel-on-insulator devices. References [1] T. Tezuka et al., Appl. Phys. Lett. 79, 1798 (2001) [2] T. Mizuno et al., Symp. on VLSI Tech., 106 (2002) [3] T. Tezuka et al., Symp. on VLSI Tech., 96 (2002) [4] T. Tezuka et al., IEDM Tech. Dig., 946 (2001) [5] S. Nakaharai et al., Extended abstracts of SSDM, 266 (2003)

2:00 PM B2.2
Fabrication of strained-silicon on insulator by direct wafer bonding using thin relaxed SiGe films as virtual substract. Jong-Jan Lee, Jer-shen Maa, Douglas Tweet and Sheng Teng Hsu; Sharp Laboratories of America, Camas, Washington.

Strained-Si films with thickness of 15 nm to 30 nm were successfully fabricated on insulator by direct wafer bonding and splitting. First, strained SiGe film with thickness between 300 nm to 350 nm and Ge concentration of 20% to 30% was deposited on (100) Si by RTCVD. Relaxation of SiGe was achieved by hydrogen ion implantation and relaxation annealing. After removing the surface undulation by CMP, thin strained Si was then deposited on this relaxed SiGe film. After another hydrogen implantation for wafer splitting, the wafer was bonded to a carrier wafer with 200 nm thermal oxide. Wafer splitting was carried out in a diffusion furnace, which was followed by a surface smoothening step and finally a step for selective removal of SiGe. The final structure was a thin strained Si directly on insulator. XRD measurement showed the strain of this thin Si was equivalent to Si film deposited on 100% relaxed SiGe with 20% Ge. Similar strain was measured after thermal annealing at 900 deg-C. Cross-sectional TEM showed a sharp Si to oxide bonding interface. No defect was detected in the as-bonded film by TEM. NMOS devices fabricated on this SSOI structure showed very good electrical characteristics. The subthreshold swing of 75mV/decade and off current of 0.1 pA/microm were obtained on device with gate length of 0.13 micron.

2:15 PM B2.3
Strained Silicon On Insulator wafers made by the Smart Cut(TM) technology. Bruno Ghyselen[1], Yann Bogumilowicz[2,3], Cecile Aulnette[1], Alexandra Abbadie[2], Benedite Osternaud[2], Pascal Besson[3], Nicolas Daval[1], Francois Andrieu[2,3], Ian Cayrefourcq[1], Hubert Moriceau[2], Thomas Ernst[2], Antoine Tiberj[1], Olivier Rayssac[1], Beryl Blondeau[1], Jean-Michel Hartmann[2], Patrick Leduc[2], Christine Di Nardo[2], Jean-Francois Lugand[2], Franck Fournel[2], Yves Campidelli[3], Olivier Kermarrec[3], Vincent Paillard[4], Laetitia Vincent[5], Alain Claverie[5] and Philippe Boucaud[6]; [1]SOITEC, BERNIN, France; [2]CEA-LETI, Grenoble, France; [3]STMicroelectronics, Crolles, France; [4]LPST-UPS, Toulouse, France; [5]CEMES-CNRS, Toulouse, France; [6]IEF-CNRS, ORSAY, France.

Strained Silicon On Insulator wafers are today envisioned as a natural and powerful enhancement to standard SOI and/or bulk-like strained Si layers. For MOSFETs applications, this new technology potentially combines enhanced devices scalability allowed by thin films and enhanced electron and hole mobility in strained silicon. In the first part, this paper is intended to demonstrate by experimental results how a layer transfer technique such as the Smart Cut technology can be used to obtain good quality tensile Strained Silicon On insulator wafers. In the second part detailed experiments and characterizations will be used to demonstrate that these substrates are compatible with the applications, especially by showing the effect of high temperatures treatments on major parameters such as surface and interface abruptness, and Ge content and strain control. Two approaches based on the Smart Cut technique will be of particular interest in this paper. Such a technique uses preferentially hydrogen implantation to peel-off the very top part of an epitaxial stack and transfer it onto another silicon substrate. The formation of an insulator, prior to bonding onto a new silicon substrate enables the formation of a Semiconductor on Insulator structure. One approach uses the realization by layer transfer of an intermediate relaxed SiGe On Insulator (SGOI) substrate on which an ultimate strained Si epitaxial growth is performed. The second approach is based on the transfer of a pre-formed strained Si layer. In this case, a SiGe free substrate can be realized. This second approach is particularly challenging as the strain needs to be maintained during many technological operations such as layer transfer, selective removal of any SiGe layer and multiple CMOS operations which include high temperature thermal treatments. First results showing how the strain is changing during such operations will be presented. Epitaxy of relaxed SiGe and strained Si layers will be addressed in detail. Studied epitaxial layers are of two kinds: starting epitaxial strained Si on relaxed SiGe buffer used as donor wafers in layer transfer operations, and also strained Si epitaxial films on SGOI substrates. In-depth physical characterizations of these epitaxial layers are used to evaluate the quality of the transferred layers (surface roughness, thickness uniformity, dislocation densities, Ge content uniformity, strain uniformity...).

2:30 PM B2.4
Material and optical properties of GaAs grown on (001) Ge/Si pseudo-substrate. Yves Chriqui[1], Ludovic Largeau[1], Gilles Patriarche[1], Guillaume Saint-Girons[1], Sophie Bouchoule[1], Daniel

Bensahel[2], Yves Campidelli[2], Olivier Kermarrec[2] and Isabelle Sagnes[1]; [1]LPN-CNRS-UPR 20, Marcoussis, France; [2]ST Microelectronics, Crolles, France.

One of the major challenges during recent years was to achieve the compatibility of III-V semiconductor epitaxy on silicon substrates to combine opto-electronics with high speed circuit technology. This new technology offers the possibility to fabricate e.g. low cost solar and optical interconnections. However, the growth of high quality epitaxial GaAs on Si is not straightforward due to the intrinsic differences in lattice parameters and thermal expansion coefficients of the two materials. Moreover, antiphase boundaries (APBs) appear that are disadvantageous for the fabrication of light emitting devices. Recently the successful fabrication of high quality germanium layers on (001) Si (forming so-called Ge/Si pseudo-substrates (PS)) by chemical vapor deposition (CVD) was reported (dislocation density 6.10^6 cm^{-2}, surface roughness rms < 0.5 nm). Due to the germanium seed layer the lattice parameter is matched to the one of GaAs providing for excellent conditions for the subsequent GaAs growth. We have studied the material morphology of GaAs grown on Ge/Si PS using atomic layer epitaxy (ALE) at the interface between Ge and GaAs. Here we present first results on the reduction of APBs and dislocation density on (001) Ge/Si PS when ALE is applied. We will show that the ALE allows the reduction of the residual dislocation density in the GaAs layers to 10^5 cm^{-2} (one order of magnitude as compared to the dislocation density of the Ge/Si PS). The optical properties of the grown material will be discussed. Using ALE, light emitting diodes based on strained InGaAs/GaAs quantum well as well as of In(Ga)As quantum dots on an exactly oriented (001)Ge/Si pseudo-substrate were fabricated and characterized.

2:45 PM B2.5
Effects of Ge on Thermal Decomposition of Ultrathin Silicon/Germanium-on-Insulator. Pengpeng Zhang[1], Bin Yang[1], Paul Rugheimer[1], Michelle Roberts[1], Feng Liu[2] and Max Lagally[1]; [1]Department of Materials Science and Engineering, University of Wisconsin-Madison, Madison, Wisconsin; [2]Department of Materials Science and Engineering, University of Utah, Salt Lake City, Utah.

Silicon-on-insulator (SOI) substrates have attracted much attention because they greatly enhance the speed and reduce the power consumption of CMOS transistors. As the Si template layer thickness in SOI is reduced to tens of nanometers, it becomes thermally unstable, decomposing into silicon islands at temperatures approaching processing temperatures [1,2]. We have studied the effect of Ge deposition on the thermal decomposition of thin SOI. The thermal decomposition temperature of ultrathin SOI decreases with increasing Ge coverage. An amount of Ge as small as 2ML can lead to a dramatic decrease of the decomposition temperature. Also, the long-range ordering of 3D Si islands seen in the decomposition of SOI is gradually lost with increasing Ge coverage. Furthermore the agglomerated SiGe islands are not predominantly bounded by {131} facets as the Si islands are on decomposed SOI. This observation can be understood in terms of misfit strain from lattice mismatch, bond energy, and surface energy anisotropy. As the Ge coverage increases, misfit strain increases so that the Si-Ge layer becomes less stable Also Ge-Ge and Si-Ge bonds are weaker compared to Si-Si bonds. These results are discussed in terms of a simple model. The lowering of the decomposition temperature of the Si template layer on SOI, to as low as 700C when Ge is present, suggests that the allowable processing temperatures, the thinness of SGOI, or the thinness of SOI on which Ge is grown that can be used may be limited. [1] B. Legrand, V. Agache, J. P. Nys, V. Senez, and D. Stieenard, Appl. Phys. Lett. 76, 3271 (2000); [2] R. Nuryadi, Y. Ishikawa, and M. Tabe, Appl. Surf. Sci. 159, 121 (2000) Supported by DOE

SESSION B3: Characterization and Defects in Strained Layers
Chair: Erich Kasper
Tuesday Afternoon, April 13, 2004
Room 2004 (Moscone West)

3:30 PM B3.1
Stress Metrology: The challenge for the next generation of Engineered wafers. Antoine Tiberj[1], Vincent Paillard[2], Cecile Aulnette[1], Nicolas Daval[1], Konstantin Bourdelle[1], Mark Kennard[1] and Ian Cayrefourcq[1]; [1]Advanced Technologies Department, Soitec, Crolles Cedex, France; [2]Laboratoire de Physique des Solides (LPST), Universite Paul Sabatier, Toulouse, France.

technology node. A thin (typically less than 200 A) Si layer under tensile strain is obtained typically by epitaxial growth of Si on a strained-relaxed SiGe buffer layer. To quantify the quality of sSi wafers in manufacturing it is necessary to measure the uniformity of the stress in the sSi film across the 8 and 12 inches wafers. The Ge content and the strain relaxation in the SiGe layers must also be monitored during different process steps used, e.g., in the production of sSOI and SGOI wafers [1]. The required metrology method must provide a high-precision and high-resolution wafer map of strain and Ge content. It should be fast, clean-room compatible, and be easily adapted in the in-line metrology tool. All these requirements represent a very serious challenge for the existing metrology/analytical techniques. The established techniques used in todays FEOL process monitoring such as ellipsometry/reflectometry, HR XRD, RBS, SIMS cannot be utilized for in-line stress/relaxation and Ge concentration measurements. They luck precision, resolution, wafer mapping capability, and clean-room capability. We will show that Raman spectroscopy (UV and visible) provide fast and precise measurements of the sSi stress, the Ge content and the degree of relaxation of SiGe layers [2,3]. We use resonant Raman scattering in Si and SiGe layers to develop wafer map capability [4]. The experimental set-up and results obtained for sSOI and SGOI wafers will be presented and discussed. [1]B. Ghyselen et al., Proceedings of the ICSI3 (Santa Fe 2003) [2]J.C. Tsang et al., Journal of Applied Physics 75, 8098 (1994) [3]I. De Wolf, Semiconductor Science and Technology 11, 139 (1996) [4]J.B. Renucci, Physical Review B 11, 3885 (1975)

3:45 PM B3.2
Strain Mapping in SiGe by Visible Raman Spectroscopy. Vasil Pajcini, Charles Evans & Associates, Sunnyvale, California.

Xie et al. have reported a 10X10 μm UV-Raman map of stress in the thin Si cap of a Si/SiGe sample where the stress map could correspond to the cross-hatch pattern seen by AFM [1]. The UV (325 nm) source results in a shallow penetration of the Si cap so that the stress measured is in the Si cap. Here we report a similar effect using visible Raman spectroscopy to probe the strain associated with threading dislocations in the $Ge_xSi_{(1-x)}$ structures below the Si cap. The Si-Si vibrating mode of SiGe layer was mapped on a square area (30X30$_\mu$m) for samples with different structures using a visible Raman spectrometer excited with an Ar^+ ion laser (514.5 nm wavelength, 1mw in the sample, 1$_\mu$m spatial resolution). Unlike the UV-Raman, the visible source results in a much deeper penetration, i. e., analysis of the stress in the underlying SiGe layer. A clear pattern of wavenumbers emerged along the <110> directions, which was conserved when the physical sample was rotated with 45^0 around the Z-axis. The Si-Si wavenumbers depend both on the Ge concentration and on the strain developed on SiGe due to lattice mismatched systems heteroepitaxial grown of Si-SiGe beyond critical thickness. The lattice mismatch results in the formation of misfit and associated threading dislocations which lead to the characteristic cross-hatch pattern of the Si strained epilayer surface. The Si-Si wavenumber pattern of SiGe layer should be stress related pattern caused by the strain developed in the SiGe layer and not to any latteral Ge distribution on the μm scale, as the Raman mapping (imaging) mimics the cross-hatch pattern usually observed optically or through AFM. As the penetration depth of 514.5 nm light is 0.5 μm in SiGe samples with 30% Ge, the strain cross-hatch pattern is probably related to the same stress distribution developed throught the entire layer of SiGe (>1$_\mu$m). The lateral scale of stress variations depended on the individual samples and was measured from 4 to 12 μm (ridge to ridge), with a stress range up to 0.2 GPa. The lateral scale of 12 μm is close to the cross-hatch pattern of the optical image of the sample and might be also comparable with the threading dislocation densities of 10^6 cm^{-2}. Visible Raman can be used successfully to measure and monitor stress developed in SiGe structures. The visible light absorption on SiGe/Si strained samples should be taken into consideration during the Raman measurements to avoid (or correct) the temperature effect on the Si-Si wavenumbers. [1] Q. Xie et al, "Characterization Techniques for Evaluating Strained Si CMOS Materials", Characterization and Metrology for ULSI Technology: 2003 International Conference, edited by D. G. Seiler, A. C. Diebold, T. J. Shaffner, R. McDonald, S. Zollner, R. P. Khosla and E. M. Secula, AIP Conference Proceedings Vol. 683, 2003 American Institute of Physics, Melville, NY, pp. 223-227.

4:00 PM B3.3
Defect Characterization of Strained Si/SiGe Epitaxial Structures. Kevin R Bray[1], Andrzej Czerwinski[1], Ludwik Kordas[1], Wenjun Zhao[1], McDonald Robinson[2] and George Rozgonyi[1]; [1]Materials Science and Engineering, North Carolina State University, Raleigh, North Carolina; [2]Lawrence Semiconductor Research Laboratory, Tempe, Arizona.

Defects in thin layers of epitaxial heterostructures of strained Si/SiGe grown on Si substrates have been studied by a wide range of dedicated electrical, structural and chemical methods. The electrical activity of misfit and threading dislocations was probed using electron-beam-induced current (EBIC) contrast measurements over a wide temperature range. At room temperature, no electrical activity was observed, while at low temperature the crossgrid array of misfit

dislocations and pile-ups of threading dislocations were visible. Defect regions observed in EBIC were marked and cross-sectional TEM samples of the defects were prepared using focused ion beam (FIB) techniques. Z-contrast and electron energy-loss spectrometry (EELS) TEM modes were utilized to characterize the defects and interfaces. A systematic calibration of the etch rate of preferential chemical etchants revealed that it is dependent on the Ge content, local stress and defects in the layers. Etch rates measured in SiGe were up to 3x times faster than in c-Si. Due to the thin layers, and the need to separate threading and misfit dislocations, bevel polishing and preferential chemical etching were also utilized to study the density and distribution of defects in the heterostructures. Bevel polishing has been extended to low-angles, i.e. with high depth magnification of up to 100x, which transforms, e.g. 200 nm layers into 20 μm wide region. Surface profilometry of the beveled samples showed a strong difference in the etch properties of films with 14% and 41% Ge. Nomarski interference optical microscopy and atomic force microscopy (AFM) were also used to examine the etched surfaces and to characterize the etch pit density and size. Finally, EBIC measurements on MOS capacitor structures under accumulation bias allow the depletion width to be collapsed, facilitating the analysis of very thin layers and near-surface defects. Preferential etchant dilutions are also employed to decrease the etch rate, enabling characterization of thin layers. These modifications enable quantitative studies of defect electrical activity and density/distributions. The results show that defects in thin Si/SiGe layers can be successfully studied with various characterization methods and expand the ability to develop high-quality Si/SiGe structures.

4:15 PM B3.4
Measurement of the Residual Macro and Microstrain in Strained Si/SiGe MOSFETs Using Raman Spectroscopy.
Peter Dobrosz[1], Steve J. Bull[1], Sarah H. Olsen[2] and Anthony G. O'Neill[2]; [1]School of Chemical Engineering and Advanced Materials, University of Newcastle, Newcastle upon Tyne, United Kingdom; [2]School of Electrical, Electronic and Computer Engineering, University of Newcastle, Newcastle upon Tyne, United Kingdom.

Electrons and holes have a higher mobility in tensile strained silicon compared with bulk Si. Hole mobility is also enhanced in compressively strained silicon germanium. Thus, use of strained Si/SiGe layers for the channel material of metal-oxide-semiconductor field-effect transistors (MOSFETs) leads to significant performance gains. Fabrication of strained Si complementary MOS (CMOS) devices uses high thermal budgets compared with other technologies which benefit from enhanced strained Si/SiGe material properties. Maintaining channel strain during processing is paramount for advanced MOSFET performance. The use of laser Raman spectroscopy to assess the residual strain in strained Si/SiGe devices is well established. The peak shift associated with the 520 cm-1 silicon peak can be used to directly measure the strain in a Si channel layer provided that the strained silicon peak can be deconvoluted from the more intense Si-Si in SiGe peak which occurs at slightly lower wavenumbers. The position of this latter peak can be used to assess the germanium content of the SiGe layer once a suitable calibration curve has been obtained. However, though peak position gives a measure of the macrostrains in the layer it is not useful for the assessment of microstrains associated with point defects which may also influence device performance; such microstrains influence the intensity of the Raman peaks and can, in principle, be monitored by this method. In this study we have undertaken an investigation of peak shape as a function of processing conditions for strained silicon on relaxed Si1-xGex, for $0 < x < 0.35$. The results suggest that changes in peak position can be correlated with macrostrains and macrostrain relaxation around extended defects such as pyramidal and pile-up dislocations (revealed by Schimmel etching). Changes in peak width can be correlated with processes which lead to changes in composition (e.g. germanium build-up at the surface after oxidation and etching). Peak intensity is found to be reduced after ion implantation and greatly increased after high thermal budget processing, implying that the creation and removal of point defects and their associated microstrain is detectable using Raman. Changes to the peak shapes are correlated with strained Si/SiGe MOSFET performance. It is proposed that these changes are not necessarily correlated with changes in macrostrain but indicate that microstrain could also be an important factor influencing device performance.

4:30 PM B3.5
Non-destructive Characterization for SiGeC Alloys with Spectroscopic Ellipsometry.
Christophe Defranoux[1], Florence Deleglise[2], adrien darragon[1], Richard Sun[1], Alexandre Talbot[2], Cyril Fellous[2] and Didier Dutartre[2]; [1]SOPRA Inc, westford, Massachusetts; [2]ST, Crolles, France.

Significant progress has been made in the field of strained Si1-xGex/Si heterostructures in the last decade. However, the strain due to larger atomic size of Ge in the pseudomorphic SiGex limits the thickness of the film. At the same time, with the device dimension continuously decreases a major challenge for the fabrication of such small devices is how to achieve steep dopant profiles. Researchers found that the best solution to overcome the above problems is to incorporate carbon in SiGe alloys. Carbon in such films can play following roles: (1) Increase the critical thickness at the fixed Ge concentration to remain compressive strain state without relaxing the film and/or causing significant misfit dislocation formation at the interface (2) suppress dopant outdiffusion to remain sharp profile. This poses significant challenges to film characterization and processing qualification. For example, the traditional nondestructive characterization technique, x-ray diffraction (XRD), will not be able to yield accurate Ge concentration in SiGeC alloys compared with binary SiGe alloy because incorporation of carbon has opposite effect as Ge to lattice parameter. In this paper, nondestructive spectroscopic ellipsometry technique will be applied to characterize such SiGeC films. Alloy model will be used to obtain Ge concentration. Effective approximation of mixture (EMA) model will be used to evaluate carbon's effect on optical density of the films. At the same time, Drude model is used to obtain the dopant (Boron in this case) concentration and conductivity of the film in the first principle. In addition, an example will be given to show the advantage of this technique in evaluating film whether it is still strained or has been relaxed based on two different alloy models (one for strained and the other for relaxed) developed at SOPRA. Finally, the results from spectroscopic ellipsometry will be discussed and compared with other techniques such as XRD, SIMS and XRF.

4:45 PM B3.6
Interference-Enhanced Raman Scattering in Strain Characterization of Ultra-thin(10nm) Strained Si and SiGe on Insulator.
Haizhou Yin[1], Karl D Hobart[2], Sean R Shieh[3], Rebecca Lorenz Peterson[1], Thomas S Duffy[3] and James C Sturm[1]; [1]POEM & Dept. of Electrical Engineering, Princeton Univ., Princeton, New Jersey; [2]Naval Research Lab, Washington, District of Columbia; [3]Dept. of Geosciences, Princeton University, Princeton, New Jersey.

The combination of strained channels and silicon-on-insulator (SOI) structure is appealing for its ability to boost carrier mobility while maintaining advantages unique to SOI structures. Due to critical thickness constraints and suppression of short-channel effects, the thickness of the strained layer, either Si for n-channel FETs or SiGe for p-channel FETs, needs to be small. While Raman scattering is in principal a useful tool to evaluate strain and composition in such structures, it is difficult to characterize ultra-thin films. In this paper we show that optical interference in SOI structures can increase the ratio of the Raman signal of the films on top to that of the substrate by more than 10 times, so that strained layers as thin as 10 nm can be characterized. The approach is demonstrated through a novel compliant substrate technique of transferring Si or SiGe onto borophosphorosilicate glass (BPSG), which allows ultra-thin strained silicon (with or without SiGe) or strained SiGe layer on insulator to be realized. Using wafer bonding and Smart-cut processes, fully-strained SiGe (up to 30 nm) and unstrained Si (up to 25 nm), initially grown pseudomorphically on Si(100) substrates, were transferred onto BPSG to form SiGe/Si on insulator structures [1-3]. The SiGe/Si layers were then patterned into islands, which were able to laterally expand to adjust the strain in the SiGe and Si films when the BPSG was softened during high-temperature annealing. We have studied various tensile Si (thickness from sub-10 nm to 25 nm with about 0.7% strain) and SiGe films (Ge content from 30% to 50% and thickness from 10 nm to 30 nm) on BPSG insulator. Tensile strain in the Si film was generated through a 30 nm compressive SiGe film on top of Si, with the SiGe removed after the island relaxed to strain the Si. The interference effect from the BPSG insulator, serving as a reflection coating, substantially enhanced the Raman signal from the top SiGe/Si films and suppressed the Raman signal from the Si substrate. Such interference enhancement was previously observed on other multi- thin film structures [4]. While the Raman signal (laser wavelength of 514 nm) from a 30 nm SiGe layer directly grown on silicon substrates was buried in background noise, the signal from a SiGe or Si layer as thin as 10 nm on BPSG was strong. Finally, the strain measured by Raman scattering accurately predicted the observed increase in mobility in strained n-channel FETs on insulator. This work is supported by DARPA (N66001-00-1-8957) 1. K.D. Hobart, et al., J. Electron. Mater. 29, 897 (2000) 2. H. Yin., et al., J. Appl. Phys. 91, 9716 (2002) 3. H. Yin, et al., Appl. Phys. Lett. 82, 3853 (2003) 4. W.S. Bacsa, et al., Appl. Phys. Lett. 61, 19 (1992)

SESSION B4: Ge Substrates
Chair: Shigeaki Zaima
Wednesday Morning, April 14, 2004
Room 2004 (Moscone West)

8:30 AM B4.1
Germanium-on-Insulator for future device generations fabricated by direct wafer bonding. Alexander Reznicek, Guy M Cohen and Steven J Koester; IBM T. J. Watson Research Center, Yorktown Heights, New York.

Germanium has higher carrier mobility than silicon for both electrons and holes. However, it was not used for MOSFETs due to the poor quality of the germanium oxide. Advances in silicon technology introduced high-k dielectrics as the MOSFET gate insulator. The high k dielectrics are also expected to be usable with germanium, thus removing the main obstacle in realizing a Ge based FET. Germanium has other advantages such as lower contact resistance and lower dopant activation temperatures than those required by silicon, thus facilitating the formation of shallow junctions.
The higher device performance obtained with Silicon-on-Insulator (SOI) can also be obtained with Germanium-On-Insulator (GOI). Additionally, since current fabs are equipped with tools design to handle silicon substrates, it is desirable that the GOI stack will be formed on a silicon wafer.
We have demonstrated the fabrication of 8-inch Germanium-on-Insulator wafers. To archive a high bonding energy the germanium surface is first roughened by argon sputtering. The sputtering also removes the native Ge oxide. A thin silicon layer is then sputtered onto the germanium surface followed by sputtered silicon oxide. A thick low temperature oxide (LTO) is deposited onto the sputtered silicon oxide and densified at higher temperature. After hydrogen implantation with the typical smart-cut dose the low temperature oxide surface is polished by CMP. The polished surface is cleaned and surface treated and then bonded to a blank silicon handle wafer. To perform the bonding the wafers are first annealed at 225C, and then annealed at a higher temperature to achieve splitting. To strengthen the bonding the final Germanium-on-Insulator structure is annealed at even higher temperature. Finally the germanium surface is touch polished to remove the roughness originated from the smart-cut process.
High-resolution x-ray diffraction measurements and TEM investigations confirm a high quality layer transfer, with a good bonding interface. No strain is found in the transferred Ge film. The mobility of the transferred film measured by the Van der-Pauw technique was found to be similar to that of bulk Ge.

8:45 AM B4.2
Germanium Substrates for Micro-Electronic Applications up to 300mm Diameter. Geoffroy Raskin[1], Igor Romandic[1], Lucien Wouters[1], David Hellin[2], Ivo Teerlinck[2], Marc Meuris[2] and Paul Mijlemans[1]; [1]Electro-Optic Materials, Umicore, Olen, Belgium; [2]ASTEG, Imec, Leuven, Belgium.

Recently germanium has come in the spotlight again as one of the promising materials for future semiconductor technology. Germanium shows higher (low field) mobility than silicon, the activation annealing of dopants could be done at low temperatures, which allows low temperature processing, and the smaller energy bandgap could allow V_{DD} scaling for reduced power consumption. Finally the integration with III/V materials is possible due to the lattice match between germanium and GaAs, which potentially adds new functionalities to the chip as optical components on the same substrate. In order to demonstrate this high potential, germanium wafers need to be available, and this at the same sizes and living up to the same standard as is the case for silicon wafers. The current standard diameter for Ge substrates is 100mm; these substrates are used in large numbers for the production of high performance solar cells. Recent developments in crystal growth and substrate production have led to the manufacturing of 200mm germanium substrates. Here 300mm dislocation-free substrates are reported, matching with principal SEMI specifications. Compared to silicon crystal growth (using the Czochralsky technique), the growth of large diameter dislocation-free crystals is more difficult, since the thermal conductivity of germanium is lower, which facilitates the formation and multiplication of dislocations. By optimising the mechanical and thermal stability of the crystal growth system, we were able to solve the technological hurdles that impeded the growth of the world's first 300mm dislocation-free germanium crystal in the world. Crystals were further processed into wafers. Although germanium appears at first sight similar to silicon, the particularities of Ge make it a difficult material to process. Germanium's weaker mechanical characteristics (weight, hardness and fracture strength) and different chemical behaviour (especially the tendency to etch very easily) requires dedicated wafering processes. The major obstacles are now solved for both 200mm and 300mm diameter: metallic surface contamination and key dimensional parameters such as TTV, bow and warp can meet up to the standard silicon specifications. Although development of germanium wafers must be further improved and is still on-going, they can now be produced to requirements of size (2" – 300mm), shape and contamination levels acceptable to mainstream Si research facilities. We believe that the development of 200mm and 300mm Ge substrates will facilitate the integration of germanium in the silicon environment, allowing the research community to demonstrate its potential use for high-performance micro-electronics.

9:00 AM B4.3
Reduced Pressure - Chemical Vapor Deposition of Ge thick layers on Si(001) for Ge-based electronics and for 1.3-1.55 micron photo-detection. Jean-Michel Hartmann[1], Alexandra Abbadie[1], Anne-Marie Papon[1], Philippe Holliger[1], Guy Rolland[1], Thierry Billon[1], Jean-Marc Fedeli[1], Mathieu Rouviere[2,3], Laurent Vivien[2] and Suzanne Laval[2]; [1]DTS, CEA-LETI, GRENOBLE, 38054, France; [2]IEF, Universite Paris Sud, ORSAY, 91405, France; [3]STMicroelectronics, CROLLES, 38926, France.

Using a production-compatible Reduced Pressure Chemical Vapour Deposition system, we have first of all studied the growth kinetics of Ge (using GeH4). At low temperatures (in-between 400 and 550 Celsius degrees), the Ge growth rate increases overtime, which is most probably due to a facetted surface. Meanwhile, at higher temperatures (600C and 750C), the Ge growth rate is almost constant overtime (smoother surface). The low activation energy Ea = 6.9 kcal. mol.-1 which is associated to the growth rate increase with the temperature implies that we are most probably faced with a supply-limited regime. We have also studied quite in-depth the structural and optical properties of miscellaneous thickness (in-between 380 and 1660 nm) Ge layers which have been deposited using a low temperature (400C) / high temperature (600C) approach. A tensile strain configuration (degree of strain relaxation : R = 103%) has been clearly evidenced for those Ge films, which are rather smooth (rms roughness : roughly 0.6 nm). The presence of this tensile strain is most probably linked to linear coefficients of thermal expansion which are larger for Ge than for Si. Using a 10 times {750C, 10 minutes / 875C, 10 minutes} thermal cycling (which promotes the glide of threading dislocations towards the edge of the substrate, thereby diminishing their density : < 2E8 cm-2) induces an increase in the tensile strain of those Ge layers (R = 109%), a surface roughening (root mean square roughness = 2 nm) and some out-diffusion of Si in Ge. A chemical mechanical polishing step in conjunction with the appropriate wet cleaning and H2 bake (2 min., T > 700C) can however make the surface fit for some epitaxial Ge re-growth, with a smooth resulting morphology (rms = 0.5 nm). Finally, we have investigated the growth of Ge thick films on patterned wafers. The growth is clearly selective, with very large loading effects (factor of 2 to 5 increase in the growth rate depending on the surface coverage by SiO2) and some faceting. The Ge layers produced are of high optical quality. An absorption coefficient alpha equal to 4300 cm-1 (3400 cm-1) has indeed been found at room temperature and for a 1.55 microns wavelength for as-grown (annealed) layers. A 20 meV bandgap shrinkage with respect to bulk Ge (0.78 eV versus 0.80 eV) is observed as well in those tensile-strained Ge epilayers, with a band edge which is less sharp for annealed than for as-grown layers (due to the out-diffusion of Si in Ge ?).

9:15 AM B4.4
Germanium-On-Insulator (GeOI) structure realized by the Smart-CutTM technology. fabrice letertre[1], eric jalaguier[2], yves matthieu le vaillant[1], pierre perreau[2], stephane pocas[2], bruce faure[1], chrystel deguet[2], nelly kernevez[2] and carlos mazure[1]; [1]DTA, Soitec S.A., bernin, France; [2]DTS / LTFC, CEA / LETI, grenoble, France.

Thin film Germanium-on-Insulator (GeOI) structure is a major research area with potential enhancements for numerous Ge-based applications. When compared to bulk germanium, GeOI with a silicon host mechanical support can enhance the capabilities of this material by various means: mechanical strength, weight reduction, optical transparency, and electrical properties. In this paper, we will present results on formation of thin film GeOI structures made by the Smart-CutTM technology Compared to SOI manufacturing, the development of GeOI requires adaptation to Germanium material. We will present results of Ge splitting kinetics and compare them to published results. Detailled characterization of GeOI will be discussed including TEM analysis for defect densities, interfaces abruptness and layers homogeneities evaluation as well as AFM for surface roughness evaluation. First results of electrical characterization of transferred Ge layers will be presented.

9:30 AM B4.5
Back–grind GeOI Substrates up to 200mm Diameter. Geoffroy Raskin[1], Robert Andosca[1], Markus Gabriel[2], Manfred Reiche[3], Mike Firth[1], Carlos Franco[1], Jeffrey Dumas[2] and Paul Mijlemans[1]; [1]Electro-Optic Materials, Umicore, Olen, Belgium; [2]Suss MicroTec, Waterbury Center, Vermont; [3]Max-Planck Institut fur Mikrostrukturphysik, Halle, Germany.

Recently germanium has come in the spotlight again as one of the promising materials for future semiconductor technology, mainly for its higher mobility properties. In order to demonstrate this high

potential, germanium wafers need to be available, and this at the same size and standard obtained for silicon wafers. Providing germanium wafers on silicon carriers, i.e. germanium-on-insulator (GeOI), gives the product some additional advantages. Germanium does not have the same strength as silicon wafers, leading to potential breakage issues in wafer fabs. GeOI allows to strengthen the wafer up to the carrier material strength (i.c. silicon). It also allows the robotic equipment to be solely in contact with silicon, partially avoiding contamination issues with germanium. Moreover integration of germanium and silicon allows for combined material electronics such as optical germanium receivers on silicon substrates. Finally, the limited availability of bulk germanium, which could otherwise hamper its use in large volume semiconductor industry, is hereby solved by limiting the germanium consumption to the top μm's of the wafer. Recent developments in crystal growth and substrate production have led to the manufacturing of 200mm germanium substrates. Here GeOI wafers with diameters of 100mm and 200mm are reported using back−grind technology. By choosing box layer deposition techniques and effective chemical, mechanical and megasonic cleaning of the wafers to be bonded, nearly void-free wafers can be produced as demonstrated by acoustic imaging. Bond strengths sufficient to withstand grinding and polishing operations without delamination were obtained by applying plasma activation under atmospheric conditions previous to bonding (Süss MicroTec patent pending). This allowed a relaxation on the thermal annealing of the bonded pairs, which is important as germanium and silicon have a large difference in thermal expansion. By optimising the bulk germanium wafer grinding and polishing process to GeOI wafers, device layer thicknesses down to 5μm were realised with TTV less than 2μm. Despite the thermal expansion differences between device and carrier materials, bow and warp figures were kept within normal Si wafer specifications. Although development of GeOI wafers must be further improved and is still on-going at Umicore Electro-Optic Materials, we believe that the development of GeOI wafers up to 200mm diameter will facilitate the integration of germanium in the silicon environment, allowing the research community to demonstrate its potential use for high-performance micro−electronics, MEMS and MOEMS.

SESSION B5/D5: Joint Session: High-k and High Mobility Substrates
Chair: Tsutomu Tezuka
Wednesday Morning, April 14, 2004
Room 2004 (Moscone West)

10:15 AM *B5.1/D5.1

Novel Deposition Processes for High-k/Ge Devices: Interface Engineering. Paul McIntyre[1], Hyoungsub Kim[1], David Chi[1], Chi On Chui[2], Baylor Triplett[1], Ali Javey[3], Hongjie Dai[3] and Krishna Saraswat[2]; [1]Materials Science and Engineering, Stanford University, Stanford, California; [2]Electrical Engineering, Stanford University, Stanford, California; [3]Chemistry, Stanford University, Stanford, California.

High permittivity dielectric materials and metal gate electrodes are currently being investigated by many research groups world-wide in an effort to continue the aggressive dimensional scaling of metal oxide semiconductor devices. The development of relatively high-quality deposited gate dielectrics to replace SiO2-based dielectrics for silicon field effect transistors presents an opportunity to consider alternative materials for the semiconductor channel in such devices. There are many fundamental advantages to using Ge in the channel in place of Si. The relative instability of GeO2 with respect to most high-k metal oxides under oxidizing conditions may avoid growth of an undesirable low-k interface layer under the deposition conditions used to form the high-k gate dielectric, in contrast to the typical situation for high-k deposition on Si. Furthermore, use of Ge may result in lower temperatures for dopant activation compared to Si. The larger (and better-matched) low-field carrier mobilities in Ge relative to Si result in devices that operate beyond the universal mobility model for Si MOSFETs. In this presentation, results obtained from atomic layer deposition- and UV-ozone oxidation-synthesized metal oxide dielectric layers on Ge (100) substrates will be compared. Physical characterization of HfO2 and ZrO2 gate dielectric layers and their interfaces with different Ge surface passivations will be emphasized. Recently published electrical data obtained from MOSCAP structures and high-k Ge MOSFETs will also be reviewed. The presence and effects of interface states on electrical behavior will be discussed, including comparison with results obtained from high-k/SiO2/Si and high-k/carbon nanotube devices.

10:45 AM B5.2/D5.2

Synchrotron Radiation Photoemission Spectroscopy of High-k Gate Stack in High-performance Ge MOS Devices.
Chi On Chui[1], Dong-Ick Lee[2], Andy A. Singh[2], David Chi[3], Paul C. McIntyre[3], Piero A. Pianetta[2] and Krishna C. Saraswat[1]; [1]Electrical Engineering, Stanford University, Stanford, California; [2]Stanford Synchrotron Radiation Laboratory, Menlo Park, California; [3]Materials Science and Engineering, Stanford University, Stanford, California.

The saturation of Si MOSFET drain current upon dimension shrinkage may limit the prospect of future scaling. The lower effective mass (and lower valley degeneracy) of Ge could alleviate the problem by providing a higher source injection velocity, which translates into higher drive current and smaller gate delay. Nonetheless, unlike Si, the poor quality Ge native dielectrics for gate insulator and field isolation have hindered the realization of Ge MOS devices in the last four decades. Inspired by the recent successes of the high-k dielectric deposition technique on Si and the thermodynamically unstable nature of the common germanium native oxides, we have investigated the possibility of applying high-k dielectrics to Ge without a native oxide interlayer. We have fabricated MOS capacitors on Ge with zirconia gate dielectric using ultraviolet-assisted ozone (UVO) oxidation of thin Zr metal at room temperature on Ge surface with various treatments. In addition, this novel dielectric technology has led to the demonstration of high-performance Ge MOSFETs with enhanced carrier mobility. To study the scalability of the gate stack and inspect the existence of an interfacial layer, high-resolution cross-sectional transmission electron microscopy (HR-XTEM) was used to examine the ZrO2-Ge interface microstructure; though the poor phase contrast between ZrO2 and GeOx (if any) mandates a better physical characterization. In this presentation, we analyze the elemental composition variation across the dielectric layer by applying synchrotron radiation photoemission spectroscopy (SR-PES) to ZrO2 on Ge samples wet etched in an atomic layer scale. Core-level spectra for Ge have been taken at specific kinetic energies to minimize the Zr subshell photoemission cross-section and thus avoiding interference. These spectra were then peak-fitted and modeled to map out the elemental depth profile. Lastly, their impact on future Ge MOSFET scaling will be addressed.

11:00 AM B5.3/D5.3

integration of high-K dielectrics and metal gate electrodes with strained silicon channels. Yanxia Lin, Veena Misra and Mehmet C. Ozturk; Electrical and Computer Engineering, North Carolina State University, Raleigh, North Carolina.

Strained Si devices can provide significant mobility enhancements for both electrons and holes and is being aggressively studied by many research groups. The incorporation of high-K dielectrics on strained silicon provides the additional benefit of low gate leakage current. In addition, to eliminate gate depletion problems and Fermi level pinning associated with polysilicon electrodes, metal gates are also necessary. This warrants the investigation of high-K gate dielectrics and metal gate electrodes with strained Si devices. Issues that need to be understood include the i) interfacial layer formation of strained Si/high-K dielectrics, ii) effects of metal gate electrodes on high-K dielectrics, and iii) corresponding effects on the channel strain. In this paper, strained Si films were deposited on <100> relaxed SiGe virtual substrate by rapid thermal chemical vapor deposition (RTCVD). Different Ge compositions in the SiGe substrate and different strained Si thickness were formed to introduce varying strain levels which were confirmed by Raman spectroscopy. HfO2, one of the most promising high-K gate dielectrics, was deposited by physical vapor deposition (PVD) of thin Hf layers followed by oxidation at 600 C in N2 for 30seconds. Different metal gate electrodes, both element metal and binary metal alloys, were deposited by PVD and MOS capacitors were fabricated. The paper will discuss the electrical characteristics of metal-gate high-K dielectrics and present a comparison of EOT, flatband voltage, interface traps, leakage current and work function between strained Si samples and bulk Si controls. Also the interfacial layer formation of strained Si/high-K system will be investigated and compared with bulk Si/high-K. Finally, thermal stability of EOT, flatband voltage will also be presented.

11:15 AM B5.4/D5.4

Physical characterization of HfO2 deposited on Ge substrates by MOCVD. Sven Van Elshocht, Bert Brijs, Matty Caymax, Thierry Conard, Stefan De Gendt, Stefan Kubicek, Marc Meuris, Bart Onsia, Olivier Richard, Ivo Teerlinck, Jan Van Steenbergen, Chao Zhao and Marc Heyns; IMEC, Heverlee, Belgium.
Germanium is currently under consideration as a way to improve transistor performance because of its, compared to Si, intrinsically higher mobility. Germanium oxide, however, is inherently thermodynamically unstable, preventing formation of the gate dielectric by simple oxidation. A solution might be a high-k dielectric as much progress has been made depositing thin high-quality layers. Also from a high-k point of view germanium might prove to be beneficial: the instability of germanium oxide could limit the formation of an interfacial layer allowing more aggressive scaling; and the higher mobility might (partly) compensate for the mobility degradation seen for high-k dielectrics on Si. We studied the growth properties of HfO2 deposited on Ge by MOCVD, using TDEAH and

O2 as precursors, and compare the results to similar layers deposited on silicon substrates. Analysis techniques include Ellipsometry, Rutherford Backscattering Spectroscopy (RBS), Transmission Electron Microscopy (TEM), X-Ray Diffraction (XRD), and Time Of Flight Secondary Ion Mass Spectroscopy (TOFSIMS). Our results show that the physical properties of MOCVD-deposited HfO2 layers on Ge are very similar to what we have observed in the past for Si. Some of the negative aspects observed for Si, such as diffusion of substrate material in the high-k layer, a low density for thin layers, or a rough top surface, are comparable or more pronounced for the case of Ge. However, a careful surface pretreatment such as NH3 annealing the Ge substrate prior to deposition greatly improves the physical characteristics. Most important observation is a very thin interfacial layer as predicted, offering more aggressive scaling possibilities for Ge. In conclusion, based on physical characterization, the deposition of HfO2 on Ge by MOCVD results in layers of comparable quality compared to Si with as major difference a much thinner interfacial layer. Similar as for Si, surface pretreatments are shown to be very important.

11:30 AM B5.5/D5.5

Retarded Growth of Sputtered HfO_2 Films on Germanium.

Koji Kita, Masashi Sasagawa, Masahiro Toyama, Kentaro Kyuno and Akira Toriumi; Dept. of Materials Science, The Univ. of Tokyo, Tokyo, Japan.

Ge CMOS has recently attracted much attention, because of the trend of using deposited high-k films than thermally grown SiO_2 for further scaling of CMOS devices, and of the intrinsically higher carrier mobility of Ge than that of Si. In this paper, we report a new advantage of high-k/Ge systems over high-k/Si, that both the interface layer and the HfO_2film on Ge are thinner than those on Si despite of simultaneous fabrication processes. HfO_2 films were deposited simultaneously on Ge (100) and Si (100) wafers, after removing the native oxides. In order to restrict the interface layer growth, an ultra-thin Hf metal layer was deposited, followed by the HfO_2 film deposition by a reactive sputtering of Hf in O_2/Ar. By using TEM and a combination of the glazing incidence x-ray reflectivity (GIXR) with the spectroscopic ellipsometry measurements, the interface layer thickness was accurately determined to be 0.5 nm on Ge and 1.1 nm on Si, for the samples annealed at 500°C in O_2 (0.1%) +N_2 ambient. This result shows that the interface layer thickness on Ge is only a half of that on Si even though the films on both substrates were processed simultaneously. The ultra-thin Hf metal layer has an important role for thinner interface layer formation on Ge, since no difference of interface layer thickness was observed when HfO_2 films were deposited directly on both substrates without Hf metal layers. This phenomenon can be explained if it is assumed that Ge oxides may form a Hf-Ge-O ternary volatile compound with Hf metal. If this is the case, the total HfO_2 film thickness (without the interface layer) on Ge must be thinner than that on Si. The fact is that the HfO_2 film on Ge was 0.6 nm thinner than that on Si with TEM and GIXR measurements. Furthermore, the film thickness difference ($\Delta T_{HfO2} = T_{HfO2(onSi)} - T_{HfO2(onGe)}$) was detected even without annealing, and then it can be assumed Hf-Ge-O volatilization would occur during the film deposition process. It is worthy of particular attention that ΔT_{HfO2} was seen as a retardation of the film growth on Ge in the very early stage of the growth. Thus it is inferred that the Hf-Ge-O volatilization would occur with the assistance of oxygen plasma until the ultra-thin Hf metal is fully oxidized, and that it is the key mechanism for forming a thinner interface layer and a thinner HfO_2 film on Ge than those on Si. Finally, C-V characterisitcs of Au/HfO_2/Ge and Au/HfO_2/Si MOS capacitors were characterized. As was expected from the thickness difference of both interface layer and HfO_2 film discussed above, HfO_2/Ge MOS capacitor showed a larger accumulation capacitance than HfO_2/Si, even though they were fabricated simultaneously by the same process. These results show a new advantage of high-k/Ge over high-k/Si system from the viewpoint of fabricating a CMOS with ultra-thin high-k gate dielectric.

11:45 AM B5.6/D5.6

Metal Oxide/Semiconductor Interfaces in UV-Ozone Oxidized High-κ Dielectric Stacks on Si and Ge (001) Substrates.

David Chi[1], Chi On Chui[3], Shriram Ramanathan[2], Baylor Triplett[1], Krishna C. Saraswat[3] and Paul C. McIntyre[1]; [1]Department of Materials Science & Engineering, Stanford University, Stanford, California; [2]Components Research, Intel, Hillsboro, Oregon; [3]Department of Electrical Engineering, Stanford University, Stanford, California.

UV-ozone oxidation of hafnium and zirconium metal films to form HfO_2 and ZrO_2 gate dielectrics has been demonstrated to yield MOS gate stacks with low leakage current densities and very high capacitance densities. In this technique, metal precursor films are deposited directly on to the substrate and are subsequently transformed to metal oxides by exposure to oxygen in the presence of UV light. Because both Hf and Zr are highly reactive metals, interaction with the substrate after deposition but before oxidation is likely. In this presentation we describe characterization of the interface between UV-ozone oxidized dielectrics and Si and Ge substrates. We demonstrate reduction of the native oxide above Si and Ge as a result of Hf or Zr deposition. However, during UVO processing, oxidation of the substrate is observed. This byproduct silicon oxide exhibits different properties than the native oxide of Si. X-ray photoelectron spectroscopy indicates a sub-oxide or silicate/germanate at the high-k/substrate interface. Results from electrical testing of MOS-capacitors with a range of oxide thicknesses will also be presented.

SESSION B6: Strained Si and SiGe Devices I
Chair: Junichi Murota
Wednesday Afternoon, April 14, 2004
Room 2004 (Moscone West)

1:30 PM *B6.1

SiGe HBT/BiCMOS Technologies and Their Applications to Communication ICs/LSIs.

Katsuyoshi Washio[1], Katsuya Oda[1] and Takashi Hashimoto[2]; [1]Central Reserach Lab., Hitachi, Ltd., Tokyo, Japan; [2]Device Development Center, Hitachi, Ltd., Tokyo, Japan.

To meet the growing demand for multi-gigabit data communication systems and wide-bandwidth radio communication systems, both high-speed digital operation with sophisticated functions and high-frequency analog operation should be implemented. High-speed monolithic integrated circuits (ICs) and large-scale ICs (LSIs) are the key components for such systems. From this point of view, the high-speed SiGe heterojunction bipolar transistor (HBT) and SiGe HBT with CMOS (BiCMOS) technologies are the most promising candidates to meet these requirements. In this paper, technologies for a self-aligned SiGe HBT and BiCMOS developed for use in optical transmission and wireless communication systems are described. A Si-cap/SiGe-base multilayer fabricated by selective-epitaxial-growth (SEG) was used to obtain both high-speed and low-power performance for the SiGe HBTs. The process except the SEG is almost completely compatible with well-established Si bipolar-CMOS technology, and the SiGe HBT and BiCMOS were fabricated on a 200-mm wafer line. High-quality passive elements, i.e., high-precision poly-Si resistors, a high-Q varactor, an MIM capacitor, and high-Q spiral inductors have also been developed to meet the demand for integration of the sophisticated functions. Both cutoff frequency and a maximum oscillation frequency of 200 GHz, and an ECL gate-delay time of 4.9 ps have been demonstrated for the SiGe HBTs. An IC chipset for 40-Gb/s optical-fiber-links, a single-chip 10-Gb/s transceiver LSI, a 5.8-GHz electronic toll collection transceiver IC, and other ICs that are applicable to optical transmission and microwave/millimeter-wave wireless communication systems have been implemented by applying the SiGe HBT or BiCMOS technique.

2:00 PM B6.2

Optimizing SiGe HBTs technology using small signal and high frequency noise device's modeling.

Jean-Guy Tartarin[1], Gilles Cibiel[1], Augustin Monroy[2], Vincent LeGoascoz[2] and Jacques Graffeuil[1]; [1]CISHT, LAAS-CNRS, Toulouse, France; [2]ST microelectronics, Crolles, France.

Well known properties of BiCMOS technology over RF dedicated technologies in terms of integration (RF circuits on the same chip than base band modules) get advantage from the introduction of SiGe in the HBT's base layer to improve the device operating frequencies : these technologies suit very well with applications such as voltage control oscillators (VCO) and low noise amplifiers (LNA), thanks to their good behavior in terms of low frequency as well as high frequency noise performances respectively. We have investigated the influence of technological parameters such as doping profile, doping level and thickness of the base layer (4 different wafers) on the dynamic and high frequency noise performances to converge towards the optimum technological process (now available with the BiCMOS6G process provided by ST miroelectronics). We made use of S-parameters measurements on the devices to extract the electrical parameters of our small signal model (according to an original technique already published by the author). The high frequency noise parameters based on the electrical model (with noise sources added to the base-emitter junction, resistances, ...) are simulated and compared with the measured noise parameters of the devices. The four noise parameters (Fmin, Rn, and complex Γopt) measurements have been performed from 1 GHz to 12 GHz, and the dynamic S parameters measurements ranged from 40 MHz to 40 GHz. Good agreement has been found on both electrical small signal and noise model and the measurements. Thus, these models have been developed for several bias conditions : this study enabled the localization of potential technological defeats (etching, junction location, ...) and the identification of the limiting parameters on the transition frequency Ft and on the maximum oscillation frequency Fmax. The study on

technological parameters influence (doping profile, doping level and thickness of the base layer) has been led, based on the confrontation between electrical models issued from the different wafers. The homogeneity and reproducibility on the wafers have also been investigated. The noise performances of these devices have been found to be at a state of the art level (compared with devices featuring the same transition frequency Ft and maximum oscillation frequency Fmax) : LNAs demonstrators based on the optimized process have been designed and the results will also be presented at the conference.

2:15 PM *B6.3
Strained Silicon MOSFETs: The Next Material Change to Extend Moore's Law. scott emmet thompson, intel, hillsboro, Oregon.

The strong enhancement of hole and electron mobility via strain has been known for 50 years [1]. In fact, due to the large change in hole mobility in strained p-type silicon, it is the dominant diaphragm type pressure sensor [2]. However, until recently [3], there has been no high yield low cost process flow for strained silicon to improve both n and p-type MOSFET transistor performance even though advantages of introducing Si1-xGex are well known and proposed by Shockley in the late 1940's[4]. In this paper we will review the history of strained silicon MOSFETs. We will compare and contrast biaxial and uniaxial strained silicon MOSFETs and describe a high yield low cost uniaxial strained silicon process flow used in a 90 nm logic technology [3]. The process flow consists of selective epitaxial Si1-xGex in the source and drain regions to create longitudinal uniaxial compressive strain in the p-type MOSEFT. A tensile silicon nitride-capping layer is used to introduce tensile uniaxial strain into the n-type MOSFET and enhance electron mobility. The strained silicon increases the saturated n-type and p-type MOSFETs drive currents by 10 and 25%, respectively. The key advantage of using uniaxial strain (unlike biaxial [5]) is that the hole mobility enhancement is present at large vertical electric fields in nanoscale transistors making this strain technique useful for advanced logic technologies[6]. Next this work will quantify the theoretical maximum benefit from strain silicon and talk about the future direction of strained silicon for nanoscale technologies. It is the opinion of the author that due to the large performance advantage of strain silicon, all high performance advance logic technologies will incorporate strain silicon in the future. REFERENCES [1] C.S. Smith, "Piezoresistive effect in germanium and silicon," Phys. Rev., vol. 94, pp. 42-49, 1954. [2] B. Kloeck and N. F. DeRooij, "Mechanical sensors, " in Semiconductor Sensors, S. M. Sze, Ed. New York: Wiley, 1994. [3] S. Thompson et al., "A 90 nm logic technology featuring 50 nm strained silicon channel transistors, 7 layers of Cu interconnects, low k ILD, and 1mm2/ SRAM cell," IEDM Tech. Dig., pp. 61-64, 2002. [4] W. Shockley US Patent 2569347 1951. [5] K. Rim et al., "Strained Si for sub-100 nm MOSFETs," VLSI Tech. Dig., pp. 98-99, 2002. [6] S. Thompson et al, "A Logic Nanotechnology Featuring Strained Silicon" submitted to Elec. Device. Letters.

2:45 PM B6.4
Current/voltage analysis of junctions formed in strain relaxed SiGe. Geert Eneman[1,2], Anne Lauwers[1], Richard Lindsay[1], Peter Verheyen[1], Romain Delhougne[1], Roger Loo[1], Matty Caymax[1], Philippe Meunier-Beillard[1,3], Eddy Simoen[1], Steven Demuynck[1] and Kristin De Meyer[1,2]; [1]IMEC, Leuven, Belgium; [2]ESAT-INSYS, K.U. Leuven, Leuven, Belgium; [3]Philips-Research Leuven, affiliated to IMEC, Leuven, Belgium.

Performance gain and cost reduction have always been the driving factors for downscaling. As scaling progresses, performance gain becomes increasingly difficult to achieve. One way to overcome this is to enhance the mobility of the carriers in the channel. It has been extensively shown that a tensile biaxial strain in the Si channel can improve the mobility of both carrier types, resulting in increased drive current for both nMOS and pMOS. A commonly used method to obtain strain in the transistor channel is by growing a pseudomorphic Si layer on top of a Strain Relaxed SiGe Buffer (SRB). However, several integration issues have to be solved before SRBs can be implemented in CMOS. In this work, we studied the influence of the Ge content and the presence of dislocations on junction behavior. For this purpose we prepared vertical pn junctions through thin SRB layers. So, the depletion region crosses the dislocation area at the SRB/Si-substrate interface. The relaxation of SiGe layers is controlled by the incorporation of a thin carbon-containing layer in the SRB during the epitaxial growth. Our SRB fabrication scheme allows a low density of threading dislocations ($1x10^6 cm^{-2}$). An 8nm thick strained Si layer was grown on top of the SRB layer. Source/drain junctions were formed by implantation of As or P (nMOS) and B (pMOS) followed by conventional spike annealing. First measurements of the vertical junctions show that the reverse bias leakage of the n+/p and p+/n junctions formed in the SiGe SRB is increased by 4 orders of magnitude or more compared to the junctions obtained by the same implant and anneal conditions in bulk Si. The junction leakage increase is to be attributed to the lower bandgap of SiGe and to the presence of threading dislocations in the SRB. The influence of silicide formation on the junction leakage was found to be minor. The effect of SRB thickness and position of the C containing layer is investigated. The junction leakage is measured as a function of the reverse bias for different temperatures to identify the leakage mechanisms.

SESSION B7: Strained Si and SiGe Devices II
Chair: Ken Rim
Wednesday Afternoon, April 14, 2004
Room 2004 (Moscone West)

3:15 PM *B7.1
Theoretical Study of the Electron Mobility in Strained-Si MOSFETs. Massimo (Max) V. Fischetti[1], Francisco Gamiz[2] and Wilfried E Haensch[1]; [1]IBM Semiconductor Research and Development Center, IBM Research Division, T.J. Watson Research Center, Yorktown Heights, New York; [2]Departamento de Electronica y Tecnologia de Computadores, Universidad de Granada, Granada, Spain.

In this talk I will present our failed attempts at explaining the experimentally observed enhancement of the electron mobility in inversion layers of strained-Si MOSFETs. In bulk Si, tensile strain on the growth plane results in a splitting of the six-fold degenerate minima of the conduction band. The energy minima of the two ellipsoids characterized by a smaller in-plane effective mass is lowered and their thermal electronic population is enhanced. The resulting lower (with respect to relaxed Si) conductivity effective mass and the reduction of intervalley scattering processes yield a larger in-plane electron mobility. In this case, experimental observations and theoretical expectations are in agreement. However, when considering transport in inversion layers, the quantization of the electronic states already causes a splitting of the lowest-energy states: The ellipsoids with lower in-plane conductivity mass exhibit the largest out-of-plane effective mass. Thus, the energy of the associated two-fold degenerate subbands (the unprimed subbands) is lowered with respect to the energy of the four-fold primed subbands. This situation exactly parallels the effect of biaxial strain. Therefore, at sufficiently large confining fields, strain should have no effect significant on the electron mobility. Indeed, this situation had been observed experimentally and explained by G. Dorda [J. Appl. Phys. (1970)] in the case of very small, mechanically applied uniaxial strain (in the so-called piezo-resistive regime). Yet, experimentally, it is exactly when least expected (i.e., at large confining fields) that a significant enhancement of the electron mobility is observed (e.g., J. Welser *etal.*, 1994; Takagi *etal.*, 1996; Rim *etal.*, 1998-2001). Pushing the calculations of the electron mobility to the most realistic level we can handle has only confirmed the existence of this problem: The phonon-limited electron mobility in strained-Si inversion layers should be significantly enhanced (with respect relaxed Si) at small sheet densities (or confining fields), but the enhancement should quickly disappear at densities of technological interest ($?10^{13}$ cm^{-2}). A careful study of the effect of scattering with surface roughness, far from solving the problem, has only exacerbated its magnitude. Only an ad hoc assumption of a smoother Si-SiO2 interface with increasing strain explains the puzzle away. While perhaps far-fetched, earlier work by the Bell Lab group (Xie *etal.*, Phys. Rev. Lett. 1994) suggests that a Si surface under tensile stress may exhibit a larger dimer bond energy at terrace-steps, thus favoring a smoother surface. Finally, I will consider the effect of strain also for holes and on different surface orientations and will conclude with full-band Monte Carlo simulations of strained-Si MOSFETs of various channel lengths.

3:45 PM *B7.2
High-Performance SiGe MODFET Technology.
Steven J Koester, Jack O Chu, Q Christine Ouyang, Katherine L Saenger and John A Ott; IBM, Yorktown Heights, New York.

SiGe modulation-doped field-effect transistors (MODFETs) are promising devices for future RF communications applications due to their potential for higher speed and lower noise than conventional Si MOSFETs [1-2]. SiGe MODFETs are made even more interesting by the emergence of strained Si CMOS [3], which could enable a new high-performance mixed-mode technology, analogous to SiGe BiCMOS [4]. This paper provides an overview of recent results by IBM on SiGe p- and n-MODFETs, a comparison with competing Si technologies, and a discussion of challenges for further performance improvement. SiGe MODFETs utilize strained $Si_{1-x}Ge_x$ heterostructures to achieve enhanced carrier mobility compared to Si. The enhanced mobility arises from strain-induced band splitting that decreases the in-plane effective mass and intervalley scattering, as well as modulation doping which populates the quantum well with minimal ionized-impurity or interface-roughness scattering. Strained-Si channel n-MODFETs have been shown to produce electron mobilities about 4 times higher than Si/SiO_2 inversion layers, while $Si_{0.2}Ge_{0.8}$-channel (Ge-channel)

p-MODFETs display mobility enhancements as high as 6 (10). Recent device demonstrations at IBM include 100 nm gate-length Ge-channel p-MODFETs with trasconductance of 488 mS/mm (687 mS/mm) at room temperature (77 K) [5], $Si_{0.2}Ge_{0.8}$-channel p-MODFETs with f_{max} of 116 GHz [6], and 80 nm gate-length n-MODFETs with a record f_{max} of 194 GHz [7]. Both the p- and n-MODFETs also show excellent high- and low-frequency noise characteristics, that compare favorably to Si MOSFETs of similar dimensions. Numerical simulations have been used to develop an optimized MODFET design for operation at 200 GHz and beyond. The design requires a vertically-scaled layer structure, which is necessary for gate-length scaling below 100 nm [8], and a buried p-type body on SiGe-on-insulator (SGOI), which is necessary to control short-channel effects. Recently, several materials innovations needed for realizing this optimized MODFET design have been demonstrated, including thin regrowth of MODFET layer structures on p-well implanted buffers, and regrowth on thin SGOI layers [9]. The main challenges for further vertical scaling are the difficulty in achieving abrupt phosphorous doping profiles and mobility degradation arising from the proximity of the regrowth interface to the high-mobility channel. [1] K. Ismail, IEDM Tech. Digest, 509 (1995). [2] M. Enciso-Aguilar et al., Electron. Lett. 39, 149 (2003). [3] K. Rim et al., Symposium on VLSI Technology (2001). [4] D. Harame et al., BCTM (1997). [5] S. J. Koester et al., IEEE Elect. Dev. Lett. 21, 110 (2000). [6] S. J. Koester et al., IEEE Elect. Dev. Lett. 22, 92 (2001). [7] S. J. Koester et al., Electron. Lett., to be published. [8] Q. C. Ouyang et al., SISPAD (2002). [9] J. O. Chu et al., Spring MRS (2004).

4:15 PM *B7.3
Enhancing Mobility for High Performance MOSFETs.
Jeffrey Welser, SRDC, IBM TJ Watson Research Center, Yorktown Heights, New York.

As static power approaches active power in upcoming generations of IC chips, shrinking transistors to increase performance becomes less efficient. Other techniques to increase on-state current without an exponential increase in off-state leakage are required. Much recent work has focused on increasing carrier mobility in transistors by altering the Si crystal structure. To gain maximum benefit, these mobility improvements should be combined with conventional scaling, as well as other performance-improving structures such as SOI. This talk covers a variety of these combinations for high performance devices. Strained Si/relaxed SiGe layers can provide global, wafer-level strain to boost CMOS performance. A thin layer of Si grown on relaxed SiGe is tensily-strained, which increases electron mobility even at low strain levels. Increasing to higher strain results in corresponding enhancements in hole mobility as well. One drawback of this structure on bulk Si is that it often requires a thick layer of SiGe to achieve relaxation, which can result in higher junction leakage due to the lower SiGe bandgap and residual defects from the relaxation process. Fabricating these layers on SOI can eliminate the leakage concerns, while transistor performance is further improved by the SOI itself. Moreover, thermal mixing techniques can be used on SOI to greatly reduce the SiGe thickness, while bonding techniques can remove the SiGe entirely, resulting in an all-silicon, ultra-thin body strained SOI device. In addition to global strain provided by wafer level epitaxy, local strain of individual transistors is possible. This can be achieved by varying the strain states of the insulating materials deposited on the transistors, or by varying the isolation and source/drain materials and fabrication. Local techniques offer an advantage in tuning stress to compressive for PFETs and tensile for NFETs, to achieve maximum enhancement at the lowest strain. However, the amount of strain achieved can vary with transistor geometry, and maintaining proper strain throughout processing can be challenging. Despite these concerns, local strain can be combined with SOI or global strain, to further enhance performance. Crystal orientation can also improve carrier mobility. Since the maximum mobility for holes and electrons is achieved on different Si surface orientations, the challenge is to build a structure with high mobility for both carriers simultaneously. Recently such a structure was demonstrated on SOI wafers, and further optimization is possible by combining this structure with strain. Enhancing carrier mobility in Si transistors offers great promise for improving CMOS performance. Understanding all the strain and orientation techniques and how they interact with each other and with other device enhancements, such as SOI and double gates, in the ultra-short channel regime, will be key to obtaining the optimum power/performance tradeoff in future transistors.

4:45 PM B7.4
High Mobility SiGe/Si n-MODFET Structures and Devices on Sapphire Substrates. Carl H Mueller[1], Samuel A Alterovitz[2], Edward T Croke[3] and George E Ponchak[2]; [1]Analex Corporation, Cleveland, Ohio; [2]NASA Glenn Research Center, Cleveland, Ohio; [3]HRL Laboratories LLC, Malibu, California.

SiGe/Si modulation doped field effect transistors (MODFETs) are currently under intensive development for high frequency applications. However, the substrate normally used is Si, which causes large losses in the passive elements required for a complete high frequency circuit. Because of its high electrical resistivity, sapphire is an almost perfect substrate for high frequency passive components, and integration of these two components is highly desirable. Furthermore, sapphire offers better device isolation, which is essential for system-on-a-chip development, than substrates such as high resistivity Si. We have designed, fabricated, and measured SiGe/Si n-MODFET structures on sapphire substrates and measured electron mobilities over 1,200 and 13,000 cm^2/V-sec at room temperature and 250 millikelvins, respectively. The electron carrier densities were 1.6 and $1.33x10^{12}$ cm^{-2} at room and liquid helium temperature, respectively, denoting excellent carrier confinement. Shubnikov de-Haas oscillations were observed, thus confirming the 2D nature of the carriers. The structures were deposited using molecular beam epitaxy (MBE), and the Sb dopants were introduced using a delta doping technique. In an alternate process, we introduced phosphorus dopants via ion implantation and annealing into undoped MBE samples. Using the MBE Sb doped structures, transistors with varying source-to-drain distances and gate lengths (1 to 5 microns) were fabricated. Although the design is not optimized, the initial results are promising. At room temperature and zero gate voltage, the transistors were normally on and were depleted with a gate bias of -0.7 V. The I-V behavior indicated the saturated drain current region extended over a wide drain voltage range, with knee voltages of approximately and 0.5 V and increased leakage starting at voltages slightly higher than 4 V. The saturation drain currents were lower than expected, and reasons for this are under investigation. A shortcoming of the aforementioned transistors is that the MODFET structures were fabricated using a very thick buffer layer. So as to enable the transistor to operate in fully depleted mode and simplify future integration of the SiGe/Si analog with Si digital circuitry, we are investigating the use of thinner buffer layers (well below 1 micron) to support growth of the high mobility n-MODFET channels. Results of this work will be presented.

SESSION B8: Poster Session
Chair: Paulo Fichtner
Wednesday Evening, April 14, 2004
8:00 PM
Salons 8-9 (Marriott)

B8.1 TRANSFERRED TO B1.5

B8.2
Strain relaxation and threading dislocation density in He-implanted and annealed $Si_{1-x}Ge_x$/Si (100) heterostructures. Juan Cai[1], Patricia M. Mooney[1], Jack O. Chu[1], H. Chen[2], S. H. Christiansen[3] and John A. Ott[1]; [1]IBM T. J. Watson Research Center, Yorktown Heights, New York; [2]IBM Microelectronics Division, East Fishkill, New York; [3]MPI-Mikrostrukturphysik, Halle, Germany.

Ideal $Si_{1-x}Ge_x$ virtual substrates for strained Si devices must have a high degree of strain relaxation, a flat surface and a low threading dislocation density. Recently, helium implantation and subsequent annealing of thin SiGe/Si (100) structures was proposed as a new method for producing high quality SiGe layers [1]. It was found that helium implantation before annealing greatly enhances the strain relaxation of metastable SiGe layers [1,2]. We have investigated strain relaxation and threading dislocation densities in $Si_{1-x}Ge_x$ (x=0.2 and 0.3) buffer layers produced by this method with x-ray diffraction and plan-view transmission electron microscopy, respectively. The influence of experimental parameters, such as layer thickness and helium implantation dose and depth, on the properties of these buffer layers has been studied. The degree of strain relaxation is very sensitive to the SiGe layer thickness; however, a similar degree of strain relaxation is obtained when the helium dose and energy are varied over a relatively wide range. In contrast, the threading dislocation density is strongly influenced by the implantation dose and depth. A composite parameter, the He dose in the SiGe layer calculated from He profiles simulated using the program Stopping and Range of Ions in Matter (SRIM), was identified as a key factor for the threading dislocation density. When this parameter increases by one order of magnitude, the threading dislocation density increases by three orders of magnitude. We have found that to achieve a low threading dislocation density, $<5x10^7$ cm^{-2}, the He dose in SiGe must be less than $1x10^{15}$ cm^{-2}. This study defines the optimal SiGe buffers that we can obtain by helium implantation and annealing, and quantitatively identifies conditions to produce such materials. 1. M. Luysberg, D. Kirch, H. Trinkaus, B. Holländer, St. Lenk, S. Mantl, H.-J. Herzog, T. Hackbarth, P. F. P. Fichtner, J. Appl. Phys. 92, 4290 (2002). 2. S. H. Christiansen, P. M. Mooney, J. O. Chu and A. Grill, Mat. Res. Soc. Symp. Proc. 686, 27 (2002).

B8.3

The role of internal dislocation sources for the strain relaxation of pseudomorphic SiGe/Si structures. Martina Luysberg[1], Norbert Hueging[1], Steffi Lenk[2], Dan Buca[2], Bernd Hollaender[2], Siegfried Mantl[2], Marcio J. Morschbacher[3], Paulo F. P. Fichtner[3], Roger Loo[4] and Matty Caymax[4]; [1]Institute of Solid State Research, Research Center Juelich and cni - Center of Nanoelectronic Systems for Information Technology, Juelich, Germany; [2]Institute of Thin Films and Interfaces, Research Center Juelich and cni - Center of Nanoelectronic Systems for Information Technology, Juelich, Germany; [3]University Federal do Rio Grande do Sul, Porto Alegre, Brazil; [4]IMEC, Leuven, Belgium.

Strained Si technology offers new prospectives for high perfomance MOS applications. A promising way to introduce strain into thin Si films is the growth onto relaxed SiGe layers. Nearly complete relaxation of SiGe layers grown on Si substrates are achieved by He implantation and subsequent annealing. The key issue of this process is the introduction of He bubbles acting as internal dislocation sources below the film/substrate interface. To date the dislocation formation and of the relaxation mechanism are not understood in detail. In our work, ex-situ and in-situ transmission electron microscopy are employed to study the evolution of the bubble and dislocation structure with increasing annealing temperature. CVD grown SiGe layers with Ge contents of 20 to 26 atpercent on Si (100) substrates were implanted with He doses in the range of 7 10^{15} to 1.5 10^{16}cm^{-2} and subsequently annealed at 200 °C up to 950 °C. The implantation energy was chosen such that the implantation depth equals twice the SiGe layer thickness. Elastic recoil detection analyses revealed that already at low annealing temperatures significant amounts of He left the sample. At about 400 °C He platelets with a pressure up to 15 GPa are formed. Already during this stage dislocation loops are observed, which are attached to the He platelets. With increasing temperature the He platelets undergo a shape transformation to almost spherical bubbles. Simultaneously, the He content further decreases until at 700 °C no He is detectable. The onset of relaxation measured by angular resolved ion channeling occurs at 600 °C. At this temperature the dislocation loops are observed to detach from the He bubble. Increasing the temperature further leads to an increase of the degree of relaxation up to 70 percent at a temperature of 950°C, accompagnied by the formation of a dense array of misfit dislocations. The interplay between He implantation induced bubbles and dislocation formation, movement and interaction will be discussed in view of the relaxation of the SiGe layers.

B8.4

Island Scaling Effects on Photoluminescence of Strained SiGe/Si (100). Rebecca Lorenz Peterson, Haizhou Yin and J C Sturm; Center for Photonics and Optoelectronic Materials, Princeton University, Princeton, New Jersey.

The fabrication of electronic devices on semiconductor islands is becoming increasingly common because of silicon-on-insulator technology and/or because of strain engineering in compliant substrate approaches [1]. While photoluminescence (PL) can be an accurate probe of Ge content and strain, in islands it can be affected by the presence of the island edges. Here we present data and a model showing that for high quality SiGe, edge effects are critical for sizes under 20 μm. A pseudomorphic 10 nm $Si_{0.8}Ge_{0.2}$ layer was grown on an n-type Si (100) substrate using rapid-thermal chemical vapor deposition, and capped with a 13 nm Si layer [2]. Square island arrays were dry-etched with island edge lengths from 5 to 500 μm and inter-island spacings of 1 to 20 μm, respectively. PL was measured using a 514 nm Argon ion laser at 77K. Band-edge PL in SiGe/Si structures comes from the recombination of carriers (or excitons) in the SiGe layer. The carriers are generated in substrate Si and diffuse to be collected by the SiGe [3]. PL for Si results from carriers that recombine in the Si substrate before making it to SiGe. PL from the $Si_{0.8}Ge_{0.2}$ layer consists of two peaks, one from recombination assisted by transverse optical (TO) phonons (945 meV) and one from non-phonon (NP) recombination, which occurs due to alloy scattering (1000 meV). Only the TO peak is observed from the Si substrate (1100 meV). In unpatterned samples, most carriers recombine in SiGe so that SiGe PL peak intensities are 5x times that from the Si substrate. No dislocation or defect peaks are visible, indicating coherent growth and good epitaxial interface quality [3]. For island sizes less than 100 μm, the SiGe TO (and NP) peak heights, relative to the Si TO peak height, decrease rapidly from 5.0 for uniform or large island samples to less than 0.02 for 5 μm islands. This indicates that for small islands sizes most carriers diffuse laterally in the SiGe after collection to combine at surface defects at the exposed SiGe edges, and thus are not available for band-edge PL. These defects are evidenced by the appearance of a new PL band for islands sizes of 40 μm or less. A model was devised to predict the decrease in PL from carriers' diffusion to island edges and a minority carrier diffusion length of 17 μm was extracted from the model. This implies (assuming D=10cm^2/s and infinite surface recombination at the edges) a lifetime of order of 0.3 μs, showing the high quality of our material. Works in progress to be presented include annealing and passivation of SiGe edges by epitaxial regrowth and application to relaxed SiGe/Si-on-insulator structures. This work is supported by DARPA/ONR N66001-00-10-8957 and ARO DAA655-98-1-0270. 1. H. Yin, et al., to be published at International Electron Devices Meeting (IEDM), Washington, DC, December 2003. 2. J. Sturm, et al., J. Vac. Sci. Technol. B 9, 2011 (1991) 3. A. St. Amour, et al., Appl. Phys. Lett. 65, 3344 (1994)

B8.5

CMOS Compatible Liquid-Phase Epitaxial Growth of Ge on Si Substrates. Yaocheng Liu[1], Michael D Deal[2] and James D Plummer[2]; [1]Materials Science and Engineering, Stanford University, Stanford, California; [2]Electrical Engineering, Stanford University, Stanford, California.

Ge has gained increased interest due to its high carrier mobility as MOSFET channel material and its applications in optoelectronics. It is particularly attractive if Ge devices can be integrated into Si-based processing. However, epitaxial growth of Ge directly on Si substrates is very difficult as the lattice mismatch between these two materials causes a very high density of defects. We have developed a simple method to make high quality single-crystal Ge structures by direct heteroepitaxial growth from Si substrates. This method makes use of the defect necking technique similar to that in Czochralski crystal growth. We deposited amorphous Ge on Si substrates and pre-patterned the Ge films to desired structures with small necking zones. Then solid-phase epitaxy (SPE) and liquid-phase epitaxy (LPE) were used to crystallize the Ge structures. Since Si and Ge are diamond structure crystals, with {111}<110> slip systems, the threading dislocations formed due to the lattice mismatch tend to lie along <110> directions on {111} planes. As a result, the dislocations and stacking faults were terminated within the necking zones and the Ge crystals beyond had high quality. Pillar structures were used to demonstrate the working mechanism. Furnace anneal was used for the SPE experiments. The SPE Ge pillars had most of the misfit defects terminated in the necking zones, but some new defects were generated at the sidewalls. The LPE samples were heated up to 940°C for 2 s by rapid thermal annealing (RTA) to melt the Ge and cooled down naturally in the RTA chamber. The Ge pillars were covered with a conformal oxide layer, which acted as micro-crucibles holding the Ge liquid from flowing randomly. Epitaxial growth occurred as the Ge liquid was cooling down. TEM study showed that LPE method can produce very high quality Ge crystals, with all the misfit defects terminated in the necking zones near the Si-Ge interface and no new defects were generated at the sidewalls of the Ge pillars. The LPE technique was successfully applied to the fabrication of Ge-on-insulator (GOI) structures. No defects could be detected with TEM in the LPE Ge films beyond the necking zones. Further experiment showed that the epitaxial growth overwhelmingly dominated the crystallization of liquid Ge - the homogeneous or heterogeneous nucleation rates were very slow. More than 20 μm long, high quality single-crystal Ge films on insulator were obtained with the LPE technique. The orientations of the Ge films were controlled by the Si substrates. Electrical measurement showed high carrier mobility for the prepared GOI structures. With this technique, Ge structures can be integrated on Si substrates at desired locations with an acceptable thermal budget, so it can be an enabling technology for Ge device fabrication, 3D integrated circuits, and heterogeneous integration.

B8.6

Effect Of Point Defect Injection On Diffusion Of Boron In SiGe:C Between 940 - 1050 Degrees Celsius. Mudith S A Karunaratne[1], Janet M Bonar[2], Jing Zhang[3] and Arthur F Willoughby[1]; [1]Materials Research Group, School of Engineering Sciences, University of Southampton, Southampton, Hampshire, United Kingdom; [2]Micrelectronic Research Group, School of Electronics and Computer Science, University of Southampton, Southampton, Hampshire, United Kingdom; [3]Department of Physics, Imperial College, London, United Kingdom.

The effectiveness of C as a suppressant of B diffusion is underpinning the advancement of the SiGe HBT technology. This so called 'C-effect' has also been observed in Si and is generally attributed to an undersaturation of interstitials caused by the out-diffusion of C from carbon rich regions. Point defect injection experiments provide a powerful tool to investigate such mechanisms, as it allows separate perturbation of interstitial and vacancy point defect densities. In this paper, we compare B diffusion measurements in epitaxial Si, Si with C, SiGe and SiGe:C under interstitial, vacancy and non-injection conditions in order to investigate the variation in point defect densities caused by inclusion of C. Boron containing marker layers of either Si or strained SiGe were grown on CZ (100) wafers using gas source MBE. Some of the wafers additionally contained a grown-in carbon peak. Each wafer was divided in to three sections; on the first

section a silicon nitride layer was deposited using LPCVD over a pre-deposited low temperature oxide (LTO) layer. The second section had only the nitride layer while the third section was left uncoated. We expect inert, vacancy and interstitial injection conditions to exist in the first, second and third sections, respectively during annealing in an oxygen ambient. These samples were rapid thermal annealed (RTA) at a number of temperature/time combinations between 940-1050 degrees Celsius in oxygen. Diffusion coefficients were extracted by computer simulation, using SIMS profiles obtained from samples before and after the RTA treatment. For samples annealed at 1050 degrees Celsius for 15s, the diffusivity extracted is compatible with values published by Fair for inert diffusion, suggesting the MBE material was of fairly high quality with a low density of grown-in defects. Diffusion of B is highest in pure Si, reduced by the incorporation of 11% Ge, reduced further in Si with 0.1% C, and the lowest value in SiGe:C. In Si, Si:C and SiGe containing samples which experienced interstitial injection during annealing, a marked increase in B diffusion was observed, compared to the inert case. In samples which experienced vacancy injection, B diffusion was suppressed for the Si, Si:C and SiGe containing samples. The increase in diffusivity for the carbon-containing samples under interstitial injection annealing conditions suggests the undersaturation of interstitials by C is probably not infinite, as the injected flux of interstitials seems to overwhelm the suppression effect by C.

B8.7

Ge MOS Dielectric Stack with ALD High-k Metal Oxide and Oxynitride Interlayer. Chi On Chui[1], Hyoungsub Kim[2], Paul C. McIntyre[2] and Krishna C. Saraswat[1]; [1]Electrical Engineering, Stanford University, Stanford, California; [2]Materials Science and Engineering, Stanford University, Stanford, California.

Future scaling of Si MOSFET devices may be limited by drain current saturation. It has been proposed that the higher intrinsic carrier mobility of Ge could alleviate the limit by providing a higher source injection velocity, which results in higher drive current and smaller gate delay. To circumvent the long-lasting problem of poor Ge native surface passivation, high-k metal oxides have been introduced as the gate dielectric materials for Ge MOS applications. Among other deposition techniques, atomic layer deposition (ALD) is particularly attractive in terms of precise thickness control and near-perfect conformality for ultrathin high-k formation. On Ge surfaces after HF vapor exposure, we have demonstrated previously locally epitaxial growth of ZrO2 on Ge without a distinct interfacial layer. Due to the large lattice mismatch between ZrO2 and Ge, the electrical characteristics of these MOS capacitors were not satisfactory. By incorporating a Ge oxynitride interlayer before the ALD of high-k on Ge, excellent MOS capacitors could be obtained with very low leakage. In this presentation, we compare the high-k/Ge interface microstructure with various surface treatments including Ge oxynitride formation. The oxynitride interlayer was formed using rapid thermal nitridation (RTN) in NH3 ambient. High-resolution transmission electron microscopy (HR-XTEM) has been used for cross-sectional imaging. To confirm the nitrogen incorporation on Ge surface while optimizing the RTN condition for the best electrical results, extensive x-ray photoemission spectra (XPS) have been taken and the nitrogen percentage has been extracted as a function of temperature. On the optimum Ge oxynitride film, wet chemical processing stability have been investigated and the film has shown to be have minimum solubility in DI water, but soluble in HF. Lastly, both the C-V and I-V characteristics of these MOS capacitors will be presented and the impact of the interlayer on the future Ge MOS device scaling will be discussed.

B8.8

Growth of High-Performance SiGe MODFET Layer Structures. Jack O. Chu, Steven J. Koester, Qiqing C. Ouyang, John A Ott, Leathen Shi and Katherine L Saenger; IBM TJ Watson Research Center, Yorktown Heights, New York.

SiGe modulation-doped field effect transistors (MODFETs) are an interesting emerging technology option for high-performance communications applications, due to their potential for higher speed and lower noise operation than Si MOSFETs [1-2]. However control of short-channel effects in sub-100nm gate-length MODFETs is difficult due to the large gate-to-channel distance[3] and because counter-doping in the channel can lead to mobility degradation. In this paper we describe the regrowth of vertically-scaled Si/SiGe n-MODFET layer structures on buried p-type layers and thin SiGe-On-Insulator(SGOI) substrates, and also show that these innovations should enable the realization of MODFETs with f_{max} well over 200 GHz. The layer structures were grown by UHV-CVD on 8" Si(100) wafers and consisted of a $Si_{0.7}Ge_{0.3}$ bottom barrier layer, a strained Si quantum well, a top undoped $Si_{0.7}Ge_{0.3}$ spacer layer, a n-$Si_{0.7}Ge_{0.3}$ phosphorous doped supply layer and a Si cap layer. The spacer and supply layers were appropriately reduced or scaled for improved performance by leveraging reduced growth rate effects for P in order to improve the steady-state incorporation of phosphorous[4]. In this way, layer structures with "thinner" n+SiGe supply layers of <10nm were grown with carrier densities of $2x10^{12}cm^{-2}$ and no mobility degradation was observed when compared to thicker samples. We have also demonstrated for the first time the growth of similar scaled layer structures on p-well implanted SiGe buffer layers. However, it was found that reduced temperature conditions were needed for the initial regrown layers to prevent 3D growth. Using lower temperature conditions Si quantum wells as close as 20nm to the regrowth interface were grown without mobility degradation compared to control samples, though some carrier depletion was observed. Finally, we have demonstrated the regrowth of high performance MODFET layer structures on thin SGOI substrates. The SGOI substrates were fabricated by wafer bonding, and consisted of a relaxed $Si_{0.7}Ge_{0.3}$ layer with thickness of 50nm. The regrown MODFET layer structures on SGOI substrates have shown high room-temperature mobility of >1700 cm^2/Vs, a value comparable to bulk controls. The total SGOI thickness after regrowth was about 100nm, which is considerably thinner than in previous work[5]. The current SGOI layer structures are planned to be used for fabricating 50nm gate-length MODFETs, which according to numerical simulations should produce f_{max} values over 200 GHz, while still maintaining acceptable voltage gain and good turn off characteristics. [1] S.J. Koester et al, Spring MRS (2004). [2] M. Enciso-Aguilar et al., Electron. Lett. 39, 149 (2003). [3] C. Ouyang et al., SISPAD (2002). [4] J.O. Chu et al, Spring MRS (1996). [5] J.O. Chu et al, Spring MRS (2001).

B8.9

Heteroepitaxial growth and characterization of Ge and SiXGe1-X films on patterned silicon structures*. Ganesh Vanamu[1], Abhaya K Datye[1] and Saleem H Zaidi[2]; [1]Chemical and Nuclear Engineering, University of New Mexico, Albuquerque, New Mexico; [2]Gratings, Inc., Albuquerque, New Mexico.

Epitaxial growth has often been a key component in the development of new materials. Recently, there has been a great interest in strained Si-based heterostructures to achieve high mobility optoelectronic materials.In order to produce relaxed Si1-xGex on a Si substrate, conventional practice has been to grow a uniform, graded, or stepped, Si1-xGex layer beyond the metastable critical thickness. The aim of the various buffer structures is to reduce the threading dislocation density in the epilayer. This work is based on novel 2-D structures on the silicon surface that facilitate strain relief and allow us to obtain epilayers that are free of defects. Conventional lithography techniques have been combined with reactive ion and wet-chemical etching to fabricate a 2-D patterns of silicon mesas. The pitch of the pattern was kept constant while the width of the posts was varied. Heteroepitaxial growth of Ge/SixGe1-x layers on these micrometer-scale structures was investigated. These types of structures can potentially absorb thermal expansion and lattice expansion mismatch as well as enable liftoff of heteroepitaxial layers for subsequent wafer reuse. While, keeping the growth parameters constant, the geometry of the structures was varied to determine the optimum configuration for the highest quality heteroepitaxial growth. In this work, the quality of the Si1-xGex buffer system was investigated using high-resolution x-ray reciprocal space mapping by triple-axis x-ray diffractometry. We have used transmission electron microscopy (TEM) to analyze the epilayer cross-sections. Surface morphology was analyzed using scanning electron microscopy (SEM), atomic force microscopy (AFM) and optical microscope. Our results show that the quality of the heteroepitaxial layers improves as the width of the posts in the 2-D pattern was decreased. *This research was performed using the facilities at the Center for High Technology Materials at UNM.

B8.10

Diffusion of Boron and Silicon in Germanium. Suresh Uppal[1], Arthur F. W. Willoughby[1], Janet M. Bonar[2], Nick E. B. Cowern[3], Tim J. Grasby[4], Mark G. Dowsett[4] and Richard J. H. Morris[4]; [1]Materials Research Group, University of Southampton, Southampton, Hampshire, United Kingdom; [2]Department of Electronics and Computer Science, University of Southampton, Southampton, Hampshire, United Kingdom; [3]School of Electronics, Computing and Mathematics, University of Surrey, Guildford, United Kingdom; [4]Physics Department, University of Warwick, Coventry, United Kingdom.

Channel engineering in combination with ultra shallow junctions using ion implantation has shown potential for improvement in performance of existing MOSFET devices. On material front, strained Si, $Si_{1-y}Ge_y$, and Ge layers grown on $Si_{1-x}Ge_x$ (y>x) virtual substrates are prospective candidates especially for p-type MOSFET. In the present work, the diffusion of boron and silicon in germanium is studied using implantation doping. Concentration profiles after furnace annealing in the temperature range 675-900°C were obtained using high resolution secondary ion mass spectroscopy (SIMS). Diffusion coefficients are calculated by fitting the annealed profiles

using TSUPREM. For boron, we obtain diffusivity values which are two orders of magnitude slower than previously reported in literature. An activation energy of 4.6(±0.3)eV is calculated for boron diffusion in germanium. The results suggest that diffusion mechanism other than vacancy should be considered for boron diffusion in germanium. For silicon diffusion in germanium, the diffusivities values calculated in this work are in agreement with previous work. The activation energy of 3.2(±0.3)eV for silicon diffusion is closer to that for germanium self-diffusion suggesting that silicon diffusion in germanium occurs via the same mechanism as germanium self-diffusion.

B8.11
Phosphorus and Boron Implantation into (100) Germanium. Yong Seok Suh[1], Roland A. Levy[1], Malcolm S. Carroll[2] and A. Sahiner[3]; [1]Materials Science and Engineering, New Jersey Institute of Technology, Newark, New Jersey; [2]Agere Systems, Allentown, Pennsylvania; [3]Evans East, E. Windsor, New Jersey.

Recent advances in process technologies, such as high-κ gate dielectrics used for high mobility germanium MOSFETs and relaxed graded buffer layers for fabrication of high quality germanium photodetectors on silicon, have created renewed interest in device fabrication with germanium. Implantation and dopant activation are crucial steps for these device structures, for which critical modeling parameters that are typically available for silicon fabrication (e.g. Pearson's implant parameters, dopant diffusivities, and solid solubilities) are either not reliable or are not readily available for germanium. In this study, we present secondary ion mass spectrometry (SIMS) and spreading resistance profiling (SRP) measurements of boron and phosphorus implants into Ge before and after dopant activation anneals. Germanium (100) n- and p-type substrates are implanted at 7° tilt with $^{31}P^+$ or $^{11}B^+$ using energies ranging from 20 to 320 keV and doses of 5×10^{13} to 5×10^{16} cm^{-2}. The SIMS as-implanted profiles (i.e. chemical profiles) are compared to SRIM simulations, which are found to significantly underestimate the trailing edge of the profiles, presumably due to channeling (e.g. the straggle or the second moment of the SIMS profiles are as much as 52% greater than that calcualted by SRIM). The profiles are therefore characterized using Pearson distributions, for all conditions, to improve modeling of the implants in this range of energies and doses. Sheet resistances of the 5×10^{13}, 1×10^{15}, and 5×10^{16} cm^{-2} boron implants are 388, 171, and 18 ohms/sq immediately after implantation indicating significant boron activation without additional annealing. Using previously reported single crystal mobilities [Sze] to make a lower estimate of the boron activation from the SRP and SIMS profiles, the peak active boron concentration is found to be 65, 8.1, and 2.3% of the peak chameical concnetration for the same respective doses. In contrast, phosphorus activation is below that of the background for all cases immediately after implant. To examine dopant activation, the samples are annealed for 3 hours at either 400, 600 or 800°C in high purity N_2. Phosphorus activation is observed to increase after annealing at 400 and 600°C for 3 hours. Furthermore, a significant amount of phosphorus diffusion is observed after 600°C annealing, which is characterized by a relatively immobile peak and a relatively long tail of 10^{19} cm^{-3} extending approximately 1.5 μm into the substrate. In contrast, relatively little boron diffusion or increase in boron dopant activation is observed even after annealing at 400 or 600°C, although active concentrations are observed to be as much as 100 times greater than a previous reported solid solubility (10^{18} cm^{-3}). Annealing at the higher temperature to improve dopant activation, 800°C for 3 hours, results in substantial roughening of the surface, perhaps due to nitridation of the exposed germanium surface reported to commence as low as 700°C.

B8.12
Strain relaxation of epitaxial SiGe layers by He implantation. Dan Mihai Buca[1,3], Bernd Hollaender[1,3], Steffi Lenk[1,3], Siegfried Mantl[1,3], Martina Luysberg[2,3], Norbert Hueging[2,3], Roger Loo[4] and Matty Caymax[4]; [1]Institut fuer Schichten und Grenzflaechen, Forschungszentrum Juelich, Juelich, Germany; [2]Institut fuer Festkoerperforschung, Forschungszentrum Juelich, Juelich, Germany; [3]cni - Center of Nanoelectronic Systems for Information Technology, Juelich, Germany; [4]IMEC, Leuven, Belgium.

We studied He implantation induced strain relaxation of pseudomorphic $Si_{1-x}Ge_x$ layers on Si(100) substrates grown by chemical vapor deposition and molecular beam epitaxy. He implantation below the $Si_{1-x}Ge_x$ layer induces a defect band in the underlying Si that promotes strain relaxation of the SiGe layer. The influence of the implantation parameters, the annealing temperature, layer thickness and germanium content on the degree of relaxation was systematically investigated for $Si_{1-x}Ge_x$ layers with thicknesses between 75 and 420 nm and Ge concentrations within the range of 19 to 31 at %. The implantation energy was varied such that the maximum He concentration was located at a depth of 50 - 300 nm below the SiGe/Si interface and He ion doses within the range of $4\text{x}10^{15}$ to $2\text{x}10^{16}$ cm^{-2} were used. We investigated the relaxation process by the use of plane view and cross-sectional transmission electron microscopy and Rutherford backscattering spectrometry and ion channeling. In summary, we found that for efficient relaxation the optimum parameters lie in the "low dose, deep implant regime". Following this rule, high degrees of relaxation up to 80 % and low threading dislocation densities of $5\text{x}10^6$ cm^{-2} were achieved after anneals at 850°C. A very small surface roughness (rms) of typically 0.6 nm was measured using atomic force microscopy.

B8.13
Atomic Force Microscopy Study of Conformal Sputtering in Strained Silicon Samples. Kuo-Jen Chao and Gary Goodman; Charles Evans & Associates, Sunnyvale, California.

Outdiffusion of Ge into the Si cap in strained Si/SiGe is a key parameter to understand, both from an epitaxial growth rate standpoint and from a CMOS thermal budget standpoint. Similarly, the depth distribution of dopants in the Si/SiGe system is critical. SIMS is the principal analytical technique to measure the outdiffusion of Ge and the depth profile of dopants. However, there is a question as to whether the cross hatch pattern in Si/SiGe degrades the SIMS depth resolution, or alters the accuracy of the depth profile. The peak-to-valley of the cross hatch pattern may range from 10's nm in non-CMP'ed samples down to several nm's in CMP'ed samples. Experimentally studying this possible effect has been challenging. Here we report on a novel AFM approach to show that the SIMS measurement process results in conformal sputtering, thus maintaining the excellent depth resolution and depth distribution accuracy capability of SIMS for these material systems. In this work, Atomic Force Microscope (AFM) has been applied to study the surface morphology issue of the strained Si samples, before and after SIMS. Two strained Si samples grown at similar conditions were investigated. One of the samples was chemical mechanical polished after the growth of the Si1-xGex cap layer, but the other sample was not. We used the SIMS (PHI ADEPT 1010) 1KeV Cs+ ion beam to sputter each of these two samples to create three rectangular craters and remove layer materials of different thickness for each crater. Normally, the SIMS crater has a wide and gradual slope as seen by AFM. However, we have found a novel approach that results in a much sharper drop in the crater edge as seen by AFM. AFM measurement across the original surface and down into the crater show that the surface roughness of the crater bottom is on the same order as the surface roughness of the near-by top surface. Neither sputtering smoothing effect is found for the non-CMP'ed sample, nor sputtering roughening effect is found for the CMP'ed sample. Furthermore, the cross hatch patterns seen at the crater bottom have been found to be similar to the cross hatch patterns in the near-by top surface for all three different depths of craters of the non-CMP'ed sample. This finding indicates that the applied ion beam sputtering process is a conformal sputtering process. As an example of the excellent SIMS depth resolution for measuring Ge outdiffusion in Si/SiGe, we will show SIMS profiles with the depth resolution of 8Å/Dec even though the cross hatch peak to valley was on the order of 30nm.

B8.14
Formation of Novel SiGe-on-Insulator Substrate Structures by Ge+ Implantation and Oxidation for Strained-Si MOSFETs Technology. Hyungsang Yuk, Kristel Fobelets and Tom Tate; Electrical and Electronic Engineering, Imperial College London, London, United Kingdom.

A new fabrication technique for Silicon-Germanium-on-Insulator (SGOI) substrates using high dosage Ge+ implantation into commercially available Silicon-on-Insulator has been successfully developed. A 1.0E + 17/cm^2 dose of Ge ions with 100 keV was implanted into Si top-layers (of thickness 193 nm) at room temperature and 550 °C. Subsequent annealing to create SiGe crystal structures in the Si top layers was carried out at 800°C to 1200 °C in N_2 or O_2 for 5 minutes in a Rapid Thermal Annealer (RTA). To extend the annealing time for obtaining fully relaxed SiGe alloy, we also used a tube furnace at 1200 °C to 1250 °C in O_2/Ar for 30 minutes to 90 minutes. SGOI substrates were completed by removing surface SiO2 growth using buffered HF and/or Chemical and Mechanical Polishing (CMP). SGOI substrates were then ready for the growth of silicon layers for Strained Si-MOSFETs. The samples were investigated by X-Ray Diffraction (XRD) and Secondary Ion Mass Spectroscopy (SIMS) for analysis of crystal structure, thickness and implantation profile. It was found that using O_2 gas during annealing can prevent Ge out-diffusion and Ge segregation. Raman Spectroscopy (RS) was used to develop a suitable process (involving different annealing times and temperatures) to obtain fully relaxed SiGe layers. Surface roughness was checked by an Atomic Force Microscope (AFM).

B8.15
High-performance infrared photodetector of SixGey PIN

diode with inductively coupled plasma deposited active layer. Yi-Fan Lai, Jia-Min Shieh and Bau-Tong Dai; National Nano Device Laboratories, Hsinchu, Taiwan.

The widespread diffusion of optical communications in the access network (i.e., the network portion devoted to connecting individual users to the backbone) is presently hindered by the high cost of optical transceivers operating in the near infrared. Such systems, in fact, are currently realized by hybrid integration of III-V laser diodes and detectors on the substrate hosting the waveguides, which connect them. The introduction of a silicon-compatible technology for the fabrication of optical network is expected with high potential, owing to a more mature technology and monolithic integration of all components on a single, small, reliable, and easily reproduced optoelectronic integrated circuit. Especially, Ge/Si or SiGe/Si photodetectors have been successfully demonstrated for the wavelengths of interest (1.3 and 1.55 gm), and their characteristics are comparable to those of commercial III-V photodiodes. In this work, inductively Coupled Plasma (ICP) CVD is used to deposit SixGey active layers and buffer layers of the SiGe photodetector. It's well known that ICP has a high fractional ionization capacity. The high dissociation capacity of ICP produces high-density plasma and a high electron temperature, but low ion bombardment, allowing the synthesis of high quality poly-SixGey films at low temperatures, assisted by high plasma power. Furthermore, using the ICP method could control the Ge concentration of the SixGey active layer easily and arbitrarily by changing the ratio of the reaction gas. Those merits of ICP films and high deposition rate associated with ICP method also let ICP SixGey films as excellent buffer layers in the applications of low-noise photodetectors. Grain size and composition of all SixGey films are analyzed by XRD and TEM with EDS and the dislocation density of SiGe/Si interface is analyzed by OM using the etch-pit density (EPD) method presented by Luan (Ref.1). The photodiodes are measured in terms of photo-responsivity and current-voltage characteristics. In conclusion, this study reports the high performance infrared photodetector using high-quality ICPCVD SixGey films with excellent active-layer (or buffer-layer) characteristics of large grains (several tens of nanometers), high deposition rate (higher than 5?/s), low roughness (1 nm), and low dislocation density (7.5E5/cm2,show in FIG.1).

B8.16

Effects of the He implantation energy on the strain relaxation of epitaxial $Si_{0.8}Ge_{0.2}$/Si(100) heterostructures. Marcio J. Morschbacher[1], Douglas L. da Silva[1], Paulo F. P. Fichtner[2,1], Fernando C. Zawislak[1], Bernd Hollaender[3], Martina Luysberg[4], Siegfried Mantl[3], Roger Loo[5] and Matty Caymax[5]; [1]Instituto de Fisica, Universidade Federal do Rio Grande do Sul, Porto Alegre, RS, Brazil; [2]Dep. de Metalurgia / IF-UFRGS, Universidade Federal do Rio Grande do Sul, Porto Alegre, RS, Brazil; [3]Institute of Thin Films and Interfaces, Research Center Juelich, Juelich, Germany; [4]Institute of Solid State Research, Research Center Juelich, Juelich, Germany; [5]IMEC, Leuven, Belgium.

Strain relaxation of 80 nm thick, epitaxial $Si_{0.8}Ge_{0.2}$ layers on Si(100) was investigated systematically after He ion implantation in the energy range of 15 to 30 keV for a fluence of $2x10^{16}$ cm^{-2}. The pseudomorphic SiGe layers were grown by CVD. For this energy range it is demonstrated that significant He loss already takes place during the implantation process. The retained He content measured by elastic recoil detection (ERD) varies from $\cong$80% of the implanted fluence for the 30 keV case and decreases with the energy down to $\cong$20% for the 15 keV case. The loss is discussed in terms of radiation enhanced diffusion and the results are compared with previous ones obtained for pure Si (100). A He-concentration versus implantation-energy diagram is derived for both, SiGe layers and bare Si. Upon 1200s thermal annealings at temperatures from 450 to 850°C, the thermal evolution of the lattice damage as detected by RBS/C measurements is correlated with the formation of He bubbles as observed by TEM. These results were further supported by ERD measurements of the He release. On the basis of these data a road-map for the formation of pressurized plate-like He filled cavities is proposed. On this base, we achieved 75% strain relaxation of the $Si_{0.8}Ge_{0.2}$ layer and we evaluated from detailed plane-view TEM investigations low threading dislocation densities of $\cong 6x10^{5}$ cm^{-2}.

B8.17

A Comparison of Equilibrium and Oxidation Enhanced Si-Ge Interdiffusion Kinetics. Nevran Ozguven, Daniel B Aubertine and Paul C McIntyre; Materials Science and Engineering, Stanford University, Stanford, California.

We will present a study of the effects of Si surface oxidation on Si-Ge interdiffusion in epitaxial heterostructures. Measurements were performed on single crystal SiGe/SiGe superlattices grown by low-pressure chemical vapor deposition onto Si (001) substrates. These superlattices have the structure $[Si_{1-x}Ge_x$ ~7nm/$Si_{1-y}Ge_y$ ~7nm$]_{40}$. By controlling the average composition of the superlattices and the amplitude of their composition modulations, one can probe the misfit stress- and intrinsic composition- dependencies of Si-Ge interdiffusion systematically. The interdiffusion kinetics and simultaneous misfit strain changes during annealing were measured via the same technique- high resolution superlattice x-ray diffraction. A Si cap, which is partially consumed during dry O_2 post-anneals, is grown on these superlattices for the oxidation experiments. Experiments were performed on identical superlattice samples annealed in both inert (N_2) and oxidizing ambients. We have observed an enhancement in the interdiffusion kinetics for the case of oxidation. This suggests that the nonequilibrium point defect concentrations created during Si oxidation can significantly alter the interdiffusion rates of Si and Ge.

B8.18

Improved SIMS Quantification for Strained SiGe Materials. Stephen P. Smith[1], Gary Goodman[1], Alice Wang[1] and Ihab Abdelrehim[2]; [1]Charles Evans & Associates, Sunnyvale, California; [2]Evans Northeast, Peabody, Massachusetts.

SIMS is the primary analytical technique used to measurement dopant and impurity depth distributions in SiGe materials, and has been used extensively for characterizing SiGe HBT materials and devices. SIMS quantification is affected by the matrix composition of the material analyzed, in this case the Si/Ge ratio, and requires reference materials. The SIMS quantification for SiGe HBTs was developed many years ago, but was focused on Ge atomic compositions of a few % to 20%, whereas the Ge content in strained SiGe materials for CMOS may range from 15% to 80%, depending upon the device design. Accurate quantification is particularly important now for TCAD, since the diffusion coefficients of B, P and As in SiGe are affected by the Ge content and by the point defect distributions in ways different from pure Si [1]. This will also be critical for 'copy exactly' processing. There is also interest in doped SiGe for junctions [2] and enhanced lateral strain on the channel [3]. We have completed a systematic study of the SIMS Relative Sensitivity Factors (RSFs) for B, As, P, Sb, O, C, F, N, Al and Ge (matrix level) in SiGe as a function of (a) Ge atomic composition (0 to 1), and (b) SIMS instrumental conditions (magnetic sector, quadrupole, O_2^+, Cs^+, incident ion impact energy and angle, detected species, and with and without O-leak). Because the actual Ge content to be used in these kinds of devices may vary over a wide range, it is very useful to develop models of the relative RSFs versus [Ge] and analytical conditions, so that calibrations done at one [Ge] content can lead to accurate calibration for other [Ge] contents. We have developed these models and compared them with experimental data to demonstrate their validity. These models and examples will be presented. [1] K. Rim et al, VLSI Technology Symposium, p. 98 (2002); J. L. Hoyt et al, IEDM, p. 2.2.1 (2002). [2] P. E. Thompson and J. Bennett, J. Appl. Phys., 92, 6845 (2002). [3] U.S. patent 6,621,131; issued to Intel Corporation September 16, 2003.

B8.19

Characterization of Structural Quality of Silicon-On-Insulator Layer by Spectroscopic Ellipsometry and Raman Spectroscopy. Nhan V. Nguyen, James E Maslar, Jin Yong Kim, Jin-Ping Han, Jin-Won Park, Dean Chandler-Horowitz and Eric M Vogel; National Institute of Standards and Technology, Gaithersburg, Maryland.

The crystalline quality of Silicon-On-Insulator (SOI) fabricated by a wafer bonding technique was examined by spectroscopic ellipsometry and Raman spectroscopy. Both techniques detect slight structural defects in the SOI layer. In this study, we investigated four SOI substrates, one of 4// and three of 8// diameter. One 8// SOI wafer was cut into smaller samples, some of which were then oxidized in an oxygen ambient at 1100°C for 12 min to 24 min to reduce the SOI layer thickness. In general, SE can be used to characterize the structural quality of all the layers in the SOI wafer once the corresponding optical properties are experimentally determined. For the BOX layer, which is a thermal oxide, the index of refraction is known to be slightly higher than that of bulk fused silica. The main interest lies in the accurate evaluation of the dielectric function of the SOI layer. If a pure crystalline Si dielectric function is assumed for the SOI layer, the spectroscopic ellipsometry data fitting yields an unacceptably large discrepancy between the experimental and modeled data. A slightly improved fit was obtained with a model including an interface roughness at the bonding surface between the BOX layer and the SOI layer, but yielded unphysical thickness of both layers, and therefore, was eliminated. The best fits for all the samples result in the dielectric function of the SOI layer that consists of a physical mixture of crystalline silicon and about 4 % to 7 % of amorphous silicon. Therefore, the spectroscopic ellipsometry results clearly indicate a slight lack of long-range order of the silicon atoms existing in the SOI layer. This observation is further supported by Raman spectroscopy measurements. The Raman spectra of all SOI samples exhibit a feature at about 495 cm 1 that is not observed in

the crystalline silicon spectrum. Features similar to the 495 cm 1 feature have been reported in the literature and attributed to dislocations or faults in the silicon lattice. The 495 cm 1 feature observed in this work is tentatively attributed to defects in the silicon lattice, presumably resulting from the hydrogen implantation step of the SOI fabrication process.

B8.20
Room Temperature laser operation of strained InGaAs/GaAs QW structure monolithically grown by MOVCD on LE-PECVD Ge/Si virtual substrate. Yves Chriqui[1], Guillaume Saint-Girons[1], Sophie Bouchoule[1], Giovanni Isella[2], Hans von Kaenel[2] and Isabelle Sagnes[1]; [1]LPN-CNRS-UPR 20, Marcoussis, France; [2]INFM and L-NESS, COMO, Italy.

A large variety III-V GaAs-based laser structures are produced at a commercial scale, and are used in a wide range of optoelectronic applications. Their monolithic integration with silicon-based microelectronic systems could allow to overcome the bottleneck of electrical interconnections, and represents a reliable low cost alternative to wafer bonding techniques. However, the direct growth of GaAs on Silicon still remains a challenge. Indeed, the differences in lattice parameters and thermal expansion coefficients between GaAs and Si, and the presence of antiphase boundaries (APBs) - resulting from the epitaxy of polar on non-polar materials -strongly affect the structural and optical properties of the GaAs layers grown on Silicon. Recently, the use of strained relaxed $Ge/Si_{1-x}Ge_x$ buffer layers grown by ultra-high vacuum-chemical vapor deposition (UHV-CVD) on Silicon substrates was proposed for the monolithic growth of GaAs on Si : due to the germanium seed layer the lattice parameter is matched to the one of GaAs providing for excellent conditions for the subsequent GaAs growth. In this contribution, we report on first room temperature (RT) laser operation at 1.04 μm from strained InGaAs/(Al)GaAs quantum well structures grown by MOVPE and monolithically integrated on Si using 6° offcut Ge/GeSi/Si -Virtual Substrate (VS) realized by Low Energy-Plasma Enhanced Chemical Vapor Deposition (LE-PECVD). Room Temperature operation at 1.04 μm was obtained from broad area devices. Identical control laser diodes grown on bulk germanium substrates showed similar threshold current density, demonstrating the potential of Ge/Si-VS for monolithic integration of long wavelength GaAs-based lasers on Si.

B8.21
Abstract Withdrawn

B8.22
Relaxation of strained SiGe on insulator by direct wafer bonding. Jer-shen Maa, Jong-Jan Lee, Douglas Tweet and Sheng Teng Hsu; Sharp Laboratories of America, Camas, Washington.

Strained SiGe was bonded to silicon dioxide and glass substrates by direct wafer bonding and Smart-cut technique. Strained SiGe with a graded 20%-30% Ge concentration was deposited by RTCVD on (100) Si to a thickness between 300 nm to 350 nm. H2 for wafer splitting was implanted at an energy varied from 40 keV to 150 keV with a dose between 2.5E16 and 4.5E16. SiGe relaxation was found to depend on wafer split temperature, and on post-split annealing temperature. SiGe relaxation of greater than 80% was observed after wafer splitting and annealing. At first it seemed that SiGe relaxation on glass was from the nature of the glass substrate. Gliding of a SiGe film weakly bonded to an oxide surface also seemed possible. In order to determine the relaxation mechanism, samples with different film structure were prepared on oxide and glass substrates. The films were then annealed at various temperature. Some film showed a high degree of relaxation, and some showed minimal relaxation. The results indicated that the generation of dislocation, not the softening of glass or film gliding on a weakly bonded interface, was the major cause of relaxation.

B8.23
Characterization of Strained Silicon on Si1-xGex on Insulator Stack with Advanced Nondestructive Techniques. Lianchao Sun[1], Christophe Defranoux[2] and Jean-Louis Stehle[2]; [1]SOPRA Inc, Westford, Massachusetts; [2]SOPRA SA, Bois Colombes, France.

Strained silicon technology has been proven to be a breakthrough for further enhancing device performance via the enhanced mobility. The processing to obtain strained silicon channel is through depositing silicon on relaxed silicon germanium virtual substrate. An optimized design for such structure starts with a thick graded SiGe layer with increasing Ge concentration and followed by a relaxed SiGe layer. A strained silicon layer with typical thickness of only 10 to 30 nm is finally produced on this relaxed SiGe layer. This complicated stack poses significant challenges to both processing itself and characterization. Spectroscopic ellipsometry has been used to determine Ge concentration and layer thickness for SiGe layer in both strained and relaxed cases. However, it might not be proper to determine strained silicon layer thickness with bulk dielectric constants from library because of the following reasons: (1) common knowledge is that there is difference between bulk and thin films in dielectric properties, (2) for very thin films, there is correlation between thickness and their optical constants. (3) strain in silicon should be dependent on Ge concentration in the underlying SiGe layer. Therefore, to study the dielectric properties of the strained silicon layer, absolute layer thickness measurement with other technique is needed. In this paper, the grazing x-ray reflectometry will be used to obtain layer thickness and then spectroscopic ellipsometry applied to calculate optical constants for strained silicon film to generate optical constants datadabe. Both spectroscopic ellipsometry and grazing x-ray reflectometry are nondestructive, non contact and optical techniques and can be combined into one tool. The related examples will be presented and results will be discussed.

SESSION B9/C9: Joint Session: SiGe Layers
Chair: Wolfgang Windl
Thursday Morning, April 15, 2004
Room 2004 (Moscone West)

8:30 AM *B9.1/C9.1
Current Understanding of Diffusion in Strained Si and SiGe. Nicholas Edward Cowern, Advanced Technology Institute, University of Surrey, Guildford, Surrey, United Kingdom.

The introduction of novel device features such as metal gates and bandgap-engineered channels into upcoming CMOS generations has placed the subject of strained Si and SiGe at the top of the materials agenda for silicon-based technology. A key problem in this field is the diffusion and segregation behaviour of host and impurity atoms in the strained material. Much work has been done in the last decade but the subject remains controversial despite fundamental analyses of the role of strain in diffusion from the points of view of thermodynamics, transition state theory and atomistic calculations, and in spite of very extensive experimental investigations. As yet it seems fair to say that there is still no firmly established understanding of stress/strain effects on diffusion. The talk will review recent progress in understanding, emphasizing the key role played by strain fields that intersect surfaces and interfaces where point defects are generated. A new theoretical framework that takes explicit account of surface strain will be outlined, and its consequences for point defects, diffusion and mass transport in non-uniformly strained structures will be considered and compared with the available experimental evidence. Part of this work was performed within the CEC projects IST/2001-34404 ARTEMIS and IST/2000-30129 FRENDTECH.

9:00 AM B9.2/C9.2
Impact of Buffered Layer Growth Conditions on Grown-In Vacancy Concentrations in MBE SiGe. Kareem M. Shoukri[1], Yaser M. Haddara[1], Andrew P. Knights[2], Paul G. Coleman[3] and Mohammad M. Rahman[4]; [1]Electrical and Computer Engineering, McMaster University, Hamilton, Ontario, Canada; [2]Engineering Physics, McMaster University, Hamilton, Ontario, Canada; [3]Physics, University of Bath, Bath, BA2 7AY, United Kingdom; [4]Electrical and Electronic Engineering, Toyama University, 3190-Gofuka, Toyama 930-8555, Japan.

Silicon-Germanium has become increasingly attractive to semiconductor manufacturers over the last decade for use in high performance devices. In order to produce thin layers of device grade SiGe with low concentrations of point defects and well-controlled doping profiles, advanced growth and deposition techniques such as molecular beam epitaxy (MBE) are used. One of the key issues in modeling dopant diffusion during subsequent processing is the concentration of grown-in point defects. There is evidence that under certain growth conditions (e.g. growth at temperatures below 350°C) a supersaturation of vacancies is grown-in. Using positron annihilation spectroscopy (PAS), we have observed the incorporation of vacancy clusters and vacancy point defects in 200nm SiGe/Si layers grown by MBE over different buffer layers. Variables included the type of buffer layer, the growth temperature and growth rate for the buffer, and the growth temperature and growth rate for the top layer. Different growth conditions resulted in different relaxation amounts in the top layer, but in all samples the dislocation density was below 10^6 cm^{-2}. Preliminary results indicate a correlation between the size and concentration of the vacancy defect clusters and the percentage relaxation in the alloy layer. At low relaxation percentages of <50% the vacancy point defect concentration is below the PAS detectable limit of approximately $1x10^{-15}$ cm^{-3}. As the relaxation is increased to a maximum value of 93%, small vacancy clusters are observed in the SiGe film.

9:15 AM B9.3/C9.3
Arsenic diffusion in Si and $Si_{1-x}Ge_x$ alloys. Suresh Uppal[1],

Janet M. Bonar[2], Arthur F. W. Willoughby[1] and Jing Zhang[3]; [1]Materials Research Group, University of Southampton, Southampton, Hampshire, United Kingdom; [2]Department of Electronics and Computer Science, University of Southampton, Southampton, Hampshire, United Kingdom; [3]Department of Electrical Enginering, Imperial College, London, United Kingdom.

Results of As diffusion in Si and Si-Ge (10 —*pthou*—Ge) are presented. Using molecular beam epitaxy (MBE), *insitu* arsenic delta doped epitaxial Si and compressively strained and relaxed Si-Ge layers were grown on Si substrates. The as-grown and annealed profiles were measured using secondary ion mass spectroscopy after rapid thermal annealing (RTA). Arsenic diffusion is clearly enhanced in Si-Ge as compared to Si and the enhancement factor is recorded to be ≅2 for 10—*pthou*— Ge content. The calculated diffusion coefficient agree well with literature values for both Si and Si-Ge. Using RTA in O_2 atmosphere, interstitial and vacancies have been injected in the sample structures at 1000°C. Diffusion enhancement with vacancy as well as interstitial injections as compared to an inert anneal is recorded in Si and Si-Ge structures. The results suggest that both interstitial and vacancy defects contribute to arsenic diffusion in Si and Si-Ge(10—*pthou*— Ge).

9:30 AM B9.4/C9.4

Modeling dopants diffusion in SiGe and SiGeC alloys. ardechir pakfar[1,2], Alain Poncet[2], Thierry Schwartzmann[1] and Herve Jaouen[1]; [1]TPS & QA - TM, STMicroelectronics, CROLLES, France; [2]LPM, INSA de Lyon, Villeurbanne, F-69621, France.

In this work, a unified physical model of dopants diffusion in SiGe and SiGeC alloys is proposed, based on the hypothesis that the different effects introduced by Germanium and Carbon incorporation in Silicon matrix modify the equilibrium concentrations of interstitials and vacancies from their standard value in pure Silicon. The primordial role of point defects in dopant diffusion is admitted and the evolution of substitutionnal atoms diffusivity is described by their concentration variation. The critical analysis of bibliographic studies allows the description of involved physical phenomena: the chemical effect in covalent alloys, the effect of strain and the Fermi-level effect, act on point defects concentration and thus, on impurity diffusion. This formulation is completed by the equations expressing the B-Ge coupling and the influence of Carbon supersaturation, to form a unified phenomenological model valid to describe the diffusivity evolution of usual dopants in SiGe and SiGeC strained and relaxed alloys. All reliable and previously published experimental data is analyzed for the calibration of the model physical parameters. Finally, the equilibrium diffusion of Boron in shallow epitaxial SiGe and SiGeC layers is measured and successfully confronted to the unified diffusion model. For the first time, experimental studies of Arsenic equilibrium diffusion are performed, showing an important diffusivity enhancement with Ge and C content of SiGeC strained layers, confirming model predictions for the Vacancy-mediated diffusion.

9:45 AM B9.5/C9.5

Athermal Ge−migration during junction formation in s-Si layers grown on SiGe-buffers. Wilfried Vandervorst[1], bartek pawlak[2], richard lindsay[1], romain delhougne[1], matty caymax[1] and bert brijs[1]; [1]mca, imec, leuven, Belgium; [2]philips research leuven, leuven, Belgium.

Solid phase epitaxial regrowth (SPER) has been proven to be highly advantageous for ultra shallow junction formation in advanced technologies. Application of SPER to strained Si/SiGe structures raises the concern that the Ge may outdiffuse during the implantation and/or anneal step and thus reduce the strain in the silicon. In the present studies we expose the 8nm strained silicon wafers to implant conditions that are characteristic for formation of the junctions by solid phase epitaxial regrowth (SPER) and conventional spike activation and measure the resulting Ge-redistribution using SIMS. We have studied the dose and energy dependence of this athermal redistribution process by using As implants (2−15 keV, 5 e14 −3e15 at/cm2) such that the location of the implants species relative to the Ge-edge could be determined by Sims as well. It is shown that the energy of the implant species or more specifically the position of the damage distribution function relative to the Ge-edge (as deduced from RBS-channeling measurements) plays a determining factor with respect to the Ge-migration. For implants whereby the damage distribution overlaps with the Ge-edge a very efficient transport of the Ge is observed, even prior to any anneal cycle. The migration is entirely correlated with the collision cascade and the resulting (forward!) Ge-recoil distribution as demonstrated by Monte Carlo simulations using SRIM. The scaling with dose for a given energy links the observed Ge-profile with a broadening mechanism related to the number of atom displacements induced in the sample. The Ge-redistribution originating from additional anneals after the implant step (or even before the implant) was also studied and is shown to be far less important as compared to the collisional mixing effects. The latter clearly supports the concept an athermal Ge-migration caused by the amorphizing implant. The observed redistribution implies that the use of the SPER process for junction formation in s-Si/SiGe inevitably leads to a strong Ge-redistribution and a corresponding loss off strain in the Si-layer.. A careful engineering of the amorphization process (such as using low dose multiple energy implants) may be required to limit the migration process.

10:00 AM B9.6/C9.6

The Role of Preamorphization and Activation for Ultra Shallow Junction Formation on Strained Si Layers Grown on SiGe Buffer. Bartlomiej J. Pawlak[1], Wilfried Vandervorst[2], Richard Lindsay[2], Indgrid De Wolf[2], Fred Roozeboom[3], Romain Delhougne[2], Alessandro Benedetti[2], Roger Loo[2], Matty Caymax[2] and Karen Maex[2]; [1]Philips Research Leuven, Leuven, Belgium; [2]IMEC, Leuven, Belgium; [3]Philips Research Labs, Eindhoven, Netherlands.

The junctions formed on strained silicon/SiGe buffers need to satisfy one additional requirement, their activation related thermal budget should not relax the strain in the channel. We investigated the role of preamorphization, doping and thermal budget separately for the junction and the channel region. In the present study we exposed the 8 nm strained silicon wafers to the conditions that are characteristic for formation of the junctions by solid phase epitaxial regrowth (SPER) and conventional spike activation. We investigated by Raman spectroscopy the stress relaxation influenced by annealing at temperatures between 550C and 1000C for 1 minute and up to 1070C spike activation. We amorphized the wafers by germanium or arsenic implantation in such a way that the amorphous layer interface is placed within the strain silicon layer or beyond in the SiGe buffer. The secondary ion mass spectroscopy (SIMS) of as-implanted junctions shows significant germanium migration towards the surface. After 1070C spike activation for the deep positioning of the a-Si/c-Si interface we observe additional redistribution of germanium towards the surface. The effect is substantially smaller in the shallow amorphized or non-amorphized samples. Raman spectroscopy analysis revealed that amorphization by germanium or arsenic relaxes the strain silicon. If the wafer is not amorphized the standard thermal budget used for solid phase epitaxial regrowth, 650C for 1 minute does not relax the silicon layer. We observed an improved dopant activation in s-Si/SiGe material of p-type junctions formed both by SPER (Ge + B) annealed at 650C for 1 minute and by spike activation (Ge + F + B) at 1070C. For the boron doped junctions activated by SPER we recognized the same silicon interstitial driven deactivation mechanism as in bulk material. For the n-type junctions doped by phosphorus and arsenic we have concluded improved activation by SPER in s-Si/SiGe material in comparison to bulk Si. Spike activation at 1070C of arsenic doped samples offers worse trade-off between junction depth and sheet resistance than in bulk material. In summary we conclude that the thermal budget used for junction formation still preserves the strain in the non-implanted channel region. For any amorphisation conditions a substantial germanium migration to the surface is observed. The strain in the junctions is relaxed due to implantation defects.

SESSION B10
Chair: Shigeaki Zaima
Thursday Morning, April 15, 2004
Room 2004 (Moscone West)

10:30 AM *B10.1

Atomically Controlled Impurity Doping in Si-Based CVD Epitaxial Growth. Junichi Murota[1], Masao Sakuraba[1] and Bernd Tillack[2]; [1]Laboratory for Electronic Intelligent Systems, Res. Inst. Electr. Comm., Tohoku University, 2-1-1 Katahira, Aoba-ku, Sendai 980-8577, Japan; [2]IHP, Im Technologiepark 25, 15236 Frankfurt (Oder), Germany.

Atomically controlled processing has become indispensable for the fabrication of ultrasmall MOS devices and Si-based heterodevices, because high performance devices require atomic-order abruptness of doping profile and heterointerfaces. In the present work, atomically controlled impurity doping in Si based CVD epitaxial growth has been investigated. By ultraclean low-pressure CVD using SiH_4 and GeH_4 gases, epitaxial growth of $Si/Si_{1-x}Ge_x/Si$ heterostructures with atomically flat surfaces and interfaces on Si(100) is achieved. For in-situ doped $Si_{1-x}Ge_x$ epitaxial growth on the (100) surface in a SiH_4-GeH_4-dopant (PH_3, or B_2H_6 or SiH_3CH_3)-H_2 gas mixture, the deposition rate, the Ge fraction and the dopant concentration are explained quantitatively assuming that the reactant gas adsorption/reaction depends on the surface site materials and that the dopant incorporation in the grown film is determined by Henry's law. Based on these results, we have developed high performance MOSFETs with a $Si_{0.65}Ge_{0.35}$ channel formed at 500°C and

MOSFETs with a 0.12 μm gate length by utilizing in-situ impurity-doped $Si_{1-x}Ge_x$ selective epitaxy on the source/drain regions at 550°C. Next, self-limiting formation of 1-3 atomic layers of group IV or related atoms in the thermal adsorption and reaction of hydride gases (SiH_4, GeH_4, NH_3, PH_3, CH_4 and SiH_3CH_3) on Si(100) and Ge(100) are generalized based on the Langmuir-type model. Si or SiGe epitaxial growth over the N, P and B layer already-formed on Si(100) or SiGe(100) surface is achieved. It is found that higher level of electrical P atoms exist in such film, compared with doping under thermal equilibrium conditions. Furthermore, the capability of atomically controlled processing for doping of advanced devices with critical requirements for dose and location control is demonstrated for the base doping of SiGe:C heterojunction bipolar transistors (HBTs). These results open the way to atomically controlled technology for ultra-large-scale integrations.

11:00 AM B10.2
Effect Of Carbon On Diffusion Of Boron In SiGe Between 940-1050 Degrees Celsius. Mudith S A Karunaratne[1], Janet M Bonar[2], Jing Zhang[3] and Arthur F Willoughby[1]; [1]Materials Research Group, School of Engineering Sciences, University of Southampton, Southampton, Hampshire, United Kingdom; [2]Microelectronics Research Group, School of Electronics and Computer Science, University of Southampton, Southampton, Hampshire, United Kingdom; [3]Department of Physics, Imperial College, London, United Kingdom.

The ability of C to suppress transient enhanced diffusion of B during post implantation heat treatment is instrumental for the fabrication of high performance SiGe HBTs. This retarding effect has also been observed in unimplanted structures as well as in pure Si. Despite the industrial importance of the phenomenon, experimental data across different temperature and concentration ranges are still lacking. One of the aims this work is to generate data that can be utilised in practical process models and thereby facilitate the design and fabrication of SiGe:C HBT devices. In this study, B containing marker layers of either Si or strained SiGe were grown on CZ (100) wafers using gas source MBE. Some of the wafers additionally contained a grown-in carbon peak. The combination of Si, Si with C, SiGe and SiGe with C matrices allowed us to separate the effects of Ge and C on the B diffusivity. To ensure inert annealing conditions a low temperature silicon oxide and nitride layers were deposited on top of Si capping layers in each sample. These samples were then rapid thermally annealed at a number of temperature/time combinations between 940-1050 degrees Celsius in oxygen. Diffusion coefficients of B in each type of matrix were extracted by computer simulation, using SIMS profiles obtained from samples before and after the RTA treatment. At 1000 and 1050 degrees Celsius, the calculated diffusivity of B in Si is compatible with values published by Fair which confirm that the annealing conditions were sufficiently inert. At 1050 degrees Celsius, in strained SiGe with about 11% Ge, diffusion of B is 25% slower than in pure Si. The presence of 0.1% C however has a more dramatic suppression effect in both Si and SiGe. The retardation observed is more than 50% in Si while a reduction of more than an order of magnitude could be observed in SiGe. The effect of C concentration on B diffusion in SiGe with 11%Ge was also studied. We found that B diffusivity decreases systematically with the C content. In anneals performed at 1000 degrees Celsius, complete suppression of B diffusion could be observed in samples containing 2% C in SiGe.

11:15 AM B10.3
Isolating the Concentration and Strain Dependence of Interdiffusion at Si/SiGe Interfaces. Daniel Aubertine, Nevran Ozguven and Paul C McIntyre; Materials Science and Engineering, Stanford University, Stanford, California.

Interdiffusion at Si/SiGe interfaces is an important consideration in determining the practical thermal exposure for strained Si CMOS device structures. Predicting the degree of Ge out-diffusion from a SiGe buffer layer into a Si channel is difficult because the intermixing rate is influenced by Ge concentration, film strain, and temperature. In this study we isolate and quantify each of these influences by measuring the decay of small amplitude Ge concentration modulations superimposed onto a series of epitaxial SiGe films with various mean Ge concentrations and strain states. Tube furnace anneals are performed in an inert atmosphere between 770°C and 870°C. Concentration modulation decay rates and film strains are measured by high-resolution x-ray diffraction about the 004 and 113 Bragg reflections. We show that both the activation enthalpy and the exponential prefactor of the interdiffusion coefficient decrease monotonically with increasing Ge concentration. Relative to concentration effects, the influence of compressive film strain is found to be very small. Model predictions based on these measurements indicate non-Fickian Ge profile shapes will be more pronounced at lower temperatures. Finally, model predictions are used to assess the thermal stability of technologically relevant Si/SiGe interfaces.

11:30 AM B10.4
Strained Channel Transistor Using Strain Field Induced by Source and Drain Stressors. Yee-Chia Yeo[1], Jisong Sun[2] and Eng Hong Ong[2]; [1]Electrical and Computer Engineering, National University of Singapore, Singapore, Singapore; [2]Data Storage Institute, Singapore, Singapore.

Strain-induced mobility enhancement is an attractive way to enhance the current drive of metal-oxide-semiconductor field effect transistors. In this paper, we explore the use of lattice-mismatched regions in the source and drain regions that act as stressors to induce strain in the transistor channel region. The lattice mismatched regions comprise a material with a lattice constant different from that of the silicon channel region, such as silicon-germanium. The strain field in the channel region is investigated using a three-dimensional finite-element method. Profiles of strain components (ϵ_{xx}, ϵ_{yy}, ϵ_{zz}) in the vicinity of the stressors are obtained. The strain component in the source-to-drain direction is generally larger than the strain component in the vertical direction. The variation of the strain components in the channel region with different transistor geometries such as the gate length and the position of the lattice-mismatched region is also explored. Design issues for strained channel transistors with source and drain stressors are discussed.

11:45 AM B10.5
Impact of Ge diffusion and wafer cross hatching on strained Si MOSFET electrical parameters. Luke Steven Driscoll, Sanatan Chatopadhyay, Anthony O'Neill, Sarah Olsen and Kelvin Kwa; School of Electrical, Electronic & Computer Engineering, University of Newcastle upon Tyne, Newcastle upon Tyne, England, United Kingdom.

A contender for future generations of CMOS technology is the strained silicon MOSFET. The mobility enhancement in strained silicon can be exploited to maintain the performance enhancements demanded by Moore's law with reduced critical dimensions. Strained Si is obtained by growth of a thin Si layer over a thick virtual substrate of relaxed SiGe. The mobility of a surface channel MOSFET is dependent on the quality of the silicon-oxide interface. The presence of Ge can lead to a reduction in mobility. Ge may out diffuse from the virtual substrate to the oxide interface causing an increase in trapping density. As the Ge content in the virtual substrate increases wafer cross hatching also increases. In this study we report systematic experimental measurements of key electrical parameters for MOSFETs having a range of Ge compositions in the virtual substrate (0-30 %) and strained Si channel thicknesses (5-10 nm). Strained silicon MOSFETs with 0.3 um gate length and 7 nm oxide were fabricated using a full thermal budget process. Channel thickness was confirmed using capacitance measurements. Interface state density was measured using quasi-static C-V and C-f methods. Mobility was extracted using a combination of split C-V, AC conductance and I-V methods. Surface roughness was measured by atomic force microscopy. The study of a matrix of devices having variable Ge composition and strained Si channel thickness is crucial in deconvolving the contributions of Ge diffusion and wafer cross-hatching roughness on electrical parameters. Increasing virtual substrate Ge composition increases the Ge concentration at the Si/SiO_2 interface and cross-hatching amplitude whereas reducing strained Si channel thickness only increases Ge concentration at the Si/SiO_2 interface and does not increase cross-hatch amplitude. Interface state density, D_{it}, gate leakage current and effective carrier mobility are presented for this two-dimensional space of virtual substrate Ge concentration and strained Si channel thickness. The relative importance of Ge diffusion and cross-hatching roughness can be seen in this data. The results help to optimize virtual substrate Ge composition for current and future technology generations of strained Si CMOS, which use lower thermal budgets and require such in-depth understanding of the performance-limiting mechanisms.