SYMPOSIUM C

Silicon Front-End Junction Formation–Physics and Technology

April 13 - 15, 2004

Chairs

Peter Pichler
Fraunhofer-IISB
Schottkystrasse 10
Erlangen, Germany
49-9131-761-227

Alain Claverie
BP 4347
CEMES/CNRS
29 rue J. Mavig
Toulouse-Cedex, 31055 France
33-562-257900

Richard Lindsay
IMEC
Kapeldreef 75
Leuven, 3001 Belgium
32-16-28-8208

Marius Orlowski
DDL Laboratories
Motorola Inc.
3501 Ed Bluestein Blvd.
Austin, TX 78762
512-933-5020

Wolfgang Windl
Dept. of Materials Science & Engineering
Ohio State University
491 Watts Hall
2041 College Rd.
Columbus, OH 43210-1178
614-247-6900

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* Invited paper

SESSION C1: Device Junction Engineering
Chair: Marius Orlowski
Tuesday Morning, April 13, 2004
Room 2002 (Moscone West)

8:30 AM *C1.1
Materials Challenges for CMOS Junctions. William J. Taylor, Motorola APRDL, Austin, Texas.

For the engineers and scientists involved in the development of CMOS source/drain technology, the challenges in the next several generations are perhaps the greatest yet faced. While the past 10 or more years have seen primarily variations to the conventional implant-and-anneal-in-Si, the next 10 will likely involve changes to both the material systems and their manner of introduction. Complicating this is the expectation that the channel and the gate stack material systems will simultaneously be undergoing significant change, to address the needs for enhanced mobility and reduced gate leakage. A further complication is the likelihood that the industry will move away from conventional planar bulk CMOS, to ultrathin SOI, double-gated structures, or 3-D devices. Against the backdrop of the ITRS predictions, we will compare methods for dopant introduction and activation, methods for making contact to these regions, and methods for measurement of material and device properties. New anneal tools provide the promise of activation without diffusion, placing the burden of Xj and abruptness upon implanters; we will investigate the feasibility of these tools meeting this challenge for a manufacturing throughput. Concurrent changes in the gate stack, with a likely need to avoid interdiffusion or recrystallization, can be expected to put an upper limit on temperature. We will therefore address the feasibility of low temperature solid phase epitaxial regrowth as a method of dopant activation. Regarding contacts to doped regions - although NiSi facilitates current CMOS integration concerns, its temperature limits can be restrictive as one looks to 3-D integrations later in the decade. Also on the horizon, movement to separate metals for low-resistance contacts to the N+/P+ regions becomes worthy of study; even the manner of measuring this resistance is a topic of interest. A thread throughout all of this development is the need for simulation to provide tactical and strategic guidance during development on expensive 300mm wafers. While 20 years have been devoted to implantation and diffusion in Si, thus facilitating variable selection for experiments in the line, a much more rapid learning curve is necessary if simulation is to provide similar support for strained-Si and SiGe device development. For longer term research, such as for contact engineering, first-principles estimates of work function can help determine which classes of materials should be studied. This paper will provide the framework for understanding the difficulties faced by CMOS technologists, and highlight in detail a number of these areas, which are in effect challenges to the experts in materials. Materials research can and should play a significant role in defining the appropriate paths through the maze of possibilities - either by answering questions and closing off dead-ends, or by discovery of new techniques or materials which break through existing barriers.

9:00 AM *C1.2
Ultra-shallow junctions for novel device architectures beyond the 65nm node. Aditya Agarwal, Advanced Technology Group, Axcelis Technologies, Beverly, Massachusetts.

Si chip manufacturing is expected to undergo a paradigm change around the 65nm node. This is due to the rapid introduction of new materials and device structures required for further scaling of performance, such as strained Si, ultra-thin-body and multiple (metal-)gate devices. These novel architectures raise fundamentally new questions for shallow junction formation, ranging from whether an amorphizing source drain implant is acceptable, as in the case of strained silicon, to whether an ultra-shallow junction technology is even necessary, as in the case of ultra thin body devices. This paper will review new experimental and simulation data on these and related issues.

9:30 AM C1.3
Device Characteristics of Ultra-shallow Junctions Formed by fRTP Annealing. Alessandra Satta[1], Richard Lindsay[1], Kirklen Henson[1], Steve McCoy[2], Jeff Gelpey[2], Kiefer Elliott[2] and Karen Maex[1]; [1]IMEC, Heverlee, Belgium; [2]Vortek Industries Ltd., Vancouver, British Columbia, Canada.

The creation of ultra-shallow junction for devices at sub-100 nm node is driving significant efforts in developing thermal processing able to give rise to high dopant activation in combination with limited diffusion. Flash-assist Rapid Thermal Annealing™ (fRTP™)* is a promising new annealing technique, which involves the heating of the bulk of the wafer to an intermediate temperature using rather conventional RTP, followed by a short and intense pulse of light localized on the implanted wafer surface. The short pulse of intense light (order of 1-10 ms) is responsible for very high dopant activation level and diffusionless profiles. fRTP™ offers the clear advantages over the conventional spike anneal of forming junctions with shallower depth and lower resistivity, simultaneously avoiding dramatic modifications to conventional process flow of a CMOS device. In this work, we have systematically investigated the junction formation of different implants under fRTP™ anneals in terms of profile and devices. In particular, in optimizing dopant profile, we have analyzed dopant diffusion and activation of fRTP™ junctions as a function of pre-amorphization, co-implantation and fRTP™ parameters. For devices, we have given particular attention to the leakage behavior of the fRTP™ diodes and residual defect presence due to the limited thermal budget. In addition, effect of such optimized fRTP™ extensions in aggressive transistor devices will be shown in order to address integrability issues, such as pattern-induced non-uniformities, dopant deactivation and junction leakage. We will show that co-implanted Ge and F species provide more box-like profile with improved activation. Although leakage currents are higher for fRTP™-annealed junctions than for spike-annealed junctions, pre-amorphization conditions provide a critical tool to control and reduce the leakage current of co-implanted fRTP™ junctions to acceptable levels. We will show how the correct implant and anneal are requested for minimizing pattern effect and improving transistor performance. *Flash-assist RTP and fRTP are Vortek trademarks.

9:45 AM C1.4
SPE integration: Effect of the density and the position of defects on electrical characteristic of 65nm CMOS.
Rebha El Farhane[1], Cyrille Laviron[3], Pierre Morin[2], Christine Rossato[2], Veronique Carron[3], Yves Morand[2], Franck Arnaud[2], Arnaud Pouydebasque[1], Francois Wacquant[2], Damien Lenoble[2] and Aomar Halimaoui[2]; [1]Crolles 2, Philips semiconductors, Crolles, France; [2]Crolles 2, ST microelectronics, Crolles, France; [3]LETI, CEA, Grenoble.

Solid Phase Epitaxy (SPE) is a promising way to perform ultra shallow and highly activated junctions. The principle of the method is to activate the dopants during the crystallization of amorphized silicon. The main advantages are the high dopant activation, the control of the junction depth and a low thermal budget that is compatible with high-k and metal gate requirements. The drawbacks are the presence of End Of Range (EOR) defects along the former a-Si (amorphous-silicon) c-Si (crystalline silicon) interface. The presence of these defects in the charge space may induce junction leakages and as well as Transient Enhanced Diffusion (TED). It is thus very important to control the density and the position of these defects. We integrated SPER into a flow chart compatible with CMOS065 platform. Both extension and deep Source/Drain are fabricated using SPE process. The splits include various Preamorphisation conditions (Ge PAI at different energies and dopant self amophization) and doping species in order to determine the effects of defects density and on the electrical characteristics of the devices. For device fabrication, we used our standard 65nmCMOS processes flow. However, we did not perform pockets implants in order to study properly the characteristics of junctions. The electrical characterization has shown that devices with high performances can be achieved by using SPE process. Indeed, a very good Ion/Ioff trade off is achieved for PMOS (Ion =200microA/micrometer for I off = 1e-8A/micrometer) at 0.9Volts. For deep preamorphization, we observed an increase of the threshold voltage for the smallest gate length. In addition, these smallest devices exhibit pocket-like behavior, although no pocket implant was performed. We attributed these effects to dopant diffusion from the channel that are trapped at the crystal defects (generated by the deep PAI). Regarding the junction leakage, the best results are achieved when shallow preamorphization is performed at extensions level and when dopant self-amorphization is used for deep Source/Drain. We will show that this result is consistent with defect position. In addition to the electrical characterization results, we will present TEM and SIMS data that will be largely discussed.

SESSION C2: Silicides and Germanides
Chair: Richard Lindsay
Tuesday Morning, April 13, 2004
Room 2002 (Moscone West)

10:30 AM *C2.1
Applications of Silicides to 45 nm CMOS and Beyond.
Jorge A. Kittl[2], Anne Lauwers[1], Oxana Chamirian[3,1], Malgorzata A. Pawlak[3,1], Mark Van Dal[4], Amal Akheyar[5], Muriel De Potter[1], Anil Kottantharayil[1], Richard Lindsay[1] and Karen Maex[3,1]; [1]IMEC, Leuven, Belgium; [2]Affiliate researcher at IMEC from Texas Instruments, Leuven, Belgium; [3]Katholieke Universiteit Leuven,

Leuven, Belgium; [4]Philips Research Leuven, Leuven, Belgium; [5]Affiliate researcher at IMEC from Infineon, Leuven, Belgium.

For the 45 nm node and beyond, modifications or departures from conventional scaling schemes may be necessary, which will impact the integration constraints for silicides, their characteristics or even the way silicides are used in CMOS circuits. Alternative gate stacks and substrates as well as novel device architectures are being considered. Metal gates may be introduced to avoid poly depletion. Fully silicided gates are one of the main candidates to replace conventional partially silicided poly gates. Silicides will continue to be used in S/D areas to provide low sheet resistance and low contact resistivity, but different substrates or device approaches (such as strained Si channel devices, use of Si-Ge, FD-SOI, FinFET, etc.) may lead to different constraints and requirements. Even for conventional scaling schemes, the reduction of lateral and vertical dimensions will continue to pose challenges to self-aligned silicide processes. This paper presents an overview of silicide development activities at IMEC for the 45 nm node and beyond, with emphasis on Ni based alloy silicides. Applications to both conventional and alternative scaling schemes will be addressed.

11:00 AM C2.2
Ni-silicided Deep Source / Drain Junctions formed by Solid Phase Epitaxial Regrowth. Anne Lauwers[1], Richard Lindsay[1], Kirklen Henson[1], Simone Severi[1], Amal Akheyar[3], Bartek Pawlak[2], Muriel de Potter[1] and Karen Maex[1,4]; [1]IMEC, Leuven, Belgium; [2]Philips Research Leuven, Leuven, Belgium; [3]affiliate researcher at IMEC from Infineon, Leuven, Belgium; [4]Katholieke Universiteit Leuven, Leuven, Belgium.

The introduction of high-K dielectrics, metal gates and advanced extension junctions in a conventional CMOS process imposes limitations on the thermal budget that can be allowed to activate the deep source/drain junctions. In the present work deep source/drain junctions were formed by solid phase epitaxial regrowth (SPER) of a doped amorphous region, obtained by As implantation or by Ge amorphisation implantation followed by B implantation. Regrowth of the amorphous region at temperatures below 700 degrees C results in a high activation level of the dopants. Due to insufficient activation of the dopants beyond the amorphous region, a very abrupt profile can be obtained with the junction depth being determined by the amorphous depth. Junction leakage, gate and active resistance, and silicide to diffusion contact resistance were studied for SPER source/drain junctions with junction depths ranging between 40 and 100 nm. Ni-silicide was used to contact the source/drain junctions. A comparison was made between SPER source/drain junctions and conventional spike annealed source/drain junctions with similar junction depth. By careful optimization of the implant and anneal conditions, lower junction leakage and lower contact resistance is obtained for the As SPER junction in comparison to a spike annealed junction of similar depth. For B we observed that the implant energy has to be optimised to allow a sufficient transfer length for acceptable contact resistance and leakage. For both As and B, the high surface doping intrinsic to SPER is shown not to degrade the sheet resistance of the NiSi.

11:15 AM C2.3
Nickel Germanosilicide Contacts to Recessed and Epitaxially Regrown SiGe(B) Source/Drain Junctions. Christian Isheden, Per-Erik Hellstrom, Henry H. Radamson, Shi-Li Zhang and Mikael Ostling; Department of Microelectronics and Information Technology, KTH (Royal Institute of Technology), Kista, Sweden.

pMOS transistors with recessed epitaxial SiGe(B) source/drain junctions formed by selective Si etching followed by selective epitaxial growth of *insitu* heavily B-doped $Si_{1-x}Ge_x$ are presented. The concept has several benefits compared to conventional junctions, such as dopant activation above the solid solubility in Si, arbitrary junction depth and perfectly abrupt junctions. Another merit is that raised source/drain structures can be implemented. The contacts to the source/drain regions are formed using Ni mono-germanosilicide because of its low formation temperature and relatively low Si consumption. A Ni film of 200 $\AA$ thickness is deposited by electron-beam evaporation and the Ni mono-germanosilicide is formed by rapid thermal processing (RTP) at a formation temperature below 600 °C in N_2. The sheet resistance is below 5 Ω/square and the specific contact resistivity for the $NiSi_{0.8}Ge_{0.2}/Si_{0.8}Ge_{0.2}$ interface is 1×10^{-7} Ωcm^2. Electrical device characteristics for the transistors will be presented.

11:30 AM C2.4
Formation and Morphology Evolution of Nickel Germanides on Ge (100) under Rapid Thermal Annealing. Siao Li Liew[1], Ka Yau Lee[1], Dong Zhi Chi[1], Soo Jin Chua[1], Hai Ping Sun[2] and Xiaoqing Pan[2]; [1]Institute of Materials Research & Engineering, Singapore, Singapore; [2]Department of Materials Science, University of Michigan, Ann Arbor, Michigan.

Nickel germanides were formed by rapid thermal annealing (RTA) 15 nm Ni film sputtered on Ge (100) at temperatures ranging from room temperature to 700 °C. Phases were identified by XRD and TEM to understand the formation sequence of nickel germanides. Ni-rich phase was first found after RTA at 250 °C whereas in the temperature range from 300 to 600 °C, stable NiGe film was formed. At higher temperature, $NiGe_2$ was detected. XRD results also identified textured NiGe film with the underlying substrate: NiGe(111)——Ge(100) from 300 to 600 °C. SEM results showed continuous germanide film up to 500 °C, after which isolated particles of germanide with exposed underlying substrate were evident. Deepening grooves and prominent grain growth were noticeable as early as 400 °C in our case, indicating the inception of agglomeration process. Sheet resistance measurement by four-point probe was also carried out. Sheet resistance as low as 10 Ω/sq. was attained after RTA from 300 to 500 °C, after which the resistance was increased tremendously. The change of sheet resistance with temperature correlated well with the surface morphology of the samples. At early annealing temperatures (below 500 °C), the resistance was governed by the resistivities of the phases present in the film. However, at higher temperatures, the electrical property was no longer controlled by the phases present but by the continuity of the film. In other words, agglomeration of the germanide film resulted in the increased sheet resistance at 600 °C and above.

11:45 AM C2.5
Erbium-silicided source/drain junction formation by rapid thermal annealing technique for decananometer-scale Schottky barrier MOSFETs. Moongyu Jang[1], Yarkyeon Kim[1], Jaeheon Shin[1], Sunglyul Maeng[1], Kyoungwan Park[2] and Seongjae Lee[1]; [1]Nano-electronic device team, Semiconductor & Basic Research Laboratory, Electronics and Telecommunication Research Institute, Gajeong-dong, Yuseong-gu, Daejon, South Korea; [2]Nano Science and Technology, University of Seoul, Seoul, South Korea.
In Schottky barrier metal-oxide-semiconductor field-effect transistors (SB-MOSFETs), source and drain regions are composed of silicide instead of impurity doped silicon. The structure is quite simple and the ultra-shallow junction can be formed easily and accurately with very low parasitic source and drain resistance, since the silicided junction depth is controlled by the deposited metal thickness and annealing temperature. The silicided junction formation temperature is very low in SB-MOSFETs, compared with the impurity doped junction activation temperature in conventional MOSFETs, giving the opportunity to use metal as gate electrode and high dielectric materials as gate insulator. Moreover, the complicated channel doping steps can be eliminated because Schottky barrier exists between junction and channel. Thus, SB-MOSFETs have been proposed as an alternative to the conventional MOSFETs for decananometer-scale application. In this work, erbium silicide is chosen as source/drain metal of n-type SB-MOSFETs, because of its low Schottky barrier height (0.28 eV) for electrons. Erbium silicide was formed by using rapid thermal annealing (RTA) technique. Annealing temperature and time was 500 °C and 5 min, respectively. During the annealing, the pressure within RTA chamber was controlled below 1.0×10^{-6} torr to prevent the oxidation of erbium. The formation of $ErSi_{1.7}$ phase was confirmed by x-ray diffraction (XRD) and Auger electron spectroscopy (AES) analysis. From the results of AES analysis, oxygen content within the erbium silicide layer increased as the annealing temperature increased over than 500 °C. This indicates the oxidation of erbium during the high temperature annealing process. The sheet resistance of $ErSi_{1.7}$ was less than 30 Ω/ even if the line width was less than 100 nm. Thus, erbium is applicable in decananometer-scale SB-MOSFETs. The manufactured 50 nm gate length n-type SB-MOSFET showed large on/off current ratio with low leakage current less than 10^{-4} $\mu A/\mu m$ and the saturation current was 120 $\mu A/\mu m$. The experimental current-voltage characteristics of 50 nm gate length n-type SB-MOSFET were fitted using newly developed theoretical model. From the curve fitting, the extracted Schottky barrier height is 0.28 eV, which is typical value of $ErSi_{1.7}$ formed on n-type silicon. The characteristics of manufactured device show the possible applicability of $ErSi_{1.7}$ as source/drain junction in decananometer-scale n-type SB-MOSFETs.

SESSION C3: Diffusion Phenomena and Diffusion Modeling
Chairs: Masami Hane and Peter Pichler
Tuesday Afternoon, April 13, 2004
Room 2002 (Moscone West)

1:30 PM *C3.1
Process Modeling for Advanced Devices. Mark E. Law[1,2] and Kevin S. Jones[2,1]; [1]Electrical and Computer, University of Florida, Gainesville, Florida; [2]Materials Science, University of Florida, Gainesville, Florida.

Rapid changes are forecast for device structures. We expect that

changes in the gate dielectric will continue, the gate material may change, and strain is being engineered in with material combinations to increase mobility. How can process simulators stay abreast? What can be done to calibrate to new materials? We will discuss some of the approaches we are taking to attack these issues. I will discuss approaches to better integrate strain in process simulation and strategies to calibrate parameters. We have begun to investigate SiGe materials and how dopants behave, and will discuss the literature data and what needs to be done to port models to new materials. We will also discuss the role of the surface and possible strategies to calibrate to new gate and capping materials.

2:00 PM C3.2
Athermal, Photonic Effects on Boron Diffusion and Activation During Microwave Thermal Processing.
Christopher John Bonifas[1], Keith Thompson[1], John Booske[1] and Reid Cooper[2]; [1]Electrical & Computer Engineering, University of Wisconsin, Madison, Wisconsin; [2]Geological Sciences, Brown University, Providence, Rhode Island.

Recent reports indicate that optically driven phenomena affect the diffusion and electrical activation of B during high temperature rapid thermal processing (RTP). Typical defect reactions require $0.5 - 4$ eV of energy to proceed. However, thermal energy follows a Boltzmann distribution whose peak is on the order of $0.1 - 0.12$ eV at typical spike anneal temperatures ($900 - 1100°$C). As a result, most defect reactions rely on multiple near-simultaneous phonon collisions or interaction with phonons from the very high-energy tail of the thermal energy distribution. Optical photons, on the other hand, possess a large amount of energy, $1 - 4$ eV, which can only be transferred to the lattice in a discrete manner. The transfer of a large amount of energy from individual high-energy photons may either enhance the already dominant kinetic reactions (causing them to proceed at faster rate), allow new chemical reactions to dominate the reaction kinetics, or both. Microwave RTP is ideal for studying the effects of optical illumination. Commercial RTP systems are primarily lamp-based, and the wafer is flooded with optical photons during the thermal treatment. While this improves the possibility of optical effects, it makes these phenomena difficult to isolate and study. Microwave RTP, on the other hand, rapidly heats the wafer at $\geq 150°$C/sec to temperatures in excess of $1000°$C without the presence of optical illumination. This paper details work demonstrating the effect of athermal mechanisms involving optical and microwave illumination on the flux of dopants in ultra-shallow doped Si layers. Optical illumination has a significant, *yettransient*, effect on the formation of ultra-shallow junctions in B doped Si. Rapid thermal annealing was performed in a "dark" microwave furnace in an ambient with an oxygen concentration controlled at 100 ppm. Optically illuminated samples illustrated a greater amount of B diffusion and a lower sheet resistance, Rs, with respect to non-illuminated samples for the B-only implanted Si. The reverse was true for BF_2 implanted samples. Illuminated BF_2 samples exhibited less net B diffusion *and* lower Rs when compared to non-illuminated samples. These differences tended to lessen as diffusion continued, and little difference in net B diffusion was seen after 10 second, $1000°$C anneals. When the spike anneal was performed in an oxidizing ambient, the effect of illumination on B diffusion in the B-only implanted Si was minimal, while illumination enhanced B diffusion in BF_2 implanted samples. Finally, the effect of illumination fails to enhance B activation during low temperature ($550°$C), 30 minute solid phase epitaxy.

2:15 PM C3.3
Simultaneous Phosphorus and Si Self-Diffusion in Extrinsic, Isotopically Controlled Silicon Heterostructures.
Hughes H. Silvestri[1,2], Ian D. Sharp[1,2], Hartmut A. Bracht[3], John L. Hansen[4], Arne Nylandsted-Larsen[4] and Eugene E. Haller[1,2]; [1]Department of Materials Science and Engineering, University of California, Berkeley, Berkeley, California; [2]Materials Sciences Division, Lawrence Berkeley National Laboratory, Berkeley, California; [3]Institut fuer Materialphysik, Universitaet Muenster, Muenster, Germany; [4]Institute of Physics and Astronomy, University of Aarhus, Aarhus, Denmark.

We present experimental results of impurity and self-diffusion in an isotopically controlled silicon heterostructure extrinsically doped with phosphorus. As a consequence of extrinsic doping, the concentration of singly negatively charged native defects is enhanced and the role of these native defect charge states in the simultaneous phosphorus and Si self-diffusion can be determined. Multilayers of isotopically controlled ^{28}Si and natural silicon enable simultaneous analysis of ^{30}Si self-diffusion into the ^{28}Si enriched layers and phosphorus diffusion throughout the multilayer structure. An amorphous 260 nm thick Si cap layer was deposited on top of the Si isotope heterostructure. The phosphorus ions were implanted to a depth such that all the radiation damage resided inside this amorphous cap layer, preventing the generation of excess native defects and enabling the determination of the Si self-diffusion coefficient and the phosphorus diffusivity under equilibrium conditions. These samples were annealed at temperatures between 850 and 1100 °C to study the diffusion. Detailed analysis of the diffusion process was performed on the basis of a foreign atom and native defect controlled mode of P diffusion. The consistency of our results with previous experiments on B and As diffusion is discussed as well as the mechanisms mediating P diffusion in Si. This work was supported by the U.S. Department of Energy under Contract No. DE-AC03-76SF00098.

2:30 PM C3.4
Room Temperature Migration of Substitutional Boron in Silicon by Kick-Out Mechanism. Enrico Napolitani[1], Davide De Salvador[1], Alberto Carnera[1], Salvo Mirabella[2] and Francesco Priolo[2]; [1]INFM and Dipartimento di Fisica, Padova, Italy; [2]MATIS - INFM and Dipartimento di Fisica e Astronomia, Catania, Italy.

Despite the extensive scientific efforts over the last decades, the present knowledge on the point defects and dopant diffusion and interaction in Si between themselves and with substrate impurities still have many important open points, from both an experimental and theoretical point of view. In particular, very few experiments have been reported so far on the behaviour of the above phenomena at the room temperature (RT) regime. Moreover, whether there are some evidences of the RT migration of Si self interstitials (I) and their interaction with impurities, there is, to our knowledge, only one paper in literature [1] in which boron is shown to migrate at RT for long distances, when put in the substrate already in interstitial position by B ion implantation. In this paper we provide an experimental evidence of the long-range migration of substitutional boron in silicon at RT through its interaction with migrating I's, i.e. via the kick-out mechanism. Several silicon samples grown by Molecular Beam Epitaxy with substitutional B deltas were depth profiled by Secondary Ion Mass Spectrometry (SIMS) using O_2^+ ions with different beam energies and currents. Some of samples were analysed both before and after amorphization, and the measurements were done at different temperatures, heating or cooling the sample with a liquid nitrogen-thermo resistance temperature controlled stage. We observed that an anomalous redistribution of boron delta occurs during the analysis of c-Si at RT, consisting in long tails on both the trailing and leading edges of the B deltas at concentrations below $1x10^{18}$/cm^3. This redistribution has not been evidenced and discussed before, but it appears to be present in most of the B delta profiles shown in literature so far. We found that the above redistribution reduces significantly after amorphization or by cooling the sample, up to complete suppression, and it has been interpreted as the result of the interaction of substitutional boron with the I's injected in the samples by the sputtering beam. The phenomenon has been simulated and the temperature dependence has been explained by considering at RT the following mechanisms: the I's are produced by the sputtering beam, migrate for long distances, interact with boron by producing mobile B species via the kick-out mechanism, and eventually the mobile B migrate for long distances resulting in the observed tails. As a result of the simulations, we provided the first experimental estimation of the B diffusivity at RT. Our data have a twofold implication. On one hand, they give significant insights on the migration and interaction of boron and point defects at RT and below. On the other hand this phenomenon, if not properly considered, induces an experimental artifact in the determination of B concentration profile by SIMS and therefore many of the observations obtained in the past might be revised. [1] E. J. H. Collart et al., Nucl. Instrum. Methods Phys. Res. B 139, 98 (1998).

2:45 PM C3.5
Boron Diffusion and Silicon Self-Interstitial Recycling between SiGeC layers. Malcolm Carroll[1] and James Sturm[2]; [1]Sandia National Laboratories, Albuquerque, New Mexico; [2]Electrical Engineering, Princeton University, Princeton, New Jersey.

Substitutional carbon in silicon or SiGe is known to react with silicon self-interstitials, which depletes the self-interstitial concentration. Layers with enough substitutional carbon to react with 100% of the self-interstitials that migrate to it have furthermore, been used to isolate a region below a SiGeC layer from silicon self-interstitials produced above it. Silicon self-interstitials in a silicon spacer layer sandwiched between two SiGeC layers may then be temporarily isolated from direct migration of silicon self-interstitials from either the surrounding bulk or surface regions and therefore offers an opportunity to examine the competition between the rate of reaction of self-interstitials with the surrounding substitutional carbon and the rate of generation of the self interstitials within the spacer. In this paper we use boron marker layers above, below and in between two SiGeC layers to examine the non-local effect of substitutional carbon on the self-interstitial concentrations in and around a silicon spacer layer between two SiGeC layers. Single crystal, 25 nm thick boron marker layers located at 150, 450, 600, and 900 nm below the surface were grown by rapid thermal chemical vapor deposition at temperatures of 550-750°C on Czchokralski silicon substrates with or

without two 25 nm $Si_{0.775}Ge_{0.22}C_{0.005}$ layers at depths of 300 and 750 nm. The samples were subsequently annealed in either nitrogen for 30-240 minutes or oxygen for 30-120 minutes at 850°C. Carbon, germanium and boron concentrations before and after annealing are measured by secondary ion mass spectrometry and boron diffusivities were subsequently extracted by fitting the resulting boron profiles using a standard process simulator. Boron diffusivities between the SiGeC layer after either nitrogen or oxygen anneals are approximately the same, indicating that silicon self-interstitials in the surface region do not pass through the intervening SiGeC layer. The boron diffusivity in the spacer is, furthermore, found to be either similar or greater than that observed in the sample without the SiGeC layers. The boron diffusivities between the SiGeC layers, therefore, show no depletion of the self-interstitial concentration in the silicon spacer despite annealing conditions believed to produce self-interstitial diffusion lengths far greater than the spacer width, which would allow them to reach and react with surrounding substitutional carbon. Simulations of the self-interstitial and carbon diffusion are used to fit the carbon profiles and indicate that the silicon self interstitial concentration in the spacer layer is sustained in part due to a silicon self-interstitial recycling process in which self-interstitials consumed in the SiGeC layer are effectively transported back to the spacer layer as mobile interstitial carbon and are subsequently released in the spacer by the reverse "kick-out" reaction.

3:30 PM *C3.6
Current Understanding and Modeling of B Diffusion and Activation Anomalies in Preamorphized Ultra-Shallow Junctions. Benjamin Colombeau[1], Andy J Smith[1], Nicholas E.B. Cowern[1], Fuccio Cristiano[2], Alain Claverie[2], Ray Duffy[3], Bartek J Pawlak[3], Christophe J Ortiz[4], Peter Pichler[4], Evelyne Lampin[5] and Christoph Zechner[6]; [1]Advanced Technology Institute, University of Surrey, Guildford, United Kingdom; [2]Ion implantation group, CEMES/LAAS-CNRS, Toulouse, France; [3]Philips Research Leuven, Leuven, Belgium; [4]Fraunhofer IISB, Erlangen, Germany; [5]IEMN/ISEN, UMR CNRS, Villeneuve d Ascq, France; [6]ISE Integrated System Engineering AG, Zurich, Switzerland.

The formation of ultra-shallow junctions (USJs) for future integrated circuit technologies requires preamorphization and high dose boron doping to achieve high activation levels and abrupt profiles. To achieve the challenging targets set out in the semiconductor roadmap, it is crucial to reach a much better understanding of the basic physical processes taking place during USJ processing. In this paper we review current understanding of dopant-defect interactions during thermal processing of device structures - interactions which are at the heart of the dopant diffusion and activation anomalies seen in USJs. First, we recall the formation and thermal evolution of End of Range (EOR) defects upon annealing of preamorphized implants (PAI). It is shown that various types of extended defect can be formed: clusters, {113} defects and dislocation loops. During annealing, these defects exchange Si interstitial atoms and evolve following an Ostwald ripening mechanism. We review progress in developing models based on these concepts, which can accurately predict EOR defect evolution and interstitial transport between the defect layer and the surface. Based on this physically based defect modelling approach, combined with fully coupled multi-stream modelling of dopant diffusion, one can perform highly predictive simulations of boron diffusion and de/re-activation in Ge-PAI boron USJs. Agreement between simulations and experimental data is found over a very wide range of experimental conditions, clearly indicating that the driving mechanism that degrades boron junction depth and activation is the dissolution of the interstitial defect band. Furthermore, the simulations enable prediction of dopant behaviour during novel thermal processing methods, such as millisecond annealing. The prospects for bringing these accurate simulation models into commercial simulation tools used by the semiconductor industry will be briefly discussed. Finally we outline some promising methods, such as co-implants and/or vacancy engineering, for further down-scaling of source-drain resistance and junction depth. This work is part of the FRENDTECH and ARTEMIS projects, funded by the EC as IST/2000-30129 and IST/ 2001-34404.

4:00 PM C3.7
On the //Life// of {113} Defects. Nikolay Cherkashin[1], P. Calvo[1], F. Cristiano[1], B. de Mauduit[1], B. Colombeau[2], Y. Lamrani[1] and A. Claverie[1]; [1]nMat group, CEMES-LAAS/CNRS, Toulouse, France; [2]Advanced Technology Institute, University of Surrey, Guildford, United Kingdom.

The simulation of diffusion anomalies in Si requires that the physical mechanisms driving the thermal evolution of interstitial defects in Si are understood. However, there is still a controversy on whether or not the so-called {113} defects undergo Ostwald ripening during annealing, i.e. whether they interchange Si atoms between them or simply release the Si atoms they are composed of. For this reason, we have decided to redo the classical Eaglesham/s experiment in which Si is implanted at 40 keV with a dose of $6x10^{13}_{cm-2}$ then annealed under N2 at 650°C, 700°C, 740°C and 815°C. Weak beam dark field imaging under appropriate conditions has been used to follow the evolution of the size-distributions and densities of the population of defects during annealing. To perform such a rigorous statistical analysis more than 300 defects were analyzed at each step and their variance identified. While the overall characteristics of the defect evolution, i.e. variation of the onset of dissolution and dissolution time with annealing temperature, were found to be roughly the same as those found by Eaglesham, our results show details which were not so clear in the original experiment. Whatever the temperature, during a first period of time, the {113} defects grow in size while their density decreases. In the meantime, the population looses a small amount of the Si interstitial atoms it contains. This quasi-conservative growth is followed by a sudden drop of the total number of Si atoms contained in the defects, the so-called dissolution regime. Atomistic simulations of the Ostwald ripening of Si precipitates in presence of an external sink have been run. In the model, it is assumed that superstable clusters of size 4 and 8 atoms exist and that the formation energy (per atom) of the {113} defects decreases when their size increases. These simulations perfectly fit the experimentally observed evolution of the size-distributions, densities and number of trapped interstitials for all temperatures. This work unambiguously shows that the mechanism driving the thermal evolution of {113} defects is an Ostwald ripening one and that the driving force for such an evolution is the decrease of the formation energy of the defects as they get longer. When the probability for a Si atom emitted by a defect to be trapped by the surface becomes of the same order than that to be trapped by another defect, the population starts to loose atoms with a high rate, its density decreases and consequently the loss rate increases further. This //catastrophic// coupling between the defect population and the surface is at the origin of the so-called defect dissolution. The thermal evolution of {113} defects in the vicinity of a recombining surface shows the typical transition from a quasi-conservative to a non-conservative Ostwald ripening. In general, such a behavior cannot be described by a simple exponential law.

4:15 PM C3.8
Doping and Mobility Profiles in Defect-Engineered Ultrashallow Junctions. Andy James Smith[1], Benjamin Colombeau[1], Russell Gwilliam[1], Erik Collart[2], Nicholas Cowern[1] and Brian Sealy[1]; [1]Advanced Technology Institute, Surrey University, Surrey, GU2 7XH, United Kingdom; [2]Applied Materials, Horsham, United Kingdom.

Silicon on Insulator (SOI) is a promising substrate material for future generations of CMOS devices with inherent advantages over bulk silicon. Performing non-amorphising MeV implants into SOI material has been shown to produce a vacancy rich region near the surface, separated from the deeper interstitial rich region by the buried oxide (BOX). We have already shown that this placement of the excess vacancies in the region of a shallow boron implant in SOI material can significantly retard the transient enhanced diffusion (TED) of the boron atoms. The present paper now considers the impact of vacancy engineering on the corresponding electrical activation. We aim to understand how control of the vacancy concentration distribution influences the electrically active boron concentration and the hole mobility as a function of depth. SOI wafers were implanted with 1MeV silicon ions with doses ranging up to $1x10^{16}$ cm^{-2}. Boron was then implanted at 500eV to a dose of $1x10^{15}$ cm^{-2} into the near-surface part of the vacancy-engineered region. Atomic profiles were determined using SIMS and electrical profiles were measured using a novel differential Hall effect technique, which enables profiling of electrically active dopants with a very shallow depth resolution. The electrical profiles provide pairs of carrier concentration and mobility values as a function of depth, which have been compared with published data to establish if the material is electrically compensated or not. Results suggest that mobility values are in accord with published data for good quality crystalline silicon. The paper will report on the role of the SOI layer and vacancy engineering conditions, as in suppressing TED and supporting high boron activation levels.

4:30 PM C3.9
The Manipulation of Dopants, Light Element Impurities and Point Defects in Silicon by Electron Irradiation. N. Stoddard[1], G. Duscher[1,2], W. Windl[1] and G. Rozgonyi[1]; [1]Materials Science and Engineering Department, North Carolina State University, Raleigh, North Carolina; [2]Condensed Matter Science Division, Oak Ridge National Laboratory, Oak Ridge, Tennessee.

It has been shown that 200 kV electron irradiation can introduce individual vacancies and self-interstitials via interaction with nitrogen. The use of nitrogen doping in high purity silicon has been an active research area in the last few years, since both Czochralski and Float Zone (FZ) single crystal silicon benefit in electronic and photovoltaic properties from the introduction of low concentrations ($< 10^{15}$ cm^{-3})

of nitrogen. Lattice atoms are given just enough energy to leave their lattice sites, and then prevented from recombining by the formation of an N-V complex. The interstitial atoms, stimulated by further electron collisions, diffuse away from the e-beam irradiated zone; then the nitrogen related complexes either accumulate vacancies to produce voids, or oxygen atoms to initiate SiO_2 nucleation. The benefit of this nanoscale TEM laboratory is that normally high-temperature extended defect nucleation processes are observed at room temperature in an area of the TEM operator's choosing. In addition to the interaction of beam electrons with light-element impurities, dopant diffusion can be enhanced in nitrogen-doped samples by the point defect enhancement and beam stimulation. In the absence of nitrogen, light elements such as boron can be driven to diffuse by electron irradiation [100] oriented N-doped FZ plan-view samples were prepared by conventional TEM thinning methods, including grinding, polishing, dimple grinding and ion milling. A Si sample implanted with $5*10^{15}$ cm^{-2} of 35 keV B^+ and 300 keV Sb^{2+} was prepared for TEM analysis by cross-sectional cleaving. The irradiation was performed at 200 kV in JEOL 2010F and Topcon 002B electron microscopes, while high-resolution imaging, Electron Energy Loss Spectroscopy (EELS), and scanning TEM (STEM) were performed on the JEOL instrument. Results will be presented where the experimental EELS spectra for vacancy and self-interstitial-rich regions are compared with simulations results. EELS spectra of point defects and their clusters are calculated based on the density of states, obtained using the Z+1 approximation applied with density functional theory. The results allow the consistent identification of vacancies, self-interstitials and aggregates thereof. Secondly, the application of the electron irradiation technique to the Sb and B co-implanted samples will be presented with Z contrast, EELS and scanning-tunneling microscope data. The uniqueness of this dopant configuration is 1) that Sb moves almost exclusively by a vacancy mechanism while B moves mostly by interstitial mechanisms and 2) that B is so much lighter of an atom than Sb, meaning that more energy can be imparted to it than to Sb. The combination of these two facts means that irradiation will cause significant diffusion of B while leaving Sb atoms relatively unmoved. The result will be a nanoscale pnp device structure of the approximate size of the irradiating beam.

4:45 PM C3.10
Investigation of Fluorine effect on the Boron diffusion by mean of Boron redistribution in shallow delta-doped layers.
Aomar Halimaoui[1], Jean Michel Hartmann[3], Cyrille laviron[3], Rebha El Farhane[2] and Frederic laugier[3]; [1]ST microelectronics, Crolles, France; [2]Philips semiconductors Crolles, Crolles, France; [3]LETI, CEA, Grenoble, France.

It has previously reported that F reduced boron diffusion. This diffusion reduction is often attributed to fluorine atoms that interact with the interstitials resulting in reduced TED. However, this is just a hypothesis without any experimental evidence. The exact role of fluorine on TED is still unclear and controversial. In this article, we have used Boron redistribution in a shallow Delta-doped Si structure in order to get some insights into the role of fluorine in the boron diffusion. The boron-doped delta Si structures used in this work were grown at 800degC and 20 Torr in an industrial Reduced Pressure Chemical Vapour Deposition system, using SiH2Cl2/HCl chemistry and B2H6 as boron source. The thickness of boron-doped layers was about 10 nm with a doping level of 1019/cm3. The structures consisted of 3 boron-doped layers separated by 40nm-thick undoped silicon. The as grown structure is preamophized by implanting Ge at 40 keV and a dose of 2x1015/cm2. We should mention that Ge implant conditions were chosen in such a way that the first (top) B-doped layer is entirely in the amorphous region, the second B-doped layer is in the crystal region but very close (underneath) to the Amorphous/Crystal (A/C) interface. The third layer is also in the crystal but far away from the A/C interface. After preamorphization, fluorine is implanted in some wafers at 20 keV and a dose of 2x1015/cm2. In such conditions, the top two B-doped layer are included in the Fluorine profile (the F concentration at the bottom side of the second B-doped layer is 1017/cm3). The effect of fluorine on boron diffusion is investigated by mean of SIMS depth profiling of B and F before and after annealing. After annealing at 650degC, we found that the deeper boron peak broaden, indicative of interstitials release from EOR. Although this interstitial release, the top two boron-peaks are found to be immobile. After a spike anneal at 1070degC, we observed a huge diffusion of boron from the two deeper B-doped layers. However, only a slight diffusion is observed from the top (close to the surface) B-doped layer. A phenomenological model is suggested to account for the observed behaviours. This model is based on the formation Fluorine-Vacancy clusters To support this model, TEM analysis is on going.

SESSION C4: Poster Session I
Chairs: Jorge Kittl and Marius Orlowski

Tuesday Evening, April 13, 2004
8:00 PM
Salons 8-9 (Marriott)

C4.1
Suppression of Ni Silicide Formation by Se Passivation of Si(001). Janadass Shanmugam, Michael Coviello, Darshak Udeshi, Wiley P Kirk and Meng Tao; University of Texas at Arlington, Arlington, Texas.

Valence mending of a semiconductor surface, such as the Se-passivated Si(001) surface, improves the chemical stability of the surface as compared to the bare Si(001) surface. In this talk, we report the suppression of interfacial reactions between Ni and Si(001) through monolayer passivation of Si(001) by Se. Ni was deposited on both Se-passivated and bare Si(001) surfaces. The samples were annealed at temperatures from 400°C to 700°C. Cross-sectional TEM revealed that Ni on bare samples reacted with Si at 400°C and formed silicide, whereas Ni on Se-passivated samples did not react with Si at 500°C. Surface composition analysis by XPS showed pure Ni surface on Se-passivated samples annealed at 400°C and 500°C, but silicide surface on bare samples annealed at the same temperatures. Hence, Se passivation suppresses the formation of Ni silicide on the Si(001) surface by over 100°C as compared to the bare Si(001) surface. These results may have important implications in source/drain engineering in sub-100 nm Si CMOS devices.

C4.2
Study of Ni(Pt) germanosilicides Formation on Fully-strained $Si_{0.9}Ge_{0.1}$ and $Si_{0.899}Ge_{0.1}C_{0.01}$ by Raman spectroscopy.
Joanna Yane-yin Chaw[1], Kin Leong Pey[1], Pooi See Lee[2], Dongzhi Chi[3] and Jinping Liu[2]; [1]Microelectronics Center, School of Electrical & Electronics Engineering, Nanyang Technological University, Singapore, Singapore; [2]Technology Development, Chartered Semiconductor Manufacturing Ltd, Singapore, Singapore; [3]Institute of Materials Research and Engineering, Singapore, Singapore.

The use of Raman spectroscopy to characterize the silicidation reaction of Ni and Ni(Pt) with Si and $Si_{1-x}Ge_x$ has previously been demonstrated. In this work, Raman spectroscopy was used to study the reaction of pure Ni and Ni(Pt 5 at.%) with fully-strained $Si_{0.9}Ge_{0.1}$ and $Si_{0.899}Ge_{0.1}C_{0.01}$ grown on Si(100) wafer and annealed by rapid thermal annealing (RTA). In addition, four point probe and X-ray diffraction (XRD) techniques were used to determine the sheet resistance and phase of the Ni(alloy) germanosilicides, respectively. With pure Ni, it was found that the incorporation of 0.1% C in the substrate resulted in out-diffusion of Ge from the germanosilicide film at 600°C, compared to 700°C for pure Ni on $Si_{0.9}Ge_{0.1}$. This Ge out-diffusion phenomenon is evident by the gradual shift in the $NiSi_{1-w}Ge_w$ ($w \leq x$) Raman peak from 213 cm^{-1} to higher wavenumbers, closer to 217 cm^{-1} reported for pure Ni/Si, an indication that Ge is being depleted from the film with increasing RTA temperatures. Hence, by monitoring this Raman shift, Ge out-diffusion from the film can be studied. In addition, it was found that severe agglomeration of the germanosilicide film occurred at a lower RTA temperature for the $Ni/Si_{0.899}Ge_{0.1}C_{0.001}$ system. From the Raman spectra, a sharp increase in the Si substrate peak at 520 cm^{-1} was observed, coupled with the appearance of the TA-phonon peak of Si at 301 cm^{-1}. When Pt was introduced into the Ni film, significant improvements in the germanosilicide film morphology was observed on both the $Si_{0.9}Ge_{0.1}$ and $Si_{0.899}Ge_{0.1}C_{0.001}$ substrates and it was shown that both Ge out-diffusion and agglomeration were delayed up to 800°C, a 50 to 100°C improvement as compared to that with a pure Ni film. Finally, it was also shown that the addition of Pt enhanced the formation of the low resistivity mono-germanosilicide phase at temperatures as low as 300°C. The Raman peak intensity of Ni(Pt) germanosilicide at 300°C was almost identical to those obtained at 400 and 500°C, indicating a possible full mono-germanosilicide formation at 300°C as compared to the mixed (Ni_2SiGe and NiSiGe) phase obtained with pure Ni. The results show that the addition of Pt is useful not only in improving the morphological stability of the germanosilicide film on fully-strained $Si_{0.9}Ge_{0.1}$ and $Si_{0.899}Ge_{0.1}C_{0.001}$, but also in lowering the formation temperature for the complete transformation of the mono-germanosilicide phase.

C4.3
Study of Nickel (Platinum) (Pt at.% = 0, 5, 10) Germanosilicide Formation Using Micro-Raman Spectroscopy. Lijuan Jin[1], Kin Leong Pey[1,2], Wee Kiong Choi[1,3], Eugene A Fitzgerald[1,4], Dimitri A Antoniadis[1,4] and Dongzhi Chi[5]; [1]Singapore-MIT alliance, National University of Singapore, Singapore, Singapore; [2]Electrical & Electronic Engineering, National Technological Univeristy, Singapore, Singapore; [3]Electrical & Computer Engineering, National University of Singapore, Singapore, Singapore; [4]Massachusetts Institute of Technology, Cambridge, Massachusetts; [5]Institute of Materials Science and Engineering,

Singapore, Singapore.

The interfacial reaction between 10 nm Ni(Pt) (Pt at.% = 0, 5, 10) and (100) $Si_{0.75}Ge_{0.25}$ substrate after rapid thermal annealing (RTA) between 400 and 900°C has been studied in detail using Micro-Raman spectroscopy. The results show that Ni or Ni(Pt) monogermanosilicide exists. For the Ni/$Si_{0.75}Ge_{0.25}$ system, a *broad* Ni($Si_{0.75}Ge_{0.25}$) peak at around 200cm^{-1} was clearly observed for the samples annealed 400 and 500°C, and two sharp and distinct peaks at 193 and 213cm^{-1} were found at annealing temperatures higher than 600°C. These peaks are similar to the reported results for the NiSi peaks. The decrease in the Ge concentration (i.e. Ge out-diffusion) in the NiSiGe grains with increasing annealing temperatures could be the mechanism responsible for the evolution of the broad peak into two distinct Raman peaks. The two distinct peaks correspond to the Ni($Si_{1-y}Ge_y$) phase with y <¡ 0.25. These results are in agreement with our previous Auger mapping and TEM results. In addition, the decrease in the Ge concentration in the NiSiGe phase with increasing temperature were further supported by a corresponding shift in the Ni-Si(Ge) peak towards a higher wavenumber in the Raman spectra, and a similar shift of the germanosilicide peaks towards a higher 2θ value in x-ray diffraction (XRD) spectra. For the Ni(Pt)(10%)/$Si_{0.75}Ge_{0.25}$ system, a *broad* Ni(Pt)SiGe peak was still observable at 600°C (i.e. 100°C higher than that of the pure NiSiGe grains). The broad peaks evolved into one distinct peak at 210 cm^{-1} at an annealing temperature higher than 700°C. The peak at 190 cm^{-1} was not apparent. For the Ni(Pt)(5%)/$Si_{0.75}Ge_{0.25}$ system, the results were similar to that of the Ni/$Si_{0.75}Ge_{0.25}$ system but with less Ge out-diffusion at higher temperature. In the Ni(Pt)/SiGe system, the evolution of a broad peak into distinct peak(s) with increasing temperature agrees with the mechanism that the depletion of the Ge concentration in the Ni(Pt)SiGe grains increases at higher annealing temperatures. Hence, Pt plays a critical role in suppressing Ge out-diffusion from the germanosilicide grains. And more Ge atoms are remained in the Ni(Pt)SiGe grains with higher amount of Pt added into the Ni(Pt) alloy.

C4.4

Ni Silicide Morphology on Small Features. Oxana Chamirian[1,2], Anne Lauwers[2], Jorge A Kittl[3], Mark Van Dal[4], Muriel de Potter[2], Christa Vrancken[2], Caroline Demeurisse[2], Richard Lindsay[2] and Karen Maex[1,2]; [1]Electrical Engineering, K.U. Leuven, Leuven, Belgium; [2]IMEC, Leuven, Belgium; [3]Affiliate researcher at IMEC from Texas Instruments, Leuven, Belgium; [4]Philips Research Leuven, Leuven, Belgium.

With continuous scaling down of device dimensions, issues in silicidation processes using CoSi2 result in the need for alternative materials. NiSi offers the advantages of low resistivity on narrow features and low silicidation temperatures. However, implementation of NiSi faces difficulties such as excessive silicidation on narrow lines, low thermal stability and epitaxial NiSi2 formation at low temperatures. In this work Ni silicide formation on narrow areas is studied in terms of the resulting silicide thickness and morphology, sheet resistance of narrow lines, and diode leakage. The presence of NiSi2 pyramids and the impact of device geometry and processing variables (dopants, processing temperatures, surface preparation) on their appearance will be addressed.

C4.5

Effects of Alloying on Properties of NiSi for CMOS Applications. Mark J. H. van Dal[1], Amal Akheyar[2], Jorge A. Kittl[3], Oxana Chamirian[4], Muriel de Potter[5], Anne Lauwers[5] and Karen Maex[4,5]; [1]Philips Research Leuven, Leuven, Belgium; [2]Affiliate researcher at IMEC from Infineon, Leuven, Belgium; [3]Affiliate researcher at IMEC from Texas Instruments, Leuven, Belgium; [4]E.E. Department K.U. Leuven, Leuven, Belgium; [5]IMEC, Leuven, Belgium.

CMOS technology is rapidly closing on the 45 nm node, pushing gate lengths to 25 nm and junction depths to 70 nm. Since scaling alone does not provide the improvements set by the ITRS Roadmap, the production of such small devices demands the integration of new materials with superior properties. For instance, NiSi is replacing $CoSi_2$ (industry/s choice for previous nodes) due to the instability of $CoSi_2$ on narrow poly gates [1]. One of the key issues for Ni silicide integration is its low thermal stability. It is well documented that thermal degradation of NiSi films can be reduced by adding an alloying element to Ni such as Ta [2], Pd [3] or Pt [3,4]. However, it is important to understand the impact of alloying on other silicide properties relevant to CMOS applications. In this paper we will present results of a study on the effect of alloying Ni with Pt and Ta with respect to (1) the process window of silicidation, (2) silicide/junction contact resistance extracted from transmission line measurements with a minimal segment length of 60 nm and (3) the stability of the Ni based silicides on narrow poly lines. First results have shown low silicide/junction contact resistance for the Ni, Ni+10%Pt and Ni+10%Ta silicides on As doped Si. Currently, contact resistance of these silicides on B junctions is under investigation. [1]. J. Kittl et al., Mater. Res. Soc. Symp. Proc. 765 (2003). [2]. M.C. Su et al., Symp. on VLSI Tech. (2003) 81. [3]. R.N. Wang et al., J. Phys.: Condens. Matter 15 (2003) 1935. [4]. D. Mangelinck et al., Appl. Phys. Lett. 75 (1999) 1736.

C4.6

Influence of ECR Plasma Hydrogenation on Nickel Silicide Formation. A. Vengurlekar[1], S. Balasubramanian[1], S. Ashok[1], D. Z. Chi[2] and D. Theodore[3]; [1]Pennsylvania State University, State College, Pennsylvania; [2]Institute of Materials Research and Engineering, Singapore, Singapore; [3]Motorola Inc., Tempe, Arizona.

Nickel monosilicide is a potential contender to replace the currently used class of silicides in CMOS devices. An important challenge in the improvement of silicide materials is the improvement of sheet resistance, because as the device is scaled down, the linewidth becomes narrower and the sheet resistance contribution to the RC delay increases. The large leakage currents observed in NiSi are also an issue of concern. The passivation of electronic defects in silicon by incorporation of atomic hydrogen is a well-known phenomenon. In this paper, we report on the characteristics of nickel silicide formed on silicon substrates subjected to an electron cyclotron resonance (ECR) plasma hydrogen (deuterium) treatment prior to nickel silicide evaporation. Silicon samples, both n-type and p-type, were subjected to hydrogen plasma treatment in an ECR plasma chamber. After cleaning, nickel silicide was formed on the samples by evaporation followed by rapid thermal annealing, at different temperatures (400-700 C). Control samples, without any hydrogenation treatment, were also fabricated. Sheet resistance measurements showed a significant decrease in resistance under hydrogen plasma treatment for samples annealed to 400 and 500 C. However this beneficial effect is absent at higher anneal temperatures. We attribute this to the passivation of defects in nickel silicide by hydrogen at lower temperatures, and out-diffusion of hydrogen at higher annealing temperatures. SIMS measurements showed the presence of small amounts of hydrogen in the samples annealed at lower temperatures, but not in those annealed at higher temperatures. Another feature observed was the enhanced diffusion of nickel beyond the silicide-silicon interface, into the silicon bulk, for the hydrogenated samples at annealing temperatures of 500 C and above. Cross-sectional TEM pictures of the samples showed dislocation loops for the hydrogenated samples annealed at 400 C. No significant change in silicide morphology was observed with hydrogenation. XRD measurements carried out on the NiSi samples did not show the formation of any extra phases in the hydrogenated samples. In conclusion, hydrogenation of Si prior to Ni deposition for silicide formation results in a lowering of the sheet resistance for temperatures below 500 C. Point defects created during hydrogen effusion result in enhanced nickel diffusion into the Si substrate.

C4.7

Effect of Ge-rich $Si_{1-z}Ge_z$ segregation on the morphological stability of $NiSi_{1-u}Ge_u$ films formed on strained (001) $Si_{0.8}Ge_{0.2}$ epilayer. Yao Haibiao[1], Dongzhi Chi[1], Shue Yin Chow[1], S. Tripathy[1], W.D. Wang[1], Soo Jin Chua[1], X.Q. Pan[2] and H.P. Sun[2]; [1]OESC, Institute of Materials Research & Engineering, Singapore, Singapore; [2]Department of Materials Science, University of Michigan, Ann Arbor, Michigan.

The solid state reaction of Ni on strained (001) $Si_{0.8}Ge_{0.2}$ was studied using various charaterization tools, with a particular emphasis on the influence of Ge-rich $Si_{1-z}Ge_z$ segregation on the morphological stability of $NiSi_{1-u}Ge_u$ films. XRD results showed that only mono-germanosilicide, i.e. $NiSi_{1-u}Ge_u$, was formed within the temperature range 400-800 °C. Micro-Raman was used to study the Ge-rich $Si_{1-z}Ge_z$ segregation by monitoring the emergence of 493 cm^{-1} Si-Si vibration signal from the segregated Ge-rich $Si_{1-z}Ge_z$ regions [1]. Micro-Raman results revealed that the onset temperature for Ge-rich $Si_{1-z}Ge_z$ segregation is critically dependent on the annealing time: 550 °C for 1s annealing and 450 °C for 180s annealing. XTEM images suggested that Ge-rich $Si_{1-z}Ge_z$ segregation takes place preferentially at the germanosilicide/$Si_{1-z}Ge_x$ interface, more specifically at the triple junctions between two adjacent $NiSi_{1-u}Ge_u$ grains and the underlying epi $Si_{1-x}Ge_x$, and it is accompanied with thermal grooving process. With prolonged annealing, the segregation process continued to proceed, and the segregated Ge-rich $Si_{1-z}Ge_z$ regions tend to grow up into the surface until complete breaking-up of the $NiSi_{1-u}Ge_u$ film. It is believed that the segregation process accelerates the thermao grooving of the $NiSi_{1-u}Ge_u$ grain boundaries at the interface. This is concluded based on the detailed analysis of XTEM images and comparison of SEM images of just agglomerated $NiSi_{1-u}Ge_u$ films with those of NiSi and NiGe films(formed on (001)Si and (001)Ge, respectively, and also just agglomerated). The observation of much smaller grains (0.1-0.2 μm) in just agglomerated $NiSi_{1-u}Ge_u$ films, as compared to

larger grains (0.5-2μm) in just agglomerated NiSi and NiGe films, can therefore been explained in terms of the suppressed grain growth by the segregation-acclerated grain boundary grooving. [1] W. Freiman, A. Eyal, Yu. L. Khait and R. Baserman, Appl. Phys. Lett. 69, 3821 (1996).

C4.8

Growth of epitaxially thin $CoSi_2$ layer using Co-N films as a cobalt source. Sunil Kim, SeungRyul Lee and ByungTae Ahn; Korea Advanced Institute of Science and Technology, Daejeon, South Korea.

Epitaxial layers of $CoSi_2$ grown on (100) Si substrate are of special interest because of their uniform and flat $CoSi_2$/Si interfaces, excellent thermal stability, low junction leakage, and ultra-shallow junction formation. For commercial application of $CoSi_2$ in nanoscale ICs, it is necessary to grow the epitaxial $CoSi_2$ layer as thin as possible, to obtain shallow junction with low leakage current. We developed a new method of forming a uniform epitaxial $CoSi_2$ layer with the thickness of less than 5nm, for the first time, using Co-N film as a cobalt source. The Co-N flim for epitaxial $CoSi_2$ layer was deposited either by reactive sputtering or by metallorganic chemical vapor deposition from cobalt carbonyl source ($Co_2(CO)_8$) using NH_3 gas at 350 450'C. The reactive sputtering was done using cobalt target in Ar and N_2 ambient at room temperature. Thin amorphous layer and silicide layer were observed between Co-N film and Si (100) substrate by cross-sectional TEM. Ti capping layer was deposited by magnetron sputtering on Co-N film because of cobalt oxidation during annealing. Epitaxial $CoSi_2$ layer on Si (100) substrate was formed by rapid thermal annealing for 5min at 800'C in Ar ambient. A few (111) $CoSi_2$ layer was observed with epitaxial $CoSi_2$ layer by XRD. For epitaxially thin $CoSi_2$ layer, Co-N film was annealed at the low temperature, 400 600'C. After annealing and unreacted metal etching, epitaxially thin and uniform $CoSi_2$ layer with 4 5nm thickness was formed. It was found that epitaxial $CoSi_2$ layer was formed by suppressing the concentration of cobalt due to amorphous layer between Co-N and Si interfaces during annealing.

C4.9

Growth of epitaxial CoSi2 from Cobalt Carbonyl on Si(100) Substrate. Raghunath Singanamalla[1], David W Greve[1] and Katayun Barmak[2]; [1]Electrical and Computer Engineering, Carnegie Mellon University, Pittsburgh, Pennsylvania; [2]Materials Science and Engineering, Carnegie Mellon University, Pittsburgh, Pennsylvania.

Beyond its applications in silicon MOSFETs, cobalt disilicide is potentially useful for the formation of epitaxially overgrown quantum dots and quantum wires. We report the formation of cobalt silicide on Si (100) and its overgrowth by silicon. Cobalt films approximately 3.5 nm in thickness have been deposited on Si (100) using a cobalt carbonyl organometallic source. We observe by RHEED that the deposited cobalt film is converted to epitaxial cobalt disilicide upon annealing at 850 C, considerably higher than the silicidation temperature typically observed for sputtered cobalt. We explain this behavior with the aid of SIMS profiling of the carbon and oxygen impurity concentrations. The cobalt disilicide layers have been overgrown with silicon at 625 C. We contrast the surface topology measured by AFM just after cobalt growth, after silicidation, and after overgrowth with silicon. The surface remains rough even after exposure to silane at a pressure of 0.55 mTorr for upto 60 minutes.

C4.10

Abstract Withdrawn

C4.11

The Use of SiGe Barriers During the Formation of p^+ Shallow Junctions by Ion Implantation. Phillip E. Thompson[1] and Susan Felch[2]; [1]Code 6812, Naval Research Laboratory, Washington, District of Columbia; [2]Varian Associates, Palo Alto, California.

Ion implantation is the standard production technique for the formation of shallow junctions. However dopant spread occurs by transient-enhanced-diffusion (TED) and boron-enhanced-diffusion (BED) after activation by rapid thermal anneal (RTA). Previously we have shown that the use of SiGe barriers increases the thermal stability of molecular beam epitaxy (MBE)-grown B-doped Si layers. In this presentation we show that the SiGe barriers reduce the B diffusion in ion implanted layers. 15 nm undoped Si layers on top of 10 nm SiGe barrier layers were grown by MBE on Si(100) Sb-doped (3−7 Ohm-cm) substrates. We have investigated 20% and 40% Ge alloys and have compared the results to pure Si samples. The wafers were plasma-doped using BF_3 at a voltage of 1 keV and doses of $1x10^{15}/cm^2$ or $5x10^{15}/cm^2$ and were activated by a 1050 ^oC spike anneal with a 250 K/s ramp-up rate and an 80 K/s ramp-down rate in a 100 ppm O_2 ambient in N_2. Sheet resistance, R_{sh}, measured in units of Ohm/square, was determined with 4-point probe, calibrated with an implantation standard. Room temperature Hall measurements were used to determine the sheet resistance, sheet carrier concentration, and the carrier mobility. The B atomic distribution profiles were obtained using a quadrapole secondary ion mass spectrometry (SIMS) instrument. ^{10}B and ^{11}B were monitored as positive ions under O_2^+ bombardment at an impact energy of 500 eV and an incidence angle of 45^o. The analysis chamber was backfilled with O_2 to a pressure of $6x10^{-7}$ torr to reduce secondary ion transient effects near the surface. The atomic concentrations of ^{10}B and ^{11}B were calculated from relative sensitivity factors (RSFs) determined from a standard sample of B in Si. The results show that the B redistribution is substantially reduced with the addition of SiGe barriers, producing a flat, box-like profile in the Si layer. The degree of the effect is proportional to the Ge content. For example, the B implant with a dose of $5x10^{15}/cm^2$ had its junction depth reduced from 48 nm without a barrier to 40 nm with the 20% Ge barrier and 35 nm with the 40% Ge barrier. The authors are especially grateful to Dr. Joe Bennett, International SEMATECH for SIMS, Ziwei Fang and Bon-Woong Koo of Varian Semiconductor Equipment Associates for the BF_3 plasma implants, and Wilfried Lerch of Mattson Technology for the spike anneals. The authors also wish to acknowledge Dr. Larry Larson, International SEMATECH, for his encouragement in pursuing this research and Mr. Larry Ardis, Naval Research Laboratory, for performing the Hall measurements. This work was supported by the Office of Naval Research.

C4.12

Strain Relaxation of Ion-implanted Strained Silicon on Relaxed SiGe. Robert T Crosby[1], Kevin Jones[1], Mark Law[1], Jinning Liu[2], A. N. Larsen[3], J. L. Hansen[3] and V. Craciun[4]; [1]SWAMP Center, University of Florida, Gainesville, Florida; [2]Varian Semiconductor Equipment Associates, Gloucester, Massachusetts; [3]Institute of Physics and Astronomy, University of Aarhus, Aarhus, Denmark; [4]Major Analytical Instrumentation Center, University of Florida, Gainesville, Florida.

The relaxation processes of strained silicon films on silicon-rich relaxed SiGe alloys have been studied. Experimental structures were generated via Molecular Beam Epitaxial (MBE) growth techniques and contain a strained silicon capping layer of approximately 50 nm. The relaxed SiGe alloy compositions range from 0 to 30 atomic perecent germanium. Samples received two distinct types of silicon implants. A 12 keV Si implant at a dose of 1x1015 atoms/cm3 was used to generate an amorphous layer strictly confined within the strained Si cap. An alternate 60 keV Si implant at a dose of 1x1015 atoms/cm3 was employed to create a continuous amorphous layer extended from the sample surface to a position 50 nm into the bulk SiGe material. The strain relaxation effects are quantified through various analysis methodologies. Secondary Ion Mass Spectroscopy (SIMS) profiles will access the occurrence of germanium inter-diffusion, while High Resolution X-Ray Diffraction (HRXRD) rocking curves will be used to determine the strain state of the silicon capping layer. Transmission Electron Microscopy (TEM) techniques are utlized to measure the thickness of the strained silicon film, monitor the growth and evolution of misfit and threading dislocations, as well as to quantify extended Type II defects morphologies. The role of injected silicon interstitials upon the strain relaxation processes at the Si/SiGe interface are discussed at length.

C4.13

Fabrication of Ultra Shallow Junctions (USJ) in silicon by excimer laser doping from spin-on glass sources. Stephane Coutanson Coutanson[1], Eric Fogarassy[1] and Julien Venturini[2]; [1]CNRS / PHASE, STRASBOURG, France; [2]SOPRA-SA, PARIS, France.

In the last few years, laser processing of semiconductors has been regarded as a promising technique for manufacturing new generations of microelectronic devices in silicon. According to the International Technology Roadmap for Semiconductors (ITRS), the doping technology requirements for the MOSFET source and drain (S/D) regions of the future CMOS generations is a major challenge. A critical point of this evolution is the formation of Ultra Shallow Junctions (USJ). As an alternative to the Rapid Thermal Processing (RTP), Laser Thermal Processing (LTP) was demonstrated to be suitable for the doping of Si by different ways, including laser annealing of ion implanted dopant and laser induced diffusion of dopant from gas or solid sources like Spin-On Glass (SOG). This presents the advantage not to require any vacuum system. In this work was investigated this simple laser doping method employing phosphosilicate (PSG) and borosilicate (BSG) glass films as dopant sources (dopant concentration : up to $2x10^{21}$ cm^{-3}) which are deposited onto Si by the spin coating technique. Both short (20 ns) and long (200 ns) pulse duration excimer laser beams were used to deposit a large amount of energy in short time onto the near-surface region. Under suitable conditions, the irradiation leads to surface melting and dopant incorporation by liquid phase diffusion from the surface. The final distribution profiles of the dopants (P and B) in the

two pulse duration regimes were studied by Secondary Ion Mass Spectrometry (SIMS) and their electrical activation was deduced both from classical techniques (sheet resistance and Hall effect) and from non-contact infrared spectroscopic ellipsometry (Drude model). Finally, both n+/p and p+/n ultra shallow junctions (<50 nm in depth) were prepared in optimized laser processing conditions and their electrical characteristics were discussed in the framework of the future technological requirement.

C4.14
Low Resistant Contacts to Laser Annealed Junctions.
Eun-Ha Kim, Peter B. Griffin and James D. Plummer; Center for Integrated Systems, Stanford University, Stanford, California.

As MOS devices scale down to smaller dimensions, contact resistance will dominate the overall series resistance associated with current flow from source to drain. Contact resistivities below $10^{-7}\Omega$-cm^2 are required for sub-100nm node devices, which represents the lowest contact resistivity that can be obtained with a maximum electrically active doping level of 2×10^{20} cm^{-3} and normal barrier heights associated with metal-silicon contacts. We have employed a laser annealing technique in order to further increase the active concentration beyond the solubility limit and investigated how these super-saturated doping levels can help reduce contact resistance. In this work, junctions were created by either laser annealing or conventional RTA, then the silicon layer was reacted with titanium or nickel to form silicide contacts at varying silicidation temperatures (400-800°C). Contact resistance measurements were performed and the corresponding specific contact resistivity was extracted based on transmission line models. An increase in contact resistance was observed at higher silicidation temperatures, due to the deactivation of super-saturated doping created by laser annealing. A particularly low contact resistance can be obtained by minimizing the thermal budget for silicidation. Nickel silicide forms at lower temperatures, and thus we have found that nickel silicide contacts show better compatibility with the laser annealing process than titanium silicide.

C4.15
Influence of Layer Stacks on Long Pulse Excimer Laser Annealing of Ultra-Shallow Junction in Silicon.
Julien Venturini[1], Miguel Hernandez[1] and Cyrille Laviron[2]; [1]Laser Division, SOPRA, BOIS-COLOMBES, France; [2]DTS, CEA-DRT - LETI, Grenoble, France.

Long Pulse Excimer Laser Annealing (LP-ELA), is considered so far to properly activate Ultra Shallow Junction (USJ) for next CMOS technology nodes beyond 65 nm as defined by the International Technology Roadmap for Semiconductors. Particularly, the specific thermodynamic cycle induced in silicon by a long laser pulse leads to interesting behaviour in both the solid phase and molten phase. According to the chosen process, one wants to reach high activation rate (solid phase) or reduced damage of the poly-Si gates (molten phase). In order to optimize the coupling of the laser light in the source and drain region to be activated between the poly-Si gates, while avoiding thermal modification of the poly-Si gates, we study here the influence of a layer stack (including both anti-reflective and reflective coatings) deposited on a Ge pre-amorphized BF2 implanted Si wafers. The process of activation of the USJ by a long pulse excimer laser (XeCl, λ = 308 nm, 200 ns) is studied as a function of the nature and the thickness of the deposited layer. Both molten phase and solid phase regime are evaluated. We rely here on four-point probe resistivity measurements, secondary ion mass spectroscopy (SIMS) depth profiles and Infra-Red Spectroscopic Ellipsometry (IRSE). Melting threshold and efficiency of the activation of the USJ are reported for the different layer stacks, defining new laser process windows. This process window and related integrity of the poly-Si gates is also discussed.

C4.16
Advanced Thermal Processing of Semiconducting Materials Using Flash Lamp Annealing.
Wolfgang Skorupa[1,2], Dieter Panknin[1], Matthias Voelskow[1], Wolfgang Anwand[1], Thoralf Gebel[2] and Rossen A Yankov[2]; [1]FWIM, Forschungszentrum Rossendorf e.V., Dresden, Germany; [2]nanoparc GmbH, Dresden, Germany.

The successful use of energy pulses from flash lamps for the advanced thermal processing of semiconducting materials will be reported at two examples: (i) For ultra-shallow junction formation in silicon Flash Lamp Processing (FLP) has become one of the challenging methods to meet the requirements for the next technology nodes defined by the ITRS roadmap. Low energy boron implants have been heat-treated in this way using peak temperatures in the range of 1100o to 1300oC and effective anneal times of 20 msec and 3 msec. Secondary ion mass spectrometry and four point probe measurements have been undertaken to determine the junction depth and the sheet resistance, respectively. Optimum processing conditions using a pulse time of 3 msec have been identified, under which one can obtain combinations of junction depth and sheet resistance values that meet the 90 nm and even the 70 nm technology node requirements. (ii) Another challenging task is related to the production of SiC-on-Silicon substrates to overcome for selected applications the need in high cost bulk SiC wafers. Using FLASiC (Flash Lamp Supported Deposition of 3C-SiC) a remarkable improvement in the quality of such cubic phase SiC layers was demonstrated performing a nanoscale liquid phase epitaxy process at the interface SiC/Si.

C4.17
Flash Lamp Annealing for 65 nm Node : Finding a Common Anneal Condition for All the Implants.
Francois Wacquant[1], Rebha El Farhane[2], Jeff Gelpey[3] and Steve McCoy[3]; [1]STMicroeletronics, Crolles, France; [2]Philips, Crolles, France; [3]Vortek Industries Ltd., Vancouver, British Columbia, Canada.

Flash lamp annealing has proven over the recent years to be a very promising technique for ultra shallow junction formation. With this anneal, the wafer is exposed to a short pulse (in the millisecond range) of intense light. This allows to reach very high temperature which improves dopant solubility and therefore activation, with minimal diffusion. However, some questions remain on the possibilities to integrate this new anneal on real devices. Indeed, the same unique anneal has to give the right activation level for all different kind of implants such as ldd, source/drain, pockets, gate etc... In this paper, we discuss results obtained on the so-called Flash-assist RTP (fRTP) anneal. We show that it is possible to obtain As and BF2 ldd junctions that meet the ITRS 65 nm specification with the same flash condition. Source/drain implants were also annealed with this technique and proved to be correctly activated. Finally, gate activation has been simulated on full sheet wafer. We show that it is possible, with minor change on the device integration scheme, to obtain the right dopant profile and activation. Thus the same fRTP anneal might be able to fulfill all requirements for all 65nm node implants.

C4.18
P Type Junction Engineering for 65 nm Node : Use of BF2 Implant Defects to Improve Activation With Minimal Diffusion.
Francois Wacquant[1], Rebha El Farhane[2] and Frederic Salvetti[2]; [1]Metal R&D, STMicroelectronics, Crolles, France; [2]Philips, Crolles, France.

In this paper the formation of P type junction has been extensively studied with the use of a design of experiment (DOE). Junction was formed by BF2 implant followed by spike anneal, in a wide range of dose (2e14 at.cm-2 to 1e15 at.cm-2), energy (from 0.5 keV to 4 keV) and temperature (1000°C to 1100°C). Sheet resistance (Rs) and junction depth (Xj) are modelled by a polynom of 2nd order depending on these 3 parameters. This simple model appears to be very efficient to predict the main junction characteristics over the entire studied domain. In particular, we show that the junction activation is not only depending on the spike anneal temperature but also on the implant condition. This suggests that the change of defects distribution due to various implant doses and energies plays a significant role on the activation mechanism of B. This gives therefore a new degree of freedom to improve junction activation without enhancing diffusion. Indeed in the last years, main focus to improve sheet resistance for given junction depth was to use sharper and sharper spike anneals that allowed to go to higher temperature. On the contrary, we show here that careful dose and energy choice allow to reach the ITRS 65 nm node specification with low temperature spike anneal.

C4.19
Defect evolution along trench edges in oxide patterned silicon wafers.
Nina Burbure and Kevin S Jones; University of Florida, Gainesville, Florida.

Pattern induced defects during advanced CMOS processing can lead to lower quality devices with high leakage currents. Within this study, the effects of oxide trenches on implant related defect formation and evolution in Si patterned wafers is examined. Oxide filled trenches approximately 4000Å deep were patterned into 300 mm <100> silicon wafers. Patterning was followed by the ion implantation of Si at energies ranging from 10 to 80 keV. Samples were amorphized with doses of $1x10^{15}$ atoms/cm^2, $5x10^{15}$ atoms/cm^2, and $1x10^{16}$ atoms/cm^2. Two independent repeating structures were studied. The first structure is comprised of silicon oxide filled trench lines, 3.7μm wide spaced 12.5μm apart, while the second structure contains silicon squares, 0.6μm on a side, surrounded by a silicon oxide filled trench. Cross-sectional and plan-view TEM samples were used to examine the defect morphology after annealing at temperatures ranging from 600°C to 950°C for various times between 1 second and 4 hours. An array of defects was observed to form near the surface at the silicon/silicon oxide interface. These trench edge defects are not related to recrystallization of the amorphous layer. They appear to coarsen with both increasing annealing time and temperature. The

width of the defect layer as seen in plan-view increases with increasing implant energy. It is believed that these defects arise from condensation of point defects at the silicon/silicon oxide interface and strain appears to play a role. Possible sources of these point defects will be discussed.

SESSION C5: Ultra-Shallow Junction Formation Engineering
Chairs: Alain Claverie and Richard Lindsay
Wednesday Morning, April 14, 2004
Room 2002 (Moscone West)

8:30 AM *C5.1
Optimized Doping and Annealing for Ultra-Shallow Junctions for 65nm and Beyond. Jeffrey Gelpey[1,3], Daniel Downey[2], Steve McCoy[3] and Edwin Arevalo[2]; [1]Vortek, Boston, Massachusetts; [2]Varian Semiconductor Equipment Associates, Gloucester, Massachusetts; [3]Vortek Industries, Vancouver, British Columbia, Canada.

To meet the requirements of smaller devices while still maintaining high performance, it is necessary to form very shallow source/drain extensions with very high activation. Although significant progress has been made in meeting these requirements as outlined in the ITRS, continued progress in meeting the needs for the 65nm technology generation and beyond remain a challenge. It will no longer be sufficient to consider the doping (ion implantation) and activation (annealing) steps independently. Both must be opimized together as a process sequence. Improvements have been made on the doping side in both traditional beamline implantation and advanced processes such as plasma doping. Advanced activation methods such as improved spike RTP anneals, solid phase epitaxial regrowth (SPER) and millisecond annealing using either flashlamps or sub-melt laser processing have been investigated and all have shown promise. This paper will survey the requirements for USJ doping and activation for the 65nm node and beyond and discuss some of the recent results in both doping and activation. Some comparisons of the annealing of shallow PLAD-doped silicon wafers using various advanced activation techniques will be presented and some discussion of the ultimate limits on "conventional" doping and activation schemes will be proposed.

9:00 AM C5.2
Evaluation of flash annealing technique for the formation of Ultra Shallow Junctions. Rebha El Farhane[1], Woo Sik Yoo[3] and Aomar Halimaoui[2]; [1]Crolles 2, Philips semiconductors, Crolles, France; [2]Crolles 2, St microelectronics, Crolles; [3]Wafermasters, San Jose, California.

The formation of Ultra Shallow Junction (USJ) is becoming a challenging task in the fabrication high-performance CMOS devices. The standard process that is a spike anneal, using Lamp-based system, is reaching its limit in the formation of USJ for 65 nm-node and beyond. Recent published data have shown that Flash annealing is a promising technique. It has been demonstrated that this technique can be achieve diffusion-less activation of implanted dopants. In the flash annealing systems, the rapid heating is achieved by radiation in the UV spectrum. In such a case, only the top surface of the wafer is heated. The bulk of the substrate is thus used as sink for a very fast cool down. We have used this technique to fabricate very shallow and well-activated junctions. SIMS measurements have shown that, for some conditions, there is no measurable diffusion of dopants that are highly activated as revealed by electrical measurements. Indeed, p+/n junction with a sheet resistance below 700 ohm/sq. and a depth of 20 nm can be easily achieved. By optimising the implant conditions (including preamorphisation step) more aggressive junctions that are compatible with 45 nm-node can be achieved. The comparison of three different techniques of annealing (with more or less aggressive thermal budget) clearly shows the benefit of the preamophization combined to fast ramp rates during annealing. We will also show the importance of preannealing conditions prior to the flash in performing shallow and well-activated junctions.

9:15 AM C5.3
Millisecond Microwave Annealing: Reaching the 32 nm Node. Keith Thompson[1,2], John H Booske[1], John Lohr[3], Lawrence Ives[2], Ken Kajiwara[3] and Yurii Gorelov[3]; [1]Electrical Engineering, University of Wisconsin, Madison, Wisconsin; [2]Calabazas Creek Research, Inc, Santa Clara, California; [3]General Atomics, San Diego, California.

Next generation, i.e. 65 nm node, ultra-shallow junctions must be less than 17 nm deep with a sheet resistance, Rs, lower than 760 ohms/square [1]. The current state of implant technology, taking into account reasonable throughput and cost considerations, results in as-implanted junction profiles that are slightly shallower than this 17 nm limit. To meet the ITRS requirements, the subsequent thermal anneal process must result in very little net diffusion while activating the implanted dopants and repairing the implant damage. One potential solution is an ultra-fast spike anneal to 1300C with the time above 800C limited to only a few milliseconds. Indeed, reports over the last 2 years indicate that millisecond annealing with advanced flash-lamp technology has resulted in a very effective, zero-diffusion, high temperature anneal process [2]. While lamp-based technology currently dominates the commercial rapid thermal processing, RTP, market, recent advances in high-power microwave equipment make microwave annealing a unique alternative to lamp-based systems. We have constructed a high-power microwave reactor that is capable of heating Si to 1300C in only a few milliseconds. This system utilizes an advanced gyrotron designed to produce more than 1 MW of continuous wave radiation at a frequency of 110 GHz. The optimal thermal treatment achieved to date with this system involves a 300,000C/sec ramp rate to 1300C; only 2 milliseconds above 800C. Net diffusion of the dopants into the wafer is extremely unlikely on this time scale, and the target temperature is high enough to ensure that a large fraction of the implanted dopants are activated. This millisecond microwave anneal process was applied to several 2.5 cm square Si samples that were pre-amorphized with Ge at 30 keV and implanted with B+ at 500 eV. The average Rs after the anneal was 542 ohms/square. Repeating this experiment on Si samples that were implanted with BF2 at 2200 eV, no pre-amorphization, resulted in an average Rs of 615 ohms/square. This talk describes the microwave reactor design and the millisecond microwave heating technique necessary to achieve the ultra-fast temperature ramp rates described. The advantages of microwave annealing, as well as the technical challenges to further implementation will be discussed. There will also be a full analysis of the ultra-shallow junctions formed including sheet resistance as measured by 4-pt. probe and junction depth as measured by SIMS. 1. International Technology Roadmap for Semiconductors, found at: http://public.itrs.net 2. J. Gelpey, K. Elliott, D. Camm, S. McCoy, J. Ross, D.F. Downey, E.A. Arevalo, "Advanced Annealing for Sub-130nm Junction Formation" in Proc. of the Electrochemical Society: Rapid Thermal and Other Short-Time Processing Technologies III, vol. pp. 2002-11, 2002.

9:30 AM C5.4
Activation, Diffusion and Defect Analysis of a Spike Anneal Thermal Cycle. Silke Paul[1], Wilfried Lerch[1], Xavier Hebras[2], Nikolay Cherkashin[2] and Fuccio Cristiano[2]; [1]Process Development, Mattson Thermal Products GmbH, Dornstadt, Germany; [2]Ion Implantation Group, LAAS-CEMES/CNRS, Toulouse, France.

Spike anneals in conjunction with ultra-low energy implants are widely used to form ultra shallow junctions for source/drain extensions in advanced CMOS devices. A deep understanding of the different phenomena involved in forming these junctions (including activation and diffusion anomalies and related defect evolution) is therefore mandatory. In this paper, the evolution of sheet resistance, junction depth and defects during the whole thermal cycle of a typical spike anneal (1050 °C) is investigated in detail. Therefore spike anneals were interrupted at peak temperatures ranging from 800 °C up to 1050 °C in temperature steps of 50 °C. These experiments were done both on B^+ (500 eV, 10^{15} cm^{-2}) and BF_2^+ (2.2 keV, 10^{15} cm^{-2}) implanted wafers. All wafers were analyzed with four point probe and SIMS, while selected samples were analyzed with TEM and SRP. It is found that BF_2^+ implanted wafers exhibit a much better electrical activation than B^+ implanted ones at temperatures below 850 °C, due to the amorphisation process occurring during the BF_2^+ implant. In this low temperature regime, Boron clustering takes place very rapidly in B^+ implanted wafers, as confirmed by both SIMS and TEM analysis. In particular, large clusters, i.e. with diameter above the TEM detection limit (2 nm), undergo a classical Ostwald ripening process (increase in size, decrease in density). SRP measurements indicate that Boron activation in this low temperature regime is not related to clusters dissolution. On the other hand, after the initial Solid Phase Epitaxial Growth, BF_2^+ implanted wafers exhibit an increase in sheet resistance, due to boron clustering induced by the dissolution of EOR defects. Finally, it is found that at higher spike anneal temperatures (above 850 °C), both B^+ and BF_2^+ implanted wafers exhibit a similar behavior, with a progressive decrease in sheet resistance due to Boron clusters dissolution and dopant diffusion. In summary, this work shows how only by choosing a large set of complementary analysis techniques, it is possible to achieve a thorough understanding of the activation mechanisms involved in forming ultra-shallow junctions.

9:45 AM C5.5
Technology computer aided design of ultra-shallow junctions in Si devices formed by laser annealing processes. Antonino La Magna[1], Paola Alippi[1], Vittorio Privitera[1], Guglielmo Fortunato[2], Marco Camalleri[3] and Bengt Svensson[4]; [1]CNR-IMM Sezione Catania, Catania, Catania, Italy; [2]CNR-IFN Sezione Roma, Roma, Italy; [3]STMicroelectronics, Catania, Italy; [4]Department of

Phisics, University of Oslo, Norway.

The laser annealing process, applied to the formation of ultra-shallow junctions in Si, offers important advantages respect to conventional thermal process such as: the control over the junction depth and a higher dopant activation efficiency. However, the process integration is extremely critical. Indeed, the irradiated transistor structure itself acts as a complex scattered to the laser light. Moreover, the concurrent evolution of the thermal field, molten regions and dopant density during the process is not predictable without suitable computational tools. Here, we present a complete methodology to the simulation of laser annealing process in transistor structures. Our approach is based: a) on the simulation of electromagnetic field in the structures formed layer of lossy (e.g. Si) or non-lossy (e.g. SiO2) dielectrics, b) on the simulation of the thermal phase and impurity fields under irradiation. Using the former tool, based on a finite difference time domain approach, we calculate the heat source distribution in the specimen. Afterwards, such source distribution is used as input in the second simulation approach, based on a phase field formalism, aimed to simulate the local temperature and phase changes and the consequent dopant redistribution during the laser annaling process. The tools are implemented in view of their integration in technology computer aided design packages. We solved numerically the phase field equations in two dimensional structures, considering as initial status the generic material modification due to an ion implant process: i.e. the implanted impurity two dimensional profile in structured samples containing also SiO2/a-Si/c-Si stacks. The model is parametrised in the case of different impurity atoms, considering the thermal properties of the materials and the impurity depending diffusivity in the solid, liquid and interfacial region (characterised by a finite dimension). In selected impurity cases molecular dynamics simulation are also used to assess such parameters. We present various simulation results by varying not only materials, implanted impurity profiles, and geometry of the CMOS-like structures but also the laser pulse conditions. With the support of the simulation results we discuss the possible problematic and the new perspectives of the excimer laser annealing process application in the fabrication of scaled CMOS devices. The simulated evolution is compared to experimental characterisation of laser annealed samples performed by secondary ions mass spectroscopy and spreading resistance profiling, transmission electron microscopy and selective etch delineation. The comparisons show the importance between the joined theoretical and and experimental investigation in order to understand the effect of laser annealing process on our specimens.

10:30 AM *C5.6
Ultra-Shallow Junction Formation Technology from the 130 to the 45 nm Node. Amitabh Jain, Texas Instruments Inc., Dallas, Texas.

One of the main materials challenges of the 130 nm silicon technology node was the need to find a processing solution to the anomalous diffusion behavior of ion-implanted dopants known from three decades of research. Reduction of implantation energy no longer proved sufficient when trying to reduce source/drain extension junction depth while increasing abruptness and limiting sheet resistance. Spike annealing, a new process in which ion implanted silicon can be heated rapidly to a temperatures required for dopant activation and then cooled down without dwelling at temperature, adequately addressed the scaling requirements of this node. The resulting junctions achieved high dopant concentration values very close to the surface while limiting junction depth. However, this increased the propensity for dopant migration to overlying layers associated with the source/drain spacer. Loss of device performance due to this and other integration-related phenomena became a strong motivating factor for further materials research in order to sustain progress through the 130 nm and 90 nm node. Complex interactions between various layers have been understood and the resulting developments in spacer materials have enabled high performance devices. Whereas the new processes have enabled early 65 nm node development, there are strong indications that they will place constraints on technology before the beginning of the 45 nm node, particularly where high performance is desired. The constraints are likely to show up first in terms of inadequate junction abruptness and then also in terms of junction depth reduction. Recent experiments using ultra-high temperature annealing with arc-lamps or cw lasers have shown that it is possible to obtain high activation while maintaining junction depth and abruptness defined by the initial implant if appropriate processing conditions are chosen. Problems associated with residual damage remain and require further investigation.

11:00 AM C5.7
Electrical profiles of ultra-low energy antimony implants in silicon. talal alzanki[1], Erik Collart[2], Russell Gwilliam[1], Neil Emerson[1] and Brian J Sealy[1]; [1]School of Electronics and Physical Sciences, University of Surrey, Guildford, Surrey, GU2 7XH, United Kingdom; [2]Parametric and Conductive Implant Division, Applied Materials, Horsham, W-Sussex, RH13 5PX, United Kingdom.

Antimony is being considered as an alternative to arsenic for the production of ultra-shallow junctions for future generations of CMOS devices. However, it is unclear as to what implant and anneal conditions produce the best electrical results for device applications. Our earlier work on 40 keV implants showed that annealing below 800°C produced electrical profiles which were identical to the as-implanted atomic profiles, with no measurable diffusion of the antimony. However, annealing at 900°C to 1100°C produced significant diffusional broadening of the electrical and atomic profiles, with a concurrent decrease in the peak electron concentration. We have continued this work by studying the electrical characteristics of both 2keV and 5keV implants of antimony at doses of $1x10^{15}$ cm^{-2}. We use a novel differential Hall effect technique to obtain accurate values of both the electron concentration and mobility profiles with a depth resolution of about 2nm. Differential Hall measurements show that junction depths of less than 20nm can be achieved. For example, the 5keV implants have junction depths of about 20nm and resistivities of about 400 ohms/square. However, the 2keV implants have junction depths in the range 15-20nm but with very high sheet resistivities of around 1200 ohms/square. The results for both the 2keV and the 5keV implants agree well with the 40keV data in that below 800°C there is no significant diffusion of antimony, but at 900°C and above the profiles broaden considerably. It appears that junction depths can be determined to a good approximation from the theoretical atomic profiles when annealing is performed at or below 800°C. We will report on a detailed study of the electrical characteristics of the antimony implanted silicon layers as a function of annealing conditions in the range 600°C to 800°C for times of seconds to hours. We will include a comparison of the electrical data with atomic profiles measured using SIMS and RBS measurements to determine the residual damage and crystal quality.

11:15 AM C5.8
Optimization of Fluorine co-implantation for PMOS Source and Drain extension formation to meet the 65nm technology node. Houda Graoui, Amir Al Bayati, Suzanne Felch and Majeed Foad; Front End Product Group, Applied Materials, Sunnyvale, California.

The main challenge for the Ultra shallow junction formation of PMOS remains the transient enhanced diffusion (TED) and the relative low solid solubility of boron in silicon. It has long been demonstrated that low energy boron and the spike annealing are key in meeting the 90 nm technology node ITRS requirements. To meet the 65 nm technology requirements (Xj<17nm, Rs<760Ohms/sq, abruptness<2.8 nm/decade) many studies have used Fluorine co-implantation with boron and Si or Ge preamorphization and spike annealing to meet these requirements. The Fluorine has been shown to reduce TED but its energy needs to be well optimized with respect to the Boron implant energy. In this work we demonstrate that not only the fluorine energy needs to be optimized to the boron's but to the germanium preamorphization step as well. We will show that the final junction formation depends on the preamorprhization dose and energy. We will also show when the fluorine co-implant is implemented, significant improvements are observed in sheet resistance, junction depth and abruptness over the junction formed only with Ge and B.

11:30 AM C5.9
Suppression of Boron Transient Enhanced Diffusion by Fluorine in Preamorphized Silicon. Giuliana Impellizzeri[1], Jose' Henrique R. dos Santos[1], Salvo Mirabella[1], Francesco Priolo[1], Enrico Napolitani[2] and Alberto Carnera[2]; [1]Department of Physics and Astronomy, MATIS-INFM & University of Catania, Catania, Italy; [2]Department of Physics, INFM & University of Padova, Padova, Italy.

It is well known that the addition of F, either separately (B + F implants) or simultaneously with B (BF_2 implant) in silicon, can decrease the transient enhanced diffusion (TED) of B, but the mechanism by which this phenomenon occurs has not been unambiguously explained as yet. On the one hand, it has been argued that fluorine interacts with self-interstitials, reducing their ability to pair with B and reducing as a result the B diffusion. On the other hand, it has been claimed that the presence of F has no bearing on the point-defect population, but there should be instead a strong B-F chemical interaction causing a drop of B diffusion. In this work, the role of fluorine in the reduction of B TED has been investigated. As a marker for the self-interstitial local concentration, we have employed a boron spike layer grown by molecular beam epitaxy. The fluorine atoms were incorporated into preamorphized Si through ion implantation to fluences of $7X10^{12}$, $7X10^{13}$ or $4X10^{14}$ cm^{-2}. The energy of the implants was 100 keV, so that the F profile overlaps with the B one, being entirely contained within the preamorphized region. The amorphized and F-implanted samples were then recrystallized by solid phase epitaxy, which leads to the formation of extended defects

beyond the original amorphous-crystalline (a-c) interface, the so-called *end − of − range* defects. Finally, we performed thermal anneals under different conditions, in order to induce the release of self-interstitials from these defects and thus provoke the TED of B atoms. The results obtained show several interesting characteristics. First, during the regrowth process, F atoms undergo segregation towards the surface region, although a substantial quantity of F remains in the regrown matrix. Second, after the recrystallization, F diffuses both towards the surface and towards the bulk, where it accumulates in the end-of-range region. Third, F diffusion is not affected by the B presence, there being no indication of B-F complexes formation through clustering. Fourth, the B TED decreases with the amount of incorporated F, up to its complete suppression for the highest fluence. Nevertheless, after annealing at 1100 ^{o}C for 30 s, we have observed a complete out diffusion of F, with the B marker experiencing diffusion consistent with TED for this thermal budget. Fifth, F is shown to be able to diminish the diffusion of B even under thermal equilibrium concentration of self-interstitials. These results allow us to conclude that there is no direct interaction between B and F, which rules out B-F chemical bonding as responsible for the slowing down of B TED. Instead, the B diffusion decreasing is owing to a strong interaction between F and self-interstitials, which results in the reduction of self-interstitials concentration.

11:45 AM C5.10
Post-Anneal Stress Reduction of 200 mm Silicon Wafers in Single Wafer Rapid Annealing. Tsuyoshi Setokubo[1], Eiichi Nakano[1], Kazuo Aizawa[1], Hidekazu Miyoshi[1], Jiro Yamamoto[1], Takashi Fukada[2] and Woo Sik Yoo[2]; [1]Hiroshima Elpida Memory, Inc., Hiroshima, Japan; [2]WaferMasters, Inc., San Jose, California.

For advanced ULSI devices below 130nm design rules, the precise control of thermal budget is one of the key issues in thermal processing from the device performance point of view. Minimizing the variation in device performance is very important for device yield management and quality control. With the shrinkage in device dimensions and allowable thermal budgets, lamp-based, single wafer rapid thermal annealing (RTA) systems became very popular for limited thermal processing applications. However, thermally induced stress in wafers during RTA processes causes small distortions on the wafer surface. This increases the difficulty of subsequent lithography steps, as the resolution of lithography is influenced by the local and global flatness of the wafer. In a lamp-based (cold wall) RTA system with multiple zone temperature functions, the temperature of an individual zone is dynamically controlled using feedback signals from in situ pyrometric temperature measurement of the corresponding zone on the wafer. Precise wafer temperature control and measurement are a significant technical challenge, as lamp power is constantly modulated by the feedback signals from the wafer temperature monitoring zones. In the dynamic wafer temperature control mode used in the lamp-based RTA systems, it is difficult to maintain temperature uniformity during the process. Local and global temperature repeatability depends on many factors, such as emissivity distribution on the wafer, chamber wall temperature and chamber wall reflectivity. Frequent calibration and maintenance is required. For advanced ULSI device applications, the temperature uniformity, temperature repeatability, emissivity dependency and pattern density effects of lamp-based RTA systems must be improved from both device performance and process integration points of view. In this paper, the authors performed a comparative annealing study of several critical RTA process steps using a hot wall-type single wafer rapid thermal furnace (SRTF) system to investigate the post-anneal wafer stress in wafers annealed using a lamp-based (cold wall) RTA system and a furnace-based (hot wall) SRTF system. Stress of various types of wafer (bare, patterned, product wafer) was measured before and after RTA under various annealing conditions. In mass production of DRAM devices with 110nm design rules, the authors were able to significantly improve electrical characteristics and post-anneal wafer stress by switching annealing steps from a lamp-based RTA system to a furnace-based SRTF system. The flatness of wafers after annealing in the SRTF system was improved around 100 times compared to those annealed using the lamp-based RTP systems. This was due to the nearly isothermal process environment of the SRTF system and the flat surface of the annealed wafers providing better results in subsequent lithography steps. The detailed wafer stress measurement data will be presented at the conference.

SESSION C6: Atomistic Simulation Approaches
Chair: Wolfgang Windl
Wednesday Afternoon, April 14, 2004
Room 2002 (Moscone West)

1:30 PM *C6.1
Modeling atomistic ion-implantation and diffusion for simulation of MOSFET intrinsic fluctuation arising from line-edge Roughness. Masami Hane, Takeo Ikezawa and Tatsuya Ezaki; Silicon Systems Research Laboratories, NEC Corporation, Kanagawa, Japan.

We have developed new simulation tools for the more precise designing of sub-100nm MOSFETs in which the intrinsic statistical aspects of the structure appear as fluctuations in device characteristics. Our three-dimensional atomistic approach to both process and device simulations enables us to closely examine the coupling effects of the most significant sources of such fluctuation, line-edge-roughness and random-discrete-dopants, in terms of these effects in practical fabrication processes. Intrinsic random variations in sub-100nm MOSFET device characteristics are expected to place significant limits on further aggressive progress in device scaling. Gate poly-silicon line-edge-roughness (LER) is one significant source of such fluctuation. Previously, several studies based on experiment or simulation have raised the alert about the problem of LER effects. The lack of reliable 3D tools, however, has meant that most previous simulations of LER have been 2D-slice simulations, although there is no inherent reason for 3D effects to be small. Furthermore, for smaller gate-length MOSFETs, the average size of the poly-Si grains becomes comparable to the gate-length, and penetration of the channel by halo implanted ions depends on the crystal orientation at the sidewall of the gate mask. In this simulation work, we modeled the statistical nature of the discrete dopant distributions by using Monte Carlo procedures for ion-implantation and dopant-diffusion/activation processes to computationally generated different LER patterns for each device. The 3D device simulations were based on the classical drift-diffusion approach in which electrostatic potentials are constructed from the long-range Coulombic components of the individual dopant atom potentials. This simulation system was applied to sub-100nm super-halo designed MOSFETs. We found that LER not only modulates Lg but also increases effective dosages from halo-implantation, since it effectively increases the area of the mask side-walls. This leads to increased penetration of the channel region by ions when halo-implantation is applied at a large tilted angle. Consequently, we saw a positive shift in average Vth for devices with Lg=65nm, and a negative shift in average Vth for devices with Lg=45nm. The analyses through simulation also revealed some diffusion-eliminating annealing processes, such as the extremely quick annealing technique called flash-lamp-annealing (FLA), rather enhances the fluctuations that arise from LER. Thus, using atomistic process simulation to examine LER has led to non-trivial insights that will be useful in further optimization of the design of fabrication processes.

2:00 PM C6.2
Fast Diffusion Mechanism of Tri-Interstitial in Si. Yaojun Du, Richard G. Hennig and John W. Wilkins; Department of Physics, The Ohio State University, Columbus, Ohio.

Abinitio nudged-elastic-band and dimer method calculations determine the dynamics of small interstitial clusters in Si. The compact tri-interstitial cluster moves as a five-atom hexahedron along the [111] directions. The correlated motion consists of a 1.31 Å translation and a 60° rotation. The compact tri-interstitial jumps with equal probability into one of the four equivalent, neighboring sites along the [111] bond directions, i.e., it diffuses through the Si bulk. The computed 0.5 eV activation energy and $0.8{\cdot}10^{-4}$ cm^2/s prefactor are strikingly similar to the measured overall interstitial diffusion rate of $10^{-5}{\cdot}\exp(-0.4\ \mathrm{eV}/k_B\mathrm{T})$ cm^2/s. We speculate that the compact tri-interstitial dominates (i) the diffusion of small interstitial Si clusters and (ii) the formation of {311} planar defects.

2:15 PM C6.3
Theoretical investigations of In-related defects in silicon. Paola Alippi, Antonino La Magna, Silvia Scalese and Vittorio Privitera; CNR-IMM, Catania, Italy.

Indium is considered as an alternative to boron as p-type dopant in silicon: although it shows a lower electrical activity, it allows in fact the realization of steeper as-implanted profiles, due to its heavier mass. Increased activation is found in samples co-implanted with carbon, presumably due to the shallow electronic level associated to In-C complex. The present work is aimed at filling the lack of atomistic theoretical investigations on In defects in silicon, providing a well-founded ab-initio picture of defects energetics and diffusivity over which a continuum diffusion model is built. Equilibrium geometries and formation energies of In complexes with silicon native defects, vacancy (V) and interstitials (I), and with C impurities are investigated within density functional theory, using the Vienna Ab-initio Simulation Package. We determine the migration energies of I- and V-mediated diffusion mechanisms through the location of the saddle points along the minimum energy paths. We also identify the In-C complex responsible for the increased electrical activation in In C-doped silicon samples and discuss its formation mechanism from the ab-initio results. Motivated by the results on In-C pair, we present

a preliminary study of In-Ge defects in silicon, aimed at discussing the efficiency of alternative isovalent (i.e., Ge) co-doping in improving In activation. Furthermore, we integrate the first principle results into a continuum diffusion model that allows the direct comparison with experimental data. The diffused profiles obtained by the simulations are compared to those measured by secondary-ion-mass-spectroscopy after implantation and thermal annealing, showing a noteworthy agreement at different process conditions.

2:30 PM C6.4
An Atomistic to Continuum View: Dynamic Simulation of Carbon-mediated Self-Interstitial Clustering in Silicon.
Sumeet Singh Kapur and Talid Sinno; Chemical and Biomolecular Engineering, University of Pennsylvania, Philadelphia, Pennsylvania.

Nucleation, growth and dissolution of Silicon self-interstitial clusters play an important part in silicon processing. Self-interstitial clusters produced during ion-implantation of boron become unstable and redissolve during annealing, creating large self-interstitial supersaturation. The presence of excess self-interstitials enhances the diffusion of implanted boron, leading to the so-called Transient Enhanced Diffusion (TED) effect. Self-interstitial clusters are also known to lead to large dislocation loop networks during Czochralski crystal growth and prevent the use of interstitial-rich material for device applications. In both cases, it is well known that a carbon atom concentration of over 1019 cm3 in the region of self-interstitial supersaturation greatly reduces interstitial cluster size evolution, but the exact mechanism remains under debate. In this work, we study the effect of carbon on self-interstitial aggregation using consistent atomistic and continuum representations. In the atomistic approach, two large-scale parallel molecular-dynamics (PMD) simulations were carried out using the multi-component Tersoff potential in a system containing 216,000 silicon atoms, each with an additional 1,000 self-interstitials initially placed in uniformly spaced tetrahedral sites. In the second simulation cell, 2,000 substitutional carbon atoms also were present, corresponding to a carbon concentration of about 0.9 % (4.6x1020 atom/cm3). We find that presence of carbon leads to slower average cluster size evolution, as is observed in crystal growth experiments. On the other hand, the evolution of single self-interstitials is unaffected by the carbon atoms, and only the evolution of larger cluster sizes show a marked difference between the two simulations. These results are investigated further with long-time diffusion calculations for each cluster size with and without carbon. The aggregation and diffusion simulations are interpreted quantitatively with a mean-field model that confirms the hypothesis that carbon mediates interstitial clustering by interfering with cluster transport and not directly on single self-interstitials. The mean-field model subsequently is used to investigate longer time evolution relevant to crystal growth and wafer processing.

2:45 PM C6.5
Accurate and fast Monte Carlo simulation of ion implantation into arbitrary 1D/2D/3D structures for Si technology.
Shiyang Tian[1], Victor Moroz[2] and Norbert Strecker[2]; [1]Synopsys, Inc., Dallas, Texas; [2]Synopsys, Inc., Mountain View, California.

As the semiconductor industry aggressively scales silicon device feature sizes down to sub-100nm regime, Si processing technology moves toward high-tilt implants with complex 3D device geometry and topography and diffusionless (<3nm) activation. Ion implantation simulation is one of the most critical steps for accurate prediction of dopant placement in a silicon device. The well-known stand-alone MC ion implantation simulators are not suitable for such tasks. In order to overcome this problem, we have developed an integrated MC simulator, which is capable of simulating implants into any amorphous materials and crystalline silicon with arbitrary geometry and topography and is capable of predicting the 1D/2D/3D as-implanted dopant distributions from sub-keV to above 10 MeV for common dopant species. Our model is based on the classical binary collision approximation (BCA) such as that used by TRIM for amorphous material and UT-MARLOWE for crystalline silicon. We used ZBL universal interatomic potential for nuclear scattering, and a modified version of electronic stopping power model which combines both local and nonlocal contributions. Damage accumulation is based on the modified Kinchin-Pease formula. The dechanneling effect of the damage is realized by switching the model from crystalline to amorphous collision model with the probability proportional to local defect concentration. This scheme is very computationally efficient, and is 10 times faster than MARLOWE-based simulators for highly damaged implants. We have implemented trajectory split and lateral trajectory replication algorithms which greatly reduce the simulation time. With the improved efficiency and seamless interface with diffusion simulations, MC implant simulation as a better alternative to analytic implant in a complete process flow becomes realistic. With this simulator, we investigated 2D LDD and halo implants, and 3D cylinder and square trench implants, and illustrated the importance of <110> channeling and lateral scattering for sub-100nm silicon technology. It is demonstrated that, in contrast to analytic implant model, integrated MC simulator is particularly suitable for high tilt halo implants, as well as implants into complex 3D structures (such as FinFET), as the complex geometry and topography, high tilt channeling effect, as well as pre-existing damage are accurately taken into account automatically. Therefore, integrated MC implant simulator is ideally suited for predictive TCAD simulations for silicon technology.

SESSION C7: Boron Activation and Diffusion Modeling
Chair: Mark Law
Wednesday Afternoon, April 14, 2004
Room 2002 (Moscone West)

3:30 PM C7.1
Boron-Interstitial Cluster Kinetics: Extraction of Binding Energies from Dedicated Experiments.
Christophe J. Ortiz[1], Giovanni Mannino[2], Peter Pichler[1], Vittorio Privitera[2], Sandro Solmi[3] and Silvia Scalese[2]; [1]Technology Simulation Dpt., Fraunhofer IISB, Erlangen, Germany; [2]IMM-CNR Sezione Catania, Catania, Italy; [3]IMM-CNR Sezione Bologna, Bologna, Italy.

In ULSI fabrication, ion implantation at ultra-low energy is nowadays a standard method for introducing dopants such as boron into silicon. Generally, this step must be followed by a high-temperature process step in order to anneal the implant damage and to electrically activate the dopant atoms. However, during annealing, boron exhibits large transient enhanced diffusion (TED) due to the high self-interstitial (I) excess concentration produced by ion bombardment. Moreover, boron activation can be incomplete, even at concentrations well below solid solubility. Small boron-interstitial clusters (BICs), which immobilize and deactivate boron were clearly identified as the main reason. However, their stoichiometry and their dissolution kinetics are still under debate. The aim of this paper is to extract binding energies of BICs by inverse modeling from dedicated experiments. For the experiments, a B-doped Si structure was prepared by chemical vapor deposition (CVD). The structure consists of a 200 nm-thick boron box with a concentration of 1×10^{19} cm^{-3} up to a depth of 0.5 μm and two lightly B-doped delta layers. After the growth, implantation damage was generated by 60 keV silicon implants with doses between 2×10^{13} and 1×10^{14} cm^{-2}. Subsequently, the wafers were annealed in nitrogen atmosphere in the temperature range 600-950°C for times varying from 2s up to 4h. Boron diffusion was analysed by means of SIMS, whereas the electrical activation was evaluated by SRP. In order to investigate the BICs dissolution kinetics, a model including the formation of {113} defects and of BICs was implemented in the PDE solver PROMIS 1.5. Our simulator was linked to a genetic algorithm to optimize values for binding energies of BICs from data obtained under different experimental conditions. The calibrated model we propose is able to predict the formation/dissolution of BICs in a wide range of experimental conditions. This work is part of the FRENDTECH Project and is funded by the European Community as IST/2000-30129.

3:45 PM C7.2
Quantitative investigation of boron-interstitial-cluster formation and dissolution.
Davide De Salvador[1], Salvatore Mirabella[2], Enrico Napolitani[1], Gabriele Bisognin[1], Elena Bruno[2], Giuliana Impellizzeri[2], Leonardo Aldegheri[1], Antonio Drigo[1], Alberto Carnera[1] and Francesco Priolo[2]; [1]Dipartimento di Fisica, INFM e Universita' di Padova, Padova, Italy; [2]Dipartimento di Fisica e Astronomia, MATIS - INFM e Universita' di Catania, Catania, Italy.

Boron is the primary p-type dopant in Si device fabrication. It was largely demonstrated that in presence of a high self-interstitials (I) supersaturation (typically produced by ion implantation and subsequent annealing) and a boron concentration above 10î8 B/cm3̂, B and I's tends to co-precipitate in immobile and electrically inactive clusters (BIC). This fact hinders the scaling-down of Si microelectronic devices being necessary to this aim progressively higher B concentration fully active. In this work we have investigated the formation and the dissolution of BICs in a 15 nm thick boron box at a very high B concentration (around 10ˆ20 B/cm3̂) grown by Molecular Beam Epitaxy (MBE). The B box is capped by 200 nm of Si, while below the B box a set of three narrow B spikes were inserted for monitoring the I supersaturation. The BICs are formed in a controlled way by a 20 keV- Si implantation in the cap layer at different doses and a subsequent annealing, in order to dissolve the implantation damage and to induce the I diffusion towards the B box and the subsequent B clustering. By means of Secondary Ions Mass Spectrometry (SIMS) measurements of B profiles and a proper modeling of B-delta markers diffusion, we have estimated the B and I doses trapped in the BIC both after their formation and during their subsequent dissolution at different temperatures. Moreover the BICs have been investigated by High Resolution X-Ray Diffraction (HRXRD) bringing to a precise determination of the strain status

induced by the BICs in the different investigated conditions. These analyses provide important information for the structure determination and evolution dynamics of BICs when formed and dissolved at high B concentrations.

4:00 PM C7.3
Atomistic Analysis Of The Role Of Silicon Interstitials In Boron Cluster Dissolution. Maria Aboy, Lourdes Pelaz, Luis A. Marques, Pedro Lopez and Juan Barbolla; University of Valladolid, Valladolid, Spain.

Ion implantation is the preferred method for introducing dopants into silicon. Subsequent thermal annealing is used to remove the implant damage, and electrically activate dopants, such as boron. However, in the initial stages of the annealing B clusters are formed and thus, a significant amount of B atoms are immobilized and are electrically inactive. High temperatures or long annealing times are required to completely activate the B atoms by the slow dissolution of these B clusters. A number of theoretical and experimental data have revealed the role of Si interstitials in the nucleation and growth of B complexes. In this work, we investigate through atomistic kinetic Monte Carlo simulations the role of Si interstitials in the stabilization and dissolution of B clusters. The implantation process generates a high Si interstitial supersaturation, leading to the rapid formation of B-Si interstitial complexes. Then the system evolves towards lower Si interstitial superaturations established by the B-Si interstitial complexes and other Si interstitial clusters or extended defect ({311} defects or loops). Also an oxidizing ambient during the anneal establishes a larger Si interstitial supersaturation compared to anneals in inert ambient. Our analysis indicates that the B cluster dissolution is slower in the presence of higher Si interstitial supersaturations. The simulation shows that the reactivation of B during the post-implant thermal treatment is slower in an oxidizing ambient than in inert ambient, in agreement with experiments [L. Radic et al, Appl. Phys. Lett. 81, 826 (2002)]. This result is consistent with Si interstitial rich B clusters having a lower total energy than those poor in Si interstitials, as proposed by several authors [L. Pelaz et al, Appl. Phys. Lett. 74, 3657 (1999); X.-Y. Liu et al, Appl. Phys. Lett. 77, 2018 (2000)]. The presence of Si interstitial superaturations favors the capture of Si interstitials by B clusters, leading to B clusters rich in Si interstitials, and hence, more stable.

4:15 PM C7.4
BIC Formation and Boron Diffusion in Relaxed Si0.8Ge0.2. Robert T Crosby[1], L. Radic[1], Kevin Jones[1], Mark Law[1], Jinning Liu[2], P. E. Thompson[3], Tony Saavedra[1] and M. Klimov[4]; [1]SWAMP Center, University of Florida, Gainesville, Florida; [2]Varian Semiconductor Equipment Associates, Gloucester, Massachusetts; [3]Electronic Technology Division, Naval Research Laboratory, Washington, District of Columbia; [4]Advanced Materials Processing and Analysis Center, University of Florida, Florida, Florida.

The relationships between Boron Interstitial Cluster (BIC) evolution and boron diffusion in relaxed Si0.8Ge0.2 have been investigated. Structures were grown by Molecular Beam Epitaxy (MBE) with surface boron wells of variant composition extending 0.25 mm into the substrate, as well as boron marker layers positioned 0.50 mm below the surface. The boron well concentrations are as follows: 0, 7.5x1018, 1.5x1019, and 5.0x1019 atoms/cm3. The boron marker layers are approximately 3 nm wide and have a peak concentration of 1x1019 atoms/cm3. Samples were ion implanted with 60 keV Si at a dose of 1x1014 atoms/cm2 and subsequently annealed at temperatures ranging from 600oC to 750oC for various times. Transmission Electron Microscopy (TEM) was used to monitor the agglomeration of injected silicon interstitials and the evolution of extended defects in the near surface region. Secondary Ion Mass Spectroscopy (SIMS) concentration profiles facilitated the characterization of boron diffusion behaviors during annealing, while Hall Effect van der Pauw techniques facilitated the measurement of active boron concentrations. High Resolution X-Ray Diffraction (HRXRD) rocking curves were also employed to observe potential strain compensation effects between the boron and germanium constituents. Interstitial supersaturation conditions and the resultant defect structures of ion implanted relaxed Si0.8Ge0.2 in both the presence and absence of boron have been succinctly characterized. The role of strain compensation in the retardation of boron diffusion in relaxed Si0.8Ge0.2 is also discussed further.

4:30 PM C7.5
The Effect of Photoresist Outgassing on Boron Clustering and Diffusion in Low Energy BF2+ Ion Implantation. Peter Kopalidis and Serguei Kondratenko; Axcelis Technologies, Beverly, Massachusetts.

During high current ion implantation into photoresist-covered substrates, evolution of gaseous by-products of photoresist breakdown occurs that can affect the dose control of the process as well as diffusion and activation of the implanted dopants in silicon. The dosimetry effects are well understood and accounted for in modern ion implanter design. In this work, we report on the effect of photoresist outgassing on the distribution of boron concentration in silicon during the subsequent annealing process, boron electrical activation and sheet resistance measurements. Experiments were performed on mono-crystalline and pre-amorphized silicon and oxide covered wafers that help elucidate the mechanism of boron accumulation and diffusion. The effects of activation temperature and photoresist carbon-containing species driven in by the ion implantation are investigated and a mechanistic explanation is presented. Finally, practical ways are proposed that ensure accurate dosimetry and sheet resistance repeatability, independent of the photoresist load.

4:45 PM C7.6
Hydrogenation-enhanced Low Temperature Activation of Boron in Silicon. A. Vengurlekar[1], S. Ashok[1] and C. E. Kalnas[2]; [1]Pennsylvania State University, State College, Pennsylvania; [2]Solid State Measurements Inc, Pittsburgh, Pennsylvania.

Device scaling and the corresponding decrease in the amount of free charge necessitate increasing the charge concentration in these regions by adding more dopant atoms and successfully activating them. Dopant clustering as well as transient enhanced diffusion due to ion implantation are additional problems that need to be addressed. The ability to activate the dopants at lower temperatures is also desirable. A recent effort to achieve this involves creating a vacancy-rich region around the boron profile by higher energy silicon implantation. The presence of vacancies enhances the boron activation. On a separate but related note, previous theoretical and experimental works have shown that the presence of atomic hydrogen leads to enhanced activation of other kinds of dopants in crystalline silicon, by relaxation of strain in the lattice. In this work, we report on the effect of hydrogen plasma treatment by an ECR plasma on the activation and diffusion of boron in silicon at ultra-shallow depths. It is known that plasma hydrogenation followed by annealing results in creation of vacancies by the out-diffusion of hydrogen during annealing. We aim to make use of the vacancies created by hydrogen effusion during rapid thermal annealing to influence activation in the boron-implanted region at various annealing temperatures. Boron was implanted into n-type silicon at 5 keV at a dose of 5E14 cm-2. Prior to implantation, some of the samples were subjected to an ECR hydrogen plasma (using deuterium instead of hydrogen to enable SIMS measurements). After implantation, the samples were rapid thermal annealed over the temperature range 450 - 850 C. Spreading resistance profiling (SRP) was carried out on all the samples to determine the profile of the electrically active boron. It was seen that there was enhanced activation of boron at the annealing temperature of 450 C. However no significant difference was observed at higher annealing temperatures. The enhancement in boron activation at lower temperature was attributed to the creation of vacancies at the boron-implanted region, in addition to the lattice-relaxation effect by the presence of atomic hydrogen. At higher temperature, more of the hydrogen diffuses and vacancies created by hydrogen out-diffusion are annealed out. SIMS measurements of the boron profile in the samples will be presented along with earlier positron annihilation data to shed further light on the role of hydrogen on boron activation and diffusion. We would like to acknowledge the assistance of Dr. Christine Kalnas and the generous support of Solid State Measurements in carrying out the spreading resistance measurements.

SESSION C8: Poster Session II
Chairs: Benjamin Colombeau and Peter Pichler
Wednesday Evening, April 14, 2004
8:00 PM
Salons 8-9 (Marriott)

C8.1
Deactivating defects of group V donors in heavily doped silicon. Dominik Christoph Mueller and Wolfgang Fichtner; Integrated Systems Laboratory, Swiss Federal Institute of Technology, Zurich, Zurich, Switzerland.

We report new insight into the deactivation mechanisms of P, As and Sb in Si. Based on our ab initio calculations, we suggest a 3 step model which is able to explain experimental data in highly n-doped samples. In the absence of excess native point defects, donor deactivation comes about by lattice distortions that form readily in the proximity of two or more donor atoms. Hence, this deactivation mechanism is strongly dependent upon the donor concentration and becomes predominant at doping levels above 10^{20} cm^{-3}. Since the process takes place without rearrangement of the impurities in the crystal, it is able to explain the measured saturation of conduction electrons above donor concentrations of approximately $5{\cdot}10^{20}$ cm^{-3} in samples prepared by low temperature molecular beam epitaxy. These

donor deactivating distortions (δ^3 for short) are a precursor to the experimentally observed Frenkel pair generation and donor-vacancy clustering. The latter constitute the second step of deactivation, observed at higher process temperatures, where diffusion of donors and point defects is prevalent. Ultimately, precipitation may set in as a last step in the deactivation chain, most prominently in the case of the large Sb atoms in Si.

C8.2
Arsenic adsorption onto silicon stepped surfaces studied by Hartree-Fock at semiempirical level. Anna Maria Mazzone, Istituto IMM, CNR, Bologna, Italy.

Arsenic adsorption onto silicon surfaces vicinal to (100) has been studied using the cluster model of the exposed surface and the Hartree-Fock method at semiempirical level. The results illustrate the properties of the As-doped steps in dependence of the step structure and of the type, substitutional or interstitial, of the impurity. The central finding is that arsenic is preferably adsorbed in the interstitial location and the physical explanation is the stronger electrostatic coupling with the step. Preferred pathways of As from surface to bulk are discussed. The study illustrates also the formation of step states and bands and the effects of As on these states.

C8.3
Classical MD Study on the Mobility of Di- and Tri-Interstitials. Matthias Posselt, Institute of Ion Beam Physics and Materials Research, Forschungszentrum Rossendorf, Dresden, Germany.

In a recent work [1], a combined simulation method was applied to investigate ion-beam-induced defect formation in silicon. BCA simulations were used to treat the ballistic processes, whereas the subsequent fast relaxation and the first stage of thermally activated processes were described by classical MD calculations. It was found that the metastable defect structure formed immediately after ion impact consists not only of isolated vacancies and self-interstitials but also of complex defects. A more detailed analysis of the results shows, that at elevated implantation temperatures or during the annealing of the defect structures obtained at room temperature, di- and tri-interstitials are formed. In some cases a high mobility of these defects is observed. In agreement with former studies [2,3], the di-interstital is found to move relatively fast. The present contribution deals with systematic investigations on the migration of di- and tri-interstitials. The classical MD simulations allow direct investigations of the motion of defects and its atomic mechanisms. Particular attention is paid to the role of transformations between different modifications of di- or tri-interstitials. These transformations may lead to an substantial increase or decrease of the defect mobility. The present results are compared with the few literature data obtained by tight-binding and density-functional methods which employ mainly static potential energy calculations. [1] M. Posselt, Mat. Res. Soc. Symp. Proc. 647 (2001) O2.1.1. [2] G. H. Gilmer, T. Diaz de la Rubia, D. M. Stock, M. Jaraiz, Nucl. Instr. Meth. Phys. Res. B 102 (1995) 247. [3] M. Hane, T. Ikezawa, G. H. Gilmer, Proc. SISPAD 2000, IEEE Catalog Number 00TH8502, p. 119 , IEEE, Piscataway, 2000.

C8.4
Interactions of Indium, Arsenic and Carbon in silicon using the pseudopotential technique. Xiyu Yan, Maxim Chichkine and Maria Merlyne De Souza; Emerging Technologies Research Centre, De Montfort University, Leicester, Leicestershire, United Kingdom.

Indium (In) is a promising option for achieving punch-through suppression and threshold voltage control in sub 100 nanometer MOSFET technologies. However, In suffers from poor activation and excessive diffusion due to Transient Enhanced Diffusion. There is an urgent requirement to resolve these issues for the 60 nm node. In comparison to the conventional p-type dopant boron, the substitutional indium introduces a deeper level in the bandgap of silicon. Using the pseudopotential planewave method (VASP), indium defects and their levels introduced within the bandgap are investigated. VASP [1] is based on density functional theory [2] in LDA approximation [3]. Ultrasoft pseudopotentials [4] were used in 64 atom supercells with 4 special k-points for integration of the Brillouin zone. For In, Si and As atoms the cut off energy of 150 eV was used, for C the cut off was increased to 250 eV. Indium activation is found to be inhibited in silicon, when two adjacent substitutional sites are occupied by these large atoms. On the other hand, the presence of the smaller carbon atom on an adjacent substitutional site enhances the activation of Indium in agreement with experiment [5,6]. This fact limits the maximum activation which can be achieved with Indium alone. Additionally, carbon efficiently trap self-interstitials, thus preventing them from forming inactive configurations with In. The influence of As atom on a substitutional site is to counter-dope the Indium atoms accompanied by a narrowing of the bandgap. On the other hand, aggregation of Indium-Arsenic atoms is inhibited via the Arsenic interstitial, in comparison to the Indium interstitial. The binding between As and In on substitutional sites is stronger than that between In and Carbon. References: [1] G Kresse and J Furthmuller, Comput Mater.Sci 6.16 (1996) ; G Kresse and J.Hafner, Phys.Rev B 47 558 (1993) [2] W Kohn, L.J.Sham, Phys.Rev., Vol.140,A1133 (1995) [3] Perdew, J.P and A Zunger, Phys.Rev.B 23 5048. (1981) [4] D. Vanderbilt, Phys Rev B, vol 41 7892-7895 (1990) [5]. H. Boudinov et al, JAP, 86, No 10, 5909 (1999). [6].S. Scalese, et al, Journal of Applied Physics Vol 93 No. 12 pg 9773 (2003).

C8.5
Behavior of Vacancies, Interstitials and Boron-Interstitial Pairs at the Si/a-SiO2 Interface. Taras A. Kirichenko[2], Decai Yu[1], Gyeong S. Hwang[1] and Sanjay K. Banerjee[2]; [1]Chemical Engineering, The University of Texas, Austin, Texas; [2]Electrical and Computer Engineering, University of Texas, Austin, Texas.

Fabrication of forthcoming nanometer scale electronic devices faces many difficulties including formation of extremely shallow and highly doped junctions. At present, ultra-low-energy ion implantation followed by high-temperature thermal annealing is most widely used to fabricate such ultrashallow junctions. In the process, a great challenge lies in achieving precise control of redistribution and electrical activation of dopant impurities. Native defects (such as vacancies and interstitials) generated during implantation are known to be mainly responsible for the transient enhanced diffusion(TED) and also influence significantly the electrical activation/deactivation. It is therefore necessary to develop a detailed understanding of diffusion and annihilation of vacancies and interstitials, along with dynamics of defect-dopant complexes. The Si substrate is generally covered with a thin amorphous oxide layer. The behavior of defects and defect-dopant complexes at the Si/a-SiO2 interface will be different from that in the Si bulk as well as on bare Si surfaces. However, a detailed study of the defect-dopant dynamics at the Si/a-SiO2 interface is still lacking despite its importance, particularly in defect annihilation and dopant precipitation. The fundamental understanding is essential for predicting diffusion profile evolution and electrical activation of dopants. In this talk, we will present our density functional theory calculation results on i) annihilation of vacancies and interstitials and ii) diffusion and precipitation of boron species at the Si-SiO2 interface. We find both vacancies and interstitials are significantly stabilized at the interface. Their configuration and energetics and the origin of their stabilization will be presented. We also find that boron-interstitial pairs become unstable near the interface, which, in turn, leads to boron precipitation and TED reduction. Along with the configuration and energetics, we will also show changes in i) bonding mechanisms (based on electron density and electron localization function topologies) and ii) diffusion pathways and barriers of vacancies, interstitials, and boron-interstitial complexes near the Si/a-SiO2 interface.

C8.6
Indium Diffusion Behavior and Implantation-Induced Damage in Indium Implanted Silicon-on-Insulator. Peng Chen[1], Ming Zhu[2,1], Zheng Hua An[2], Ricky King Yu Fu[1], Wei Li Liu[2] and Paul K. Chu[1]; [1]City University of Hong Kong, Hong Kong, Hong Kong; [2]Shanghai Institute of Microsystem and Information Technology, Shang Hai, China.

Ion implantation induced damage and the diffusion behavior of indium implanted into silicon-on-insulator (SOI) substrates at different energies and doses and annealing at different temperatures were studied. Using Rutherford backscattering spectroscopy (RBS) in the channeling mode and secondary ion mass spectrometry (SIMS), the redistribution of indium in both the top silicon and buried SiO2 layer of SOI after annealing was investigated. At a relatively high implantation energy and dose (200 kV, 1e14 cm-2), the diffusion behavior of indium in SOI is different from that in bulk silicon. Indium segregates to the buried Si/SiO2 interface and the effects of end of range indium damage are quite prominent. Our results indicate that in-diffusion of indium is effectively blocked and so transient enhanced diffusion (TED) is less pronounced in SOI than in bulk Si, thereby making it easier to get a steep retrograde channel profile (SRCP) in SOI that is beneficial to subsequent device fabrication. Hence, the use of indium as an n-channel dopant in SOI is a distinct possibility.

C8.7
Experimental characterization and modelling of indium implanted in silicon. Silvia Scalese, Antonino La Magna, Paola Alippi and Vittorio Privitera; CNR-IMM, Catania, Italy.

A systematic experimental study on indium implantation in silicon over a large range of implant energies and doses was performed. The evolution of the implant damage following thermal annealing was observed. A critical issue concerning In is represented by its outdiffusion, taking place during the thermal processes, that is a

limiting factor to get In peak concentration needed for applications in microelectronics. Then the use of different kinds of thermal processes has been evaluated, with particular attention to achieve a reduction of the outdiffusion and an increase of the electrical activation of In in silicon. The role of C, present in the silicon substrate as a contaminant or as a co-implanted species, on the electrical activation and diffusion of In in silicon was also investigated. In order to explain the peculiar electrical behaviour of In, arising from the presence of C, a model based on the formation of Ins-Cs complexes due to the interaction between In and C atoms present in the silicon matrix, was implemented into the simulation software FLOOPS and used to simulate the experimental results. This model, considering the reaction between In, C, interstitials and vacancies, based on the energetics obtained from first-principle calculations, allows to succesfully reproduce both the diffusion and the electrical activation of In in Si.

C8.8
Multiple Implantations - Experiments and Computer Simulations. Matthias Posselt, Michael Maeder, Andrei Lebedev and Rainer Groetzschel; Institute of Ion Beam Physics and Materials Research, Forschungszentrum Rossendorf, Dresden, Germany.

Advanced technologies use successive implantations of p- and/or n-dopants without any intermediate annealing steps. A characteristic example is the engineering of the regions of source, drain, extension and halo. The sequence of the implantations may influence the final distribution of dopants and radiation damage. In particular it affects the as-implanted distribution of dopants if in one or more implantation steps the direction of ion incidence is close to a major crystallographic axis of the silicon substrate. For example, extension implantations are often performed perpendicularly to the wafer surface, i.e. nearly parallel to the [100] axis. The defect production in previous implantations influences the shape of dopant and damage profiles in a subsequent channeling implantation step, since these defects may lead to increased dechanneling. Furthermore, the amorphization dose in a certain implantation step may be affected by the level of radiation damage formed during the previous steps. The present work deals with the simple example of two consecutive implantations in order to demonstrate the effects mentioned above. Two implantation sequences are investigated: (i) 35 keV B followed by 50 keV As into the [100] channel direction, (ii) 50 keV As followed by 35 keV B [100] channeling implantation. The depth profiles of B and As are measured by SIMS. The as-implanted damage is determined by RBS/C. The experimental data can be reproduced by atomistic computer simulations using the Crystal-TRIM code with an improved phenomenological model for damage buildup during multiple implantations. The present results contribute to a better understanding of ion-beam-induced defect formation and to progress in TCAD.

C8.9
Simulation of BF2 ion implantation into crystalline silicon: Influence of fluorine on boron activation.
Lilya Ihaddadene-Le Coq, Jerome Marcon and Kaouther Ketata; Laboratory of Electronics Microtechnology and Instrumentation (LEMI)-University of Rouen, Mont Saint Aignan, France.

We have investigated and modeled the diffusion of boron implanted into crystalline silicon in the form of boron difluoride BF2+. Secondary ion mass spectrometry (SIMS) has been used to measure dopant profiles in ion implanted samples with ion energy of 500 eV (i.e 1e15 cm-2, 2 KeV BF2+ implantation. RTA was carried out at 950°C, 1000°C, 1050°C and 1100°C for 10s, 20s, 30s and 60s). During ion implantation, fluorine is introduced into silicon either by BF2+ ion implantation or by boron and fluorine co-implantation. BF2+ is traditionally one of the favored ion species used for p-type shallow and ultra-shallow junction formation due to its amophization ability and small projected ranges compared to boron at the same implant energy. Recently, it has been shown, that the addition of fluorine through introducing more damage in silicon is an effective way to reduce the number of silicon interstitials causing boron transient enhanced diffusion (TED) and enhancing boron activation. Several experimental and theoretical investigations on the diffusion of fluorine and its effects on boron diffusion and activation have been published in the literature. In a recent work, we have investigated the diffusion of ultra-low energy boron implanted in crystalline silicon and tested a complete simulation program which takes into account the effect of the silicon boride layer as a source of self-interstitials. However our last model was still to be improved for simulating the deeply channeled fluorine tails. We have developed an accurate model based on the last one and on the effect of fluorine on the boron activation and diffusion. The simulations are consistent with most of experimental conditions.

C8.10
A simple model for boron segregation to Rp defects. Na An and Jianxin Xia; School of Microelectronics and Solid-State Electronics, University of Electronic Science and Technology of China, Chengdu, Sichuan, China.

Boron exhibits anomalous diffusion during the initial phases of ion implant annealing. Boron transient enhanced diffusion (TED) is characterized by enhanced tail diffusion coupled with an immobile peak. Though the peak concentration is lower than the boron solubility in silicon, the immobile boron peak is electrically inactive. A simple model of boron segregation to Rp (the projected range) defects has been developed to explain this phenomenon. The immobile peak is due to the segregation of boron to Rp defects which arise upon annealing. The driving force of boron segregation is the difference of potential energy between boron atoms in the matrix and those at the periphery of Rp defects. After implantation, there is a net excess of interstitials with dose equal to the implanted dose and distribution mimicking the implanted ion distribution, and these interstitials coalesce into Rp defects. The evolution of Rp defects is closely related to the evolution of immobile boron peaks. Rp defects are assumed to decrease exponentially with time. A segregation energy of 0.57 eV was used as a parameter in this model. The enhanced diffusivity and duration in TED are calculated from an interstitial clustering model. A comparison between experimental and simulated boron profiles is shown for samples annealed at 800 °C in nitrogen ambient for different times and implanted with dose of 2×10^{14} cm^{-2} at 15 keV and 30 keV, respectively. The satisfactory agreement between experimental profiles and simulations confirms the immobile part of implanted boron during annealing originates from boron segregation to Rp defects.

C8.11
Concentration Dependence of Boron Interstitial Cluster Formation in Silicon-On-Insulator (SOI).
Antonio Fernando Saavedra[1], Kevin S Jones[1], Ljubo Radic[2], Mark E Law[2] and Kevin K Chan[3]; [1]Materials Science and Engineering, University of Florida, Gainesville, Florida; [2]Electrical and Computer Engineering, University of Florida, Gainesville, Florida; [3]IBM Semiconductor Research and Development Center, IBM, Yorktown Heights, New York.

It has been shown recently that significant differences in boron activation exist between silicon-on-insulator (SOI) and bulk Si. This investigation set out to understand the effect of boron concentration on electrical activation in SOI materials. SIMOX and SOITEC wafers having surface Si thickness of 75 nm and 145 nm were implanted with 11B at 5.5 keV. The dose of the implant was varied from 3x10Î14 cm-2 to 1x10Î15 cm-2 to provide different boron concentrations within the clustering regime. Inert ambient anneals were performed for various times at temperatures ranging from 750C to 1000C to investigate the kinetics of the boron interstitial cluster (BIC) process in SOI. Hall effect was used to measure the fraction of active boron within the surface Si layer. A significant reduction in the active fraction of boron in SOI was observed and depended slightly on the boron concentration. However, increasing the dose loss of boron to the buried oxide (BOX) actually enhanced the active fraction of boron for thin SOI. This is attributed to a loss of boron interstitial clusters for thin SOI. However, the maximum active fraction of boron in thin SOI is limited by dose loss due to the implant, as well as segregation into the BOX. Thus, there appears to be a tradeoff between dose loss of boron to the BOX and maximum activation obtained in SOI. Prospects for modeling of dopant activation in SOI will also be presented.

C8.12
The Role of Stress in Dopant Activation, Solid Phase Epitaxy Regrowth, and Defect Evolution. Michelle Shirly Ann Phen and Kevin Jones; University of Florida, Gainesville, Florida.

During silicon integrated circuit fabrication, wafers undergo internal stresses. The effect of these stresses on the doping process is of critical interest. This study investigates the role of stress on dopant activation, solid phase epitaxial regrowth, and defect evolution. Ultra-thin 50μm 100mm <100> silicon wafers were amorphized with 1E15 atoms/cm3 of Ge+ at energy of 30 keV. Amorphization was followed by the implantation of 2 keV B+ at a dose of 1E15 atoms/cm3 or 2E14 atoms/cm3. A known stress of 170MPa was applied to the wafers by bending them at a controlled radius of curvature so that the amorphous layer is in tension or compression. The bent wafers were then annealed at temperatures between 550-750øC to determine solid phase epitaxial regrowth rate. Active dopant concentrations are obtained through the use of Hall Effect measurements. Cross-sectional and plan-view TEM samples were utilized to examine defect formation and evolution. Preliminary data shows that regrowth rate was highest when no stress is applied. Wafers strained in tension appeared to have higher regrowth rates compared to those strained in compression. These results are inconsistent with those that were previously reported, therefore, further investigation is needed to confirm them. Hall results indicate that the solid phase regrowth at 620øC of the boron implanted layer activates about 45%

of the 1x1015 dose independent of the sign of the stress. Additional results on the role of stress on defect evolution will be presented.

C8.13
High Concentration Fluorine: Experiments and Models.
Robert Russell Robison[1], Mark E Law[1] and Antonio F Saavedra[2]; [1]Electrical and Computer Engineering, University of Florida, Gainesville, Florida; [2]Materials Science and Engineering, University of Florida, Gainesville, Florida.

Previously, we developed a lower concentration (sub-amorphizing dose) fluorine model, showing the abnormal diffusion of fluorine and its time-dependency. However, other results have indicated that annealing behavior of samples amorphized with fluorine as well as Si pre-amorphized samples implanted with fluorine is distinct from the behavior in crystalline silicon. We have completed new experimental work examining high concentration (amorphizing dose) fluorine and extended our model to explain the behavior. This model continues to fit our previous experimental work. Boron doped FZ silicon wafers of 80-200Ohm-cm were first pre-amorphized with dual implants of 150keV and 40keV 1x10$\hat{1}$5/cm$\hat{2}$ Si to create a continuous 2800A deep amorphous region. Samples were subsequently implanted with the fluorine conditions of 16keV at 2x10$\hat{1}$5/cm$\hat{2}$ or 8x10$\hat{1}$5/cm2 dose, or 30keV at 2x10$\hat{1}$4/cm2 dose. Samples were annealed by either conventional furnace or RTA with an N2 ambient for various times at temperatures of 550-750C. SIMS was used for depth profiling, and TEM images were also taken of the samples to check for defects. The high-concentration model was based on our existing model for fluorine diffusion, using the same base equations and binding energies. The model was extended to include Si-Fx complex equations with binding energies based on published chemical data and other experiments. Additionally, a {311}/loop model was incorporated into the simulations to account for the damage accumulation, interstitial trapping, and time-dependent release at the end of range. The model obtains good qualitative agreement with the experiments. Tail motion, peak concentration, and time dependency are modeled well in the 2x10$\hat{1}$5/cm$\hat{2}$ simulations at 550 and 750C. The "flat top threshold", an observed phenomena in which the profile after annealing shows a flattened peak at 10$\hat{2}$0 concentration, is in reasonable agreement with the model in both cases. The 2x10$\hat{(}$14)/cm$\hat{2}$ 650C sample shows negligible motion after the anneal, a behavior that is distinct from the result in crystalline silicon, is also well modeled. A re-simulation of our previous crystalline results shows that the model both well describes the difference in behavior, and is still compatible with previous results. The 8x10$\hat{1}$5/cm$\hat{2}$ 750C results show some clustering effect which is not accounted for by the current model, but is being further investigated

C8.14
Modeling B cluster dissolution in Si and $Si_{0.8}Ge_{0.2}$.
Ljubo Radic[1], Aaron Lilak[3], Robert Crosby[2] and Mark Edward Law[1]; [1]Department of Electrical and Computer Engineering, University of Florida, Gainesville, Florida; [2]Department of Materials Science and Engineering, University of Florida, Gainesville, Florida; [3]TCAD Department, Intel Corporation, Hillsboro, Oregon.

Diffusion behavior of B in silicon can be affected by transient phenomena, such as the transient enhanced diffusion (TED) or formation of the boron-interstitial clusters (BIC). An experiment is performed to investigate the dissolution properties of BICs. Initially, B implanted Si samples are annealed at 750 ^{o}C for 30 minutes. During this anneal, the BICs form and deactivate the large part of implanted B dose, thus providing the clustered condition. The samples are then subjected to the reactivation anneal at 850 ^{o}C for times up to 60 minutes, in an oxidizing or inert ambient. Hall-van der Pauw measurement of the B active dose shows lower activation in the oxidizing vs. inert ambient anneals. This implies an interstitial release reaction is required to dissolve a significant cluster specie, since the oxidation of silicon is known to inject interstitials. Such a behavior is not predicted by the interstitial poor BICs (e.g. B_4I, B_3I) as the dominant clusters, which are used in the current models. Also, the reactivation time dependence indicates the reactivation is the result of the dissolution of more than one cluster. The initial increase in activation at short times (less than 10 minutes) is observed irrespective of the annealing ambient, while reactivation at longer times depends strongly on the ambient. Recent ab-initio calculations provide a qualitatively different B clustering model, with two significant cluster species. Dissolution of B_2I_3 accounts for the short term reactivation and is insensitive to the ambient. On the other hand, B_4I_4 dissolution is affected by interstitial injection from the surface, providing the ambient sensitive reactivation at longer times. Based on these energetics, with B_2I_3 and B_4I_4 as the two significant cluster species, we have developed a new physically based model that for the first time accounts for the experimentally observed cluster dissolution time and ambient dependence. The model is also tested on an experimental characterization of B clustering in relaxed $Si_{0.8}Ge_{0.2}$. The B well structures are grown by molecular beam epitaxy (MBE) with concentrations of $7.5x10^{18}$, $1.5x10^{19}$ and $5.0x10^{19}$ cm^{-3}, from surface to 0.25um depth. The samples are implanted with Si dose of $1.0x10^{14}$ cm^{-2} at 60 keV. Activation is monitored via Hall-van der Pauw measurement, while the buried B marker layer provides information on interstitial supersaturation.

C8.15
The effect of varying fluorine implantation energy on boron diffusion in SiGe. Huda El Mubarek, Janet Bonar and Peter Ashburn; Electronics and Computer Science, University of Southampton, Southampton, United Kingdom.

Recently, fluorine implantation to suppress boron transient enhanced diffusion in silicon has been of great interest in the literature. However, to date there have been no reports of the effects of fluorine on boron diffusion in SiGe. Boron marker layers in SiGe (14% Ge) were grown by Low Pressure Chemical Vapour Deposition (LPCVD) on (100) silicon wafers. Transient enhanced boron diffusion as well as thermal boron diffusion were separately studied by characterising the boron diffusion in samples of the same wafer with and without a 288keV, 6x1013cm-2 P+ implant. The effect of varying the fluorine implantation energy was studied by using two different F+ implants. Samples were either implanted with a 36keV, 9x1014cm-2 F+ implant, which coincides with the peak of the boron in the marker layer, or with a 185keV, 2.3x1015cm-2 F+ implant, which coincides with the peak of the P+ implant. The samples were then annealed in nitrogen by Rapid Thermal Anneal (RTA) at either 950C or 1025C for 30s. Boron (B11), germanium (Ge 74) and fluorine (F19) concentration depth profiles were obtained on all samples by Secondary Ion Mass Spectroscopy (SIMS). The fluorine implantation completely suppressed boron transient enhanced diffusion and significantly reduced boron thermal diffusion in silicon germanium. A greater reduction in boron thermal diffusion was obtained for the high energy (185keV) F+ implant (63%) compared with the low energy (36keV) F+ implant (43%) at the high anneal temperature 1025C. A greater reduction in boron thermal diffusion due to the high energy (185keV) F+ implant (79%) was obtained at the lower anneal temperature (950C) compared with (63%) at the higher anneal temperature (1025C). The annealed fluorine profiles showed an interesting fluorine peak within the SiGe layer coinciding with the boron marker layer. It is proposed that this peak is responsible for the suppression in boron diffusion.

C8.16
Abstract Withdrawn

C8.17
Two-Dimensional Junction Profiling on Integrate Circuit Devices by Scanning Electron Microscopy. Wen-Chu Hsiao[1], Chuan-Pu Liu[2], Luen-Chian Sun[1] and Ying-Lang Wang[2]; [1]Department of Materials Science and Engineering, National Cheng-Kung University, Tainan, Taiwan; [2]Taiwan Semiconductor Manufacturing Company, Tainan, Taiwan.

Secondary electron (SE) imaging in a scanning electron microscopy (SEM) is used to map out the dopant profiles of metal-oxide-semiconductor (MOS) structures. SE imaging of dopant profiles in a SEM exhibits strong bright and dark contrast for p- and n-type regions, respectively. With reducing the size of the integrated curcuit (IC) devices, the doping concentration in the source and drain would not be easily determined by other techniques such as secondary ion mass spectroscope, etc. However, the Dopant contrast on SE images can be used to measure the active dopant concentration and distribution. In this paper, two types of MOSFET are characterized including a 0.35-μm-long gate (NMOS) and a 0.3-μm-long gate (PMOS). The digital SE images were acquired where the area from the doped regions of interest is flesh. Digital image processing allows us to measure the contrast quantitatively for the MOS devices. The contrast between the bright p-type areas and the dark n-type areas was maximized at the accelerating voltage of 1 kV with a through-lens SE detector. Dopant contrast can be enhanced by various surface treatments as well as an applied bias across $p-n$ junctions *insitu* in the SEM. We compare the vertical and lateral distribution of the dopant regions by selective chemical etching in a mixture solution containing HF, CH_3COOH and NH_4F from the dopant contrast. The mechanisms for the enhanced contrast are discussed in the paper as well.

C8.18
Vibrational Spectra of Nitrogen-Oxygen Defects in Nitrogen Doped Silicon Using Density Functional Theory.
Faouzia Sahtout Karoui, Abdennaceur Karoui and George A. Rozgonyi; Materials Science and Engineering, North Carolina State University, Raleigh, North Carolina.

The vibrational spectra of nitrogen-oxygen complexes in nitrogen doped Czochralski silicon (N-CZ Si) has been investigated using

quantum mechanics density functional theory (DFT) calculations. After relaxation, the local vibration modes (LVM) were determined within the harmonic oscillator approximation. Calculations have been performed for N2, VN2 and V2N2 (V: Si vacancy), and N2On, VN2On and V2N2On with a single or two oxygen atoms (n=1,2) bridging the Si-Si dilated bond next to the N-N core. We found that N2 in split position has two infrared active LVMs, 779 and 986 cm-1, matching 771 and 967 cm-1 FTIR frequencies used to measure [N] in N-CZ Si [1]. Even though not so stable, VN2 has one line 781 cm-1 falling around observed 771 cm-1 frequency. The calculated LVMs for V2N2, 615, 627, 638 cm-1, does not match any of the measured FTIR lines. Nevertheless, V2N2O and V2N2O2 have one frequency 819 cm-1 and 810 cm-1 respectively, close the measured 815 and 806 cm-1 frequencies. This finding corroborates our previous work in which we suggested that V2N2 is a nucleation center for oxygen precipitates [2]. The N2O complex exhibits three infrared active LVMs with frequencies 814, 1003 and 1029 cm-1. These frequencies match very well the observed 815, 1000 and 1031 cm-1 lines [3]. By adding one O atom, these lines are shifted to 825, 945 and 1019 cm-1. Therefore, the observed 1021 cm-1 frequency [3] is likely due to N2O2 complexes. VN2On defects have two infrared active frequencies, 797 and 820 cm-1 matching 806 and 815 cm-1 lines. Nevertheless, because VN2On complexes are not stable [2], they don't contribute to the measured N-O lines in the as-grown material. In summary, calculated LVMs for N2, N2O and N2O2 provide the best matching with N-pairs and N-O FTIR measured frequencies. The measured 806 and 815 cm-1 absorption lines might be also a signature for V2N2On complexes. Emphasize through this work is on including N-O FTIR 806, 815, 1000, 1021, 1031 cm-1 lines while measuring [N] in N-CZ Si in addition to 771 and 967 cm-1 lines. References [1]: H.J.Stein, Mat. Res. Soc. Symp. Proc., Vol. 59, p.523 (1986). [2]: F. Sahtout Karoui,A. Karoui, G. A. Rozgonyi, M. Hourai and K. Sueoka, Solid State Phenomena, 95-96, 99 (2004). [3]:P. Wagner, R. Oeder, W. Zulehner, Appl. Phys. A, 46, 73-76 (1988).

C8.19
Atomistic Modeling of Impurity Atmospheres in Silicon and Dislocation Locking Effects. Abdennaceur Karoui, Materials Science and Engineering, North Carolina State University, Raleigh, North Carolina.

A theoretical study of edge dislocation locking by impurities in silicon is presented. Three atom groups have been considered: (i) light O, N, and C, (ii) large Ga, Ge, and As, and (iii) small dopant atoms B, Al, and P. The binding energy of a dislocation with its impurity atmosphere and the shear stress capable of separating a dislocation from its atmosphere were calculated based on an impurity size effect model, for which we had to calculate the dislocation self-energy. Molecular Dynamics on a large atomic system (H terminated axisymmetric rod of 34552 Si atoms with an edge dislocation along its axis) provided a self energy of 156 meV/A for a clean edge dislocation. Calculated binding energy and separation shear stress showed that the three impurity groups exhibited dissimilar effects of dislocation locking. The O, N, and C radial distributions are similar with a slightly stronger occupancy probability for O and N in the vicinity of the dislocation core. These impurities locate themselves at the core of edge dislocation to which they strongly bind. At a local fraction of 1E-4, O, N, or C atoms spread over a cylinder whose radius is about 7 neighbors about the dislocation line. The penta-ring and the upper hexa-ring, both in the compressive part of the dislocation domain, are the most likely zones for O localization; whereas the septa-ring, which is in the dilation side of the dislocation, repels O atoms. Likewise N and C in tetrahedral interstitial positions locate themselves in the compressive side of the dislocation. It was found that carbon is distributed in a more diffuse way than nitrogen and oxygen. From the second group, Ge is rarely gettered by edge dislocation since it has a very small chance to reach the dislocation core. Besides, Ge atmosphere can withstand only 1/3 of the separation stress that the first group can sustain. From the third group, P atoms are not trapped by edge dislocation. Phosphor weak atmosphere has no shear stress resistance to dislocation separation. The temperature dependency of impurity concentration around an edge dislocation was found to have an Arrehnius behavior. As can be seen in Table I, at local atomic fraction of 1E-4, the impurity binding energy with an edge dislocation varies from 0.008 eV/A for P to 1.7 eV/A for N and 1. 8 eV/A for O atoms. Table I: Edge dislocation-impurity binding energy in silicon, for an atomic fraction of 1E-4.

C8.20
Abstract Withdrawn

C8.21
Theory of Native Defect-Assisted Diffusion of Acceptors in Silicon. Giorgia M. Lopez[1], Claudio Melis[1], Paolo Schirra[1], Paola Alippi[2] and Vincenzo Fiorentini[1]; [1]INFM and Dept. of Physics, University of Cagliari, Monserrato, Italy; [2]IMM, CNR, Catania.

We present a complete picture of acceptor diffusion in silicon, based on ab initio density-functional-based calculations on the structure, extrinsic levels, formation and migration energies of the B, Al, Ga, and In acceptors in crystalline Si, and of their complexes with vacancies and self-interstitials. Complexes are known to be responsible for the transient enhancement of dopant diffusivity in implanted Si, a key issue in the formation of ultrashallow junctions in Si-based CMOS integrated circuit technology. We find self-interstitial assisted diffusion to be preferred over vacancy assisted mechanisms in all cases, although the two become competitive as the acceptor increases in size. The ground state of the complexes is unexpected and "anomalous" in several cases: Al and In coupled to a vacancy go off-site forming a divacancy-interstitial complex; the standard self-interstitial/substitutional acceptor complex predicted for B and In is unstable for Al and Ga, which are ejected in the interstitial region and are electrically deactivated as acceptors.

SESSION C9/B9: Joint Session: SiGe Layers
Chair: Wolfgang Windl
Thursday Morning, April 15, 2004
Room 2004 (Moscone West)

8:30 AM *C9.1/B9.1
Current Understanding of Diffusion in Strained Si and SiGe. Nicholas Edward Cowern, Advanced Technology Institute, University of Surrey, Guildford, Surrey, United Kingdom.

The introduction of novel device features such as metal gates and bandgap-engineered channels into upcoming CMOS generations has placed the subject of strained Si and SiGe at the top of the materials agenda for silicon-based technology. A key problem in this field is the diffusion and segregation behaviour of host and impurity atoms in the strained material. Much work has been done in the last decade but the subject remains controversial despite fundamental analyses of the role of strain in diffusion from the points of view of thermodynamics, transition state theory and atomistic calculations, and in spite of very extensive experimental investigations. As yet it seems fair to say that there is still no firmly established understanding of stress/strain effects on diffusion. The talk will review recent progress in understanding, emphasizing the key role played by strain fields that intersect surfaces and interfaces where point defects are generated. A new theoretical framework that takes explicit account of surface strain will be outlined, and its consequences for point defects, diffusion and mass transport in non-uniformly strained structures will be considered and compared with the available experimental evidence. Part of this work was performed within the CEC projects IST/2001-34404 ARTEMIS and IST/2000-30129 FRENDTECH.

9:00 AM C9.2/B9.2
Impact of Buffered Layer Growth Conditions on Grown-In Vacancy Concentrations in MBE SiGe. Kareem M. Shoukri[1], Yaser M. Haddara[1], Andrew P. Knights[2], Paul G. Coleman[3] and Mohammad M. Rahman[4]; [1]Electrical and Computer Engineering, McMaster University, Hamilton, Ontario, Canada; [2]Engineering Physics, McMaster University, Hamilton, Ontario, Canada; [3]Physics, University of Bath, Bath, BA2 7AY, United Kingdom; [4]Electrical and Electronic Engineering, Toyama University, 3190-Gofuka, Toyama 930-8555, Japan.

Silicon-Germanium has become increasingly attractive to semiconductor manufacturers over the last decade for use in high performance devices. In order to produce thin layers of device grade SiGe with low concentrations of point defects and well-controlled doping profiles, advanced growth and deposition techniques such as molecular beam epitaxy (MBE) are used. One of the key issues in modeling dopant diffusion during subsequent processing is the concentration of grown-in point defects. There is evidence that under certain growth conditions (e.g. growth at temperatures below 350°C) a supersaturation of vacancies is grown-in. Using positron annihilation spectroscopy (PAS), we have observed the incorporation of vacancy clusters and vacancy point defects in 200nm SiGe/Si layers grown by MBE over different buffer layers. Variables included the type of buffer layer, the growth temperature and growth rate for the buffer, and the growth temperature and growth rate for the top layer. Different growth conditions resulted in different relaxation amounts in the top layer, but in all samples the dislocation density was below 10^6 cm^{-2}. Preliminary results indicate a correlation between the size and concentration of the vacancy defect clusters and the percentage relaxation in the alloy layer. At low relaxation percentages of <50% the vacancy point defect concentration is below the PAS detectable limit of approximately $1x10^{-15}$ cm^{-3}. As the relaxation is increased to a maximum value of 93%, small vacancy clusters are observed in the SiGe film.

9:15 AM C9.3/B9.3

Arsenic diffusion in Si and $Si_{1-x}Ge_x$ alloys. Suresh Uppal[1], Janet M. Bonar[2], Arthur F. W. Willoughby[1] and Jing Zhang[3]; [1]Materials Research Group, University of Southampton, Southampton, Hampshire, United Kingdom; [2]Department of Electronics and Computer Science, University of Southampton, Southampton, Hampshire, United Kingdom; [3]Department of Electrical Enginering, Imperial College, London, United Kingdom.

Results of As diffusion in Si and Si-Ge (10 —*pthou*—Ge) are presented. Using molecular beam epitaxy (MBE), *insitu* arsenic delta doped epitaxial Si and compressively strained and relaxed Si-Ge layers were grown on Si substrates. The as-grown and annealed profiles were measured using secondary ion mass spectroscopy after rapid thermal annealing (RTA). Arsenic diffusion is clearly enhanced in Si-Ge as compared to Si and the enhancement factor is recorded to be $\cong$2 for 10—*pthou*— Ge content. The calculated diffusion coefficient agree well with literature values for both Si and Si-Ge. Using RTA in O_2 atmosphere, interstitial and vacancies have been injected in the sample structures at 1000°C. Diffusion enhancement with vacancy as well as interstitial injections as compared to an inert anneal is recorded in Si and Si-Ge structures. The results suggest that both interstitial and vacancy defects contribute to arsenic diffusion in Si and Si-Ge(10—*pthou*— Ge).

9:30 AM C9.4/B9.4

Modeling dopants diffusion in SiGe and SiGeC alloys. ardechir pakfar[1,2], Alain Poncet[2], Thierry Schwartzmann[1] and Herve Jaouen[1]; [1]TPS & QA - TM, STMicroelectronics, CROLLES, France; [2]LPM, INSA de Lyon, Villeurbanne, F-69621, France.

In this work, a unified physical model of dopants diffusion in SiGe and SiGeC alloys is proposed, based on the hypothesis that the different effects introduced by Germanium and Carbon incorporation in Silicon matrix modify the equilibrium concentrations of interstitials and vacancies from their standard value in pure Silicon. The primordial role of point defects in dopant diffusion is admitted and the evolution of substitutionnal atoms diffusivity is described by their concentration variation. The critical analysis of bibliographic studies allows the description of involved physical phenomena: the chemical effect in covalent alloys, the effect of strain and the Fermi-level effect, act on point defects concentration and thus, on impurity diffusion. This formulation is completed by the equations expressing the B-Ge coupling and the influence of Carbon supersaturation, to form a unified phenomenological model valid to describe the diffusivity evolution of usual dopants in SiGe and SiGeC strained and relaxed alloys. All reliable and previously published experimental data is analyzed for the calibration of the model physical parameters. Finally, the equilibrium diffusion of Boron in shallow epitaxial SiGe and SiGeC layers is measured and successfully confronted to the unified diffusion model. For the first time, experimental studies of Arsenic equilibrium diffusion are performed, showing an important diffusivity enhancement with Ge and C content of SiGeC strained layers, confirming model predictions for the Vacancy-mediated diffusion.

9:45 AM C9.5/B9.5

Athermal Ge−migration during junction formation in s-Si layers grown on SiGe-buffers. Wilfried Vandervorst[1], bartek pawlak[2], richard lindsay[1], romain delhougne[1], matty caymax[1] and bert brijs[1]; [1]mca, imec, leuven, Belgium; [2]philips research leuven, leuven, Belgium.

Solid phase epitaxial regrowth (SPER) has been proven to be highly advantageous for ultra shallow junction formation in advanced technologies. Application of SPER to strained Si/SiGe structures raises the concern that the Ge may outdiffuse during the implantation and/or anneal step and thus reduce the strain in the silicon. In the present studies we expose the 8nm strained silicon wafers to implant conditions that are characteristic for formation of the junctions by solid phase epitaxial regrowth (SPER) and conventional spike activation and measure the resulting Ge-redistribution using SIMS. We have studied the dose and energy dependence of this athermal redistribution process by using As implants (2−15 keV, 5 e14 −3e15 at/cm2) such that the location of the implants species relative to the Ge-edge could be determined by Sims as well. It is shown that the energy of the implant species or more specifically the position of the damage distribution function relative to the Ge-edge (as deduced from RBS-channeling measurements) plays a determining factor with respect to the Ge-migration. For implants whereby the damage distribution overlaps with the Ge-edge a very efficient transport of the Ge is observed, even prior to any anneal cycle. The migration is entirely correlated with the collision cascade and the resulting (forward!) Ge-recoil distribution as demonstrated by Monte Carlo simulations using SRIM. The scaling with dose for a given energy links the observed Ge-profile with a broadening mechanism related to the number of atom displacements induced in the sample. The Ge-redistribution originating from additional anneals after the implant step (or even before the implant) was also studied and is shown to be far less important as compared to the collisional mixing effects. The latter clearly supports the concept an athermal Ge-migration caused by the amorphizing implant. The observed redistribution implies that the use of the SPER process for junction formation in s-Si/SiGe inevitably leads to a strong Ge-redistribution and a corresponding loss off strain in the Si-layer.. A careful engineering of the amorphization process (such as using low dose multiple energy implants) may be required to limit the migration process.

10:00 AM C9.6/B9.6

The Role of Preamorphization and Activation for Ultra Shallow Junction Formation on Strained Si Layers Grown on SiGe Buffer. Bartlomiej J. Pawlak[1], Wilfried Vandervorst[2], Richard Lindsay[2], Indgrid De Wolf[2], Fred Roozeboom[3], Romain Delhougne[2], Alessandro Benedetti[2], Roger Loo[2], Matty Caymax[2] and Karen Maex[2]; [1]Philips Research Leuven, Leuven, Belgium; [2]IMEC, Leuven, Belgium; [3]Philips Research Labs, Eindhoven, Netherlands.

The junctions formed on strained silicon/SiGe buffers need to satisfy one additional requirement, their activation related thermal budget should not relax the strain in the channel. We investigated the role of preamorphization, doping and thermal budget separately for the junction and the channel region. In the present study we exposed the 8 nm strained silicon wafers to the conditions that are characteristic for formation of the junctions by solid phase epitaxial regrowth (SPER) and conventional spike activation. We investigated by Raman spectroscopy the stress relaxation influenced by annealing at temperatures between 550C and 1000C for 1 minute and up to 1070C spike activation. We amorphized the wafers by germanium or arsenic implantation in such a way that the amorphous layer interface is placed within the strain silicon layer or beyond in the SiGe buffer. The secondary ion mass spectroscopy (SIMS) of as-implanted junctions shows significant germanium migration towards the surface. After 1070C spike activation for the deep positioning of the a-Si/c-Si interface we observe additional redistribution of germanium towards the surface. The effect is substantially smaller in the shallow amorphized or non-amorphized samples. Raman spectroscopy analysis revealed that amorphization by germanium or arsenic relaxes the strain silicon. If the wafer is not amorphized the standard thermal budget used for solid phase epitaxial regrowth, 650C for 1 minute does not relax the silicon layer. We observed an improved dopant activation in s-Si/SiGe material of p-type junctions formed both by SPER (Ge + B) annealed at 650C for 1 minute and by spike activation (Ge + F + B) at 1070C. For the boron doped junctions activated by SPER we recognized the same silicon interstitial driven deactivation mechanism as in bulk material. For the n-type junctions doped by phosphorus and arsenic we have concluded improved activation by SPER in s-Si/SiGe material in comparison to bulk Si. Spike activation at 1070C of arsenic doped samples offers worse trade-off between junction depth and sheet resistance than in bulk material. In summary we conclude that the thermal budget used for junction formation still preserves the strain in the non-implanted channel region. For any amorphisation conditions a substantial germanium migration to the surface is observed. The strain in the junctions is relaxed due to implantation defects.

SESSION C10: Amorphous Silicon and Solid-Phase Epitaxy
Chair: Bill Taylor
Thursday Morning, April 15, 2004
Room 2002 (Moscone West)

10:45 AM C10.1

Atomistic Modeling of Ion Beam Induced Defects in Si: From Point Defects to Continuous Amorphous Layers. Lourdes Pelaz, Luis A. Marques, Ivan Santos, Maria Aboy and Juan Barbolla; University of Valladolid, Valladolid, Spain.

Amorphization occurs during the fabrication of Si devices due to the use of high dose implants. Also preamorphizing implants are carried out to reduce channeling and to achieve improved electrical activation of dopants during the regrowth. Therefore, it is essential to develop ion induced amorphization models, compatible with process simulators, which are able to capture the features of the crystal-amorphous transition and the solid phase epitaxial regrowth during the anneal. In this work we combine the fundamental understanding of damage evolution provided by molecular dynamics simulations, with the extended time and space scales provided by Kinetic Monte Carlo codes. The elementary units used to reproduce the defective zones are Si interstitials, vacancies and the IV pair, which is a local distortion of the Si lattice without any excess or deficit of atoms. More complex defect structures can be formed as these elementary units cluster. The amorphous pockets are treated as

agglomerates of IV pairs, whose recrystallization rate depends on the local density of these defects. The local excess or deficit of atoms in the amorphous regions experiences some rearrangement as recrystallization takes place. In sub-amorphizing implants amorphous pockets are disconnected and when they recombine, they leave behind the local excess of Si interstitials and vacancies. When a continuous amorphous layer initially extends to the surface, the excess or deficit atoms are swept towards the surface during the regrowth. Our atomistic model describes the main features of the crystalline to amorphous transition and the defect evolution during the regrowth. The same consistent model and parameters are used for non-amorphizing and amorphizing implants, and amorphization is the result of the simulation itself.

11:00 AM C10.2
Dopant diffusion in amorphous silicon. Ray Duffy[1], Vincent Venezia[1], Anco Heringa[1], Marco Hopstaken[2], Geert Maas[2], Thuy Dao[2], Yde Tamminga[2] and Fred Roozeboom[3]; [1]Philips Research Leuven, 3001 Leuven, Belgium; [2]Philips CFT-Materials Analysis, 5656 AA Eindhoven, Netherlands; [3]Philips Research Laboratories, 5656 AA Eindhoven, Netherlands.

In recent years interest has increased significantly in preamorphization and low-temperature recrystallization techniques to produce highly steep ultrashallow junction profiles with above-equilibrium levels electrical activation. However, during solid phase epitaxial regrowth (SPER) complex physical phenomena occur that require careful consideration, such as dopant diffusion in the amorphous region and segregation at the moving amorphous-crystalline interface, as well as uphill diffusion after SPER is complete. In this work we investigate the diffusion of high-concentration ultrashallow B, F, P and As profiles in amorphous Si. Wafers were first preamorphized to a depth of 105 nm by Ge implantation. Then B, F, P, or As was implanted to a dose of 1×10^{15} cm^{-2} with energies of 0.5 keV, 1 keV, 1.5 keV, and 2 keV, respectively. Wafers were annealed in an inert N_2 ambient, for various times, in the 400 °C to 600 °C temperature range. Dopant profiles were analyzed by SIMS. RBS channeling measurements confirmed that the dopant profiles remained in amorphous Si for the entire duration of the anneals. Previous studies on H and transition metals have shown that they diffuse more slowly in amorphous Si than in crystalline Si. We demonstrate that B and F diffuse more quickly when in amorphous Si, during low-temperature thermal annealing. The diffusivities of As and P are less enhanced by being in amorphous Si. The entire F profile is highly mobile in the amorphous region, and significant out-diffusion from the surface is observed. In the case of B, diffusion occurs between the concentrations of approximately 2×10^{20} cm^{-3} and 3.5×10^{18} cm^{-3}, with little movement observed in the peak or tail of the profile. We have also established the time, temperature, and concentration dependence of B diffusion in amorphous Si. Recent experimental work on SPER of B-doped junctions has shown that the addition of F (1×10^{15} cm^{-2}, 6 keV) can be beneficial, producing superior sheet resistance versus junction depth performance. We demonstrate that B diffusivity in the amorphous region is similar with and without F. However, F dramatically slows down the recrystallization rate, allowing the B profile a longer time to experience diffusion in amorphous Si, with a diffusivity that is several orders of magnitude higher than the corresponding diffusivity in crystalline Si. The basis for using preamorphization and low-temperature SPER processing techniques is to activate dopants at high concentrations while minimizing diffusion. We demonstrate in this work that diffusion in amorphous Si during SPER is extremely significant, for B and F in particular, and must be considered to accurately optimize ultrashallow junction profiles. We have shown that the radically different behaviour of the four species studied here indicates that the mechanism of dopant diffusion in amorphous Si is complex and requires further understanding.

11:15 AM C10.3
Processes for Fluorine Enhanced Boron Diffusion in Amorphous Silicon. Jeannette M. Jacques[1], Kevin S. Jones[1], Mark E. Law[2], Lance S. Robertson[3], Daniel F. Downey[4], Leonard M. Rubin[5], Joe Bennett[6], Meredith Beebe[6] and Mikhail Klimov[7]; [1]Materials Science & Engineering, University of Florida, Gainesville, Florida; [2]Electrical & Computer Engineering, University of Florida, Gainesville, Florida; [3]Texas Instruments Inc., Dallas, Texas; [4]Varian Semiconductor Equipment Associates, Gloucester, Massachusetts; [5]Axcelis Technologies, Beverly, Massachusetts; [6]International SEMATECH, Austin, Texas; [7]AMPAC/MCF, University of Central Florida, Orlando, Florida.

In prior works, we demonstrated the phenomenon of fluorine enhanced boron diffusion within amorphous silicon. Present studies address the process dependencies of low temperature boron motion within ion implanted materials. Silicon wafers were preamorphized with either 70 keV Si or 80 keV Ge implants at a dose of $1x10^{15}$ atoms/cm^2. Subsequent 500 eV $1x10^{13}$ atoms/cm^2 and $1x10^{15}$ atoms/cm^2 ^{11}B implants, as well as F implants with energies ranging from 3 keV to 100 keV and doses from $5x10^{14}$ atoms/cm^2 to $5x10^{15}$ atoms/cm^2 were also done. Furnace anneals at both 475°C and 550°C were conducted for varying times under an inert N_2 ambient. Secondary Ion Mass Spectroscopy (SIMS) was utilized to characterize the occurrence of boron diffusion within amorphous silicon at both room temperature and during the solid phase epitaxial regrowth process. Enhanced motion at room temperature is isolated to the boron tail region, while diffusion during solid phase epitaxial regrowth is generally exhibited at boron concentrations above $1x10^{18}$ atoms/cm^3. Boron motion within as-implanted samples is observed at fluorine concentrations greater than $1x10^{20}$ atoms/cm^3. The magnitude of the boron motion scales with increasing fluorine concentration, such that a 6 keV F implant with a dose as low as $5x10^{14}$ atoms/cm^2 can induce motion. Maximum boron diffusion is exhibited when the projected range of the fluorine implant coincides with the tail region of the boron concentration profile. Retarded boron motion is observed at depths shallower than the tail region, while no increases in motion are demonstrated as the fluorine projected range moves deeper than the boron profile. Fluorine enhanced diffusion at room temperature does not appear to follow the same process as the enhanced diffusion observed during the regrowth process.

11:30 AM C10.4
The role of stress on the shape of the amorphous-crystalline interface and mask-edge defect formation in ion-implanted silicon. Carrie E Ross and Kevin S. Jones; Materials Science and Engineering, University of Florida, Gainesville, Florida.

Stress is known to affect the regrowth velocities during recrystallization of an amorphous layer. This study investigates how the stress from patterned structures alters regrowth and in turn affects defect formation. Prior to patterning, 80Å SiO_2 and 1540Å of silicon nitride were deposited on a 200 mm (100) silicon wafer. A 40keV Si^+ amorphizing implant at a dose of $1x10^{15}$ atoms/cm^2 was then performed into the patterned wafer. The regrowth of the amorphous layer along the mask edge was studied by partially recrystallizing the layer for various times at 550°C both with the mask present and after etching off the oxide and nitride pads. A significant number of cross-sectional Transmission Electron Microscopy (TEM) samples were prepared and imaged. It was found that the stress from the patterned structures enhances the vertical and lateral regrowth velocities by 19% and 13% respectively, as well as alters the shape of the amorphous-crystalline interface during regrowth. Previous studies have shown that uniaxial tensile stress increases the regrowth velocity. FLOOPS simulations have shown that the region of interest in these samples is under tensile stresses, suggesting that this type of stress should accelerate the regrowth velocity vertically. The enhancement in the lateral regrowth velocity was not expected. In addition for certain geometries dislocation half loops are observed to form along the mask edge. These defects arise during regrowth and are directly affected by the film stress. The relationship between the stress from the patterned structures, the regrowth of the amorphous layer, and the formation of dislocation half-loops along the mask edge will be discussed.

11:45 AM C10.5
Channel engineering and junction overlap issues for ultra-shallow junctions formed by SPER in 45 nm CMOS technology node. Simone Severi[1,2], Kirklen Henson[1], Richard Lindsay[1], Anne Lauwers[1], Bartek Pawlak[1,3], Radu Surdeanu[1,3] and Kristin De Meyer[1,2]; [1]SPDT/DIP, IMEC, Leuven, Belgium; [2]ESAT_INSYS, K.U.Leuven, Leuven, Belgium; [3]Philips-Research, affiliated to IMEC, Leuven, Belgium.

The necessity to control the Short Channel Effects (SCE) for the 45 nm technology node and beyond requires the complete suppression of dopant diffusion in order to control the lateral and vertical depth and the abruptness of the junction profile. It is known that junctions formed by Solid Phase Epitaxial Regrowth (SPER) of a doped amorphous region allow for meta-stable high activation level and perfectly abrupt profiles. The excellent abruptness of SPER junction results from a poor activation level in the crystalline Si below the amorphous region. Despite the excellent vertical junction profile, several integration issues rise from the lateral amorphisation and from the End of Range (EOR) defects. In the present work an experimental analysis of the lateral dopant and defect profile obtained by this low thermal budget process is presented through electrical pMOS and nMOS transistors characterization. We observe a strong dependence of the lateral amorphous region profile near the gate on the implantation parameters used. Unless optimized this leads to poor doping active concentration under the gate that significantly increases the overlap resistance. Through a SPER extension process only, species combinations of Ge, Ar, BF2 and B for PMOS, and Ge and As for NMOS have been characterized for transistor performance. Under the correct conditions, the transistor performance can be recovered if compared to the spike annealed reference. An optimised SPER junction can preserve the oxide integrity and avoid the degradation of the poly. The issue of HALO deactivation in the EOR region is

studied in detail through capacitance measurements and threshold voltage roll-off. It is shown that the degradation in the SCE control can be recovered for both NMOS and PMOS. For PMOS a far superior control on the short channel behaviour is observed with SPER junctions compared to the equivalent resistance spike annealed reference.

SESSION C11: Characterization Techniques
Chairs: Alain Claverie and Wilfried Vandervorst
Thursday Afternoon, April 15, 2004
Room 2002 (Moscone West)

1:30 PM *C11.1
Two-dimensional carrier profiling : quantitatively measuring invisible atoms with nanometer resolution.
Wilfried Vandervorst[1], Pierre eyben[1], duhayon natasja[1], marc fouchier[1] and david alvarez[1,2]; [1]mca, imec, leuven, Belgium; [2]infineon, munich, Germany.

Two-dimensional carrier profiling in semiconductors is one of the most demanding metrology tasks (presently still labeled red in the International Technology Roadmap for Semiconductors), as one needs to combine extreme spatial resolution (⟨ 1 nm), with very high concentration sensitivity (⟨ 5 %), a large dynamic range (5-6 orders of magnitude) and an excellent quantification accuracy (⟨ 3 %). Among the potential candidates (Scanning Capacitance microscopy, Electron Holograhy,..) for this application, Scanning Spreading Resistance Microscopy (SSRM) has evolved recently towards a performance level closely meeting the ITRS-targets. Recently a tip-technology has been developed based on molded solid diamond tips, which provide an optimum pyramidal tip shape and fine tip radius such that a drastically improved spatial resolution can be obtained. Based on dedicated spatial resolution test structures (sandwiched buried oxides, dopant spikes,..), it is shown that with these tips SSRM achieves a spatial resolution better than 1 nm. Dopant gradients as steep as 1-2 nm/dec have been measured as well. This excellent spatial resolution is combined with straightforward quantification and excellent sensitivity (over the entire dopant range) such that cross correlation with process simulators becomes feasible and details of the Vt-adjust and halo-implants and LDD/HDD-structure can be studied. Using this excellent spatial resolution analysis of emerging devices such as SOI-transistors and FinFET devices were performed. Excellent agreement between effective channel lengths as determined with SSRM versus electrical performance of SOI-devices could be demonstrated, allowing to predict based on the measured underdiffusion, that for that particular technology a 50 nm (physical gate length) transistor would be totally shortened. Effective channel lengths as small a 15 nm could easily be discerned. Recently we also have applied SSRM to (strained) Si/SiGe-based CMOS structures and were able to deduce the different diffusion characteristics in the Si and the SiGe-layers (whereby each of these had a very limited thickness , 5-10 nm). In this paper we will also make a comparison to SCM results (as obtained on the resolution test structures) and electron holography on CMOS-transistors.

2:00 PM C11.2
Lateral Dopant Profile Metrology using Carrier Illumination.
Edward Budiarto, Peter Borden, Susan Felch and Houda Graoui; Applied Materials, Santa Clara, California.

As CMOS device scaling continues into the sub-100nm regime, the precise control of source/drain extension (SDE) lateral diffusion and dopant profile overlap under the poly-silicon gate has become increasingly critical, directly impacting the transistor saturation drive current. The SDE gate overlap is typically achieved by dopant lateral diffusion during the rapid thermal annealing (RTA) process following the SDE implant. As device dimensions continue to shrink, it becomes necessary to produce <30nm vertical SDE junctions, which may require a diffusion-less dopant activation process such as laser annealing. Without lateral dopant diffusion, a high tilt-angle implantation may be employed to produce the desired amount of SDE gate overlap. Either approach requires a highly sensitive measurement technique capable of monitoring the SDE gate overlap during processing. This work describes the application of the Carrier Illumination (CI) technique to conduct such measurement. CI is a non-destructive optical interference technique for measuring the dopant profile depth of ultra-shallow junctions with <2 angstrom resolution. The CI signal from a patterned structure of doped and undoped lines is a linear superposition of individual signals from the fully doped and fully undoped regions, enabling determination of the line dimensions. Therefore, the extent of implant lateral straggle or the impact of a high tilt-angle implant can be measured by comparing the implant mask dimensions to the pre-anneal CI measurement of the width of the implanted regions. Similarly, the extent of dopant lateral diffusion after annealing can be measured by comparing the as-implanted dimensions to the post-anneal CI measurement of the final width of the doped regions. Experimental results on test structures implanted with Boron at implant angles of 0 to 30 degrees and then spike-annealed at temperatures from 950 to 1100 degrees C will be discussed.

2:15 PM C11.3
Highly Parallelized Molecular Dynamics Simulation of Silicon Dislocation Behavior and Dislocation Identification Based on Two-beam Theory.
Takako Okada[1], Toshiaki Yokoi[2], Manabu Kuwabara[3], Yasuyuki Kumagai[3], Kunie Ochiai[3], Shinji Onga[1], Ann Marshall[4], Kyeongjae Cho[5] and Robert W. Dutton[6]; [1]Corporate Research & Development Center, Toshiba corporation, Kawasaki, Kanagawa, Japan; [2]Toshiba I. S. corporation, Kawasaki, Kanagawa, Japan; [3]Information Systems Center, Toshiba corporation, Kawasaki, Kanagawa, Japan; [4]Laboratory for Advanced Materials, Stanford University, Stanford, California; [5]Department for Mechanical Engineering, Stanford University, Stanford, California; [6]Center for Integrated Systems, Stanford University, Stanford, California.

During the fabrication of a silicon integrated circuit, defects and dislocations are often generated in the silicon substrate. Once present in the substrate, dislocations can lead to leakage that degrades performance. Understanding of the dislocation characteristics and generation criteria is an indispensable aid in robust process design for silicon devices. To facilitate of quantitative discussion of TEM images, a computer code for identification of defects and dislocations was developed. Using the code one can identify the Burgers vector and its direction which is otherwise invisible on TEM photos. Among various kinds of silicon defects and dislocations, the morphology can be specified. Moreover, in order to infer atomic structure of the defects/dislocations, the generation mechanism, and its behavior in a stress field for large area images, parallelized molecular dynamics simulations using MPI (Message-Passing Interface) have been developed. Using the simulators, analysis of dislocations has been performed on B^+ implanted Si wafers. In this paper, the simulation method and the results are reported. In the source code for dislocation identification, well-established two-beam TEM procedures for modeling metal and alloy structure are basically adopted. The Howie-Whelan differential equations have been solved. Integration of the electron beam intensity is performed across the entire specimen, taking into account atomic displacements due to defects/dislocations. For molecular dynamics simulations of dislocations, speed-up of calculation is the most important issue since large numbers of Si atoms in the range of 10^3 to 10^5 are needed. We have parallelized a molecular dynamics simulator using MPI in the PC cluster system. Additionally, we have modified the simulation algorithm using a well-optimized cell-subdivision method. Using the improved code, more than 10^4 silicon atoms can be treated in the simulator. Among various examples which we have done, we call upon herein a silicon implantation characterizing study. A boron doped p-type Si wafer had been prepared prior to this experiment. B^+ ion implantation was performed using 350 keV, and then annealing was performed in N_2 ambient at 1050 °C for 20 s for dislocation generation. TEM observations were performed at low magnifications of 40,000 - 80,000. We examined the detail of the dislocations which had periodic image contrast under the two-beam condition. Using the simulator, dislocations were categorized as two major types – (1)edge dislocation dipoles on {113} habit plane and (2)60° dislocation dipoles having {111} habit plane. Using a rigorous MD part, we have visualized the atomistic structure of dipole/habit plane in detail. In the simulation, approximately 25nm x 14nm x 2nm simulation cell composed of more than 30000 Si atoms was used. Simulation results for its resonant behavior will be also shown at the conference.

2:30 PM C11.4
Direct observation of thermal vacancies in highly n-type Si.
Ville Ranki and Kimmo Saarinen; Laboratory of Physics, Helsinki University of Technology, Espoo, Finland.

The thermal vacancies in Si have escaped the direct experimental observation, despite their fundamental and technological importance. Hence their basic thermodynamical properties such as the formation enthalpy have been unknown. In this work we present direct experimental observation of thermal vacancies in Si. The vacancies are created by thermal annealings and observed as quenched to vacancy-impurity complexes in highly As and P-doped Cz Si. The detailed atomic structure of vacancy-impurity complexes present in highly n-type Si can be experimentally determined by combining positron lifetime and electron momentum distribution measurements [1]. The monovacancy surrounded by three As atoms (V-As_3) is the dominant vacancy-impurity complex in Czochralski Si doped with As up to 10^{20} cm^{-3} [1]. By studying the annealing of V-As pairs formed by electron irradiation, we can show that the V-As_3 complexes are formed as a result of the subsequent migrations of V-As and V-As_2 [2]. In the experiments of this work, we create thermal vacancies by annealing highly As and P doped Si at 900 - 1100 K. After the

annealing we observe increased concentrations of vacancy defects and identify that the vacancies are surrounded by three As or P dopant atoms. We infer that the thermal vacancies get trapped by impurities, and form the V-As_3 and V-P_3 complexes by migration similarily as in electron irradiated Si [2]. These results provide thus direct experimental information on thermal vacancies and explain the formation of deactivating vacancy-impurity complexes during the growth. A preliminary estimate of about 2 eV can be deduced for the vacancy formation enthalpy in highly n-type conditions where the Fermi level is close to the conduction band. This estimate is in good agreement with recent theoretical results [3]. [1] K. Saarinen et al., Phys. Rev. Lett. 82, 1883 (1999). [2] V. Ranki et al., Phys. Rev. Lett. 88, 105506 (2002). [3] M. J. Puska et al., Phys. Rev. B 58, 1318 (1998).

2:45 PM C11.5
Damage Influence on Electrical Characterizations After Solid Phase Epitaxial Regrown. Xavier Hebras[1], Filadelfio Cristiano[1], Wilfried Lerch[2], Silke Paul[2], ray Duffy[3] and Alain Claverie[1]; [1]LAAS/CNRS, Toulouse, France; [2]Mattson Thermal Product, Daimlerst, Germany; [3]Philips research Labs, Kapaldreef, Belgium.

Sheet resistance and spreading resistance measurements are the most common methods for evaluating the activation level of semiconductors. These techniques are sensitive to carrier concentration and electrical junction position. Defects generated by ion implantation can modify these parameters. Solid Phase Epitaxial Regrowth (SPER) is considered as a promising doping technology to provide solutions for highly-activated, shallow, and abrupt dopant profiles for sub 65nm CMOS technologies. However the principal drawback of this method is the high density of defects. Under certain conditions, the defects can generate a local space charge region, reorganize the carrier distribution end deactivate dopant. This raises a question about the perturbations of electrical characterizations due to the presence of a large defect band after SPER. The aim of this work is to evaluate the influence of defects on electrical characterizations. We will show results from Nano-SRP measurements on p+/n junctions made with different preamorphization conditions. The results strongly depend on the position of the damage area: the electrical junction disappears when the defects are located in the space charge region. To investigate these interactions further we realized a well targeted CVD structure in order to have a well known metallurgical junction with constant doping level. Ultra low energy boron implantations have been made into this structure to check the over activation level during SPEG. Different amorphous layer depths have been made to follow the activation and deactivation of the CVD with or without implantation. The effect of the relative position of the defect on the sheet resistance, nano-SRP and hall measurement will be discussed.

3:30 PM C11.6
Measurements of Ultra-shallow Junction (USJ) Sheet Resistance with a Non-Penetrating Four Point Probe. John O Borland[2], robert j hillard[1] and Win Ye[1]; [1]Applications, Solid State Measurements, Inc., Pittsburgh, Pennsylvania; [2]Job Technologies, South Hamilton, Massachusetts.

An accurate method for measuring the sheet resistance (Rs) of USJ source-drain structures by a novel four point probe (4pp) is described. The new method utilizes Elastic Material gate (EM-gate) probes to form non-penetrating contacts to the silicon surface. The probe design is kinematic and the force is controlled to ensure elastic deformation of the probe material. The probe material is selected so that large direct tunneling currents can flow through the native oxide thereby forming a low impedance contact. Sheet resistance measurements on USJ Arsenic-implanted structures with SIMS junction depths of 30 nm and smaller have been made. The sheet resistance values obtained with the new EM-gate 4pp method were around 280 Ohms and were consistent with expectations. Additionally, the results were in close agreement with Variable Probe Spacing (VPS)(1) Rs values. (VPS is another method that has been used for determining sheet resistance on USJ structures.) In this paper, the new 4pp will be demonstrated on a variety of implanted USJ structures. (1) ECS Journal, Vol. 131, No. 2, Feb-1984, p. 392

3:45 PM C11.7
Simultaneous determination of ultra-shallow junction depth and abruptness using thermal wave technique.
Lena Nicolaides[1], Alex Salnick[1], Jon Opsal[1], Amitabh Jain[2], Duncan Rogers[2] and Lance Robertson[2]; [1]Therma-Wave Inc., Fremont, California; [2]Texas Instruments, Inc., Dallas, Texas.

Thermal wave (TW) studies of ultra-shallow junctions (USJ) formed by ion implantation into a semiconductor wafer followed by rapid thermal annealing (RTP) are described. It is shown that using the TW technique allows for a simultaneous determination of the most important USJ parameters, depth and profile abruptness. In a TW-based system, the USJ depth is obtained using the quadrature component of the TW signal while determination of USJ profile abruptness is based on the analysis of the TW quadrature and in-phase components measured at two different pump-probe beam offsets. Experimental results for junction depth and abruptness obtained on a set of B+ implanted, RTP-annealed USJ samples show better than 0.99 correlations to the corresponding secondary ion mass spectroscopy (SIMS) data.

4:00 PM C11.8
Analysis of Ion Implantation Damage in Silicon Wafers.
Richard Ahrenkiel[1,3], Jamiyana Dashdorj[1,3], Dean Levi[1] and Bohumil Lojek[2]; [1]Measurements and Characterization Division, National Renewable Energy Laboraatory, Golden, Colorado; [2]Atmel Corporation, Colorado Springs, Colorado; [3]Department of Physics, Colorado School of Mines, Golden, Colorado.

Rapid thermal annealing (RTA) is required to heal the lattice damage created by heavy ion implants such a boron or arsenic. The RTA process maintains the structural integrity of the semiconductor used for submicron-integrated circuits. Quick, efficient, and contactless diagnostics of the implantation damage are highly desirable in both research and production environments. A new measurement technique has been applied to this problem and correlated with other diagnostics. The resonant-coupled photoconductive decay (RCPCD) technique uses a deeply penetrating, low-microwave-frequency probe in conjunction with a variable-wavelength pulse from a tunable laser source. The recombination lifetime of the implanted region decreases many orders of magnitude after implantation. The crystallinity is restored by RTA, and the degree of restoration varies with the details of the RTA process. We are looking at efficient ways of assessing the efficacy of various processeses for removing damage. The damage is manifested in a sharp decrease in the lifetime when using strongly absorbed light. This damage strongly effects the surface lifetime, which is the lifetime measured using strongly absorbed light. The as-implanted layer acts as a sink for minority carriers, and the surface lifetime becomes very small. We are using the latter as a metric of the implantation damage anneal. The implanted region also shows optical properties similar to amorphous silicon as determined by variable-angle scanning ellipsometry (VASE). Other electrical measurements, such as capacitance-voltage and sheet resistivity, show changes characteristic of implantation damage. We have assumed a model for which the implanted region has optical and electronic properties similar to amorphous silicon. In this work, we correlate the surface lifetime of implanted wafers with the optical constants acquired with VASE measurements. The lifetime increases with various annealing processes, and the optical constants approach those of amorphous silicon. We will correlate the lifetime changes with the measured optical spectra for a variety of annealing conditions. We will also show data for the sheet resistance and the correlations with the surface lifetime. For the fully activated implantation layer, the device structure acts to produce charge separation, and the lifetime may become larger than the original bulk lifetime. In this case, the photoconductive decay time of the annealed structure is shown to be related to the leakage current in the finished device. In summary, we will present a protocol for quickly evaluating the effectiveness of various implantation annealing processes.

4:15 PM C11.9
Novel, non-contact mapping metrology for ultra-shallow junction sheet resistance and leakage current.
Michael Ira Current, Vladimir Faifer, Phuc Van, Wojtek Walecki, S. H Lau and Ann Koo; Frontier Semiconductor, San Jose, California.

Production controls for ultra-shallow junctions requires in-line methods for measurements of sheet resistance in the range from 100 to 900 Ohm/square for junction depths in the range of 30 to less than 10 nm (according to the ITRS03 requirements). Physical probing methods are limited by effects such as junction penetration, probe current heating and leakage current induced errors in sheet resistance measurements. Optical interference and reflection methods give structural information on junction depth and damage density but have limited or no sensitivity to electrical activation of shallow junction dopants. This paper describes a novel, non-contact method for determination of ultra-shallow junction sheet resistance and leakage current density which combines pulsed photo-generation of surface carriers with analysis of amplitude and phase signals from capacitance probes. At light pulsing frequencies of about 100 kHz, the surface voltage signal gives a direct measure of the junction sheet resistance, independent of the junction depth. At lower light pulsing frequencies, the junction leakage current density is determined. This method provides for direct monitoring of sheet resistance in the range from 50 to 10,000 Ohms/square and junction leakage current densities in the range from 10-6 to 10-3 A/cm2. Coupling this capacitive monitoring of pulsed photo-generated free carriers with a precision wafer motion stage allows for rapid acquisition of sheet resistance and leakage data for efficient wafer-scale mapping applications. Examples of the use of this novel non-contact metrology for electrical characterization of ultra-shallow junctions, including a variety of

implant and pulsed heating anneal techniques, will be described.

4:30 PM C11.10
XAFS as a Direct Local Structural Probe in Revealing the Effects of C Presence in B Diffusion in SiGe Layers.
Mehmet Alper Sahiner[1], Parviz Ansari[1], Malcolm S. Carroll[2], Charles W. Magee[3] and Joseph C. Woicik[4]; [1]Seton Hall University, South Orange, New Jersey; [2]Sandia National Laboratories, Albuquerque, New Mexico; [3]Evans East, East Windsor, New Jersey; [4]NIST, Gaithersburg, Maryland.

The local structural information around the germanium atom in boron doped SiGe alloys is important in understanding the dopant diffusion mechanisms. Epitaxial SiGe test structures with B markers were grown on Si substrates by using rapid thermal chemical vapor deposition (RTCVD). In these structures, C was also incorporated with various concentrations. The local structure around the Ge atom was probed using Ge K-edge x-ray absorption fine structure spectroscopy (XAFS) to determine the effects of the C and B on the Ge sites. The concentration profiles obtained from secondary ion mass spectroscopy are correlated with the Ge XAFS results. The modifications on the local structure around the Ge atoms are revealed from the multiple scattering analysis on the Ge near neighbors. The trapping mechanism for the B diffusion due to the presence of the C atoms will be discussed using the SIMS concentration profiles and these local structural changes.

4:45 PM C11.11
On the diffusion of interstitial Fe in $Si_{1-x}Ge_x$ alloys.
Gerd Weyer[1,2], H.P. Gunnlaugsson[1], K. Bharuth Ram[3], M. Dietrich[2], R. Mantovan[5], D. Naidoo[3] and R. Sielemann[4]; [1]Department of Physics and Astronomy, Aarhus University, Geneva 23, Denmark; [2]EP Division, CERN, CH-1211 Geneva 23, Switzerland; [3]School of Pure and Applied Physics, University of Natal, 4041 Durban, South Africa; [4]Hahn-Meitner Institute, D-14109 Berlin, Germany; [5]Laboratorio MDM-INFM, 20042 Agrate Brianza, Italy.

Among the transition metal impurities in silicon Fe and interstitial Fe_i in particular can be said to be the best studied. The detrimental role of Fe_i in devices is to a large extent due to a deep donor state in the band gap and a fast diffusivity, which in silicon is different by more than an order of magnitude at low temperatures for neutral and positively charged ${Fe_i}^{0/+}$. Recently, the diffusivity of ${Fe_i}^{+}$ in $Si_{1-x}Ge_x$ for $x<0.1$, measured for an ensemble of jumps, was found not to be affected by alloying with Ge, whereas the donor state shifts towards the valence banc [1]. Here we report on the observation of diffusional jumps of Fe_i on an atomic scale by means of the resulting line broadening in their Mössbauer spectra, which is directly proportional to the jump frequency. Radioactive ${}^{57}Mn^{+}$ ions ($T_{1/2}$=1.5 min.) were implanted at the ISOLDE facility into bulk and epitaxially grown $Si_{1-x}Ge_x$ alloys ($x\leq 0.08$) with 60 keV energy to fluences $<10^{12}/cm^2$. The crystals were held at 500-800 K. The radiation damage from the implantation of single ions is known to anneal at these temperatures during the ${}^{57}Mn$ lifetime and the ${}^{57}Mn$ probe atoms are incorporated on substitutional lattice sites. An average recoil energy of 40 eV, imparted on the ${}^{57m}Fe$ daughter atoms in the nuclear decay to the 14 keV Mössbauer state, expels the majority into tetrahedral interstitial sites. A few diffusional jumps of the interstitial ${}^{57m}Fe_i$ atoms during the lifetime of the Mössbauer state (140 ns) lead to a line broadening and eventually to the formation of Fe_i-V pairs with the vacancy created in the recoil process. Thus determined jump frequencies were found to increase in $Si_{1-x}Ge_x$ with increasing x. The implications of this effect for the purely interstitial Fe_i diffusion mechanism as well as conclusions from a comparison to the unaffected "macroscopic" diffusion, as determined in ref. 1, will be discussed. It is noteworthy that the ${Fe_i}^{0/+}$ diffusivities in pure silicon determined by, respectively, similar techniques as in ref. 1 [2] and by analogous Mössbauer experiments as the present [3] are in very good agreement for both charge states. References: [1] A. Mesli et al., Phys. Rev. B 66 (2002) 045206 [2] T. Heiser and A. Mesli, Phys. Rev. Lett. 68 (1992) 978 [3] H.P. Gunnlaugsson et al., Appl. Phys. Lett. 89 (2002) 2657