SYMPOSIUM D

High-k Insulators and Ferroelectrics for Advanced Microelectronic Devices

April 12 - 16, 2004

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* Invited paper

TUTORIAL

Electrical Characteristics of High-k-Based MOS Devices
Monday April 12, 2004
1:30 PM - 5:00 PM
Room 2006 (Moscone West)

The scaling of the gate dielectric in the future generations of MOS (Metal-Oxide-Semiconductor) devices is recognized as a major issue in the field of microelectronics. Consequently, tremendous research efforts have been focused in recent years to the investigation of high-k gate dielectrics for the potential replacement of silicon dioxide in MOS devices. One of the key issues concerns the characterization and understanding of the electrical properties of these structures. After a general introduction to the field, the electrical characteristics of these devices will be described in details. Issues such as threshold voltage control and instabilities, mobility degradation, charge trapping, defect generation and ionic transport in high-k gate stacks, device lifetime and dielectric breakdown, and negative and positive bias temperature instabilities will be covered. Our current understanding of these properties will be emphasized. Based on these results, possible future directions in the field (including high mobility substrates, metal gates, etc.) will be discussed.

Instructor:
Michel Houssa, IMEC

SESSION D1: Atomic Layer Deposition of High-k Dielectrics
Chairs: Jamie Schaeffer and Bob Wallace
Tuesday Morning, April 13, 2004
Room 2006 (Moscone West)

8:30 AM *D1.1
Recent Developments in Understanding Local Effects and Device Properties of Hf-based High-k Dielectrics. Glen Wilk[1], Dave Muller[2] and Jan Willem Maes[1]; [1]ASM America, Phoenix, Arizona; [2]Department of Applied and Engineering Physics, Cornell University, Ithaca, New York.

Atomic-scale electron spectroscopy is used to determine the local electronic structure of atomic-layer-deposited HfO_2 gate dielectrics as a function of annealing conditions. Oxygen core-loss spectra from monoclinic crystallites exhibit a more strongly pronounced crystal-field splitting with increasing anneal temperature up to 1000°C, consistent with a decrease in point defects. Concomitantly, electrical measurements of the same structures show a correlated reduction of fixed charge. An unintentional 5 $\AA$ SiO_2 layer is observed at the *top* interface, between the HfO_2 and poly-Si electrode. No Hf-silicate intermixing is detected at either interface on a scale down to 2 $\AA$. In addition, improved understanding of the nucleation and growth behavior of ALD HfO_2 and HfSiO(N) has led to well-engineered interfaces, thus allowing smaller incubation times for HfO_2 growth. With these tailored dielectric stacks, much improved transistor characteristics have been achieved, including higher carrier mobilities and higher drive currents for both high-performance and low standby-power devices.

9:00 AM D1.2
The growth kinetics of HfO2 films on Si (100) grown by atomic-layer deposition using in-situ medium energy ion scattering. Hyo Sik Chang[1], Hyunsang Hwang[1], Mann-Ho Cho[2] and Dae Won Moon[2]; [1]Department of Materials Science and Engineering, Kwangju Institute of Science and Technology (KJIST), Gwangju, South Korea; [2]Nano Surface Group, Korean Research Institute of Standards and Science (KRISS), Daejeon, South Korea.

The growth kinetics and initial growth stage of HfO2 films on p-type Si(100) grown by atomic-layer deposition (ALD) was investigated using in-situ medium energy ion scattering (MEIS). The interaction between adsorbed HfCl4 molecules and Si substrate was examined in relation to the film thickness, substrate temperatures, and surface states of the Si substrates. Interfacial reaction between Hf and Si at the initial growth stage was occurred and significantly depended on the surface state of the Si. The HfO2 with an amorphous structure was grown on the oxidized Si substrate at an initial growth stage. In particular, the interfacial layer thickness and the stoichiometry of the layer were depended on the surface state of Si substrate. The physical analysis of the films with XPS and TEM also supported the interfacial reactions. Based on the interfacial interaction at the initial growth stage, we suggested the model for the interaction between Hf and Si at the initial growth stage in relation to the atomic size, bonding characteristics, and formation energy. This study will be helpful to understand the interfacial reactions at the initial growth stage and to control the reactions for the application of high-k dielectrics.

9:15 AM D1.3
Interval Annealing During Alternating Pulse Deposition.
John F. Conley, Douglas J Tweet, Yoshi Ono and Greg Stecker; Advanced Technology Group, Sharp Labs of America, Camas, Washington.

Thin films deposited via atomic layer deposition tend to be less dense than the bulk material. Densification typically requires high temperature post deposition annealing that may violate the thermal budget of a sensitive process. We have found that modulated temperature annealing of pulse deposited films, in which in-situ elevated temperature anneals are performed after every n deposition cycles, results in film densification. HfO_2 films were deposited via a dual metal precursor technique in which alternating pulses of $Hf(NO_3)_4$ and $HfCl_4$ are separated by N_2 purges. Rapid thermal anneals (30 sec at approx 420°C in N_2) were performed after every n deposition cycles where n ranged from one to the total number of cycles. Films were characterized via ellipsometry, x-ray diffraction, x-ray reflectivity, capacitance vs. voltage, current vs. voltage, and limited TEM. Film thickness and deposition rate / cycle were found to decrease and film density was found to increase with decreasing anneal interval (more frequent annealing). Using interval annealing, we were able to "tune" the density of HfO2 thin films from 7.7 (for samples annealed only at the end of the deposition) to 10 g/cc. It was found that the highest density films (10 g/cc) can be achieved only by every-cycle annealing. Densification was likely due to the removal of unreacted ligands that remain after a deposition cycle is complete. Consistent with the film density results, it was found that the refractive index of the films ranged from 1.9 for the samples annealed only once to about 2.2 for the every-cycle annealed samples. For films annealed every cycle, XRD results indicate the appearance of an additional crystallization peak suggesting the presence of a dense orthorhombic phase. Films annealed every cycle and every other cycle demonstrated improvement in dielectric properties. Films annealed every cycle were shown to have a reduction in interfacial layer thickness from 1.1 nm to 0.5 − 0.6 nm. The level of densification and improvement of electrical properties observed in the every cycle annealed films could not be achieved by post deposition annealing.

9:30 AM D1.4
ALD Grown Lutetium-Based Oxides for Gate Dielectric Applications. Giovanna Scarel[1], Sabina Spiga[1], Gabriele Seguini[1], Claudia Wiemer[1], Grazia Tallarida[1], Emiliano Bonera[1], Marco Fanciulli[1], Igor Fedushkin[2], Herbert Schumann[2], Andrei Zenkevich[3] and Yuri Lebedinskii[3]; [1]Laboratorio MDM, INFM, Agrate Brianza, Italy; [2]Institut fuer Chemie, TU Berlin, Berlin, Germany; [3]Physics of Solids, Moscow Engineering Physics Institute, Moscow, Russian Federation.

Rare earth oxides could represent a valuable alternative to SiO2 in CMOS devices. In particular, Lu2O3 is proposed because, despite the calculated κ only in the range between 12-13, it is predicted to be thermodynamically stable on silicon with a high (> 2 eV) conduction band offset (CBO), expected as a consequence of three factors. (i) The large band gap, related to the completely filled 4f shell of Lu, (ii) the possibility of only one oxidation number (3), which avoids mixed Lu-oxide stoichiometries with different electronic structures, and (iii) the 2:3 metal:oxygen stoichiometry ratio which promotes a low value of the charge neutrality level and hence a high CBO at the oxide/silicon interface. In addition, low density of interfacial traps are predicted for Lu2O3 due to the intrinsic high energy of the 5d shells and their low occupancy (only one electron) in Lu. Lu-silicates are also promising candidates due to their predicted thermo-dynamical stability on Si, accepatble CBO, and κ. Moreover, silicates have a higher crystallization temperature than the corresponding oxides. To assess the quality of Lu-based oxides, Cp(Me3Si) and (Me3Si)2N ligands were synthetized and bound to Lu atoms to form volatile and monomeric complexes. These complexes were used as Lu precursors during atomic layer deposition (ALD) in a temperature range between 350 °C and 380 °C of Lu-based oxides on Si(100) using H2O or O3 as oxygen sources. Compositional, structural, and morphological analysis revealed that the ALD Lu[Cp(Me3Si)]3+H2O process gave rise to a stoichiometric, polycrystalline, and quite rough (rms roughness of about 2.7 nm for a 19 nm thick film) Lu2O3 layer. In particular, x-ray diffraction and Fourier transform infrared spectroscopy analyses identified respectively the cubic IA-3 structure with a lattice parameter of 1.034 nm and absorption bands at 300 cm-1, 340 cm-1, and 385 cm-1, similar to those of cubic Y2O3. On the other hand, the ALD Lu[(Me3Si)2N]3+H2O and Lu[(Me3Si)2N]3+O3 processes produced amorphous layers of a form of Lu-silicate, as revealed from Rutherford back-scattering analysis and x-ray photoelectron spectroscopy (XPS) measurements. The evolution of the Lu and O chemical states in both the Lu2O3 and the Lu-silicate layers is

monitored with XPS upon annealings in O2 and vacuum at 750 °C and 950 °C, respectively, and the binding energy positions of Lu4f and the O1s peaks in the film layer do not shift significantly, indicating a remarkable thermal stability. MOS capacitors were fabricated by Al thermal evaporation through a shadow mask. The κ value measured in the 10-300 kHz frequency range for as-grown Lu2O3 and Lu-silicate films was respectively around 10-11 and 7-8. CV curves revealed fixed positive charges and large hysteresis in both Lu-based oxides. Interface state density is found to be of the order of 10î1 eV-1 cm-2, with a remarkable increase for the Lu-silicate films grown using O3 as oxygen precursor.

9:45 AM D1.5
Optimization of ALD grown HfO2 properties based on a novel precursor combination including Hf(OtBu)2(mmp)2 and HfCl4. Giovanna Scarel, Sabina Spiga, Claudia Wiemer, Grazia Tallarida, Emiliano Bonera, Sandro Ferrari and Marco Fanciulli; Laboratorio MDM, INFM, Agrate Brianza, Italy.

HfO2 as well as Hf silicates and aluminates are among the most promising candidates to substitute SiO2 as active dielectrics in CMOS-based devices. In this work we study the combination of the monomeric and non-air-sensitive Hf(OtBu)2(mmp)2 precursor with HfCl4 for the growth of HfO2 films using atomic layer deposition (ALD) on Si(100) with chemical oxide or upon HF-last treatment. The mentioned precursor combination leads to excellent structural and morphological properties combined with good electrical ones. Upon injection in the reaction chamber of Hf(OtBu)2(mmp)2, the reaction proceeds, at 375 °C, through partial decomposition of the precursor leaving $(OH)^-$ species on the growing surface. The injection of HfCl4 not only efficiently reacts with these $(OH)^-$ surface species, but supplies an additional amount of Hf atoms so that the growth rate (0.17 nm/cycle) is almost doubled compared to the Hf(OtBu)2(mmp)2 + H2O or O3 (both about 0.09 nm/cycle) ALD processes. For HfO2 films obtained from Hf(OtBu)2(mmp)2 and HfCl4, x-ray reflectivity measured an electronic density of 2.37 e-/$\acute{A}^3$, as expected for thin HfO2 layers in the monoclinic phase. Indeed, both by x-ray diffraction and Fourier transform infrared spectroscopy analysis on as grown films detect the monoclinic phase with a small fraction of a metastable component. The latter is a remarkable result compared to HfO2 films from HfCl4+H2O, where both the monoclinic and the orthorhombic phases were detected. Surface roughness is much lower than in HfO2 films of comparable thickness obtained from other precursors and weakly dependent on thickness. For example, on a 50 nm thick film from Hf(OtBu)2(mmp)2+HfCl4 an rms roughness of 0.6 nm is measured. This value is lower to the rms roughness of 1 nm measured on a 10 nm thick film from HfCl4+H2O. The interfacial roughness (0.5-0.6 nm) is comparable to the surface roughness, suggesting that the Hf(OtBu)2(mmp)2+HfCl4 ALD process generates highly conformal films. Carbon contaminations due to the metalorganic precursor decomposition are detected by time of flight – secondary ion mass spectrometry, and chlorine concentration is higher than in films deposited through the HfCl4+H2O ALD process at the same growth temperature. This finding suggests that the desorption of HCl is less efficient in the Hf(OtBu)2(mmp)2+HfCl4 ALD process. Capacitance-voltage curves of HfO2 films grown from Hf(OtBu)2(mmp)2 + HfCl4 on chemical oxide show no dispersion in a frequency range from 10 kHz to 500 kHz, small hysteresis and a low density of interface states ($\approx$8 x 10î0 eV^{-1} cm^{-2}). The measured κ is around 13-15.

10:30 AM *D1.6
Novel Ultra-thin TiAlOx Alloy Oxide for Next Generation of Gate Dielectric. Orlando Auciello[1], Wei Fan[2], Sanjib Saha[3], Bernard Kabius[4], John M. Hiller[5], John A. Carlisle[6], Cirillo Lopez[7], Eugene A. Irene[8] and Raul A Baragiola[9]; [1]Materials Science Division, Argonne National Laboratory, Argonne, Illinois; [2]Materials Science Division, Argonne National Laboratory, Argonne, Illinois; [3]Materials Science Division, Argonne National Laboratory, Argonne, Illinois; [4]Materials Science Division, Argonne National Laboratory, Argonne, Illinois; [5]Materials Science Division, Argonne National Laboratory, Argonne, Illinois; [6]Materials Science Division, Argonne National Laboratory, Argonne, Illinois; [7]Department of Chemistry, University of North Carolina, Chapel Hill, North Carolina; [8]Department of Chemistry, University of North Carolina, Chapel Hill, North Carolina; [9]Department of Materials Science and Engineering, University of Virginia, Charlottesville, Virginia.

We will review our recent work focused on fundamental and applied science directed at developing a novel TiAlOx alloy oxide as an alternative gate oxide material for CMOS devices (patent pending). Ultra-thin TiAl films with physical thickness 3-20 nm were grown on n-Si (100) by sputter deposition. In-situ oxidation was then performed by using both molecular oxygen (P=1.0x10-3 Torr) and atomic oxygen sources (P=1.0x10-4 Torr). The formed TiAlOx exhibits amorphous structure on Si, as revealed by XRD and TEM analyses. In-situ XPS study shows that a full oxidation of TiAl can be achieved at 500 oC using both oxygen sources. However, the TiAlOx layer formed through atomic oxygen annealing presented a leakage current 150 times lower than the one with molecular oxygen annealing. Since both Ti and Al have more negative oxide formation energies than Si, the presence of Ti and Al at the interface with Si significantly reduces the formation of interfacial SiO2. This result has been confirmed by XPS depth profile, ellipsometry and high-resolution cross-section TEM, which revealed 1 nm SiOx layer formed at the oxide/semiconductor interface with 500oC oxidation. An amorphous TiAlOx layer with equivalent oxide thickness (EOT) of 1.7 nm and negligible hysteresis was obtained via atomic oxygen exposure at 500oC, exhibiting high permittivity (30) and low leakage current density (1.2x10-2 A/cm2). After post deposition annealing with top gate electrode in place, the leakage was further improved and reached 5.4x10-5 A/cm2. Furthermore, extended study shows that a full transition of TiAl to TiAlOx can be accomplished at room temperature by exposure to atomic oxygen beam. Interfacial SiO2 formation, therefore, was practically eliminated or at the most is one to two monolayers. TiAlOx layers with EOT less than 1 nm were achieved on Si using room temperature oxidation with atomic oxygen. Bandgaps of up to 4 eV have been measured using spectroscopic ellipsometry and EELS. Initial measurements of interface density of states show values of 1012 trapps/cm2. * This work was supported by the U.S. Department of Energy, BES-Materials Sciences, under Contract W-31-109-ENG-38.

11:00 AM D1.7
HfO_2 Thin Films from Cyclopentadienyl Precursor by Atomic Layer Deposition. Jaakko Niinisto, Matti Putkonen and Lauri Niinisto; Laboratory of Inorganic and Analytical Chemistry, Helsinki University of Technology, Espoo, Finland.

For the atomic layer deposition (ALD) of HfO_2 the $HfCl_4/H_2O$ process has mostly been applied. However for gate oxide applications, some problems, such as chloride contamination and corrosion problems have caused concern. Therefore, it is important to explore alternative precursor combinations. In this work, HfO_2 thin films have been deposited onto native oxide or H-terminated Si(100) substrates by ALD using $Cp_2Hf(CH_3)_2$ (Cp=cyclopentadienyl, C_5H_5) and water as precursors at deposition temperatures ranging from 300 to 500^oC. Processing parameters were optimised and ALD-type growth verified at 350^oC. Stoichiometric HfO_2 films deposited at 350^oC had impurity levels below 0.2 and 0.4 atomic-% for carbon and hydrogen, respectively as analyzed by TOF-ERDA. The crystallinity, morphology and dielectric properties were characterized. The effective permittivity of HfO_2 in Al/HfO_2/native oxide or HF-etched/Si/Al capacitor structures was dependent on the HfO_2 layer thickness and substrate pretreatment used. Strong inhibition of HfO_2 film growth was observed with the water process on HF-etched Si. The effect of the oxygen source on the properties and growth of HfO_2 films is discussed, while comparative depositions with ozone as an oxygen source have been made.

11:15 AM D1.8
In-situ Analysis of HfO_2 Formation of Remote Plasma Atomic Layer Deposition Process. Sang Wook Park, Ju Youn Kim, Seok Hoon Kim and Hyeongtag Jeon; Division of Materials Science and Engineering, Hanyang Univ, Seoul, South Korea.

High dielectric constant materials are recently attracted for alternative gate dielectric application in sub-0.1μm in metal-oxide-semiconductor (MOS) devices due to its thermodynamical stability on silicon, a high dielectric constant, a high breakdown field, and a large band gap.Among the several high dielectric constant materials, HfO_2 gate oxide has been focused to study to increased during recent years due to its high dielectric constant and good thermal stability in contact with silicon. We investigated the HfO_2 gate dielectric material deposited by remote plasma enhanced atomic layer deposition (PEALD) method.HfO_2 films were deposited at 200̃350°C using tetrakis-dimethyl-amino- hafnium (TDEAH) as Hf precursor and oxygen plasma as reactant gas.In this study, in-situ analysis system is constructed and is connected with remote PEALD system. We deposited HfO_2 with this system and thickness of HfO_2 was controlled by the number of deposition cycle. One cycle of HfO_2 deposition consists of Hf precursor supply and O_2 or O_2 plasma supply.Each step of one cycle was monitored by in-situ XPS (X-ray photoemission spectroscopy) and AFM (atomic force microscopy). We observed XPS peak related with silicate grown from the first cycle of plasma enhanced ALD process. But no silicate peak was observed with O_2 supply of normal ALD process. After growing HfO_2, the electrical properties of HfO_2 of MOS capacitor were measured.The physical and chemical characteristics of HfO_2 film were analyzed by cross-sectional transmission electron microscope (XTEM), Auger electron spectroscopy (AES), XPS.The electrical properties and reliability characteristics including EOT, hysteresis, leakage current and capacitance were evaluated by I-V and C-V measurements. This paper will present the characteristics and in-situ surface analysis of HfO_2 gate dielectric deposited by remote PEALD using metal organic

precursor.

11:30 AM D1.9
Atomic Layer Deposition of Aluminum Nitride Thin Films from Trimethyl Aluminum (Tma) and Ammonia. Xinye Liu, Sasangan Ramanathan, Eddie Lee and Thomas E. Seidel; Genus, Inc., Sunnyvale, California.

Aluminum nitride (AlN) thin films were deposited from trimethyl aluminum (TMA) and Ammonia (NH3) by thermal atomic layer deposition (ALD) and plasma enhanced atomic layer deposition (PEALD) on 200 mm silicon wafers. 100% step coverage was achieved for 100nm trenches with aspect ratio of 34 to 44. Film thickness increased linearly as number of cycles increased. Large number of incubation cycles was needed to deposit AlN film on Si wafers. Temperature dependence of deposition rate was studied at susceptor temperature from 200 C to 470 C. X-ray diffraction (XRD) data showed that films deposited at from 370 C to 470 C were polycrystalline. Glancing angle X-ray specular reflection (XRR) results showed that roughness of film was about 12 A for thermal ALD films with 800 A thickness, which is consistent with atomic force microscopy (AFM) measurement. Density of film derived from XRR measurement is 75% to 100% of known bulk value. Mercury probe measured dielectric constant was about 7.5.

11:45 AM D1.10
Atomic Layer Deposition (ALD) of High-k Dielectrics: Lanthanum Aluminum Oxide and Praseodymium Aluminum Oxide. Antti Rahtu, Philippe de Rouffignac and Roy G Gordon; Chemistry and Chemical Biology, Harvard University, Cambridge, Massachusetts.

Lanthanum aluminum oxide thin films were grown by ALD from a new lanthanum precursor, tris(N,N'-diisopropylacetamidinato) lanthanum, trimethylaluminum and water. Smooth, amorphous $La_xAl_{1-x}O_3$ films were deposited on HF-last silicon and measured without post-deposition annealing. Their composition was measured by RBS, XPS and SIMS. The films contained less than 1 at. % of carbon. C-V and I-V curves were measured with mercury electrodes and also with sputtered gold electrodes. A thin (9.8 nm) film showed low leakage current ($<5*10^{-8}$ A/cm^2 at 1 V at an equivalent oxide thickness of 2.9 nm), flat-band voltage of -0.1 V and low hysteresis (20 mV). Thicker films had even lower leakage currents ($<10^{-8}$ A/cm^2 at 2 MV/cm) but larger flat-band shifts and more hysteresis. The permittivity of the films was 13 and the dielectric strength 4 MV/cm. Cross sectional HRTEM showed a sharp interface between the $La_xAl_{1-x}O_3$ and the silicon substrate. Thin films of praseodymium aluminum oxide, $Pr_xAl_{1-x}O_3$, were also grown using a similar new praseodymium precursor, tris(N,N'-diisopropylacetamidinato) praseodymium. Their electrical properties will be reported and compared with those of the $La_xAl_{1-x}O_3$ films.

SESSION D2: Electrical Chaacterization and Reliability of High-k - Oxynitrides
Chairs: Jean-Luc Autran and Glen Wilk
Tuesday Afternoon, April 13, 2004
Room 2006 (Moscone West)

1:30 PM *D2.1
Threshold Voltage Instability and Inversion Layer Mobility Degradation of HfAlOx(N) Gate Dielectric CMOS. Akira Toriumi[1,2], Naoki Yasuda[3], Hiroyuki Ota[2], Hirokazu Hisamatsu[3], Watarru Mizubayashi[2], Toshihide Nabatame[3] and Tsuyoshi Horikawa[2]; [1]The University of Tokyo, Tokyo, Japan; [2]MIRAI-AIST, Tsukuba, Japan; [3]MIRAI-ASET, Tsukuba, Japan.

The threshold voltage instability and the mobility degradation are main concerns of high-k gate stack technology. In order to clarify each degradation mechanism, high-k CMOS (n- and p-MOSFETs) with the same dielectric film (HfAlOx(N)) and the same gate electrode (TaN or n+poly-Si) were fabricated through the same thermal processes. The interface layer at HfAlOx(N)/Si was varied in terms of the thickness and the material (SiO2 and SiON). First, the difference of Vfb (Vth) between n- and p-MOSFETs is discussed. In particular, δVfb=Vfb(n-MOSFET)-Vfb(p-MOSFET) has been compared with the Fermi potential difference, $\delta\phi_F$, in Si substrates for TaN and n+poly Si gate electrodes. In the case of TaN, δVfb is roughly a half of $\delta\phi_F$, while in the case of poly-Si δVfb is in good agreement with $\delta\phi_F$, even though the interface states density is nearly the same. This fact clearly indicates that Vfb (Vth) is very sensitive to the interface characteristics between gate electrode and high-k dielectric film, and that electronic states are induced at the top interface with metal gate. The mobility degradation has been also investigated from the viewpoint of the scattering mechanism differences between electron and hole in the inversion layer. As the absolute value of the mobility is different between electron and hole due to the effective mass difference, we have paid attention to the ratio, ρ, of the actual mobility with the universal one, so as to discuss the scattering probability rather than the absolute value of the mobility. The relationship between the ratio, ρ, and the inversion carrier density, Ns, indicates a remote scattering characteristic as well as a clear difference of scattering mechanism between electron and hole in the high-k MOS inversion layers. Since we employed absolutely the same gate stack for both n- and p-MOSFETs, it is strongly suggested that the experimental results come from a scattering rate difference between electron and hole. Furthermore, it is noted that $\sigma=\tau\text{new}^{-1}/\tau\text{universal}^{-1}$, which is defined as the ratio of a scattering rate newly introduced into high-k MOSFET, τnew^{-1}, to that of the universal one, $\tau\text{universal}^{-1}$, can be described by ρ^{-1}-1. It is worthy of particular attention that σ values for both electron and hole seem to be approximately proportional to $\text{Ns}^{-0.5}$, and moreover that detailed observation shows the significant scattering enhancement and the non-monotonic Ns dependence of σ for electron in spite of the same gate stack structure.

2:00 PM D2.2
Improved Electrical Characteristics of Hafnium Oxynitride High-k Dielectric Films Prepared by Ultraviolet-Assisted Oxidation and Nitridation. Chad Robert Essary, Joshua M. Howard, Valentin Craciun and Rajiv K. Singh; Materials Sci & Eng, University of Florida, Gainesville, Florida.

Currently in the search for an alternative high-k dielectric material to replace silicon dioxide, hafnium oxide has shown promise due to its thermodynamic stability on silicon and higher dielectric constant. This study focuses on Hf metal thin films deposited on Si substrates using a pulsed laser deposition technique in vacuum and in ammonia ambients. The films were then oxidized at 400 °C in 300 Torr of O_2. Half the samples were oxidized in the presence of ultraviolet radiation from a Hg lamp array. X-ray photoelectron spectroscopy, atomic force microscopy, and grazing angle X-ray diffraction were used to compare the crystallinity, roughness, and composition of the films. Capacitance-voltage and current-voltage measurements were used to compare the electrical properties of the films. Equivalent oxide thicknesses of 9 angstroms and leakages of less than $1\text{x}10^{-4}$ A/cm^2 at 1.5 V were obtained. Low hysteresis, near zero flatband voltages, and low interfacial traps illustrate the benefits of using ultraviolet assisted oxidation and nitridation of hafnium films.

2:15 PM D2.3
Characterization of High-K Nano-laminates of HfO_2 and Al_2O_3 Used as Gate Dielectrics in pMOSFETs. Dongping Wu[1], Jun Lu[2], Stefan Persson[1], Per-Erik Hellstrom[1], Elizaveta Vainonen-Ahlgren[3], Eva Tois[3], Marko Tuominen[3], Mikael Ostling[1] and Shi-Li Zhang[1]; [1]Dept. of Microelectronics and Information Technology, Royal Institute of Technology, Kista, Sweden; [2]The Angstrom Laboratory, Uppsala University, Uppsala, Sweden; [3]ASM Microchemistry Oy, Espoo, Finland.

In order to combine the merits of both HfO_2 and Al_2O_3 as high-K gate dielectrics for CMOS technology, high-K nano-laminate structures in the form of either $Al_2O_3/HfO_2/Al_2O_3$ or $Al_2O_3/HfAlO_x/Al_2O_3$ were implemented in pMOSFETs and electrically and microstructurally characterized. The nano-laminates, with a nominally 4-nm thick HfO_2 or $HfAlO_x$ sandwiched by two nominally 0.5-nm thick Al_2O_3 capping layers, were deposited on LOCOS-isolated Si substrates by atomic layer deposition (ALD). TiN films were then deposited by ALD on top of the high-K nano-laminates and served as the metal gate electrodes for the MOSFETs. After full transistor-processing including a rapid thermal processing step at as high temperature as 930 °C, the two interfaces of the high-K nano-laminates remain flat and distinct, indicating no observable occurrence of surface chemical reaction between the high-K films and Si-channel or TiN gate. The two thin capping Al_2O_3 layers were found to remain in the amorphous state for both types of the high-K nano-laminates by using high resolution transmission electron microscopy. The HfO_2 layer in the former nano-laminate, however, was found to be crystallized. In contrast, the $HfAlO_x$ layer in the latter high-K nano-laminate, remains in the amorphous state. Good capacitance-voltage (C-V) characteristics were observed for transistors with the both high-K nano-laminates. The transistor with the $HfAlO_x$ layer shows a hysteresis of 20 mV at a gate bias range of +/- 2 V, while the transistor with HfO_2 film exhibits a degraded value of 45 mV. The sub-threshold slopes for pMOSFETs with the HfO_2 and $HfAlO_x$ films were determined to be 100 and 75 mV/dec., respectively, indicating that the nano-laminate with the amorphous $HfAlO_x$ yields a substantially improved interface quality compared with the nano-laminate with the polycrystalline HfO_2.

2:30 PM D2.4
An Advanced High-k Transistor Utilizing Organic Precursors in an ALD Deposition of Hafnium Oxide and Hafnium Silicate with Ozone as Oxidizer. Jim Gutt[1], George Brown[1],

Chadwin Young[1,3], Seung Park[2] and Yoshi Senzaki[2]; [1]Sematech, Austin, Texas; [2]Aviza Technology, Scotts Valley, California; [3]North Carolina State University, Raleigh, North Carolina.

As transistor sizes continue to shrink, gate oxide thicknesses are scaling below 1.0 nm to increase the gate stack capacitance, which will allow further scaling of overall device sizes according to Moore's Law. With decreasing gate oxide thickness, however, direct tunneling becomes a major device issue as it contributes to leakage current and, subsequently, to increased standby power consumption. By increasing the permitivity of the gate dielectric, the leakage current can be reduced and the capacitance can still be scaled. Researchers have recently been studying hafnium-based high-k dielectrics as an alternative to SiO2. Further, the method of deposition often investigated has been Atomic Layer Deposition (ALD). Previous work has emphasized ALD utilizing inorganic precursors. We shall describe a process in which hafnium oxide and hafnium silicate films were deposited from alternating pulses of volatile metal-organic Hf/Si liquid precursors and ozone on 200mm diameter Si substrates using an Aviza Technology PantheonTM ALD system. Electrical characterization of the films is presented, including equivalent oxide thickness (EOT), gate leakage, and electron mobility data, showing an achievement of 1.44 nm EOT with low mA/cm2 Jg and high field mobility equal to 74% of that of SiO2 (2.2 nm film).

3:15 PM *D2.5
Limitations of poly-Si gated CMOS devices with high-k gate dielectrics. Eduard Albert Cartier, Research Division, IBM, YORKTOWN HEIGHTS, New York.

Finding a suitable replacement for SiO_2 as the gate dielectric in CMOS devices appears to be a precondition to continue conventional device scaling. Without replacing SiO_2, the power consumption due to gate leakage becomes unacceptably large in scaled devices. It would be in the industry's interest to only replace the SiO_2 gate oxide, such that the established self-aligned CMOS manufacturing process, which uses n- and p-doped poly-Si gate electrodes for the nFET and pFET, respectively, can be used with minimal changes. However, concerns are increasing that the selected high-k materials are incompatible with the established manufacturing process and that the successful introduction of high-k dielectrics may require more substantial changes, such as simultaneously replacing the n- and p-doped poly-Si gate electrodes by metals. In this presentation, the electrical performance of CMOS devices with high-k gate dielectrics and poly-Si gates will be reviewed. Three major challenges can be identified: 1) Accurate control of the transistor threshold voltage is difficult. Threshold voltage control is particularly poor for the p-FET with Hafnium based dielectrics. 2) The channel mobility is reduction with a high-k dielectric in the gate stack. The mobility degradation is generally more severe for the nFET, especially for aggressively scaled devices with minimized SiO_2 buffer layers between the Si substrate and the high-k dielectric. 3) The threshold voltage stability during device operation is reduced. Charge trapping in the Hafnium based high-k dielectric causes large threshold voltage instabilities primarily in nFET. Extensive process optimization and materials modifications have provided partial solutions for some of these issues. However, it remains challenging to realize an aggressively scaled high-k gate stack with poly-Si electrodes that overcomes all limiters simultaneously. Some of the discussed difficulties may be fundamentally tied to the properties of the selected gate materials.

3:45 PM D2.6
Effect of Structural Defects on Hf-Based Gate Stack Transistor Performance. Gennadi Bersuker, Chadwig Young, Joel Barnett, Naim Moumen, Jeff Peterson, Patrick Lysaght, George A Brown, Peter M Zeitzoff, Mark Gardner, Robert W Murto and Howard R Huff; International SEMATECH, Austin, Texas.

Aggressive transistor scaling required to achieve higher drive current calls for an equivalent electrical thickness (EOT) of the gate dielectric less than 1 nm as well as a low gate leakage current. These conditions cannot be supported by the conventional SiO2 dielectric. On the other hand, transistors built with the high-k gate dielectric, which can provide both low EOT and low leakage current, usually exhibit low drive currents. In this presentation, we analyze several structural features of the high-k films, which may contribute to the degradation of transistor performance. The presence of electron traps may lead to the loss of the inversion charge in the channel. Reduction of the charge would be interpreted as a degradation of the channel mobility. By applying a fast transient measurement technique to the transistors manufactured with various HfSiO dielectric thicknesses, it was demonstrated that trapping occurs on a very small time scale as compared to DC measurements, manifesting itself as a mobility reduction. The data suggest that the bulk high-k traps, rather than the traps located at the high-k/SiO2 interface, are responsible for the inversion charge loss. Coulomb scattering by the fixed charges in the high-k gate dielectric located in close proximity to the interface with the substrate can reduce the carrier mobility. From the Vfb dependence on EOT for a wide range of the dielectric thicknesses, we found a significant difference between the interface charge of the ALD and MOCVD Hf-based dielectrics, higher interface charges correlating to lower mobility in the corresponding samples. At the same time, both charge pumping and DC-IV data do not show any significant difference between the interface state densities of these gate stacks, indicating that the interface states are not responsible for the observed degradation of the carrier mobility. In the set of Hf-silicide samples with 20% SiO2 deposited on the thermally grown SiO2 layers in the range of 0.9 nm to 0.4 nm, the final (post-processing) interfacial SiO2 thickness was electrically estimated to increase by 0.1 nm to 0.3 nm. This small increase of the process-grown SiO2 thickness correlates to mobility degradation, which may be caused by the low quality of this thin process-grown sub-layer formed during the high-k deposition process at temperatures as low as 300C. Structural non-uniformity in the high-k gate dielectric, which may be associated with the random grain orientation of the crystallized high-k film, or compositional non-uniformity of the silicate films caused by phase separation, or non-uniformity of the interfacial oxide thickness, results in the non-uniformity of the vertical electric field in the transistor channel that may suppress carrier mobility. This non-uniformity effect increases for the thinner interfacial SiO2 layers and higher k values of the gate dielectrics.

4:00 PM D2.7
Dielectric Breakdown Characteristics of HfAlOx/SiON gate stack. Kazuyoshi Torii[1], Hiroshi Ohji[1], Takaaki Kawahara[1], Riichiro Mitsuhashi[1], Atsushi Horiuchi[1] and Seiichi Miyazaki[2]; [1]Semiconductor Leading Edge Technologies, Tsukuba, Ibaraki, Japan; [2]Hiroshima university, Higashi-Hiroshima, Hiroshima, Japan.

Hf based oxide thin films with high dielectric constant (high-k) have been intensively studied because of their potential use as alternative gate dielectrics. The integration of HfAlOx gate dielectrics into sub-100 nm FET has already been demonstrated; however, there are few reports on the reliability of HfAlOx. In this study, we investigate the dielectric breakdown behavior of CMOSFETs with HfAlOx gate dielectric fabricated using mass production worthy 300 mm process. The Poly-Si gate FETs were made using standard CMOS process adapted to high-k gate stack. The HfAlOx thin film was deposited by ALD on a wafer with an intentionally formed interfacial layer (IL). Because of higher crystallization temperature (>1000°C), the Hf content of less than 30% was selected. The uniformity of the Hf concentration is ±1.8% and that of the optical thickness is ±2.5% over a 300 mm wafer. The gate leakage depends little on the temperature and it shows a good linearity in a F-N plot under higher gate voltage. The time dependent dielectric breakdown (TDDB) behavior was examined using constant voltage stress. If SiO_2 is used as an IL, the IL reduction and the intermixing between the HfAlOx layer and the IL occurred, which makes the IL thickness variation larger. In the TDDB measurements, it causes extrinsic breakdown resulting in lower Weibull slope. By using the SiON as an IL, the interfacial reaction can be suppressed and the extrinsic breakdown component can be eliminated even if the post process temperature is as high as 1000°C. In the case of gate injection, abrupt increase of gate leakage was observed, and gradual increase is followed after that. Using either E-model or 1/E model, the MTTF (for $0.1cm^2$ at 125°C) is long enough. On the other hand, gate leakage starts to increase gradually at a certain stress period without abrupt jump in the case of substrate injection. Therefore, it is difficult to determine the time to breakdown, T_{BD}. If we define the T_{BD} at the onset of leakage current increase, the MTTF would be only 3.7 years if it obeys the E-model (MTTF predicted by 1/E-model was 1.6×10^7 years). In order to discuss the mechanism of the TDDB, the band diagram was examined using XPS. The band gap and the valence band offset of HfAlOx are determined to be 6.5eV and 3.6eV, respectively. This band alignment suggests that the leakage current is restricted by the IL in the case of the substrate injection while it flows through both HfAlOx and IL in the case of the gate injection. The mechanism of TDDB is not clear at the moment; however, we would interpret the results in the context that the gradual increase in the leakage is due to the HfAlOx wear out whereas the life of the HfAlOx/SiON gate stack is mainly determined by the IL.

4:15 PM D2.8
Electrical breakdown in a two-layer dielectric in the MOS structure. Xiaolong Yang[1], Qianghua Xie[2] and Meng Tao[1]; [1]Department of Electrical Engineering, University of Texas at Arlington, Arlington, Texas; [2]Process and Materials Characterization Laboratory, Motorola Inc, Tempe, Arizona.

The formation of interfacial oxide between high-k and Si creates a two-layer dielectric in the MOS structure. In this talk, we present a model to describe electrical breakdown in the two-layer dielectric. The leakage current through the two-layer dielectric shows three regimes with applied voltage: both layers intact, one layer breakdown, and

both layers breakdown. Accordingly, three conduction mechanisms are presented for the three regimes: tunneling through two layers, tunneling through one layer, and hard breakdown for both layers. Our model has been compared with experimental data obtained from the HfO_2/SiO_2 MOS structure, and good agreement is achieved. This model can be used to estimate either the thickness, breakdown field, or dielectric constant of each of the two dielectric layers. It can also predict the overall breakdown field for different combinations of dielectric layers. When combined with C-V measurements, more information about the two-layer dielectric is obtained.

4:30 PM D2.9
Physical impact of a high-temperature post-nitridation anneal on advanced plasma nitrided gate dielectrics (45nm to 65nm technologies). Maud Bidaud[1], Jerome Bienacel[2], David Barge[1], Nicolas Emonet[2], Francois Guyader[2], Lucky Vishnubhotla[3] and Kathy Barla[2]; [1]Philips Semiconductors R&D, Crolles, France; [2]STMicroelectronics, Crolles, France; [3]Motorola, Crolles, France.

It is common knowledge that the continued scaling of CMOS devices will require the integration of high-K gate dielectrics in the very near future. However, extensive screening of high-K material properties still shows a number of unresolved issues, and their integration into the 45nm platform remains uncertain. Consequently, the downward extension of plasma nitrided gate oxides is being actively pursued. Typically, plasma processes are performed in three serial steps including a thermal pre-oxidation, the nitrogen incorporation and a high temperature post-nitridation anneal. In this paper, we propose simple physical models for understanding the nitrogen incorporation and distribution after each individual step. Several in-line techniques such as X-ray photoelectron spectroscopy (XPS), second ion nitrogen profiling (SIMS) and delay-to-reoxidation are used to estimate the concentration and location of nitrogen species. We show that nitrogen atoms are chemically implanted into the bottom oxide prior to diffusing down to the silicon-oxide interface. Oxidizing (O2) and neutral (N2) anneals are processed at various temperatures from 500C to 1000C, and the specifics of each is detailed. Using this knowledge, the need for a post-nitridation anneal is discussed in terms of dielectric film stability. We show that annealing plasma nitrided oxides at a high temperature allows an efficient reorganization of nitrogen bonds in the silica lattice, with interfacial Si-N-(O)2 unstable bonds turning into N-(Si)3 stable bonds. The nitrogen dose incorporated in annealed and un-annealed oxides is also monitored with time, showing that a significant amount of nitrogen is released in the ambience when the films are not annealed. This parasitic outgasing is directly correlated to the local concentration of nitrogen at the dielectric top surface, and can lead to nitrogen dose non-repeatability in the case of non-clustered nitridation-anneal sequences. Finally, previous results are compared with end-of-line characteristics from 1.7-2.1nm CET (Capacitance Equivalent Thickness) plasma nitrided oxides. The effect of the high temperature anneal on the gate leakage vs. CET trend is reviewed for various process conditions. Its impact on the device effective mobility and on the dielectric reliability is discussed as well.

4:45 PM D2.10
Study of pulsed RF DPN process parameters for 65 nm node MOSFET gate dielectrics. Aude Rothschild[1], P A Kraus[2], T C Chua[2], F Nouri[2], Florence N Cubaynes[3], Anabela Veloso[1], Sofie Mertens[1], Lucien Date[4], Rob Schreutelkamp[4] and Marc Schaekers[1]; [1]IMEC, Leuven, Belgium; [2]Applied Materials Inc., Sunnyvale, California; [3]Philips Research Leuven, Leuven, Belgium; [4]Applied Materials Belgium, Leuven, Belgium.

Balancing between gate leakage current, device performance and gate dielectric reliability is a major challenge when using oxynitrides (SiOxNy) as gate dielectric layer in advanced MOSFET technology. Compared to furnace nitridation, plasma nitridation techniques - Remote Plasma Nitridation (RPN), Decoupled Plasma Nitridation (DPN), and pulsed-RF DPN (pRF-DPN) - have demonstrated reduction in Equivalent Oxide Thickness (EOT) and gate leakage current (Jg) by incorporating a higher concentration of nitrogen atoms into the dielectric film. However, nitrogen incorporation leads typically to channel mobility degradation and threshold voltage shift (Vt), especially for pMOSFET devices. Although improvements of the plasma nitridation techniques have alleviated these issues, control of the incorporation of nitrogen remains a challenge in order to meet the ITRS specifications for the 65 nm technology node. In order to understand how the nitrogen plasma conditions impact on the incorporation of nitrogen species into the film, tuning of each individual pRF-DPN process parameter was performed: peak power, duty cycle (DC), frequency (f), process time and some cross-combinations (DC and f, DC and process time). The plasma and the dielectric film were characterized using respectively Langmuir probe analysis (LP), X-ray Photo-electron Spectroscopy (XPS) and Delay to Reoxidation (D2R) techniques. The correlation between density and energy of the charged species in the pRF-DPN nitrogen plasma versus physical thickness and nitrogen concentration was thus established. The results indicate that effective power (peak power*DC) and DPN process time are the two key parameters determining the physical characteristics of the SiOxNy film. From the combination of DC and DPN process time, the importance of the off-time portion of the pulse was revealed. With the help of a modified pRF DPN generator allowing to decrease the frequency below 10kHz, electrical evaluation was performed at an EOT of 1.2 nm. It was demonstrated that when decreasing the frequency down to 2kHz, the electrical performance of the devices is improved by 5%.

SESSION D3: Poster Session: High-k and Ferroelectric Layers
Chairs: Michel Houssa and Bob Wallace
Tuesday Evening, April 13, 2004
8:00 PM
Salons 8-9 (Marriott)

D3.1
Room temeprature formation of TiO2 thin films by using UV-enhanced atomic layer deposition. Yong J. Kwon, Young J. Jang and Myung Mo Sung; Chemistry, Kookmin University, Seoul, South Korea.

We have deposited TiO2 thin films on Si substrates at room temperature by UV-enhanced atomic layer deposition (ALD) with titanium isoproxide and water as the precursor. The ALD is a gas-phase thin film deposition method by using self-terminating surface reaction. The ALD method relies on sequential saturated surface reactions which result in the formation of a monolayer in each sequence. in may cases, however, the surface reactions in ALD are not complete at low temperatures. In this study, the surface reaction in the ALD of the TiO2 thin film was enhanced by using UV irradiation at room temperature. The structure, chemical composition, morphology, and thickness of the TiO2 thin films were investigated by XRD, XPS, AFM, UV, and TEM.

D3.2
Pulsed laser deposition of high dielectric constant oxide films on silicon. Valentin Craciun[1], Chad Essary[1], Nabil D Bassim[2] and Rajiv K Singh[1]; [1]Materials Science and Engineering, University of Florida, Gainesville, Florida; [2], Naval Research Laboratory, Washington, District of Columbia.

High-k oxides have recently become the focus on intense research as replacements in advanced MOS devices of the extremely thin SiO2 gate oxides. Pulsed laser deposition (PLD), although not a microelectronics production tool, is one of the best techniques for the growth of high quality complex oxide thin films for conducting rapid investigations of deposited oxides properties and their chemical interactions with the substrate or the gate material. One of the main problems encountered during PLD of high-k dielectrics directly onto Si samples, as well as other investigations using different growth techniques, is the formation of an unwanted interfacial layer at the interface with the Si substrate. Even though the grown oxides were found to exhibit excellent electrical properties such as high dielectric constants, the presence of this interfacial layer diminishes this advantage for the resulting structure. We have investigated the oxygen source and the kinetics of the interfacial layer growth during deposition and thermal treatments of HfO2, Y2O3 and ZrO2 layers on Si. Several techniques having nanometer scale resolution were employed to elucidate the interfacial layer complex chemistry and growth kinetics. The positions and shape of the metal, oxygen and Si XPS peaks suggest that at the temperatures used for deposition (< 650 deg.C) the SiO2 layer is physically mixed with the deposited oxide layer without forming silicate compounds. X-ray reflectivity and cross-section transmission electron microscopy investigations confirmed the presence of the interfacial layer, whose density was found to be higher than that of pure SiO2 but lower than that of the corresponding silicate, corroborating the XPS results. New processing routes using ultraviolet-assisted low temperature conditioning of the Si substrate prior to deposition to reduce interfacial layer thickness and optimize the electrical characteristics of the grown structures will be also presented.

D3.3
Surface Modification for Area-Selective Atomic Layer Deposition. Rong Chen[1], Hyoungsub Kim[2], Junsic Hong[3], Paul C. McIntyre[2] and Stacey F. Bent[3]; [1]Department of Chemistry, Stanford University, Stanford, California; [2]Department of Material Science and Engineering, Stanford University, Stanford, California; [3]Department of Chemical Engineering, Stanford University, Stanford, California.

Gate dielectrics with permittivities greater than that of SiO2 are required to continue the downward dimensional scaling of MOSFET devices. Among many possible deposition techniques, atomic layer

deposition (ALD) is very promising for preparing high-κ dielectric materials because it can produce high quality films with excellent conformality and precise film thickness control. While ALD inherently provides nano-scale control of materials in the vertical direction, we are investigating an area-selective ALD technique that will enable nano-scale definition of the lateral structure. Our research emphasizes controlling the substrate surface chemistry in order to impart spatial selectivity to ALD. Availability of area-selective ALD processes for the application of gate dielectric and gate electrode deposition could substantially reduce the number of lithography, etch, and cleaning operations required for integrated circuit fabrication. We are taking a two-pronged approach to generate a patterned substrate in which certain well-defined regions have been "primed" for deposition and others have been "deactivated". We have focused mainly on HfO2 and ZrO2 as the high-κ gate dielectric layers in the ALD process because of their compatibility with conventional metal-oxide-semiconductor device processing. We will show that well-controlled self-assembled monolayers (SAMs) are efficient deactivating agents to block HfO2 and ZrO2 growth by ALD. A series of SAMs of organosilanes have been investigated as deactivating agents for the HfO2 ALD process. Three important factors for the quality of SAMs formation–molecular chain length, reactivity and steric effect–were studied by water contact angle (WCA) measurement, ellipsometry, X-ray photoelectron spectroscopy (XPS), transmission electron microscopy (TEM) and atomic force microscopy (AFM). The effect of these factors on ALD deactivation was investigated by a combined XPS, TEM and AFM analysis. We find that it is crucial to choose deactivating agents with high reactivity, low steric effects and certain chain length in order to form condensed, highly hydrophobic film for the deactivation. The analysis provides insight into the mechanism of the deactivation and ALD growth. The area-selective ALD approach is, in principle, quite general and could be applied to many other materials or varieties of shapes and surfaces in the future. Moreover, an area-selective ALD process, which reduces the number of patterning and etching steps by depositing materials only where they are needed, would be particularly useful for fabrication of expensive materials, fabrics that are difficult to be etched away, processes that required non-residual contaminations, non-planar MOSFETs and other complex nano-devices.

D3.4

Atomic Layer Deposition of Zirconium oxide and Hafnium Oxide from novel metal-organic precursors. Juntae Kim and sangman Koo; Chemical Engineering, Hanyang University, Seoul, South Korea.

High-k metal oxides are sought-after for a variety of applications in the electronic industry.To meet the demand of preparation of these materials in a manner compatible with conventional Si-based processes,Atomic layer deposition(ALD) is desired for film growth. In this study, thin films of ZrO_2 and HfO_2 have been depostied by ALD using novel metal-organic precursors,[$M(macact)_2(ONeop)_2$]in the temperature range of 300-500°C on silicon substrate :(macact=methyl acetoacetate ;neop=neopentyl ; M=Zr,Hf). The films were characterized by a combination of transmission electron microscopy,Auger spectrometry ,atomic force microscopy and X-ray diffractometery.

D3.5

Optical Properties of Hafnium Oxide Films Grown by Laser Assisted Molecular Beam Deposition. Lianchao Sun[1], James F Garvey[2], Robert L DeLeon[2], Gary S Tompa[2], Richard Moore[3] and Harry Efstathiadis[3]; [1]SOPRA Inc, Westford, Massachusetts; [2]AMBP Tech Corporation, Amherst, New York; [3]School of NanoSciences and NanoEngineering, University at Albany-SUNY, Albany, New York.

Hafnium oxide thin films have successfully been deposited on silicon substrates by Laser Assisted Molecular Beam Deposition (LAMBD). The films were grown at the substrate temperature of 300 ?C and 27 oC at process pressure 1 Torr. The LAMBD process uses a pulsed laser to create hot plasma to ablate material from a rotating hafnium target rod. Oxygen was used as the carrier gas to entrain the ablated material in a cooling expansion process. The choice of carrier gas exerts considerable control over the process; it can control both the chemical composition and the temperature of the ablation plasma.. Depositions yielded controlled thickness of 5 nm to 100 nm of stoichiometric HfO2 films. In this work the film microstructure will be compared to the microstructure of films deposited by LAMBD at room temperature. Optical characterization of high dielectric constant (k) hafnium oxide (HfO2) was performed by means of spectroscopic ellipsometry (SE) and grazing x-ray reflectivity (GXR) measurements. The thickness is obtained with absolute GXR technique for very thin films and the optical constants are calculated from ellipsometry measurement. The relationship between microstructure and their optical properties will be discussed in this paper.

D3.6

Thermal stability of amorphous praseodymium silicate films on silicon. Raffaella Lo Nigro[1], Graziella Malandrino[2], Roberta Toro[2], Vito Raineri[1] and Ignazio Luciano Fragala'[2]; [1]sezione di Catania, IMM-CNR, Catania, Italy; [2]Dipartimento di Scienze Chimiche, Universita' di Catania, Catania, Italy.

New dielectric materials with sufficiently high permettivity are needed as future insulators to replace SiO2 in complementary metal oxide semiconductors (CMOS) devices. Praseodymium silicate amorphous films can be an interesting alternative. We have investigated the effect of the thermal annealing on praseodymium silicate films obtained by Metal Organic Chemical Vapor Deposition (MOCVD). Praseodymium silicate films have been obtained at 750 C using the Pr(tmhd)3 [(H-tmhd=2,2,6,6-tetramethylheptane-3,5-dione)] precursor. Their structural characterisation have been performed by X-ray diffraction (XRD) as well as by transmission electron microscopy (TEM) analysis. Both investigation have demonstrated that as-deposited praseodymium silicate films are amorphous. Evidence of the thermal stability of the praseodymium silicate films has been obtained by post annealing processes. In fact it is well known that one of the most critical issue, for the implementation of new dielectrics in substitution of silicon oxide, is their structural and chemical stability against the thermal processes during the fabrication of MOSFET devices. In this context, the thermal stability of the deposited films have been tested by two different annealing processes: Rapid Thermal Annealing (RTA) and long ramped annealing in a furnace, in order to evaluate time dependence of praseodymium silicate thermal stability. The influence of the process atmosphere has been fully investigated and the praseodymium silicate has been found to be stable up to 900 C in argon or nitrogen controlled atmosphere. In fact, their XRD spectra have shown no peaks as in the as-deposited film patterns, thus indicating that no other phases are formed upon heating and, consequentially, that the praseodymium silicate phase is thermally stable. Moreover, no changes occurred on film morphologies as assessed by TEM analyses. However evidence of crystallisation processes have been detected at 800 C in oxygen environment. In fact, the XRD patterns have shown some of the most intense reflections that are characteristics of the stoichiometric Pr8Si6O24 phase. TEM cross section images have clearly shown that praseodymium grains morphology have changes and rounded grains 100 nm large have formed. These results imply significant oxygen diffusion through the praseodymium silicate dielectric layer during the thermal treatment at 800 C, however it has demonstrated not to suffer of any structural and compositional variation up to 900 C in controlled atmosphere.

D3.7

Determination of nitrogen concentration of oxynitride gate dielectric films by using spectroscopic ellipsometry. Yong Jai Cho, Hyun Mo Cho, Hyun Jong Kim, Won Chegal and Yun Woo Lee; Department of Optical Metrology, Korea Research Institute of Standards and Science, Daejeon, South Korea.

We have applied spectroscopic ellipsometry (SE) to investigate a set of lightly nitrided silicon dioxide films and to correlate their optical properties with the nitrogen concentrations of the films. Silicon oxynitride is an intermediate solution for high-k gate dielectrics in present and future ultralarge-scale-integrated (ULSI) devices. Advantages of oxynitrides as a gate dielectric in the ULSI devices improve hot carrier reliability with a little nitrogen at Si-SiO2 interface and prove a diffusion barrier for boron in poly-silicon gate, and reduce tunneling currents. Therefore, in the future ULSI technology, it will be needed to evaluate the reliability in measurements of the thickness and nitrogen concentration of ultrathin oxynitride film. Ultrathin oxynitride films were grown on Si substrate by NO thermal deposition and then annealed at a high temperature. SE measurements were performed on a spectroscopic ellipsometer. The dielectric functions of these films were determined by using widely used dispersion models and Bruggeman effective medium approximation, respectively. It will be shown which model can be used to effectively describe the optical properties of the ultrathin oxynitride films. We will also show that SE can easily and quickly quantify the nitrogen concentration of oxinitride films without employing a more elaborate method such as a medium energy ion scattering spectroscopy (MEIS).

D3.8

Effects of Annealing on the Mechanical and Electrical Properties of DC Sputtered Tantalum Pentoxide (Ta_2O_5) Thin Films. Jaya Murli Purswani[1], A P Pons[1], J T Glass[2,1], R D Evans[3,1] and J D Cogdell[3]; [1]Chemical Engineering, Case Western Reserve University, Cleveland, Ohio; [2]Electrical and Computer Engineering, Duke University, Durhan, North Carolina; [3]The Timken Company, Canton, Ohio.

Variations in annealing temperature alter the physical, materials, and electrical properties of tantalum pentoxide (Ta_2O_5) thin films. In this

experiment, Ta_2O_5 films were deposited onto p-type silicon substrates using reactive DC magnetron sputtering. This study examines the effect of varying the annealing temperature on the film properties. Samples were annealed for one hour in a dry air ambient at temperatures of 730°C, 780°C, and 830°C. Mechanical properties examined include stress, hardness, elastic modulus, and surface roughness. Annealing is shown to reduce stress, and results in compressive stress for samples annealed at 730°C. Samples annealed at 780°C and 830°C were tensile, but were on the order of 100 MPa lower in stress than the as-deposited samples. Elastic modulus did not vary significantly. Hardness values were approximately 7 GPa, with the exception of the sample annealed at 780°C which demonstrated a hardness of 12 GPa. Surface roughness was lowest for the as-deposited samples. For the annealed samples, a minimum was observed at 780°C, with surface roughness increasing for samples annealed at 830°C. Electrical properties studied were leakage current, breakdown field, resistivity, and dielectric constant. Leakage current generally improved with annealing, especially at the lower temperatures; electrical breakdown was observed for as-deposited and the 830°C annealed film. Resistivities of the films were 6.5×10^9 to 6.1×10^{12} ohm-cm, with the film annealed at 830°C being the most conductive. Annealing also led to an increase in dielectric constant up to 780°C, before decreasing at 830°C. Dielectric constants varied from 7.7 for the as-deposited to 19.1 for the 780°C annealed sample.

D3.9

TiO2-based Tunneling Transistors on Silicon Substrates.
Ashkan Behnam, Bahman Hekmatshoar, Shams Mohajerzadeh, Behnaz Arvan, Farshid Karbasian and Ebrahim Asl-Soleimani; Electrical and Computer Engineering Deptartment, Univ. of Tehran, Tehran, Iran.

We have successfully fabricated tunneling transistors on Si substrates based on TiO_2 insulator films. The structure used for such transistors is a sandwich of Ni-Si/TiO_2/Ni-Si/TiO_2 layers with the thickness of 100Å/150Å/30Å/150Å on an n-type (100) Si substrate. All deposition steps were carried out consecutively in a single run using a multi-target RF-sputtering system at a base pressure of 10^{-6}torr. A mesa structure was realized by chemical etching to form the top emitter, intermediate base and bottom collector regions. Also the intermediate Ni-Si layer acts as the contact to the intrinsic base. The voltage applied between the top emitter and the base silicide layers sets the level of electrons tunneling through the top TiO_2 film to form the emitter current. Part of the electrons that pass through the base silicide layer can pass over the bottom oxide and make the collector current. In this configuration, "β" is defined as the ratio of the collector current to the base one and it has been found to be around 11 with an emitter current of 2mA. From the electrical characteristics of the device, one can observe a "kink" in the current-voltage behavior of the transistors. This "kink" occurs when the base current becomes minimal and "β" rises. We believe that the titanium dioxide layer deposited using RF-sputtering does not possess good quality in terms of leakage current and stoichiometry, leading to higher base currents. To improve the quality of the TiO_2 layers and achieve better devices, we have developed a low temperature, atmospheric pressure chemical vapor deposition (APCVD) of TiO_2 films using a mixture of $TiCl_4$ and O_2. The presence of H_2O_2 during the deposition of the oxide significantly improves the electrical and crystalline quality of the TiO_2 layers as confirmed using XRD, SEM and FTIR spectroscopy tools. H_2O_2 is believed to be an additional source of oxygen radicals, enhancing the growth conditions and yielding high quality films. Also the electrical quality of the insulating layer was examined by means of fabricating MOS capacitors on p-type (100) Si substrates. The films are grown at temperatures ranging from 150 to 300°C. The films grown at 170°C in the presence of H_2O_2 show a leakage current density of 10^{-8}A/mm^2, a breakdown filed of 10^7V/cm, and a relative permittivity of 19 to 21. Also from the capacitance-voltage (C-V) characteristics a threshold voltage of 1 volt is measured for the MOS structure. Since the growth temperature of the oxide film is as low as 150°C, one can possibly use a plastic substrate in place of the silicon base. The fabrication of the TiO_2-based tunneling transistors on polyethylene terephthalate (PET) plastic substrates is being carried out and the electrical characterization of the devices is currently underway. We speculate that such transistors may be used as high performance switches for flexible electronic applications.

D3.10

Leakage current behavior in CaZrO3 thin films for high-k applications.
Ting Yu, weiguang Zhu, xiaofeng Chen and yuekang Lu; Microelectronics Center, school of Electrical and Electronic Engineering, Nanyang Technological University, Singapore, Singapore.

Electrical properties and leakage current mechanisms of perovskite CaZrO3 dielectric thin films have been studied in this paper. CaZrO3 thin films were deposited on Pt/SiO2/n-Si substrate by the sol-gel wet chemical technology, and then annealed at temperatures ranging from 550 to 700 °C for 1h in O2. The films with platinum (Pt) top and bottom electrodes were characterized with respect to the leakage current as a function of temperature and applied voltage. It showed good electrical properties in terms of a dielectric constant of about 20 and leakage current density of 10^{-7} A/cm2 at high applied electrical field 2.6 MV/cm. The data can be interpreted via a thermionic emission model. The conduction mechanism at low electric fields is due to Ohmic conduction. On the other hand Schottky mechanism dominates at the intermediate fields. The high dielectric constant, low leakage current density and high breakdown strength suggest that the CaZrO3 thin film is a promising candidate for high-k applications.

D3.11

Engineering the nm-thick interface layer formed between TaOx high k film and silicon substrate.
Yue Kuo and Jiang Lu; Thin Film Nano & Microelectronics Research Laboratory, Texas A&M University, College Station, Texas.

Tantalum oxide (TaOx) is a promising high-k gate dielectric material to replace thermally grown SiO2 in the sub 0.1 micrometer technology node. However, TaOx forms a low quality interfacial layer when it is in contact with silicon [1]. Previously the authors reported that when Ta2O5 was doped with Hf, several advantages were obtained: increasing the amorphous-to-polycrystalline transition temperature, improving interface layer quality, and enhancing the k value [2]. When a 5 angstrom tantalum nitride (TaNx) was inserted between the Hf-doped TaOx and silicon, many of the film dielectric properties were further improved [3]. Effects of Hf doping process and the insertion of the ultra-thin TaNx layer on the interfacial layer material and electrical property changes after a high temperature annealing step had not been systematically studied, previously. In this paper, we investigate these subjects with advanced thin film analytical instruments, such as SIMS, ESCA, TEM, and IV/CV measurements on the fabricated MOS capacitors. The following results have been obtained: 1) the Hf dopant in the TaOx film was involved in the interface formation process, e.g., forming a new, thinner high-k HfSixOy interface layer than the SiOx layer. 2) when the TaNx interface was inserted, the interface further changed, e.g., by forming new TaOxNy and HfSixOy compounds. No hafnium nitride or oxynitride was detected. 3) the interface layer structure was changed, e.g., from single-zone to multi-zone with various compositions. 4) when a low concentration of Hf existed in the TaOx film, most of the dielectric properties, such as the k value, fixed charge density, dielectric strength, were improved. 5) when the thin TaNx interface layer was inserted, the above electric properties were further improved. However, the fixed charge density and interface states were increased. However, the high temperature annealing step lowered these values. Above results were due to the inclusion of nitrogen into the interface layer and the repairing of damaged bonds. In summary, the interface layer structure and properties of the TaOx high-k film were improved with the doping process and the insertion of an ultra-thin TaNx interface film. This research is partially supported by NSF DMI-0243409 and DMI-0300032 projects. [1] K. J. Hubbard and D.C. Schlom, J. Mater. Res 1996; 11: 2757-2776. [2] J. Lu, J. -Y. Tewg, Y. Kuo, and P. C. Liu, ECS Proc. 1st Intl. Symp. High Dielectric Constant Materials: Materials Science, Processing, Manufacturing, and Reliability Issues, PV 2002-28, pp 105-112, 2003. [3] Y. Kuo, J. Lu, and J.-Y. Tewg, Jpn. J. Appl. Phys., 42(2), 7A, L.769-771, 2003.

D3.12

Effects of Al_2O_3 layer thickness in Al_2O_3/HfO_2 gate oxide deposited by Atomic Layer Deposition Method.
Myungjin Park, Jaehyoung Koo and Hyeongtag Jeon; Division of Materials Science and Engineering, Hanyang Univ., Seoul, South Korea.

As the metal-oxide-semiconductor (MOS) device is scaled down to the sub-micrometer, the high-k dielectrics are needed as new gate oxide materials. Among the various high-k dielectric candidates, HfO_2 and Al_2O_3 have been mainly investigated due to their large band gap, good thermal stability, and relatively higher dielectric constant compared to SiO_2. For these reasons, HfO_2 is expected to replace SiO_2 as an alternative high-k (k=2530) gate oxide in MOSFET. But, even though HfO_2 has a lot of advantages over other high-k dielectrics, it has also problems to solve such as, high leakage current and undesired interfacial layer. According to earlier reports, this interfacial layer causes lowering dielectric constant and flat band voltage shift. Al_2O_3 is one of materials, which exhibits the amorphous phase in contact with Si substrate. And this material is considered to be very effective to stop the diffusion of hydrogen and oxygen atoms. In this study, we used this Al_2O_3 material to prevent interfacial layer formation. To investigate the effects of Al_2O_3 thickness, we deposited various thicknesses of Al_2O_3 and followed by HfO_2 deposition by atomic layer deposition (ALD) method. This ALD method is already known as one of the method to deposit very thin film precisely and high quality films. With this experiment, we investigated the HfO_2 formation depending on the thickness of Al_2O_3 interfacial layer. The physical and chemical properties of Al_2O_3/HfO_2 films were analyzed by high-resolution transmission electron microscope (HRTEM), X-ray

photoelectron spectroscopy (XPS) and Auger electron spectroscopy (AES). The electrical properties were calculated and analyzed by using capacitance-voltage (C-V) and current density-voltage (J-V) measurements. Characteristics of Al_2O_3/HfO_2 films will be discussed based on the results mentioned above.

D3.13
Reduction of CV Histeresis in Metal/High-k MISFETs Using Flash Lamp Post Deposition Annealing. Takeo Matsuki, Yasushi Akasaka, Kiyoshi Hayashi, Masataka Noguchi, Koji Yamashita, Hideyuki Syoji, Kazuyoshi Torii, Naoki Kasai and Tsunetoshi Arikado; Reserch Dept. 1, Semiconductor Leading Edge Tech. Inc., Tsukuba-shi, Ibaraki-ken, Japan.

HfAlOx is one of the candidate for high-k dielectric for high performance MISFETs, though large CV hysteresis has been observed in poly-Si/HfAlOx stacked MISFET with high temperature annealing, at over 1000°C, for PDA and dopant activation. By using the damascene or replacement metal gate process, the high temperature process after high-k deposition can be avoided. On the contrary, the thermal budget of the PDA should be low because thermally unstable NiSi on S/D for high performance LSI was formed before high-k deposition. Flash lamp is a strong candidate for very short time heating process compared with conventional RTA process. In this work, we investigated electrical properties of flash lamp annealed HfAlOx using n/p-MISFET with W/TiN/HfAlOx/SiO_2 gate stack, where these films were formed after source/drain formation and the activation. A 2.5 nm-thick HfAlOx was deposited on a 1nm-thick SiO_2 by atomic layer deposition(ALD) at 300°C. The Hf concentration, Hf/(Hf+Al), was 0.3. For the flash lamp PDA, the wafer was set on the stage held at RT - 500°C, and was irradiated with energy density of 24-27 J/cm ^{2} in 0.6-0.8 msec. High temperature PDA at 1050°C was carried out for reference samples with poly-Si and W/TiN gate electrode. W and TiN was deposited by CVD at 100nm and 10nm respectively. The samples with poly-Si gate electrode were annealed at 1000°C for 3sec after the gate patterning for the gate dopant activation. The EOT value of the reference sample with W/TiN was 1.5nm. CV hysteresis of the poly-Si and W/TiN gate reference samples was approximately 50mV at the inversion and 20mV at the accumulation in nMISFET. This asymmetry was observed in the W/TiN gate reference samples too. In pMISFET, hysteresis at the accumulation was lager than that at the inversion. These results and the direction of the hysteresis loop suggest that origin of the hysteresis is electron injection from substrate or electrode. In the case of the substrate injection, the amount of injected electron is limited by the interfacial SiO_2 , resulting in lager hysteresis at the inversion in nFET or at the accumulation in pFET. Using flash lamp PDA for the W/TiN gate, CV hysteresis in TiN/HfAlOx/SiO_2 n/pMISFETs was minimized to less than 10mV by 26J/cm2 and 220°C-stage-temperature at both the inversion and the accumulation. Even though the flash lamp PDA was applied, the high temperature activation for the poly-Si gate caused a hysteresis about 100mV. The lower thermal budget achieved by the flash lamp annealing and metal gate is effective to suppress the interfacial reaction which causes the traps responsible for the hysteresis.

D3.14
High-k (ZrO_2, HfO_2) Dielectrics on Si Substrates Synthesized by Elevated Temperature UV-Ozone Oxidation Technique. Kang-ill Seo[1], Paul C. McIntyre[1] and Krishna Saraswat[2]; [1]Materials Science & Engineering, Stanford University, Stanford, California; [2]Electrical Engineering, Stanford University, Stanford, California.

Recently, there has been a significant effort in developing high-k metal oxide materials such as ZrO_2 and HfO_2 to replace SiO_2 as the gate dielectric in future CMOS devices. Among many methods to grow high-k dielectrics, the UV-ozone oxidation (UVO) technique has shown potential for growing high quality thin films at room temperature. UVO processing also avoids incorporation of impurities related to incomplete reaction of precursor molecules used in alternative deposition methods such as chemical vapor deposition and atomic layer deposition. In this presentation, we report the oxidation kinetics of Hf and Zr via the UVO technique in the temperature range from 25°C to 300°C, and correlate these results with the microstructural and electrical properties of UVO ZrO_2 and HfO_2 films grown on Si (001). In the oxidation kinetics study, nuclear reaction analysis (NRA) was performed at various oxidation times and temperatures to determine oxygen areal density with monolayer sensitivity. To synthesize MOSCAP structures, 20 50$\AA$ Zr or Hf metal were deposited by e-beam evaporation on Si after different surface cleaning/ultrathin oxide passivation pretreatments. $In-situ$ UV-ozone oxidation was performed in the temperature range from 25°C to 300°C. , Platinum electrodes were deposited $ex-situ$ by e-beam evaporation through a shadow mask. NRA data show that the oxidation kinetics of Hf and Zr are enhanced significantly as the UVO temperature is increased. For given oxidation times and UVO processing conditions, the incorporated oxygen in the Hf oxidation product is much less than for Zr oxidation. Capacitance-voltage measurements indicate that frequency dispersion of the capacitance decreases with increasing UVO temperature. The capacitance-derive equivalent oxide thickness evolves with UVO process times and temperatures in a manner consistent with a competition between reduction of the initial SiO_2 surface passivation by the reactive Zr or Hf metal precursor layer, and oxidation of the underlying Si substrate to thicken this interface layer. The leakage current density is significantly reduced as the UVO temperature increases due to interfacial oxide growth and, perhaps, improved oxygen stoichiometry of HfO_2 films.

D3.15
Abstract Withdrawn

D3.16
The effect of ZrO2 incorporation into rare earth Gd2O3 film grown on Si(111). so ah park[1], Yongkuk Kim[1], J.H. Baeck[1], M.H. Cho[2], M.K. Nor[1] and K.H. Jeong[1]; [1]Yonsei university, seoul, South Korea; [2]Korea Rearch Institution of Standard Science, seoul, South Korea.

Gd2O3 films incorporated with ZrO2 were deposited on Si(111) using electron-beam evaporation by reactive thermal evaporation. High resolution x-ray diffraction and RBS data showed that Gd2O3 films incorporated with ZrO2 are superior epitaxial quality to pure Gd2O3 films. The improved crystallinity is caused by interfacial reaction between rare earth metal Gd and Si substrate. The chemical state of the films investigated using X-ray photoelectron spectroscopy indicated that the incorporated Zr played an important role to restrain silicate layer. The preferred silicide formation between Si and Gd were observed in as-grown film and the silicate formation was started at the reaction sites during post annealing treatment. The reaction at interfacial region significantly influenced thermal stability of the films such as morphology and crystallinity. The suppressed interfacial reaction and improved crystal quality resulted in decrease the leakage current and oxide trap charge density.

D3.17
$Ba_{0.50}Sr_{0.50}TiO_3$thin films processed in microwave oven. Talita Mazon, Maria Aparecida Zaghete, Mario Cilense and Jose Arana Varela; CMDMC - LIEC, Instituto de Quimica - UNESP, Araraquara, So Paulo, Brazil.

$Ba_{0.50}Sr_{0.50}TiO_3$ (BST50) thin films were deposited on Pt/Ti/SiO_2 substrates and, for the first time, sintered in a domestic microwave oven. The X-ray diffraction patterns showed that the films are polycrystalline. Scanning Electron Microscopy (SEM) and Atomic Force Microscopy (AFM) were used to analyse the influence of this type of heat treatment on the film microstructure. The results indicated that the films treated at temperatures below 600°C for 10 min were homogeneous and dense, and the electrical properties confirmed the good quality of these films.

D3.18
Influence of Pre-Oxidation of an Ir Film on Chemical Composition and Crystal Property of a PZT Film Deposited on the Ir Film by Sputtering. Susumu Horita and Makoto Shouga; School of Materials Science, Japan Advanced Institue of Science and Technology, Tatsunokuchi, Ishikawa, Japan.

We investigated the influence of pre-oxidation of an Ir film on the chemical composition and crystal property of the PZT film deposited on the pre-oxidized Ir film. The Ir film was deposited on a thermally oxidized Si substrate at 600°C by Ar gas sputtering with an Ir metallic target. The Ir film had (111) preferable orientation. The pre-oxidation of the Ir film was performed at 600°C in 10 Pa of O_2 gas for 20 min in the deposition chamber prior to depositing a PZT film. The PZT film was deposited on the Ir film at 600°C by reactive sputtering of Ar+O_2(9:1) gas with a 100-mm-diameter ceramic PZT target and 10-mm-diameter PbO pellets. In this experiment, we changed the target composition to be $Pb_{1.1}(Zr_{0.2}Ti_{0.8})O_3$, $Pb_{1.1}(Zr_{0.52}Ti_{0.48})O_3$ and $Pb_{1.2}(Zr_{0.8}Ti_{0.2})O_3$. Also, on each target, 8 or 15 pieces of PbO pellet were placed circularly to control Pb stoichiometry in the PZT film. At fist, we found from the XRD measurement that a strong PbO(101) peak appeared from the PZT film deposited on the pre-oxidized Ir film with the target of Zr/Ti = 52/48 and 15 PbO pellets although no PbO peak was observed from the PZT film deposited on the non-oxidized Ir film with the same target. Also, while a small (100) or (001) perovskite PZT peak was observed from the PZT film on the pre-oxidized Ir film, a large perovskite PZT peak was observed from the film on the non-oxidized Ir film. The RBS measurement showed that the chemical composition ratio of Pb/(Zr+Ti) on the pre-oxidized Ir film was about 3.5 much larger than that on the non-oxidation Ir film, 1.3. This means that oxidized Ir film has a role to suppress the Pb and PbO re-evaporation during the PZT film deposition. The same phenomenon was observed

in the PZT film deposited from the Zr/Ti=20/80 target. However, in the case of the Zr/Ti=80/20 target, the chemical composition of the PZT film on the pre-oxidized Ir film was almost equal to that without pre-oxidation regardless of the number of PbO pellet. Also, the ratios of Pb/(Zr+Ti) for the pre- and non-oxidation cases were decreased with the number of PbO pellet in the same manner. We speculate the reasons of these results as follows; Since some reports have mentioned that XRD peak of (110) IrO_2 is observed from the oxidized Ir film, the surface of the pre-oxidized Ir film may contain IrO_2(110) phase. Because the lattice constants of (101) PbO plane are 0.605 and 0.339 nm which are near 0.634 and 0.314 nm of (110) IrO_2 plane, (101)PbO phase can easily grow on the IrO_2(110) phase film. The crystallization of PbO phase prevents itself from decomposition and re-evaporation during the PZT film deposition, which increases the amount of Pb contents in the deposited film. On the other hand, as Zr oxide is thermally stabler, oxides containing much of Zr may be hardly decomposed during the deposition. So, for Zr/Ti = 80/20, the chemical composition of the PZT film is independent on the surface state of the Ir film, i.e., oxidized or metallic surface.

D3.19
Effect of excess Cu on dielectric properties of CaCu$_{3}$Ti$_{4}$O$_{12}$ thin films by pulsed laser deposition. Ram S Katiyar, Vinay Gupta, Anju Dixit, Pijush Bhattacharya and Rasmi R Das; Department of Physics, University of Puerto Rico, San Juan, Puerto Rico.

High dielectric constant oxides have become increasingly important in microelectronic applications due to continuous size reduction of microelectronic devices. Cubic perovsikite CaCu$_{3}$Ti$_{4}$O$_{12}$ (CCT) has been paid much attention due to very high dielectric constant (10^{4}) in bulk and ceramic forms at room temperature and remains constant from 100 K to 600 K. In this study, the thin films of CCT were fabricated on platinized Si and Nb doped SrTiO$_{3}$ by using stoichiometric and excess Cu ceramic targets. The films were fabricated at an oxygen pressure of 200 mTorr and the substrate temperature of 750 ^{0}C using pulsed laser deposition. The X-ray diffraction and atomic force microscopy measurements revealed that the films were polycrystalline in nature having uniformly distributed grains. The Raman vibrational modes of CCT thin films are in agreement with the reported results on bulk CCT. The dielectric constant and the loss tangent for CCT films were investigated in a wide frequency range (100Hz to 1MHz) CCT films at different temperatures range 100- 500 K. The room temperature dielectric constant was increased from 1575 to 2200 in the films deposited with the excess copper at 100 KHz. The Authors acknowledge the financial support of NSFINT0097018, NASA#NCC3-1034. One of the authors (VG) is also thankful to DST, India, for BOYSCAST fellowship and financial assistance

D3.20
Dielectric Properties of $KTa_{0.524}Nb_{0.446}Ti_{0.03}O_3$ Thin Film using PLD. Hyung-jin Bae[1], Jennifer Sigman[1], Byoung-seong Jeong[1], L A Boatner[2] and David P Norton[1]; [1]Materials Science and Engineering, University of Florida, Gainesville, Florida; [2]Solid State Division, Oak Ridge National Laboratory, Oak Ridge, Tennessee.

$KTa_{1-x}Nb_xO_3$ (KTN) has been intensively studied for its ferroelectric properties in microwave applications and optical wave guide. A key issue for these materials is losses at frequency. One approach to minimizing losses of paraelectrics is through cation doping. In this study, 3 at % of Ti was doped in $KTa_{0.524}Nb_{0.446}O_3$ (KTN:Ti) target. The Ti doped KTN films were grown on MgO (100) single crystal in different oxygen pressure at 750°C of deposition temperature, and 3J/cm^2 of laser energy density with 4 cm of distance between target and substrate by PLD. The dielectric properties of Ti-doped KTN were observed as a function of oxygen growth pressure, and film thickness using C-V measurement. The physical properties of KTN:Ti films were characterized with XRD, and AFM. This loss properties of the Ti doped KTN films will be compared to these for undoped materials.

D3.21
MOCVD Processes for Electronic Materials Adopting $Bi(C_6H_5)_3$ Precursor: Kinetics and Mechanisms. Cedric Bedoya[1], Guglielmo Guido Condorelli[1], Giuseppe Anastasi[1], Judit Lisoni[2], Dirk Wouters[2] and Ignazio Luciano Fragala'[1]; [1]Dipartimento di Scienze Chimiche, Universita di Catania, Catania, Italy; [2]IMEC, Leuven, Belgium.

Bi_2O_3-based layered-perovskites are promising materials for superconducting electronics and for the new non-volatile ferroelectrics memories (NVFeRAM). Among ferroelectric oxides, $SrBi_2Ta_2O_9$ (SBT) and $Bi(La_xTi_{1-x})_4O_{12}$ (BLT) are very attractive materials due to their superior endurance resistance and good remnant polarization. High level integration required by commercially competitive 1T1C stacked ferroelectric cells is entirely suited with MOCVD due to the better conformality of deposition and the higher throughput with respect to other available deposition techniques. b-diketonates or alkoxides have been proposed as Bi sources to obtain smooth and homogeneous morphologies. These sources, however, require MOCVD reactors equipped with liquid delivery systems (LDS) due to their low thermal stabilities precluding efficient sublimation/evaporation processes. Moreover, they are highly moisture-sensitive, thus requiring particular care for storage and manipulations. By contrast, $Bi(C_6H_5)_3$ is more versatile and represents the most used, thermally stable precursor. It can be efficiently used in both classical and LDS equipped MOCVD reactors without problems for storage and manipulations. In this paper we report on a extensive study of MOCVD processes on technological substrates involving $Bi(C_6H_5)_3$. Insights on the mass transport process as well as on the mechanisms of MOCVD deposition have been obtained combining in situ FT-IR and ex situ XRD, SEM and EDX techniques. In situ FT-IR monitoring has proven that $Bi(C_6H_5)_3$ possesses suited thermal stability upon sublimation and good mass-transport properties since it can be sublimed and transported intact to the deposition zone up to 270°C. Intriguing relationships between deposition parameters, growth kinetics, film structure and morphology have been studied as a function of deposition operational parameters and the substrate nature. Homogeneous films have been obtained in the 350-550°C temperature range on technological $Pt/TiN/SiO_2/Si$ and $Ir/TiN/SiO_2/Si$ substrates. In the 350-450°C temperature range, the deposition mechanism involves a heterogeneous pathway including the dissociation of phenyl groups and the formation of polycrystalline Bi_2O_3. O_2 plays a determining role in both the precursor decomposition and Bi_2O_3 growth. Above 450°C, other decomposition pathways, involving the oxidative break-down of the aromatic ring, occurs. This leads to various oxidation products and, therefore, to less clean processes.

D3.22
Ferroelectric phase transitions in laser ablated ferroelectric Ca doped Barium titanate thin films. Victor Pushparaj[1], J. Nagaraju[2] and S.B. Krupanidhi[1]; [1]Materials Research Center, Indian Institute of Science, Bangalore, Karnataka, India; [2]Instrumentation, Indian Institute of Science, Bangalore, Karnataka, India.

Photo refractive barium - titanate crystals are used for self - pumped phase conjugation in advanced laser systems for laser - beam cleanup via two - wave mixing and for optical interconnects. Doping of the Ca in the BaTiO3 ceramics had showed a remarkable improvement in the electromechanical behavior, increase in the temperature range of the stability of the tetragonal phase and inhibited the formation of the unwanted hexagonal phase of BaTiO3. Ba1-xCaxTiO3 (at. % Ca x = 0.05, 0.1, 0.13 and 0.18 at%) targets were prepared by solid state reaction technique and the BCT thin films were deposited on Pt coated Si substrates by pulsed excimer laser ablation technique. The dielectric constant and ferroelectric phase transition temperature in both the bulk and the thin films were found to decrease with the increase of Calcium content in Barium titanate matrix. At higher Ca contents, ($x > 0.1$), a sharper phase transition temperature was observed for the Ca substituting Ba site , while it exhibited a diffuse phase transition with the higher amount of Ca entering the Ti site with a significant decrease in the transition temperature. This anomaly in the decrease of phase transition temperature has been investigated which could have arised due to the size effect in ferroelectric domains, intergranular stresses, strain existing at the film - substrate interface. Attempts on the structural correlation of these thin films are also done. There was a diffused phase transition been observed for the higher calcium content (> 10 at.% Ca) on Pt coated Si substrates and also exhibited frequency independence on temperature beyond the curie temperature. This vividly exhibits a cross over from the ferroelectric to non lead relaxor type behavior observed, for the higher calcium concentration. This might be due to the isovalent of A site entering the B site thereby disrupting the dipoles in the B site and creating disorder. There is an evidence from neutron diffraction, of the possibility of the Ca ions going into the B site. As a result o f the Ca going into the Ti sites, the energetics and dynamics of the reorientation of the Ca oxygen vacancy (Ca:Vo) pair defect results in the relaxor behavior beyond certain at.% substitution.

D3.23
Preparation of Ferroelectric $Pb(Zr_{0.35}Ti_{0.65})O_3$ Films on Conducting Oxide Ga-Doped ZnO Films for Ferroelectric Transparent Thin-Film Transistors. Kwang Bae Lee[1], Kyung Haeng Lee[1] and Byeung Kwon Ju[2]; [1]Computer & Electronic Physics, Sangji University, Wonju, Gangwondo, South Korea; [2]Microsystems Research Center, Korea Institute of Science and Technology, Seoul, South Korea.

We have investigated the feasibility of ferroelectric transparent thin-film transistors using $Pb(Zr_{0.35}Ti_{0.65})O_3$ (PZT) and Ga-doped

ZnO (GZO), which act as a ferroelectric layer and a transparent conducting oxide, respectively. Sputter-deposited GZO films having the minimum resistivity of 3×10^{-4} Ωcm were obtained at the substrate temperature of 250 °C, and the sol-gel derived ferroelectric PZT films deposited on GZO could be obtained at the annealing temperature of 580 °C in O_2 ambient. However, for such conventional annealing in O_2 ambient, the resistivity of GZO increased rapidly with increasing the annealing temperature, which implied the failure of gate layers. Hence we attempted the rapid thermal annealing (RTA) process in N_2 ambient. The ferroelectric PZT films with relative low resistive GZO electrodes could be successfully prepared by using such RTA process in N_2 ambient. GZO/PZT/GZO capacitors showed the P-E hysteresis loops with the typical remanent polarization and the coercive field of 28 $\mu C/cm^2$ and 95 kV/cm, respectively. In this study, we also showed the characteristics of ferroelectric transparent thin-films transistors, basically consisted of the GZO/PZT/GZO structure.

D3.24
Effect of La-doping on the structure and electrical properties of $SrBi_{2\}}Ta_2O_2$. Ram S Katiyar, Nora Ortega, Sudipta Bhattacharyya and Pijush Bhattacharya; Department of Physics, University of Puerto Rico, San Juan, Puerto Rico.

Bismuth-layered ferroelectrics have been the major focus of interest in the field of ferroelectric memories. SBT was one of the foremost candidates belonging to this family, which met all the requirements of a nonvolatile memory device. Moreover, it is already established that the lanthanum doping in bismuth-layered ferroelectrics significantly alters the processing parameters without compromising in their ferroelectric properties. This led us to dope lanthanum in pure SBT to study its effect on processing and electrical properties. In this report, we have demonstrated that phase pure SBT bulk samples can be synthesized with up to 15 % lanthanum doping without any phase segregation. The lanthanum-doped SBT ceramics were used as targets for depositing thin films by pulsed laser ablation. The XRD patterns indicated the incorporation of lanthanum ions inside the lattice without any significant peak shift. The absence of any lattice distortion indicated an isovalent replacement of bismuth with lanthanum, which had the same ionic radius. We have compared the normal Raman modes in doped as well as undoped samples. The ferroelectric soft mode (at 27 cm^{-1} had shifted towards lower frequencies as the doping concentration was increased at room temperature. The dielectric constant was nearly constant (150) irrespective of the lanthanum content. The thin film data will be compared with those of bulk SBT. The temperature dependence of the dielectric and Raman spectra will be presented in this paper

D3.25
The Influence of Composition on Properties and Structure of PZN-PLZT Ceramics. Li Ai Ding[1], yong zhang[1] and suming li[2]; [1]Key State Lab. of Materaials, Shanghai Institute of Ceramics, Chinese Acedamy of Sciences, Shanghai, China; [2]Shanghai Hengtong Optic & Elcetric Technology Co., Ltd, Shanghai, China.

PZN-PLZT ferroelectric ceramics with different composition has been successfully prepared by hot-pressed sintering in oxygen atmosphere. The results showed that structure and properties sensitively affected by the cotent of La, Zr and Ti and the ratio between PZN and PLZT. X-ray analysis and SEM in acoustic mode showed that the non-perovskite structrue formed easily in PZN-PLZT ceramics as the ratio of PZN/PLZT is larger than 1.[0.3(PbZn1/3Nb2/3)-0.7(PLZT(9/65/35))] ceramics exhibits excellent optical transpatent for wavelength from near ultraviolet to infrared and electro-optical properties. Good piezoelectric properties are shown in [0.3(PbZn1/3Nb2/3)-0.7(PLZT(4/54/46))]. PZN-PLZT ceramics with both outstanding piezoelectric properties and electro-optical properties can be realized by adjusting the composition and such PZN-PLZT ceramics is useful for MEMS and integrated optic system.

D3.26
Grain distribution of ferroelectric BT-based films for high-density semiconductor memories. Weon-il Kweon[1], Mi-Jin Jin[1], Beelyong Yang[1], No-Jin Park[1], Sung-Jin Kim[1], Suk-Kyong Hong[2], Seug-Suk Lee[2] and Young-Jin Park[2]; [1]Materials Science & Engineering, Kumoh National Institute of Technology, Gumi-Si, Gyeongbuk, 730-701, South Korea; [2]Memory R & D Division, Hynix Semiconductor Inc., Icheon-Si, Kyongki-do, 467-701, South Korea.

Issues of ferroelectric high-density memories (>64Mb) indispensable for upcoming ubiquitous era have been on the cell integration less than 0.1um2 and reliabilities. Thus nanoscale control of microstructures of ferroelectric films with large switching polarization has been one of the issues to obtain the uniform electrical properties for realization of high-density memories. In this study the grain orientation and distribution of BT-based films by spin-on coatings were examined by FEG-SEM/EBSD and XRD. Ferroelectric domain characteristics by PFM were also performed to study the dependency of reliabilities on grain orientation and distribution. Film process effects such as RTA and furnace annealing on grain orientation and uniformity will be discussed aiming at understandings of the nucleation and growth of the films during the processes.

D3.27
Influence of the tungsten and nickel dopants on the crystallization and electrical properties of PZT. Maria Aparecida Zaghete[1], Rubens Soeiro Goncalves[2,3], Denilson Moreira dos Santos[2,3], Carlos Oliveira Paiva - Santos[2] and Jose Arana Varela[2]; [1]DBTQ, CMDMC, LIEC, Instituto de Quimica, Universidade Estadual Paulista, Araraquara, Sao Paulo, Brazil; [2]DFQ, CMDMC, LIEC, Instituto de Quimica, Universidade Estadual Paulista, Araraquara, So Paulo, Brazil; [3]DQ, CEFET - Maranhao, Sao Luis, Maranhao, Brazil.

Ferroelectrics ceramics based on lead titanate zirconate (PZT) have a remarkable impact on a large number of practical applications in the electronic industry. It has been reported many different methods and dopants to obtain PZT ceramics with better properties. Nevertheless, chemical based processes have been revealed as a promising preparation route due to their low cost processing and the facility for controlling the stoichiometric of complex systems. The objective of this research was to investigate the influence of the tungsten and nickel dopants on crystallization and physical properties of the $Pb(Zr_{0.53}Ti_{0.47})O_3$ .Pure, tungsten and nickel doped PZT with concentration range from 2 to 8 %mol were prepared by the polymeric precursor method. The polymers were decomposed at 300°C during 4 hours and calcined at 700 °C for 3 hours. The samples were sintered at 1100 °C for 3 hours in a closed system. The influence of dopants concentration on the structural, microstructural and electrical properties were investigated by thermoanalysis, X-ray diffraction, scanning microscopy and termistor hysteresis loop. The X-ray diffraction patterns of powders showed that there are only PZT crystalline phase. The addition of nickel shift the shrinkage temperature to low values while tungsten shifts the shrinkage temperature to higher values compared to pure PZT. The highest values for remanent polarization, Pr (40 mC/cm^2) and coercive field , Ec (1200 V/cm) were observed for the sample doped with 8 % molar of tungsten

D3.28
Analysis of Ferroelectric Microcapacitors by Scanning Probe Microscope. Nobuhiro Kin and Koichiro Honda; Fujitsu Laboratories Ltd., Atsugi, Japan.

In order to promote the development of higher density FRAM, the cell size should be reduced. Therefore, the size effects resulting from processing and the physical properties must be measured. So it has become important to analyze the electric characteristics of a single bit cell capacitor. On the other hand, as the characteristic of ferroelectric material, it is known that the Vc increases at low temperatures and the Pr falls at high temperatures. In order to evaluate the impact of temperature on the ferroelectric, we constructed a new evaluation system based on scanning probe microscope, which was able to measure the electric characteristics of a single bit cell capacitor. This system can be used in the temperature range from -120 degrees C to 300 degrees C. It is realized by circulating liquid nitrogen around a SPM stage and an electrical heater. We measured the electrical properties of ferroelectric microcapacitors by using a sample with a IrOx/PZT/Pt structure. As a result, 2Pr is 41.9 [uC/cm2], Vc+ is 0.8 [V] and Vc- is ?1.1 [V] at 25 degrees C. However, at -45 degrees C, 2Pr is 46.2 [uC/cm2], Vc+ is 1.1 [V] and Vc- is ?1.6 [V]. That is, it can be shown that Vc increases 10% at low temperatures also in an actual FRAM single bit cell capacitor.

D3.29
Structural and electrical investigations on laser ablation grown Ba1-xCaxTiO3 thin films on Si substrate in MFS structure. Victor Pushparaj[1], J. Nagaraju[2] and S.B. Krupanidhi[1]; [1]Materials Research Center, Indian Institute of Science, Bangalore, Karnataka, India; [2]Instrumentation, Indian Institute of Science, Bangalore, Karnatak, India.

Ferroelectric thin films are playing a vital role in the areas of MEMS, microwave applications, capacitors and electro-optic devices. The $Ba_{1-x}Ca_xTiO_3$ crystals plays a dominant role in the areas of electro - optic modulators and related devices. There are very few reports in the open literature on $Ba_{1-x}Ca_xTiO_3$ thin films and hence in this study we have grown $Ba_{1-x}Ca_xTiO_3$ ($0 < x < 0.15$) thin films (thickness 0.3μm) by pulsed excimer laser ablation technique on p - type Si substrate in Metal - Ferroelectric - Semiconductor (MFS) configuration. A thorough electrical and structural analysis has been made on the integration of $Ba_{1-x}Ca_xTiO_3$ thin films on Si substrate. The structural studies involves the Micro - Raman spectroscopy,

SIMS, SEM, TEM and the electrical characterization involves the C - V measurement, dc leakage current conduction behavior and inteface states analysis. The dielectric constant calculated in the accumulation region was found to decrease with increase of Ca in Ba site of the $Ba_{1-x}Ca_xTiO_3$. The interface states calculated were order of 10_{11} $eV_{-1}cm_{-2}$ for $Ba_{1-x}Ca_xTiO_3$ thin films deposited on the Si substrate. As x increases, the interface states was found to increase which could have arised due to the decrease in grain size (i.e. when larger amount of Ca replaces Ba site) which leads to large number of dangling bonds at the interface. These investigations are very essential in order to realize a good electro - optic modulator on the Si substrate. The Space Charge limited conduction mechanism was found to obey the dc leakage current behavior observed in our case.

D3.30
Effect of different annealing procedures on microstructural and electrical properties of CSD derived BST thin films.
Sandip Halder[1], Theodor Schneller[1] and Rainer Waser[1,2]; [1]IWE-II, RWTH Aachen, Aachen, NRW, Germany; [2]Institut for Festkoerperforschung, Forchungzentrum Juelich, Juelich, NRW, Germany.

Processing of BST thin films is becoming more and more important for microwave electronics and for its probable incorporation in future high density DRAM's. A correlation between processing and final device characteristics is of utmost importance. Differences in microsrtructure and electrical properties were observed when chemical solution deposited thin films of BST were annealed using a conventional diffusion furnace and a rapid thermal annealing furnace. Films were prepared by depositing a solution made by the all propionate precursors (APP) route, of different concentrations (0.1M-0.3M), on Pt coated silicon wafers and crystallized between 550^oC and 700^oC. Cross sectional SEM on the films reveal differences in microstructure for the films annealed by different methods. Differences of microstructure are also evident when films of different concentration are used. The electrical properties of the films were found to vary considerably. Frequency dependence of dielectric constant and IV measurements were performed on the differnt types of films.

D3.31
Suppression of Read-Out Data-Disturb Effect by Novel Ferroelectric-Gate Structures. Eisuke Tokumitsu and Hirokazu Saiki; Precision and Intelligence Lab, Tokyo Institute of Technology, Yokohama, Japan.

One-transistor (1T) type ferroelectric random access memory (FeRAM) using ferroelectric-gate transistors is promising for future nonvolatile memory applications. To read-out the stored data from transistor-arrays of 1T-type FeRAM, the drain current of the non-accessed devices should be zero, regardless of the ferroelectric polarization. In other words, the device should be normally-off. To realize this, the threshold voltage should be controlled by channel ion-implantation or changing the work function of the gate electrode material. However, when the read voltage is applied to read-out operation after the device is retained at VG =0, the drain current for read-out operation becomes small, because the operation point of the device goes into one of the minor P-E hysteresis loops. In this work, to overcome the read-out data disturb problem, two approaches have been discussed. First approach is the use of a split-gate structure, where an additional MOSFET is equivalently connected to the ferroelectric-gate FET. The MOSFET is used to cut off the drain current when VG =0. On the other hand, the ferroelectric-gate FET can be remained on state when VG=0, hence, the device still can use the major P-E loop and produce large on drain current. SPICE simulation demonstrates that the drain current for read-out becomes much smaller than that in the write process for conventional ferroelectric-gate FETs, whereas the degradation in the read drain current is negligible for the proposed new structure. Second approach is a new device structure which consists of an MOSFET with a ferroelectric capacitor and an additional normal dummy capacitor, where both two capacitors are connected to the gate of MOSFET. When the device is retained at VG = 0V, this capacitor is negatively biased because of the remanent polarization of ferroelectric capacitor, which compensates the total charge applied to the gate of MOSFET. Hence, the device can realize off state when the gate voltage is zero and still can use a major P-E loop for read-out operation. P-E characteristics required for the ferroelectric-gate transistors are also discussed in the presentation.

D3.32
Microwave Dielectric Properties of Modified CaTiO3-Based Ceramics System. liu tao and chen wen; Department of Material Science and Engeering, Wuhan University of Technology, Wuhan, Hubei, China.

The microwave dielectric properties of CaTiO3-based system were investigated, especially for temperature coefficient of resonate frequency (TCF). Perovskite-type dielectric ceramic, CaTiO3, with high dielectric constant and high quality factor value Qf and unacceptable negative TCF, was modified by Ca(Mg1/3Nb2/3)O3(CMN), (Li1/2Ln1/2)TiO3(LLT) and Al2O3(AO), which all have negtive TCF, to form compounds system: (1-x)CaTiO3-xCMN/LLT/AO. The compounds present excellent microwave dielectric properties: near-zero TCF at certain x value and remain high dielectric constant and low dielectric loss. The temperature compensated series show adjustable properties as a function of the composition x. Intrinsic reason of the relationship of structure and properties for the dielectric compounds, such as top-shared Ti-O octahedron, cation order and structure stability, were also discussed.

D3.33
Structural,Dielectric and Pyroelectric properties of Lanthanum modified Lead Titanate Thin Films.
Tarachand Goel[1], Sonalee Chopra[2], Seema Sharma[3] and R.G Mendiratta[4]; [1]Physics, IIT Delhi, New Delhi, Delhi, India; [2]Physics, IIT Delhi, New Delhi, Delhi, India; [3]Physics, IIT Delhi, New Delhi, Delhi, India; [4]Physics, NSIT Delhi, New Delhi, Delhi, India.

Ferroelectric lead lanthanum titanate (Pb1-x Lax Ti1-x/4 O3)(PLTx) thin films (x=0.04,0.08 and 0.12) have been prepared by sol-gel spin coating process on ITO coated 7059 glass substrates. Investigations have been made on the crystal structure, surface morphology, dielectric and ferroelectric properties of the films. For a better understanding of the crystallization mechanism, the structural investigations were carried out at various annealing temperatures (350, 450, 550 and 650 OC). Characterization of these films by X-ray diffraction show that the films annealed at 650C exhibit tetragonal structure with perovskite phase. Replacement of lanthanum in lead titanate results in reduction of tetragonal ratio (c/a), resulting in better mechanical stability. Microstructural analysis of the films were carried out by taking the Atomic Force Microscope (AFM) pictures. AFM images are characterized by slight surface roughness with a uniform crack free, densely packed structure. Dielectric, pyroelectric and ferroelectric studies carried out on these films have been reported. Dielectric constant and pyroelectric coefficient increases while Curie temperature decreases with increase in La content. The pyroelectric figures of merit of the films have also been calculated which suggest that 8 % lanthanum is best suited matial for pyroelectric detectors owing to its high pyroelectric coefficient (29nC/cm2K), high voltage responsivity (420Vcm2/J), high detectivity (1.04X10-5 Pa-1/2) and low variation of pyrocoefficient with temperature.

D3.34
Single transistor type ferroelectric memory with $Pt/SrBi_2Ta_2O_9/Pt/CeO_2/Si$ MFMIS gate structure.
Sun Il Shim[1,2], Ik Soo Kim[1], Young Suk Kwon[1], Seong-Il Kim[1], Yong Tae Kim[1] and Jung Ho Park[2]; [1]systems technology division, Korea Institute of Science and Technology, Seoul, South Korea; [2]Electronical Engineering, Korea Univerity, Seoul, South Korea.

The single transistor type ferroelectric random access memory (1T Type FRAM) has advantages over the capacitor type FRAM in nondestructive readout and small cell size. In spite of its advantages, the short data retention time and the high operating voltage are still major problems. The metal ferroelectric metal insulator semiconductor (MFMIS) gate structure have been proposed for overcoming the finite retention problem. In order to lower the operating voltages and prevent the insulating layer from breaking down, the insulating layer with high dielectric constant and the high area ratio of MIS capacitor to MFM capacitor were required because the voltage induced the insulating layer decreases and the voltage induced the ferroelectric layer increases. We have developed the MFMISFET with CeO_2 film as a high-k insulating layer. The CeO_2 film with the thickness of 20 nm was deposited by rf sputtering of Ce target in the reactive oxygen ambient and annealed at 800 °C for 30 min in the oxygen ambient. The MFMIS capacitor and MFMISFET were fabricated with various area ratios and the electrical characteristics were investigated. The $SrBi_2Ta_2O_9$ (SBT) film was used as a ferroelectric gate material. The inductively coupled plasma reactive ion etching (ICP-RIE) system was adapted to remove the useless ferroelectric film and electrode. The drain current - gate voltage (I_D-V_G) characteristics with the area ratio of 2 showed the threshold voltage difference of 1.5 V at the 5 V operating voltage. The drain current - drain voltage (I_D-V_D) characteristics showed that the drain current difference between programmed on state and erased off state was more than 2 and 5 orders at the operation voltage of 3 and 5 V, respectively. The electrical performance of MFMISFET shows that it has good ferroelectric memory characteristics and programmable operation.

D3.35
Dielectric properties of epitaxial $Ba_{0.6}Sr_{0.4}TiO_3$ films on silicon substrates using bi-axially oriented ion-beam-assisted

deposited MgO as template layers. Bo Soo Kang, Jang-Sik Lee, L. Stan, R. F. DePaula, P. N. Arendt and Q. X. Jia; Materials Science and Technology Division, Los Alamos National Laboratory, Los Alamos, New Mexico.

The nonlinear dielectric property of $Ba_{1-x}Sr_xTiO_3$ makes it very attractive for electrically tunable microwave devices. Recently, there have been many studies to obtain a large capacitance change ratio [tunability=$(C_{max} - C_{min})/C_{max}$] of $Ba_{1-x}Sr_xTiO_3$ films grown on single crystal oxide substrates, such as $LaAlO_3$ and MgO. In order to achieve silicon-compatibility of the devices, we have deposited epitaxial $Ba_{0.6}Sr_{0.4}TiO_3$ (BST) films on silicon substrates using pulsed laser deposition, by introducing a bi-axially oriented MgO as the template layer. The epitaxial BST films were successfully grown at 750°C under 200 mTorr oxygen. The dielectric properties of the BST films were measured in coplanar capacitor structures by depositing gold electrodes on top of the BST surface. The structural properties of the BST films were found to be closely related to the in-plane mosaic spread of the template layers. The effects of the crystallinity of the BST films on their dielectric properties were investigated. This work demonstrates the importance of the crystalline quality of the template layers in pursuit of silicon-compatibility of the tunable microwave devices using BST films.

D3.36
Investigations of $Pb_xSr_{1-x}TiO_3$ Thin Films and Ceramics for Microelectronic Applications. Menka Jain[1], Yu. I. Yuzyuk[2], R. S. Katiyar[1], Y. Somiya[3], A. S. Bhalla[3], F. A. Miranda[4] and F. W. VanKeuls[5]; [1]Physics, University of Puerto Rico, San Juan, PR, Puerto Rico; [2]Physics, Rostov State University, Rostov-on-Don, Russian Federation; [3]Materials Reserach Institute, The Pennsylvania State University, University Park, Pennsylvania; [4]NASA Glenn Research Center, Cleveland, Ohio; [5]The Ohio Aerospace Institute, Cleveland, Ohio.

We have investigated electrical and optical properties of thin films and ceramics of $(Pb_xSr_{1-x})TiO_3$ (PST) in the complete range. The Curie temperature and the lattice parameters of $Pb_xSr_{1-x}TiO_3$ (PST-x) solid solutions were found to be dependent upon Pb/Sr ratio. Only one phase transition in the PST system (compared to three in $Ba_xSr_{1-x}TiO_3$) was recorded. The studies indicate that PST has potential for tunable microwave devices in the paraelectric phase whereas in the ferroelectric phase it is suitable for ultra-large-scale integration (ULSI) dynamic random access memory (DRAM) capacitors. PST compositions with x = 0.4 are paraelectric at room temperature and exhibit ferroelectric phase transition below room temperature. In the present studies, $Pb_{0.2}Sr_{0.8}TiO_3$ (PST-20) and $Pb_{0.3}Sr_{0.7}TiO_3$ (PST-30) ceramics were prepared by the conventional solid-state reaction method and thin films of PST were prepared by sol-gel technique. X-ray, dielectric, electrical, and Raman measurements were performed on these samples. Sharp phase transition was observed by dielectric and Raman measurements for PST-20 and PST-30 ceramics at -60 ^oC and 10 ^oC, respectively. Raman measurements revealed well-pronounced soft-mode behavior below the Curie temperature in both compounds. The thin films of PST deposited on platinized-silicon substrate were polycrystalline and those on lanthanum aluminate (LAO) were highly (100) oriented. These films were characterized in terms of their electrical properties and dielectric behavior at low frequencies (1kHz-1MHz). Eight element coupled micro-strip phase shifters (CMPS) were fabricated on the PST films deposited on LAO and tested in terms of their degree of phase shift and insertion loss characteristics at microwave frequencies. The average figure of merit of 48 ^{o}/dB for PST30 film shows the potentiality of these films for high frequency tunable dielectric devices. This work is supported in parts by NSF-INT (0097018), NASA-NCC5-518, and DOD (N00014-02-1-0215), and DABT (63-98-1-002) grants.

D3.37
High dielectric permittivity in Ca1-xBixTi1-xCrxO3 ferroelectric perovskite ceramics. Chao-Yu Chung, National Cheng Kung University, Tainan City, Taiwan.

The ferroelectric ceramic, Ca1-xBixTi1-xCrxO3 is synthesized by solid state reaction technique; χ is ranged from 0 mole—% to 0.5mole%. All of the compositions have been found to have orthorhombic structure. The structure of the compositions upto $\chi \leq$ 0.05 is similar to that of CaTiO3. The structures changes gradually from CaTiO3 to BiCrO3 in the composition range of $0.05\langle\chi\langle0.50$. Dielectric constants, at room temperature have been found to increase with increasing the substitute concentration upto X=0.30 (—*epsilon≈ 25000) and thereafter it decreases with increasing χ upto 0.50. Orientation and space charge polarizations contribute to the dielectric behaviour of these material. In addition, the electric resistances of these materials were higher than 10G Ω, this is due to balance of valence compensation.

SESSION D4: Metal Gates
Chair: Marc-Aurel Nicolet
Wednesday Morning, April 14, 2004
Room 2006 (Moscone West)

8:30 AM *D4.1
Investigations of Metal Gate Electrodes on Hafnium Oxide. Jamie Schaeffer, C. Capasso, L.R.C. Fonseca, O. Adetutu, E. Luckowski, C. Hobbs, H.H. Tseng, D. Gilmer, M. Zavala, L.B. La, B-Y. Nguyen, B.E. White and P.J. Tobin; Advanced Products Research and Development Laboratory, Motorola, Austin, Texas.

As traditional poly-silicon gated MOSFET devices scale, the additional series capacitance due to poly-silicon depletion becomes an increasingly large fraction of the total gate capacitance, excessive boron penetration causes threshold voltage shifts, and the gate resistance is elevated. To solve these problems and continue aggressive device scaling we are studying metal electrodes with suitable work-functions and sufficient physical and electrical stability [1,2,3]. Our studies of metal gates on HfO2 indicate that excessive inter-diffusion, inadequate phase stability, and interfacial reactions are mechanisms of failure at source drain activation temperatures that must be considered during the electrode selection process. Understanding the physical properties of the metal gate/HfO2 interface is critical to understanding the electrical behavior of MOS devices. In particular, Fermi level pinning due to charge transfer between the metal and dielectric layers complicates implementation of metal gate electrodes. Fermi level pinning has been observed with poly-silicon [4] electrodes on HfO2 dielectrics and metal gate electrodes [5]. This research investigates Fermi level pinning by comparing the work functions of multiple electrodes on SiO2 and HfO2 dielectrics. We will present experimental data that characterizes the magnitude of the intrinsic and extrinsic contributions to Fermi level pinning and discuss specific defects that can contribute to work function pinning. In our research, experimental and calculated results emphasize the need to control the interface chemistry, the preferred crystal orientation, and the interface defects which can have a significant impact on the extracted metal work functions. [1] S. Samavedam, et al., 2002 IEDM Tech. Dig., 433-436, (2002), [2] S. Samavedam, et al., Procedings of Symposium on VLSI Tech. Dig., 24-25, (2002), [3] J.K. Schaeffer, et al., J. Vac. Sci. And Tech. B., 21, 1 (2003), [4] C. Hobbs, et al. 2003 Symp on VLSI Tech. Digest, 2003, [5] Y.C. Yeo, et al., IEEE Elec. Dev. Lett. Vol. 23 (6), p.342, 2002.

9:00 AM D4.2
Highly Reliable Metal Gate nMOSFETs by Improved CVD-WSix films with 4.3eV of Workfunction. Kazuaki Nakajima, Hiroshi Nakazawa, Katsuyuki Sekine, Kouji Matsuo, Tomohiro Saito, Tomio Katata, Kyoichi Suguro and Yoshitaka Tsunashima; Toshiba corporation Semiconductor company, Yokohama, Japan.

In this paper, we first propose an improved CVD-WSix metal gate with 4.3eV of workfunction as gate electrode for nMOSFETs and the relationship between the Si/W ratio of CVD-WSix and the reliability of MOSFETs. In this study, we fabricated CVD-WSix gate transistors by using Damascene gate process. After dummy gate removal, ion implantations were carried out through the gate groove in order to make local channel profile for adjusting threshold voltage of transistors. Activation annealing by spike RTA at 1000°C. Plasma SiON and CVD-WSix film are used for gate insulator and gate electrode, respectively. Workfunction of CVD-WSi3.9 gate estimated from C-V measurements was 4.3eV. Therefore, CVD-WSi3.9 gate is an attractive material as metal gate electrode for nMOSFETs. We measured the relationship between Tinv and gate leakage current (Jg) at 4.5MV/cm2 of electrical field. By using CVD-WSi3.9 electrode, Jg can be suppressed 1.5 order lower compared to that of n-polySi gate for same Tinv. The CVD-WSi3.9 / EOT 1.36nm gate oxynitride interface was observed by high-resolution TEM. No interaction between CVD-WSi and gate oxide can be observed in TEM image. We measured subthreshold characteristics of CVD-WSi3.9 gate MOSFETs. Vth variation of L/W=1μm/10μm CVD-WSi3.9 nMOSFETs can be suppressed to be lower than 8mV in 22chip. In CVD-WSi3.9 gate MOSFETs, where gate length is 50nm, a drive current of 636μA/μm was achieved for off-state leakage current of 35nA/μm at 1.0V of power supply voltage. Using CVD-WSi3.9 gate, highly reliable metal gate nMOSFETs can be realized. The relationship between the Si/W ratio of CVD-WSix and the reliability of MOSFETs will be discussed.

9:15 AM D4.3
Tunable workfunction with TaN metal gate on HfO2-HfxSiyO dielectrics. Christopher Sean Olsen[1], Philip A Kraus[1], Khaled Z Ahmed[1], Shreyas Kher[1], Steven Hung[1], Nety Krishna[1], Xiaoyi Chen[1], Lucien Date[1], Marc Burey[1] and Jason Campbell[2,1]; [1]Applied Materials, Sunnyvale, California; [2]Engineering Science and Mechanics, Pennsylvania State University, University Park, Pennsylvania.

MOSCAPS were fabricated from MOCVD HfO_2 and Hf_xSi_yO gate dielectrics with ALD TaN / PVD Ta metal electrodes. Dielectrics with 1.8 to 2.6 nm equivalent oxide thickness (EOT) were investigated with gate leakage (Jg) of 1E-7 to 1E-3 A/cm^2 at Vfb-1V. In addition to the C-V and I-V characterization of the MOSCAPs, XPS physical characterization was performed on monitor wafers to determine composition and physical thickness. From the combined results of the electrical and physical characterization, the relative dielectric constants of the Hf-Si-O films and the metal electrode work functions are determined, and simple models for the compositional dependence of the dielectric constant are formulated. Capacitors with the same dielectric composition and thickness exhibited 100 mV Vfb change when the thickness of the ALD TaN electrode layer was changed. This change is attributed to a change in the work function of the aggregate TaN / Ta metal electrode. Workfunctions were found to be located near middle of the Si band gap, with workfunctions of 4.6 eV to 4.7 eV.

9:30 AM D4.4
High-κ Interface Engineering: the Interaction of Reactive Metal Electrodes with ALD-ZrO_2/SiO_2 and HfO_2/SiO_2 Gate Stacks. Hyoungsub Kim[1], Paul C. McIntyre[1], Susanne Stemmer[2], Chi On Chui[3] and Krishna C. Saraswat[3]; [1]Materials Science and Engineering, Stanford University, Stanford, California; [2]Materials Department, University of California, Santa Barbara, California; [3]Electrical Engineering, Stanford University, Stanford, California.

Continued transistor scaling requires the use of high-κ gate dielectric materials in order to increase the gate capacitance while maintaining the low gate leakage current. Available metal oxide deposition techniques including atomic layer deposition result in the unavoidable formation of a thin interfacial oxide layer. Because this thin interfacial layer generally has a low dielectric constant, it seriously limits the further scaling of equivalent oxide thickness (EOT) for future high-speed transistors. In this study, we demonstrate the use of a reactive thin metal electrode which can result in decomposition of the thin SiO_2-based interfacial layer, thus greatly reducing the EOT of high-κ gate stacks. We characterized the microstructural and electrical properties of ALD-ZrO_2 and HfO_2 dielectrics on Si substrates after removal of the interfacial oxide. To prepare high-κ dielectric films, ZrO_2 and HfO_2 films were deposited using atomic layer deposition (ALD) on Si substrates passivated by a thin chemical oxide layer. Pt, Al, and Ti were deposited as gate electrodes via room temperature e-beam evaporation. Microstructural and chemical analyses were performed using a HR-TEM, EELS, and annular dark field STEM imaging. Electrical properties such as C-V and I-V characteristics were compared using capacitor structures fabricated through a shadow mask process. In the case of Al metal electrodes, the ALD-ZrO_2 films reacted with the Al and a thin interfacial oxide, which is believed to be Al_2O_3, was observed. For the Ti electrode case, the interfacial oxide between the high-κ film and the Si substrate was completely removed for both metal oxides, which was confirmed by various TEM and electrical characterization methods. A proposed SiO_2 reduction mechanism based on oxygen solubility in the Ti electrode will be presented.

9:45 AM D4.5
The characterization of hafnium nitride films as gate-electrode synthesized by MOCVD. Yukihiro Shimogaki and Wen Wu Wang; Dept. of Materials Engineering, Univ. of Tokyo, Tokyo, Japan.

With the continued scaling of MOS (Metal-Oxide-Semiconductor) transistor dimensions, the replacement for poly-Si with metal electrodes is becoming necessary. In this work, the composition and interfacial characteristics of hafnium nitride (HfN) formed by MOCVD were investigated for the first time as the metal gate electrode of MOS devices. The growth of HfN thin films was carried out on Si substrate with thermal oxides by means of MOCVD technique using tetrakis-diethylamido hafnium ($Hf[N(C_2H_5)_2]_4$:TDEAHf) precursor and ammonia (NH_3). The composition, electrical and interfacial properties were investigated by XPS, SIMS, TEM and four-point probe technique, respectively. As a result, the HfN films with good quality were fabricated, and the impurities of O and C remained in the films were below the detection limit of XPS depth profile analysis. The interface between HfN and SiO_2 substrate was very smooth and uniform from TEM image, whereas based on the measurement of XPS depth profile analysis, very thin HfOxNy interfacial oxide layer, which is a kind of high-k material, was formed during deposition. This interfacial layer slightly changed with the variation of experimental conditions and pretreatment process. This indicated that O diffusion from SiO_2 substrate may occur and promote the growth of HfOxNy thin layer, which can further reduce the equivalent oxide thickness (EOT). In addition, the application of Ar ions bombardment may optimize the N/Hf ratio of films; furthermore improve the resistivity of HfN films. The CV characteristics of $HfN/SiO_2/Si$ and $HfN/HfO_2/Si$ structure will be reported at the conference.

SESSION D5/B5: Joint Session: High-k and High-Mobility Substrates
Chairs: Matty Caymax and Akira Toriumi
Wednesday Morning, April 14, 2004
Room 2004 (Moscone West)

10:15 AM *D5.1/B5.1
Novel Deposition Processes for High-k/Ge Devices: Interface Engineering. Paul McIntyre[1], Hyoungsub Kim[1], David Chi[1], Chi On Chui[2], Baylor Triplett[1], Ali Javey[3], Hongjie Dai[3] and Krishna Saraswat[2]; [1]Materials Science and Engineering, Stanford University, Stanford, California; [2]Electrical Engineering, Stanford University, Stanford, California; [3]Chemistry, Stanford University, Stanford, California.

High permittivity dielectric materials and metal gate electrodes are currently being investigated by many research groups world-wide in an effort to continue the aggressive dimensional scaling of metal oxide semiconductor devices. The development of relatively high-quality deposited gate dielectrics to replace SiO2-based dielectrics for silicon field effect transistors presents an opportunity to consider alternative materials for the semiconductor channel in such devices. There are many fundamental advantages to using Ge in the channel in place of Si. The relative instability of GeO2 with respect to most high-k metal oxides under oxidizing conditions may avoid growth of an undesirable low-k interface layer under the deposition conditions used to form the high-k gate dielectric, in contrast to the typical situation for high-k deposition on Si. Furthermore, use of Ge may result in lower temperatures for dopant activation compared to Si. The larger (and better-matched) low-field carrier mobilities in Ge relative to Si result in devices that operate beyond the universal mobility model for Si MOSFETs. In this presentation, results obtained from atomic layer deposition- and UV-ozone oxidation-synthesized metal oxide dielectric layers on Ge (100) substrates will be compared. Physical characterization of HfO2 and ZrO2 gate dielectric layers and their interfaces with different Ge surface passivations will be emphasized. Recently published electrical data obtained from MOSCAP structures and high-k Ge MOSFETs will also be reviewed. The presence and effects of interface states on electrical behavior will be discussed, including comparison with results obtained from high-k/SiO2/Si and high-k/carbon nanotube devices.

10:45 AM D5.2/B5.2
Synchrotron Radiation Photoemission Spectroscopy of High-k Gate Stack in High-performance Ge MOS Devices. Chi On Chui[1], Dong-Ick Lee[2], Andy A. Singh[2], David Chi[3], Paul C. McIntyre[3], Piero A. Pianetta[2] and Krishna C. Saraswat[1]; [1]Electrical Engineering, Stanford University, Stanford, California; [2]Stanford Synchrotron Radiation Laboratory, Menlo Park, California; [3]Materials Science and Engineering, Stanford University, Stanford, California.

The saturation of Si MOSFET drain current upon dimension shrinkage may limit the prospect of future scaling. The lower effective mass (and lower valley degeneracy) of Ge could alleviate the problem by providing a higher source injection velocity, which translates into higher drive current and smaller gate delay. Nonetheless, unlike Si, the poor quality Ge native dielectrics for gate insulator and field isolation have hindered the realization of Ge MOS devices in the last four decades. Inspired by the recent successes of the high-k dielectric deposition technique on Si and the thermodynamically unstable nature of the common germanium native oxides, we have investigated the possibility of applying high-k dielectrics to Ge without a native oxide interlayer. We have fabricated MOS capacitors on Ge with zirconia gate dielectric using ultraviolet-assisted ozone (UVO) oxidation of thin Zr metal at room temperature on Ge surface with various treatments. In addition, this novel dielectric technology has led to the demonstration of high-performance Ge MOSFETs with enhanced carrier mobility. To study the scalability of the gate stack and inspect the existence of an interfacial layer, high-resolution cross-sectional transmission electron microscopy (HR-XTEM) was used to examine the ZrO2-Ge interface microstructure; though the poor phase contrast between ZrO2 and GeOx (if any) mandates a better physical characterization. In this presentation, we analyze the elemental composition variation across the dielectric layer by applying synchrotron radiation photoemission spectroscopy (SR-PES) to ZrO2 on Ge samples wet etched in an atomic layer scale. Core-level spectra for Ge have been taken at specific kinetic energies to minimize the Zr subshell photoemission cross-section and thus avoiding interference. These spectra were then peak-fitted and modeled to map out the elemental depth profile. Lastly, their impact on future Ge MOSFET scaling will be addressed.

11:00 AM D5.3/B5.3
integration of high-K dielectrics and metal gate electrodes with strained silicon channels. Yanxia Lin, Veena Misra and Mehmet C. Ozturk; Electrical and Computer Engineering, North Carolina State University, Raleigh, North Carolina.

Strained Si devices can provide significant mobility enhancements for both electrons and holes and is being aggressively studied by many research groups. The incorporation of high-K dielectrics on strained silicon provides the additional benefit of low gate leakage current. In addition, to eliminate gate depletion problems and Fermi level pinning associated with polysilicon electrodes, metal gates are also necessary. This warrants the investigation of high-K gate dielectrics and metal gate electrodes with strained Si devices. Issues that need to be understood include the i) interfacial layer formation of strained Si/high-K dielectrics, ii) effects of metal gate electrodes on high-K dielectrics, and iii) corresponding effects on the channel strain. In this paper, strained Si films were deposited on <100> relaxed SiGe virtual substrate by rapid thermal chemical vapor deposition (RTCVD). Different Ge compositions in the SiGe substrate and different strained Si thickness were formed to introduce varying strain levels which were confirmed by Raman spectroscopy. HfO2, one of the most promising high-K gate dielectrics, was deposited by physical vapor deposition (PVD) of thin Hf layers followed by oxidation at 600 C in N2 for 30seconds. Different metal gate electrodes, both element metal and binary metal alloys, were deposited by PVD and MOS capacitors were fabricated. The paper will discuss the electrical characteristics of metal-gate high-K dielectrics and present a comparison of EOT, flatband voltage, interface traps, leakage current and work function between strained Si samples and bulk Si controls. Also the interfacial layer formation of strained Si/high-K system will be investigated and compared with bulk Si/high-K. Finally, thermal stability of EOT, flatband voltage will also be presented.

11:15 AM D5.4/B5.4
Physical characterization of HfO2 deposited on Ge substrates by MOCVD. Sven Van Elshocht, Bert Brijs, Matty Caymax, Thierry Conard, Stefan De Gendt, Stefan Kubicek, Marc Meuris, Bart Onsia, Olivier Richard, Ivo Teerlinck, Jan Van Steenbergen, Chao Zhao and Marc Heyns; IMEC, Heverlee, Belgium.

Germanium is currently under consideration as a way to improve transistor performance because of its, compared to Si, intrinsically higher mobility. Germanium oxide, however, is inherently thermodynamically unstable, preventing formation of the gate dielectric by simple oxidation. A solution might be a high-k dielectric as much progress has been made depositing thin high-quality layers. Also from a high-k point of view germanium might prove to be beneficial: the instability of germanium oxide could limit the formation of an interfacial layer allowing more aggressive scaling; and the higher mobility might (partly) compensate for the mobility degradation seen for high-k dielectrics on Si. We studied the growth properties of HfO2 deposited on Ge by MOCVD, using TDEAH and O2 as precursors, and compare the results to similar layers deposited on silicon substrates. Analysis techniques include Ellipsometry, Rutherford Backscattering Spectroscopy (RBS), Transmission Electron Microscopy (TEM), X-Ray Diffraction (XRD), and Time Of Flight Secondary Ion Mass Spectroscopy (TOFSIMS). Our results show that the physical properties of MOCVD-deposited HfO2 layers on Ge are very similar to what we have observed in the past for Si. Some of the negative aspects observed for Si, such as diffusion of substrate material in the high-k layer, a low density for thin layers, or a rough top surface, are comparable or more pronounced for the case of Ge. However, a careful surface pretreatment such as NH3 annealing the Ge substrate prior to deposition greatly improves the physical characteristics. Most important observation is a very thin interfacial layer as predicted, offering more aggressive scaling possibilities for Ge. In conclusion, based on physical characterization, the deposition of HfO2 on Ge by MOCVD results in layers of comparable quality compared to Si with as major difference a much thinner interfacial layer. Similar as for Si, surface pretreatments are shown to be very important.

11:30 AM D5.5/B5.5
Retarded Growth of Sputtered HfO_2 Films on Germanium. Koji Kita, Masashi Sasagawa, Masahiro Toyama, Kentaro Kyuno and Akira Toriumi; Dept. of Materials Science, The Univ. of Tokyo, Tokyo, Japan.

Ge CMOS has recently attracted much attention, because of the trend of using deposited high-k films than thermally grown SiO_2 for further scaling of CMOS devices, and of the intrinsically higher carrier mobility of Ge than that of Si. In this paper, we report a new advantage of high-k/Ge systems over high-k/Si, that both the interface layer and the HfO_2film on Ge are thinner than those on Si despite of simultaneous fabrication processes. HfO_2 films were deposited simultaneously on Ge (100) and Si (100) wafers, after removing the native oxides. In order to restrict the interface layer growth, an ultra-thin Hf metal layer was deposited, followed by the HfO_2 film deposition by a reactive sputtering of Hf in O_2/Ar. By using TEM and a combination of the glazing incidence x-ray reflectivity (GIXR) with the spectroscopic ellipsometry measurements, the interface layer thickness was accurately determined to be 0.5 nm on Ge and 1.1 nm on Si, for the samples annealed at 500°C in O_2 (0.1%) $+N_2$ ambient. This result shows that the interface layer thickness on Ge is only a half of that on Si even though the films on both substrates were processed simultaneously. The ultra-thin Hf metal layer has an important role for thinner interface layer formation on Ge, since no difference of interface layer thickness was observed when HfO_2 films were deposited directly on both substrates without Hf metal layers. This phenomenon can be explained if it is assumed that Ge oxides may form a Hf-Ge-O ternary volatile compound with Hf metal. If this is the case, the total HfO_2 film thickness (without the interface layer) on Ge must be thinner than that on Si. The fact is that the HfO_2 film on Ge was 0.6 nm thinner than that on Si with TEM and GIXR measurements. Furthermore, the film thickness difference ($\Delta T_{HfO2} = T_{HfO2(onSi)} - T_{HfO2(onGe)}$) was detected even without annealing, and then it can be assumed Hf-Ge-O volatilization would occur during the film deposition process. It is worthy of particular attention that ΔT_{HfO2} was seen as a retardation of the film growth on Ge in the very early stage of the growth. Thus it is inferred that the Hf-Ge-O volatilization would occur with the assistance of oxygen plasma until the ultra-thin Hf metal is fully oxidized, and that it is the key mechanism for forming a thinner interface layer and a thinner HfO_2 film on Ge than those on Si. Finally, C-V characterisitcs of Au/HfO_2/Ge and Au/HfO_2/Si MOS capacitors were characterized. As was expected from the thickness difference of both interface layer and HfO_2 film discussed above, HfO_2/Ge MOS capacitor showed a larger accumulation capacitance than HfO_2/Si, even though they were fabricated simultaneously by the same process. These results show a new advantage of high-k/Ge over high-k/Si system from the viewpoint of fabricating a CMOS with ultra-thin high-k gate dielectric.

11:45 AM D5.6/B5.6
Metal Oxide/Semiconductor Interfaces in UV-Ozone Oxidized High-κ Dielectric Stacks on Si and Ge (001) Substrates. David Chi[1], Chi On Chui[3], Shriram Ramanathan[2], Baylor Triplett[1], Krishna C. Saraswat[3] and Paul C. McIntyre[1]; [1]Department of Materials Science & Engineering, Stanford University, Stanford, California; [2]Components Research, Intel, Hillsboro, Oregon; [3]Department of Electrical Engineering, Stanford University, Stanford, California.

UV-ozone oxidation of hafnium and zirconium metal films to form HfO_2 and ZrO_2 gate dielectrics has been demonstrated to yield MOS gate stacks with low leakage current densities and very high capacitance densities. In this technique, metal precursor films are deposited directly on to the substrate and are subsequently transformed to metal oxides by exposure to oxygen in the presence of UV light. Because both Hf and Zr are highly reactive metals, interaction with the substrate after deposition but before oxidation is likely. In this presentation we describe characterization of the interface between UV-ozone oxidized dielectrics and Si and Ge substrates. We demonstrate reduction of the native oxide above Si and Ge as a result of Hf or Zr deposition. However, during UVO processing, oxidation of the substrate is observed. This byproduct silicon oxide exhibits different properties than the native oxide of Si. X-ray photoelectron spectroscopy indicates a sub-oxide or silicate/germanate at the high-k/substrate interface. Results from electrical testing of MOS-capacitors with a range of oxide thicknesses will also be presented.

SESSION D6: Theory - Physical, Chemical, and Electrical Characterization I
Chairs: Ed Cartier and Jonder Morais
Wednesday Afternoon, April 14, 2004
Room 2006 (Moscone West)

1:30 PM *D6.1
Electrical modeling and simulation of nanoscale MOS devices with a high-permittivity dielectric gate stack. Jean-Luc Autran[1], Daniela Munteanu[1] and Michel Houssa[2]; [1]L2MP-CNRS, Marseille, France; [2]IMEC, Leuven.

High-permittivity dielectrics are currently widely investigated for the replacement of SiO2 as gate insulator in (deca)nanometer MOSFETs. A major reason is that scaling of the SiO2 layer thickness at this scale of integration approaches its limits, especially from the point-of-view of gate leakage current limitation. Much effort has recently been devoted to the understanding of the electrical properties of MOS devices with high permittivity gate dielectrics as well as to the investigation of defects present in these materials. In this work, numerical simulations are used to explore and predict the effect of

some fundamental limitations of high-k materials on the electrical response of MOS capacitors and nanoscale transistors. Two important current limitations have been considered: the trapped charge fluctuations in the high-k layer and the physical dielectric thickness versus its equivalent-oxide-thickness (EOT) for very high-k materials. The first one is now well-identified to induce a stretch-out of the capacitance-voltage characteristics and threshold voltage dispersion, the second problem is known to be at the origin of the loss of the electrostatic control of the channel by the gate electrode. In both cases, we will illustrate with simulation results the importance of these two problems for decananometer devices and we will push our investigations to ultimate double-gate devices working in the ballistic regime.

2:00 PM D6.2
Electronic structure of Nitrided High K gate oxides.
John Robertson, P W Peacock and G Shang; Engineering, Cambridge University, Cambridge, United Kingdom.

Nitrogen is often added to gate oxides to improve their reliability, performance, either by co-oxidation or deposition, or by annealing in a nitrogen containing atmosphere. This is also true for high dielectric constant oxides such as HfO2 or the silicates and aluminates. We have calculated the effect of nitrogen on the electronic structure of the oxides. Nitrogen atoms were added to supercells of HfO2, La2O3 and HfSiO4, withdrawing oxygens so as to maintain an insulating configuration. The total energy of the structure was relaxed to find the equilibrium configuration. We find that in general nitrogen prefers a 4-fold coordinated configuration. We find that N introduces N 2p states above the oxide valence band maximum. This narrows the band gap by about 1.2 eV. This reduces the valence band offset. Neverthless, we find that even in La2O3 which has a smaller VB offset, the offset is still large enough to act as an adequate hole barrier. The conduction band offset remains large enough.

2:15 PM D6.3
Ab Initio Dielectric and Dynamical Properties of High-k Oxides. Alessio Filippetti, Pietro Delugas and Vincenzo Fiorentini; Dept. of Physics, University of Cagliari, Monserrato, Italy.

We present ab initio density-functional-theory calculations of the lattice structure, dynamical Born charges, vibrational, IR and Raman spectra, dielectric constants, and band structure of selected high-k oxides candidate to replace silica as gate insulators in CMOS integrated circuits. We employ a combination of ab initio total-energy [1], linear-response [2], finite-field [3], and self-interaction correction [4] methods. We concentrate on the complex bixbyite-structure oxide Lu2O3 and on the perovskite LaAlO3, comparing our calculations with recent experiments. [1] M. Payne et al., Rev. Mod. Phys. 64, 1045 (1992) [2] P. Giannozzi et al., Phys. Rev. B 43, 7231 (1991) [3] I. Souza et al., Phys. Rev. Lett. 89, 117602 (2003) [4] A. Filippetti and N. A. Spaldin, Phys. Rev. B 67, 125109 (2003)

2:30 PM D6.4
Defect Levels in SrTiO3, HfO2, ZrO2 and La2O3. K Xiong, P W Peacock and John Robertson; Engineering, Cambridge University, Cambridge, United Kingdom.

The leakage currents, stability and reliability of high dielectric constant (K) gate oxides will depend on their intrinsic defect energy levels. There have been few calculations of these defect levels. In many cases, for those levels high in the band gap, the results are affected by the correction of the band gap for the error in the local density formalism used. Here we find the energy levels and behaviour of oxygen vacancies in key oxides, by referencing the levels to those of possible shallow donors next to the conduction band edge. This is the so-called 'marker method' which has been used for wide gap systems like diamond. The method is tested on oxygen vacancies in SrTiO3 using substitutional La as a reference. The vacancy is found to be shallow, as in experiment. It is then used for O vacancies in ZrO2, where the results correspond well to those of Louie et al using the GW approximation. These results allow us to build up a more accurate picture of the vacancy and interstitial levels in these wide gap oxide systems.

3:15 PM *D6.5
Physical and electrical characterization of MBE deposited high-κ dielectrics. Athanasios Dimoulas[1], George Apostolopoulos[1], George Vellianitis[1], Jacob C. Hooker[2], Zacharias M. Rittersma[2], Tierry Conard[3], Luigi Pantisano[3], Marco Fanciulli[4], Claudia Wiemer[4], Marin Alexe[5] and Bogdan Mereu[5]; [1]NCSR "DEMOKRITOS", Athens, Greece; [2]Philips Research Leuven, Leuven, Belgium; [3]IMEC, Leuven, Belgium; [4]Laboratorio MDM, INFM, Agrate (Milano), Italy; [5]Max-Planck Institute, Halle, Germany.

Using molecular beam epitaxy (MBE) we investigated a number of oxides such as Y_2O_3 or La_2O_3 and its combinations with HfO_2 and Al_2O_3 with the aim to obtain high- gate dielectrics for aggressive scaling of mainstream devices with EOT well below 1 nm. We focus on electrically active defects which cannot be determined using standard methodologies based on quasi-static C-V measurements because of the high density of these defects and the high leakage current. Based on previous work [1], we developed a new multi-frequency model for the analysis of complex admittance measurements on MOS capacitors where the C-V and G-V curves are fitted simultaneously to extract values of the EOT, VFB, the carrier capture cross-section cn,p and the energy distribution of interface traps in the gap, which is then compared with values obtained by more conventional G-measurements. Interestingly, in several cases the capture cross-section of holes is found to be in the 10^{-17} cm^2 range, which is lower by at least an order of magnitude compared to the SiO_2/Si interfaces. This has certain implications regarding the influence of the high- medium on the potential of the trap centers which will be discussed in detail. Using newly developed methodologies based on injector structures, we measured the pristine oxide defects, which trap carriers leading to electrical instabilities. Remarkably, the concentration of such defects in La containing materials such as the $La_2Hf_2O_7$ compound is significantly reduced compared to MBE or ALD HfO_2, which could be advantageous for the reliability of high- transistor devices. Several other factors which may influence the electrical quality of the high- layers, such as the stability of the oxides on silicon, the microstructure, the Si in-diffusion and the mass density of the oxides were studied using a large variety of in-situ and ex-situ analytical methods such as RHEED, HRXRD, XRR, HRTEM, ToF SIMS and XPS. [1] P. Masson et al., Appl. Phys. Lett. 81, 3392 (2002).

3:45 PM D6.6
Measurement of high-k dielectric stacks for nonvolatile memory applications by internal photoemission.
Julie D. Casperson[1], L. Douglas Bell[2], Robert J. Walters[1], Damon B. Farmer[3], Roy G. Gordon[3] and Harry A. Atwater[1]; [1]Watson Laboratory of Applied Physics, California Institute of Technology, Pasadena, California; [2]Jet Propulsion Laboratory, Pasadena, California; [3]Department of Chemistry, Harvard University, Cambridge, Massachusetts.

Solid state memory device speeds are limited by electron tunneling through the gate dielectric barrier. By fabricating dielectric gates from multiple layers of dielectric materials, with appropriate band offsets and dielectric constants, voltage application causes the electron tunneling barrier to be lowered, resulting in significantly faster read/write times, without sacrificing retention time. Such silicon-compatible layered barrier heterostructures that enable a large drop in the barrier height with applied voltage are promising candidates to replace single dielectric films as the tunnel barriers for nonvolatile memories. Floating gate MOS capacitor structures have been fabricated using these heterostructures as the tunnel barrier and results will be presented. Additionally, the voltage-dependent barrier lowering may also form the operating principle for a new class of photodetectors with electrically-tunable cutoff wavelengths. We have modeled and fabricated silicon-compatible, layered high-dielectric constant structures that enable carrier injection from a silicon channel to a floating gate or contact electrode that can be modulated by an applied bias. We utilize an effective mass-based tunneling model to predict the current-voltage characteristics and carrier distributions in layered tunnel barrier structures under applied bias. We find from our simulations that some of the most promising structures for layered tunnel barriers consist of Al_2O_3 with HfO_2 and we have fabricated such structures. We have fabricated and characterized the layered barrier structure HfO_2 /Al_2O_3/HfO_2 as well as single- and double-layered structures using these materials. The Al_2O_3 and HfO_2 were deposited by atomic layer deposition. Experimental characterization of tunneling and band offsets has been performed using current-voltage, capacitance-voltage, and internal photoemission spectroscopy measurements. Internal photoemission spectroscopy measurements have been performed on metal-insulator-semiconductor structures with semi-transparent gates in order to directly measure the band offsets of layered tunnel barriers using a tunable arc-lamp source for illumination. Our measurements indicate band-offsets for SiO_2 and Al_2O_3 to be 3.5 eV and 3.1 eV, respectively. Measurements for other single dielectrics and heterostructures will be presented.

4:00 PM D6.7
Pr4f occupancy and VB/CB band offsets of Pr2O3 at the interface to Si(001) and SiC(0001) surfaces. Dieter Schmeisser, [1]Applied Physics, BTU Cottbus, Cottbus, Germany; [2]IHP, Frankfurt, Germany.

Resonant photoelectron spectroscopy (PES) at the Pr4d and Pr3d absorption edges is used to study the electronic properties at the interface of epitaxial grown Pr2O3 on Si(001). We com-pare these results to Pr2O3 films grown on SiC(0001) surfaces. In the electronic structure of bulk Pr2O3 the valence band (VB) states are predominantly of Pr6s and O2p atomic parentage. Weak contributions

from Pr4f states are identified from the strong increase the VB features at the Pr4d and Pr3d resonances. They are the consequence of mixed valency caused by ligand-to-Pr4f charge transfer states. On SiC(0001) surfaces Pr2O3 films are prepared by a wet chemical treatment. Here the oxide forms an amorphous layer. There is an intermediate range of about 1nm thickness in which a silicate is formed. At the Si(001) interface in-situ prepared epitaxial layers (d<5nm) enable us to study the con-tribution of the Pr4f electronic states in the valence band population as a function of layer thickness. We also find a silicate intermediate. In that range (1nm) the weak occupancy of the Pr4f states in the bulk phase of Pr2O3 is significantly enhanced. There is an additional 4f state which appears right at the valence band maximum (VBM). On the other hand, in the XAS data we find the features of localized Pr4f states to be quenched. We conclude that the silicate causes an enhanced hybridization (covalent bonding) of the Pr4f states into the valence band. In our coverage dependent data the offset in the VB maxima is determined from the relative position of the valence band spectra. We find an offset of 2eV as well as a 1eV increase in the electron affinity caused by an interface dipole moment. In addition, there is a negative space charge within first 1nm of the Pr2O3 layer, most probably caused by Pr vacancies. The offset of the conduction bands is deduced from the onset of the Si2p and Pr4d XAS data, it is of the order of 2eV again. Our data allow to derive a full description of the interface properties of that high K material, a prerequisite for its possible application in storage, logic, and power electronics.

4:15 PM D6.8
The physical metrology of high-k layers: how can we obtain an accurate measurement of composition and thickness?
Thierry Conard[1], Hugo Bender[1], John Wolstenholme[2], Roumen Vitchev[3], Laurent Houssiau[3], Andreas Bergmaier[4] and Wilfried Vandervorst[1]; [1]MCA, IMEC, Leuven, Belgium; [2]ThermoVGScientific, East Grinstead, United Kingdom; [3]LISE, FUNDP, Namur, Belgium; [4]University of Munich, Munich, Germany.

With the downscaling of the gate insulator (SiO2) in advanced metal-oxide-semiconductor (MOS) devices, one expects its thickness to reach the fundamental limits both from the point of view of gate leakage current as well as from intrinsic reliability. A solution to this problem is the use of dielectric layers with higher electrical permittivity than SiO2. Consequently, alternative gate insulators with high electrical permittivity are currently widely investigated for the future generations of MOS transistors. The mainstream research concentrates on Hf based oxide systems but the understanding of the physical properties of these films remains a challenge. Many different analysis techniques are usually considered for the determination of thickness and/or composition of thin layers. Among those, one usually finds Ellipsometry, TEM, XPS, TOFSIMS, XRR, ERD, RBS ... In the first part of this study we concentrate on the metrology aspect of the analysis of those layers through the intercomparison of results obtained on a limited set of sample composed of HfO2, Al2O3 and their mixture. From these analysis we were able to determine the necessary physical parameters (electron mean free path, dielectric function, ...) to get a coherent characterisation with the different techniques. Recent development in the field of high-k dielectrics include the presence of nitrogen in or around the stack (interfacial layers and/or nitride capping layer). In this study, both MOCVD and ALCVD layers will be considered. For the performance of the devices, it is very important to be able to acquire knowledge of the depth distribution of the nitrogen in the layers with enough accuracy. This remains a real challenge for SIMS due to varying matrices in which the nitrogen is distributed. Next to the usual operational mode (Xe, Ar and Cs profiling in positive and negative detection mode), we investigated the possibility of nitrogen detection through the use of MCs+ clusters while reducing surface Cs concentration at low energy by a Xe-Cs co-sputtering set-up. We also recently introduced the possibility to detect nitrogen through the detection of CN- clusters by a carbon flooding scheme. This work has been extended now and its results will be validated against some known layer structure.

4:30 PM D6.9
Structural Properties of (ZrO2)x(Al2O3)1-x on Si (100).
Ming Zhu[1,2], Peng Chen[1], Ricky K. Y. Fu[1], Weili Liu[2], Chenglu Lin[2] and Paul K. Chu[1]; [1]City University of HongKong, Hong Kong, Hong Kong; [2]Shanghai Institute of Microsystem and Information Technology, Shanghai, China.

(ZrO2)x(Al2O3)1-x composite films were deposited on p-type Si (100) substrate by ultra-high vacuum electron-beam co-evaporation at room temperature, followed by rapid thermal annealing (RTA) conducted in N2 ambient for 30s at 100?C increments between 800?C and 1100?C. X-ray diffraction (XRD) was conducted to determine the crystallization temperature and high-resolution transmission electron microscopy (HRTEM) was used to study the interfacial quality and the morphology of the (ZrO2)x(Al2O3)1-x film annealed at 900?C. The chemical compositions and thermal stability of the annealed samples were determined by x-ray photoelectron spectroscopy (XPS) and the current-voltage characteristics were measured by producing a metal/DLC/Si MIS structure. Our results show that the amorphous structure of the (ZrO2)0.67(Al2O3)0.33 film is maintained up to a post-annealing temperature of 900?C, and the higher the Al concentration, the higher the crystallization temperature. Moreover, the expansion of the interfacial layer at high temperature is suppressed and the structure of the (ZrO2)0.67(Al2O3)0.33 film is stable up to 900?C. These phenomena can be explained as follows. It is known that an interfacial silicate layer is formed due to excessive oxygen in the deposition chamber or the annealing furnace diffusing into the interface. Our (ZrO2)0.67(Al2O3)0.33 film does not crystallize at 900?C, and so a much smaller amount of oxygen can diffuse along the grain boundaries in the film. Moreover, since Al2O3 is known to have a much lower oxygen diffusion coefficient compared to ZrO2 at high temperature, the (ZrO2)x(Al2O3)1-x film becomes a better oxygen barrier than pure ZrO2. Hence, the interfacial oxide and silicate layer cannot form without excess oxygen. Moreover, the leakage current density of (ZrO2)0.67(Al2O3)0.33 film at a gate voltage of 1 V is about 2E-7 A/cm2 indicating excellent leakage current properties. Hence, the (ZrO2)x(Al2O3)1-x film is a promising candidate for SiO2 gate dielectric in MOSFETs.

4:45 PM D6.10
On the nature of weak spots in high-k layers submitted to anneals. Jasmine Petry[1,2], Wilfried Vandervorst[1,2], Olivier Richard[1], Thierry Conard[1], Peter Dewolf[4], Vidya Kaushik[3], Annelies Delabie[1] and Sven Van Elshocht[1]; [1]SPDT/MCA, IMEC, Leuven, Belgium; [2]INSYS, KULeuven, Leuven, Belgium; [3]International Sematech c/o IMEC, Leuven, Belgium; [4]Veeco Instruments S.A., Dourdan, France.

In the path to the introduction of high-k dielectric into IC components, a large number of challenges have still to be solved. Some of the major issues concern the low mobility of carriers and the reliability of the device. Trapped charges in the stack have been identified as being the cause of these issues. With this in view, we used Conducting Atomic Force Microscopy, combined with physical analysis to discover the nature of these charges. In this contribution, we have studied the uniformity of thin HfO2 and HfSiO layers, with and without anneal. The Conducting Atomic Force microscopy measurements showed spots of higher conductivity. Recording local current voltage curves in those weak spots suggests that they consist of positive charge. On the other hand, XPS and ToFSIMS analysis show a diffusion of the interfacial SiO2 upwards into the high-k layer. Finally, the comparison of samples with differing high-k material and crystallinity indicates a strong correlation between the weak spots and the presence of silicon in the film.

SESSION D7: Silicates and Nitrogen Incorporation into High-k Layers
Chairs: Jean Fompeyrine and Michel Houssa
Thursday Morning, April 15, 2004
Room 2006 (Moscone West)

8:30 AM *D7.1
A Review of HfSiON Gate Dielectrics Luigi Colombo, Texas Instruments, Inc., Silicon Technology Development, Dallas, Texas.

Hafnium based dielectrics are the most common high-k gate dielectrics being investigated today to replace the incumbent reliable silicon oxynitride. While many have reported on both HfO_2 and HfSiON, HfSiON has better thermal stability against crystallization, has better electrical stability such as EOT degradation and leakage current degradation with annealing, can be scaled to < 1nm with poly Si, has less trapped charge, and has higher channel mobility. Overall, based on the data available HfSiON is a robust dielectric. However many high-k gate dielectrics including HfSiON have a large flat band offset with respect to the expected flat band voltage. The objective of this presentation is to review HfSiON basic materials characteristics, deposition processes, dielectric scaling, thermal and electrical stability characteristics, reliability properties and limitations poly Si gates.

9:00 AM D7.2
Nitrogen distribution in HfO_xN_y gate dielectrics deposited by MOCVD using $[(C_2H_5)_2N]_4Hf$ with NO and O_2. Minsoo Lee[1], Dolf Landheer[2], Xiaohua Wu[2], Martin Couillard[3], Zhenghong Lu[1], Wai Tung Ng[4] and Gianluigi Botton[3]; [1]Materials Science and Engineering, University of Toronto, Toronto, Ontario, Canada; [2]Institute for Microstructural Science, National Research Council Canada, Ottawa, Ontario, Canada; [3]Brockhouse Institute for Materials Research, McMaster University, Hamilton, Ontario, Canada; [4]Electrical and Computer Engineering, University of Toronto, Toronto, Ontario, Canada.

Crystallization temperatures of less than 500 °C and high impurity

diffusion rates are serious concerns if HfO_2 is to replace silicon oxynitride as a gate dielectric in deep submicron CMOS applications. Nitrogen incorporation was reported to improve these properties in sputter-deposited HfO_2 films [1]. This paper describes the deposition and characterization of HfO_xN_y gate dielectrics deposited by metal organic chemical vapor deposition (MOCVD) using tetrakis(diethylamido)hafnium (TDEAH, $[(C_2H_5)_2N]_4Hf$) and NO. The films were analyzed by x-ray photoelectron spectroscopy (XPS), high resolution transmission electron microscopy (HRTEM), and electron-energy loss spectroscopy (EELS). Si <100> substrates were given an HF-last RCA clean and introduced into an ultra high vacuum cluster-tool with a low pressure MOCVD chamber, in-situ XPS spectrometer, and an evaporation chamber with a high-temperature quartz-halogen in-situ heating stage. By introducing TDEAH and oxidizing gas, either O_2 or NO, into the MOCVD system in separate pulses, we deposited high-purity HfO_xN_y films. The N 1s XPS peak had (N-O), (N-Hf) and (N-C) components due to N bonded to O, Hf, and C, respectively. The (N-C) component, due to un-reacted precursor at the surface, was removed by in-situ thermal annealing. The distribution of the N in the films was determined by EELS and by XPS coupled with etch-back in 1% HF solution. Using standard sensitivity factors for the O 1s (O-Hf), N 1s (N-Hf) and Hf 4f peaks the atomic concentration of nitrogen in the films deposited with NO as the oxidant was determined to be 11 $\pm$ 1 % while those deposited with O_2 was 4 $\pm$ 1 %. The interface layer deposited using O_2 was silicon dioxide, while with NO it was silicon oxynitride, but a contribution from sub-oxides cannot be ruled out. HRTEM images revealed that the HfO_xN_y films containing 11% nitrogen stayed amorphous following post-deposition anneal at 800 °C in vacuum. Oxidation of the films in O_2 using a rapid thermal processor resulted in a shift of the Hf 4f $^{7/2}$ XPS spectrum toward that of pure HfO2 at 17.9 eV and a reduction in the N 1s (N-Hf) peak, indicating that bulk nitrogen was replaced with oxygen. This reduction in N concentration was investigated by EELS analysis. We are grateful to S. Moisa and T. Quance for their expert technical assistance. [1] M. R. Visokay, J. J. Chambers, A. L. P. Rotondaro, A. Shanware, and L. Colombo, Appl. Phys. Lett., 80, 3183 (2002).

9:15 AM D7.3
Incorporation of N and H in High-k Dielectric Films. Leonardo Miotti[1], Rafael Pezzi[1], Karen Paz Bastos[1], Gabriel Vieira Soares[1], Carlos Driemeier[1], Jonder Morais[1] and Israel J. R. Baumvol[2]; [1]Institute of Physics, UFRGS, Porto Alegre, RS, Brazil; [2]Centro de Ciencias Exatas e Tecnologicas, UCS, Caxias do Sul, RS, Brazil.

The search for an alternative high-k material to replace the silicon dioxide as gate dielectric is currently a subject of intensive research. Most investigations have suggested the use of high-k films consisting of metal oxides and silicates. The integration of these new materials into the fabrication process of advanced VLSI technology relies on their stability during post deposition processing steps. Among the several critical issues involved, a successful high-k integration has to present electrical, structural and thermodynamical stability characteristics and a passivated high-k/Si interface. Recent investigations indicated that incorporation of nitrogen and hydrogen into the metal oxide and silicate films provided substantial improvements in the direction of overcoming the above mentioned requirements. We report here on nitrogen and hydrogen incorporation into HfSiO, HfSiON, HfSiN, and AlON films deposited on Si(001) by different deposition methods. Atomic transport, exchange, and loss of the involved species after post-deposition thermal processing steps (performed under different atmospheres) are also addressed. Isotopic substitutions of N, O, and H were used in order to be able to distinguish between species incorporated from the gas phase and those previously existing in the films. The areal densities of the involved species were determined, before and after post-deposition thermal processing, by Rutherford backscattering spectroscopy (RBS) and nuclear reaction analysis (NRA), whereas the concentration versus depth distribution of these species were determined by narrow nuclear reaction resonance profiling (NRP). The chemical environments were accessed by x-ray photoelectron spectroscopy (XPS) and the composition of the outermost atomic layer of some samples were determined by low-energy ion scattering (LEIS).

9:30 AM D7.4
Ozone-Based Atomic Layer Deposition of HfO2 and HfxSi(1-x)O2 and Film Characterization. Yoshi Senzaki[1], S.G. Park[1], John F. Conley[2], Douglas Tweet[2] and Yoshi Ono[2]; [1]Aviza Technology, Scotts Valley, California; [2]SHARP Laboratories of America, Camas, Washington.

A series of measurements were performed on five 20nm thick HfxSi(1-x)O2 films deposited by atomic layer deposition (ALD). HfxSi(1-x)O2 films were deposited from alternating supply of metal-organic Hf/Si source gases and ozone. The use of ozone allows process temperatures below 400C. Precise control of film thickness can be achieved as the film grows linearly with the number of chemical pulse cycles. Spectroscopic ellipsometry (SE) was performed on the as-deposited and annealed samples to determine susceptibility to densification. Electrical measurements were performed on capacitors formed from Pt evaporated dots with all samples showing high densities of trap states that disappear with a forming gas anneal. The leakage current densities for the silicates with x=0.4 and 0.6 were the lowest and suggests that a hafnium silicate may serve to reduce leakage and maintain carrier mobilities in a device structure. X-ray measurements revealed the film densities and thicknesses for the as-deposited and 1000C annealed samples. The densification with anneals seen in the SE measurements were confirmed. The as-deposited amorphous HfO2 and Hf0.8Si0.2O2 were crystallized after a 600C anneal. The HfO2 formed the well known monoclinic phase while the silicate formed a face-centered-cubic (fcc) structure. This fcc phase has only recently been mentioned in the literature [1] and may be important to developing high quality dielectric films. In this paper, ALD film deposition process of HfxSi(1-x)O2 films, where x = 0.2, 0.4, 0.6, 0.8, 1.0, and film characterization including composition, density, crystallinity, capacitance-voltage and current-voltage properties, and thermal anneal effect will be discussed. Ref.: [1] R.B. van Dover, et al., Appl. Phys. Lett. 83, 1459 (2003)

9:45 AM D7.5
Nitridation of Hafnium Silicate Thin Films. Hood Chatham[1], Yoshi Senzaki[1] and Wesley Nieveen[2]; [1]Aviza Technology, Inc., Scotts Valley, California; [2]Charles Evans and Associates/Evans Analytical Group, Sunnyvale, California.

High quality gate dielectrics with higher dielectric constant to replace SiO_2 are required to meet future device requirements as the integrated circuit device scale decreases. Conventional SiO_2 gate dielectrics suffer from leakage and reliability deficiencies as the silicon oxide thickness decreases below 1.8 nm. Acceptable high-k gate dielectric materials must be thermally stable with Si and provide good electrical properties. Metal oxides such as HfO_2, ZrO_2, and the silicate form of these materials have been studied as promising alternatives to SiO_2 [1], with the hafnium materials being the leading candidates. HfSiON is of particular interest as it remains amorphous and shows no leakage current degradation or increase in EOT (equivalent oxide thickness) even after annealing at 1100°C in an inert gas [2]. We have developed an atomic layer deposition (ALD)-based $Hf_xSi_{1-x}O_2$ (x = 0.1 to 1) process using volatile liquid precursors at temperatures $\leq$400°C. The use of ozone allows us to process at low temperatures and provides good electrical properties [3]. In this paper, we discuss the nitridation of ALD-deposited hafnium silicate films by either post-deposition NH_3 rapid thermal annealing or by remote nitrogen plasma annealing. Nitrogen concentration [N] as measured by X-ray photoelectron spectroscopy (XPS) is determined as a function of the annealing temperature and other process conditions for both nitridation methods. The effect of [N] on the electrical properties determined from the current-voltage and capacitance-voltage characteristics of HfSiON films with and without additional high temperature annealing. Information on the structure and properties of HfSiON and the resulting interface with silicon as determined by transmission electron microscopy (TEM) will be presented. References: 1. G. Wilk, R. M. Wallace, and J. M. Anthony, J. Appl. Phys., 89, 5243 (2001). 2. M. R. Visokay, J. J. Chambers, A. L. P. Rotondaro, A. Shanware, and L. Colombo, Appl. Phys. Lett., 80, 3183 (2002). 3. Y. Senzaki, S. G. Park, R. Higuchi, L. Bartholomew, H. Chatham, S. Al-Lami, C. Barelli, S.-I. Lee, A. Helms, Jr., 201th ECS Meeting, April 30, 2003, Paper#944.

10:30 AM *D7.6
Process Optimization and Integration of HfO_2 and Hf-Silicates. Hideki Takeuchi and Tsu-Jae King; Dept of Electrical Engineering and Computer Sciences, University of California-Berkeley, Berkeley, California.

In order to scale CMOS technology beyond the 50nm node, high-δ dielectrics will be necessary to replace SiO_2-based gate dielectrics. Although the candidate materials seem to have been narrowed down to Hf(hafnium)-based dielectrics through many research efforts over the past years, the optimal dielectric composition is still not evident. Besides, issues such as degraded carrier mobility, large V_{fb} shift, and charge trapping still need to be resolved, *i.e.* dielectric charge properties need to be well understood. In this work, we first investigated the compositional dependence of the scaling limit of Hf-silicate films, using a figure of merit introduced in the direct tunneling leakage current model for bulk-Si CMOS transistors. Pure HfO_2 is predicted to have an advantage over Hf-silicates. However, a HfO_2 film typically is accompanied by an interfacial layer which significantly increases the equivalent oxide thickness (EOT). By employing an interfacial Si_3N_4 diffusion barrier, the formation of this interfacial layer can be suppressed, to allow for more effective EOT scaling. Alternatively, if a relative permittivity of 11 can be achieved, 20%Hf-silicate (without an interfacial layer) can be more scalable than HfO_2 (with an interfacial layer). We have recently developed new

methodologies for characterizing the bulk and interface charge properties of dielectric films. Surface charge analysis (SCA) is used to extract interface state densities, fixed charge densities, and near-interface trap densities of ultra-thin dielectrics, and is useful for tracking the influence of post-deposition processing on the HfO_2/Si interface charge properties. Spectroscopic ellipsometry is used to obtain the absorption spectra in the band-tail region of HfO_2 films. An extra absorption peak is observed inside the bandgap of HfO_2, and its intensity is clearly correlated with leakage current and near-interface trap densities. Based on our observations, the defects within the HfO2 films are likely to be oxygen vacancies.

11:00 AM D7.7
High Quality HfSixOy Gate Dielectrics Fabricated by Solid Phase Reaction Between Metal Hf and SiO_2 Underlayer. Heiji Watanabe, Motofumi Saitoh, Nobuyuki Ikarashi and Toru Tatsumi; NEC Corporation, Sagamihara, Kanagawa, Japan.

High permittivity metal oxides, such as HfO_2 and its silicate, have been extensively studied as alternative gate dielectrics. The main concern with high-k gate devices is to improve the film and interface properties. Impurities in high-k films that were introduced from source gases must be eliminated, and the insertion of SiO_2 underlayers is indispensable to improve interface properties. Current research in high-k film fabrication has been concerned with depositing the metal oxides using CVD techniques. However, we think that high-quality film should be prepared by interface reactions just like oxidation at the SiO_2/Si interface. Previously, we proposed a novel high-k fabrication method based on interface solid phase reaction between metal and SiO_2 underlayer for preparing La-silicate gate dielectrics [1]. In this work, we report on fabrication of high-quality HfSixOy gate dielectrics by the solid phase reaction method and results from its physical and electrical characterization. Thin Hf-metal layers ranging from 0.2 to 1 nm thick were deposited on SiO_2 underlayers using low-damage PVD equipment. The PVD system has sufficient controllability and film uniformity. High-quality HfSixOy gate dielectrics were formed by diffusing Hf into the oxide underlayer. In this method, the metal composition and profile were controlled by the Hf layer thickness and annealing conditions. The permittivity of the oxide underlayer increases due to metal diffusion (Hf-silicate formation at the metal/SiO_2 interface) and, thus, the electrical thickness of the insulator becomes thinner than that of the initial SiO_2 underlayer. An EOT of less than 1 nm was achieved and we confirmed that the silicate films endured activation annealing. When using a conventional poly-Si gate electrode, the gate leakage reduction compared with SiO_2 ranged from two to four orders of magnitude depending on the amount of Hf metal. The interface trap density was in the order of 10^{10} $eV^{-1}cm^{-2}$ and hysteresis of C-V curves was as low as 10 mV (-2V - 2.5V). These results clearly indicate advantages to this solid phase reaction based method for the fabrication of high-quality high-k gate dielectrics. [1] H. Watanabe et al. Appl. Phys. Lett. 83 (2003) 3546.

11:15 AM D7.8
Effect of plasma and different oxygen precursors on stability of hafnium oxide and hafnium silicate thin films grown on Si(100). Harish Babu Bhandari, Ping Chen and Tonya M Klein; Department of Chemical Engineering, University of Alabama, Tuscaloosa, Alabama.

The downscaling of MOSFET devices has brought considerable attention to the possible high-k dielectric replacements for SiO_2, owing to its high leakage current. Hafnium oxide and hafnium silicate are among the alternative high-k dielectric materials being considered for its thermal and chemical stability. Hafnium oxide thin films were grown using plasma enhanced chemical vapor deposition (PECVD) reactors using different oxygen precursors such as N_2O, water vapor and high purity O_2. Silane was used to grow hafnium silicate thin films using the different oxygen precursors. Hafnium-t-butoxide was used as the precursor for all the thin films grown. These films were then compared with those grown without the plasma source. Profilometer and X-ray diffraction (XRD) were used to determine the deposition rate and crystallinity. The films were characterized for atomic composition using X-ray photoelectron spectroscopy (XPS) and the depth profile was performed using auger electron spectroscopy (AES) for different thermal treatments.

11:30 AM D7.9
Systematic Examination of Boron Diffusion Phenomenon in HfSiON High-k Gate Insulator. Masato Koyama[1], Tsunehiro Ino[1], Yuuichi Kamimuta[1], Masamichi Suzuki[1], Chie Hongo[2] and Akira Nishiyama[1]; [1]ASL, Toshiba Corp., Yokohama, Japan; [2]ADL, Toshiba Corp., Kawasaki, Japan.

Boron penetration is a major issue when integrating high-k gate dielectrics into conventional CMOS devices, because this phenomenon is reported to be enhanced in high-k materials such as Al2O3 and HfO2 compared to the case of SiON. HfSiON is thought to be a promising high-k material since it has high resistance to boron diffusion even at high-temperature (1000 oC) [1,2]. It is suggested that the suppression of the film crystallization by N-incorporation is responsible for the improved boron penetration [2]. However, a more comprehensive understanding, such as its dependence on the film composition is necessary. In this paper, boron diffusivity in HfSiON films was systematically examined, widely changing the film composition (Hf/(Hf+Si) = 22 80 %, [N] = 5 38 at.%). Thick HfSiON films (100 nm) were deposited onto Si substrates by co-sputtering of Hf/Si targets in an Ar/O2/N2 ambient, followed by deposition of poly-Si layers with 300 nm thickness. Boron ions were implanted into poly-Si layers at an acceleration energy of 30 keV with a dose of 5E15 atoms/cm2. Specimens were annealed at 1000 oC for 30 min, in order to drive boron atoms into the HfSiON films. Poly-Si layers were then completely removed by dry etching and boron profiles inside the HfSiON films were measured by means of SIMS (secondary ion mass spectroscopy) from the surface of the specimens. Good fit of the experimental results to the complementary error function gave us the boron diffusivities in the material. As a result, we confirmed that boron diffusivity in HfSiON decreased monotonically with increasing [N] of the film when Hf/(Hf+Si) was almost the same. It was also shown that higher [N] leads to the suppression of the film crystallization through the annealing by XRD (x-ray diffractometry). Based on these results, we think the film microcrystallization plays an important role in the microscopic diffusion process of boron. On the other hand, we also found that the diffusivity increased for one order of magnitude by increasing Hf/(Hf+Si) from 20 % to 60 %, even at the same [N] content that is high enough to keep the film in an amorphous state ([N] > 30 at.%). This experimental finding indicates that some additional factors that determine the diffusivity should be taken into account. The dominant factors of boron diffusion in HfSiON with various chemical compositions will be clarified and presented in this paper. [1] M.Koyama et al., Tech. Dig. Int. Electron Devices Meet., 2002, p849. [2] M.A.Quevedo-Lopez et al., Appl. Phys. Lett., vol.82, 2003, p4669.

11:45 AM D7.10
Ultrathin Dielectric Films Grown by Solid Phase Reaction of Pr with Thermal SiO2. Hans-Joachim Muessig, Jarek Dabrowski and Christian Wenger; IHP, Frankfurt (Oder), Germany.

A major problem in fabrication of high-k dielectric films to substitute SiO2 in future CMOS technologies is the interface engineering. The density of interfacial traps Dit is low when a SiO2 buffer layer separates the substrate from the film, but this very buffer increases the equivalent oxide thickness EOT of the gate dielectric stack. These self-contradicting demands (low Dit and low EOT) may possibly be efficiently compromised in high-k silicates grown by solid phase reaction. For this purpose, an ultrathin thermal SiO2 is grown and then enriched with metal in-diffused from a deposited metal layer, so that a high-k silicate is obtained. We report results of structural and electrical measurements for ultrathin silicates obtained by Pr in-diffusion. Depending on the growth and annealing conditions, films with various morphologies, composition, and electrical parameters are obtained. We interpret these observations in terms of formation energies obtained from ab initio calculations and from experimental thermodynamical data, focusing on the physical mechanisms responsible for the resulting EOT. We discuss feasibility of the in-diffusion method for preparation of high-quality gate dielectrics with EOT below 1 nm and conclude that a careful tailoring of growth and annealing procedure is needed to avoid hazardous inhomogeneities in composition of the film which are detrimental to its electrical performance.

SESSION D8: Ferroelectrics I
Chairs: Athanasios Dimoulas and Tsu Jae King
Thursday Afternoon, April 15, 2004
Room 2006 (Moscone West)

2:00 PM *D8.1
Ferroelectric Thin Films for High Frequency Applications. Stephen R. Gilbert, Agilent Technologies, Agilent Laboratories, Palo Alto, California.

Ferroelectric thin films have attracted considerable attention for use in a wide range of wireless communications products. For advanced digital baseband circuits, high-density, embedded ferroelectric memory (FeRAM) based upon $Pb(Zr,Ti)O_3$ (PZT) has the potential to be a low-power, high-performance substitute for embedded DRAM, SRAM, and Flash technologies. In the RF front end of wireless devices, the large and voltage-variable permittivity of $(Ba,Sr)TiO_3$ (BST) is being exploited for thin film varactor and high-density capacitor applications, and shows considerable promise for use within compact, frequency agile front end modules. Moreover, the

piezoelectric properties of PZT may be exploited for a variety of filter and sensor components. In this presentation, we will review recent advances in the deposition of ferroelectric thin films, and the primary integration issues that must be considered when fabricating parallel plate capacitors for RF applications. The most technologically significant thin film deposition technologies include metalorganic chemical vapor deposition (MOCVD), physical vapor deposition (PVD), and chemical solution deposition (CSD), and the relative merits of each will be reviewed. Next, requirements for diffusion barriers, adhesion layers, and capacitor electrodes are presented, and high frequency metallization schemes described. The primary sources of integration-induced damage will also be addressed, and strategies to mitigate their effects reviewed. Finally, the requisite electrical properties of these capacitors at high frequency will be described in detail.

2:30 PM D8.2
Sharp Ferroelectric Phase Transition in Strained Single-Crystalline SrRuO3/Ba0.7Sr0.3TiO3/SrRuO3 Capacitors. Regina Dittmann[1], R. Plonka[2], E. Vasco[1], N. A. Pertsev[1], J. Q. He[1], C. L. Jia[1], S. Hoffmann-Eifert[1] and R. Waser[1]; [1]Institut fuer Festkoerperforschung, Forschungszentrum Juelich, Juelich, Germany; [2]IWE 2, RWTH Aachen, Aachen, Germany.

Single-crystalline all-perovskite SrRuO3/Ba0.7Sr0.3TiO3/SrRuO3 (BST/SRO/BST) thin-film capacitors epitaxially grown on SrTiO3 by pulsed laser deposition exhibit a sharp paraelectric-to-ferroelectric phase transition at 350 K with a maximum permittivity of about 6660 [1]. This value is comparable to that of bulk ceramics and exceeds by several times the highest values reported for BST thin film capacitors. A detailed study of dielectric properties, which have been correlated to the BST microstructure, of our thin film heterostructures is performed. X-ray, RBS and HRTEM measurements indicate the presence of a critical thickness of 10 nm for the formation of misfit dislocations and thickness-dependent lattice strains in our epitaxial BST films. The influence of the strains on the observed temperature and thickness dependence of the dielectric response is analyzed with the aid of a thermodynamic theory. Hence, the increase of the transition temperature by about 40 K relative to the bulk value can be attributed to the in-plane compressive misfit strains. It is shown that the weak decrease of the permittivity with the BST thickness decreasing from 200 to 10 nm can be explained solely by the thickness-dependent strain relaxation in epitaxial films without assuming the presence of low-permittivity layers at the film/electrode interfaces. We compare these results to SRO/BST/Pt thin-film capacitors which have the same crystalline quality but show a paraelectric-to-ferroelectric phase transition which is strongly influenced by the top Pt- BST interface. [1] R. Dittmann, R. Plonka, E. Vasco, N. A. Pertsev, J. Q. He, C.L. Jia, S. Hoffmann-Eifert and R. Waser, to appear in Appl. Phys. Lett., 6. Dez. 2003

2:45 PM D8.3
The Influence of Crystallization Route on the Properties of Lanthanum Doped Bi4Ti3O12 Thin Films Prepared From Polymeric Precursors. Alexandre Zirpoli Simoes[1], Noberto Luiz Amsei Junior[1], Cristiane Quinelato[1], Carla dos Santos Riccardi[1], Mario Cilense[1], Andreas Ries[1], Maria Aparecida Zaghete[1], Jose Arana Varela[1] and Elson Longo[2]; [1]Physics-Chemistry, Chemistry-Institute-Unesp, Araraquara, So Paulo, Brazil; [2]Physics-Chemistry, Chemistry-Institute-Ufscar, Sao Carlos, So Paulo, Brazil.

Polycrystalline lanthanum doped Bi4Ti3O12 thin films were synthesized on Pt/Ti/SiO2/Si substrate using the polymeric precursors solution. The spin-coated films were specular and crack-free and crystallized after annealed at 700 degree Celsius for 2 hours. Crystallinity and morphological evaluation were followed by X ray diffraction (DRX), scanning electron microscopy (SEM), and atomic force microscopy (AFM). Multilayered films obtained using the intermediate-crystallized layer route present a dense microstructure with spherical grains. Films obtained using the intermediate-amorphous layer present elongated grains around 200 nm in size. The dielectric and ferroelectric properties of the lanthanum doped Bi4Ti3O12 films are strongly affected by the crystallization route.

3:30 PM D8.4
Identification of hydrogen induced atomic deformation in $SrBi_2Nb_2O_9$ thin film. Ik Soo Kim[1], Yong Tae Kim[1], Jeong Yong Lee[2] and Dong Chul Yoo[2]; [1]Semiconductor Materials and Devices Lab., Korea Institute of Science & Technology, Seoul, South Korea; [2]Department of Materials Science, Korea Advanced Institute of Science & Technology, Daejeon, South Korea.

Even if it has been well known that hydrogen annealing degrade ferroelectric properties, there is no conclusive report to confirm that hydrogen influences on atomic arrangement in $SrBi_2Nb_2O_9$ (SBN) thin films. In this work, for the first time, we have investigated how hydrogen annealing at Curie temperature causes atomic deformation with high resolution TEM. In order to investigate exactly the same area before and after the hydrogen annealing, and oxygen recovery annealing, we have locally ion-milled backside of Si substrate and left about 5 nm thick SBN film on the spot area. Before the hydrogen annealing of this specimen, we observed the spot area with HR-TEM. The same specimen was annealed at 435°C in 3% of hydrogen containing ambient for 15min and the spot area was investigated by HR-TEM. Finally, the HR-TEM specimen was recovery-annealed at 600°C in oxygen ambient for 15min and investigated with HR-TEM. After the hydrogen and oxygen recovery annealing processes, we observed atomic arrangement of the same spot area. As a result, before the hydrogen annealing, the SBN was oriented along (0 0 1) planes. Then, after the hydrogen annealing we found that the atomic arrangement of a (1 1 5) plane was shifted upward and the second (1 1 5) plane was shifted downward along (1 1 5) plane and the third (1 1 5) plane was not changed. Consequently, inter-plane distance of normal {1 1 5} planes is 3.081$\AA$, but that of the shifted {1 1 5} planes is reduced to 3.056 $\AA$. Due to the shift in the atomic arrangement of {1 1 5} planes, perovskite structure will be transformed, resulting in degradation of ferroelectric property after the hydrogen annealing. However, we found that the atomic shift becomes to be recovered without any deformation after recovery annealing at 600°C in oxygen ambient. It would be due to that the tilted angle is relatively small as 10° after hydrogen annealing.

3:45 PM D8.5
Low Temperature Sputter Deposition of Ba0.96Ca0.04Ti0.88Zr0.12O3 (BCTZ)thin films on Ni Electrodes. Thottam S. Kalkur, Nick Cramer, Elliott Philofsky and Lee Kammerdiner; Electrical and Computer Engineering, University of Colorado at Coloardo Springs, Colorado Springs, Colorado.

The investigation of high-K materials such as ferroelectrics in the paraelectric phase in integrated circuits presents several challenges. If high-K materials are deposited on-chip after or between Al metallization steps, then those chalenges include limits on processing gas composition, deposition temperature and electrode material. Specifically, the atmosphere present during deposition and annealing must be oxygen free, the deposition and and annealing temperatures must not exceed 450 C and the electrode material must be etchable with chemical techniques. We studied rf magnetron sputtered BCTZ with Ni electrodes because this system meets all the above requirements. The BCTZ deposition process uses pure Ar as the sputter gas and a substrate temperature of 450 C. Subsequent anneals may be performed in a reducing (forming gas) atmosphere with a little effect on either dielectric constant or leakage current. The Ni electrodes provide a good substrate for BCTZ films and much easier to integrate than Pt films. Observed values for the relative dielectric constant K exceeding 100 were not as high as for BCTZ films on Pt electrodes however these values are sufficient to provide clear advantage over other non-ferroelectric materials. Overall, the device characteristics observed prove that the Ni/BCTZ/Ni capacitor is a valuable technology for on-chip capacitor applications.

4:00 PM D8.6
Epitaxial growth of Ba1-xSrxTiO3 thin films by polymer-assisted deposition. Yuan Lin[1], Haiyan Wang[1], Jang-Sik Lee[1], Yuan Li[1], S. R. Foltyn[1], Quanxi Jia[1], G. Collis[2], A. K. Burrell[2] and T. M. McCleskey[2]; [1]Material Science & Technology Division, Los Alamos National Lab, Los Alamos, New Mexico; [2]Structural and Inorganic Chemistry, Division of Chemistry, Los Alamos National Laboratory, Los Alamos, New Mexico.

Ba1-xSrxTiO3 (BST) thin films with different Ba/Sr ratio (x=0, 0.3, 0.5, 0.7, 1) were epitaxially grown on (001) LaAlO3 (LAO) substrates using polymer-assisted deposition (PAD) we developed recently. Microstructural studies by x-ray diffraction and transmission electron microscopy show that the films are epitaxial with an orientation relationship of (001)BST//(001)LAO and [100]BST//[100]LAO. Systematic changes in dielectric behavior with x values were measured and the dielectric properties of the films were proved to be as good as those epitaxially grown by pulsed laser deposition. This work shows that PAD is an alternative approach for growth of high quality epitaxial metal-oxide films.

4:15 PM D8.7
Heteroepitaxial Pb(Zr,Ti)O3 thin film growth by hydrothermal treatment. Kyoon Choi[1], June Choi[1], Ho-Yong Lee[2] and Eui-Seok Choi[1]; [1]Thin Film & Single Crystal Lab, Korea Inst of Ceramic Eng & Tech, Seoul, South Korea; [2]Ceracomp Co., Ltd., Asan, South Korea.

The dense and thick lead zirconate titanate (PZT) films were synthesized via hydrothermal treatment on BaTiO3 (BT) and Ba(Zr0.1Ti0.9)O3 (BZT) perovskite crystals that are grown by the

solid-state single crystal growth (SSCG). The PZT films were grown in a strong alkaline solution (pH>13.9) with variation of the solute concentration and time where Zr to Ti ratio was 56/44 and no excess lead was added. The film obtained showed an epitaxial relationship with the substrate crystal while the film characteristics depended on the hydrothermal condition. The BZT crystal is determined to be more effective substrate for the PZT film because of their low lattice mismatch.

4:30 PM D8.8
Microstructure and Ferroelectric Characteristics of Ultra-Thin BaTiO3 Films. Yariv Drezner and Shlomo Berger; Materials Engineering, Technion-Israel Institute of Technology, Haifa, Israel.

Microstructure studies of ultra-thin BaTiO3 films (2-10nm thick) show nano-domains having a width as small as one unit cell. High resolution TEM investigation revealed only 180o nano-domains and 90o domain-boundaries formed in multi-domains structures. The domains are mostly oriented in parallel to the film plane, but few domains were observed out of the plane orientation. The ferroelectric behavior was characterized as a function of thickness in vertical to the films plane. A polarization hysteresis loop was recorded even in the 2nm thick films having a remanent polarization of about 3nC/cm2 and a coercive field of 0.7MV/cm. Fatigue tests show an initial degradation of the remanent polarization at about 107 cycles under a continuous 5Vac load at a frequency of 1kHz. The values of remanent polarization and fatigue edge are improved with increasing the film thickness. The switching response of the nano-domains is relatively fast in the range of few nano seconds. The switching time decreases with increasing the applied electric field according to power law dependence with a coefficient of minus 2.5. The dependence of the leakage current on the applied electric field is characteristic to a hopping conductivity mechanism. The measured values of the leakage current density and activation energy are comparable to bulk size ferroelectric films. Two temperature-dependent peaks of dielectric constant were observed; a broad peak that spans between 60-80oC and a narrow peak between 105-110oC. These peaks are attributed to two Curie temperatures associated with the orientation of the nano-domains relative to the in-plane stress direction. The two peaks are slightly shifted towards the bulk Curie temperature as the film thickness increases. A correlation between microstructure, film thickness, film stress and ferroelectric properties is demonstrated and discussed.

4:45 PM D8.9
Thickness dependence of leakage conduction in MOCVD deposited Pb(Zr,Ti)O_3 and $PbTiO_3$ thin films. David V. Taylor, Maxim B. Kelman, Lawrence F. Schloss and Paul C. McIntyre; Materials Science and Engineering, Stanford University, Stanford, California.

The next generation of low-power, high density nonvolatile embedded memory technology required for wireless devices will necessitate cost-effective integration with CMOS logic and other components. Among the contenders, Ferroelectric Random Access Memory (FeRAM / FRAM) appears to be the most advanced. Although FeRAM is considered nonvolatile since the two polarization states are stable upon removal of the field, several long-term reliability issues such as fatigue, imprint and retention loss are of concern. Since these FeRAM device limiting phenomena are believed to be closely related to trapping of electronic charges, detailed leakage conduction studies should shed light on degradation mechanisms which can ultimately lead to memory failure. In addition, major film thickness scaling (<100 nm) will be required to meet the operating voltages specified by the International Technology Roadmap for Semiconductors (ITRS). We will present a comprehensive investigation of leakage current characteristics of state-of-the-art MOCVD deposited polycrystalline Pb(Zr,Ti)O_3 (PZT) thin film capacitors as a function of film thickness (<100 nm) and compare them with those of epitaxial $PbTiO_3$ films deposited on lanthanum-doped (001)-oriented $SrTiO_3$. Temperature-dependent measurements are used to assess the conduction mechanisms responsible for the observed leakage behavior.

SESSION D9: MBE, PLD, and MOCVD of High-k
Chairs: Luigi Colombo and Dolf Landheer
Friday Morning, April 16, 2004
Room 2006 (Moscone West)

8:30 AM *D9.1
Epitaxial gate dielectrics: Complex oxides technology to meet silicon's future. Jean Fompeyrine[1], Gerd Norga[1], Chiara Marchiori[1,2], Alexandre Guiller[1], David Halley[1], Jin Won Seo[3], Heinz Siegwart[1], Daniele Caimi[1], Dave J. Webb[1], Christophe Rossel[1], Roland Germann[1] and Jean-Pierre Locquet[1]; [1]Zurich Laboratory, IBM Research, Rueschlikon, Switzerland; [2]Laboratorio MDM, INFM, Agrate-Brianza, Italy; [3]IPMC, EPFL, Lausanne, Switzerland.

Complex oxides grown epitaxially on silicon may provide a path towards gate dielectrics with very low equivalent oxide thicknesses (EOT<0.5nm). Nevertheless, they could allow device engineers to not compromise on power consumption and keep gate leakage at low levels. This unique combination derives from their intrinsically higher k. A substantially greater physical thickness (100?) can be afforded with respect to amorphous high-k. Clearly, this first objective can only be reached if the formation of an amorphous low-k interfacial phase is kept under tight control. Any interfacial monolayers will increase EOT by more than 20% for such low EOT ranges. In light of this objective, the latest development in this field have been done following five complementary approaches: (1) materials selection guided by bulk thermodynamics; (2) interface thermodynamics; (3) structural matching of the silicon and epitaxial oxide lattices; (4) oxidation kinetic control during all process stages and (5) development of process-specific tools. The aim of this talk is to prove that deposition processes can be developed with an appropriate combination of these five cornerstones. It allowed us and a few other research groups to control the transition from silicon to an oxide layer, using perovskites Sr(Ti,Zr)O3 or pyrochlores La(Zr,Hf)O3.5 Together with the development of a specific MBE deposition tool, we will then show that our initial objective has been reached.

9:00 AM D9.2
Alkaline Earth Hafnate Oxide Films on Si(001) Substrates. Zhiyi Yu[1], Xiaoming Hu[1], Jay A. Curless[1], Yong Liang[1], Brad Craigo[1], Karen Moore[1] and Rich Gregory[2]; [1]Microelectronics and Physical Sciences Laboratory, Motorola Labs, Tempe, Arizona; [2]Process and Materials Chacterization Laboratory, Motorola SPS, Tempe, Arizona.

Hf-based metal oxides are attractive for high-k gate dielectric applications in the sub-90nm CMOS technology. We report the deposition and properties of alkaline earth hafnate films on Si(001) substrates. Epitaxial strontium hafnate and barium hafnate oxide films were grown by molecular beam epitaxy (MBE) using an ultra-thin SrTiO3 buffer layer on Si. Reflection high energy electron diffraction (RHEED) oscillation technique and the certain signature oxide surface reconstructions were used for flux calibration and real-time stoichiometry monitoring of the growing oxide film, respectively. Meanwhile, amorphous alkaline earth hafnate films were deposited on Si(100) surface in an MBE chamber. Various in-situ and ex-situ techniques were utilized to characterize these hafnate films. For example, in addition to atomic force microscopy (AFM), x-ray diffraction (XRD) and Rutherford backscattering spectroscopy (RBS), ultra-violet spectroscopic ellipsometry (UV-SE) and x-ray photoelectron spectroscopy (XPS) techniques were used to determine the optical band gap energy and the band offset of the hafnate film on Si, respectively. Contrary to SrTiO3 on Si with a negligible conduction band offset, the alkaline earth hafnate films posses sufficient band gap as well as fairly balanced conduction band offset and valence band offset against Si. These characterization results indicate that the hafnates could become a new class of high-k gate dielectric materials for future generation CMOS technology.

9:15 AM D9.3
Deposition of Amorphous $LaScO_3$ on Silicon by MBD for Alternative Gate Dielectric Applications. Lisa F. Edge[1], Darrell G. Schlom[1], Scott A. Chambers[2], Matt Copel[3], Bernhard Hollander[4] and Jurgen Schubert[4]; [1]Materials Science and Engineering, Pennsylvania State University, University Park, Pennsylvania; [2]Fundamental Science Division, Pacific Northwest National Laboratory, Richland, Washington; [3]IBM T. J. Watson Research Center, Yorktown Heights, New York; [4]Institut fur Schichten und Grenzflachen ISG1-IT, Forschungszentrum Julich GmbH, Julich, Germany.

$LaScO_3$ is being studied as an alternative gate dielectric material for the replacement of SiO_2 in silicon MOSFETs. A major challenge in the growth of alternative gate dielectrics on Si is the formation of excessive SiO_2 at the interface between Si and the high-K gate dielectric. Although this potentially improves device performance and reliability, it impacts adversely on the smallest attainable values of the equivalent oxide thickness, EOT. One technique to prevent the formation of SiO_2 is to grow in a low temperature / kinetically-limited oxidation regime. We have investigated the oxidation kinetics of La and Sc from their elemental state to fully oxidized La_2O_3 and Sc_2O_3 in the presence of oxygen using an in situ quartz crystal microbalance (QCM). This enabled a quantitative determination of the minimum oxygen partial pressure required to achieve fully oxidized $LaScO_3$, and therefore minimize the amount of interfacial SiO_2. Using a codeposition process, amorphous $LaScO_3$ films as thin as 10 Å were grown on (100) Si by molecular beam deposition (MBD) using the minimum oxygen partial pressure conditions identified. XPS analyses indicate that the films are fully oxidized, and in addition, as expected

from the growth kinetics, show no detectable SiO_2 or Si-O bonding at the interface with Si. The films also do not show evidence for interfacial oxidation even after prolonged exposure to air making $LaScO_3$ a promising material for the replacement of SiO_2.

9:30 AM D9.4
Lanthanum Hafnate High-κ Gate Dielectrics by MBE.
George Vellianitis[1], Athanasios Dimoulas[1], Georgia Mavrou[1], Anastasios Travlos[1], Jacob C. Hooker[2], Zacharias M. Rittersma[2], Marco Fanciulli[3], Claudia Wiemer[3] and Sandro Ferrari[3]; [1]Institute of Materials Science, NCSR "DEMOKRITOS", Athens, Greece; [2]Philips Research Leuven, Leuven, Belgium; [3]Laboratorio MDM, INFM, Agrate (Milano), Italy.

Ultimate scaling of devices with EOT as low as 0.5 nm requires high-κ gate dielectrics with atomically sharp interfaces with silicon, which could be obtained by molecular beam epitaxy (MBE) methodologies. The stoichiometric $La_2Hf_2O_7$ (LHO) compound being lattice matched to silicon is a model material for epitaxial growth. This is a new material which has not been investigated before in the context of high-κ dielectrics. We show that the delicate balance between the growth temperature T_g and the O_2 partial pressure control the structural and electrical quality of thin LHO films. At temperatures lower than 650 ^{0}C, the material is amorphous. In as-grown films, the measured EOT decreases from 1.2 nm to 0.7 nm as T_g varies between 60 and 600 ^{0}C, compatible with κ values around 20. However, the gate current J_g increases from $6x10^{-5}$ to about $2x10^{-1}$ A/cm^2 @ 1V accumulation in the same temperature range. This behavior could be attributed to the fact that a low-κ, O-rich interfacial layer is formed at low T_g, which becomes unstable at higher temperature given that the growth takes place at a reducing atmosphere with a low partial pressure of O_2 around $2\text{-}4x10^{-6}$ Torr. At higher temperatures in the range of 720-770 ^{0}C the oxide is crystalline with a preferential orientation along the (001) direction of growth. The oxide exhibits a complex microstructure, where the random fluorite and the ordered pyrochlore phases coexist. As observed by TEM, the lattice planes continue from the substrate into the oxide epilayer indicating commensurate growth and perfectly clean interfaces with no interfacial layer as required for aggressive device scaling. However, the exposure of the surface to O_2 prior to growth creates Si {111} facets which affect the oxide epilayer inducing excess roughness. This prevents the electrical characterization of the crystalline LHO oxides, given that the fabrication and testing of reliable MIS capacitors is not possible unless smooth morphology films are obtained.

9:45 AM D9.5
Epitaxial Growth and Structure of Thin Single Crystal γ-Al_2O_3 Films on Si (111) Using e-Beam Evaporation of Sapphire in Ultra-High Vacuum. Minghwei Hong[1,3], A. Refik Kortan[1], J. Raynien Kwo[2,3], Joseph Mannaerts[1], S. Y. Wu[1] and C. P. Chen[1]; [1]Materials Science and Engineering, National Tsing Hua University, Hsin Chu, Taiwan; [2]Physics, National Tsing Hua University, Hsin Chu, Taiwan; [3]Industrial Technology Research Institute, Hsin Chu, Taiwan.

Hetero-epitaxial growth of insulators on semiconductors and vice versa is of great interest in many branches of science and technology. Typical examples are the growth of GaN on sapphire, which provides a basis for blue, green lasers and LEDs, and the epitaxial growth of insulators on Si. A subsequent single-crystalline growth of other semiconductors on these insulating layers may provide a basis for achieving single crystal growth of GaN or GaAs indirectly on Si. Additional application is found in the efforts of high k dielectrics on Si, an important and urgent technological issue. Here, we report an epitaxial growth of single crystal γ Al_2O_3 films on Si (111). The structural studies of these Al_2O_3 films and their epitaxy to Si (111) were carried out using in-situ RHEED and single-crystal x-ray diffraction. A high-purity source of sapphire single crystals was employed in this work to avoid the contamination of carbon and nitrogen. E-beam evaporation was used due to the high melting point of sapphire, and the evaporation took place in ultra-high vacuum. Si wafers 2-inch in diameter with (111) as the normal to the wafer plane were put into a multi-chamber MBE/UHV system, after being cleaned with an RCA method and an HF dip. Heating the Si wafers to temperatures above 300C has resulted in a sharp and streaky RHEED pattern with Kikuchi arcs, indicative of the attainment of a clean Si surface. Additional growth of Si films 5 nm thick in one of the MBE chamber ensures a chemically clean and atomically sharp Si (111) surface. The wafers were then transferred under UHV (hence any possibility of Si oxidation was eliminated) to an oxide chamber for the Al_2O_3 deposition. Streaky RHEED patterns along the in-plane axes of [110] and [112] of Si were observed after growth of 1-2 nm thick oxide, indicative of in-plane alignment between the oxide film and the Si substrate. Additional and more accurate structural measurements were carried out using single-crystal x-ray diffraction on a triple-axes four-circle diffractometer using a 12 kW Cu-K_α rotating anode source. For x-ray diffraction study a film 11 nm thick was made. The oxide film is very uniform as studied from reflectivity measurements (small angle x-ray diffraction). The atomic structure of the Al_2O_3 film is determined to be the gamma-phase. The <111> axes of the film and the Si substrate are well aligned. Mosaic scan of the Al_2O_3 (222) peak (with no in-plane component) finds a 0.3 degree mosaic spread. All three unit cell vectors of the film and the substrate are parallel, but the in-plane cone scans of the {004} and {044} diffraction peaks about the surface normal find a ± 3 degree film in-plane rotation with respect to the substrate surface orientation. More detailed characteristics of the oxide films and their interface to Si will be presented.

10:30 AM D9.6
Rare-Earth Scandate Thin Films as Alternative Gate Oxides for Microelectronic Applications. Juergen Schubert[1], Y. Jia[2], T. Heeg[1], O. Trithaveesak[1], L. Edge[2] and D.G. Schlom[2]; [1]ISG 1-IT, Forschungszentrum Juelich GmbH, Juelich, Germany; [2]MRI, Penn State University, University Park, Pennsylvania.

The rare-earth scandates ($ReScO_3$, where Re is a rare earth element) were recently proposed as candidate materials for the replacement of SiO_2 in silicon MOSFETs in either amorphous or epitaxial form. Measurements on single crystals of three different rare-earth scandates: $DyScO_3$, $GdScO_3$, and $SmScO_3$ indicated that rare-earth scandates are promising for this application. All showed relatively high dielectric constants (K), high optical band gap energies, and stability in direct contact with silicon. In this work we investigate the dielectric properties and structural perfection of epitaxial $ReScO_3$ thin films, including compositions identical to those whose properties have been studied as single crystals (i.e., $DyScO_3$ and $GdScO_3$) as well as a new composition whose high melting temperature prevented its growth so far and studied as a single crystal (i.e., $LaScO_3$ with T_m 2290°C). Epitaxial $LaScO_3$, $GdScO_3$, and $DyScO_3$ films with good crystalline perfection were grown by pulsed laser deposition (PLD) to form metal-insulator-metal structures. High K -values up to 26- were measured for these epitaxial scandate films. Amorphous films of these $ReScO_3$-materials were prepared by PLD directly on silicon substrates. The growth was performed at different temperatures to investigate the thermal stability of the scandates in contact with silicon. Rutherford Backscattering Spectrometry was used to investigate diffusion processes between silicon and the scandate thin films.

10:45 AM D9.7
MOCVD of SrTa2O6 Thin Films for High-k Applications.
Stephan Regnery[1,2], Peter Ehrhart[1], Reji Thomas[1], Rainer Waser[1], Peer Lehnen[2], Stefan Miedl[2] and Marcus Schumacher[2]; [1]Forschungszentrum Juelich, Juelich, Germany; [2]Aixtron AG, Aachen, Germany.

Thin films with thickness between 50 and 150nm were deposited in a multi-wafer planetary MOCVD reactor combined with a TRIJET liquid delivery system. The precursor was a mixed strontium-tantalum-(methoxyethoxy)-ethoxide single source precursor dissolved in toluene. A rather narrow process window for the deposition of stoichiometric SrTa2O6 was found for this single source precursor at low pressures and a suszeptor temperature around 500C. Films were grown on Pt/TiO2/SiO2/Si on TiN/Si and on SiO2/Si substrates. The as deposited films were X-ray amorphous and very smooth, with roughness values similar to the underlying substrates. The amorphous films could be crystallized by post-annealing at a minimum temperature of 650C. The SrTa2O6 phase was dominating within a rather broad range of compositions (Sr/Ta: 0.3 to 0.8) and a perovskite type phase was observed for Sr/Ta > 0.8. The electrical properties have been investigated after sputter deposition of Pt top electrodes. The amorphous films had a permittivity, e, in the range of e = 25 to 40, which was independent of thickness and of elemental composition within a wide range (Sr/Ta: 0.20 to 1.3). Leakage currents were rather low, typically 10-10A/scm at 1V and loss tangents were in the range of 0.002. The crystalline films were investigated only on platinum electrodes as the TiN electrodes were destroyed during annealing. For stoichiometric SrTa2O6 the dielectric permittivity reached values of e = 100 to 110, but the leakage currents are increased, typically 10-6A/scm at 1V. Remarkably, the permittivity is not very sensitive to deviations from the exact stoichiometry of the SrTa2O6 phase and a drastic decrease to values of e = 30 to 40 is only observed along with the phase transition at high Sr contents.

11:00 AM D9.8
New Atomic Vapour Deposition (AVD (R)) Process for High Performance HfO2 Dielectric Layers. Vincent Cosnier, [1]STMicroelectronics, Crolles, France; [2]Aixtron, Aachen, Germany.

The introduction of "high k" dielectrics in the gate of CMOS is facing two basic challenges: the lowest EOT (equivalent oxide thickness) associated with a controlled leakage current. It is well known now that the Hf-family oxide compounds appears as the best candidate for the

gate dielectric materials, and can be elaborated in a wide bench of techniques; among them ALD and MOCVD are the most advanced. In this contribution, an innovative technique of deposition, named Atomic Vapour Deposition (a sort of pulsed MOCVD) is used for the deposition of HfO2. The precursor, diluted into a solvent, is pulsed through specific injectors (TriJet (R)), get vaporised and is distributed to the substrate through a showerhead. This pulsed technique associated with the wafer rotation leads to a uniformity of 0.75 percent at 1 sigma over a 200 mm wafer, is easily expandable to 300 mm, and is very versatile given the broad variety of precursors which can be injected and precisely controlled. Two precursors have been studied. Depositions have been performed at different pulse injection frequencies, different temperatures (400 to 600 C), and different gas flows or pressures. ATR-FTIR and Hg probe measurements have been extensively used to evaluate the materials. Moreover, an in-line ellipsometer allowed a direct evaluation of the quality of this material. The characterisation of the material in terms of crystallinity, density and roughness has been performed using mostly XRD, XRR and AFM measurement techniques. Damascene capacitors with TiN gate have shown the potential of this deposition technology. Indeed, one of the best-known performances has been obtained for MOCVD pure HfO2: and EOT of 1.15 nm with a leakage current of 6.10-2 A/cm2 at —Vfb— 1 V, that is to say about 3 orders of magnitude below what is obtained with optimised SiO2. Moreover, the uniformity of leakage, Cox and Vfb position over the wafer is excellent. And finally, a very good achievement obtained with this material and this technique of deposition is that C-V sweeps (from -2 to 2 V) show very lmited hysteresis, around 5 mV. This work has been made in the frame of the MEDEA T207 european project with the help of Air Liquide and Epichem.

11:15 AM D9.9
Growth of Pr2O3 layers by pulsed liquid injection MOCVD.
A Abrutis[1], A Bartasyte[1], A Teiserskis[1], Z Saltyte[1], P K Baumann[2], M Schumacher[2], J Lindner[2] and T McEntee[2]; [1]Dep. of General and Inorganic Chemistry, Vilnius University, Vilnius, Lithuania; [2]Semiconductor Equipment, AIXTRON AG, Aachen, Germany.

Praseodymiumoxide (Pr2O3) is a potential high-K dielectric for use in DRAM or CMOS devices. Here we present results on metal organic chemical vapor deposition (MOCVD) and characterization of amorphous and crystalline Pr2O3. The layers were grown on Si(100) by pulsed liquid injection MOCVD in the temperature range 400-750C. Pr(thd)3 (thd = 2,2,6,6-tetramethyl-3,5-heptanedionate) dissolved in monoglyme (1,2-dimethoxyethane) or toluene was used as precursor solution. The influence of deposition conditions on film composition, growth rate, crystallization and surface roughness has been investigated. The main parameters influencing film composition and properties were substrate temperature and partial oxygen pressure during deposition. The presence of molecular oxygen in the reactor leads to the growth of Pr6O11 as the most stable phase or its mixture with PrO2. Only deposition in inert atmosphere (Ar) allows to obtain Pr2O3 films which were amorphous or crystalline depending on the deposition temperature. Crystallized (polycrystalline) Pr2O3 films can be obtained at the growth temperatures 650C and higher, while crystalline Pr6O11 films grow in the whole range of studied temperatures (400-750C). No interaction between praseodymium oxide and silicon substrate at high deposition temperature has been observed by XRD. Ex-situ annealing (750C, vacuum) of the amorphous Pr2O3 films leads to film crystallization. Annealing of crystalline as-deposited films improves the crystallinity of the films. Step coverage studies have been performed for amorphous and crystallized Pr2O3 films. Electrical properties of thin (10 nm) Pr2O3 films were investigated. Encouraging k-value, leakage current and breakdown field data have been obtained for the thin films deposited at various temperatures. Further deposition and characterization studies to optimize the film properties are underway and will be reported.

11:30 AM D9.10
Properties of Pr-based high k dielectric films obtained by Metal-Organic Chemical Vapor Deposition.
Graziella Malandrino[1], Raffaella Lo Nigro[2], Roberta Toro[1], Vito Raineri[2] and Ignazio Luciano Fragala'[1]; [1]Dipartimento Scienze Chimiche, Universita, Catania, Italy; [2]IMM sezione di Catania, IMM-CNR, Catania, Italy.

The need for a higher dielectric constant replacement for silicon dioxide in order to sustain Si complementary-metal-oxide-semiconductor scaling is well documented. It is therefore desirable to employ a dielectric which exhibits an enhanced permittivity over that of SiO2, remains amorphous during processing, and avoids the need for a reaction barrier at the interface. We report on the microstructural characteristics of Pr-based oxide films grown on silicon substrate by Metal-Organic Chemical Vapor Deposition (MOCVD). Praseodymium based films were deposited from the Pr(tmhd)3 (H-tmhd=2,2,6,6-tetramethyl-3,5-heptanedione(precursor using as carrier gas a 100 sccm Ar flow under 10-3 torr oxygen partial pressure. Films have been characterised by X-ray diffraction (XRD), transmission electron microscopy (TEM), photoelectron spectroscopy (XPS) and capacitance versus voltage as well as current densities versus voltage measurements. The interfacial composition and its effect on the dielectric properties have been fully examined. In particular, the interface structure has been investigated by High-Resolution TEM image and it consists of an SiO2 layer and a bottom praseodymium oxide based layer, about 8 nm thick, having no long range order. The 8 nm bottom layer have shown a selected area diffraction pattern typical of an amorphous layer and its chemical composition has been investigated by Energy Filtered transmission electron microscopy (EF-TEM) analysis using the three windows method. This represents an innovative technique to study chemical composition and film/substrate interface in a non-destructive way. The EF-TEM analyses point to the formation of three layers whose chemical composition has been assessed to be: a SiO2 layer at the Si interface, an oxygen-rich 8 nm layer, and the praseodymium oxide layer. Moreover, in order to establish the chemical composition of the amorphous layer, films grown for 10 minutes consist of a 8 nm layer have been analyzed by angle resolved X-ray photoelectron spectroscopy. The recorded spectra at various incidence angles (20, 45 and 80 degrees) point to the formation of a silicate interfacial layer. The formation of multiple layer stacks consisting of REO/RESiO/SiO2, where RE is an element of rare earths, has been already observed for other RE elements such as Y and La, in both physical vapour deposition (PVD) and chemical vapour deposition (CVD) processes. Polycrystalline Pr2O3 and amorphous Pr-silicate films have shown interesting dielectric characteristics. In particular, the potentiality of the praseodymium silicate amorphous layer as alternative gate dielectrics for Si complementary metal oxide semiconductor technology has been investigated. Considering all of the desired properties these materials possess, praseodymium silicate could be an excellent materials candidate for advanced gate dielectrics.

SESSION D10: Ferroelectrics II - Physical, Chemical, and Electrical Characterization
Chairs: Orlando Auciello and Steve Gilbert
Friday Afternoon, April 16, 2004
Room 2006 (Moscone West)

2:00 PM D10.1
Processing and On-Wafer Measurements of Ferroelectric Interdigitated Tunable Microwave Capacitors.
Alexander M Grishin, Jang-Yong Kim and Sergey I Khartsev; Condensed Matter Physics, Royal Institute of Technology, Stockholm-Kista, Sweden.

Na0.5K0.5NbO3 (NKN) and Pb(Zr0.53Ti0.47)O3 (PZT) films have been grown by rf-magnetron sputtering and pulsed laser deposition techniques, correspondingly, on sapphire (Al2O3-01-12, r-cut), YAlO3 + 1% Nd (Nd:YAlO3-001), and quartz (Y+36o-cut) single crystal substrates. Interdigital capacitor (IDC) of coplanar waveguide (CPW) structures were defined by a standard lift off technique in a Au(0.5μm)/Cr(10nm) electrode electron beam evaporated on ferroelectric film surface. IDCs consisted of five pairs of fingers separated by 2 μm gap. Microwave network analyzer (Agilent Technology E8364A) with G-S-G Picoprobe and Cascade Microtech probe station were used to perform on-wafer microwave measurements with an external DC bias. Assumed equivalent circuit for the IDC/CPW structure contains planar capacitor under test C, the coplanar line with a complex impedance ς and a parasitic capacitance Cp between the signal and ground lines. The de-embedding technique has been employed to determine all six complex parameters C, ς and Cp from S-parameter measurements performed for three different device structures: device, open and thru. Comparison of various IDC/CPW properties is presented in the frequency range 1 to 40 GHz. NKN film interdigital capacitors on sapphire show superior performance in this microwave range: the frequency dispersion was as low as 18%, voltage tunability = 1 - C(40V)/C(0) (40V, 200 kV/cm) about 14%, loss tangent 0.11, K-factor = tunability/tanδ from 131% @ 10GHz to 56% @ 40GHz. The reliability of the de-embedding procedure is clearly proved by analysis of the frequency dependences of the parasitic capacitance and tangent loss as well as impedance of the coplanar line. Within the accuracy of experimental data and de-embedding calculations these values appear to be voltage independent: Cp 70 fF, parasitic tan δ changes from 0.07@10GHz to 0.15@40GHz; real and imaginary part of interconnect impedance increases with frequency from 0.16 Ω@10 GHz to 0.36 Ω@40 GHz and from 1.6 Ω@10 GHz to 5.84 Ω@40 GHz respectively.

2:15 PM D10.2
Enhanced Dielectric and Electrical properties of $Ba_{0.5}Sr_{0.5}TiO_3$ Heterostructured Thin Films by Sol-Gel

Technique for Phase Shifter Applications. Menka Jain[1], S. B. Majumder[1], R. S. Katiyar[1], A. S. Bhalla[2], F. A. Miranda[3] and F. W. VanKeuls[4]; [1]Physics, University of Puerto Rico, San Juan, Puerto Rico; [2]Materials Research Institute, The Pennsylvania State University, University Park, Pennsylvania; [3]NASA Glenn Research Center, Cleveland, Ohio; [4]Ohio Aerospace Institute, Cleveland, Ohio.

The preparation of BST heterostructures by sequential deposition of thin films of low dielectric materials (e.g. MgO or $MgTiO_3$) and barium strontium titanate by sol-gel technique is demonstrated to be an effective approach to synthesize dielectric films with low dielectric losses. Although the dielectric constant and tunability are reduced somewhat by the insertion of low dielectric material, the dramatic reduction in the dielectric loss tangent effectively increased the figure of merit of the hetero-structured thin films as compared to the pure BST films. We prepared BST:MgO and BST:$MgTiO_3$ (BST:MT) heterostructured films with different thicknesses of BST/MgO/$MgTiO_3$, and found that there is a considerable effect of thicknesses and the starting layer on the properties of the heterostructured films. The dielectric properties, including tunability, loss tangents, and phase transition behavior, were measured in the frequency range of 1kHz-1MHz on the films. The synthesized films were used to make eight element coupled micro-strip phase shifters and characterized in terms of their degree of phase shift and insertion loss characteristics in a frequency range of 13-15 GHz. BST:MT films showed the figure of merit of 58 ^{o}/dB measured at 533 kV/cm. In the optimized BST:MgO heterostructured film, the high frequency figure of merit (κ=phase shift/insertion loss), dramatically improved to 87 ^{o}/dB measured at 533 kV/cm, which is the highest known value measured in the Ku band region for BST based materials. These results represent the current state of the art technology.

2:30 PM *D10.3
Reliability Issues for ultra-thin ferroelectric thin film capacitors for high-density FRAM applications.
Choong-Rae Cho, YoungSoo Park, Sang Min Shin and June Mo Koo; MD lab., Samsung Advanced Institute of Technology, Suwon, South Korea.

To realize high-density, low operating voltage ferroelectric random access memory devices, reliability issues such as fatigue, imprint, and retention properties for ultra-thin ferroelectric thin films should be resolved, while these properties have been deteriorated seriously as the film thickness is decreased below 100 nm. We have prepared sets of MOCVD PZT thin films with different thickness from 25 nm to 150 nm on different kinds of pure metal and metal oxide substrates. Several tendencies on thickness dependent dielectric and ferroelectric properties have been observed according to electrode material, which could be explained by intrinsic and extrinsic reasons. From the results on systematic studies of the reliability issues, the feasibility for Gigabit density FRAM would be discussed.

2:45 PM D10.4
Data Retention Characteristics and Hydrogen-Induced Degradation in $Bi_{3.25}La_{0.75}Ti_3O_{12}$ Thin Films on Conductive $SrRuO_3$ Electrodes. Jang-Sik Lee, B. S. Kang, Y. Lin, Y. Li and Q.X. Jia; Materials Science and Technology Division, Los Alamos National Laboratory, Los Alamos, New Mexico.

The electrical properties of ferroelectric thin films strongly depend on the electrode materials and crystalline orientation. In this work, $Bi_{3.25}La_{0.75}Ti_3O_{12}$ (BLT) thin films were prepared on $SrRuO_3$ and Pt electrodes by pulsed laser deposition. The electrical properties of the BLT films on different electrode materials were characterized. Both crystalline orientation and the electrical property were controlled by the substrate and the type of the bottom electrode being used. Also, it was found that the conductive oxide electrode showed better endurance over Pt electrode especially in data retention and hydrogen-induced degradation in BLT films. The effects of electrode materials and crystalline orientation on the data retention characteristics and hydrogen-induced degradation in BLT thin films will be discussed in detail.

3:00 PM D10.5
Oxygen Vacancies, Domain Switching and Their Implication for Fatigue in Ferroelectric Perovskites. Yu Xiao and Kaushik Bhattacharya; California Institute of Technology, Pasadena, California.

The role of oxygen vacancy in dielectric breakdown and fatigue has been a topic of intense research in ferroelectric perovskites like $BaTiO_3$. This paper presents a comprehensive model that treats the ferroelectrics as polarizable wide gap semiconductors where the oxygen vacancies act as dopants. First, a fully coupled and nonlinear model is developed with space charges, polarization, electric potential and elastic displacements as variables without making any priori assumptions on the space charge distribution and the polarization profile. Both analytical and numerical results show that polarization profiles and space charge distributions change dramatically when the film thickness and doping level are varied. Particularly, an donor-doped Pt/$BaTiO_3$/Pt structure is considered in this paper in view of the fact oxygen vacancies are acting as donors in ferroelectric perovskite. Second, a 2-D FEM simulation show the interactions of oxygen vacancies with 180° and 90° domain walls. Numerical results show that 90^odomain wall may play a significant role in the fatigue process. Finally the forced diffusion of oxygen vacancies under local electric fields due to nonuniform polarization and space charge generation is considered. The switching process and fatigue are then studied by examining the stability of the system. The probability of fatigue as intrinsic property of the system under different circumstances (film thickness, doping level, defects level etc.) are investigated. Comparison with experimental results and implications for device design are discussed.

3:45 PM D10.6
***InSitu* Infrared Spectroscopy of High-K Dielectric Growth on Si (100).** Rhett Brewer[1], K. Z. Zhang[1], Ming -Tsung Ho[1], Lyudmila Goncharova[1], Marek Boleslawski[2], Torgny D. Gustafsson[1], Eric Garfunkel[2] and Yves J. Chabal[1]; [1]Physics and Chemistry, Rutgers University, Piscataway, New Jersey; [2]Aldrich Chemical Co, Sheboygan Falls, Minnesota.

We have used *insitu*, transmission infrared (IR) spectroscopy and $ex-situ$ Medium Energy Ion Scattering (MEIS) to investigate the growth mechanisms of atomic layer deposition (ALD) of Al_2O_3 and HfO_2 on Si (100). The high-κ materials were deposited by alternating exposures of organometallic precursors (trimethylaluminum for Al_2O_3 and tetrakis(ethylmethylamino)hafnium for HfO_2) and D_2O at 300° C. IR spectroscopy makes it possible to identify the adsorbed precursor products, the growth of the high-κ films, and the formation of an interfacial layer, such as SiO_2. For ALD directly on hydrogen terminated Si (100) we observe the formation of interfacial SiO_2; moreover, several ALD exposure cycles are required before the high-κ film can nucleate on the surface and begin to grow. Functionalizing the surface with a pretreatment of NH_3 results in high-κ film growth from the first cycle exposure, and reduces the formation of interfacial SiO_2 by acting as a barrier and providing a nucleation layer for the high-κ growth. In this talk, we will compare HfO_2 and Al_2O_3 growth.

4:00 PM D10.7
Crystallization Behaviour of Hf-rich Aluminates and Influence on Film Dielectric Properties. Manuel Climent[1], Barbara Crivelli[1], Gabriella Righini[2], Stefano Alberici[1], Mauro Alessandri[1], Alice Camille Elbaz[1], Giuseppe Pavia[1] and Claudia Wiemer[3]; [1]Central R&D, STMicroelectronics, Agrate Brianza MI, Italy; [2]ASM Italia, Agrate Brianza; [3]Laboratorio MDM-INFM, Agrate Brianza, Italy.

The continuous scaling down of transistors and memory devices toward 65-45 nm technology nodes and beyond demands for the replacing of ultra thin SiO2 based dielectrics with high-k materials. Then it is interesting to obtain materials with the highest value of the dielectric constant (k) keeping a good stability of the film during the process flow for the device formation. Thus, it is important to know the influence of the composition, thermal treatments and type of crystallization. In this study, the investigation of physical-chemical stability of Al2O3-HfO2 alloys and their properties upon prolonged post-deposition annealings (PDA) are presented. Different Hf-rich aluminates were analysed, ranging between 20% and 47% Al2O3 mol%. Amorphous films were deposited on RCA treated p-type silicon by ALCVDTM. Post-deposition annealings were carried out in N2 atmosphere, at 800 C for 2 minutes, and 900 C for 2 and 30 minutes. The films were grown in amorphous phase and after PDA treatments the samples were crystallized in different ways. Depending on the crystallization phase, orthorhombic, cubic or monoclinic, the k value can strongly change. Non-contact and XRD techniques were used for the EOT analysis, showing that the k value increases with the temperature and the time of PDA treatments and is strongly affected by the composition of the material. XRF analysis evidenced that samples containing less Al2O3 had a higher k value, that it is a function of the Hafnium concentration. Cross-TEM analysis, evidenced a clear relationship of the crystallization phenomena with PDA treatments and the material composition, showing, for instance, that Hf-rich aluminates crystallizes with orthorhombic phase during treatments at 800 C and 900 C for 2 minutes, and with the monoclinic phase at 900 C for 30 minutes. A full analysis will be reported. As a conclusion, it is possible to tune the final k value of the Al2O3-HfO2 alloys deposited by ALCVDTM by changing the film composition and the temperature and duration of post-annealing treatments.

4:15 PM D10.8
Effects of NH3 pre-anneal deposition on high-k gate stacks.
Naim Moumen[1], Jeff J Peterson[1], Joel Barnett[1], Robert W Murto[1], Gennadi Bersuker[1] and Howard R Huff[1]; [1]FEP, SEMATECH, Austin,

Texas; [2]SEMATECH, AUSTIN, Texas.

The ITRS roadmap calls for the implementation of high-k material as gate dielectric starting with the 65nm technology generation. This requires high quality interfaces between the high-k dielectrics and Si substrate in the channel region. We investigated the effect of surface preparation prior to high-k film deposition on transistor performance. The surface preparation affects the growth of the high-k film and the final EOT. This work discusses the effect of NH3 anneals and process conditions on high-k transistor performance such as gate leakage, Vt and electron mobility. Transistors were fabricated on 200 mm p-type epi <100> Si substrate using a conventional silicon gate transistor process flow with thin high-k dielectrics deposited by atomic layer deposition ALD. The ALD-HfO2 does not grow very consistently on an HF-last surface and the resulting films exhibit high gate leakage current or non-working devices. However, the addition of NH3 pretreatment is shown to affect the properties of the interfacial layer at the silicon/high-k interface, which is critical for controlling the final EOT. An NH3 anneal pretreatment, i.e., an NH3 predeposition anneal (PreDA), after HF-last clean led to the reduction of the interfacial layer at the silicon/high-k interface to 5A which is about 50% thinner than that seen with ALD films grown on chemical oxides without the NH3 PreDA. Lower EOT and lower leakage current are obtained when an NH3 PreDA for ALD HfO2 films follows the HF-last. These surface preparation processes result in an EOT reduction of 4A to 5A versus chemical oxides, providing a potential solution to achieving a sub-1nm EOT

4:30 PM D10.9
IR Absorption Study of HfO_2 and HfO_2/Si Interface Ranging from 200cm^{-1} to 2000cm^{-1}. Kazuyuki Tomida, Haruka Shimizu, Koji Kita, Kentaro Kyuno and Akira Toriumi; Materials Science, The University of Tokyo., Tokyo, Japan.

This paper reports the IR absorption study of HfO_2 ($HfSiO_x$) and HfO_2/Si interface. Although a number of reports on HfO_2 system for CMOS gate dielectrics application have been published, no systematic study with the IR absorption has been reported. The IR absorption data provide the local bonding information of the microscopic structure, the crystallization, inter-diffusion and reaction. First, the thermal treatment effects on bulk HfO_2 and HfO_2/Si interface were investigated with FT-IR as functions of annealing temperature, ambient and initial film thickness. 30 nm HfO_2 was deposited on FZ-Si wafers by RF sputtering, followed by annealing at 400-1000°C for 5minutes in O_2. In the FT-IR measurement, TGS (2000cm^{-1} 600cm^{-1}) & PE-TGS (600cm^{-1} 200cm^{-1}) were employed for the wide range of sensitive detection. Before annealing, it was hard to detect any signal mid-IR region, while there was a broad structure in far-IR region. However, after annealing at 600-1000°C all the annealed samples showed absorption peaks around 1070cm^{-1} and 750cm^{-1}, while in far-IR region absorption peaks at 250, 325, 410, 512 cm^{-1} were clearly observed. The peak intensity of HfO_2, particularly the 325cm^{-1} one, increased with annealing temperature. This fact indicates the local bonding relaxation of annealed samples with the monoclinic phase structure (confirmed by XRD). On the other hand, the 1075cm^{-1} peak is assigned to the Si-O-Si anti-stretching mode, which indicates that SiO_2 was formed at HfO_2/Si interface. To investigate a quantitative difference between the interface grown and thermally grown SiO_2 films, the dependence of the peak wave number on SiO_2 thickness were compared. As a result, no difference was observed between the interface and thermally grown SiO_2. This fact means that the interface grown layer is basically the thermal SiO_2 in terms of the network structure. Next, since it is not easy to distinguish a small amount of silicate in annealed HfO_2/Si system, 20nm $HfSiO_x$ was intentionally deposited by the co-sputtering (Ar+10%O plasma) of Si (3 10%) and Hf, followed by annealing at 400 1000°C for 5 minutes. The sample annealed at 1000°C showed the crystalline structure with monoclinic or orthorhombic, depending on Si %. Only a few at % Si incorporation into HfO_2 drastically reduced the IR intensities of typical HfO_2 peaks such as 250, 325, 410 and 512cm^{-1} ones, even though the monoclinic phase was maintained. Further Si incorporation (about 10 at %) into HfO_2 showed the crystalline structure change from monoclinic to mixed phase of monoclinic with orthorhombic in XRD analysis, and made a new broad IR peak at 450cm^{-1} evidently which was quite different from the monoclinic HfO_2 spectrum. Those far-IR spectra indicate that the bond structure of $HfSiO_x$ (a few percent of Si) is very sensitive to the amount of Si. Conversely, a small amount of Si substantially changes the local bonding characteristics in HfO_2 film.

4:45 PM D10.10
Controlling the metal-oxide-silicon interface: role of initial surface preparation and post deposition annealing.
Ragesh Puthenkovilakam and Jane P Chang; Chemical Engineering, University of California, Los Angeles, California.

Alternative gate dielectric materials such as HfO_2 are required in the future generations of microelectronic devices to enable the rapid scaling of MOSFET devices. As the thickness of gate dielectrics decrease, the electrical performance of the dielectric/Si interface will dominate the transport properties of the MOSFET device. Hence the initial surface preparation of the Si(100) surface prior to the gate dielectric deposition and post deposition annealing can significantly affect the resulting device characteristics. In this work, we investigate the material and electrical properties of ultra thin HfO_2 films on Si(100) substrate. The Si(100) surface was pretreated with a thin layer of rapid-thermally-grown SiO_2 or SiN_x, or a thin layer of SiO_2 grown by UV/O_2 oxidation. HfO_2 films were deposited by an atomic layer controlled deposition process involving alternate pulses of Hf-t-butoxide precursor and oxygen at deposition temperatures from 390°C to 470°C. Post deposition annealing was performed in-situ in various chemistries including O_2, N_2, N_2O, NH_3 and H_2/D_2 at temperatures from 500°C to 1000°C. MOS capacitors were fabricated by depositing aluminum electrodes on top of the deposited films and followed by photolithographic patterning. Material characteristics of the deposited films were analyzed by x-ray photoelectron spectroscopy (XPS), extended x-ray absorption fine structure (EXAFS), and spectroscopic ellipsometry. XPS measurements indicated the formation of interfacial layer between the HfO_2 and silicon and its structural changes upon annealing will be addressed in this talk. EXAFS measurements indicated that the short-range order in these films resembled to that of the monoclinic phase. Capacitance-voltage measurements were performed on MOS devices to extract the dielectric constants, flat band voltage shifts, and interface state densities. Temperature dependent current-voltage measurements were performed to elucidate the conduction mechanisms in these ultra thin films. The as-deposited HfO_2 samples yielded dielectric constants from 18-23 depending on the processing conditions and their leakage currents were significantly less than that of SiO_2 films at the same equivalent oxide thickness. Post-deposition annealing in O_2, NH_3 and N_2O ambient is found to significantly reduce the leakage currents by orders of magnitude though the overall dielectric constant is reduced by O_2 annealing due to the formation of an interfacial layer. Spectroscopic ellipsometry measurements showed notable changes in the dielectric function of the materials upon post-deposition annealing indicating that the bulk properties of the films were affected. Post-deposition annealing in H_2 or D_2 resulted in reduced interface state densities and improved leakage current characteristics while D_2 annealing is shown to increase the reliability of HfO_2 dielectrics upon constant voltage stress.