SYMPOSIUM F

Materials, Technology, and Reliability for Advanced Interconnects and Low-k Dielectrics

April 13 - 15, 2004

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* Invited paper

SESSION F1: Scaling and Integration Challenges
Chairs: Richard Carter and John Ekerdt
Tuesday Morning, April 13, 2004
Room 2003 (Moscone West)

8:30 AM *F1.1
Challenges for the Aggressive Scaling of Advanced Interconnects. Karen Maex, IMEC, Leuven, Belgium.

The introduction of low k materials in IC processes has been very cumbersome due insufficient insight in all materials aspects of the implementation of new materials in such a complex process. Meanwhile the insight in low k dielectrics, their properties and their impact on the processing has become much clearer based on a lot of scientific studies. Besides the low k dielectrics, the aggressive scaling of narrow Cu wires reveals new phenomena and requires novel solutions to maintain or improve the electrical performance of the wires. In this paper an overview will be given on the status and future of aggressive scaling of the Cu/Low k technology. The results will be brought in a wider perspective of the specifications for electrical performance in integrated circuits.

10:00 AM *F1.2
Molecular Caulk: A Pore Sealing Technology for Ultra-Low K Dielectrics. Jay J Senkevich[1], Christopher Jezewski[2,1], Deli Lu[1], William A Lanford[2], Gwo-Ching Wang[1] and Toh-Ming Lu[1]; [1]Physics, Rensselaer Polytechnic Institute, Troy, New York; [2]Physics, University at Albany, Albany, New York.

Much effort has been undertaken to develop high performance ultra-low k (< 2.2) (ULK) dielectrics to improve the interconnect speed and performance of ultra-large scale integrated devices. Metallization issues and their poor mechanical properties have plagued the successful integration of these porous ULK dielectrics. Both of these issues are exasperated by their open pore structure. We have developed a pore sealing technology, which may allow the successful integration of these materials. We have coined the term Molecular Caulking to describe the materials that use the parylene platform for the chemical vapor deposition of these polymers. They are very unique since they can be conformally coated on demanding geometries pin-hole free at a 10 A thickness. We have shown that the 1st generation material is selective against copper and can seal porous-MSQ after 30 A of deposition. This is roughly the pore diameter of this porous ULK dielectric. These materials have a very fast lateral growth rate. In the past parylene supported TEM grids were made with a 16 um hexagonal grid array. An overview will be give with respect to the Molecular Caulking technology.

10:30 AM F1.3
Understanding Plasma-Induced Damage in Integration of Porous Organosilicate Ultra Low-K Materials. Qinghuang Lin[1], S.-T. Chen[2], Stefanie Chiras[1], Steve Cohen[1], Tin Dalton[1], Nick Fuller[1], Andrew Kellock[3], David Klaus[1], Kaushik Kumar[2], Nancy Klymko[2], Vincent McGahay[2], Henry Nye[2], Eva Simonyi[1], Terry Spooner[2], Christy Tyberg[1], H. Wildman[2] and David Gidley[4]; [1]IBM TJ Watson Research Center, YORKTOWN HEIGHTS, New York; [2]IBM Microelectronics Division, Hopewell Junction, New York; [3]IBM Almaden Research Center, San Jose, California; [4]University of Michigan, Ann Arbor, Michigan.

Integration of porous ultra low-K materials into dual damascene Cu interconnects poses significant challenges due to new material chemistry, incorporation of porosity, and degraded mechanical properties. The present work aimed to understand critical materials issues in integration of porous organosilicate ultra low-K materials, particularly plasma-induced dielectric material damage. Extensive analytical techniques were employed to investigate the chemistry, nanostructure, and properties of a porous organosilicate low-K material exposed to both patterning etch and photoresist strip etch chemistries. These analytical techniques include FT-IR, 29Si Nuclear Magnetic Resonance Spectroscopy (NMR), Rutherford Backscattering Spectroscopy (RBS), X-ray Photon Spectroscopy (XPS), Positronium Annihilation Lifetime Spectroscopy (PALS), Surface Contact Angle, and Scanning Electron Microscopy (SEM), dielectric constant, and breakdown measurements on a metal-insulator-silicon structure. While patterning etch does not change the electrical properties of the porous organosilicate low-K material appreciably, various photoresist strip etch chemistries cause significant increases in the dielectric constant and leakage current as well as formation of dielectric voids in the resultant plasma-treated porous organosilicate low-K material. The degradation of the electrical properties of the plasma-treated porous organosilicate low-K material is attributed to the de-methylation and partial cleavage of Si-O-Si bonds to form more hydrophilic Si-OH groups in the surface layer. A bilayer model has been found to account for the plasma-treated porous organosilicate low-K material. This bilayer model consists of an unaltered bottom layer and a hydrophilic, denser, higher-K surface layer. The chemistry, nanostructures, properties, and pore-sealing capability of the plasma-damaged surface layer will be presented. Implications of the bilayer model for the integration of porous organosilicate low-K materials will also be discussed.

10:45 AM F1.4
Repair of Porous Carbon Doped Ultra low-k Films Using Supercritical CO2. Bo Xie and Anthony J Muscat; Chemical & Environmental Engineering, University of Arizona, Tucson, Arizona.

The next generation of low-k dielectric films will contain manufactured pores to achieve dielectric constants below 2.6 for the 65 nm technology node and beyond. Low-k films are needed in device integration to lower power consumption and minimize cross talk between metal lines. Pores compromise the structural integrity of low-k films and must be cleaned, free of etching damage, and capped before deposition of the barrier and seed layers. Water is introduced into organosilicate low-k layers in the form of silanol (Si-OH) groups during ashing of photoresist. Supercritical carbon dioxide (scCO2) has no surface tension, which makes it a promising technology for cleaning and repair of porous low-k films. Fourier transform infrared (FTIR) spectroscopy, electrical measurements, and contact angle were used to investigate the effect of adding Si-bearing precursors to scCO2 to repair etched and ashed blanket porous ultra low-k (ULK) methyl silsesquioxane (MSQ) films (JSR LKD5109) (k = 2.5). ULK MSQ films were processed in scCO2 containing 1-2% precursor by volume at 200-300 atm and 45-55°C for 2 min soak times. The results with the Si-bearing precursors hexamethyldisilazane (HMDS) and trimethylchlorosilane (TMCS) showed that both lone (SiO-H) and H-bonded (SiO-H) silanol groups reacted. A k value of 2.5 ± 0.2 was measured on MIS devices made using the blanket films from CV curves in accumulation. The contact angle was over 100° indicating that the surface of the film was hydrophobic. Ashing in an oxygen plasma converted a portion of the Si-CH3 groups into silanol (SiO-H) groups in the pores of the MSQ films. The silanol moieties raised the k value to 3.5 ± 0.1 and reduced the contact angle below 10° indicating that the surface was hydrophilic. The hydrophobicity of the starting surface before ashing was recovered after HMDS and TMCS treatments as confirmed by contact angle measurements (>80°), and the dielectric constants were reduced to 2.4 and 2.6, respectively, which are close to the starting value before ashing. Moreover, films repaired with these chemistries were stable over time with minimal uptake of water from ambient air. Cross-sectional transmission electron microscopy (TEM) images showed that after 1% HMDS addition to scCO2 at 212 atm and 57°C for 2 min, the pores had nearly spherical geometries with diameters of approximately 1-6 nm. HMDS and TMCS treatments are an effective approach to restore the degradation of ULK MSQ films due to plasma ashing but work is needed to learn how to completely close off the pores at the surface. Electrical leakage measurements after different steps in the processing sequence are currently being done to complement the CV curves and spectroscopic information obtained on ULK MSQ films. In addition, work is in progress to systematically investigate precursor chemistries.

11:00 AM F1.5
Sidewall Damage and Electrical Performance of Porous Dielectrics in Narrow Spaced Interconnects. Francesca Iacopi[1,2], Youssef Travaly[1], Michele Stucchi[1], Victor Sutcliffe[3], Herbert Struyf[1], Stefan Peeters[4], Rik Jonckheere[1], Peter Leunissen[1], Marleen Van Hove[1] and Karen Maex[1,2]; [1]SPDT, IMEC, Leuven, Belgium; [2]E.E. Dept., Katholieke Universiteit Leuven, Leuven, Belgium; [3]affiliate at IMEC from, Texas Instruments, Dallas, Texas; [4]affiliate at IMEC from, LAM Research, Fremont, California.

Recent studies have shown that porous low-k dielectrics are extremely sensitive to exposure to plasma processes, due to the diffusion of reactive species into the film through the pore network. The damage induced in the low-k material upon exposure to dry etch and ash plasmas through recesses sidewalls is a point of major concern in terms of preservation of the dielectric properties. The weight of the damaged dielectric portion will have an increasing effect onto the overall electrical performance as interconnects line spacing shrinks. Meander-fork structures with spacings between 250nm and 70nm are used in this study as vehicle to investigate trends in electrical performance for different dielectrics and patterning chemistries. SiO2 and SiOC:H low-k materials with increasing porous volume are compared as Inter-Metal-Dielectrics. For SiO2 no significant dependence of dielectric performance on interline spacing is found. A clear worsening in leakage and breakdown is observed for the porous materials as the spacing shrinks, especially when oxidizing strip chemistries are used. In the latter case, I-V curves indicate a deviation from the expected Schottky conduction mechanism [1] that could point to an increased ionic contribution. The extent of processing damage is found to be larger for increasing dielectric porosity, as indicated by the electrical equivalent sidewall damage [2] extracted from interline capacitance measurements. Line-to-line electrical analysis is also supported by physical characterization of the

interconnect structures by Energy Filtering TEM. [1] T.C.Chang et al, Electrochem.Solid St. 6(4), F13-F15, 2003; [2] F.Iacopi, M.Stucchi, O.Richard, K.Maex, to appear in Electrochem.Solid St.

11:15 AM F1.6
The effect of hydrogen plasma on extreme low-k porous SiCOH dielectrics. Alfred Grill and Vishnubhai Patel; IBM - T.J. Watson Research Center, Yorktown Heights, New York.

SiCOH (carbon-doped oxide) films are often exposed to hydrogen containing plasmas in the interconnect integration process. Hydrogen plasma treatments have been proposed to prevent hybrid organic siloxane polymer (HOSP) films, of similar compositions to SiCOH, from damage during photoresist stripping in oxygen plasma. The present study was directed to understand the effect of hydrogen plasmas with, extreme low-k porous SiCOH (pSiCOH) films. The pSiCOH prepared by plasma-enhanced chemical vapor deposition (PECVD), have been exposed to hydrogen plasmas on grounded or negatively biased substrates, in the as-deposited or after thermal anneals. The films treated in the hydrogen plasmas have been characterized by Fourier transform infrared (FTIR) spectroscopy, Rutherford backscattering and forward recoil elastic scattering analysis, and electrical measurements on metal-insulator-silicon structures. It was found that the hydrogen plasma removes CH3 fractions from the films, decreases the amounts of cage type SiO bonds, and densifies the films, thus increasing the dielectric constants. These effect were enhanced on films exposed to ion bombardment on the negatively biased substrates during the treatment in the hydrogen plasma.

11:30 AM F1.7
Optimization of Dielectric Cap Adhesion to Ultra-Low-k Dielectrics. Greg Spencer, Alfred Soyemi, Kurt Junker, Jason Vires, Michael Turner, Stuart Kirksey and David Sieloff; Semiconductor Products Sector, Motorola, Inc., Austin, Texas.

In order to meet the RC-delay requirements of future technologies, low-dielectric constant (low-k) back-end integrations are required. The 2002 ITRS roadmap indicates dielectric k values of less than 2.7 will be required for the 130nm technology node with a reduction to ultra-low-k (ULK) dielectric k values of less than 2.4 for the 90nm node, and further reduction to less than 2.1 for the 65nm node. While the integration of materials with k value near 3.0 has been demonstrated, the integration of ULK materials poses many new challenges due to the low mechanical strength and high porosity of the dielectrics. In addition, ULK dielectric interface adhesion strength, both to underlying substrates and to capping materials, has been observed to be an issue. It is integration challenges such as these that are likely to lead to the push-out of ULK target nodes when the 2003 ITRS roadmap is released. This current work focuses on improving the adhesion strength of chemical vapor deposition (CVD) dielectric caps to ULK materials as this is the weakest interface for the materials studied, i.e. adhesion failures during 4-point bend testing consistently occur at this interface. These dielectric cap materials are required due to the relatively low mechanical strength of ULK materials, and since the cap material must provide adequate strength to act as a chemical-mechanical polish (CMP) stop, adhesion of the cap is critical to prevent delamination during polishing. In this work, the adhesion of CVD dielectric caps to a ULK MSQ (Methylsilsesquioxane) spin-on dielectric (SOD) with a k value of 2.2 and a ULK CVD material with a k value of 2.6 is presented along with preliminary results for an MSQ ULK SOD with a k value of 2.0. A substantial improvement in cap adhesion to both the k2.2 ULK MSQ SOD and the ULK CVD material is demonstrated. This improvement is obtained using a low-k CVD glue material between the ULK dielectric and the subsequent cap material, and by optimizing the CVD cap film deposition. Four-point bend measurement of adhesion strength is used to quantify the improvement in interface adhesion. These measurements indicate a 100% improvement in the cap to k2.2 ULK SOD film adhesion and more than a 75% improvement in the cap to ULK CVD film adhesion. This improvement in CVD cap adhesion is demonstrated to be strongly dependent upon both the glue layer film and the cap deposition conditions. In addition, the improvement in cap adhesion is obtained without significant degradation (<2%) in the k value of the dielectric stack. The preliminary work on the k2.0 MSQ ULK SOD shows that while the k2.0 and k2.2 materials are similar, the improvement in adhesion does not convey to the k2.0 material. These results indicate that as the k value of ULK materials continue to decrease, more work will be needed to improve the adhesion of capping materials to the ULK dielectric films.

11:45 AM F1.8
Process-Oriented Stress Modeling and Stress Evolution During Cu/Low-k Beol Process. Charlie Jun Zhai[1], Paul R. Besser[1], Frank Feustel[2], Amit Marathe[1] and Richard C Blish[1]; [1]Advanced Micro Devices, Sunnyvale, California; [2]Advanced Micro Devices, Dresden, Saxony, Germany.

The damascene fabrication method and the introduction of low-K dielectrics present a host of reliability challenges to Cu interconnects and fundamentally change the mechanical stress state of Cu lines. In order to capture the effect of individual process steps on the stress evolution in the BEoL, a process-oriented modeling approach was developed. In this model, the complete stress history at any step of BEoL has been simulated as a dual inlaid Cu structure is fabricated. Element birth and death, a modeling feature embedded in commercial FEA software ANSYS, is used to achieve this objective. By using element birth and death, any element during the simulation can be killed or activated so as to replicate the actual process, which adds (CVD dielectric deposition/Cu plating) or removes (dielectric etch or Cu CMP) materials. The inputs to the model include the temperature profile during each process step and materials constants. The film stress evolution is simulated during the process of multi-step processing, and the fabricated dual inlaid Cu/FTEOS and Cu/low-k (CVD carbon-doped dielectrics) structures are subject to thermal mechanical loading conditions (i.e. temperature cycling). Furthermore, the modeling was applied to investigate the effect of line width, line space (pitch), dielectric material properties and barrier metal thickness on the volume-average Cu line stress. While only linear elasticity is considered during the process-modeling, the structure is subject to temperature cycling, and the stress-relaxation behavior of Cu at elevated temperatures is modeled using a power-law creep model to simulate. The modeling results are verified in two ways: through wafer-curvature measurement during multiple film deposition processes and with X-Ray diffraction to measure the mechanical stress state of the Cu interconnect lines fabricated using 0.13um CMOS technology.

SESSION F2: Diffusion Barriers
Chairs: Toh-Ming Lu and Jay Senkevich
Tuesday Afternoon, April 13, 2004
Room 2003 (Moscone West)

1:30 PM *F2.1
Study of inorganic-organic interface formation by the reaction of organo-transition metal complexes with self-assembled monolayers with tailored organic functional endgroups. James R Engstrom, Chemical Engineering, Cornell University, Ithaca, New York.

Organic materials are playing an increasing role in modern microelectronic devices- beyond their traditional role as photoresists. New areas include their application as low-κ dielectrics. Interfaces between organics and metals are also of interest, including in fields such as molecular electronics and organic light-emitting diodes. To date, the great majority of the work concerning the formation of organic-metal interfaces on pre-existing organic layers has involved metal thin films deposited by (elemental) evaporation. In the work described here we examine an alternative approach to the formation of inorganic-organic interfaces, namely, via the use of organometallic (e.g., Ti and Ta) complexes. Concerning the organic layer itself, we make use of self-assembled monolayers (SAMs) with a variety of organic functional endgroups (OFG), e.g., -OH, -NH_2 and -CH_3. Using a variety of techniques, including molecular beam scattering and x-ray photoelectron spectroscopy, we have investigated a number of issues that are key to the formation of abrupt and robust interfaces between organic materials and inorganic thin films. These issues include the kinetics and mechanism of adsorption of the organometallic precursors on surfaces possessing different organic functional groups, the ability of the precursor to penetrate the organic layer, and the ability to form uniform inorganic multilayers on the SAMs using atomic layer deposition. In addition to examining the temperature dependence of these processes, using supersonic molecular beam techniques we are also able to examine explicitly the roles of incident molecular kinetic energy and beam angle of incidence in promoting reaction between the organometallic precursors and the OFG, penetration of the SAM, etc. Finally, in selected cases we are able to compare directly to predictions made by *abinitio* quantum chemical calculations of the reaction kinetics, which provides additional insight into inorganic-organic interface formation.

2:00 PM F2.2
Using Self-Assembled Monolayers as Model Substrates for ALD. Caroline Mary Whelan[1], Anne-Cecile Demas[1], Jorg Schuhmacher[1] and Karen Maex[2,1]; [1]SPDT, IMEC, Leuven, Belgium; [2]Electrical Engineering, KUL, Leuven, Belgium.

The trend towards increasing functional density in integrated circuits cannot be supported by traditional materials. Device performance dictates a transition from SiO2 to an insulator with lower dielectric constant (k) and Cu instead of Al for lower resistance wiring. Such interconnect metallization requires the introduction of a barrier layer to prevent Cu diffusion under electrical bias. It is, however, difficult to

obtain conformal barriers of the thicknesses (< 5 nm) foreseen in future device architectures without resorting to unconventional methods. To this end, the unique self-limiting and inherently conformal method of atomic layer deposition (ALD) of films from W, Ti, and Ta compounds is being investigated. Based on sequential saturated gas phase-surface reactions, the growth rate in ALD is in theory layer-by-layer, controlled by the number of deposition cycles. In practice, the early stages of film formation may be non-linear, involving three-dimensional growth depending on substrate reactivity. Due to the heterogeneous nature of low-k materials, our understanding of the role of the initial surface on ALD-mediated growth mechanisms is limited. In this study, we explore the use of self-assembled monolayers (SAMs), organic films formed spontaneously upon adsorption from the gas or liquid phases, as model substrates for ALD WCN diffusion barrier nucleation and growth. Multi-technique characterisation including X-ray, fluorescence, mass, and electron spectroscopies and high-resolution microscopies are used to evaluate various ALD/organic systems. Our results reveal that variation of the alkyl chain length and terminal functionality (comprising for example methyl, cyano, thiol, halide groups) of silane-derived SAMs can be used to manipulate metal deposition and hence barrier properties. We demonstrate that, via tuneable structure and surface chemistry, SAMs provide a novel approach to interface engineering, essential in extending the boundaries of current microelectronics technology.

2:15 PM F2.3

Carboxyl terminated molecular assemblies as interfacial diffusion inhibitors for future nano-devices. P.G. Ganesan, Amit Pratap Singh and Ganapathiraman Ramanath; Material Science and Engineering, Rensselaer Polytechnic Institute, Troy, New York.

As the device dimension shrinks systematically, in sub-50-nm scale devices, inhibiting interfacial diffusion is very challenging. Particularly, in the case of Cu/SiO_2 interface, conventional barriers (refractive metal based materials) are ineffective at thickness less than 10 nm, due to difficulties in conformal deposition in high aspect ratio trench structure. Although, evolving ALD technique yields conformal barriers, interfacial mixing and high level of diffusion paths limits its effectiveness at sub-5-nm thickness. This leads to exploring new materials and process. Recently, we demonstrated use of molecular assembly of nanolayers as a diffusion barrier at Cu/SiO_2 interface. The rationale of using molecules for inhibiting Cu diffusion is based on anchoring the termini of the molecular constituents to the overlayer and underlayer through strong, but highly local, interfacial interactions. We show molecules with carboxyl functional group effectively inhibits deleterious Cu diffusion to SiO2 under layers. Interpose of carboxyl terminated branched molecules such as Polyacrylic acid (PAA)/ Polyethyleneimine (PEI) polyelectrolyte bilayers, at the Cu/SiO_2 interface leads to 10-fold enhancement in lifetime of the $Cu/SiO_2/Si$ MOS device. Similarly, carboxyl terminated linear molecules such as self-assembled monolayers also show 14-fold enhancement in device lifetime indicating molecular structure is insignificant in blocking Cu. Analysis of device lifetime as a function of number of polyelectrolyte layers, and fracture surface by X-ray photoelectron spectroscopy show that interfacial interaction of COOH group and Cu is critical factor to inhibit Cu diffusion. In particular, coordination complex formation between Cu^+ and COOH at barrier/Cu interface hinders diffusion of Cu^+ions into SiO_2. Barrier performance of the carboxyl-terminated molecular assembly is batter than all the other functional group molecular assembly we studied and also batter than conventional Ta barrier layer. Based on the above, we will present a model to explain important factors that influence interfacial diffusion in Cu/molecular layer/dielectric structures.

3:00 PM *F2.4

Growth and Properties of Ultra-thin Composite Ru/Ta Barriers. John G. Ekerdt[1], Qi Wang[1], Andrew Lemonds[1], Tibor Bolom[1], Patrick Fitzpatrick[1], Wesley Ahern[1], Yang Ming Sun[2] and John M White[2]; [1]Chemical Engineering, University of Texas at Austin, Austin, Texas; [2]Chemistry and Biochemistry, University of Texas at Austin, Austin, Texas.

This paper addresses near-zero thickness copper diffusion barriers needed to realize interconnect performance improvements by reducing the RC delay in the sub-50 nm technology nodes. Growth of ultra-thin films of Ru on Ta by chemical vapor deposition (CVD) and growth of ultra-thin Ta films on various dielectric surfaces by atomic layer deposition (ALD), and the supporting surface chemistry to explain the growth processes are presented. The materials properties of the constituent films and the composite films are reported. Composite barrier effectiveness against copper diffusion will be tested $in-situ$ using metal-insulator-semiconductor test structures and will be reported at the meeting. Ruthenium films are selected because of their excellent wetting properties with Ta and Cu, their potential for seedless Cu plating, and the reducibility of its oxide. A low temperature CVD process for ultra-thin Ru films on PVD Ta and SiO2 surfaces was developed using ruthenium carbonyl $[Ru_3(CO)_{12}]$ as the precursor. Films deposited at substrate temperatures between 423 and 593 K were characterized using $in-situ$ X-ray photoelectron spectroscopy (XPS), atomic force microscopy, and $in-situ$ four-point probe resistance measurements. A pure, 3.5 nm thick Ru film with low resistivity (30 $\mu\Omega$.cm) was deposited on SiO_2 at 423 K. Ion scattering spectroscopy (ISS) and Ta 4f XPS peak attenuation indicated that the minimum thickness to form a continuous Ru film on Ta and on SiO_2 is 2.5 nm. The barrier properties will be reported as both the Ru thickness is varied from 2.5 to 5 nm and the Ta thickness is varied from 3 to 0 nm. The ALD deposition of Ta-Si thin films was achieved on SiO_2 at 473 K through the repetition of separate, alternating exposures to TaF_5 and Si_2H_6. Films were deposited and $in-situ$ analyzed by XPS to evaluate growth kinetics, interfacial chemistry with the substrate, and film composition. The first 25 exposure repetitions result in an average film thickness of 0.3 nm. Afterwards, film thickness increased linearly at a rate of 0.1 nm/cycle and films deposited using 50 ALD cycles were about 2.5 nm thick. The Si content, which is uniform throughout the films, can be as high as 40 percent and is dependent on temperature and exposure cycle times. Fluorine concentration is highest at the growth surface yet fluorine persists into the film. On-going experiments to eliminate the fluorine and minimize the silicon will be presented at the meeting.

3:30 PM F2.5

Interfacial differences between sputter-deposited Ru and Ta on low-dielectric substrates: The role of carbide formation. Jeff A. Kelber, Xiaopeng Zhao and Jinghong Tong; Chemistry, University of North Texas, Denton, Texas.

We report XPS studies of the interfacial chemistries between sputter-deposited Ru, sputter-deposited Ta on parylene and Si:O:C low-dielectric substrates. Ruthenium is the subject of increasing interest for ULSI copper/low-k applications, due to its semi-noble nature and the fact that the conductive nature of ruthenium oxide phases may mitigate contact resistance problems. Parylene is contemplated as a pore-sealing material for porous ultra-low dielectric substrates. Sputter deposition of Ta on parylene yields a tantalum carbide (TaC) phase approximately $60\AA$ thick, prior to the evolution of metallic Ta. Similar results are observed for Ta sputter-deposited onto an Si:O:C substrate. Subsequently deposited Cu will not wet TaC, and therefore the formation of a TaC interphase before metallic Ta formation limits the ultimate thickness of sputter-deposited Ta barriers on carbon-containing substrates. In contrast, sputter deposition of Ru on parylene results in conformal growth of the first layer, followed by 3-D nucleation of metallic Ru in the second layer, without carbide formation. Similar results are observed for Ru deposition on an Si:O:C substrate. These results indicate the formation of a laminar Ru/substrate interface, without thickness limitations imposed by a carbide interphase. These results suggest a substantially higher kinetic barrier to Ru carbide than to Ta carbide formation, since the corresponding enthalpy of formation is greater for Ru carbide. The data also indicate that substantially thinner barrier layers are possible for sputter deposited Ru than for Ta on these materials.

3:45 PM F2.6

Formation of ALD Ta(N) Barriers on Porous Trikon Low k Surface. Junjun Liu[1], Michael Scharnberg[1], Junjing Bao[1], Paul S. Ho[1] and Michael Lu[2]; [1]Microelectronic Research Center, University of Texas, Austin, Texas; [2]LSI Logic, Portland, Oregon.

Proper surface chemistry and sealed top surface are important for formation of ultra-thin barrier layer by atomic layer deposition (ALD) on porous ultra-low k dielectric surfaces. An ALD system with in-situ XPS analysis capabilities was developed to study the formation of ALD barriers on low k dielectrics. The versatile surface pre-treatments with an atom/ion hybrid source and in-situ XPS analysis capabilities make this system well-suited for studying the effects of surface modification and pore sealing pre-treatments of porous low k surfaces prior to the deposition of ALD barriers. The formation of ALD Ta(N) barriers on a dense Organosilicate Glass (OSG) film and porous Trikon low k films under various process conditions has been investigated in detail with in-situ XPS analysis. A long incubation period and slow initial growth rate were observed even on the dense OSG film. More energetic or reactive nitrogen species were found to deplete the methyl groups from the surface and result in a surface with more nitrogen termination. The correlation between the ALD growth rate and surface concentration of Si-O and Si-N bond densities was observed. Addition of sufficient atomic hydrogen species at an optimal substrate temperature was found to be able to enhance the reaction, reduce the metal compound to a more conductive phase and decrease the chlorine impurity content. Nitridation of the low k surface with atomic species extracted from NH3 ECR plasma is compared with several other treatments. Effectiveness of pore sealing with these surface treatments is to be investigated by angle dependent XPS and cross section high resolution TEM.

4:00 PM F2.7

Nucleation and Growth Dependence of ALD WNC on Substrate Surface Condition. Thomas Abell[1], Jorg Schuhmacher[2], Youssef Travaly[2] and Karen Maex[2]; [1]Intel, Leuven, Belgium; [2]IMEC, Leuven, Belgium.

Atomic layer deposition (ALD) is an attractive method to deposit ultrathin Cu diffusion barrier films for semiconductor interconnect applications due to the high conformality of deposition. The ALD process relies upon chemisorption of precursor molecules onto the surface of the substrate for nucleation. Thus, ALD processes are inherently sensitive to the starting surface chemisty of the substrate. Integration of ALD with porous low k dielectric materials can be problematic due to the heterogenous nature of the surface chemistry at a molecular level and the ability of gaseous ALD precursors to penetrate into the porous structure of dielectrics allowing unwanted internal deposition. This work focused on the WNC ALD process and attempted to assess the sensitivity of the precursor chemisty to the starting surface condition for several material types from thermal oxide to ultra low k dielectric films. An investigation into different surface treatment conditions to modulate the nucleation and growth was also conducted. ALD WNC nucleation and growth was observed to be strongly affected by different substrate materials and surface chemistries. Nucleation was found to be inhibited on hydrophobic surfaces, which is attributed to low concentrations of chemisorbtion sites for precursor molecules as confirmed by TOFSIMS. Surface closure and surface roughness of the WNC layer was found to strongly correlate with starting surface condition as measured by TOFSIMS, EP and AFM. Surface densities of chemisorbtion sites (e.g. -OH, -NH2) can be increased for low k materials by plasma treatments. These plasma treatments can also seal the surface of some low k materials to penetration of precursor molecules into the bulk of the films. Various reactive and non-reactive plasma treatments were investigated for sealing, changes in surface chemistry and WNC growth. W penetration into porous surfaces was studied with RBS, XRR, TEM and spot EDS. Resitivity of the WNC films was also seen to vary with different surface condition as measured by 4 point probe with SE, TEM and XRR thickness measurements. W concentration in the resulting films was measured by RBS and XRF. Thickness and resistivity differences lead us to believe that the structure of the WNC ALD films was strongly affected by the initial nucleation site density. Low nucleation densities appear to lead to less conductive films. Interestingly, XRR indicates similar top surface densities for the different films. It is believed that once surface closure was complete the ALD process became independent of the starting surface and produced top surfaces of similar density. These results will be compared to fundamental reaction chemistry for the WNC process and nucleation and growth models.

4:15 PM *F2.8

Ultra low-dielectric-constant materials for 65nm technology node and beyond. Hao Cui, APMD, LSI Logic Corp., Gresham, Oregon.

The impact of different dielectric layers in Cu dual-damascene (DD) interconnects on the overall effective dielectric constant (k) have been simulated. Positron Annihilation Lifetime Spectroscopy and Ellipsometric Porosimetry analyses show that interconnected mesopores of diameter greater than 3.5 nm start to appear in PECVD SiCOH materials as the k value goes below 2. This presents great process integration and reliability challenges. Reducing the k values of other dielectric layers in Cu DD structures helps to alleviate the k value requirement of the ILD materials while still meeting the effective k value target. Properties of PECVD hydrogenated silicon carbide (SiC) films with k of 3.0 were studied for dielectric barrier and etch-stop applications. These films were also compared to PECVD SiC and silicon carbon nitride (SiCN) films with k of 4.5-5.0. The chemical compositions of these films were determined using RBS and HFS. The C/Si ratio of the ultra low-k SiC films was found to be close to 2:1, compared to 1:1 of SiC films with higher k. These indicate that less Si-C networks are formed and more micro-porosity is incorporated in the ultra low-k SiC films. The chemical bonding structures were studied using FTIR spectrum. Using MIS capacitors with Cu as the gate electrode, the leakage current of these films at 1.0 MV/cm was measured to 2.3E-10 A/cm2, which is about 5 times lower than SiC and SiCN films with higher k. The etch rates of ultra low-k SiC films have been found to be negligible using standard SiCOH etch chemistry. Such extremely high etch selectivity makes these films robust etch-stop layers.

4:45 PM F2.9

Evaluation of PECVD deposited Boron Nitride as Copper Diffusion Barrier on Porous Low-k Materials. Jun Liu[1,2], W. D. Wang[1], Lei Wang[1], D. Z. Chi[1] and Kian Ping Loh[2]; [1]Institute of Materials Research and Engineering, Singapore, Sinapore, Singapore; [2]Chemistry Department, National University of Singapore, Singapore, Singapore.

Ultra low dielectric constant (k) material is needed as the inter-metal dielectrics to reduce RC delay when device dimension scales to sub-0.1um dimension. Nanoporous materials have been considered as good candidates for the inter-metal dielectrics due to their ultra low-k properties. Identifying a copper diffusion barrier on the nanoporous substrate is critical for the damascene fabrication process. In this study, we have evaluated the compatibility of plasma-deposited amorphous Boron Nitride film as copper diffusion barrier on two types of porous low k materials: LKD5109 (from JSR) and Zirkon 2200 (from Shipley). Both Microwave Plasma CVD (2.45 GHz) and Radio-frequency Plasma CVD (13.56 MHz) were applied for the BN deposition in order to evaluate the compatibility of the two plasma processes with the nanoporous films. Growth parameters were optimized to minimize the boron diffusion and carbon depletion within the nanoporous substrate, which were found to have deleterious effects on the dielectric properties. FTIR, Raman and XPS were employed for analyzing the changes in chemical structure of the low-k films after BN growth. Capacitance-voltage measurement was used to characterize the dielectric constants of amorphous BN ($k\approx2.4$) on Si and BN-integrated porous low k materials (keff ≈2.3). I-V measurement and SIMS characterization were carried out to estimate the performance of the BN film against copper diffusion. We found that an ultra-thin (20 nm, by XSEM) densified layer that was formed on the surface of LKD after BN deposition may enhance the diffusion barrier performance.

SESSION F3: Poster Session: Low-K Materials,
Diffusion Barriers, and Metallization
Chairs: Richard Carter and Stefan Schulz
Tuesday Evening, April 13, 2004
8:00 PM
Salons 8-9 (Marriott)

F3.1

Characterization and preparation of porous low dielectric films using silsesquioxane(SSQ) polymer and silica sol nano particle as constructing materials, cyclodextrin derivatives as nanopore forming materials. Taewan Kim[1], Jihoon Rhee[1], Jong baek Seon[2], Kwang hee Lee[2], Daechul Park[1], Jaho Koo[1] and Hyundam Jung[2]; [1]R&D CENTER, Samsung Corning, Suwon, Kyounggi-Do, South Korea; [2]EM-LAB, Samsung Advanced Institiue of Technology (SAIT), Yongin, Kyounggi-Do, South Korea.

The industry has been strongly interested in integrating porous low-k materials to enhance mechanical properties to meet manufacturing demands of LSI device. Porous silica films are strong candidates among those, which were formed from silsesquioxane (SSQ) polymer by the addition of nanopore forming materials to the SSQ polymer. As nanopore forming materials such as cyclodextrin derivatives were introduced into SSQ polymer matrix in thin films, not only dielectric constant was decreased on account of formed nanopore but also mechanical properties such as hardness and modulus were worsed, while the demand of mechnical properties have been increased strongly for the application of the film into interlayer dielectric structure of the LSI device. The low-k thin films using silica sol as one of constructing materials have good transparency, high hardness and modulus, while their dielectric constant is still relatively lower than that of the other ceramic sol. Nanosized silica sol was very unstable in hydrophobic solvent which has less hydroxyl group because of a large amount of hydroxyl group on its surfaces. Silica Sol whose primary particle size is 5 15 nm in those solvents not requiring surface modification of particle and adding an additive, was prepared and characterized. Thin films using a silsesquioxane (SSQ) polymer and the nanosized silica sol which has significant amount of hydroxyl group on the surface as constructing materials and cyclodextrin derivatives as nanopore forming materials were prepared. Especially the electrical properties of the films were monitored with varying porogen contents. Surface morphology and nanostructure were investigated by using AFM, vertical SEM and TEM. In addition, residual hydroxyl group of thin films was investigated by using FT-IR. Mechanical properties of the film were better than those of thin film made from only silsesquioxane (SSQ) polymer as constructing materials, though k-value was increased slightly. These results indicated that there is difference of mechanical properties between used only silsesquioxane (SSQ) polymer as constructing materials in thin films and silsesquioxane (SSQ) polymer and nanosize silica sol which has significant amount of hydroxyl group on its surface as constructing materials.

F3.2

Engineered Low-k ($k < 2.5$) PECVD a-SiCO:H films for 65nm Technology and Beyond. Byung Keun Hwang, Mark Loboda, M.-S. Tzou, B. Nguyen, M. Tomalia, W.B. Heilig, P. Cannady and G.A. Zank; Advanced Technologies & Ventures, Dow Corning Corporation, Midland, Michigan.

For silicon CMOS microelectronics applications targeted with 65 nm gate lengths, it is expected that low-k dielectric materials with k<2.8 will be required in order to produce interconnection structures with the required minimum gate delay. Research to develop low dielectric constant materials with k<2.8 have tended to concentrate on producing porous films by both CVD and spin on technologies [1]. Integration efforts using designed porous low-k materials have not produced results consistent with expectations based on experiences from established low-k processes at the 130 and 90 nm technology nodes. Continuing research in Dow Corning Thin Film Technology Platform focuses on developing molecular engineering concepts to extend the performance of incumbent organosilicon low-k PECVD processes [2] and produce robust films with k<2.8. In one approach, as an alternative to porous oxide strategy, the C/Si ratio in the film can be manipulated in a way to reduce the film permittivity. As an example, the experimental performance results of one new carbon enriching PECVD process chemistry have demonstrated it is possible to reduce the relative permittivity to the range of 2.5 to 2.2 with a specifically designed precursor. The properties of new engineered a-SiCO:H films are shown in the attached tables. The typical atomic composition of the a-SiCO:H film with the dielectric constant < 2.5 shows a ratio of carbon to silicon of 2.6 by X-ray photoelectron spectroscopy (XPS) and 3 by Rutherford backscattering (RBS). The bulk film density measured by RBS-HFS was 1.2 g/cm3. These films have good electrical isolation characteristics and show thermal stability to 400 C. Unexpectedly, it is observed that while the permittivity of the SiCOH film is reduced, the density and mechanical properties are comparable with that of trimethylsilane-based a-SiCO:H films with the dielectric constant of 2.7. 1. Y. Yang etal, IEEE International Interconnect Technology Conference, pp 12 (2003); E. Moyer etal, ibid, pp 196 (1998). 2. M.J. Loboda etal, 1999 Advanced Metalization Conference; W.D. Gray etal, 2002 Advanced Metalization Conference

F3.3

Nanoporous Organosilicates Templated from Unimolecular Self Organizing Polymers. james lupton hedrick, T Magbitang, V Y Lee, H.-C. Kim, W Volksen and R D Miller; IBM Research, San Jose, California.

We have demonstrated that star-shaped polymers with a compatibilizing outer corona can be dispersed into a thermosetting organosilicate and used to create a nanoporous material. These stimuli-responsive, copolymers create nano-sized domains through a matrix-mediated collapse of the interior core of the core-corona polymeric structure. Clearly, this approach relies on the outer corona of the star to compatibilize the insoluble core with the thermosetting resin and prevent aggregation such that these individual molecules template the crosslinking of the matrix and ultimately generate a single hole. The organic polymer was selectively thermalized to leave behind its latent image in the matrix with a pore size that reflected the size of the polymer molecule, and provided the expected reduction in dielectric constant. The smallest pore sizes achieved by the star and dendrimer-like star macromolecular architectures is in excess of 10nm, which is too large for future device generations. To address this, we will describe the templating of organosilicates from new macromolecular architectures that reside at the interface of small-molecule and polymeric amphiphiles. By developing new and well-defined synthetic procedures to produce environmentally responsive macromolecules, macroscopic, nano-structured thin films of technological interest were produced.

F3.4

Preparation and structure of Organic/Inorganic Hybrid Materials Based on Polyphenylsilsesquioxane.
Seung Sang Hwang, Sungwon Ma, Hangseok Lee and Cheol Chung; Polymer Hybrid Center, Korea Institute of Science & Technology (KIST), Seoul, South Korea.

New hybrid materials which have low dielectric constants were prepared. Polyphenylsilsesquioxane(PPSQOH) with hydroxyl end groups was synthesized by following the existing method. Hydroxyl-functionalized polystyrene(PSOH) and hydroxyl-functionalized poly lactic acid (PLOH) were also prepared by anionic and bulk polymerization. PSPPSQ series at various composition ratios and molecular weights were obtained using reaction between PPSQOH and PSOH. PLPPSQ series at various composition ratios and molecular weights were also obtained from reaction between PPSQOH and PLOH. These hybrid materials were characterized by 1H-NMR and FT-IR. The thermal decomposition behavior of hybrid materials was examined by thermogravimetric analysis(TGA). Their surface morphology was investigated by transmission electron microscope(TEM). The results from the TEM micrographs exhibits the existence of highly porous structures and the pores size ranged below 5 nm are regularly dispersed. These hybrid materials would be useful for various applications to better electric and optical device.

F3.5

Characterization and preparation of porous low dielectric films that use various molecular weight (M.W) and polydispersity (PD) of silsesquioxane (SSQ). Rhee Ji-hoon[1], Kim Taewan[1], Lee Kwang-Hee[2], Koo Ja ho[1] and Jeong Hyun-Dam[2]; [1]R & D Center, Samsung Corning Corp. Ltd, suwon, South Korea; [2]Electronic Materials Lab, Samsung Advanced Institiue of Technology (SAIT), suwon, South Korea.

The industry has been strongly interested in integrating porous low dielectric constant materials to meet new technical demands of future LSI device. Porous low dielectric films are strong candidates among those, which were formed from new silsesquioxane (SSQ) polymer by the addition of a sacrificial material to the SSQ. The electrical property of the porous low dielectric films was significantly affected by molecular weight (M.W) and polydispersity (PD) of SSQ. In this study, we have characterized the network structure of the thin films and molecular weight (M.W) and polydispersity (PD) of SSQ by means of Gel permeation chromatography (GPC) and Particle counter and dynamic layer spectrometry (DLS) and Transmission Electron Microscopy (TEM), and residual hydroxyl group of thin films using FT-IR. In addition, we monitored the electrical properties and mechanical properties of the porous thin films in order to know the potential as a low-k material. We found that the mechanical properties of porous low-k thin film prepared with polydispersity (PD) of SSQ and molecular weight(M.W) was correlated to density of the thin film. Network structure and density in the thin film strongly depend on molecular weight (M.W) as well as polydispersity (PD) of SSQ. These results indicated that the lower molecular weight (M.W) and polydispersity (PD) of silsesquioxane (SSQ) in the thin film was increased slightly the mechanical properties of the thin film such as hardness and modulus.

F3.6

New hybrid low-k dielectric materials prepared by vinylsilane polymerization. Jung-Won Kang, Byung-Ro Kim, Gwi-Gwon Kang, Myung-Sun Moon, Bum-Gyu Choi and Min-Jin Ko; Corporate R&D, LG Chem, Ltd., Daejeon, South Korea.

Spin-on Low-K materials are potentially very attractive as interconnection materials in a wide range of semiconductor structures. A large variety of polymers has been proposed for use as low-k materials with low dielectric constants for applications in microelectronics. Inorganic polymers such as silsesquioxane are more like SiO2 than other polymeric dielectrics. They have perceived advantages for higher Tg, hardness and adhesion to polar surfaces. However, the main disadvantage for these inorganic polymers is that they are also brittle. This makes them susceptible to damage during CMP. Organic polymers, especially aromatic carbon with thermal stability, have higher toughness yielding crack free film. But they show somewhat high CTE and low mechanical strengths (hardness, adhesion). In this work, we have prepared new organic-inorganic hybrid low-K dielectrics by vinylsilane polymerization. The dielectric constants of these materials were evaluated to be 2.3 3.1, which depend on these composition and additional fabrication. The hardness was 2.0GPa after 430oC curing. These materials also show very high toughness and good adhesion properties. The fracture toughness of these thin film was 0.22 Mpa*m1/2 without adhesion promoters. This result indicates that these organic-inorganic hybrid materials are very promising polymers for low-K dielectrics that have low dielectric constants with high thermal and mechanical properties.

F3.7

Inter-pore interactions in highly porous ultra low-k films. Nobuhiro Hata[1,2], Peter Kluvanek[2], Nobutoshi Fujii[3], Hirofumi Tanaka[3], Chie Negoro[2], Kazuhiro Yamada[3] and Takamaro Kikkawa[4,1]; [1]MIRAI-ASRC, AIST, Tsukuba, Ibaraki, Japan; [2]ASRC, AIST, Tsukuba, Ibaraki, Japan; [3]MIRAI-ASET, Tsukuba, Ibaraki, Japan; [4]RCNS, Hiroshima Univsersity, Higashi-Hiroshima, Hiroshima, Japan.

Catastrophic deterioration of electrical, chemical and mechanical stabilities of porous low-k films, which occurs when the porosity exceeds a critical porosity Xc of about 35 %, is known as one of the biggest issues in development of ultra low-k materials. We hypothesized that the deterioration is caused by strong inter-pore interactions such as random coagulation of pores, perforation path formation, and formation of large voids. We took advantages of the three different pore characterization techniques of in-situ spectroscopic ellipsometry in a home-made quartz optical cell for heptane or toluene vapor sorption at room temperature, volumetric argon or nitrogen physisorption analyses at cryogenic temperature, and thin film X-ray analyses based on small angle X-ray scattering technique, to investigate pore structures in silica-based highly porous (above Xc) low-k films. The ultra low-k films were prepared by spin coating of precursor solutions of sacrificial surfactant templated sol-gel synthesis.

The results from X-ray scattering and total adsorbed amount evidenced successful control of pore size and porosity, respectively, by the selection of the template molecule and its concentration. The pore-size controllability was confirmed also by sorption isotherm analyses based on Brunauer-Emmett-Teller theory and Kelvin equation. Coherence of X-ray was utilized to examine the existence of ordered structures. The in-situ ellipsometry spectra were analyzed with the optical model of low-k films on c-Si substrate to obtain vapor pressure dependencies of the film thicknesses and refractive indices, which were then used to calculate the adsorbed vapor amounts, or adsorption / desorption isotherms. Not only the refractive index but also the film thickness changed with the vapor sorption, because the film shrinkage by the adsorbate surface tension varied with the meniscus curvature or the vapor pressure. In the strong inter-pore interaction regime, the simple assumption of mutually independent pores with simple identical shapes such as sphere or cylinder, which is frequently used for lower porosity low-k film analyses, was shown to be incorrect. The observed hysteresis loops in adsorption / desorption isotherms were analyzed to clarify the meta-stable adsorption states due to the existence of necks in adsorptive perforation paths. Also the slopes of sorption isotherms at high partial pressure region and of X-ray scattering spectra in low scattering angle region were analyzed to reveal large voids. From these results it has been demonstrated that not only high porosity periodic porous silica films but also disordered porous silica films can be made free from random pore coagulations, long random perforation paths, and large voids. It has been shown that careful control through preparation conditions of pore structures in highly porous low-k films is a key for realizing highly stable ultra low-k films for future low-k / Cu interconnects.

F3.8

The preparation of mechanically strong order mesoporous silica ultra-low-k film using low temperature and fast ozone ashing dry technology. A. T. Cho and F. M. Pan; National Nano Device Laboratories, Hsinchu, Taiwan.

Ozone ashing dry technology has been applied in the formation of a mesoporous silica ultra-low-k film with an ordered pore structure, uniform pore size distribution, well electrical reliability of k 2.0 and strong mechanical strength. The ozone ashing process was used to remove the organic templates efficiently and rapidly at low temperature to form the mesoporous silica low-k film with an order nm-scale pore structure. Which possesses higher mechanical properties than that formed through traditional thermal calcination. To meet requirements of 70 nm node technology, materials of dielectric constant value k 2 have been required. In order to satisfy this requirement, incorporation of nm-scaled pores into the dielectric materials was proposed, however, the porous materials have been facing trade-off in the dielectric constant and mechanical properties. Incorporation of more pores in the dielectric film to decrease the dielectric constant will degrade mechanical properties, such as Young's Modulus and hardness. It is supposed that low-k materials with a low mechanical strength are difficulties to endure during integrating cycles such as CMP, dry etching, and packaging processes. Recently mesoporous ultra-low-k silica dielectric prepared by self-assemble templating synthesis was developed and demonstrated of better mechanical properties than other nano-porous films. The mesoporous low-k films need calcinations at a temperature higher than 4000C to remove the templates. It is reported that the Cu/low-k interconnect integration has some integration problems of the thermal copper diffusion and agglomeration of narrow Cu interconnect at high temperature. So, the processing temperatures after Cu interconnect formation might be kept lower. In this paper, we reported the application of a novel low temperature ozone ashing treatment in the formation of an ordered mesoporous silica ultra-low-k film. The ozone ash was used to remove organic templates and to form nm-scale ordered pore structure in the mesoporous silica film at low temperatures. The results showed that the ozone treatment leads to a narrow pore size distribution with high mechanical strength compared to thermal calcination. Therefore, the novel ozone treated dry techniques results in improved mechanical properties of ultra-low-k mesoporous silica films, such as increased Young's modulus and film hardness with well electrical reliability, as well as in dramatically reduced process time and process temperature.

F3.9

Pulse plasma enhanced atomic layer deposition of WC_xN_y diffusion barrier for copper interconnect. Hyun Sang Sim, Ji-Ho Park, Seong-Il Kim and Yong Tae Kim; Semiconductor Materials and Devices Lab., Korea Institute of Science and Technology, Seoul, South Korea.

We have deposited the W-C-N thin films on oxide layer with pulse plasma enhanced atomic layer deposition (PPALD) method by using WF_6, CH_4 and NH_3. WF_6 gas was introduced for 0.2 1 s and then purged with N_2 gas. After that, CH_4 gas was introduced for 0.2 3 s and purged with N_2 gas and WF_6 gas was exposed again and purged. Finally, NH_3 gas was also introduced for 0.2 3 s and purged with N_2 gas. During a cycle of ALD process, pulse plasma was applied for the exposure cycles of CH_4 and NH_3 gas. The pulse plasma power was 8 kV of peak-to-peak voltage. The substrate temperature was 300 to 400 °C. The W-C-N film was deposited with the rate of 2.0 Å/cycle at 350 °C. Stoichiometric ratio of W-C-N film was determined by Rutherford backscattering (RBS) and Auger electron spectroscopy (AES). During the PPALD processes, the N and C concentration is uniformly distributed in the W-C-N film. The growth rate and the stoichiometry were not changed with each cycle time. The interface between W-C-N film and Si was observed by high resoultion transmission electron microscopy (HR-TEM). In order to investigate the performance of PPALD grown W-C-N thin films (thickness is 22 nm) as a diffusion barrier against Cu diffusion, 200 nm thick Cu film was deposited on the W-C-N/TEOS/Si structure. The Cu/W-C-N/TEOS/Si structures were annealed at 500 700 °C for 30 min in N_2 ambient. After the annealing processes, the samples were analyzed with RBS, HR-TEM, C-V, I-V measurements to determine whether the Cu diffusion occurrs or not through the W-C-N diffusion barrier. As a diffusion barrier for the Cu interconnect, experimental results reveal that 22 nm thick W-C-N successfully prevents the Cu diffusion after the annealing at 700 °C for 30 min.

F3.10

Structural and functional characterization of W-Si-N sputtered thin films for copper metallizations.
alberto vomiero[1,2], Stefano Frabboni[3], Enrico Boscolo Marchi[4,2], Matteo Ferroni[5], Alberto Quaranta[6,2], Rita Tonini[3], Gianantonio Della Mea[6,2], Gino Mariotto[4], Giampiero Ottaviani[3], Stefano Polizzi[5] and Alvise Benedetti[5]; [1]Dept. of Physics, Univesity of Padova, Padova, Italy; [2]INFN Laboratori Nazionali di Legnaro, Legnaro (PD), Italy; [3]Dept. of Physics, Univesity of Modena, Modena, Italy; [4]Dept. of Physics, Univesity of Trento, Trento, Italy; [5]Dept. of Chemical Physics, Univesity of Venice, Venice, Italy; [6]Dept. of Materials Engineering and Industrial Technologies, Univesity of Trento, Trento, Italy.

In the framework of the development of new materials to be applied as ultrathin diffusion barriers for Cu interconnected structures in microelectronics, ternary W-Si-N thin layers (200 nm thick) are produced by RF magnetron sputtering, starting from a W5Si3 target. The aim of this work is to add information about a ternary system, which is less studied with respect to other one, such as Ti-Si-N. Nitrogen incorporation is obtained by inserting N2 gas in the inert Ar plasma atmosphere, giving rise to a reactive sputtering process. The structural as well as the functional properties of the layers are characterized before and after annealing, in order to investigate the effects of heating on the stability of the deposited films. Heat treatments are performed in vacuum in the range 600 - 1000 C. The stoichiometric composition is measured by the means of Rutherford Backscattering (RBS) and Elastic Recoil Detection Analysis (ERDA). The growing N2 flux results in an N enriched film, with a maximum N atomic concentration of 57%. Film density is obtained by combining RBS results with the measured films thickness. Preliminary results indicate that the higher is N concentration, the denser film is growing. Intense preferential Si resputtering is detected in the layers with low N, resulting in a high Si understoichiometry in the Si:W atomic ratio in the film with respect to the target composition. Fourier Transform Infrared Spectroscopy (FT-IR) is applied to detect the formation of Si-N bonds similar to the bond in Si3N4. The increase in the number of Si-N bonds with the increasing N is detected. The presence of N can give explanation of the reduced Si resputtering in the N rich layers. Surface morphology is investigated via Atomic Force Microscopy (AFM), in order to obtain information about surface roughness and its evolution during annealing. Transmission Electron Microscopy (TEM) and X-Ray Diffraction (XRD) are applied in the characterization of the microcrystalline structure of the films for the as grown as well as for the annealed layers. A nearly amorphous structure for all the untreated samples appears, regardless for the composition. TEM on annealed films allows the determination of the crystallization temperature and its dependence on the stoichiometric composition of the films. Film resistivity is measured by the means of a four-point probe method before and after annealing. Dynamic measurements are also performed, by monitoring film conductivity in situ during annealing, in order to investigate changes in the electrical behaviour, related to the structural modification of the layers.

F3.11

Diffusion Barrier Properties of Nano-crystalline ZrCN films in Cu/Si Systems. Chen Cheng-Shi[1,2,3], Liu Chuan-Pu[1,2,3] and Tsao Chi Y.A.[1,2,3]; [1]National Cheng-Kung University, Tainan, Taiwan; [2]National Cheng-Kung University, Tainan, Taiwan; [3]National Cheng-Kung University, Tainan, Taiwan.

ZrN has a lower negative formation energy and a lower resistivity than TaN. Therefore, ZrN system could be a good candidate for the diffusion barrier in IC technology, In this paper, the proposed novel

zirconium carbon nitrides (ZrCN) layers were deposited by reactive sputtering ZrC target (50:50 wt% and 99.5% in purity) in a mixture of Ar and N2 ambient. The physical and electrical properties of the Zr-C-N films were examined with respected to the N2 content. The barrier properties of Zr-C-N films were evaluated and compared to the cases of Zr-C and Zr-N films. For thermal stability analysis, the prepared samples were subsequently subjected to thermaltreatment at temperatures in the range of 300 900 C in a vacuum tube with the base pressure of 3x10E-5torr. Possible chemical reactions and Cu diffusion inside the annealed Cu/barrier/Si contact systems due to thermal annealing were examinedd by using four-point probe for sheet resistance neasurement, scanning electron microscopy (SEM) for suface morphology investigation, X-ray diffraction (XRD) technique for phases of possible reaction products identification, and the interdiffusion of each species upon annealing is studied by Auger electron spectroscopy (AES). Finally, the possible mechanism governing for the failure of the present barrier after high temperature annealing was discussed.

F3.12

Barrier layer morphological stability and adhesion to porous low-k dielectrics. Ravi Saxena, Woojin Cho, Oscar Rodriguez, William N. Gill and Joel L. Plawsky; Chemical Engineering, Rensselaer Polytechnic Institute, Troy, New York.

Two particularly important reliability issues facing the integration of low-k dielectric films are the fracture energy of the barrier-dielectric interface and the barrier layer integrity during processing. The effect of dielectric porosity and pore size distribution on the physical properties of contiguous copper barrier layers has not been studied. We have noticed that the compressive stresses in the barrier layers lead to spontaneous delamination and formation of telephone-cord like morphologies. These morphologies allow the measurement of fracture energy and are advantageous over artificially contrived features to yield realistic debonding parameters. The fracture energy of two barrier films, TaN and Ta, was determined using this method for varying porosity nanoporous silica. Detailed surface area characterization was done for the substrates using two complementary techniques of AFM (Atomic force Microscope) and EP (Ellipsometric Porosimetry). The dielectric properties i.e. pore size and chemistry, were varied and their effect on fracture energy was determined. Strong correlation was found in the dielectric chemistry, available surface area, porosity and the fracture energy. The mechanisms of such a correlation will also be discussed.

F3.13

The Growth of Tantalum Nitride by Atomic Layer Deposition on Organosilicate and Organic Polymer-Based Low Dielectric Constant Materials. Oscar van der Straten, Yu Zhu, Kathleen Dunn and Alain Kaloyeros; UAlbany Institute for Materials, University at Albany - SUNY, Albany, New York.

A previously developed metal-organic atomic layer deposition (ALD) tantalum nitride (TaN_x) process was employed to investigate the growth of TaN_x liners on low dielectric constant (low-k) materials for liner applications in advanced Cu/low-k interconnect metallization schemes. ALD of TaN_x was performed at a substrate temperature of 250°C by alternately exposing low-k materials to tertbutylimido-tris(diethylamido)tantalum (TBTDET) and ammonia (NH_3), separated by argon purge steps. The dependence of TaN_x film thickness on the number of ALD cycles performed on both organosilicate and organic polymer-based low-k materials was determined and compared to baseline growth characteristics of ALD TaN_x on SiO_2. In order to address the effect of the deposition of TaN_x on surface roughness, atomic force microscopy (AFM) measurements were carried out prior to and after the deposition of TaN_x on the low-k materials. The stability of the interface between TaN_x and the low-k materials after an applied thermal budget was studied by examining interfacial roughness profiles using cross-sectional imaging in a high-resolution transmission electron microscope (HR-TEM). The wetting and adhesion properties of Cu/low-k were quantified using a solid-state wetting experimental methodology after integration of ALD TaN_x liners with Cu and low-k dielectrics.

F3.14

Atomic Layer Deposition of Tantalum Nitride Thin Films for Copper Metallization Applications. Wanxue Zeng, Degang Cheng, Yu Zhu, Eric Eisenbraun and Alain E. Kaloyeros; UAlbany Institute for Materials, Albany, New York.

Atomic layer deposition (ALD) has been regarded as a highly promising thin film deposition technique for growing copper diffusion barrier/seed layers [1] particularly in 45 nm technology node and below [2], due to its excellent step coverage and precise control of ultrathin barrier layer thickness. In this work, a low temperature ALD process has been developed for the growth of ultra thin TaN_x films with the use of $TaCl_5$ as Ta-containing precursor and NH_3 as co-reactant gas in a 200-mm wafer platform. An optimized process was identified by performing a systematic study of the film growth rate as function of $TaCl_5$ pulse time, NH_3 pulse time, and Argon purge time. The properties of the TaN_x films deposited via the optimized process conditions were studied using Rutherford back-scattering spectrometry (RBS), scanning electron microscopy (SEM) and cross-sectional SEM (CS-SEM), transmission electron microscopy (TEM), x-ray diffraction (XRD), atomic force microscopy (AFM), Auger electron spectroscopy (AES), and nuclear reaction analysis (NRA). It was found that the as-deposited TaN_x films had a Ta/N ratio of 3/5, excellent step coverage, an orthorhombic microstructure, and low oxygen, hydrogen and chlorine contamination levels. The preliminary copper diffusion barrier performance as investigated by RBS shows that a 2 nm-thick TaN_x film could prevent copper from diffusing into silicon substrate up to 500 °C for 1 hour. Reference: 1. J. Park, M. Lee, C. Lee, and S. Kang, Electrochemical and Solid-State Letters, 4 (4), C17 (2001) 2. A. Hand, Semiconductor International, May (2003)

F3.15

The Initial Growth of Tantalum Carbon Nitride Films by Plasma Enhanced Atomic Layer Deposition (PEALD). Degang Cheng, Alvin Grant and Eric T. Eisenbraun; School of NanoSciences and NanoEngineering, University at Albany, SUNY, Albany, New York.

Tantalum carbon nitride, Ta(C)N, films are of potential interest in copper barrier and front-end electrode applications owing to their low resistivity, robust diffusion barrier properties, and excellent thermal stability. Key aspects of such materials are the initial growth and nucleation characteristics, as these will play a significant role in their ultimate performance. To study this, Ta(C)N films were deposited by a plasma-enhanced atomic layer deposition (PEALD) process employing terbutylimido tris(diethylamido) tantalum (TBTDET) as precursor and a hydrogen plasma as the reducing agent at a temperature of 250°C. The deposited films demonstrate promising diffusion barrier properties for copper metallization at thicknesses as small as 1nm. Initial growth was investigated by varying the number of deposition cycles, yielding films ranging from 0.4nm to 10nm thick. The resultant films were analyzed by atomic force microscopy, Rutherford backscattering spectrometry, and transmission electron microscopy. Nanostructural characteristics are discussed, and a mechanism is proposed for the observed diffusion barrier behavior.

F3.16

Effect of Annealing on The Structural, Mechanical and Tribological Properties of Electroplated Cu Thin Films. Pallavi Shukla[1,2], Parshuram Balkrishna Zantye[1,2], Arun Sikder[2], Ashok Kumar[1,2] and Mahesh Sanganeria[3]; [1]Department of Mechanical Engineering, University of South Florida, Tampa, Florida; [2]Nanomaterials and Nanomanufacturing Research Center, University of South Florida, Tampa, Florida; [3]Novellus Inc., San Jose, California.

The increasing demand for faster and more reliable integrated circuits (ICs) has promoted the integration of Copper-based metallization. Electroplated Cu films demonstrate a microstructural transition at room temperature, known as self annealing. In this paper we intend to investigate the annealing behavior of electroplated Cu films grown on a seed Cu layer on top of the barrier layers over a single crystal silicon substrate. All the samples were undergone through a multistep annealing process. Grazing incident x-ray diffraction pattern shows stronger x-ray reflections form Cu (111) and (220) planes but weaker reflections from (200), (311) and (222) planes in all the electroplated Cu samples. Transmission electron microscopy was performed on the cross section of the samples and the diffraction pattern showed the crystalline behavior of both seed layer and electroplated Cu. Nanoindentation was performed on all the samples using the continuous stiffness measurement (CSM) technique and it was found that the elastic modulus varies from 110 to 130 GPa while the hardness varies from 1 to 1.6 GPa depending on the annealing conditions. The tribological properties of all the copper films were also measured using the Bench Top CMP tester. Subsequently, Nanoindentation was performed on the samples after polishing the top surface in order to investigate the work hardening and an increase in hardness and modulus was observed. The surface morphology and roughness of Cu films before and after polishing were characterized using Atomic Force Microscopy. Finite Element Modeling is to be performed in order to investigate the stress behavior during nanoindentation.

F3.17

Copper Metallization in High Aspect Ratio Trenches Using Filtered Vacuum Arc Deposition. Yong Ju Lee and Othon Monteiro; Lawrence Berkeley National Laboratory, Berkeley, California.

With decreasing feature size and increasing complexity of the metal

wiring in microelectronics, the signal delay introduced due to the increasing resistance of the longer metal lines became critical. It exceeds the gate delay itself for feature sized smaller than 250 nm. Copper (Cu) is posed to take over as the main on-chip conductor for all types of integrated circuits to decrease the resistance compared with aluminum and tungsten. We introduce the filtered cathodic vacuum arc (FCVA) technique for the deposition of Cu capable of filling trenches with lateral dimensions of 150 nm and high aspect ratios. The method uses a filtered cathodic arc plasma source with tighty ion energy control. With the FCVA technique, the plasma stream is steered through a magnetic filter to eliminate neutral particles generated at the cathode. By applying a variable bias to the substrate, the energy of ions impinging the substrate can be controlled in the range from tens to hundreds of electron volts. 100-nm-wide trenches with the aspect ratio of 8:1 were effectively filled by the Cu ions. The thickness of the copper film on the horizontal surface of the wafer is significantly smaller than the depth of the trenches, suggesting that filling is accomplished at least in part with material sputtered from or reflected by the film on the trench wall.

F3.18

Thermal Conductivity of Carbon Nanotube Composite Films.

Quoc X. Ngo[1], Brett A. Cruden[2], Alan M. Cassell[2], Qi Ye[2], Jun Li[2], Megan D. Walker[2], Jessica Koehne[2], M. Meyyappan[2] and Cary Y. Yang[1]; [1]Center for Nanostructures, Santa Clara University, Santa Clara, California; [2]Center for Nanotechnology, NASA Ames Research Center, Moffett Field, California.

Carbon nanotubes (CNT) possess exceptional thermal properties such as high heat-carrying capacity. Developing new materials that can disperse heat has long been a challenge in space exploration. Exploiting CNT films for their superior thermal conductance properties has the potential for such applications that require efficient heat transfer. Another potential application includes using CNT films as heat sinks for ultra-large-scale integration (ULSI) of microelectronic circuits, where power density is a critical reliability metric. State-of-the-art integrated circuits (IC) for microprocessors routinely dissipate power densities on the order of 50 W/cm^2. This large power is due to the localized heating of ICs operating at high frequencies, and must be properly controlled for future high-frequency microelectronic applications. In this work, we present fundamental thermal conductivity measurements of CNT composite films. CNTs grown using the plasma-enhanced chemical vapor deposition (PECVD) process [1] have been optimized for dense vertical arrays of nanotubes. These as-grown nanotubes can be estimated as having 10-20 percent packing density, providing relatively small surface area for thermal conductance through the nanotubes. Clearly, the remaining 80-90 percent of the sample is essentially filled with air, a poor thermal conductor ($k=2.5\times10^{-4}$ W/cm.K). By filling these gaps with a material exhibiting more efficient heat-carrying properties, we can maximize thermal conductivity of the CNT composite film. To characterize the conduction capability of these materials, we used the methodology applied to diamond-like carbon films by Goodson, et al. [2]. In this approach, a thin platinum microwire is deposited on the sample and used to induce localized Joule-heating on with transient voltage pulses. A Wheatstone bridge circuit is employed to measure resistance changes in the microwire, through which transient temperature response is calculated and thermal conductivity is inferred. Additional calculations are performed to account for lateral heat conduction through the film. A variety of CNT composite films with different gap-fill materials have been investigated for efficient heat transfer. The characterization results will be presented comparing the merits and drawbacks of all test structures. [1] B.A. Cruden, A.M. Cassell, Q. Ye, and M. Meyyappan, J. Appl. Phys., 94, 4070 (2003). [2] K.E. Goodson, O.W. Kading, M. Rosler, and R. Zachal, J. Appl. Phys., 77, 1385 (1995).

F3.19

Silver Patterning by Ecr-Ribe for Advanced Interconnects.

Liming Gao, Juergen Gstoettner, Rainer Emling, Pengfei Wang, Walter Hansch and Doris Schmitt-Landsiedel; Technical University Munich, Institute for Technical Electronics, Munich, Germany.

As devices continuously shrink in ultra large-scale integration (ULSI), the RC delay of the interconnection system becomes one of the most critical limitations on IC performance. Silver, with a lower bulk resistivity than that of copper and also a potentially lower surface scattering property, is being codsidered by many as the next metallization of choice. Ag has also received attentions as a potential interconnection in the large area TFT/LCDs because of its lowest resistivity and high electromigration resistance. It has been shown that a sputtered Ag metallization is possibly more suitable for ULSI than sputtered Cu due to a much higher electrical conductivity in features sizes below 100 nm. To evaluate the potential application of silver metallization in industry, one of the important aspects is the pattern transfer by etch processing. Dry etching of silver for the metallization in microelectronics is investigated. Etching is performed using an electron-cyclotron-resonance reactive-ion-beam-etching system (ECR-RIBE) in an Ar/CF4 or Ar/CF4/O2 mixture. The etch characteristics are strongly affected by ion energy (beam voltage and microwave energy). By changing the beam voltage from 250 V to 600 V, there is an increase in etch rate from 3.3 nm/min to 112.6 nm/min. The O2 concentration in the reactive mixture has only a small effect on the etching speed. However, the root-mean-square (RMS) roughness at 500 V beam voltage with only CF4 reactive gas is less than that of 500 V beam voltage with reactive gas CF4 and O2 (9:1), and also the surface after etching is clearer after etching without oxygen.An anisotropic, smooth etch profile and clean surface are obtained. Focused ion beam (FIB) and atomic force microscopy (AFM) have been used to study the etched profile and the roughness, respectively.

F3.20

Free-standing line patterns of nanocrystalline electrodeposits.

Karen Pantleon[1], Marcel A.J. Somers[1], Henrik M. Jensen[2] and Andy Horsewell[1]; [1]IPL - Dept. of Manufacturing Engineering and Management, Technical University of Denmark, Lyngby, Denmark; [2]MEK - Dept. of Mechanical Engineering, Technical University of Denmark, Lyngby, Denmark.

Electrochemical deposition has become the key technology in manufacturing functional thin films with finite structures, e.g. for microsystems and microcomponents. The two most popular materials in that field are copper, which has become the dominant material for interconnects in integrated circuits in microelectronics, and nickel, a promising material to realize movable structures for micro-electro-mechanical systems (MEMS). Finite metal structures with very small dimensions in the micrometer- or even nanometer range are either inlaid in trenches of an insulator (like Cu-damascene lines) or they form free-standing patterns on a substrate (like so-called LIGA-structures). The functionality and reliability of such films depend on their microstructure - however, the thermodynamically non-equilibrium state of as-deposited films may cause substantial changes of the microstructure and related properties with time at room temperature and/or elevated (operating) temperatures. Free-standing discontinuous Cu- and Ni-line patterns were manufactured by combining photo-lithography and electrochemical deposition. Several pattern geometries varying in line width and interline distance in the range of a few micrometers were deposited onto two different seed-layers (substrates): a polycrystalline Au-layer and an X-ray amorphous Ni-P layer. For comparison with the line patterns also continuous non-patterned Cu- and Ni-films were deposited with identical deposition parameters and used as reference. X-ray diffraction (XRD) averaging over hundreds of identical lines was applied to study the effect of both the substrate and the pattern geometry on the developing microstructure of the line patterns. Comprehensive XRD studies of crystallographic texture, including calculations of the orientation distribution function for texture quantification, and lattice strain measurements were performed for several line patterns and continuous films. XRD studies were accompanied by investigations of the morphology and topography of the deposits by means of light optical and electron microscopy. For Cu-line patterns, finite element modeling (FEM) of strain distributions within individual free-standing lines was carried out. FEM-results were used to simulate X-ray diffraction peak profiles, which were compared to experimental results.

F3.21

Pulsed CVD of Cu seed layer using a (hfac)Cu(3,3-dimethyl-1-butene) source plus H2 reactant.

JaeBum Park and JaeGab Lee; A School Of Advanced Materials Engineering, Kookmin University, seoul, South Korea.

For electroplating Cu, thin seed layer of cu has been successfully deposited over 0.1 um wide trenches with a high aspect of 22 by pulsed CVD of Cu using a organometallic Cu(I) source, DMB and H2 reactant gas. Prior to pulsed CVD of Cu, about 20 nm of MOCVD TiN was deposited using TDMAT at 300C over the deep submicron trenches, which acted as a glue adhesion layer for Cu metallization. After deposition of MOCVD TiN, the resultant trench profiles show 50 nm wide trench with aspect ratio over 40:1. The growth proceeds by exposing the MOCVD TiN coated trenches alternately to the Cu precursors and the following Ar pulse, and H2 pulse. The typical deposition cycle consisted of 3sec DMB pulse, 6sec Ar purge, and 3sec H2 pulse step at the substrate temperature of 50 to 250C and the pressure of 0.4 torr. Compared with ALD Cu using a organometallic Cu(II) source, pulsed CVD using a Cu(I) precursor can provide a significantly lower deposition temperature for nucleation and growth, and thus resulting in much improved surface morphology. AFM analysis reveals the root mean square of the surface roughness ranging from 5 to 9 nm and the four point probe measuring the resistivity of 4.2 to 1.8 uohm-cm, depending on the thickness of Cu. In addition, the growth rate of pulsed Cu shows a weak function of substrate temperature. The addition of H2 pulse step remarkably reduces the

growth rate of Cu and carbon contamination as well. Further, the added H2 pulse decreases a sticking probability, and thus leading to excellent conformal deposition of Cu over high aspect ratio trenches. The Cu films were found to be highly conformal, with uniform step coverage in trenches with aspect ratio over 40:1. These films can be suitable as a seed layer for the electroplating of Cu in an advanced device.

F3.22
Effects of ion irradiation on anisotropic plasma chemical vapor deposition of Cu. Kosuke Takenaka, Manabu Takeshita, Kazunori Koga, Masaharu Shiratani and Yukio Watanabe; Dept. of Electronics, Kyushu University, Fukuoka, Japan.

We have proposed an anisotropic plasma chemical vapor deposition method by which Cu is filled preferentially from bottom of a trench without sidewall deposition.[1,2] We have studied the deposition and sputtering rates on top surface, bottom surface, and sidewall of a trench as a parameter of flow rate ratio $R = H_2/(H_2+Ar)$. The deposition rates on the top and bottom surfaces tend to decrease with increasing R and eventually they become zero for $R > 83\%$, whereas no deposition on the sidewall takes place for $R > 11\%$. On the other hand, the sputtering rates on the top and bottom surfaces decrease slightly with increasing R, whereas no sputtering on the sidewall takes place. These results indicate that the ion irradiation is the key to the anisotropic deposition and is not appreciable on the sidewall. We have identified ionic species irradiating on the substrate surface with a quadrupole mass-spectrometer. The dominant light and heavy ionic species in the discharge are H_3^+ and ArH^+. Signal intensities of H^+, H_2^+ and H_3^+ increase by one order of magnitude with increasing R from 11 to 83%, while those of Ar^+ and ArH^+ are nearly constant in the same range. Roles of these ions on the anisotropic deposition will be discussed in the presentation. [1]K. Takenaka, et al., Mater. Sci. Semicon. Processing. **5**, 301 (2003). [2]K. Takenaka, et al., Mater. Res. Soc. Symp. Proc. **766**, E3.8.1 (2003).

F3.23
Preparation and Characterization of Copper Film on Plastic Substrate by ECR-MOCVD Coupled With a DC Bias.
Joong-Kee Lee, Bupju Jeon and Byung Won Cho; Eco-Nano Research Center, Korea Institute of Science and Technology, Seoul, South Korea.

Metallized polymers are very interesting materials for microelectronic packaging of flexible PCB and COF (chip on film), flexible solar cell, gas barrier and EMI (electromagnetic interference) shielding purpose. However, a lot of plastics can be hardly coated with well-adhering layers without pretreatment due to lack of nucleation sites. Conventional methods for metallization of polymer are electrochemical plating and physical vapor deposition (PVD) such as thermal evaporation and magnetron sputtering. Wet chemistry processes, however, have some inherent problems such as complex procedures and environmental pollution. For the PVD, it is technically difficult to maintain metal film on the polymer substrate due to poor adhesion, substrate deformation and an aging effect. CVD processes for the preparation of copper films are of considerable interest since continuous deposition of large areas can be easily achieved with good film characteristics. However, most established metal organic chemical vapor deposition techniques for the preparation of copper film are based on thermal CVD procedures. Operating temperatures in the range of 150 to 200°C have to be used to prepare copper thin films by PECVD. Therefore, the deposition of thin copper film on polymer substrates by the MOCVD method at room temperature has not been tried. Recently, there has been great interest in using MOCVD at ambient temperature in order to produce metallized polymer. Chemical vapor deposition at ambient temperature using organometallic precursors should be possible with the aid of a DC bias. The aim of this work was to test the ECR-MOCVD method for deposition at room temperature and characterize the films prepared thereby. We also report the results of experiments designed to investigate the deposition of copper and carbon containing hybrid thin films from $Cu(hfac)_2$ as a copper precursor in an Ar-H_2 atmosphere by using ECR microwave plasma coupled with a DC bias. The structural and chemical analyses of the Cu/C films were carried out and their electrical resistances were determined as a function of H_2/Ar mole ratio, microwave power, periodic negative voltage and the magnet current.

F3.24
Thermal stability and electrical properties of Ag(Al) metallization. H. C. Kim[1], N. D. Theodore[2], J. W. Mayer[1] and T. L. Alford[1]; [1]Chemical and Materials Engineering, Arizona State University, Tempe, Arizona; [2]Digital DNA Labs., Motorola Inc., Tempe, Arizona.

The thermal stability and electrical resistivity of Ag(Al) alloy thin films on SiO_2 are investigated and compared to pure Ag thin films by performing various analyses: Rutherford backscattering spectrometry, X-ray diffractometry, optical microscopy, and four-point probe measurements. The susceptibility to agglomeration of Ag on SiO_2 layer is a drawback of Ag metallization. Ag(Al) thin films show good thermal stability on SiO_2 layers without any diffusion barrier. The films are stable up to 600 °C for 1 hour in vacuum. Electrical resistivity of as-deposited Ag (5 at % Al) thin film is slightly higher than that of pure Ag thin film. However, the resistivity of Ag(Al) samples annealed at high temperatures (up to 600 °C for 1 hour in vacuum) remains constant due to the improvement of thermal stability (significant reduction of agglomeration). This finding can impact metallization of thin film transistors (TFT) for displays, including flexible displays, and high-speed electronics due to the lower resistivity value of Ag compared to Cu thin films.

F3.25
Morphology of $Ti_{37}Al_{63}$ Thin-Films Deposited by Magnetron Sputtering. N. D. Theodore[1], H. C. Kim.[2], K. S. Gadre[3], J. W. Mayer[2] and T. L. Alford[2]; [1]Digital DNA Lab., Motorola Inc., Tempe, Arizona; [2]Chemical and Materials Engineering, Arizona State University, Tempe, Arizona; [3]Intel Inc., Hillsboro, Oregon.

TiAl based thin-films possess high oxidation-resistance and high melting points, making them possible candidates for application in high-temperature electronics. The behavior of the films upon exposure to various temperatures is of interest for such application. In the present study, $Ti_{37}Al_{63}$ thin films were deposited onto SiO_2 substrates using RF magnetron sputtering from a compound target. Anneals were performed in vacuum at temperatures ranging from 400 °C to 700 °C. The phases and microstructural behavior of the films were evaluated as a function of annealing. Microstructural behavior was correlated with resistivity changes in the films. The results are relevant for potential application of the films to electronics.

F3.26
Cu Electroless Deposition of Atomic Layer Deposited Pd Passivated TaN Barrier Layers. Young-soon Kim[1], G.A. Ten Eyck[1], D Ye[1], D. Liu[1], T. Karabacak[1], G. -C. Wang[1], H. S. Shin[2], J. J. Senkevich[1] and T. -M Lu[1]; [1]Physics, Rensselaer Polytechnic Institute, Troy, New York; [2]Department of Chemical Engineering, Chonbuk National University, Chonju, chollabuk-do, South Korea.

Because of the gap filling capability, many researchers have studied Cu electrochemical plating and electroless plating. Electroless deposition (ELD) of Cu already used in electronic packaging, and in the fabrication of Cu on-chip interconnects to fill features. Cu ELD typically requires a catalytic surface to oxidize the reducing agent. Typical catalytic materials are platinum(Pt), palladium(Pd), silver(Ag), gold(Au), rhodium(Rh), or iridium(Ir), where Pd is preferred. However, activation wet chemical solutions don't lend themselves to integration into semiconductor processes. Further, they have stability problems and yield large colloids rather than conformal deposits. In this work, we have deposited Pd by atomic layer deposition, and then we have to deposit Cu by electroless plating. The blanket and patterned TaN of 10 nm thick was obtained from Intel with the size of 130 nm and aspect ratio of 2. Palladium film of 3 nm was deposited on TaN by atomic layer deposition [1]. Chemicals were used in ethylenediaminetetraacetic acid (EDTA) as chelating agent, glyoxylic acid as a reducing agent, and additional chemicals such as polyethylene glycol and 2,2, dipyridine is surfactant and stabilizer individually. The pH of bath was adjusted 11.8 with tetramethyammonium hydroxide (TMAH). The solution temperature was maintained at 65°C. There has been success the super-filling and fill-up on TaN. The samples were characterized by using SEM, AFM and XPS. Reference [1] Jay J. Senkevich, Fu Tang, Diana Rogers, Jason T. Drotar, Christopher Jezewski, William A. Lanford, Gwoching Wang, and Toh-Ming Lu, Chemical Vapor Deposition, 9(5), 2003.

SESSION F4: Ultra Low-K Materials
Chairs: Grant Kloster and Stefan Schulz
Wednesday Morning, April 14, 2004
Room 2003 (Moscone West)

8:30 AM *F4.1
Aluminosilicate Preparation for ILD Applications.
M. A. Morris, J. D. Holmes, R. Farrell and E. Brennan; Dimensional Solids Group, University Cork College, Cork, Israel.

Porous solid films afford the opportunity of fabricating interlayer dielectrics (the insulating layers between metal interconnects) with dielectric constant (K) below the limits imposed by silica. Ordered mesoporous systems that have defined structure and pore size1 are particularly interesting because of the regularity of the structure and mass transport limitations based on small pore diameters. For industrial use, techniques must be developed which allow mesoporous

thin films (MTFs) to be cast that are commensurate with the requirements of the processing technology. Strict control of the MTFs and their precursors is required. I.e. the films must be isotropic and have the required properties in terms of dimension, adhesion, and mechanical performance. The films also have to be sufficiently chemically robust to survive secondary processing environments. The films produced here where prepared from clear gels synthesised from hydrolysis and condensation of tetraethylorthosilicate (TEOS) in the presence of poly-(alkylene oxide) block copolymers templates. Films were cast onto silicon wafers by both spin coating and dip coating techniques. These were dried and calcined at temperatures between 600 and 800 K to provide MTFs. A typical MTF film structure from high and low resolution electron images illustrates the crack free and highly ordered nature of the film. X-ray diffraction data suggest the films are almost single crystal in nature. In all cases studied here, the properties of the MTFs such as adhesion, mechanical performance and chemical robustness could be greatly improved by the addition of alumina into the silica framework of the film so as to prepare Al-MTFs. This was carried out at the gel synthesis stage by incorporation of alumina secbutoxide and careful control of the hydrolysis reaction. MASNMR shows that aluminium is bound within the silica framework of the MTF but located mainly at the surface of the pores. The beneficial effects of aluminium addition can be seen in figure 2 where the hardness of films is plotted against aluminium content. Data is presented showing how aluminium incorporation improves chemical robustness. The films exhibit K values below 2. Strict control of process conditions are required to prevent contamination of the film and resultant high K values. At low aluminium loadings the K value is largely unaffected compared to native silica films. The possible use of MTFs in ILD applications is discussed in light of these results. References 1. C T Kresge, M E Leonowicz, J C Roth, J C Vartulli, J S Beck, Nature; 359(1992)710.

9:00 AM F4.2
Theoretical Investigation of the Dielectric Constant and the Elastic Modulus of Porous Materials for Designing Pore Structures of Ultra Low-k Films with High Mechanical Strength. Hidenori Miyoshi[1], Hisanori Matsuo[1], Hirofumi Tanaka[1], Kazuo Kohmura[1], Nobutoshi Fujii[1], Yoshiaki Oku[1], Syozo Takada[2], Nobuhiro Hata[3] and Takamaro Kikkawa[3,4]; [1]MIRAI-ASET, Tsukuba, Ibaraki, Japan; [2]ASRC-AIST, Tsukuba, Ibaraki, Japan; [3]MIRAI-ASRC-AIST, Tsukuba, Ibaraki, Japan; [4]RCNS, Hiroshima Univ., Higashi-Hiroshima, Hiroshima, Japan.

The desirable structures and arrangements of pores in the dielectrics for the development of ultra low-k porous films with high mechanical strength were investigated in detail. We calculated the dielectric constant (k) and the elastic modulus (E) of porous films in the film thickness direction by finite element methods (FEM) assuming that properties of the wall materials are constant. We have previously shown that the periodicity in pore structure increases E with maintaining k. Shrinkage of pores in the film thickness direction will hinder the simultaneous achievement of ultra low dielectric constant and high elastic modulus. Two-dimensional periodic porous films have anisotropy in both k and E. Decreasing the domain size of ordered structures and shortening the pore length are the effective method for reducing the anisotropy in k. Disordered porous films having cylindrical pores with well-controlled pore sizes will have isotropic characteristics, and have the similar relationship between E and k as the two-dimensional periodic porous films in which cylindrical pores are oriented parallel to the wafer substrate. Periodic porous films having the three-dimensional cubic arrangement have higher E/k ratios than the two-dimensional periodic porous films. The three-dimensional cubic porous films have isotropy in k. If the porous films have the form of the single crystal of the cubic lattice, values of E depend on the crystal orientations. When the porous films consist of polycrystalline domains where each domain has the periodic cubic pore structure, the films have isotropy in E. Periodic porous silica films and disordered porous silica films can be synthesized by use of a self-assembling technology of surfactant and an acidic silica derived from silica sol. These films are shown to be promising candidates of ultra low-k films with high mechanical strength.

9:15 AM F4.3
Chemical Vapor Deposition Strategies For Porous Low Dielectric Constant Films. Kenneth K.S. Lau[1], Daniel D. Burkey[2] and Karen K. Gleason[1]; [1]Chemical Engineering, Massachusetts Institute of Technology, Cambridge, Massachusetts; [2]Chemical Engineering, Northeastern University, Boston, Massachusetts.

Chemical vapor deposition is explored as a means to produce porous low dielectric constant films. The choice of precursors is found to be critical in developing robust films with a strong matrix and closed pores. Siloxane ring structures, such as trimethyltrivinylcyclotrisiloxane and tetramethylcyclotetrasiloxane, are found to be suitable in building a strong Si-O-Si network. Additional strengthening of the film network is achieved through condensation chemistries, analogous to sol-gel reactions, during post-deposition anneal. Si-OH and Si-OR structures, introduced by water and tetraethoxysilane additives, allowed Si-O-Si bonds to form by the elimination of H_2O and ROH. Film porosity is generated by incorporating thermally labile porogen units, such as methyl methacrylate, that are removed during post-deposition anneal. Films are deposited by pulsed plasma enhanced chemical vapor deposition (PPECVD). Fourier transform infrared spectroscopy (FTIR) captured structural changes during post-deposition anneal due to condensation and porogen decomposition reactions. Film thickness and refractive index were measured by variable angle spectroscopic ellipsometry (VASE). Mechanical hardness was evaluated by nanoindentation. A mercury probe was used to determine dielectric constant and porosity was measured by positron annihilation spectroscopy (PALS). Films with dielectric constants in the range of 1.9 to 2.3 can be achieved. PALS determined the pores to be essentially closed, on the order of 1.4 to 1.6 nm in diameter. Film thickness loss during annealing remains an issue, although retention of up to 89% thickness has been achieved.

9:30 AM F4.4
Novel Epoxy Siloxane Polymer as Low-k Dilectric.
Pei-I Wang[1], Jasbir Singh Juneja[1], Shyam Murarka[1], Toh -Ming Lu[1], Rajat Ghoshal[2] and Ram Ghoshal[2]; [1]Center Of Integrated Electronics, Rensselaer Polytechnic Institute, Troy, New York; [2]Polyset Chemical Co. Inc., Mechanicville, New York.

The semiconductor industry has adopted Copper as the choice of interconnect metal but is still struggling to find an acceptable low-k material to further reduce the RC interconnect delay. There are stringent electrical, mechanical, chemical and thermal property requirements for the candidate low-k materials. This paper introduces a low-k dielectric material, a novel epoxy siloxane polymer, which has promising properties. The polymer was spin-deposited, and thickness and optical properties were measured using variable-angle spectroscopic ellipsometry (VASE). FTIR, done on as deposited and cured polymer, showed that the polymer is fully cured at 165 °C. The low curing temperature of the polymer lowers stress in BEOL stack and thus improves the reliability. The polymer is thermally stable up to at least 350 °C. The polymer has Young/s modulus of 5 GPa and hardness of greater than 0.4 GPa. After multiple stress cycles up to 300 °C, the residual stress in the polymer at room temperature is less than 60 Mpa. The polymer has good adhesion with semiconductor and dielectrics such as Si, SiC, SiO2, metals such as Al, Cu, Co, W, and barrier materials such as TaN. The bulk dielectric constant of the polymer is 2.4 - 2.7. The leakage current density in the polymer at the applied electrical field of 1 MV/cm is in 10^{-9}A/cm^2 range and the breakdown field of the polymer is above 7 MV/cm. The polymer when subjected to BTS (bias temperature stress) conditions of 150 °C and 0.5 MV/cm shows no C-V shift for at least up to 100 min indicating that the polymer resists Copper diffusion. The current density under stress conditions of 150 °C and 0.5 MV/cm was less than 10^{-9} A/cm^2 for at least up to 7 hrs.

9:45 AM F4.5
Thin Polyoxymethylene Film as a Sacrificial Layer for Air-Gap Fabrication. Kelvin Chan and Karen Gleason; Massachusetts Institute of Technology, Cambridge, Massachusetts.

The goal of this research is to devise a novel technique for fabricating air gaps using polyoxymethylene (POM) thin films. Air has the lowest dielectric constant of 1.0 and would decrease the parasitic capacitance between metal lines if it replaced current intra-layer dielectrics. In addition, air has the lowest refractive index of 1.0, and the replacement of current low-index materials with air would enable high-reflectance optical filters to be made with fewer layers. Polyoxymethylene decomposes in the absence of oxygen into formaldehyde gas as the only product at approximately 250 °C, leaving behind negligible residue. Thermogravimetric analysis results show that the mass loss during decomposition of POM is over 99.5% for a variety of samples. In addition, POM is an engineering plastic with high modulus and strength and is resistant to most chemical attacks. These properties make POM a viable sacrificial material for fabricating closed-cavity air gaps. The scheme of fabrication includes, at a minimum, four steps–thin-film deposition of POM, patterning of POM film, deposition of overcoat layer, and decomposition of POM. During decomposition, formaldehyde diffuses through the overcoat layer, leaving structured voids behind. Chemical-vapor-deposition and spin-on techniques have been developed for depositing thin films with thicknesses on the order of 1000 Å. POM patterning is accomplished through oxygen-plasma etching with SiO_2 or photoresist as a mask. The etch selectivity of POM to photoresist is at least 5:1, and the etch rate is on the order of 1000 Å/min in a low-power plasma. Closed-cavity single-level air-gap structures have been fabricated, and multilevel structures can be fabricated by repeating the procedure. Air gaps as narrow as 2 μm have been fabricated, and these are visualized using cross-sectional scanning electron microscopy. With better lithographic tools, smaller air gaps may be fabricated.

10:30 AM *F4.6

Supercritical CO2 Treatments for Semiconductor Applications. Shubhra Gangopadhyay[2], Jorge A Lubguban[2], Bashar Lahlouh[1], G. Sivaraman[1], K. Biswas[1], T. Rajagopalan[1], N. Biswas[1], H.C. Kim[3], W. Volksen[3] and R.D. Miller[3]; [1]Physics, Texas Tech University, Lubbock, Texas; [2]University of Missouri, Columbia, Missouri; [3]IBM Almaden Research Center, San Jose, California.

Supercritical fluids (SF) have been used in a wide variety of applications; in industrial processes, analytical, waste detoxification, etc. Recently, its usefulness extends to the semiconductor industry. Researches have shown that supercritical CO2 (SCCO2) can be used to remove photoresists and significantly reduce the amount of waste from solvents in comparison to conventional stripping techniques. SF will also find its usefulness in cleaning high aspect ratio vias as semiconductor features shrink to sub-micron levels. We will report here the use of supercritical CO2 treatments in extraction of porogens from a hybrid film fabricated via templated-porogen approach and its use in repairing the damage in porous films from plasma ashing. We will show that SCCO2 /co-solvent extraction of porogens is a better alternative to thermal degradation route of creating nanoporosity in the films. The ability to tune the solvation and diffusion power of SCCO2 and to swell the film matrix makes it a good medium for silylation to restore hydrophobicity and functionalize the film.

11:00 AM F4.7

Novel Templates for Ordered Mesoporous Low k Films Prepared in Supercritical Carbon Dioxide. Rajaram Achut Pai, Jason J Testa and James J Watkins; Chemical Engineering, University of Massachusetts, Amherst, Massachusetts.

The preparation of ordered mesoporous films by the replication of block copolymer templates in supercritical carbon dioxide offers a versatile route to robust low k films. Recently, we reported films exhibiting dielectric constants of 2.1 and hardness of 0.75 GPa using commercially available poly(ethylene oxide)-poly(propylene oxide)-poly(ethylene oxide) (PEO-PPO-PEO) triblock copolymers as templates. The procedure involves the infusion and selective condensation of silicon alkoxides within microphase separated block copolymer templates dilated with supercritical carbon dioxide. X-ray diffraction and electron microscopy indicated the films exhibited ordered spherical and cylindrical morphologies. One attribute of the Supercritical Fluid-based process is that the template preparation and organization occur prior to silica network formation. This removes cooperative template/precursor assembly as a requirement for system selection and offers a great deal of flexibility with respect to template selection and modification. Here, we report the preparation of mesoporous films using second generation template systems in which both domains of the template system are pre-organized and amorphous. The morphology of the template was studied was studied using atomic force microscopy. Mesostructured silicate and organosilicate films were prepared using these templates and characterized using x-ray diffraction and transmission electron microscopy. Both the as-infused silica/template composites and the detemplated films show exceptional degree of order. The consequences for performance as low k films will be discussed.

11:15 AM F4.8

Sacrificial Porogens for the Production of Low-k Organosilicates: Nucleation and Growth vs. Templating. Robert D. Miller[1], Victor Lee[1], Eric Connor[2], James L Hedrick[1], Craig J Hawker[1], Teddie Magbitang[1], Ho-Cheol Kim[1] and Willi Volksen[1]; [1]K17F, IBM Almaden Research Center, San Jose, California; [2]Symyx Technologies, Santa Clara, California.

The drive toward smaller device features and increasing functional densities is fueling the push for new low-k materials. Dielectric targets with k< 2.2 will require porous materials. We have studied for some time the generation of porosity in organosilicates using sacrificial macromolecular porogens. These porogens can function by either a nucleation and growth mechanism or by templating. The latter process ultimately produces pores which reflect the size and shape of the porogen molecule in the thermosetting matrix. Recently, we have found that extensive particle crosslinking is not necessary to achieve templating behavior in organosilicate matrices. Unimolecular polymeric amphiphiles containing a nonpolar core and a compatibilizing corona show nanoparticle-like behavior in many organosilicate matrices. Star-shaped amphiphilic block copolymers show micelle-like behavior without the need for dynamic self assembly. Materials of this type can be prepared by various tandem polymerization techniques such as controlled radical-radical and anionic-radical procedures. These use of these materials for the preparation of nanoporous thin film organosilicates will be discussed.

11:30 AM F4.9

Atomizer Delivery of Porogen for Creating Porous Low-k Dielectrics by Chemical Vapor Deposition. April Denise Ross and Karen K Gleason; Chemical Engineering, Massachusetts Institute of Technology, Cambridge, Massachusetts.

There is an increasing need for low-k solutions in integrated circuits that can be extended to future generations. Two different pathways are explored to lower the dielectric constant of these materials relative to silicon dioxide (k 4). By incorporating atoms and bonds that have a lower polarizability, such as alkyl groups, or by lowering the density of the material, either sterically or through the integration of air, the value of the dielectric constant is reduced. Creating porous films using an organosilicate glass (OSG) matrix is an avenue for introducing void space and thereby decreasing density and lowering the dielectric constant. Since the introduction of porosity severely diminishes the mechanical integrity of the material, understanding the relationship between film structure and mechanical properties becomes extremely important. The main dichotomy of methods for producing low-k materials is between chemical vapor deposition (CVD) and spin-on dielectrics (SOD). At this time, the focus in literature has been on SOD using an OSG matrix/porogen approach. Due to increasing awareness and concern for environmental, safety and health (ESH) issues, CVD has the advantage of being a solventless process and therefore is favorable when compared to SOD. In addition, discovering a CVD process for the creation of porous materials would lead to easier integration with existing toolsets. Depositing matrix and porogen precursors simultaneously using CVD creates many obstacles as the deposition requirements of the two species are significantly different. A novel approach to alleviate this problem is to use pre-formed porogens, such as polystyrene micro-spheres or cyclodextrin. This allows use of the deposition conditions that give the optimal matrix material structure, with disregard to the effect on the porogen deposition. An ultrasonic atomizer can be used to introduce these porogen materials into the reactor for deposition. Another advantage gained from this technique is that the pore size is controlled and determined by size of the porogen. Cyclodextrin is a prime porogen candidate due to its low decomposition temperature and small molecular size. The OSG matrix was deposited using pulsed plasma-enhanced CVD from octamethylcyclotetrasiloxane (D4). In addition, hydrogen peroxide (H2O2) was used as an oxidant to promote OH end groups throughout the film. Upon annealing the films at 40°C, condensation reactions occur between proximal Si-OH groups, liberating water and generating Si-O-Si network bonds to strengthen the film. A study of the film structure before and after annealing through FTIR analysis confirms increased crosslinking upon annealing and provides a key step to understanding the link between film structure and mechanical properties. For a deposition with a precursor flowrate ratio of H2O2 to D4 of 25:1 and an equivalent power of 30W, a two fold increase in hardness was observed upon annealing (0.201 to 0.417 GPa).

11:45 AM F4.10

Comparative Studies of Ultra Low-k Porous Silica Films with 2D-Hexagonal and Disordered Pore Structures. Nobutoshi Fujii[1], Kazuhiro Yamada[1], Yoshiaki Oku[1], Nobuhiro Hata[2], Yutaka Seino[2], Chie Negoro[2] and Takamaro Kikkawa[2,3]; [1]MIRAI-ASET, Tsukuba, Japan; [2]MIRAI-ASRC-AIST, Tsukuba, Japan; [3]RCNS, Hiroshima Univ., Higashi-Hiroshima, Japan.

In order to reduce interconnect delays of high-speed ULSIs, it is necessary to develop ultra-low-k materials whose dielectric constants are less than 2.5. We have developed periodic porous silica films having a 2-dimensional hexagonal cylinder pore structure by use of sol-gel self-assembly technique. The pore structure was controlled by the static electrical interaction between the micelle of the surfactant and the silica oligomer. The size of the micelle was controlled by the molecular length of the surfactant. In this study, a disordered porous silica film have been developed using a nonionic surfactant as a template. It is shown that the disordered porous silica films have wormhole like network with a uniform pore channel diameter. The precursor of the disordered porous silica was synthesized based on tetraethyl-orthosilicate (TEOS), ethanol, methyl-silicate and the tri-block copolymer ((EO)x(PO)y(EO)x, where EO is polyethylene oxide and PO is polypropylene oxide block). No X-ray diffraction peaks were observed for this disordered mesoporous silica film, while the small angle X-ray scattering spectroscopy showed the pore diameter distribution ranging from 2.0 to 4.0 nm. Comparing the properties of 2-D hexagonal and disordered porous silica films, it is found that the dielectric constant (k∼2.2), Young's modulus (E∼5GPa) and Hardness (H∼0.5GPa) were nearly the same for both the 2-D hexagonal and disordered porous silica films
while were derived from the same surfactant and had the same porosity.

SESSION F5: Ultra Low-K Characterization and Reliability
Chairs: Shubhra Gangopadhyay and Ehrenfried Zschech
Wednesday Afternoon, April 14, 2004
Room 2003 (Moscone West)

1:30 PM *F5.1
Porosity Characterization of Mesoporous Dielectric Thin Films Using Positron Annihilation Spectroscopy (PAS).
Kelvin G. Lynn[1,2], Marc Weber[1,2] and Cai-Lin Wang[1,2]; [1]Center for Materials Research, Washington State Univ., Pullman, Washington; [2]Physics Department, Washington State University, Pullman, Washington.

Beam based Positron Annihilation Spectroscopy (PAS) is a recent addition to the spectrum of diagnostic tools useful for the characterization of low-dielectric constant (low-k) thin films. Using the annihilation signatures of positronium (Ps: H-like positron-electron atom), PAS provides information on total porosity, pore size, pore size distribution and void interconnectivity (percolation) as a function of film depth. In this presentation examples of the utility of various PAS techniques to characterize porous MSSQ films as a function of porogen load will be presented. The PAS results are subsequently compared to more traditional characterization techniques including CV, AC-conductivity, FE-SEM, FTIR, TGA, elipsometry, and hardness measurements. Various beam PAS techniques (PALS, 3-γPs annihilation, Doppler Broadening) were used in this work to obtain a global picture of film porosity. We report results from measurements of various types of mesoporous films, in which the porosity has been varied. The following aspects of this work will be highlighted in this paper: (1) Positron Lifetime Spectroscopy (PALS) lifetime distributions, from which pore size distributions are derived. (2) 3g - Ps self-annihilation measurements, from which void interconnectivity and the fraction of open cell and closed cell porosity. (3) Ps momentum sensitive Doppler Broadening techniques from which pore distributions and pore interconnectivity are deduced (4) Various positron depth-profiles from which non-uniform pore distributions, open and closed cell porosity can be determined. Examples, on how information of open versus closed porosity, the total porosity, the pore sizes and a measure of the average length of connected pores will be briefly discussed. This work shows that PAS offers a number of unique techniques for the characterization of thin film porosity and compared to other measurements. The authors wish to thank collaborations with Ken Rodbell, M. Petkov, C. Fisher on various stages of this work.

2:00 PM F5.2
3-dimensional evaluation of nm-pores in porous low-k films using TEM stereoscopic / electron tomographic observation method.
Junichi Shimanuki[1], Shinichi Ogawa[2], Miyoko Shimada[2] and Yasuhide Inoue[1]; [1]Nano Analysis Section Research Department, NISSAN ARC, LTD., Yokosuka, Japan; [2]Semiconductor Leading Edge Technologies, Inc., Tsukuba, Japan.

Porous low-k films are expected to be one of ultra low dielectric materials for multilevel Cu interconnects below 65nm node. It is notable that shape and size of pores and spatial distribution in the films may affect mechanical and electrical properties of the interconnects during BEOL processes such as metallization, CMP, and cleaning, and packaging processes. Several methods for characterizing the pore distribution have been eagerly studied, e.g. high-resolution specula X-ray reflectivity, small-angle neutron scattering, and gas-absorption, however these methods are not able to detect pore shape and spatial distribution. On the other hand, since the contrast from the amorphous layer affect the pore imaging, pores are difficult to be imaged in amorphous film. Thus only several works on TEM observations of the pores have been reported (1), while TEM has a high potential to observe nm size structures directly. In general, because TEM images are 2-dimensional transmitted, it is difficult to obtain sufficient information of pores in the amorphous layer as compared with three-dimensional imaging. In this work, two methods of the three-dimensional TEM observation techniques were introduced. One is TEM stereoscopic observation method and the other is electron tomography. In the former method, the three dimensional image was taken by superposing only two images, which were obtained by tilting a specimen in two different angles. The shape and size of pores and spatial distribution in the films were evaluated qualitatively. As for the latter method, several tens images were taken by tilting the sample from low to high angles using a special TEM holder. 3-D reconstruction and image quantitative analysis were done by a commercial software. As the result, the amorphous contrast was reduced, and pores are not spherical but distorted shape with a minimum size of less than 1 nm. These pores heterogeneously distributed in the films and concentrated at the interfaces. It was clarified that novel knowledge of pores in the porous low-k films was obtain by 3-dimensional TEM observation technology. (1) S. Ogawa et al, 2003 IITC Proc. P.100

2:15 PM F5.3
Structural Characterization of Methylsilsesquioxane based Low-k Films Using X-ray and Neutron Porosimetry.
Hae-Jeong Lee[1], Christopher L Soles[1], Bryan D Vogt[1], Da-Wei Liu[1], Barry J Bauer[1], Wen-li Wu[1], Eric K Lin[1], Gwi-Gwon Kang[2] and Min-Jin Ko[2]; [1]Polymers Division, National Institute of Standards and Technology, Gaithersburg, Maryland; [2]LG Chemical LTD, Taejon, South Korea.

The characterization of pore structure in porous thin films is essential to develop robust low dielectric constant materials that are compatible with adjacent semiconductor processes. X-ray porosimetry (XRP) and neutron porosimetry (NP) are recently developed methodologies to extract the detailed pore structures. These methodologies utilize capillary condensation of solvent molecules (probe molecules) inside the accessible pores as a function of relative partial pressures. The partial pressure of the solvent is isothermally varied by mixing stream of dry air and solvent saturated air in different ratio. As the partial pressures increases, larger pores are filled gradually. In XRP, the partial pressure is converted into pore sizes using the Kelvin equation and the amount of probe molecule uptake is used to determine the population of pores corresponding to that size. The mass uptake determined from the critical angle for total x-ray reflection without additional assumption concerning physical parameters using specular x-ray reflectivity. In NP, contrast matched (CM) solvent with a scattering length density (SLD) that is the same as that of wall material is first determined from a series of small angle neutron scattering (SANS) curves collected under a saturated solvent environment composed of different mixtures of hydrogenated and deuterated solvent. Because the SANS intensity is minimized at this match point, wall mass density can be estimated from the SLD of solvent mixture displaying minimum scattering intensities. The correlation lengths of pores are determined at various partial pressures of CM solvent and the porosities at same partial pressure determined from the XRP are used to convert the SANS correlation lengths into pore sizes. In this work, we investigate pore structures in the methylsilsesquioxane-based materials with porogen loadings from 0 % to 45 %. We will discuss the influence of porogen loading on the detailed structural information of pores in the thin films such as pore size distribution, wall density, average density, depth profile, wall homogeniety and porosity by using XRP and NP as complementary methodologies.

2:30 PM F5.4
Ellipsometric Porosimetry of Porous Low-K Films with Quazi-Closed Cavities.
Mikhail Baklanov[1], Konstantin Mogilnikov[2] and Jin-Heong Yim[3]; [1]IMEC, Leuven, Belgium; [2]SOPRA, Bois Colombes, France; [3]Samsung Advanced Institute of Technology (SAIT), Kyungki-do, South Korea.

Introduction of porous low-K films as interlevel dielectrics has met number of controversial requirements. An increase of porosity decreases dielectric constant but also reduces mechanical properties. Decrease of the pore size facilitates surface sealing. However, materials with small pore size and thin walls between the pores have deteriorated mechanical properties [1]. For this reason, several companies have developed porous low-K films with relatively large embedded voids. Most of these materials have narrow necks, connecting the voids with air. The "necks" may be a constitutive property of the matrix material and might be formed during the porogen evaporation. Evaluation of pore structure of these materials is quite difficult. PALS shows multimodal porosity but the information has a limited practical value because it doesn't predict the pores behavior during the gas, solvent, and Cu diffusion. Moreover, limitation of postronium movement from large voids to small "necks" can result an erroneous conclusion that these voids are completely closed [2]. In this paper, we report a method for evaluation of low-K films with "quasi-closed" voids (cavities). We demonstrate that the method based on Ellipsometric Porosimetry (EP) provides results that are in good agreement with SEM/TEM analysis and, therefore, provide a realistic measure of the pore structure. Porous CSSQ (cyclic silsesquioxane) based films developed by SAIT and used in this study are described elsewhere [3]. Evaluation of porosity and pore size distribution was done using EP-10 at IMEC. Calculation of void and neck sizes is based on theory of pore "blocking effects" that has been developed starting from pioneering work of Kraemer [4]. It is shown that theory of pore "blocking effects" can be successfully used in EP and the results accurately describe the pores structure of such systems. Theory of the "pore blocking" phenomena and experimental results are discussed. 1.K.Maex, M.R.Baklanov, D.Shamiryan, F.Iacopi, S.Brongersma, Z.Sh.Yanovitskaya. J.Appl.Phys. 93, 8793, 2003. 2.K.P.Mogilnikov, M.R.Baklanov, D.Shamiryan and M.P.Petkov. Jpn.J.Appl.Phys., 2003. 3.J.-H Yim, Y.-Y Lyu et al. Advanced Functional Materials, 13(5), 386, 2003. 4.E.O.Kraemer, Treatise on Physical Chemistry, D. Van Nostrand: New York, 1931; B.V.Derjagin, Acta Phys.-Chim. 12, 181, 1940; J.C.P. Broekhoff, J.H.deBoer, J.Catal., 10, 153, 1968; A.Vishnyakov, A.V.Neimark, Langmuir, 19,

3240, 2003.

3:15 PM F5.5

Cross-section nano-indentation for rapid adhesion evaluation.
Sywert H Brongersma[1], Jerome Souiller[1], Dominiek Degryse[1], Bart Vandevelde[1] and Karen Maex[1,2]; [1]SPDT/ITTO, IMEC, Leuven, Belgium; [2]E.E.Department, Katholieke Universiteit Leuven, Leuven, Belgium.

As the complexity of back-end-of-line processing continues to increase with the use of many new materials and deposition techniques, the need for reliable rapid adhesion evaluation becomes increasingly important. 4-point bending has established itself as the reference technique based on its ability to yield reproducible quantitative data. Additionally it is independent of stresses in the stack as both sides of the tested interface remain fixed on a substrate after testing. Consequently it yields real interface adhesion, although this may not always be a good indicator for performance in an actual structure. Sample preparation and obtaining good statistics is, however, quite time consuming resulting in a slow feedback for process optimization. A faster method for adhesion evaluation is cross-section nano-indentation where a diamond tip is pressed into the side surface of a cleaved sample. By doing this just behind (several microns) the deposited stack, cracks can form from two of the corners of the triangular shaped tip outwards. When these cracks deflect into the weakest interface of the stack, delamination occurs and the length of delamination can be directly observed in the microscope of the indenter set-up. A series of 4-5 of such indents at several distances behind the interface normally yields a clear correlation between the force exterted and the delamination observed, and from this adhesion can be obtained. For quantification of the results we depend on both finite element simulations and a comparitive study with 4-point bending. So far results have been obtained for adhesion of the copper-barrier interface using several different deposition techniques for both layers (SIP, ALD, electroplating, direct plating). Now the technique is ready to be implemented as a quick screening tool, while applicability for other stacks/materials is being investigated. Finally, it should be noted that also crack propagation from the indent, through a damascene structure up to the surface can yield interesting data on sidewall interfaces.

3:30 PM F5.6

Adhesion Strength Evaluation of Low-k Interconnect Structures Using a Nanoscratch Method.
jiping ye[1], Kenichi Ueoka[1], Nobuo Kojima[1], Junichi Shimanuki[1], Miyoko Shimada[2] and Shinichi Ogawa[2]; [1]Research Dept., NISSAN ARC LTD., Yokosuka, Japan; [2]Semiconductor Leading Edge Technologies, Inc., Tsukuba, Japan.

Low-k dielectric materials have attracted a great deal of attention for application to multilevel Cu interconnects and packaging structures. The integration of microelectronic components results in various interfaces between the low-k material and inorganic dielectric layers, such as SiO_2 and SiC. Usually, the low mechanical properties exhibited by low-k dielectric materials are apt to cause debonding of the low-k layer and poor interfacial adhesion will lower the reliability of the interconnect structures. In this work, the adhesion of low-k interconnects with a SiO_2 cap layer was evaluated using a nanoscratch method combined with AFM and TEM observations. The investigation focused on the fact that the low-k layer with a rare-gas plasma pretreatment exhibited low delaminated densities in Cu CMP process. Specimens having a microstructure of Cu/Ta/TaN/pSiO_2/low-k/SiC/pSiO_2/Si-sub were examined, where the low-k layer of some samples was pretreated with rare-gas plasma before growing the SiO_2 cap layer. In the nanoscratch measurement, the fracture strength was characterized on the basis of the critical normal load at the first abrupt decrease in the friction coefficient. It was observed that specimens with the rare-gas plasma pretreatment displayed a high friction coefficient and a higher critical normal load than specimens without the pretreatment. AFM observation showed that larger pile-ups were not present ahead of the nanoscratch but on the nanoscratch sides for specimens with the rare-gas plasma pretreatment. As for specimens without the rare-gas plasma pretreatment, it was observed that a scratch residual was situated ahead of the nanoscratch and was easily peeled while much smaller pile-ups were found at the nanoscratch side. These nanoscratch measurements demonstrated that the rare-gas plasma pretreatment reinforced the adhesion strength of the low-k interconnect with the SiO_2 cap layer, which agreed with the CMP test results. The results indicated that the nanoscratch method make it possible to predict the CMP process endurance of the low-k interconnect structures and processes.

3:45 PM F5.7

Effect of mode-mixity and porosity on interfacial fracture of low k dielectric.
caroline catherine merrill[1,2] and Paul S. Ho[2]; [1]INTEL, albuquerque, New Mexico; [2]Laboratory for Interconnect & Packaging, University of Texas at Austin, Austin, Texas.

With device scaling continuing beyond the 130 nm node, low-k interlevel dielectrics (ILD) are being implemented to replace oxide in Cu interconnects. Their weak thermo-mechanical properties cause significant reliability problems for Cu/Low-k interconnects. Indeed, their low modulus and high thermal expansion coefficient can cause interfacial debonding during thermal cycling or CMP. The dual-damascene structure of the Cu interconnect can give rise to complex stress states at the Cu/ILD interface. Therefore, it is important to study interfacial adhesion as a function of mode-mixity, from pure tension to pure shear. In this study, we developed a system allowing interfacial adhesion measurements as a function of mode-mixity. This system was evaluated by measuring the adhesion of a porous MSQ-based spin-on-glass to different cap layers and comparing the results with previous results obtained with the four-point bending method. Critical adhesion energies were measured at different stress states ranging from mode I loading (pure tension) to mixed-mode loading (mode I and II combined) to mode II loading (pure shear). It was found that in every case, the debonding energy increases, by a factor of 3 to 10, as the amount of shear stress increases, approaching mode II conditions. The crack propagation path as a function of mode-mixity was also investigated using analytical tools including SEM, FIB and AFM. Additionally, the debonding energy was found to decrease with increasing porosity. The effect of plastic deformation of surrounding thin film layers on the adhesion energy was also observed.

4:00 PM F5.8

Steady State Delamination of an Interface of Interest For Repeatable G_C in Adhesion Studies of Low-k Dielectric Thin Films.
Charles T. Malone[1], Roey Shaviv[1], Dayton Cheatham[1], Carole Mars[2], Easwar Srinivasan[2] and David Mordo[1]; [1]Novellus Systems, Inc., San Jose, California; [2]Novellus Systems, Inc., Tualatin, Oregon.

As interconnect technology progresses, interfacial adhesive strength becomes critical for successful Cu / low k dielectric integration. The 4-point bend test is the most accepted technique for quantifying interfacial fracture resistance, G_C. This technique is used in several different ways with varied success. There are common sample structures and test conditions that can often result in catastrophic delamination at an interface other than the one being studied. This has been particularly true in the development and integration of brittle low k dielectric film stacks and their adjacent barriers and caps, where it can be more challenging to get steady state delamination at the interface of interest. This paper details our work with such film stacks. We describe details of sample preparation procedure and test velocity settings that are helpful in obtaining steady state delamination of an interface of interest. We also suggest methods for quantifying the quality of a critical load plateau. In addition, we explain our failure analysis methodology that identifies the delaminated interface and failure mechanism.

4:15 PM F5.9

Anisotropic Elastic Properties of Low-k Dielectric Materials.
Alexei A Maznev[1], Gretchen Alper[1], C.J.L. Moore[1], Michelle T. Schulberg[2], Raashina Humayun[2], Archita Sengupta[2] and Jia-Ning Sun[2]; [1]Philips Advanced Metrology Systems, Natick, Massachusetts; [2]Novellus Systems, San Jose, California.

While low-k dielectrics are being pursued by the semiconductor industry because of their electrical characteristics, mechanical properties such as hardness and elastic modulus are equally important in terms of providing structural integrity of interconnect structures. Techniques currently accepted in the industry for measuring mechanical properties (e.g. nano-indentation) are based on the assumption that film properties are isotropic. In thin film deposition, however, the presence of a substrate presents an asymmetric condition that may lead to structural anisotropy resulting from one-dimensional shrinkage, preferential alignment of polymer chains or ordering or orientation of the pores. Consequently, elastic properties of thin film materials may be different for the directions parallel and perpendicular to the plane of the film. Nano-indentation is not adequate for characterization of such anisotropic materials. Methods based on surface acoustic waves, on the other hand, have proved capable of determining anisotropic elastic properties of thin films [1]. In this work, we characterized elastic properties of Novellus low-k materials by a non-contact technique utilizing laser-generated surface acoustic waves. Two materials were analyzed: a PECVD-deposited CORAL film (k = 3.0), and a novel porous ultra-low k film (k = 2.2). The most interesting finding is that of a strong elastic anisotropy in the advanced porous low-k material. Namely, the "in-plane" compressional modulus is found to be 2-3 times larger than the "out-of-plane" modulus. We will discuss the relationship between the elastic anisotropy and the structure of the films, as well as the potential impact of a higher in-plane stiffness on the film performance

in processing steps such as CMP and packaging. [1] J.A. Rogers, L. Dhar and K.A. Nelson, Appl. Phys. Lett. 65, 312 (1994).

4:30 PM F5.10
Reliability of Dielectric Barrier Films in Copper Damascene Applications. Albert Sanghyup Lee, Annamalai Lakshmanan, Nagarajan Rajagopalan, Zhenjiang Cui, Maggie Le, Deenesh Padhi, Girish Dixit, Li Qun Xia, Bok Heon Kim and Hichem M'Saad; Dielectric Systems & Modules Product Business Group, Applied Materials, Inc, Santa Clara, California.

With the advent of copper dual damascene, dielectric copper barriers are becoming the cornerstone for back end of line device reliability. This paper will address two concepts for dielectric thin film reliability: hermeticity of the bulk barrier film and adhesion between the barrier and copper layers. It is known that improved adhesion corresponds to improved electromigration. In this paper, we show that adhesion is improved by interfacial engineering of the barrier film. We introduce the concept of hermeticity, which is the film's ability to prevent moisture from penetrating into the underlying layer. The barrier film hermeticity is important because a non-hermetic film can allow copper oxide formation at the barrier-copper interface, leading to adhesion loss and poor electromigration performance. In this work we have optimized the hermeticity of BLOκ I™ low-κ copper barrier film. In addition, we have examined methods to modify the interface between copper and barrier films in such a way as to dramatically improve the adhesion of the BLOκ I and Damascene Nitride™ SiN films to copper. We deposit BLOκ I in a PECVD Producer® Twin Chamber™. We used a method to quantify the film's hermeticity, where 500Å of the dielectric barrier is deposited on top of a 1μm TEOS oxide film with tensile stress, and the stack is subjected to 85°C and 85% humidity for 17 hours. A stress change in the stack indicates moisture uptake by the underlying oxide film, and a stress change of >20 MPa indicates a non-hermetic barrier film. We adjusted the BLOκ I bulk film properties by varying the process deposition conditions to optimize the hermeticity. We compare the hermeticity of four films: 1) the optimized BLOκ I, 2) Damascene Nitride, 3) an unoptimized BLOκ I film and 4) a reference with no barrier cap. The results demonstrate that the optimized BLOκ I allows a stress change of <10MPa in the underlying oxide layer, and the hermeticity of BLOκ I is comparable to that of silicon nitride. We used the 4-point bend technique to characterize the adhesion of BLOκ I and Damascene Nitride to copper. We engineered the interface between the dielectric barrier and copper to promote adhesion of the two materials. During deposition of Damascene Nitride and BLOκ, an in-situ pre-treatment step is used to remove copper oxide prior to depositing the barrier film. We optimized the transition between the pre-treatment and deposition to improve the barrier film adhesion to copper. By modifying the interface between the dielectric barrier and copper, we were able to significantly improve the adhesion strengths to >10 J/m^2 for both films. By optimizing both the bulk film properties (hermeticity) and the interface with copper (adhesion), we have demonstrated barrier film performance that minimizes reliability issues related to copper electromigration and stress migration.

4:45 PM F5.11
Scanning Near-Field Microwave Probe for In-line Metrology of Low-k Dielectrics. Vladimir V Talanov[1], Robert L Moreland[1], Andre Scherz[1], Andrew R Schwartz[1] and Youfan Liu[2]; [1]Neocera, Inc., Beltsville, Maryland; [2]International Sematech, Austin, Texas.

We have developed a novel microwave scanning probe technique for measurement of the dielectric constant of low-k films. The technique is non-contact, non-invasive, requires no sample preparation, and can be used for low-k metrology on production wafers. The probe has a few micron spot-size, and provides precision and accuracy better than 1% and 5%, respectively, for dielectrics with k < 4. The measurement can be done on both porous and non-porous dielectric films. The near-field microwave probe is based on a balanced microwave transmission line tapered down to a one-micron tip aperture. This novel approach reduces the stray fields by a few orders of magnitude when compared to the conventional unbalanced apertureless schemes. A shear-force approach is employed to actively control the tip-sample separation with 1 nm precision. When the probe tip is placed in close proximity to the sample its fringe capacitance depends on the film and the substrate permittivities, the tip geometry, and the tip-sample separation. A microwave resonator operating at 4 GHz is employed to measure this capacitance with resolution down to 0.1 aF. Extraction of the k-value is based on an original theory describing the probe-sample interaction, which provides for direct removal of the substrate contribution. For probe calibration we employ highly conducting bulk Si and a thermal oxide film. We will present results for both SOD and CVD low-k dielectric films on Si substrates and show excellent correlation with Hg-probe measurements.
Results for k-value mapping on blanket wafers will be presented as well.

SESSION F6: Poster Session: Integration and Reliability

Chairs: Grant Kloster and Toh-Ming Lu
Wednesday Evening, April 14, 2004
8:00 PM
Salons 8-9 (Marriott)

F6.1
Deposition and Integration of a Novel Ultra-Low k (2.2) Material. Michelle T. Schulberg, Raashina Humayun, Archita Sengupta and Jia-Ning Sun; Novellus Systems, Inc., San Jose, California.

Increasing demands for faster chip speed and reduced power consumption are driving the semiconductor industry to develop insulating layers with lower dielectric constants. As the dielectric constant of a material is reduced, however, it becomes increasingly difficult to achieve the mechanical strength required to manufacture a multilevel interconnect. A new route to the synthesis of mesoporous silica has been demonstrated on 200 mm wafers. Silicate precursors dissolved in supercritical CO_2 are infused into a block copolymer film. The polymer is then removed, but the resulting porous SiO_2 replicates its ordered structure, which enhances the strength of the network. Incorporation of alkyl silicates further lowers the dielectric constant. Post-treatment to cap residual silanol groups renders the surface of the film hydrophobic and stabilizes it under air exposure. By appropriate choice of the block copolymer and other process parameters, the pore size and density can be varied and k values as low as 1.8 can be achieved. For a film with a dielectric constant of 2.2, the pore size is 4 nm. The hardness and modulus are 0.6 GPa and 4.0 GPa, respectively, as measured by nanoindentation. Four-point bend measurements yield fracture energies of 9.8 J/m^2. More importantly, the film can withstand chemical mechanical planarization (CMP) using standard oxide polishing conditions.

F6.2
A Novel Organosiloxane Vapor Annealing Process for Improving Elastic Modulus of Porous Low-k Films. Kazuo Kohmura[1], Shunsuke Oike[1], Masami Murakami[1], Hirofumi Tanaka[1], Syozo Takada[2], Yutaka Seino[3] and Takamaro Kikkawa[3,4]; [1]MIRAI-ASET, Tsukuba, Ibaraki, Japan; [2]ASRC-AIST, Tsukuba, Ibaraki, Japan; [3]MIRAI-ASRC-AIST, Tsukuba, Ibaraki, Japan; [4]RCNS, Hiroshima Univ., Higashi-Hiroshima, Hiroshima, Japan.

As ultra large scale integrated circuits (ULSIs) are scaled down, the signal delay through metal interconnects increases due to the parasitic capacitance. For 45 nm technology node, ultra-low dielectric constant ($k \leq 2.0$) materials are needed. In order to reduce the dielectric constant, porous materials have been developed, while the introduction of pores to the film has caused severe degradation of the mechanical strength such as the elastic modulus and hardness. The motivation of this work is to achieve both ultra-low-k and high elastic modulus of the dielectric films. It is demonstrated that the mechanical strength of the porous silica films can be significantly improved by a novel organosiloxane vapor annealing process. The 1,3,5,7-tetramethylcyclotetrasiloxane (TMCTS) vapor treatment to the porous silica film was performed at the temperature range from 250°C to 400°C in nitrogen ambient. It is found that the elastic modulus of the porous silica film increased significantly with TMCTS treatment at 350°C or higher. When the porous silica film was treated by TMCTS at 400°C, the elastic modulus and the hardness of the film were enhanced by a factor of 2.5 and 3.0, respectively, as compared with the case without TMCTS. The FT-IR analysis indicated that the increase of the elastic modulus corresponds to the increase of the ratio of C-H stretching peak intensity arising from Si-CH3 groups to the Si-H stretching peak. The thermal desorption spectroscopy analysis also suggested that the part of Si-H groups of TMCTS reacted with Si-OH groups on the porous silica wall surface via dehydrogenation, and the residual Si-H groups were converted to Si-OH groups through hydration by desorption of water. Subsequently, Si-OH groups of TMCTS reacted with another TMCTS. Finally polymerized TMCTS network was formed on porous silica wall surface, resulting in the significant improvement of the mechanical strength of the porous silica film.

F6.3
Abstract Withdrawn

F6.4
Effect of Aqueous Solution Chemistry on Accelerated Cracking of Nanoporous Thin-Films. Eric P. Guyer and Reinhold H. Dauskardt; Materials Science & Engineering, Stanford University, Stanford, California.

Considerable effort has been directed toward integrating nanoporous

inorganic ultra-low dielectric constant materials into the interconnect structures of high-density integrated circuits. The reliable fabrication of devices containing these extremely fragile materials is, however, a significant technological challenge due to their propensity for mechanical failure during all levels of processing and subsequent device packaging in which they are subjected to mechanical loads in the presence of chemically active environments. While the effect of moisture and temperature on crack growth has received some attention, virtually nothing is known about the effect of more aggressive aqueous solutions. In this presentation, we demonstrate anomalously high crack growth rates of nanoporous methylsilsesquioxane (MSSQ) thin-films exposed to weakly acidic hydrogen peroxide solutions. Results vary markedly from those predicted by solution pH, as acidic environments are generally considered to inhibit cracking. Design strategies that involve energy dissipation by local plasticity in thin ductile layers on increasing the resistance to cracking of MSSQ films is demonstrated. We elucidate the fundamental chemical interactions and molecular mechanisms responsible for the accelerated cracking in terms of the reaction rate and the mass transport of chemically active species. Implications for the integration of nanoporous thin-films into emerging device technologies are considered.

F6.5

Probing Effects of Etching and Stripping Plasmas on the Properties of Porous Low-k Dielectrics. Lei Wang[1], Jun Liu[1], Weide Wang[1], Dongzhi Chi[1], David W. Gidley[2] and Albert F. Yee[2]; [1]Institute of Materials Research & Engineering, Singapore, Singapore; [2]University of Michigan, Ann Arbor, Michigan.

The application of porous low-k interlayer dielectrics is needed for reducing the parasitical capacitance, especially for 65-nm technology and beyond.The understanding of process modifications of these materials' properties of porous low-k materials is crucial for a successful integration. The dry etching and stripping processes of porous low-k materials are the important modules in ULSI fabrication. In this study, the interaction between MSQ-based JSR LKD-5109 films (shown by PALS to have interconnected 2.8 nm pores) with CF_4/O_2 plasma has been investigated. The various ratios of O_2 content were designed to characterize its effects on the etch rate, formation of the polymerization layer, and properties of the LKD-5109 films. The surface morphology and hydrophilicity of the etched LKD-5109 films were studied by AFM, contact angle measurement, and FTIR. It is found that structural damages caused by the etching chemistries are restricted to the surface of the films by comapring the peak intensities of Si-O (cage-like), Si-O (network like), and Si-CH_3 in FTIR spectra. However, moisture up-take and fluorine diffusion are observed after etch processing. The influence of etching chemistries on the morphological characteristics of thin Ta barrier layers (5-nm in thickness) deposited on etched low-k films was further investigated by PALS and SEM, and it is found that different etching chemistries pose significant differences on its morphological characteristics. The influence of oxygen plasma exposure to the LKD-5109 films was also studied, and it was observed that partial carbon depletion occured near the surfaces of the films. Furthermore, FTIR showed significant moisture absorption probably due to the carbon depletion in the surface region by the oxygen plasma. Methods for recovering will be discussed along with some experimental results.

F6.6

Dry Etch and Wetclean Process Characterization of Ultra Low-k (ULK) Material Nanoglass E. Badam Ramana Murthy[1], Chang Chang Kuo[1], Ahila krishnamoorthy[1], Yu wen Chen[1] and Ananth Naman[2]; [1]SPT Lab (MF), Institute of Microelectronics, SINGAPORE, Singapore; [2]Honeywell, Sunnyvale, California.

Silicon based ultra low-k dielectric material (ULK), NanoGlass-E (NGE) with k-value of 2.2 was integrated for 130nm Cu/ULK interconnect technology. This paper is focused on determining the effect of reactive ion etching (RIE) and wet chemical clean process on surface condition, electrical behavior and reliability of blanket and patterned NGE. Experiments were conducted to study etch rate, selectivity, surface roughness after dry plasma and wet chemical treatments. For trench process dual hard mask of SiC + USG was deposited on top of 5000A-NGE. Two different etch schemes were evaluated such as etching-under photoresist and etching under hard mask. Trench etching was done with different conventional gas mixtures and compared. Two gas combinations: CHF3 and C4F8 gave a near-vertical profile and critical dimension (CD) within 10%. Monotonic decrease of post etch CD was observed and attributed to pitch effect. Striations and trench side wall damage could be minimized by using non-selective etching with CHF3 gas mixture. RIE lag was found to be minimum (0.723) for CHF3 plasma and maximum (0.863) for CO-free plasma. However, resist loss during etch was found to be contradicting the RIE lag trend. Micro loading effect due to etch was found to be insignificant across the pitch. It was found that using CO-free plasma surface roughness could be reduced in the range of 30-50% compared to other gas mixtures. Etching under hard mask scheme has provided key advantage of complete elimination of strip plasma exposure to ultra low-k film. This may reduce the extent of damage to ULK which is a major concern in low-k dielectric stripping. Effect of different strip plasma chemistries on etch profile was also studied. Results showed that undercut in the trench profile can be minimized using H2/N2 gas plasma compared to O2 plasma strip with no significant impact on carbon depletion. Three formulations of post-etch wet clean conditions were evaluated for both blanket and patterned structures. For electrical testing, metal comb and serpentine structures were measured for metal continuity and bridging. Good continuity of 1 m long serpentine structures with 0.18/0.18 micron line-width/spacing was achieved. The leakage current was measured for a comb structure with 0.18/0.18 micron line-width/spacing and it was within specification. Further reliability characterization of etch process splits was done through voltage ramp test at dense and isolated structures and results showed that film was sensitive to certain plasmas.

F6.7

Pore Sealing and Its Consequences on Nanoporous Materials during Fluorocarbon Plasma Treatment. Woojin Cho[1], Oscar Rodriguez[1], Ravi Saxena[1], Ravi Achanta[1], Manas Ojha[1], Joel L Plawsky[1], William N Gill[1] and Mikhail Baklanov[2]; [1]Chemical Engineering, Rensselaer Polytechnic Institute, Troy, New York; [2]IMEC, Leuven, Belgium.

Future integrate circuit requires low dielectric constant (k) material as interlayer dielectric (ILD). The incorporation of porosity is the most plausible way of reducing the dielectric constant of a material below 2. Porous silica or silica xerogels are one promising alternative dielectric material as they can be made hydrophobic and the porosity and thickness can be tailored to desired values. Nevertheless, the porous material has several shortcomings such as metal precursor penetration into pore during CVD, ALD and/or PVD processes, poor mechanical strength, and low thermal conductivity, etc. To avoid metal penetration during its deposition process, the pore sealing of the top surface of the porous material has been proposed without affecting the dielectric properties of the nanoporous material and it might even be improved. The fluorocarbon plasma is widely used to etch the low-k material and its intrinsic polymerization always exists during the process. We used CHF3 as a reactant gas to expedite the rate of polymerization due to the presence of hydrogen atom. Pressure is widely varied from 30mTorr to 90mTorr to change the number of neutrals which act as the polymerizing species. Film morphology is investigated by the scanning electron microscopy and perfect pore sealing is observed at 90mTorr on 56% porosity film.

F6.8

Diffusion of Metals in Nanoporous Dielectrics. Oscar Rodriguez, Ravi Saxena, Woojin Cho, Ravi Achanta, Joel Plawsky and William N Gill; Chemical Engineering, Rensselaer Polytechnic Institute, Troy, New York.

This work is aimed at understanding the nature of the interactions between metal interconnects and dielectrics (dense and nanoporous) in integrated circuits. The mechanism for metal diffusion and charge injection and its dependence on porosity, pore size, surface area and surface chemistry of the dielectric is discussed. Electrical testing of MOS capacitors is used to assess charge injection and Cu diffusion in the dielectric in the presence of an electric field. A quantitative analysis of Cu drift in dense and nanoporous dielectrics that reveals the role of Cu ions in the degradation and breakdown of the dielectric is presented. The concentration of injected Cu ions in the dielectric is characterized as a function of temperature, electric field and bias hold time. We have found that surface modification of nanoporous silica reveals the importance of chemically bounded or adsorbed water species in the dielectric and how they trigger metal diffusion. We propose that these water-related traps in the dielectric have two effects on metal diffusion: (a) they ionize the metal to form a non-stoichiometric oxide, which acts as the source of metal ions for diffusion; this is a crucial step since the metal needs to be ionized to respond to an external electric field; and (b) water-related traps in the dielectric are generated by the action of the external electric field and once generated they create space charged regions where the local electric field exceeds the external applied field by a few orders of magnitude, which enhance metal charge injection. The relationship between moisture uptake and porosity and pore size in nanoporous dielectrics is presented and correlated to metal charge injection. In dense dielectrics the presence of hydrogenous and hydroxyl-related species can be quantified from the hysteresis effect in the CV curves. A physically-based mathematical model of diffusion through dense and nanoporous solids has been developed considering bulk and surface diffusion and different concentration of water-related traps. The nonlinear effect of having a varying electric field, which depends on the ionic environment in the dielectric, has been included and the mechanism of Cu oxidation and diffusion through the dielectric is

discussed. The upper limit of Cu diffusivity in nanoporous silica is estimated, and the model simulates the current observed during BTS testing reasonably well.

F6.9
Pore Structure Determination and the CMP Performance of a Spin-On Porous Low-k Film Created with a Meso-Templating Technique. Wen-li Wu[1], Youfan Liu[2,3], Brendan Foran[2], Hae Jeong Lee[1] and Bryan Vogt[1]; [1]Polymers Division, NIST, Gaithersburg, Maryland; [2]International Sematech, Austin, Texas; [3]Intel, Hillsborough, Oregon.

A methylsilsesquioxane (MSQ)-based porous spin-on dielectric film produced using a mesoscale-templating scheme containing tubular structural units has been evaluated for advanced interconnect applications. The film structure was determined quantitatively with a combination of small-angle neutron scattering (SANS), specular X-ray reflectivity (SXR) and transmission electron microscopy (TEM). The tubular pores were found to align along both the free surface as well as the film/substrate interface. The number of surface aligned layers could be determined non-destructively from SXR results, which agreed with observations from cross sectional TEM. Other structural information, including porosity, average pore diameter and the density of the matrix material were also determined. The possible connection between the layered structure of the film and the cohesive failure of this film type during chemical-mechanical polish (CMP) process will be discussed.

F6.10
Fundamental Limits for 3D Wafer-to-Wafer Alignment Accuracy. Markus Wimplinger[1], Jian-Qiang (James) Lu[2], Jian Yu[1], Yongchai Kwon[1], Thorsten Matthias[3], Timothy S. Cale[1] and Ronald J. Gutmann[1]; [1]EV Group Inc., Phoenix, Arizona; [2]Focus Center - New York, Rensselaer: Interconnections for Hyperintegration, Rensselaer Polytechnic Institute, Troy, New York; [3]EV Group Inc., Schaerding, Austria.

Fundamental Limits for 3D Wafer-to-Wafer Alignment Accuracy M. Wimplinger, J.-Q. Lu*, J. Yu*, Y. Kwon*, T. Matthias**, T.S Cale*, and R.J. Gutmann* EV Group Inc., 3701 E. University Dr., Phoenix, AZ 85034 *Rensselaer Polytechnic Institute, 110 8th Street, Troy, NY 12180 ** EV Group, E. Thallner Str. 1, 4780 Schaerding, Austria luj@rpi.edu Wafer-level three-dimensional (3D) integration as an emerging architecture for future chips offers high interconnect performance by reducing delays of global interconnects and high functionality with heterogeneous integration of materials, devices, and signals. Various 3D technology platforms have been investigated, with different combinations of alternative alignment, bonding, thinning and inter-wafer interconnection technologies. Precise alignment on the wafer level is one of the key challenges affecting the performance of the 3D interconnects. After a brief overview of the wafer-level 3D technology platforms, this paper focuses on wafer-to-wafer alignment fundamentals using test structures. Particularly, correlation of misalignment with starting wafer properties such as bow, coefficient of thermal expansion (CTE), run-out of die placement over the wafer and topological features are presented. In addition to the alignment accuracy achieved prior to bonding, the impacts of wafer bonding and subsequent wafer thinning will be discussed. Key techniques to improve the alignment accuracy will be proposed, based on the understanding of alignment issues gained from the data.

F6.11
Optical Interconnect Components for Wafer Level Heterogeneous Hyper-Integration. Peter D. Persans, M. Ojha, R. Gutmann, J.-Q. Lu, A. Filin and J. Plawsky; Rensselaer Polytechnic Institute, Troy, New York.

Future computer chips will include novel components that may include quantum spin state, quantum dot, magnetic, and/or magneto-optic components, some of which may be based on molecular-scale structures. It is likely that these components will be integrated with CMOS-like drivers and with significant portions of the chip based on CMOS manufacturing technologies. Connection to, or reading of, some of these components will be facilitated by direct optical interaction. High-speed communication off the chip will also be facilitated by integrating optics onto the chip. Here we describe optical waveguides for three-dimensionally stacked chip fabrication technologies, in which optical connection between layers plays a central role. We will address CMOS-compatible approaches to optical via and waveguide fabrication. Detailed modeling is used for design optimization and also addresses how manufacturing variations from ideal design may affect device performance.

F6.12
The Study of Modified Layers in Porous Dielectrics Formed by Plasma Interactions. Marcus Andre Worsley[1], Stacey Bent[1], Stephen Gates[2], Nicholas Fuller[2] and Timothy Dalton[2]; [1]Chemical Engineering, Stanford University, Stanford, California; [2]T.J. Watson Research Center, IBM, Yorktown Heights, New York.

Integration of new low-k interlayer dielectrics (ILD) with current damascene schemes is a continuing issue in the chip manufacturing industry. During integration of the ILD, processing steps such as etch, resist strip and chemical-mechanical planarization are known to chemically alter a layer of the dielectric. Here, porous and non-porous organosilicate glass films (OSG) are investigated. Both spectroscopic ellipsometry and XPS are used to characterize the modified layer of the OSG film after exposure to O_2 or H_2 resist strip plasmas. The effects of the two types of plasma etch chemistry on the formation of the modified layer were studied and found to differ significantly. These effects include both the degree of modification (i.e. chemical composition) and depth of modified layer. A key difference between the O_2 and H_2 plasma is the fact that Si-H_x is present in the modified layer after exposure to H_2 plasma but not after exposure to the O_2 plasma. In addition, the influence of OSG porosity on the etch rate and modified layer thickness was investigated for porosities ranging from 0-40%. The etch rate was found to increase rapidly with porosity. Finally, conditions including relative gas flows and substrate temperature for the H_2 plasma were varied. These parameters produced considerable changes in the chemistry of the modified layer, especially in the amount of hydrogen incorporated into the film. Details of these results will be discussed in the context of the mechanism by which modification and etching occurs. The effects of process variables on the mechanism will also be discussed.

F6.13
Effect of Porosity on the Properties and Processability of Low k Dielectrics. Ananth Naman[1], Teresa a Ramos[2], Anil Bhanap[1], Anna Camarena[1], Yohannes Negga[1] and Rob Roth[2]; [1]Honeywell Electronic Materials, Sunnyvale, California; [2]Nanopore Incorporated, Albuquerque, New Mexico.

The need for lower dielectric constant materials for use as intermetal and interlevel dielectrics is well-known in the semiconductor industry. The adoption has been well delayed compared to the ITRS forecast due to difficulties in integrating them into established BEOL process flows. In this work, we present a systematic evaluation of the effect of porosity on the NANOGLASS family of materials. NANOGLASS offers the unique opportunity to tailor the porosity between 3.0 and 2.0 but maintaining the same polymer backbone. Predictably, increases in porosity lead to linear decrease in both dielectric constant as well as elastic modulus. The impact on porosity is not fully understood until these materials are used to build single level damascene interconnect structures. Integration issues such as the adhesion to adjoining layers is shown to also degrade. Additionally, the porous material shows much higher permeability resulting in higher moisture uptake along with higher susceptibility to damage during plasma processing such as RIE and ashing. The news however is not all bad. Development of adhesion promotion materials along with toughening agents have proved that integration of materials with dielectric constants as low as 2.0 can be possible. Blanket film properties will be discussed with responses of interest being optical, electrical, thermal, mechanical, and elemental. In addition, single level damascene structures will be shown to demonstrate actual use in a typical integration process flow.

F6.14
Characterization and Properties of MesoELK Low-k Dielectric Thin Films. Steven Gerard Mayorga[1], Lee A Senecal[1], Scott J Weigel[2], James E Mac Dougall[2], John F Kirner[2], Thomas R Gaffney[1] and Kelly A. Chandler[1]; [1]Schumacher, Carlsbad, California; [2]Air Products and Chemicals, Inc., Allentown, Pennsylvania.

Properties of SOD low-k dielectric thin films were investigated as a function of formulation and processing variables. Formulation variables investigated included siloxane content, porogen type and porogen content. Formulations were shown to have excellent shelf life stability under standard storage conditions. All films were processed under low temperature (< 400C), short duration (< 3 min.) cure conditions. Film post-treatment resulted in substantially improved mechanical properties. Physical, mechanical and electrical properties of films are reported. Using these techniques, films with a dielectric constant of 2.2 and an elastic modulus of 5.6 GPa were obtained, while maintaining an average pore size of 3 nm with a narrow distribution. In addition, films exhibited excellent film thickness uniformity, high adhesive strength and were successfully integrated into a dual-damascene copper integration scheme.

F6.15
Investigation of the Interfacial Adhesion and its Correlation with Chemical Mechanical Polishing for Various Low-k and Cu-low k Multi-layered Thin Films.
Parshuram Balkrishna Zantye[1,2], Arun Sikder[2] and Ashok Kumar[1,2]; [1]Department of Mechanical Engineering, University of South Florida,

Tampa, Florida; [2]Nanomaterials and Nanomanufacturing Research Center, University of South Florida, Tampa, Florida.

There is increasing implementation of low k materials as inter layer dielectrics (ILD) and multilevel metallization schemes using Cu-low k single and dual damascene structures to reduce the RC (Resistance X Capacitance) delay in modern day Integrated Circuits (IC). The inherently soft ultra low dielectric constant materials have weak interfacial adhesion with the other constituent thin films of the Cu damascene structure. The failure of the interface gives rise to the defects and delamination when these materials are subjected to Chemical Mechanical Polishing (CMP). Estimation of interfacial adhesion energy is done using the four-point bend test. In this research, after having done the four point bend test, we have performed nano-scratch testing with the three sided diamond Berkovich tip on the candidate low k and Cu-low k systems using the CETR universal bench top tribometer. The mathematical correlation between the interfacial energy obtained using the four-point bend test and scratch testing was established. The results of four point bend and scratch testing were then correlated with the CMP behavior of these materials under predetermined CMP conditions. The objective of the entire research is to establish an efficient pre-CMP interfacial energy estimation module to reduce the process developmental delay to solve the delamination problem.

F6.16

Evaluation of Thin Dielectric-Glue Wafer-Bonding for Three-Dimensional Integrated Circuit-Applications.
Yongchai Kwon, Jian Yu, Jay J McMahon, Jian-Qiang Lu, Timothy S Cale and Ronald J Gutmann; Focus Center - New York, Rensselaer, Rensselaer Polytechnic Institute, Troy, New York.

Wafer level monolithic three-dimensional (3D) integration is an emerging technology to increase the interconnect performance and functionality of future integrated circuits (ICs). In our approach, wafer bonding using benzocyclobutene (BCB) glue of 2.6 micron thickness has been used as a key process step. Reducing the thickness of the BCB lowers the inter-wafer via aspect ratio, which is desirable for future applications. However, thickness reduction may result in decrease of the fraction of bonded area and weak adhesion at the BCB interface, which are discussed in this manuscript. The fraction of bonded area and the adhesion energy are evaluated by optical inspection and four-point bending, respectively, for BCB thicknesses between 0.4 micron and 2.6 micron. A threshold BCB thickness for void-free bonding with sufficient adhesion strength (e.g., more than 10 J/m$\hat{\{2\}}$) is not fixed, but depends on the chip fabrication process and the interfacial chemistry. Systematic bonding experiments are conducted by varying material on the substrate surfaces (e.g., silicon, silicon oxides, silicon nitride, and non-TCE matched glass), BCB thermal processing steps, and thermal cycling to determine the dependence of threshold BCB thickness on these critical parameters. Those evaluation results will be discussed.

F6.17

Mechanical Properties of Low-k CDO Materials Prepared by Plasma Enhanced Chemical Vapor Deposition. Dong Niu, Qingguo Wu, Ananda Bandyopadhyay, Haiying Fu and David Mordo; Novellus Systems, Tualatin, Oregon.

As the interconnect design continues to shrink, the back end of the line (BEOL) technology encounters severe challenges due to increasing signal propagation delay and crosstalk among metal lines situated in close proximity. To minimize above effects, significant efforts are being made to develop low dielectric constant (low k) material, such as carbon doped oxide (CDO), that can be aptly used as interlayer dielectrics for 90nm and 65nm technology nodes. The current method for the development of low-k CDO film primarily relies on the incorporation of methyl group (-CH3) in the Si-O matrix. However, this approach adversely affects the mechanical properties of the CDO film, thus elevating adhesive and cohesive failures in the Cu-low k integrated structure. Consequently, a tradeoff has to be made between the k value and the mechanical strength of the bulk CDO film. Herein, we report the results of our studies directed toward obtaining improved mechanical properties of CDO film deposited by using plasma enhanced CVD method. Various properties of as-deposited films, including k, stress, hardness, modulus, and cracking behavior, have been extensively studied to achieve deeper understanding of their interdependence. In addition, their correlation with film composition and structure has been researched. With appropriate optimization of film deposition conditions, the mechanical strength and the cracking resistance of CDO film are dramatically improved without sacrificing its dielectric constant.

F6.18

Chemical Routes to Improved Mechanical Properties of PECVD Low K Thin Films. Steven Bilodeau, Alexander S Borovik, Abigail A Ebbing, Daniel J Vestyck, Chongying Xu, Jeffrey F Roeder and Thomas H Baum; ATMI, Danbury, Connecticut.

Increasing the elastic modulus and hardness of low K films addresses one of the key challenges towards integration of these materials into future integrated circuits. Several approaches are under consideration for increasing the hardness of CDO dielectrics. We have evaluated a variety of low K precursors their mixtures specifically chosen to enhance the hardness and modulus of CDO films through chemically induced cross-linking. FTIR spectroscopy shows that these precursors increase the amount of Si-CH_2-Si bonding in the deposited films. This has been observed to result in improved film hardness and modulus at relatively low deposition temperatures. For the hardener alone we have measured film hardness and modulus of 2.5 GPa and 14.5 GPa for a deposition temperature of 300°C. For tetramethylcyclotetrasiloxane (TMCTS) with 25% hardener we have observed film hardness and modulus as 1.4GPa and 8.8GPa, respectively, for a deposition temperature of 180°C. These film properties are significantly higher that we have observed for TMCTS alone under similar deposition conditions. We believe that the increased hardening at low deposition temperatures is particularly useful for ULK approaches that use thermally sensitive porogens.

F6.19

Abstract Withdrawn

F6.20

Measurement of Pore Size and Matrix Characteristics in Low-k Dielectrics by Neutron Contrast Variation.
Ronald C Hedden[1], Barry J Bauer[2], Hae-Jeong Lee[2], Christopher L Soles[2], Wen-Li Wu[2] and Eric K Lin[2]; [1]Materials Science and Engineering, Penn State University, University Park, Pennsylvania; [2]Polymers Division, NIST, Gaithersburg, Maryland.

We have recently applied small-angle neutron scattering (SANS) contrast variation to probe the structure of nanoporous low-k thin films. Using a flow-through sample cell for SANS, samples are exposed to saturated solvent vapor in air, whereby the pores fill with liquid by capillary condensation. The pores are filled with mixtures of hydrogen and deuterium containing solvents to vary the neutron contrast with the matrix (wall). The composition of the solvent mixture is systematically varied to identify a composition that minimizes the scattered intensity (contrast match point). From the contrast match point composition, film characteristics including matrix density and homogeneity are assessed. Previously, we applied SANS contrast variation to characterize four spin-on low k materials including a methylsilsesquioxane (MSQ), an organic polymer, a xerogel, and a hydrogensilsesquioxane (HSQ). Calculated matrix mass densities were comparable to independent density measurements obtained by an established specular X-ray reflectivity (SXR) technique. We found no evidence of "closed pores," defined as pores inaccessible to the probe solvent, in any of the materials studied. Our recent work has combined SANS contrast variation with capillary porosimetry, creating a new approach to the determination of pore size distributions. Capillary porosimetry experiments are conducted using solvent vapor of the contrast match point composition. The solvent partial pressure P is varied incrementally from zero to Po (where Po = saturated vapor pressure) at constant temperature. As P is increased, pores fill with liquid solvent in order from smallest pores to largest. The SANS measurement quantifies the correlation length within the material as different populations of pores are filled with the contrast match fluid. The SANS contrast match experiment is more powerful if the volume fractions of solvent-filled and "empty" pores are known at each value of P. The uptake of solvent at each partial pressure P can be accurately measured by SXR. Combining size information from SANS with solvent uptake from SXR characterizes the pore size distribution directly without the need for a thermodynamic model for adsorption.

F6.21

SANS characterization of mesoporous materials using contrast match method. Bryan D Vogt[1], Hae-Jeong Lee[1], Ronald C Hedden[1,3], Christopher L Soles[1], Wen-li Wu[1], Eric K Lin[1], Barry J Bauer[1], Rajaram Pai[2] and James J Watkins[2]; [1]Polymers Division, NIST, Gaithersburg, Maryland; [2]Department of Chemical Engineering, University of Massachusetts, Amherst, Massachusetts; [3]Department of Materials Science and Engineering, Pennsylvania State University, College Park, Pennsylvania.

The pore structure of thin mesoporous silica films have been characterized using a small angle neutron scattering SANS) porosimetry technique. The films were synthesized via a CO₂-based infusion process using block copolymers containing hydrophilic and hydrophobic domains as the mesopore template. The nature of the process allows for adjustment of the composition of the framework of the mesoporous structure. Structures containing various levels of carbon in the framework as well as pure SiO₂ were prepared by the selection of an appropriate precursor or mixtures of precursors. SANS porosimetry exploits the

partial pressure dependence of capillary condensation of a probe molecule within a pore on the pore size. Therefore, changes in the scattering profile as a function of partial pressure can be directly related to the pore structure. For ease of data analysis, a contrast match solvent is used as the probe molecule. To create a contrast match solvent for the porous films, the scattering profiles of the films were collected under a series of saturated solvent environments composed of deuterated and protonated toluene. At a concentration of approximately 40 % (v/v) deuterated toluene, all the coherent scattering from the sample was eliminated, indicating a contrast match point. At this point, the scattering length density of the wall material equals that of the solvent, which can be used to determine the wall mass density with knowledge of the wall material chemical composition. The presence of a match point indicates that (1) all the pores are accessible to the toluene vapor and (2) the wall material is homogeneous. The pore structure is then determined by varying the relative partial pressure of the contrast match solvent from 0 to 1. In the case of all empty pores (p/p_o = 0), the scattering profile contains two distinct structures; a strong Bragg peak corresponding to the mesopores templated by the block copolymer and a Debye-type scattering corresponding to disordered micropores with an average dimension of approximately 11 Å. These micropores are likely a result of the interpenetration of the silica network and the hydrophillic domains of the block copolymer. Analysis of films synthesized in the same manner as the mesoporous sample, but using a homopolymer template of the same chemical composition as the hydrophilic domain in the block copolymer template supports this view. In the case of the homopolymer template, disordered micropores with the same dimension were observed.

F6.22

Characterization of PECVD Low-k Films by Positronium-Annihilation Lifetime Spectroscopy (PALS).
Toshiyuki Ohdaira[1], Ryoichi Suzuki[1], Yoshimi Shioya[2] and Kazuo Maeda[2]; [1]Photonics Research Institute, National Institute of Advanced Industrial Science and Technology, Tsukuba Ibaraki, Japan; [2]Semiconductor Process Laboratory co., Ichikawa Chiba, Japan.

Positronium annihilation lifetime spectroscopy (PALS) was used to measure pore (free volume) size distributions in SiOCH films for low-k ILD and Cu diffusion barriers, which were grown by PECVD with source gas of HMDSO(hexamethyldisiloxane).In the PECVD, the dielectric constant(k) of the film changes with the deposition conditions such as gas flow rate, pressure, temperature, RF power, etc. The PALS results showed that the PECVD-grown SiOCH films with k in the range from 2.6 to 4 contain pores with average sizes from 0.4 to 1.2 nm, and that the k value of the film correlates with the pore size. PALS depth profiling was also carried out for the SiOCH films with various beam irradiations.

F6.23

Morphology and Physical Properties of Hybrid Materials based on Novel Poly(methyl phenylsilsesquoxanes.
Soon Man Hong, Seung Sang Hwang, Kwang Ung Kim, Hangseok Lee, Cheol Chung and Sungwon Ma; Polymer Hybrid Center, Korea Institute of Sience & Technology(KIST), Seoul, South Korea.

Inorganic/organic hybridization based on polyorganosilsesquioxane(PSSQs) has greatly attracted scientific and industrial interests because of excellent optical transparency and low refractive index of inorganic polymer. The organic dispersed inorganic matrix would be applied to innumerable industrial fields such as microelectronic packaging insulators, optical devices, liquid crystal display elements and coating materials. We synthesized novel polymethylphenylsilsesquioxane(PMPSQ), used as matrix resin. We synthesized Poly(D,L-lactide), Poly(D,L-lactide-co-e-caprolactone) and Poly-D, L-lactic acid-1,6-hexanediol (PDLLA-1,6-hexanediol), used as poragen materias. Prepared inorganic/organic hybrids are investigated in terms of nano-scaled morphology by AFM (Atomic Forced Microsocopy) and TEM (Transmission Electron Microscopy). The hybrids exhibit excellent film coatability, adhesion, and planarity. Nanofoaming process was carried out at optimized conditions. The characteristics of nanofoamed PMPSQ thin films based on polymethylphenylsilsesquioxane(PMPSQ) and Poly(D,L-lactide), Poly(D,L-lactide-co-e-caprolactone) and Poly-D, L-lactic acid-1,6-hexanediol (PDLLA-1,6-hexanediol) are studied by thermal behaviors, morphologies and dielectric properties.

F6.24

Electrical and Thermal Stability of Molecularly Templated Nanoporous Silica Dielectrics for Cu Metallization.
Jr-Yu Chen[1], Fu-Ming Pan[1,2], Li Chang[1], An-Thung Cho[2] and Kuei-Jung Chao[3]; [1]Materials Science and Engineering, National Chiao Tung University, Hsinchu, Taiwan; [2]National Nano Device Laboratories, Hsinchu, Taiwan; [3]Chemistry, National Tsing Hau University, Hsinchu, Taiwan.

Nanoporous silica thin films are believed to be a potential candidate for intermetal dielectrics for sub-70 nm technology nodes due to their ultra-low dielectric constants (k < 2.0) and chemical compatibility with modern ULSI process technologies. The as-prepared nanoporous silica films are usually hydrophilic, and, therefore, needed to be chemically modified to improve the hydrophobicity so that stable dielectric properties can be obtained. Trimethylsilylation is a common method to enhance hydrophobicity of porous silica films. However, trimethylsilyl groups thereby created in the porous film may be destroyed during the subsequent IC processes, causing reliability problems. In this work, thermal and dielectric stabilities of surfactant templated nanoporous silica films exposed to hexamethyldisilazne (HMDS) vapor, have been studied. Hydrophobicity of the as-calcined nanoporous silica films spin-coated on Si wafers was significantly improved by the trimethylsilyl treatment. The nanoporous silica thin films have a pore size of 4 nm, and a k value smaller than 2 after the trimethylsilylation treatment. Thermal desorption spectroscopy (TDS), Fourier transformation infrared spectroscopy (FTIR) and Auger electron spectroscopy (AES) indicate that trimethylsilylated nanoporous silica films are stable up to 450°C. The films are stable over 50 days in terms of the dielectric and chemical properties. However, the trimethlsilylated nanoporous silica films suffer obvious degradation in chemical structure when the anneal temperature are over 600°C. This was revealed by the Si-O-Si stretching absorption mode and the thermal desorption signal of methyl groups. For a film stack of Cu, Ta(N) and the nanoporous silica film, delamination between layers was not observed after the anneal at 600°C. However, nano-sized tantalum carbide particle was found to be present at the interface between the nanoporous film and the Ta(N) diffusion barrier layer. Little metal ions were detected in the nanoporous dielectric under electrical stress test. The results show that trimethylsilylated nanoporous silica films have superior thermal and electrical stabilities, and may be integrated into dualdamascene architecture.

F6.25

Three Dimensional Interconnect Stress Modeling for Back End Process.
Xiaopeng Xu and Victor Moroz; TCAD R&D, Synopsys, Inc., Mountain View, California.

In modern integrated circuits, interconnects consist of multilevel metal lines that are embedded within dielectric insulators and separated by diffusion barriers above the silicon transistors. The back end process for interconnect fabrication includes material deposition and etching steps at room temperature and elevated temperatures, and temperature ramps in between. Stresses are generated during the temperature ramps due to thermal expansion mismatches of different materials and during deposition steps due to intrinsic formation process. These stresses are relaxed in the meantime due to viscous deformations of the low k dielectric insulators and diffusion barriers, and they are redistributed during deposition and etching steps due to the rebalance of forces. The stress levels in the interconnects depend on the temperature ramping history, the evolution of constrains from surrounding viscous materials, and the geometry changes due to deposition and etching steps. The evolution of constrains and geometry changes are three dimensional in nature. The residual stresses in interconnects are known to cause yield and reliability issues and it has been a major effort to develop stress models for back end processes. Historically, interconnect stresses are modeled with various assumptions. For example, 2D plane strain or 2D axisymmetric simplifications are made for a 3D structure; viscous relaxations in low k dielectric insulators are ignored; and ad hoc numerical treatments are introduced to activate and deactivate elements in the mesh for deposition and etching of materials. Stress simulations with such assumptions become increasingly inadequate to predict stress distributions inside interconnects that are fabricated with complex back end process flows. In this study we use our three-dimensional process simulator Taurus-Process to simulate the stress evolution for the entire interconnect fabrication process flow. No ad hoc assumptions regarding stress states are required during region additions and removals. Intrinsic stresses from material formation, thermal mismatch stresses from temperature ramps, stress relaxations from viscous deformation, and stress profile redistribution from deposition and etching are all considered at every process step by solving stress equilibrium equations with evolving boundary conditions. Parametric studies are carried out to examine the effects of intrinsic stress, process thermal budgets, layout variation, viscous flow and material selection. Full stress evolution histories are obtained for all components in the interconnect structure. A TCAD assisted design approach is suggested for lowering stress levels of relevant stress components. The implications of the stress modeling results on reliability issues like stress voiding are discussed.

F6.26

Thermomechanical Stresses in Copper Interconnect/Low-k Dielectric Systems.
Y.-L. Shen, Mechanical Engineering, University of New Mexico, Albuquerque, New Mexico.

This study is devoted to thermomechanical stresses and their modeling in copper interconnects. Constitutive behavior of encapsulated copper films is first determined by experimentally measuring the stress-temperature response during thermal cycling. The material model is subsequently used for predicting stresses in copper interconnect/low-k dielectric structures using finite element analyses. Various combinations of oxide and polymer-based low-k dielectric schemes are considered. The evolution of stresses and deformation pattern in the dual-damascene copper, barrier layers, the dielectrics and their interfaces is seen to have direct connections to the structural integrity of contemporary and future-generation devices. In particular, stresses experienced by the thin barrier layers and the mechanically weak low-k dielectrics are critically assessed. Salient features are compared with those in traditional aluminum interconnects. Practical implications in reliability issues such as voiding, interface delamination, electromigration and dielectric failure are also discussed.

F6.27
Near-Field Acoustic Holography: A Novel Probe for Sub-Surface Nanoscale Nondestructive Imaging of Soft, Hard and Hybrid Structures. Gajendra S Shekhawat[1] and Vinayak P Dravid[2]; [1]Institute for Nanotechnology, Northwestern University, Evanston, Illinois; [2]Material Science and Engineering, Northwestern University, Evanston, Illinois.

We have developed a near-field ultrasonic holography (NFUH) system which combines the nanometer-scale spatial resolution of conventional scanning probe microscopes (SPMs) with the surface and sub-surface imaging capabilities. In NFUH, a high frequency (500 KHz) acoustic wave is launched from the bottom of the specimen and another one is launched on AFM-type cantilever but at a slightly different frequency. The speciment acoustic wave interacts with feature/defects in the specimen and subsequently interferes with the cantilever "reference" wave. The very local and, sub-surface acoustic interference is then measured and analyzed by the scanning probe tip as an "antenna". The resultant measurement can be readily split between the phase and amplitude part of the local interference, lending remarkable useful information about the "internal" structure of specimen. This technique will fill a critical void in characterization and investigation of the static and dynamic mechanics of nanoscale systems , ranging from engineering system to biologically active structures, in-vitro. In the presentation, we will report our results on high resolution sub-surface imaging copper vias (without doing any cross-sectioning) and in-vitro biological structures (e.g. looking through the cell-membrane, implant-bio interfaces etc.) at acoustic carrier frequency of 2 MHz. It will be argued that ramping the cantilever frequency to 100 MHz would enable the extraction of sub-surface defects (voids, delamination, cracks and etc.) with Z height resolution (defect
height) of $<$ 5 nm, while maintaning the high spatial resolution of SPM.

SESSION F7: Copper Reliability
Chairs: Christine Hau-Riege and Stefan Hau-Riege
Thursday Morning, April 15, 2004
Room 2003 (Moscone West)

8:30 AM *F7.1
Circuit-Level Assessments of the Reliability of Copper-Based Metallization. Carl V. Thompson, M.I.T., Cambridge, Massachusetts.

The metallization of integrated circuits consists of complexly connected segments between nodes. Nodes include vias and junctions at which segments join other segments, either in the same level of metallization or in other levels of metallization. Most strategies for circuit-level reliability assessments are based on analyses of segments that are treated as independent fundamental reliability units. However, as has now been shown for both Al-based and Cu-based metallization, the reliability of a segment depends on the numbers, types, and stress conditions of neighboring segments, so that segment-based circuit-level reliability assessments give projections that are neither consistently conservative nor optimistic, and in fact have no usefulness. When vias fully block electromigration, interconnect trees can be defined as independent fundamental reliability units and can be used as the basis for accurate circuit-level reliability assessments. Interconnect trees are a collection of connected segments that are bound by segments that terminate at vias. Significant differences in the reliability of Cu-based and Al-based interconnect trees have now been identified, so that it has been necessary to develop a modified tree-based strategy for circuit-level reliability assessments. This alternative strategy will be described, along with its implementation in circuit-level reliability analyses using a new tool SysRel, which has been developed for this purpose. This tool permits assessment of the impact of critical assumptions on reliability assessments, and can guide the development of technology improvements that will have the greatest impact on circuit-level reliability.

9:00 AM F7.2
Mortality Dependence of Cu Dual Damascene Interconnects on Adjacent Segments. Choon Wai Chang[1], Chee Lip Gan[2,1], Carl V. Thompson[3,1], Kin Leong Pey[2,1], Wee Kiong Choi[4,1] and Nam Hwang[5]; [1]Advanced Materials for Micro- & Nano-Systems, Singapore-MIT Alliance, Singapore, Singapore; [2]Material Science & Engineering, Nanyang Technological University, Singapore, Singapore; [3]Material Science, Massachusetts Institute of Technology, Cambridge, Massachusetts; [4]Electrical & computer, National University of Singapore, Singapore, Singapore; [5]Micro-Module Component, Institute of Microelectronics Singapore, Singapore, Singapore.

Different values of critical current-density line-length product $(jL)_{cr}$ for Cu interconnects, below which the interconnects are immortal, have been reported. We report studies of the mortality conditions in interconnect segments connected to active and inactive adjacent segments. Experiments were carried out on straight via-terminated lines with an additional via in the middle that creates two segments with 25 μm lengths ("dotted-I" structures). The test structures were in metal 2 and connected to metal 1 leads in "via-below" configurations. The current density in the right segment was kept constant at 0.5 MA/cm^2 with the electrons flowing from the right via towards the middle via, while the current density in the left segment was varied from 0 to 2.5 MA/cm^2, with electrons flowing in both directions. All the samples were stressed for 780 hours and the failure criterion was set as 30% resistance increment. Due to the low failure rate of the samples, comparison between the different test conditions was done using the failure percentage instead of t_{50}. Mortalities were found in the dotted-I right segment with a jL value as low as 1250 A/cm compared to the lowest reported $(jL)_{cr}$ of 1500 A/cm. Moreover, we found that the mortality of a dotted-I segment is dependent on the direction and magnitude of the current in the adjacent segment. The failure percentage of the right segment reduces with the current density when the electrons flow in the same direction in the left segment. It increases with current density when the electrons flow in the opposite direction, with the lowest failure percentage corresponding to about 0.35 MA/cm^2 in opposite direction. For the cases in which the left segments have a current density of 1.5 MA/cm^2 or 2.5 MA/cm^2, flowing in the same direction as the right segment, over 40% of these samples' right segments failed earlier than the left segments, even though the current densities in the left segments were higher. These results suggest that there is not a definite value of the jL product that defines true immortality in individual segments that are part of an interconnect tree. Moreover, the critical jL value for a single segment of Cu interconnects may be reduced or increased by an adjoining segment. Therefore independently determined $(jL)_{cr}$ values cannot be directly applied to interconnects with branched segments, but rather the magnitude as well as the direction of the current flow in the adjoining segments must be taken into consideration in evaluating the immortality of particular interconnects.

9:15 AM F7.3
Unexpected Mode of Plastic Deformation in Thin Films Undergoing Electromigration. Arief S. Budiman[1], N. Tamura[2], B. C. Valek[1], K. Gadre[3], J. Maiz[3], R. Spolenak[4], W. A. Caldwell[2], A. A. MacDowell[2], R. S. Celestre[2], H. A. Padmore[2], J. C. Bravman[1], B. W. Batterman[2,5], W. D. Nix[1] and J. R. Patel[1,2]; [1]Materials Science & Engineering, Stanford University, Stanford, California; [2]Advanced Light Source (ALS), Lawrence Berkeley Laboratory (LBL), Berkeley, California; [3]Intel Corporation, Hillsboro, Oregon; [4]Max-Planck-Institut fur Metallforschung, Stuttgart, Germany; [5]SSRL/SLAC, Stanford University, Stanford, California.

An early (pre-failure) mode of plastic deformation was previously reported during in-situ x-ray micro-diffraction experiments on electromigration (EM) in the Al(Cu) system. Similar observations on passivated lines of damascene Cu interconnects during electromigration are described in this paper. During in-situ electromigration studies on Cu lines, streaking or broadening of Laue spots transverse to the direction of electron flow has been observed. Some broadening of Laue spots was detected at the anode end of the line and preliminary findings indicate that the bending of individual grains is convex. From the broadening we calculate the dislocation density in an individual grain while from the observed peak splitting in the broadened spot we can determine the tilt of small angle polygonization boundaries. The deformation geometry leads us to conclude that dislocations introduced by plastic flow lie predominantly in the direction of electron flow and provide additional easy paths for the transport of point defects. A qualitative model that can account for the observed phenomena is proposed. Since these findings occur long before any observable voids or hillocks are formed, they should have direct bearing on the final failure stages of EM.

9:30 AM F7.4
Coupling Between Precipitation and Plastic Deformation During Electromigration in a Passivated Al (0.5wt % Cu) Interconnect. Rozaliya I Barabash[1], Gene E. Ice[1], Nobumichi Tamura[2], Bryan Valek[3], John Bravman[3], Ralph Spolenak[5] and Jim Patel[4,2]; [1]Metals and Ceramics Div., Oak Ridge National Laboratory, Oak Ridge TN, Tennessee; [2]Advanced Light Source, Advanced Light Source, Berkeley, California; [3]Dept. Materials Science and Engineering, Stanford University, Stanford, California; [4]Stanford Synchrotron Radiation Laboratories, Stanford, California; [5]Max Planck Institut fur Metallforshung, Stuttgart, Germany.

The scaling of device dimensions with a simultaneous increase in functional density imposes a challenge to materials technology and reliability of interconnects. White beam X-ray microdiffraction is particularly well suited for the in-situ study of electromigration. The technique was used to probe microstructure in interconnects and has recently been able to monitor the onset of plastic deformation induced by mass transport during electromigration in Al (Cu) lines even before any macroscopic damage became visible. In the present paper, we demonstrate that the evolution of the dislocation structure during electromigration is highly inhomogeneous and results in the formation of unpaired randomly distributed dislocations as well as geometrically necessary dislocation boundaries. When almost all unpaired dislocations and dislocation walls with the density n are parallel (as in the case of Al-based interconnects), the anisotropy in the scattering properties of the material becomes important, and the electrical properties of the interconnect depend strongly on the direction of the electric current relative to the orientation of the dislocation network. A coupling between the dissolution, growth and diffusion of Al2Cu precipitaties and the electromigration-induced plastic deformation of grains in interconnect is observed.

10:15 AM *F7.5
Effect of mass transport along interfaces and grain boundaries on copper interconnect degradation.
Ehrenfried Zschech, Moritz Andreas Meyer and Eckhard Langer; Materials Analysis, AMD Saxony LLC & Co. KG, Dresden, Germany.

For leading edge microprocessors, both advanced process technologies and new combinations of materials bring new reliability challenges to on-chip interconnects: different interconnect microstructure, other types of interfaces and new degradation phenomena. Electromigration, stress-induced migration and mechanical weakness in case of low-k materials are reliability concerns for inlaid copper interconnects. In addition to standard reliability tests which allow statistically relevant conclusions, the study of degradation mechanisms for a limited number of representative samples is needed to understand process weaknesses and to exclude reliability-related failures in copper interconnects. We designed experimental setups to study reliability-limiting degradation mechanisms in interconnects in such a way that mass transport and interconnect degradation are visualized in-situ at fully embedded copper via/line test structures [1,2]. Depending on the interface bonding copper/etch stop layer and copper/barrier layer, voids are formed at one of the interfaces. Initial shallow voids remain at their position until a certain critical size is reached. The mass transport dominates along the weakest interface, i. e., the pathway with the highest transport rate, towards the end of the line. The discontinuous, step-like void movement process depends on the localization of grain boundaries. At the line end, the voids merge into a larger void which subsequently grows within the via. Once a large void, and consequently an inner surface, has been formed, the void growth process seems to be dominated by diffusion along inner surfaces. Since the diffusion rate is expected to be different for different crystallographic orientations of the grain next to the void, grains with different orientation are disintegrated at different speeds. It is an important observation from these in-situ SEM experiments that both the void movement along the copper line and the void growth in the via are discontinuous step-like processes. To make this time-dependent void evolution more visible, we have analyzed the projected void area from the SEM image for the via/line interconnect structure [3]. Combining the results of the in-situ SEM study with copper microstructure data based on EBSD, it can be clearly shown that void formation, growth and movement, and consequently interconnect degradation, depend on both the interface bonding and the copper microstructure of the inlaid copper structures. [1] M. A. Meyer et al., In Situ SEM Observation of Electromigration Phenomena in Fully Embedded Copper Interconnect Structures, Microelectronics Engineering 64, p. 375, 2002 [2] G. Schneider et al., Dynamical X-ray Microscopy Investigation of Electromigration in Passivated Inlaid Cu Interconnect Structures, Appl. Phys. Lett. 81, p. 2535, 2002 [3] E. Zschech et al., Failures in Copper Interconnects: Localiza-
tion, Analysis and Degradation Mechanisms, Proc. IPFA, in press, 2003

10:45 AM F7.6
Fatal Void Size Comparisons in Via-Below and Via-Above Cu Dual-Damascene Interconnects. Zung-Sun Choi[1], Chee Lip Gan[2,3], Carl V. Thompson[1,2] and Jung Hoon Lee[4]; [1]Materials Science and Enginnering, MIT, Cambridge, Massachusetts; [2]Singapore-MIT Alliance, NUS, MIT, Singapore, Singapore; [3]School of Materials Engineering, Nanyang Technological University, Singapore, Singapore; [4]Electrical Engineering and Computer Science, MIT, Cambridge, Massachusetts.

The median-times-to-failure (t50's) for straight dual-damascene via-terminated copper interconnect structures, tested under the same conditions, depend on whether the vias connect down to underlaying leads (metal 2, M2, or via-below structures) or connect up to overlaying leads (metal 1, M1, or via-above structures). Experimental results for a variety of line lengths, widths, and numbers of vias show higher t50's for M2 structures than for analogous M1 structures. It has been shown that despite this asymmetry in lifetimes, the electromigration drift velocity is the same for these two types of structures, suggesting that fatal void volumes are different in these two cases. A numerical simulation tool based on the Korhonen model has been developed and used to simulate the conditions for void growth and correlate fatal void sizes with lifetimes. These simulations suggest that the average fatal void size for M2 structures is about two to three times the size of that of M1 structures. This result supports an earlier suggestion that preferential nucleation at the Cu/Si3N4 interface in both M1 and M2 structures leads to different fatal void sizes, because larger voids are required to span the line thickness in M2 structures while smaller voids at the base of vias can cause failures in M1 structures. However, it is also found that the fatal void sizes corresponding to the shortest-times-to-failure (STF's) are similar for M1 and M2, suggesting that the voids that lead to the shortest lifetimes occur at or in the vias in both cases, where a void need only span the via to cause failure. Correlation of lifetimes and critical void volumes provides a useful tool for distinguishing failure mechanisms.

11:00 AM F7.7
Void Growth and Failure Statistics for Electromigration in 0.18 μm Cu Interconnects. M Hauschildt[1], S Thrasher[2], L Michaelson[2], R Hernandez[2], P Justison[2], M Gall[2], H Kawasaki[2] and P S Ho[1]; [1]Interconnect and Packaging Group, The University of Texas at Austin, Austin, Texas; [2]DigitalDNA Laboratories, Motorola, Austin, Texas.

The introduction of Cu and low-k dielectrics and continuing scaling of on-chip interconnects raise serious reliability concerns on electromigration (EM) and stress-induced voiding (SIV). EM lifetime statistics usually follow a lognormal distribution with the median lifetime depending on the quality of the interface, which controls the mass transport. The standard deviation σ is a key parameter for extrapolating EM lifetime under operating conditions, yet its origin is not well understood. In this study, we investigate EM failure statistics and the origin of σ for Cu interconnects by analyzing the statistics of EM lifetime and void size distributions at various stages during EM testing and their correlation to the grain size distribution. EM experiments were performed on 0.18 μm Cu test structures at 300°C and 1.5 MA/cm2 where tests were terminated after specific amounts of resistance increases for void growth analysis. To examine the statistical correlation of EM lifetime, void size and grain size distributions were analyzed in 0.18 μm Cu lines using focused ion beam and transmission electron microscopy. The lifetime and void size distributions were found to follow lognormal distribution functions with σ values of both data sets decreasing with higher percentages of resistance increase. Results on grain size analysis showed that σ decreases with the number of combined grains, but their values are larger than the corresponding values of EM lifetime and void size. This result suggests that geometrical factors related to the grain size distribution cannot account for the observed EM and void growth characteristics. Statistical factors governing the kinetics of mass transport for different grain interfaces have to be considered, together with the statistics of initial void formation and its effect on void morphology. The statistical correlation among these parameters is being evaluated using Monte Carlo simulations. Initial results indicate that void size distributions can indeed be simulated by considering geometrical variations of the void shape. Results will be reported.

11:15 AM F7.8
Stress-induced voiding in Cu/oxide interconnect structure.
Won-Chong Baek and Paul S. Ho; University of Texas at Austin, Austin, Texas.

Stress-induced voiding in Cu/oxide interconnect structure with 0.36 um via was investigated. Via chain structures composed of two metal levels with different linewidth connected by vias were used. Results show two kinds of void formation mechanisms depending on linewidth. In narrow line structures (linewidth = 0.44 um and via = 0.36 um), temperature dependence of resistance increase indicates a typical

behavior of stress-induced voiding with an activation energy of 0.75 eV, and peak rate at 240 °C. The activation energy is consistent with that of interfacial mass transport in Cu. Most of resistance increases aroused from void formation at the periphery of via bottom as FIB observations revealed. This phenomenon occurred at relatively low temperatures. However the resistance increase was small, so further study is needed to evaluate the influence of this type of stress-induced voiding on reliability. In wide line structure (linewidth = 2.0 um, via = 0.36 um), resistance increases did not follow the typical type of stress-induced voiding. The rate of void formation did not show a peak at an intermediate temperature. Instead, resistances continued increasing exponentially up to 350 °C. The activation energy was found to be 1.0 eV. Similar to narrow lines, most of resistance increases aroused from void formation in the lower metal lines. This phenomenon is significant at relatively higher temperatures, and at 350 °C, the resistance increase was four times as large as that of peak rate of narrow line stressmigration. Further study is underway to investigate this phenomenon.

11:30 AM F7.9
Effect of Dielectric Materials on Stress and Stress Induced Damages in Damascene Cu Lines. Jong-Min Paik[1], Hyun Park[1], Ki-Chul Park[2] and Young-Chang Joo[1]; [1]School of Material Science & Engineering, Seoul National University, Seoul, South Korea; [2]Advanced Process Development Project Team, System LSI Division, Samsung Electronics Co., Ltd., Young-In.

The effect of low-k materials on the stress and stress distribution in dual damascene Cu interconnects were studied using x-ray diffraction and three-dimensional finite element analysis. For this purpose, periodic line structures and via-line structures incorporating two different dielectric materials, tetraethyl orthosilicate (TEOS) and low-k materials, were investigated. Damascene Cu lines varied in width and spacing simultaneously were fabricated by controlling a lithography dose and measured the volume averaged stress of the lines using x-ray diffraction. For the case of the lines with TEOS which has a relatively low coefficient of thermal expansion (CTE) and a high elastic modulus, the each principle stress component varied as line spacing. On the other hand, the line spacing dependence on stress is not prominent in case of lines with CORAL which have higher CTE and very low Young's modulus. Using a three-dimensional finite element analysis, the stress and stress distributions of the via-line structures were calculated with two types of dielectrics. In the case of TEOS, large hydrostatic stress was concentrated at the via and the top of the lines, where it was suspected that the void should nucleate. On the other hand, in the via-line structures integrated with organic low-k materials, large von-Mises stress is maintained at the via, and thus the deformation of the via, rather than voiding, is the anticipated main failure mode. A good correlation between the FEM prediction and experimentally observed failure was obtained in the different dielectric materials. Based on experimental and simulated results, it was found out that stress-induced damages are caused by level and distribution of von-Mises and hydrostatic stress and grain structures of the lines which are related to vacancy diffusion path. From successive stress-migration tests, the optimized process condition and geometries of via-line structures to prevent stress induced damage are obtained.

11:45 AM F7.10
Characterization of the Copper Migration through Dielectric Materials during Bias Temperature Stressing by Capacitance-Voltage Measurement and the Numerical Analysis. Ki-Su Kim[1], Jang-Yeon Kwon[2], Young-Chang Joo[1] and Ki-Bum Kim[1]; [1]Materials Science and Engineering, Seoul National University, Seoul, South Korea; [2]Samsung Advanced Institute of Technology (SAIT), Yongin, Gyeonggi-do, South Korea.

The copper migration through inter-metal dielectric (IMD) materials is one of the serious problems in the reliability concerns for copper metallization. In order to develop the comprehensive model to describe the copper migration in IMD, the copper migration through IMD during bias temperature stressing (BTS) was investigated by capacitance-voltage (C-V), current-voltage (I-V), time-dependent dielectric breakdown (TDDB) measurements and the numerical analysis. Room temperature C-V measurement at 1 MHz was performed to measure the flatband voltage shift of Cu/dielectric material/Si capacitors during BTS at the electric field of 0.5 and 1.0 MV/cm and temperatures between 150 to 275°C. Previously, we developed the method to calculate the copper concentration in SiO_2 during BTS by one-dimensional finite differential method. Using this method and the experimental results, the flatband voltage shift of $Cu/SiO_2/Si$ capacitor, which is caused by migration of copper ions through SiO_2 during BTS, was investigated. The results by the numerical analysis showed a good agreement with the measured flatband voltage shift with BTS time. However, the diffusivity and the maximum solid solubility of copper in dielectric materials should be investigated for quantitative numerical analysis. The method to extract the copper diffusivities in dielectric materials using the numerically evaluated and the measured flatband voltage shift with BTS time was developed. In particular, copper diffusivities in thermally grown SiO_2, plasma-enhanced chemical vapor deposition (PECVD) SiO_2 and PECVD oxynitride were obtained as 2.22×10^{-3} exp $(-1.54eV/kT)$, 2.59×10^{-5} exp $(-1.18eV/kT)$ and 3.09×10^{-5} exp $(-1.34eV/kT)$ cm^2/s, respectively. It is thought that the present numerical method can be used to evaluate the copper diffusivity in various low-k dielectric materials with the C-V measurement of Cu/low-k dielectric material/Si capacitors during BTS. Finally, based on the results during BTS such as the evolution of copper concentration in dielectric materials by numerical analysis, conduction modes by I-V measurement, and time-to-failure (TTF) characteristics by TDDB measurement, two-stage model to describe the copper migration in dielectric materials was suggested.

SESSION F8: Metallization
Chairs: Manfred Engelhardt and Thomas Gessner
Thursday Afternoon, April 15, 2004
Room 2003 (Moscone West)

1:30 PM *F8.1
MEMS Metallization. Thomas Gessner[1,2], Andreas Bertz[1] and Knut Gottfried[2]; [1]Center for Microtechnologies, Chemnitz University of Technology, Chemnitz, Germany; [2]Micro Devices and Equipment, Fraunhofer Institute IZM, Chemnitz, Germany.

Today crystalline silicon is the dominant material for MEMS fabrication. Its usage is not limited to act as the base plate (substrate) but as the functional film or component too. The electrical resistivity of crystalline silicon can be varied in a wide range (0.005 up to 1000 Ohmcm) offering a large flexibility as MEMS material. However, from an application and technology point of view in certain cases metal films are to be used. For example for RF MEMS a resistivity as low as possible is desired in order to minimize electrical losses. Metals with a resistivity of a few 10e-6 Ohmcm meet this requirement. Furthermore light reflection from MEMS components can also be increased by metal coating of surfaces. Several effects for signal transducing offer other application fields: e.g. thermalelectrical, thermalmechanical (bimorph) and magneticelectrical transducers. Further fields for metal application are given by technology. The galvanoforming process within the LIGA technology represents a powerful method for shaping materials, even if they are difficult to etch. For mass fabrication by using bulk technology nowadays metal is often used as an electrode and contact pad material. In this case the requirements are for instance: good adhesion, low thermal mismatch to adjacent films (substrate) and high long-term stability (relaxation, migration). This is quite comparable to IC fabrication. Surface micromachining by sacrificial layer etching underneath metal films as known from RF devices and laminated post CMOS MEMS illustrates much more challenges with respect to the mechanical properties. Thin film stress, yield strength, hardness and Youngs modulus are critical issues. Although structure bending can be minimised by stress compensation, stress hysteresis due to relaxation can influence reliability and long-term behaviour deeply. Thus even metal surrounded crystalline silicon core structures like SCREAM devices indicate strong temperature dependence. On the other hand it is shown that metal based devices can offer excellent reliability through continuous research (TI's Digital Mirror Device). Data as published recently indicate that problems like hinge fatigue, hinge memory, temperature and light influence can be solved by material and technology adaptation. Metal based fixtures for the fabrication of highly capacitive isolated anchor structures are proven to be stable enough for its application within certain MEMS. Further challenges for MEMS metallization within special applications are given when the operation temperature is increased up to 400 degree C. Thus the interconnect system as well as the whole packaging concept has to be adapted. The huge number of possible interactions within and between several materials of the functional parts at elevated temperatures are critical. Nevertheless, metallization concepts exists and have been verified even at the harsh atmosphere of a car exhaust and a surrounding temperature up to 400 degree C.

2:00 PM F8.2
Chlorine-based Reactive Ion Etching Process to Pattern Platinum for MEMS Applications. Jon Victor Osborn and Sung H. Choi; Microelectronics Technology, The Aerospace Corporation, El Segundo, California.

We have developed platinum deposition and chlorine-based Reactive Ion Etch (RIE) processes that are needed to deposit, pattern and embed low loss RF transmission lines deep within a MEMS process flow. Various combinations of chlorine-based gases were tested to find the optimum gas mixture for RIE. A mixture ratio 1: 0.25 of pure chlorine to argon and 100-150 Watts of RF microwave power were

found to be optimum conditions for the RIE of platinum metal. The addition of argon gas to chlorine was found to contribute to the anisotropic etching of platinum, obtaining vertical shaped side-wall patterns. A simple model of the platinum etching mechanism is proposed. Following the plasma enhanced formation of platinum and chlorine ions, volatile products of platinum chlorides were formed and washed away at an elevated temperature. As a demonstration of our RIE process, using our gas mixture of pure chlorine and argon, micron-sized platinum patterns with vertical side-walls were fabricated. Currently we are investigating the chemistry behind this etching process for platinum using Micro-Auger analysis. Results of this work will be presented.

2:15 PM F8.3
Silver Metallization with Reactively Sputtered Tin Diffusion Barrier Films. Liming Gao[1], Ch. Linsmeier[2], Juergen Gstoettner[1], A. Wiltner[2], Rainer Emling[1], Walter Hansch[1] and Doris Schmitt-Landsiedel[1]; [1]Technical University Munich, Institute for Technical Electronics, Munich, Germany; [2]EURATOM Association, Max-Planck-Institut f. Plasmaphysik, Garching b. Munich, Germany.

As devices continuously shrink in ultra large-scale integration (ULSI), the RC delay of the interconnection system becomes one of the most critical limitations on IC performance. Silver is being codsidered by many as the next metallization of choice for advanced interconnects and has also received attentions as a potential interconnection in the large area TFT/LCDs because of its lowest resistivity and high electromigration resistance. No chemical reactions occurring at a Ag/Si interface, however, adhesion of silver to Si or SiO2 is poor. Ag also diffuses rapidly in silicon to degrades the devices. This report discusses process development and characterization of titanium nitride (TiN) as a diffusion barrier for silver (Ag) metallizations. RF reactively sputtered TiN films with Ar/N2 ratio of 10/5 sccm and the barrier thickness of 12 nm and covered by 200 nm Ag were deposited. The thermal stability of Ag/TiN metallizations on Si, as-deposited after annealing at 300-650 0C, was investigated with sheet resistance measurement, X-ray diffraction (XRD), focused ion beam-scanning electron microscopy (FIB-SEM), atomic force microscope (AFM) and X-ray photoelectron spectroscopy (XPS). No change of sheet resistance was observed after annealing at 600 0C, but an abrupt rise appeared at 650 0C annealing. Focus ion beam-scanning electron microscopy was used this is due to the surface morphology change (agglomeration) after annealing of the samples at different temperatures. After an annealing of a Ag/TiN/Si sample at 650 0C, a constant oxygen concentration with the result of XPS was found because of the slight oxidiation during the high temperature annealing. However, no evidence of Ag diffusion through the TiN diffusion barrier, AgxSiy formation, was observed after high temperature annealing up to 650 0C. The breakdown of the diffusion barrier is presumably due to local defects of the TiN films. This paper shows that titanium nitride thin films an effective barrier against silver diffusion.

3:00 PM *F8.4
Electrical Behavior of Nano-Scaled Interconnects.
Manfred Engelhardt, Guenther Schindler, Werner Steinhoegl, Gernot Steinlesberger and Martin Traving; Corporate Research, Infineon Technologies, Munich, Germany.

Sub-lithographic damascene copper lines were fabricated to investigate already today the physical phenomena of metallic conductors in the metallization scheme of chip generations which are believed to be in production 10 years from now and later. Using standard manufacturing processes and state-of-the-art process tools, including standard lithography tools, narrow copper lines were fabricated at the expense of a relaxed pitch by use of a removable spacer technique. These copper nano interconnects were passivated and subjected to electrical measurements. Our results show that continuous down scaling to increase device performance will result in an unfavourable increase of the electrical resistivity of copper in state-of-the-art metallization schemes. As a consequence, RC delays associated with interconnects will gain increasing importance on the overall performance of future highly integrated circuits. Electrical measurements over a wide range of temperatures down to cryogenic temperatures reveal the limited potential of cooling to reduce resistivity of conductors as lateral dimensions will be shrinked down to the sub-100nm regime. Electromigration life times of sub-100nm copper lines embedded in oxide were found to be comparable with those obtained for similar structures fabricated with todays feature sizes. By down scaling of copper diffusion barriers in damascene trenches, barrier functionality was demonstrated after high temperature anneals and excessive bias-temperature stress tests for films meeting or even exceeding end-of-roadmap thickness requirements. An analysis of the results of leakage current measurements at very high electric fields applied between neighboring damascene lines suggests that the conduction mechanism in the intermetal dielectric is Frenkel-Poole type rather than Schottky emission.

3:30 PM F8.5
Correlating Resistivity and Nanostructure in Ultra-Fine Copper Wires. Yu Zhu, Miryam Elouneg-Jamroz, Oscar van der Straten, Kathleen A. Dunn and Alain E. Kaloyeros; UAlbany Institute for Materials, School of NanoSciences and NanoEngineering, University at Albany - SUNY, Albany, New York.

The resistivity of Cu interconnects increases as the wire cross section approaches the electronic mean free path for scattering, 40 nm in copper. This rise is attributed to the gradually higher contributions from surface scattering as function of decreasing cross section due to the wave nature of electrons. Other contributors to the rise in resistivity include grain boundary and surface roughness scattering. This study seeks to correlate the electronic scattering in a wire with key micro- and nanostructural features in order to isolate the individual contributions of each of these phenomena. Accordingly, relatively wide copper lines were patterned by damascene processing into 960, 320 and 240 nm-wide electrical test structures embedded in silicon dioxide. In these trenches, 10 or 20 nm-thick TaN_x diffusion barriers were first deposited by either physical vapor deposition (PVD) or atomic layer deposition (ALD). The trenches were then filled with 400 nm PVD Cu and the excess Cu removed by mechanical polishing using different Al_2O_3 particle size to modify surface roughness. Alternatively, narrower copper test structures (100, 80, and 40 nm) were fabricated by a 2-step lift-off process. In the first step, electron beam lithography was used to pattern 120 nm-thick PMMA photoresist to define the ultra-fine Cu lines and the 3-micron wide contacts. PVD Cu, 40nm thick, was deposited on the patterned resist, and standard lift-off procedures were used to remove the PMMA and leave the copper lines on the oxide substrate. A second lift-off process employed standard optical lithography to define the 150 by 150 micron square contact pads for electrical testing of fine lines. The geometry and surface morphology of the resulting Cu lines were measured by focused ion beam scanning electron microscopy (FIB-SEM) equipped with an electron back-scattered diffraction (EBSD) detector for determining local orientation of grains as small as 10 nm. Surface roughness was measured by atomic force microscopy (AFM) and resistance was measured by probe contact and multi-meter. While it is not surprising that the measured resistivity of Cu wires increases as the wire width decreases, additional results demonstrate that surface roughness and local grain orientation can also play a significant role in the increase in resistivity as well.

3:45 PM F8.6
Kinetics and Adhesion Enhancement for Cu Metallization in Supercritical Carbon Dioxide. Yinfeng Zong and James J Watkins; Chemical Engineering, University of Massachusetts Amherst, Amherst, Massachusetts.

Copper is the material of choice for advanced interconnects due to its low electrical resistance and superior electromigration resistance. However, as the device size shrinks, the difficulty of filling of high aspect ratio feature increases rapidly. Supercritical Fluid Deposition (SFD) is a promising hybrid technique for single step conformal metal deposition that is extendable to sub 45 nm device structures. Here we report a kinetic study of Cu SFD using Bis(2,2,7-trimethyloctane-3,5-dionate) Cu(II) [Cu(TMOD)2] as the precursor. Film deposition rates in the temperature range of 200 °C to 250 °C as a function of the relevant experimental parameters including precursor and H2 concentration will be reported and the implication of these results for mechanistic pathways for Cu deposition in CO2 will be discussed. We also report a novel adhesion enhancement of Cu films deposited from CO2 onto current and potential barrier systems. In particular, the efficacy of a sacrificial adhesion promoting layer is demonstrated. The surface modification produces strongly adherent Cu films as evidenced by scribe tape testing. The films and interfaces are characterized by x-ray photoelectron spectroscopy depth profiling, field emission scanning electron microscopy, spectroscopic ellipsometry, atomic force microscopy and four point probe measurements.

4:00 PM F8.7
Microscopic Process and Driving Force for Room-temperature Recrystallization in Cu Thin Films.
Makoto Wada and Junichi Koike; Dept. of Materials Science, Tohoku University, Sendai 980-8579, Japan.

Cu thin films undergo microstructure change at room temperature, known as room temperature recyrstallization. Its microscopic mechanism and effects on the final microstructure after heat treatment are not well understood. A driving force is also in controvercy. In this work, we investigated the microscopic mechanism and effects on the heat-treated texture in electroplated Cu thin films. A driving force was also investigated in sputtered Cu thin films. The recrystallization process was monitored by x-ray diffraction, nanoindentation, and

scanning electron microscopy with electron backscattering diffraction. As-plated films had a random texture and was highly strained. After three hours at RT, strain-free grains appeared. Each neighboring grains were in a twin orientation relationship. Recrystallization was completed after 10 hours and more than 60% of recrystallized grain boundaries were coherent (111) twin interfaces. When the as-plated film and RT- recrystallized film were heated to 723 K, no difference was found in the heat-treated microstructure. This was because the as-deposited film underwent the same microstructure change as in the RT recrystallized film during initial portion of heating at about 100 oC. Thus the both films had the same microstructure before grain growth occurred at higher temperatures. A driving force was investigated by using sputtered films. Two types of films were prepared, one having a random texture and another having a <111> texture. Grain size of the both films were nearly the same, eliminating proposed possibility of grain boundary energy as a major driving force. The use of sputtered film also eliminated proposed influence of chemical impurities that would otherwise be originated from electroplating solution. RT recrystallization was observed in the random film but not in the <111> film. XRD peak position indicated that both films were initially highly strained to a similar magnitude. Strain relaxation was observed only in the random film associated with the RT recrystallization. On the other hand, peak width was much larger in the random film than in the <111> film. This indicated that the strain variation among grains are larger in the random film than in the <111> film. The obtained results suggested a major driving force to be a gradient of strain energy density.

4:15 PM F8.8
A Study of Dilute Cu Alloys for Dual-Damascene Interconnect Applications. C. Hutchison[1], A. Bhanap[1], M. Pinter[2], W. Yi[2], K. Scholer[1], N. Truong[1], R. Prater[1] and E. Lee[1]; [1]Electronic Materials, Honeywell, Sunnyvale, California; [2]Electronic Materials, Honeywell, Spokane, Washington.

In an effort to identify potential candidate alloys with reduced electro- and stress-migration for Cu dual damascene applications, 6N Cu and Cu alloys with 0.5 at. % of Ag, Al, Sn, Ti, and 1.3 at. %Mg were evaluated. Targets were made in the Applied Materials ENDURA® IMP configuration and films were prepared by depositing on a TaN/Ta barrier layer in the ENDURA. Alloying addition refined target grain size and increased hardness. One notable finding was that the grain refinement resulted in improved deposition yield. Alloying elements increased electrical resistivity and decreased thermal conductivity. Ti increased electrical resistivity most and Ag least. However, there was no significant difference in sputtering performance. All Cu seeds showed predominantly <111> orientation regardless of composition, but the electrochemically deposited Cu film deviated from complete <111> orientation by 10% to 44%. AFM examination revealed that deposited film grain size was refined with alloying addition, 6N Cu (110 nm), CuAl (115 nm), CuTi (86 nm), CuSn (57 nm), CuAg (25 nm). Ti and Al were found to retard corrosion most upon exposure to moisture by forming a passivating layer. SIMS analysis showed that solute atoms diffused readily through electroplated Cu at 400°C, Sn and Ag being the fastest diffusing species. Alloying addition imparted little affect on the electrical resistivity of plated Cu except with Ti and Sn in blanket films. All alloyed seed layers showed good adhesion to Ta barrier. For test structures, 6N Cu seed rendered the lowest line resistance and CuTi the highest. There was no discernible difference in the line to line leakage current for all alloys. This paper also discusses the strengths and weaknesses of each alloy and suggests potential candidate alloys for future interconnect conducting materials.

4:30 PM F8.9
The Effect of Stress Distribution on the Textural Evolution of Cu Interconnects after Annealing with the Different Line Width. Jae-Young Cho[1] and Hyo-Jong Lee[2]; [1]Materials Engineering, McGill University, Montreal, Quebec, Canada; [2]SamSung Electronics Co., LTD, Yongin-City, South Korea.

An influence of stress distribution on the textural evolution of Cu interconnects after annealing with the different line width is investigated. Texture measurements were performed on the surface area of Cu interconnects using OIM (orientation imaging microscopy) before and after annealing at 200?C for 10 minutes. To analyze a relationship between the stress distribution and textural evolution in the samples investigated, micro stress were calculated as line width decrease using FEM (finite element modeling). In this investigation, it was found that the inhomogeneity of stress distribution in the Cu interconnects is an important factor for understanding textural evolution after annealing. New interpretation of textural evolution with an increase of line width in damascene interconnects lines after annealing is suggested, based on the state of stress in different interconnect lines.

4:45 PM F8.10
The initial nucleation behavior during Al, Cu, W-CVD on barrier metal layers. Yukihiro Shimogaki[1], Tomohisa Iino[1], Masakazu Sugiyama[3], Takeshi Momose[1], Young Sok Kim[1], Takeshi Tsumura[2], Yuya Kajikawa[2], Suguru Noda[2] and Hiroshi Komiyama[2]; [1]Dept. of Materials Engineering, Univ. of Tokyo, Tokyo, Japan; [2]Dept. of Chemical System Engineering, Univ. of Tokyo, Tokyo, Japan; [3]Dept. of Electronic Engineering, Univ. of Tokyo, Tokyo, Japan.

The ever growing shrinkage of ULSI devices requires nano-meter level ultra thin metal films with smooth surface morphologies and good adhesion onto the under layer in multi level interconnects. The high aspect ratio trenches or holes also require CVD process to deposit metal thin films, like as Al, Cu, and W onto barrier layer. We have investigated the initial nucleation behavior of Al, Cu and W-CVD using laser light reflection method. TiN thin films prepared by PVD or CVD were used for underlayer of Al, Cu, and W-CVD. Ta thin films were also used as under layer for Cu-CVD. The incubation period, in which no nuclei were observed on the surface, was easily identified with this technique. The surface chemical compositions during the incubation period was analised by XPS and micro-AES methods. We found that several monolayers of adsorbates exists on the barrier layer during the incubation period. When this adsorbates exceeds certain amount, small nuclei in the order of 10nm were formed. The effects of preparation method and pretreatment method of barrier layer onto the nucleation behavior will be discussed.