SYMPOSIUM J

Silicon Carbide–Materials, Processing, and Devices

April 14 - 15, 2004

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* Invited paper

SESSION J1: Devices & Processing
Chair: T. Kimoto
Wednesday Morning, April 14, 2004
Room 2009 (Moscone West)

8:30 AM *J1.1
SiC Power Devices - An Overview. Anant Kumar Agarwal, Power Devices, Cree Inc., Durham, North Carolina.

An overview of SiC Power Devices will be provided. Progress in SiC Schottky diodes (600 V, 1200 V), SiC PiN diodes, SiC Power MOSFETs, SiC BJTs and Thyristors will be described. SiC Schottky diodes have already been commercialized. The next step of inserting these diodes in Si IGBT modules is happening now. Emphasis will be placed on the problems and issues at the SiC device/process interface which need to be urgently addressed such as the roughness created during the implant anneals, reliability of the gate oxide under positive and negative bias, low current gain of the BJTs, forward voltage instability in the pn junctions etc. Overcoming these issues in the near future will be critical to the successful commercialization of SiC devices.

9:00 AM J1.2
Doping-Induced Strain and Relaxation of Al-doped 4H-SiC Homo-Epitaxial Layers. SungWook Huh[1], HunJae Chung[1], Marek Skowronski[1] and Joseph Sumakeris[2]; [1]Carnegie Mellon University, Pittsburgh, Pennsylvania; [2]Cree, Inc, Durham, Pennsylvania.

Aluminum-doped 4H SiC epilayers with Al concentrations in the 7.4x1018 - 2.6x1020 cm-3 range were deposited on off-orientation (0001) wafers by chemical vapor deposition method and analyzed using high resolution x-ray diffraction, transmission electron microscopy, and KOH etching. K-space maps of (0008) reflection revealed two distinct peaks separated along the 2? axis. The higher 2? peak was identified as due to Al-doped strained epilayer due to increase of c-lattice parameter with Al-doping. For Al-concentration up to 2.0x1020 cm-3, 10 ?m thick layers were fully strained with the a-lattice parameter of the layer matching that of the substrate. The basal planes of the epilayers were tilted in respect to the substrate in the direction of the off-cut. The amount of tilt is consistent with the elastic strain in the epilayer. The layer with highest Al-concentration ([Al]=2.6x1020 cm-3) was partially relaxed. The Full Width at Half Maximum of (0008) reflection increased by a factor of approximately two, the c-lattice parameter decreased, while at the same time the a-lattice parameter increased compared to the lattice parameter of the strained epilayer. The threading dislocation density in relaxed layer estimated by KOH etching exceeded 106 cm-2. Since no inclusions has been found in the relaxed region by TEM, we interpret the above changes as due to film relaxation. This assertion agrees with the estimates of the critical layer thickness. This is the first observation of strain relaxation in an epilayer of hexagonal semiconductor.

9:15 AM J1.3
Pressure Dependence of Aluminum Doping in SiC Vapour Phase Epitaxy. Adolf Schoner and Malin Gustafsson; Acreo AB, Kista, Sweden.

The control of the doping incorporation in vapour phase epitaxy (VPE) of SiC is an important issue for the growth of device structures. The dopant incorporation in SiC-VPE can be controlled through the parameters dopant precursor flow, silicon precursor flow, carbon to silicon (C/Si) ratio in the gas phase, growth temperature, and reactor pressure. In this study we will report on the aluminum incorporation in 4H-SiC and 6H-SiC in dependence on the total pressure in the reactor. The experiments on the pressure dependent aluminium incorporation were done in a VPE reactor of hot wall type equipped with substrate rotation. Hydrogen was the carrier gas, silane and propane were the growth precursors. Trimethylaluminum (TMAl) was the precursor for aluminium doping. To compare the growth at different reactor pressure, parameters like growth temperature, silane flow, C/Si ratio, and the TMAl flow were kept constant. The reactor pressure was varied in the range 150mbar to 250mbar. In addition, epitaxial growth was done with periodic opening and closing of the pressure control valve in the pumping system. The open-close cycle period was about 20 seconds. For comparison, epitaxial growth runs with pressure change were performed for n-type doping with nitrogen. The biggest influence of the reactor pressure on the aluminum incorporation was seen for the medium concentration range (1e16/ccm to 1e19/ccm). A change in the reactor pressure from 210mbar to 150mbar reduced for example the net doping concentration determined from capacitance-voltage (C-V) measurements from about 3e18/ccm to 1.7e18/ccm. The doping variation divided by the average doping increases with decreasing aluminum concentration and variations of factor 7 to 9 could be observed at concentrations around 1e16/ccm to 1e17/ccm. Periodic pressure change resulted in sinus-like depth profiles of the net doping concentration with a variation of the net doping by the factor 3 to 7, depending on the average net doping level. The variation of the net doping can only be explained by a change in the aluminium concentration. The concentration of compensating donors is typically below 1e15/ccm in hot wall VPE reactor cells. Therefore compensating donors are not responsible for the observed variation of the net doping with changing pressure. In addition, a change of the n-type doping concentration for nitrogen doped epilayers grown with periodic pressure change was not measured by C-V characterisation.

9:30 AM J1.4
Ion Implantation and 1 MeV Electron Irradiation of 4H-SiC—Comparative Studies. andrew O evwaraye[2,1], Steven R. Smith[2,1], William C Mitchel[1,2] and Gary C Farlow[2,1]; [1]Air Force Research Laboratory, Wright-Patterson Air Force Base; [2]Physics, University of Dayton, Dayton, Ohio.

In silicon carbide based electronic device technology, ion implantation of donor/acceptor ions (N, P/Al, B) is widely used to selectively dope silicon carbide. This is necessary because the thermal diffusion rates of the dopant species in SiC is low at reasonable temperatures (<12000C). Ion implantation causes lattice damage and local stoichiometric imbalance. A post ion implantation anneal at high temperatures (1600 -17000C) is therefore necessary to repair the damaged lattice and to activate the implanted species. Some implantation induced defects survive the high temperature anneal and these may, especially the deep defects, affect the performance of electronic devises. High energy electron irradiation of silicon carbide produces point defects-vacancies, interstitials, and anti-sites. These may form thermally stable complexes such as divacancies (Vsi -Vc). In this work, we compare the defects produced by Ar+ implantation in 4H-SiC with those produced by 1 MeV electron irradiation of 4H-SiC. A 4 micron meter thick nitrogen-doped 4H-SiC epitaxial layers with a doping concentration of 1.5 x 1015 cm-3 was Ar+ implanted at 6000C. The energy of the ions was 160 keV and at a dose of 2 x 1016 cm-2. Post implantation anneal was carried out at 1600 0C for five minutes. An n-type 4H-SiC bulk with a doping concentration of 1.5 x 1017 cm-3 was irradiated with 1 MeV electrons at a dose of 0.1 to 6.1 x 1017 cm-2. The electron irradiation was carried out at room temperature; the temperature of the sample did not rise above 50 0C during irradiation. Both the Ar + implanted and electron irradiated samples were studied with deep level transient spectroscopy (DLTS) and the results compared. After electron irradiation dose of 4.1 x 1017 cm -2, three strong peaks at Ec - 0.30 eV, Ec - 0.63 eV and at Ec - 0.78 eV were observed. The defect at Ec -0.63 eV is the Z1/Z2 and the defect at Ec - 0.78 is the so called RD1/2. The concentration of Ec -0.63 eV increases with the electron fluence. This suggests that vacancies play a significant role in the formation of this complex. The isochronal annealing of the electron induced defects show that the annealing behavior of these defects may depend on the source of formation. The DLTS measurements of the Ar+ 4H-SiC reveal six capacitance peaks. The two most prominent peaks are at Ec - 0.74 eV and at Ec -0.81 eV. A photo-DLTS measurements showed that the peak at Ec - 0.81 eV shifted to lower temperatures when the sample was illuminated with white light. However, illumination of the electron irradiated sample produced no observable effect.

9:45 AM J1.5
A Robust Process for Ion Implant Annealing of SiC in a Low-Pressure Silane Ambient. Shailaja P Rao[1], Stephen E Saddow[1], Roberta Nipoti[2], Fabio Bergamini[2], Yusuf Emirov[1] and Anant Agarwal[3]; [1]Electrical Engineering, University of South Florida, Tampa, Florida; [2]CNR, CNR - IMM Sezione di Bologna, Bologna, Italy; [3]Cree, Inc, Durham, North Carolina.

High-dose Al implants in n-type epitaxial layers have been successfully annealed at high temperatures without any evidence of step bunching. Anneals were conducted in a silane ambient and at a pressure of 150 Torr. Silane, premixed in UHP Ar, was further diluted in a 6 slm Ar carrier gas and introduced into a CVD reactor where the sample was heated via RF induction. A 30 minute anneal was performed followed by a purge in Ar at which time the RF power was switched off. The samples were then studied via plan-view secondary electron microscopy (SEM) and atomic force microscopy (AFM). The resulting surface morphology was step-free and flat. Results of the annealing process and characterization results will be presented along with electrical data relating to the dopant activation and implanted region conductivity.

SESSION J2: Crystal Growth & Processing
Chair: P. G. Neudeck
Wednesday Morning, April 14, 2004
Room 2009 (Moscone West)

10:30 AM *J2.1
Homoepitaxial growth and characterization of thick SiC

layers with a reduced micropipe density. Hidekazu Tsuchida, Isaho Kamata, Syunsuke Izumi, Takeshi Tawara, Tamotsu Jikimoto, Toshiyuki Miyanagi, Tomonori Nakamura and Kunikazu Izumi; Yokosuka Research Laboratory, Central Research Institute of Electric Power Industry, 2-6-1 Nagasaka, Yokosuka, Kanagawa 240-0196, Japan.

The growth techniques of thick SiC epitaxial layers with a reduced micropipe density have been developed using a vertical hot-wall CVD reactor with an inner susceptor configuration. Micropipe closing by growing an epilayer at a low C/Si ratio of the source gases is possible with a nearly 100% probability for 4H-SiC(0001) and (000-1) substrates off-cut towards either <11-20> or <1-100> directions. Growth of low-doped and thick SiC epitaxial layers is also possible in the reactor with high growth rates of 15-20 μm/h achieving a small roughness. A 210 μm-thick 4H-SiC epitaxial layer with a doping concentration of 9x10^{13} cm^{-3} demonstrated 14.4 kV blocking performance for a 1 mmϕ Ni Schottky barrier diode with a low leakage current density. Growth of epitaxial layers on (000-1) substrates with low doping at mid 10^{14} cm^{-3} and a low epi-induced defect density was also demonstrated. Dislocations and stacking faults in epilayers grown on substrates off-angled towards different directions and substrates oriented different faces were investigated by reflection synchrotron x-ray topography using a monochromator, KOH etching and photoluminescence mapping. The character and densities of basal plane dislocations and in-grown stacking faults were compared for the different off-cut directions. The carrier lifetime of 4H-SiC epilayers was evaluated by time-resolved photoluminescence and microwave-detected photoconductive decay. A long carrier lifetime of 1.4 μs at room temperature and 6.8 μs at 500 K was measured from a sample, while a large sample-to-sample variation was observed. The deep centers, impurities and dislocations were investigated to determine the lifetime killer of the epitaxial layers, and we found a correlation between carrier lifetime, and $Z_{1/2}$ and $EH_{6/7}$ centers.

11:00 AM J2.2
Epitaxial Growth of 3C-SiC on T-shape columnar Si Substrate. Shigehiro Nishino, Akira Shoji, Taro Nishiguchi and Satoru Ohshima; Electronics and Information Science, Kyoto Institute of Technology, Kyoto, Kyoto, Japan.

Cubic SiC is a suitable semiconductor material for high temperature, high power and high frequency electronic devices, because of its wide bandgap,high electron mobility and high saturation electron drift velocity. The usage of Si substrates has the advantage of large area substrates for the growth of 3C-SiC layers. However, a large mismatch between 3C-SiC and Si has caused the generation of various defects at the SiC/Si interface.Lateral epitaxial overgrowth (LEO) of 3C-SiC on Si substrates has been reported to reduce the defect density. In this report, epitaxial growth of 3C-SiC on (100) Si and (111) Si substrates has been investigated to reduce interfacial defects. Epitaxial growth of 3C-SiC on the patterned seed 3C-SiC was performed by CVD using hexamethyldisilane (HMDS) as a source gas. Various patterned Si substrates were prepared. We employed new approach for the substrate which is prepared by combining RIE and in-situ HCl etching and T-shape pattern was created on the Si substrate. Seed 3C-SiC layers were deposited on 3C-SiC on (100) Si and (111)Si. Top surface of T-shape pattern consists of 1 micron thick , 50 micron wide 3C-SiC and 50 micron wide seed is supported by Si column with 5 micron width. Epitaxial growth of 3C-SiC was carried out as following three steps. First step is in situ etching of the substrate. Second process is carbonization of the substrate. Third step is 3C-SiC deposition by atmospheric-pressure chemical vapor deposition. For (100) Si substrate, growth temperature was 1370 oC. Flow rate of H2 carrier gas and HMDS were 2.5 slm and 0.3sccm, respectively. For (111) Si substrate, the seed 3C-SiC layer was grown at the growth temperatures of 1350 oC. Grown layer showed trapezoidal shape and extended laterally. Crystal quality of the 3C-SiC film on the Si substrate and extended region without Si support is discussed.

11:15 AM J2.3
Dry Thermal Oxidation of SiC: Modelization and Elemental Composition of the Interface. Fernanda Chiarello Stedile[1], C Radtke[2], B C Ferrera[1], J Bavaresco[1], E M Comin[1], L C Goedtel[1], I J R Baumvol[2] and R M C de Almeida[2]; [1]Instituto de Quimica, UFRGS, Porto Alegre, RS, Brazil; [2]Instituto de Fisica, UFRGS, Porto Alegre, RS, Brazil.

We propose a model based on reaction diffusion equations to describe the oxidation of silicon carbide in dry O_2 and we present experimental evidences of the SiO_2/SiC interface elemental composition using oxygen isotopic tracing. In the model we take into account several experimental facts: i) the sample geometry is explicitly considered, since it has been experimentally verified that oxidation kinetics curves depend on the face exposed to the oxidant atmosphere: C-face, Si-face, or (11$\bar{2}$0)-face; ii) after oxidation is completed, we find an amorphous SiO_2 film on c-SiC, with C located mainly near the SiO_2/SiC interface; and iii) Si atoms concentrations in SiC bulk and SiO_2 are different. Reaction diffusion equations are proposed in one dimension, taken to be the direction normal to the sample surface, where the variables are the local concentrations of Si, C and O, either in their diffusive or fixed states. The sample geometry is introduced as initial condition. Reactions between the diffusing and fixed species are considered. Adequate sets of reaction rates and diffusion coefficients yield different kinetics curves depending uniquely on the initial sample geometry, as found in experiments. Different oxidation pressures yield different kinetics curves which may be collapsed by adequate scaling time. In a previous work [1] we observed that dry thermal oxidation of SiC and of Si produced similar silicon oxide films in the near surface and bulk regions for both semiconductors. However, the amount of O from a second oxidation performed in ^{18}O enriched O_2 gas (following a previous one in $^{16}O_2$), incorporated in the near interface region, was always smaller in the case of SiO_2/SiC samples as compared to those of SiO_2/Si, in which the concentration of ^{18}O was equal to the isotope enrichment of the gas. In the present work we prepared symmetric samples of SiO_2/SiC and SiO_2/Si oxidized either in $^{18}O_2$ / $^{16}O_2$ or in $^{16}O_2$ / $^{18}O_2$ gas sequences in order to determine the presence of O from the first oxidation in the interfacial region by ^{18}O nuclear reaction profiling. Results indicate that in the case of SiO_2/SiC samples both O isotopes are present in this region. The effect of the temperature of the second oxidation step and the role of carbonaceous species (mainly CO) formed during oxidation were also investigated. Besides, the presence of C and/or Si are also needed to complete stoichiometry of the dielectric film close to the interface. Complementary analyses by ^{29}Si and ^{13}C nuclear reaction profiling and SIMS to be performed in the next months will help to confirm our hypothesis, as well as the one of a SiO_2/SiC more gradual interface as compared to the SiO_2/Si, predicted by our model. [1] I.C. Vickridge, I. Trimaille, J.-J. Ganem, S. Rigo, C. Radtke, I.J.R. Baumvol and F.C. Stedile, Physical Review Letters 89 (2002) 256102-1.

11:30 AM *J2.4
Status of 4H-SiC Substrate and Epitaxial Materials for Commercial Power Applications. Adrian R Powell, Joe J Sumakeris, Robert T Leonard, Mark F Brady, Stephan G Muller, Valeri F Tsvetkov, Robert Trussell, Calvin H Carter, Al A Burk, Rob C Glass and H McD Hobgood; Cree Inc., Durham, North Carolina.

Based on the predicted performance enhancements offered by the new generation of high power devices there is enormous potential for growth in SiC power devices in the next few years. In the development of substrate and epitaxial materials for this emerging commercial market, it is imperative to develop the product to meet the needs of the targeted application. We will discuss the status and requirements for SiC substrates and epitaxial material for power devices such as Schottky and PiN diodes. For the SiC Schottky device where current production is approaching 50 amp devices, there are several material aspects that are key. These include: wafer diameter (3-inch and 100 mm), micropipe density (<0.3 cm^{-2} for 3-inch substrates and 20 cm^{-2} for 100 mm substrates), epitaxial defect densities, epitaxial doping and epitaxial thickness uniformity. For the PiN diodes the major challenge is the degradation of the V_f characteristics due to the introduction of stacking faults during the device operation. We have demonstrated that the stacking faults are often generated from basal plane dislocations in the active region of the device. Additionally we have demonstrated that by reducing the basal plane dislocation density, stable PiN diodes can be produced. At present typical basal plane dislocation levels in our epitaxial layers are 100 to 500 cm^{-2}; however, with proprietary epitaxial procedures we have achieved densities as low as 4 cm^{-2} in epitaxial layers grown on 8° off-axis 4H-SiC substrates. Work supported in part by DARPA contracts N00014-02-C-0306, N00014-02-C-0302, and Title III contract F33615-99-C-5316

SESSION J3: Devices & Processing
Chair: S. E. Saddow
Wednesday Afternoon, April 14, 2004
Room 2009 (Moscone West)

1:30 PM *J3.1
Charge Controlled Silicon Carbide Switching Devices. Peter Friedrichs, SiCED GmbH & Co. KG, Erlangen, Bavaria, Germany.

Silicon carbide power devices are believed to revolutionize the power semiconductor business in the next decade. A first step was realized by the commercial availability of SiC Schottky barrier diodes from Infineon and Cree in 2002. Looking into the near future, the following logical step in the device chain should be a SiC switching device. The perspectives range from high voltage applications in energy systems down to the huge market for low voltage power switches, where even in the blocking voltage range below 100V SiC is believed to be one

potential candidate for fulfilling the increasing demands on power density. Clearly this development should be empowered by a high volume production which is at the moment rather visible in the blocking voltage range around 1000V or even down to 600V for applications where charge controlled silicon devices are not suited (hard switching, high frequency bridge topologies with freewheeling functions e.g.). Based on a success of these efforts devices with blocking voltages above 3kV will be available as a next generation of SiC switches. The decision which type of device can play a vanguard role is not straightforward to decide. Facing the today's volume numbers, charge or voltage controlled device structures are clearly favored due to their powerless control and the unique compatibility with most of the driving circuits available at the market. Thus, the silicon carbide power MOSFET was for a long period developed and tested, however, even reflecting the newest results regarding the stability and channel conductivity issue the availability at the market will take place most probably soonest in 2006. As an alternative the silicon carbide VJFET silicon MOSFET combination was developed at SiCED. Several improvements where performed which make the device more attractive for the customer. It will be shown which factors drive these optimization and how they can be implemented. The result is a device which behaves for the user more and more like a classical MOSFET with respect to the input as well as the output characteristic. Although the primary target for this devices is the >1000V blocking voltage range, it will be discussed how the important 600V power switch market can be accessible for SiC power devices too. With respect to high blocking voltages two concepts were developed by SiCED. Firstly a stacked switch based on the VJFET technology was introduced which behaves like a cascode but with blocking voltages exceeding several kV. As second step a bipolar modulated switch called BIFET was developed showing a promising performance especially for blocking voltages above 3kV. The presentation will give an overview about the developments of SiC power switches at SiCED, in addition some potential applications serving as drivers for the SiC power switch development will be sketched. Finally, an outlook to near and long term perspectives for SiC power switches will be given.

2:00 PM J3.2
4H-SiC MIS structures using oxidized Ta_2Si as high-k dielectric. Perez Amador[1], Philippe Godignon[1], Narcis Mestres[2], Josep Montserrat[1], Dominique Tournier[1] and Felip Sandiumenge[2]; [1]CNM-IMB-CSIC Centre Nacional de Microelectronica, Bellaterra, Barcelona, Spain; [2]ICMAB Institut de Ciencia de Materials, Bellaterra, Barcelona, Spain.

Among compound semiconductors, only SiC can be thermally oxidized to grow insulating SiO_2 layers. The use of amorphous, thermally grown SiO_2 as a gate dielectric offers several key advantages in CMOS processing, including a thermodynamic and electrical stable interface as well as superior electrical isolation properties. Nevertheless, the high density of defects encountered at the SiC/SiO_2 interface represents a major obstacle in the successful fabrication of MOS electronic devices. In fact, the inversion channel mobility of SiC 4H-SiC nMOSFETs is far below of the predicted value from their bulk electron mobility. The use of alternative dielectrics as gate material, with a higher dielectric constant, can be considered as a valuable alternative in order to enhance the channel conduction and reduce the oxide degradation due to current injection. We propose the use of deposited and oxidized Ta_2 Si films on 4H-SiC substrates as dielectric in metal-insulator-semiconductor structures. In a previous work [1], the feasibility of this insulator was demonstrated onto 6H-SiC substrates. Ta_2Si target films of 150Å and 400Å thickness have been deposited by direct sputtering after a SNC cleaning process. X-ray diffraction analysis showed no specific peaks of Ta, Si or Ta_2Si, indicating that the as-deposited films were amorphous. Following the deposition the samples were oxidized in dry environment at 950°C and 850°C during 90min. Using X-ray diffraction analysis, Ta_2O_5 peaks are clearly evidenced implying an orthorhombic Ta_2O_5 [1 11 0] preferential orientation. Thereby, no peaks corresponding to Ta, Si or Ta_2 Si have been observed. MIS capacitors were fabricated with the insulator previously described using Al as gate metal or without permanent metallization using a mercury probe. An effective dielectric constant of 16 has been achieved for the Ta_2Si deposited and oxidized insulating films derived from C-V measurements along with SIMS depth profiling analysis. This result has been fitted using a simple physical model.From C-V measurements, the interface states density spectra of the different samples has been derived by means of Terman, conductance and Hi-Low method. For the samples oxidized at 950°C, an interface traps density of $10^{12}cm^{-2}eV^{-1}$ has been obtained at E_C-E_T=0.2eV. Thus, a similar Dit to thermal non-nitridated SiC/SiO_2 insulators has been inferred. Nevertheless, for the samples oxidized at 850°C a significant reduction in interface traps density $10^{11}cm^{-2}eV^{-1}$ has been obtained at E_C-E_T=0.2eV. The average breakdown field has been extracted from I-V measurements. For the 150Å Ta_2Si 950°C oxidized sample, a critical breakdown field of 6MV/cm has been acquired. In spite of that, considering the equivalent thickness of SiO_2, that is, the theoretical thickness of SiO_2 that would be required to achieve the same capacitance density, the critical breakdown field would be of 16MV/cm. [1] A. Perez et Al. Proc. of the ICSCRM 2003 (Lyon).

2:15 PM J3.3
The Effects of Surface Passivation Treatments on Large Signal Characteristics of SiC MESFETs in Class A and Class B Operations. Ho-Young Cha[1], Y C Choi[1], Lester F Eastman[1], A O Konstantinov[2], C I Harris[2], P Ericsson[3] and Michael G Spencer[1]; [1]Electrical and Computer Engineering, Cornell University, Ithaca, New York; [2]AMDS AB, Kista, Sweden; [3]ACREO AB, Kista, Sweden.

High breakdown field and high saturation velocity coupled with high thermal conductivity make SiC very attractive for high power microwave applications. To date, SiC MESFETs have suffered from a current instability problem due to a trapping phenomenon in the substrate and at the surface. In wide bandgap semiconductors, the trapping/detrapping is a slow process which causes degradation of both DC and RF performances. Recent progress in SiC growth technology has resulted in high purity semi-insulating substrates, with dramatically reduced Vanadium content. Using better semi-insulating substrates should result in improved device performance. Nevertheless, the surface issue cannot be managed completely by growth techniques alone. Instead, it is dominated by the fabrication process, and can be mitigated considerably by using surface passivation. In this work, the influence of SiO_2 and Si_3N_4 passivation treatments was investigated by comparing electrical characteristics before and after passivation. Both SiO_2 (two different types of SiO_2) and Si_3N_4 films were deposited using a PECVD system. Regardless of passivation type, DC current instability was suppressed dramatically, and f_T and f_{MAX} decreased slightly due to parasitic capacitance. The improvement of RF performance did depend on passivation type and operation conditions. CW RF performances in both class A and B operations were measured before and after passivation. Among different passivation types, Si_3N_4 passivation resulted in the best RF performance, especially in class B operation where the power added efficiency increased from 30% up to 50%. After passivation treatments, the output power improved to equal the theoretical value derived from the DC characteristics. The enhancement of output power has a correlation with the suppression of DC current instability, which can be explained by a reduction in trapping effects at the surface after passivation. The fact that the improvement of RF power performance was more pronounced in class B operation than in class A operation suggests that the trapping effects would be more apparent in class B than in class A operation before passivation. In class B operation, the gate bias is close to the pinch-off, which is a high reverse bias condition in the Schottky contact between the gate metal and the semiconductor. A high reverse bias applied to the barrier increases the field in the junction and thus increases the probability for an electron to tunnel from the metal into the semiconductor. A higher number of injected electrons from the gate increases the probability of trapping. It is clear that the passivation treatments suppress the trapping effects at the surface improving both DC and RF performances. Passivation results using an MBE grown AlN layer are expected by the time of this conference.

2:30 PM J3.4
Laser Direct Write and Gas Immersion Laser Doping Fabrication of SiC Diodes. Islam Salama[2], Nathaniel R Quick[1] and Aravinda Kar[2]; [1]AppliCote Associates, LLC, Lake Mary, Florida; [2]University of Central Florida, Orlando, Florida.

Silicon carbide diodes are fabricated using a combination of gas immersion laser doping (GILD) and laser direct write (LDW) in situ metallization in a commercial SiC wafer. Trimethylaluminum (TMAl) and nitrogen are the precursors used to produce p-type and n-type silicon carbide semiconductors, respectively. Nd:YAG and excimer laser nitrogen doping, in SiC epilayer and single crystal substrates, increase the dopant concentrations by two orders of magnitude. Nd:YAG produces deep (500-600 nm) junctions while excimer produces shallow (50 nm) junctions. Laser-assisted effusion/diffusion is introduced and utilized to dope Al in SiC wafers. Using this GILD technique, a 150 nm p-type doped junction is fabricated in semi-insulating 6H-SiC and n-type doped 4H-SiC wafers. Ohmic contacts are created by laser direct metallization producing patterned conductive phases in these doped materials. No metal is added to the SiC during LDW. These conductors are carbon rich when processed by nano-second-pulsed frequency doubled Nd:YAG (532 nm wavelength) laser and exhibit a stable contact resistance after annealing up to 3 hours at 950 degrees Centigrade. Alternatively, an excimer (193 nm, 248 nm and 351 nm wavelength) laser can be used to create silicon rich Schottky contacts. The geometry of the diodes can be vertical or planar to the wafer surface and the laser processes are thought to reduce defect densities in the irradiated areas. Interconnection can be accomplished by LDW in situ metallization on the surface or through the volume of the wafer. These laser processed diodes are intended for use in high-temperature, high-voltage and

high frequency switching and sensing applications.

2:45 PM J3.5
Improvement of GaN epitaxial growth by using SiC buffer layers with skin layer on. Marina Mynbaeva and Alla Sitnikova; Ioffe Physico-Technical Institute, St.-Petersburg, Russian Federation.

It has been shown that porous silicon carbide (PSC) is an effective buffer for homoepitaxy of SiC, as it allows one to reduce the density of point defects and dislocations penetrating from the substrate into the epitaxial layer [1,2]. Another application for PSC is using it as a buffer layer for heteroepitaxy of GaN on SiC. It is known that main cause of defect formation in heteroepitaxial layers is stress is due to lattice mismatch and thermal stress due to thermal expansion coefficient mismatch. Both types of stresses, on one hand, hinder defects to penetrate from the heterosubstrate into the epitaxial layer. On the other hand, relaxation of these stresses is accompanied by formation of dislocations in the epitaxial layer. In this work, we present the data showing that using PSC buffer layers it is possible to reduce the effect of mismatch in GaN/SiC heterostructures. By employing PSC buffer layers, substabtial reduction in structural defect concentration in GaN layers was achieved. Growth experiments were performed using PSC buffer layers with various thickness and morphology of porous structure. The important role of the skin layer covering porous structure will be demonstrated. 1. Saddow S.E., Mynbaeva M., Choyke W.J., et al., Mater. Sci. Forum 353-356, 115 (2000). 2. M. Mynbaeva, S.E. saddow, G. Melnychuk, et al., Appl. Phys. Letters 78, 117 (2001).

SESSION J4: Sensors
Chair: P. Gouma
Wednesday Afternoon, April 14, 2004
Room 2009 (Moscone West)

3:30 PM *J3.1
SiC a Sensor Material for Extreme Environment.
Anita Lloyd Spetz, IFM, Linkoping University, Linkoping, Sweden.

The excellent properties of silicon carbide have paved the way for commercially available Schottky devices for high power from Infinion Technologies in Munich, Germany and UV flame detectors from General Electric in the US [1,2]. The high band gap preserves the semiconducting feature of the material even at 1000C and makes it suitable for high temperature sensors and electronics. The high melting point and chemical inertness makes it especially suitable for rough and corrosive environments, and also a biocompatible material. A metal insulator silicon carbide field effect transistor, MISiCFET, with buried source, drain and channel region has been developed [3]. It functions as a gas sensor by the application of catalytic gate metals, like Pt and Ir. The voltage at a constant current is the sensor signal, which changes to a lower voltage e.g. in the presence of hydrogen, hydrocarbons or ammonia. The sensitivity to ammonia requires a porous gate metal. The device developed by ACREO, Stockholm, Sweden, is a short channel MISiCFET device, and the baseline and the size of the gas response can be controlled by an applied negative voltage on the substrate. The MISiCFET sensors have successfully been tested in several applications. Selective Catalytic Reduction, SCR, of NOx by NH3 in the catalytic converter in diesel exhausts can be regulated by an NH3 sensitive MISiCFET sensor operated at 300C. A cold start sensor, which can be operated at 550C already a few seconds after start of the engine, will reduce emissions substantially. The combustion process in a boiler can be controlled by a MISiCFET sensor array measuring online in the flue gases. These applications require very long term stable and, especially in the case with the NH3 sensor, very selective and sensitive sensors. Nanoparticles of e.g. Al2O3 impregnated with Pt or Ir is developed as the gate material for the MISiCFET devices. This will provide a very large amount of active sites for the gas response and hopefully a very stable metal / insulator interface. The possibility to process MISiCFET sensors as a free standing chip with integrated heater and temperature control as well as processing devices on a micro-hot plate will be discussed. [1] http://www.infineon.com/cgi/ecrm.dll/ecrm/scripts/prod_cat.jsp?oid=-8681 [2] D. M. Brown, J. Kretchmer, J. Fedison, T. Dean, Electrochem. Soc. Proc. 3, 83 (2002). [3] Recent Major Advances in SiC, eds. Jim Choyke, Hiroyuki Matsunami, Gerhard Pensl, Springer, Berlin, chapter 36, pp. 879-906.

4:00 PM J3.2
Colour image sensor based on amorphous silicon carbide p-i-n structures. paula louro[1], M. Fernandes[1], A. Fantoni[1], A. Macarico[1], M. Vieira[1], N. Carvalho[2] and G. Lavareda[2]; [1]DEETC, ISEL, Lisboa, Portugal; [2]CFM, IST, Lisboa, Portugal.

Photodiodes based on p-i-n amorphous silicon structures have several applications in the field of photosensitive devices. In this work we report its use as a colour image sensor. These structures exhibit a strong dependence of the spectral response on the applied voltage, which means that the spectral sensitivity can be electrically tuned. We used several p-i-n structures based on amorphous silicon and amorphous silicon carbide produced by PE-CVD with the configuration glass/ITO/p(a SiC:H)/i(a Si:H)/n(a SiC:H)/Al-ITO. All have the same intrinsic layer and in the doped layers we changed the resistivity through the addition of methane to the doping gas. For the optical characterisation of the devices we measured the I(V) characteristics under daylight-like illumination (AM1.5) and with appropriate neutral density filters we also varied the photon flux. Interference filters with maximum transmission at wavelengths 450 nm, 550 nm and 650 nm and half width (FWHM) of 40 nm were also used in order to evaluate the I(V) characteristics under monochromatic illumination at different photon fluxes. Results show that for 650 nm illumination a higher voltage is needed for complete collection of photo-generated carriers, while for 450 nm illumination a lower voltage is sufficient to reach the wavelength-dependent saturation current. Thus, at a constant photon flux it is possible to separate different wavelengths at distinct bias voltages. The spectral response dependence on the applied voltage and on optical bias was also studied. Results show that the spectral sensitivity is strongly dependent on the applied voltage, namely the maximum spectral sensitivity shifts with the voltage, and the spectral response goes down to zero at certain wavelengths, which allows a different selectivity and enables colour recognition. In the low voltages range the red signal is suppressed allowing green recognition. The red information is obtained by tuning the voltage to higher values where the green signal goes down to zero. Combining the signal information at these voltages a colour image can be acquired. The dependence of the transport mechanism on the spectral region and on the applied bias voltage is explained taking into account the experimental data and the results obtained through a detailed numerical simulation based on the ASCA simulator.

4:15 PM J3.3
Robust Gas Sensors using 3C-SiC/Si Epitaxial Layers. John T Wolan[1], Timothy Fawcett[1], Rachael L Myers[1], Jeremy Walker[2] and Stephen E Saddow[2]; [1]Chemical Engineering, University of South Florida, Tampa, Florida; [2]Electrical Engineering, University of South Florida, Tampa, Florida.

A hydrogen gas sensor consisting of planar electrical ohmic contacts formed on the surface of a 3C-SiC epitaxial layer grown on Si(001) has been fabricated and tested. The n-type, 4 μm thick 3C-SiC epi layer was grown under low-pressure conditions with an approximate doping density of 1018 cm-3. This sensor demonstrates a two-fold repeatable improvement in stability and sensitivity in comparison to an n-type Si sensor of the same type also fabricated and tested under the same conditions. Both the 3C-SiC/Si and Si sensors operated up to 250 °C; however, the 3C-SiC/Si sensor was able to detect hydrogen at concentrations far exceeding that of the Si sensor. The 3C-SiC/Si device detected hydrogen at concentrations ranging from 0.333% to 100% in Ar while the Si sensor could only detect hydrogen at concentrations ranging from 2% to 100% in Ar. Based on this preliminary data, it has been shown that 3C-SiC/Si hydrogen sensors of this type have a larger dynamic range and higher sensitivity to hydrogen than Si sensors, thus allowing for harsh environmental applications. The 3C-SiC/Si sensor response to hydrocarbons, moisture, and air will also be presented. In addition, the second generation contact design for high temperature operation will be demonstrated.

4:30 PM *J3.4
Development of SiC-Based Gas Sensors For Aerospace Applications. Gary W. Hunter[1], Philip G. Neudeck[1], Jennifer Xu[1], Dorothy Lukco[2], Michael A. Artale[3], Peter S. Lampard[3], Drago Androjna[3], Chung-Chiun Liu[4], Darby B. Makel[5] and Benjamin J. Ward[5]; [1]NASA Glenn Research Center, Cleveland, Ohio; [2]QSS Group, Inc., Cleveland, Ohio; [3]Akima/NASA Glenn Research Center, Cleveland, Ohio; [4]Case Western Reserve University, Cleveland, Ohio; [5]Makel Engineering, Inc., Chico, California.

Silicon carbide (SiC) based gas sensors have the ability to meet the needs of a range of aerospace applications including leak and fire detection, emission monitoring, and environmental control. The ability of SiC-based gas sensors to potentially operate at a range of temperatures, in oxygen free environments, or in extreme conditions contributes to this considerable versatility. A common challenge for each of these applications is the design and operation of the sensor in such a way so as to detect the species of interest at the appropriate concentration ranges while maintaining stable operation. Each application has its own requirements. Interface issues surrounding the various components of the SiC gas sensor structure play a crucial role in determining the feasibility of the sensor for use in a given application. This structure varies depending on the application but typically includes a reactive sensing layer, an interface layer between

the sensing layer and the semiconductor, and the SiC semiconductor. This paper discusses the gas sensing needs of several aerospace applications and the use of SiC-based gas sensors, often in conjunction with other gas sensors, to meet these needs. In particular, this paper will discuss methods being used to tailor the sensor structure for the application. For example, a carbide or oxide intermediate layer can improve the sensor stability at higher temperatures while changing the sensing material decrease the sensitivity to certain hydrocarbons. Most importantly, the approach of using atomically flat SiC to provide an improved and uniform SiC semiconductor surface for sensor deposition will be discussed. Examples of the demonstration of SiC gas sensors in aerospace applications will also be given. It is concluded that, while significant progress has been made, the development of SiC gas sensor systems is still at a relatively early level of maturity for some applications.

SESSION J5: Poster Session
Wednesday Evening, April 14, 2004
8:00 PM
Salons 8-9 (Marriott)

J5.1
Abstract Withdrawn

J5.2
Aluminum-ion implantation into 4H-SiC (11-20) and (0001). Yuki Negoro, Tsunenobu Kimoto and Hiroyuki Matsunami; Electronic Science and Engineering, Kyoto University, Kyoto, Japan.

Aluminum-ion (Al^+) implantation into 4H-SiC (11-20) and (0001) has been investigated (RT). Implantations were carried out at 500 °C or room temperature. Post-implantation annealing was performed in an Ar ambient at 1800 °C with a graphite cap made from photo-resist. The graphite cap suppressed surface roughening of high-dose Al^+-implanted (0001), resulting in an excellent flatness with an rms roughness of 1.0 nm. Regarding electrical properties, a sheet resistance of 1.9 kΩ/sq. could be achieved by co-implantation with carbon ions, in the case of RT implantation into (11-20). For 500 °C implantation, the lowest sheet resistance of 1.7 kΩ/sq. was obtained by increasing the Al^+ dose up to 6.0×10^{16} cm^{-2}. The Hall-mobility (hole) differs in (11-20) and (0001). The mobility in (11-20) is 10 cm^2/Vs at RT, which is about 3 times higher than that in (0001). The temperature dependence of free hole concentration for each face is extremely weak. Annealing time dependence of sheet resistance, SIMS profile, and surface morphologies of Al^+-implanted 4H-SiC (11-20) and (0001) will be discussed.

J5.3
Morphology-controlled synthesis of nanostructured silicon carbide. Xiang-Yun Guo and Guo-Qiang Jin; State Key Laboratory of Coal Conversion, Institute of Coal Chemistry, Taiyuan, Shanxi Province, China.

The sol-gel route was employed to synthesize nanostructured silicon carbide materials. In the route, tetraethoxysilane (TEOS) and phenolic resin were used for preparing a binary carbonaceous silicon xerogel, the xerogel precursor was then temperature-programmed heated to about 1250°C and kept at the temperature for 20 hours in an argon flow. Purified β-SiC was obtained by removing excess silica, carbon and other impurities. By controlling different additives in the sol-gel process, we can obtain differently nanostructured SiC materials: (a) SiC whiskers if no additive employed, (b) SiC nanowires under the presence of alumina sol, (c) mesoporous SiC under the presence of a small quantity of nickel nitrate and (d) spherical SiC nanoparticles under the presence of excessive nickel nitrate. The different products indicate that the additives in the sol-gel process results in a self-organization of primary colloidal particles, which usually forms large secondary grains consisting of phenolic resin and embedded silica particles. The self-organization has changed the reaction environment of carbothermal reduction, as a result differently morphological SiC samples can be produced.

J5.4
600V 4H-SiC RESURF-type JFET. Satoshi Hatsukawa, Michitomo Iiyama, Kazuhiro Fujikawa and Atsushi Ito; Energy and Enviromental Technology Research Laboratories, Sumitomo Electric Industries, LTD., Osaka, Japan.

An integrated circuit module with SiC switching devices is promising, because of low loss and high temperature operation, especially in an electric or hybrid automobile. A lateral switching device is suitable for the module from the point of view of system integration. In spite of recent progress, SiC-MOSFETs have still suffered from the low channel mobility and oxide reliability. A RESURF-type JFET is suitable structure as a lateral switching device with the breakdown voltage of above 600 V for an inverter module which drives motors of an electric or hybrid automobile. In this study, 600 V RESURF-type JFETs were fabricated to investigate the operation and characteristics. The drift region between the drain and the source areas has a double RESURF structure to reduce the on-resistance. The width and the length of the channel are 200 μm and 10 μm, respectively. The distance between the drain and the gate areas, which is the drift length, is 15 μm. The fabricated devices showed normally-off operation. The threshold voltage is about 0.3 V. The saturation current is about 0.6 mA at a gate voltage of 3 V. The specific on-resistance is about 160 m$\Omega$$cm^2$. The maximum breakdown voltage is 720 V.

J5.5
Deep Level Defects in He-implanted 6H-SiC Studied by Deep Level Transient Spectroscopy. Xudong Chen, Department of Physics, The University of Hong Kong, Hong Kong, Hong Kong, China.

Deep level transient spectroscopy (DLTS) was used to study deep level defects in He-implanted n-type epi-6H-SiC samples. Low dose He-implantation (1X10$\hat{1}$1 cm$\hat{}$2) has been employed to keep the as-implanted sample conductive so that studying the annealing behavior of the He-implantation induced defects becomes feasible. Strong DLTS peaks at Ec-0.6/0.9eV and Ec-0.5eV were observed in the as-implanted sample. The intensities of the Ec-0.6/0.9eV levels increase even with filling pulse widths longer than 10 ms. The electrons captured at these traps were found to depend logarithmically on the duration time of the filling pulse. This indicates that these traps may be related to the charged dislocation defect. This peak can be significantly reduced by annealing the sample at 500 C. For the Ec-0.5eV peak, it anneals at about 300 C. Moreover, Ec-0.53eV and Ec-0.3/0.4eV (E1/E2) deep levels were found to be generated after the He-implanted sample was annealed at 500 C. ACKNOWLEDGEMENT This work is supported by the RGC, HKSAR (No.:7085/01P) and CRCG, HKU.

J5.6
The interaction of C_{60} with Si(111) and Co/Si(111). Md. AK Zilani, Hai Xu, Xue-sen Wang and Andrew Thye-Shen Wee; Physics, National University of Singapore, Singapore, Singapore.

We report STM (scanning tunneling microscopy) and XPS (X-ray photoelectron spectroscopy) studies of the interaction of C_{60} on Si(111)-7x7 and Co/Si(111) at different annealing temperatures (room temperature to ~720 °C). On Si(111), Si(100) [1], Pt(111) and Ni(110) [2], C_{60} molecules decompose completely at 900 °C, 850 °C, 780 °C and 490 °C, respectively. They form SiC at the interfaces with Si and graphite sheets with Pt and Ni surfaces, the latter surfaces catalyzing the decomposition process. Usually SiC films are grown by chemical vapor deposition at 1300-1600 °C. Due to the 8% difference in the thermal expansion coefficients and 20% lattice mismatch between Si and SiC, SiC grows with a high density of defects during high temperature carbonization process. One way to improve the crystallinity of the film and the quality of interface is to reduce the synthesis temperature. Several papers have reported growing SiC at lower temperatures (800-1000 °C) using C_{60} as a precursor on Si(100) and Si(111). One recent study using supersonic C_{60} beams on Si(111) surface reported SiC formation at 750 °C [3]. We have done a comparative study of the thermal decomposition of C_{60} on Si(111) and Co/Si(111). The C-1s core level XPS peaks show the shift of the carbon peak and formation of SiC. The C_{60} cage begins to break at ~500 °C on Co/Si(111) which is ~250 °C lower than in previous reports [4]. The C-C component disappears completely with only the C-Si component remaining at 910 °C on Si(111) and 720 °C on Co/Si(111). The growth of a small peak at the higher binding energy end of the Si-2p peak confirms SiC formation on both surfaces. Our STM images are in agreement with the XPS results where we see "ball-like" C60 molecules as well as small SiC clusters at 450 C on Co/Si(111) indicating partial decomposition of C60. STM line profiles show that some C_{60} molecules have opened their cages and formed SiC clusters with thickness of 25 Å. STM images also show localized SiC reconstructions at 625 °C and regular SiC clusters at 720 °C on Co/Si(111). We conclude that cobalt acts as a catalyst to open the C_{60} cage at significantly lower temperatures, facilitating SiC growth. References: [1] C. Cepek, P. Schiavuta, M. Sancrotti and M. Pedio, Phys. Rev. B 60, 2068-2073 (1999). [2] C. Cepek, A. Goldoni, and S. Modesti, Phys. Rev. B 53, 7466-7472 (1996). [3] L. Aversa, R. Verucchi, G. Ciullo, L. Ferrari, P. Moras, M. Pedio, A. Pesci and S. Iannotta, Appl. Surf. Sci 14 (2001) 350-355. [4] Kazuyuki Sakamoto, Daiyu Kondo, Yoshimitsu Ushimi, Masashi Harada, Akio Kimura, Akito Kakizaki and Shozo Suto, Phys. Rev. B 60, 2579-2591 (1999).

J5.7
Saturation and Flow Rate Effects on the Response of a Pd/AlN/SiC Hydrogen Sensor. Md Habibur Rahman[1], E. F. McCullen[2], L. Rimai[3], G. Newaz[4], S. Ng[1], R. Naik[2] and G Auner[3];

[1]Department of Chemical Engineering and Materials Science, Wayne State University, Detroit, Michigan; [2]Department of Physics and Astronomy, Wayne State University, Detroit, Michigan; [3]Department of Electrical and Computer Engineering, Wayne State University, Detroit, Michigan; [4]Department of Mechanical Engineering, Wayne State University, Detroit, Michigan.

Pd/AlN/SiC thin film devices were fabricated by a combination of plasma source molecular beam epitaxy (PSMBE) and magnetron sputtering techniques. A typical device consisted of 500 Å thick AlN film deposited by PSMBE on the n type 6H-SiC wafer. A circular 1 mm diameter, 1900 Å thick Pd film was deposited onto the AlN as a catalytic electrical contact and 1800 Å of Pt were deposited onto the back side of the wafer to form an ohmic contact. The metal depositions were carried out by magnetron sputtering. Details of the fabrication, as well as preliminary data on the response to Hydrogen have been presented. [1] The electrical behavior of these structures is that of a rectifying diode, the forward bias corresponding to positive Pd contact. The sensor response was obtained by monitoring the change in forward bias required to keep a preset constant current as the concentration of Hydrogen in the surrounding flow was being changed. Detailed results will be presented describing the dependence of this bias shift on hydrogen concentration and on flow rate and temperature effects. At fixed flow rate, the response initially increases roughly linearly with concentration, but eventually becomes completely saturated. The magnitude of the response as well as the saturating concentration increase with temperature. The response saturates at 60 ppm at 120 °C, and at 125 ppm at 250 °C. The magnitude of the response also increases with flow rate, up to a flow rate of about 250 sccm beyond which it remains constant. In the linear region, the magnitude of the response increases by a factor of 6 between 120 and 250 °C, at a flow rate of 250 sccm. At this flow a typical sensitivity of 0.02 V/ppm was obtained, with a detection limit of 1ppm determined by instrumental noise. Reference: 1. F. Serina, K.Y.S. Ng, C. Huang, G.W. Auner, L. Rimai, and R. Naik, Appl. Phys. Lett. 79, 3350-3352 (2001).

J5.8
The electrical behavior of Pd/AlN/Semiconductor thin film hydrogen sensing structures. L. Rimai[1], E F McCullen[2], M. H. Rahman[3], Z Linfeng[1], J. S. Thakur[1], R. Naik[2], G. Newaz[4], K. Y.S. Ng[3] and G. W. Auner[1]; [1]Department of Electrical and Computer Engineering, Wayne State University, Detroit, Michigan; [2]Department of Physics and Astronomy, Wayne State University, Detroit, Michigan; [3]Department of Chemical Engineering and Materials Science, Wayne State University, Detroit, Michigan; [4]Department of Mechanical Engineering, Wayne State University, Detroit, Michigan.

Earlier work [1,2] has shown that such structures, either on Si or on SiC substrates respond selectively to small (ppm) concentrations of H2 in the surrounding gas flow, but in different manner. The device on Si substrates behaves as an MIS capacitor with the AlN playing the role of insulator, and the responds to Hydrogen is given by a shift of the depletion capacitance vs. bias (C(V)) profile along the bias voltage axis. The device on SiC behaves as a rectifying diode and the presence of hydrogen causes a shift of the forward current vs voltage (I(V)) plot. Furthermore, the reverse bias dependence of the capacitance of the latter device does not exhibit the characteristic shape of that for a MIS capacitor. In this report we present detailed measurements of the electrical characteristics of the Pd/AlN/SiC devices. They show behavior which is consistent with that expected from an AlN/SiC heterojunction, with an apparent barrier height in the absence of hydrogen of about 1.5 eV (AlN thickness of 500 Å). In the presence of 100 ppm of hydrogen, at 250 °C this barrier is reduced by about 0.25 V. The magnitude of this response is in the same order as the shift in the C(V) curve of the Si based device with approximately the same thickness and at the same temperature. It will be shown that the response of either type of device can be explained as resulting from the accumulation of positive charges within the AlN but in the vicinity of he Pd/AlN interface. The source for these charges are the catalytically dissociated atoms of Hydrogen which diffuse through the Pd and at the interface with the AlN leave the electron behind in the conduction band of the Pd. These charges (protons) set up an additional voltage across the structure thus resulting in the observed shifts. Whether the AlN behaves as a near ideal insulator, or as a semiconductor will depend on the distribution of conduction electrons (and or holes) across the layers. These experimental results can be analyzed to obtain information about the difference in such distributions for the two types of structures. Reference: 1. F. Serina, K.Y.S. Ng, C. Huang, G.W. Auner, L. Rimai, and R. Naik, Appl. Phys. Lett. 79, 3350-3352 (2001). 2. F. Serina, C. Huang, G.W. Auner, R. Naik, S. Ng, and L. Rimai, Pd/AlN/ Si or SiC Structure for Hydrogen Sensing Device, Mat. Res. Soc. Symp. Vol. 622 (2000)

J5.9
Growth of Large Diameter Semi-Insulating 6H SiC Crystals by Physical Vapor Transport. Murugesu Yoganathan[1], Avinash Gupta[1], Edward Semenas[1], Ejiro Emorhokpor[1], Christopher Martin[1], Thomas Kerr[1], Ilya Zwieback[1], Andrew Souzis[1], Thomas Anderson[1], Charles Tanner[2], John Chen[2], Donovan Barrett[1,2], Richard Hopkins[2], Carl Johnson[2], Fei Yan[3], W. J. Choyke[3] and R. P. Devaty[3]; [1]Wide Band Gap Materials Group, II-VI, Inc., Pine Brook, New Jersey; [2]Wide Band Gap Materials Group, II-VI, Inc., Saxonburg, Pennsylvania; [3]Department of Physics and Astronomy, University of Pittsburgh, Pittsburgh, Pennsylvania.

Semi-insulating 6H SiC boules of up to 100mm diameter have been grown using the physical vapor transport (PVT) technique. The importance of void-free seed bonding and defects originating from voids in the seed bond layer are discussed. The semi-insulating properties are achieved by compensating shallow acceptors (or donors) by vanadium. The micropipe densities have been substantially reduced during the last year as compared to our previously quoted values. The typical room temperature resistivity (under room light illumination) for vanadium-doped semi-insulating 6H SiC substrates is about 108Ωcm. The issues related to non uniformity of vanadium doping are discussed. Low temperature photoluminescence (LTPL) data will be presented showing the Ti lines in the visible spectrum and the V lines in the near infrared. Luminescence lines associated with other deep centers will also be reported.

J5.10
A kinetic model for doping in silicon and silicon-carbide epitaxy by CVD. Bhavesh Mehta and Meng Tao; University of Texas at Arlington, Arlington, Texas.

A kinetic model based on 1) the collision theory of heterogeneous unimolecular elementary reactions, 2) statistical physics, and 3) the concept of competitive adsorption is proposed for doping in silicon and silicon-carbide epitaxy by chemical vapor deposition (CVD). The model provides analytical equations to describe carrier concentration as a function of deposition conditions including temperature and partial pressures of various precursors. The model agrees well with the experimental data for both p-type and n-type doping in silicon epitaxy. It also predicts the carrier concentration as a function of the carbon to silicon ratio in silicon-carbide epitaxy. By assuming the reaction mechanism for a precursor, the model also presents a method to estimate the activation energy for the particular heterogeneous reaction. This model has been successfully applied to describe the kinetics of thermal CVD, photo-CVD, and MOCVD.

J5.11
Formation of Si/SiC Heterostructures for Silicon-based Quantum Devices Using Single CH_3SiH_3-gas Source Free Jet. Ryota Ohtani, Yoshifumi Ikoma and Teruaki Motooka; Department of Materials Science and Engineering, Kyushu University, Fukuoka, Japan.

Silicon carbide (SiC) can be epitaxially grown on Si(100) substrates and the SiC/Si(100) heterointerface has a large band offset. Therefore, SiC is potentially useful for applications to silicon-based quantum devices. Recently, we successfully formed Si/SiC heterostructures by supersonic free jet CVD, using Si_3H_8 and CH_3SiH_3. In this study, we have investigated formation of SiC/Si/SiC/Si(100) heterostructures utilizing single gas source, CH_3SiH_3 10% diluted by H_2. At first, the substrate temperature was set at 850 °C and a SiC layer was grown on Si(100) by irradiation of 18000 free-jet pulses. Then the substrate temperature was reduced at 600 °C and a Si layer was formed on SiC layer by irradiation of 18000 pulses. For growth of the Si layer, CH_3SiH_3 jets were excited using a tungsten hot filament. Finally, the substrate was heated again at 850 °C and the top SiC layer was grown by irradiation of 18000 pulses. These samples were characterized by using cross-sectional transmission electron microscopy and x-ray photoelectron spectroscopy measurements. It was found that SiC (∼5 nm)/Si (∼20 nm) multilayes were successfully formed on epitaxial SiC layers (∼15 nm). Electrical measurements characterizing the SiC/Si/SiC quantum confinement effects are currently under way.

J5.12
SiC power diodes improved by fine surface polishing. Philippe Godignon[1], Raul Perez[1], Dominique Tournier[1], Narcis Mestres[1], Hugues Mank[2] and Daniel Turover[2]; [1]Power Dept., Centro Nacional de Microeletronica, Cerdanyola, Barcelona, Spain; [2]R&D, NOVASIC, Le Bourget du Lac, France.

Surface polishing can be considered as a potential technological process to improve electrical and reliability characteristics of SiC devices. It is already used as surface treatment prior to epilayer growth on SiC substrates. In this work we take profit of a novel fine polishing process to improve the electrical characteristics of Boron implanted Schottky and pn planar diodes. The mentioned fine polishing process allows to remove a layer thickness of 100nm to 3000nm on the surface of a processed SiC wafer. The impact of this process on the surface properties of the sample is analysed in this

paper through both physical characterisation and electrical characterisation using a highly surface quality sensitive devices such as high voltage Schottky diodes. Schottky and pn planar diodes have been fabricated using room temperature Boron implantation to form the JTE termination as well as the P+ anode of the pn diodes. The targeted breakdown voltage is 2.5KV. One of the critical step is the high temperature annealing, performed at 1700C, which degrades the samples surface but is necessary to correctly activate the Boron impurities. After this process, the RMS measured by AFM is 10.7nm on 5mmx5mm area and can reach 20.9nm on 15mmx15mm area in some parts of the sample. The measured breakdown voltage of the diodes is in the range of 900-1100V. The ohmic contacts made on the pn diodes are rectifying. This is due to the fact that the boron implanted near the surface has exodiffused and the true concentration of boron impurities is far less than expected in this near surface region. This has a direct impact on the JTE termination efficiency and the ohmic contact formation. After removing the top layers of metal and passivation, fine polishing process has been made. The RMS values measured by AFM after the polishing are 1.4nm on 5mmx5mm area and maximum 5.35nm on 15mmx15mm area in some parts of the sample. The diodes have been fabricated again with the same process and mask set. After the polishing process, we do not observe a degradation of the forward characteristics of the diodes. Schottky barrier, ideality factor and On-resistance are almost unchanged. At low current, we see an improvement of the I-V characteristics, indicating a possible removal of surface defects in localised part of the sample. In the reverse mode we observed a clear improvement of breakdown voltage. This results is due to several factors. First of all, it is due to the elimination of surface un-doped region caused by the Boron exodiffusion. Second, there is also an improvement of surface roughness and a removal of residues thanks to the polishing step. We are also expecting a possible improvement of yield on large area devices. This point is under study and will be presented at the conference.

J5.13

First Observation of Deep Level Defects in 4H SiC Diodes with Magnetic Resonance. Shane K. Yerkes[1], Patrick Lenahan[1] and Robert S. Okojie[2]; [1]The Pennsylvania State University, University Park, Pennsylvania; [2]NASA Glen Research Center, Cleveland, Ohio.

We report the first observation of deep-level defects in 4H SiC PIN diodes with a very sensitive electron spin resonance technique called spin-dependant recombination (SDR). The diodes were subjected to high current stressing prior to SDR measurements. We observe a relatively strong SDR signal consisting of at least two peaks. The stronger peak has a g value of approximately 2.005 when the magnetic field is oriented parallel to the crystalline c-axis. The stronger signal exhibits weak g anisotropy. Although we have yet to develop a detailed model of the defect structure, we very tentatively link the paramagnetism to unpaired electrons in silicon wave functions. The SDR amplitude is a strong function of forward bias voltage; the signal is strongly peaked at a forward bias of 2.2 volts. This result is consistent with, and strongly supports the idea that the observed signal is caused by deep-level defects (presumably involving stacking faults) which play dominating roles in recombination events in the depletion region of the diodes. According to Lindefelt and coworkers, a stacking fault in 4H-SiC PiN diode acts as a one-dimensional quantum well, thus altering the physical and electronic properties of the crystal [1]. This idea is based on total energy calculations of a 4H-SiC crystal containing an intrinsic SF, where it has been found that a narrow band is split off from the bottom of the conduction band and extends about 0.2 eV into the bandgap of 4H-SiC [2]. [1] U. Lindefelt and H. Iwata, in "Recent Major Advances in SiC", Springer-Verlag, Berlin (2003). In press. [2] M. S. Miao, S. Limpijumnong, and W. R. L. Lambrecht, Appl. Phys. Lett. 79(26), p. 4360 (2001).

J5.14

Transient Enhanced Diffusion of Boron in 4H and 6H SiC Co-implanted With Boron and Nitrogen Ions. Igor Usov[1], A A Suvorova[2] and A V Suvorov[3]; [1]MST-STC, Los Alamos National Laboratory, Los Alamos, New Mexico; [2]Centre for Microscopy and Microanalysis, University of Western Australia, Crawley, Western Australia, Australia; [3]Cree Inc., Durham, North Carolina.

The effect of boron (B^+) and nitrogen (N^+) co-implantation in silicon carbide (SiC) wafers on subsequent transient enhanced boron diffusion during annealing has been investigated. 4H and 6H SiC n-type epitaxial films were co-implanted with 90 keV B^+ and 150 keV N^+ with ion doses $2x10^{14}$ cm^{-2} and $5x10^{13}$ cm^{-2}, respectively. The energy of nitrogen ions was chosen in such a way that their projected range was 50 nm deeper that of boron ions. Samples implanted with only B^+ and N^+ were also prepared for comparison. The annealing was performed at 1700 ^oC in a rapid thermal annealing system under argon overpressure of 1 atm or in a vacuum furnace under silicon and carbon vapors. The annealing time was varied from 10 sec to 30 min. Boron and nitrogen depth profiles were measured by secondary ion mass spectroscopy. Transmission electron microscopy has been used to determine the structural properties of implanted layers. Nitrogen concentration profiles remained unchanged after the annealing. Boron atoms showed strong out- and in-diffusion in both studied SiC polytypes. Deep penetrating diffusion tails extending up to 4 μm were observed in samples both implanted with only B^+ and co-implanted with N^+. However, the amount of mobile boron atoms, which formed the tail region, was approximately 4 times less in the co-implanted samples as opposed to samples implanted with B^+. Boron diffusion parameters in 4H and 6H SiC have been determined and boron diffusion mechanism has been discussed.

J5.15

Porous GaN/SiC templates for epitaxial growth. Marina Mynbaeva[1], Andrei Sarua[2] and Martin Kuball[2]; [1]Ioffe Physico-Technical Institute, St.-Petersburg, Russian Federation; [2]H.H. Wills Physics Laboratory, University of Bristol, Bristol, United Kingdom.

Despite much progress in III-nitride technology, the task of reducing the density of defects caused by micmatch in parameters of III-nitride epitaxial layers and foreign substrates is still on the agenda. One of the ways to reduce the defect density in epitaxially grown material is to use porous buffer layer formed on the substrate surface. Our preliminary results on the growth of GaN epitaxial layers on porous GaN/SiC structures, obtained on 1x1 cm2 samples, showed that porous substrate allowes one to improve epitaxial growth of GaN [1]. In this work, we report on the development of porous GaN/SiC templates with 2" in diameter. We show that by selecting optimal formation conditions it is possible to fabricate porous substrate with reduced level of residual strain, as compared to initial GaN/SiC heterostructures. Most remarkable is the fact that to reduce the strain to the minimum possible value, porous structure in GaN/SiC template must be developed not only in the GaN layer, but in the SiC substrate as well. We discuss technology matters related to fabrication of porous templates with such type of structure. 1. M. Mynbaeva, A. Titkov, et al. MRS Internet J. Nitride Semicond. Res. 4, 14 (1999).

J5.16

Laser Direct Write of a Tunable SiC Filter for Sensor Applications. Islam Salama[2], Nathaniel R Quick[1] and Aravinda Kar[2]; [1]AppliCote Associates, LLC, Lake Mary, Florida; [2]University of Central Florida, Orlando, Florida.

Laser direct write fabrication of a silicon carbide optical filter with a tunable response in the infrared (IR) regime of the electromagnetic spectra is presented. The approach relies on the fact that the optical properties of n-type 4H-SiC are controlled by its free carrier concentration. A laser direct write technique is used to fabricate metal-like contacts in situ in n-type 4H-SiC (approximately 5 x 10E19/cc)substrates generating a conductor-semiconductor-conductor structure without the addition of metal. Application of a biasing voltage, either forward or reverse, between two contacts in this structure affects the optical transmissivity of the n-type SiC semiconductor. The transmission increases as the magnitude of the applied voltage increases for wavelengths higher than 1500 nm at an applied bias of 5-7 volts. For an applied bias of 9 volts, the transmission increased over the entire spectra (200-2500 nm). However, at this biasing level, the maximum absorption (approximately 470 nm) did not change. In the wavelength range 2000-3000 nm the transmission is a maximum at 2400 nm which is follwed by a rapid decay in the transmissivity leading to a minimum value at 2670 nm. The difference between the maximum and minimum values increases with the applied bias. These results indicate that the laser fabricated SiC conductor-semiconductor- conductor device can act as a tunable optical filter in the infrared regime. The origin of the tunability is related to the free carrier absorption phenomenon, i.e., the free carrier response to the incident electromagnetic field, at the IR wavelength, in the presence of the biasing voltage or the electric field. When the sample is under no external bias the optical transmission at a given photon energy smaller than the bandgap is controlled by both the sub-bandgap transition and free carrier absorption. This tunable filter will select radiation for detection by a SiC Schottky diode sensing element fabricated by laser doping and laser metallization.

J5.17

Fabrication of SiC microtubes with a villus-like microstructure. Jae-Won Kim[1], Seoung-Soo Lee[1], Yeon-Gil Jung[1], Je-Hyun Lee[1] and Chang-Yong Jo[2]; [1]Material Science and Engineering, Changwon National University, Changwon, Kyungnam, South Korea; [2]High Temperature Materials Group, Korea Institute of Machinary and Materials, Changwon, Kyungnam, South Korea.

Silicon carbide microtubes were successfully fabricated by reacting between SiO vapors and carbon microfibers. Silicon carbide precursor

was prepared by mixture of Si/ SiO_2. The precursor leaded to complete conversion of (SiO_{gas}+ C_{solid}) into (SiC_{solid} +CO_{gas}) through overall reaction with heat treatment under inert gas flow at temperature higher than 1623K. The amount of unreacted carbon was determined by thermogravimatric analysis (TG/DTA), fourier transfer infrared spectroscopy (FTIR) and scanning electron microscopy (SEM). Low surface area (1 2 m^2g^{-1}) of carbon fibers was gradually converted to high specific surface area SiC microtubes (50 100 m^2g^{-1}) after removing of the residual carbon by oxidation. Inner surface of SiC microtubes showed a villus-like microstructure, which consists of sub-micron ($\leq$0.5mm) sized SiC particles, while outer surface of SiC microtubes was smooth. The smooth inner surface of SiC microtubes transformed into villus-like morphlogy with increasing sintering temperature. The thickness of villus-like layer in the SiC microtube also increased with increasing sintering temperature.

J5.18
Epitaxial Growth of 2 inch 3C-SiC on Si Substrates by Atmospheric Hot Wall CVD. Jiliang Zhu, Yi Chen, Yusuke Mukai, Akira Shoji, Satoru Ohshima and Shigehiro Nishino; Electronics and Information Science, Kyoto Institute of Technology, Kyoto, Kyoto, Japan.

As a high mobility, wide bandgap semiconductor, 3C-SiC has great promise. In this paper, we examined to obtain 3C-SiC epilayer on Si substrates using hot-wall CVD furnace and report the use of hexamethyledisilane (HMDS) and propane as reaction gases to grow uniform thickness on 2 inch (100) ,(111),(110) and (211) orientation of Si substrates. A horizontal atmospheric pressure CVD reactor was used. A reaction zone was specially designed. The suceptor has a square hole, 60 mm wide,8 mm high and 110 mm long. To obtain uniform thickness of the epilayer, inside of the susceptor hole was intentionally tapered along flow direction as follows; inlet of the square hole is 11 mmx60 mm and outlet of the hole is 4 mm x 60 mm. The susceptor was surrounded by graphite foam. Temperature of the suscepotor was measured at inside wall of the susceptor by optical pyrometer. HCl flow rate for etcnig was 1.0 - 2.0 sccm. An initial carbonization procedure was performed using 1 sccm propane at 1250 oC for 2-3 minutes. During the growth of SiC at 1300 oC for 1 hour, the flow rate of HMDS was 0.75-1.2 sccm and the flow rate of propane was 0.1-0.5 sccm . The hydrogen carrier gas flow rate was 3-10 slm. Typical growth rate was 3 micron /h. Uniform thick 3C-SiC was obtained. The samples were examined using optical microscopy, SEM and RHEED. Electrical properties are also discussed

J5.19
Characterization and Mapping of Crystal Defects in Silicon Carbide. Ejiro T Emorhokpor[1], Thomas Kerr[1], William T Elkington[2], Ilya Zwieback[1], Michael Dudley[3], Thomas Anderson[1], John Chen[2] and Carl Johnson[2]; [1]Wide Bandgap Materials Group, II-VI Inc., Pine Brook, New Jersey; [2]Wide Bandgap Materials Group, II-VI Inc., Saxonburg, Pennsylvania; [3]Department of Materials Science and Engineering, State University of New York at Stony Brook, Stony Brook, New York.

A method is presented for detecting, counting and mapping dislocations and micropipes in n+, undoped, and semi-insulating Silicon Carbide wafers. The technique is based on etching in molten Potassium Hydroxide (KOH). The polish-etch regime of the etching process has been optimized to produce etch pits which allow quick and accurate analysis of the optical contrast. Etch pits from dislocations and micropipes are detected and differentiated by an image processing system that is sensitive to the optical reflection profile of the etch pit. The instrument probes an area of 700 x 700 mm$\hat{2}$ and is capable of producing topographic maps showing distribution of dislocation and micropipe densities (MPD). The MPD scan time for 2-inch wafers is less than two hours per wafer. The created MPD maps are in good agreement with the contrast images produced by the Synchrotron White Beam X-Ray Topography.

J5.20
The Effect of Doping Concentration and Conductivity Type on Preferential Etching of 4H-SiC by Molten KOH. Ying Gao[1], Zehong Zhang[2], Robert Bondokov[2], Stanislav Soloviev[2] and Tangali Sudarshan[2]; [1]Bandgap Technologies, Inc., Columbia, South Carolina; [2]University of South Carolina, Columbia, South Carolina.

Molten KOH etching of SiC is a simple and effective method for revealing structural defects. However, it has been reported that molten KOH etching is better able to identify specific defects in medium and low doped n-type wafers than in highly doped SiC wafers. This is a more effective defect delineation tool when preferential etching is enhanced compared with isotropic etching. In this work, molten KOH etching was implemented to delineate defects on the Si-face of on- and off-axis n- and p-type 4H-SiC samples with different doping concentrations. The dimensions of the etch pits were compared using Normaski Differential Interference Contrast (NDIC) microscope. The etch preference is significantly influenced by both the doping concentration and the conductivity type. The etch preference for Si-face 4H-SiC substrates is n+ < n- < p- $\approx$ p+. It is concluded that the molten KOH etching process is a combination of a chemical and an electrochemical process, during which the isotropic etch rate and preferential ecthing are competitive. Based on the above observations, the n+ 4H-SiC wafer was converted to p-type by diffusion of boron followed by molten KOH etching at 600 ^oC for 10 min. The results clearly showed three kinds of distinguishable etch pits corresponding to threading screw, threading edge and basal plane dislocations even in highly doped n+ substrates. In addition, this approach has been used to investigate defect correlation between the 4H-SiC epilayer and substrate.

J5.21
Photoluminescence Characterization of Defects Introduced in 4H-SiC During High Energy Proton Irradiation and Their Annealing Behavior. Mo Ahoujja[1], H C Crocket[2], M B Scott[2], Y K Yeo[2] and R B Hengehold[2]; [1]Physics, University of Dayton, Dayton, Ohio; [2]Engineering Physics/ ENP, Air Force Institute of Technology, WPAFB, Ohio.

The robust nature of SiC makes it an ideal material in both space-based and high temperature environments where conventional Si and GaAs based devices would fail. However, a clear understanding of how SiC behaves under a radiation environment is required before it is incorporated in devices for space applications. In this paper, we report on the optical properties of defects introduced in epitaxial 4H-SiC by 2 MeV protons using photoluminescence spectroscopy. The near band edge characteristics of nitrogen-doped n-type 4H-SiC are present in the optical spectrum of the as-grown samples. Following a proton irradiation, the material is altered and the luminescence of the shallow centers is attenuated almost entirely with the emergence of deeper shallow traps at energies greater than 350 meV below the conduction band. Subsequent high-temperature thermal annealing of the material results in an increase in the emission spectrum at both the near band edge region (Eg = 3.25 eV) and between 2.65 and 2.95 eV. Recovery of the characteristic nitrogen-related peaks at the near band edge following high-temperature annealing (TA) is identified, but is not complete at TA = 1500 oC. In the deep trap region below 2.95 eV, activation of trap centers with annealing results in a sharp increase in the signal intensity of an irradiation-induced defect trap (2.90 eV) as well as the associated phonon replicas. Based on previous ion-implantation studies in 4H-SiC, the emergence of the 2.90 eV defect complex and associated phonon replicas may not be related to hydrogen implantation as a result of the proton irradiation, but instead as a result of the ensuing lattice damage.

J5.22
High Resolution Optical Defect Mapping in High-Resistivity Boron-Doped Silicon Carbide Wafers. Millard G Mier and John J Boeckl; US Air Force, Wright Patterson AFB, Ohio.

Silicon carbide (SiC) is a promising materials system for extreme-environment high power substrates. While the carrier mobility in SiC itself limits performance to X-band frequency, higher-mobility device layers can use the high thermal conductivity of SiC to dissipate heat. This environmental tolerance comes with a price: SiC has no useful melt phase and new growth technology had to be developed. The leading technique involves growth by physical vapor deposition (PVD). A number of defects unique to the PVD growth have appeared, the most troublesome being the micropipe (uP), a hollow hexagonal screw dislocation running along the growth axis. These uPs can have any size from sub-micron dimensions to hundreds of microns. It is a tribute to the ability of SiC crystal growers that uP density is typically no greater than a few tens per cm2. The uP defect, unfortunately, propagates into epitaxial device layers grown on SiC substrates. Even small uPs degrade device performance severely and must be avoided. We show here a nondestructive whole-wafer visible-light optical technique for high-resolution mapping of defects, including uPs, in bare SiC wafers and measure a number of experimental 2-inch boron-doped high-resistivity SiC wafers. Substrate wafer information is stored in a conventional compressed bitmap file and can be restored and analyzed at full resolution for comparison to device and device failure results. Defects located by this analysis of optical data are confirmed by conventional optical and scanning electron microscopy techniques. We have obtained both transmission and reflection visible-light scans of the whole wafers at various resolutions down to one micron resolution. Our analysis of this data reveals and allows us to map the locations of optically detected defects in each wafer. We conclude that the intrinsically nondestructive technique of visible-light optical scanning with the data stored in a compressed bitmap is a practical way to collect and store substrate information for troubleshooting subsequent processing difficulties.

J5.23

Structural characterization of 3C-SiC films grown on Si layers wafer bonded to polycrystalline SiC substrates.

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Single crystal 3C-SiC epitaxial layers have been grown on SOI substrates using low-pressure chemical vapour deposition (LPCVD). The SOI substrates consist of nominally 150Å Si layers bonded to 100 mm poly 3C-SiC substrates using direct wafer bonding and SOI film transfer techniques. Miscut Si(100) films were incorporated into the wafer bonding process for the first time in an effort to further reduce anti-phase domain formation in the 3C-SiC films. The Si films were transferred from Si(100) wafers miscut 4° toward the (110) direction. For growth of 3C-SiC layers, a two-step process is needed. First the Si is carbonized using propane mixed in a hydrogen carrier gas to convert the surface to SiC at atmospheric pressure. Next SiC growth is conducted by the addition of silane into the gas mix and a reduction of the process pressure to 150 Torr. Characterization of these films via SEM and XRD indicate that the films are single crystal and oriented with respect to the starting Si bonded film. The films are of high quality and XRD FWHM of less than 600 arc-sec have been achieved. In this work we present results of TEM analysis of these films which show details of the atomic structure at the 3C-SiC/poly-crystalline SiC interface where an amorphous region is observed, likely the SiO_2 originally present between the bonded Si film and poly SiC substrate. The TEM cross sections indicate that the Si film is wholly carbonized which is advantageous for more optimized growth temperatures exceeding the melting point of Si. A detailed study of this material system is presented with the aim of providing feedback for possible improvements in the 3C-SiC growth process.

J5.24

6H-SiC Bulk Growth by Advanced PVT.

Avinash Gupta[1], Yoganathan Murugesu[1], Edward Semenas[1], Ilya Zwieback[1], Ejiro Emorhokpor[1], Christopher Martin[1], Thomas Kerr[1], Andrew Souzis[1], Thomas Anderson[1], John Chen[2], Charles Tanner[2], William Elkington[2], Donovan Barrett[2], Richard Hopkins[2] and Carl Johnson[2]; [1]Wide Bandgap Materials Group, II-VI, Inc., Pine Brook, New Jersey; [2]Wide Bandgap Materials Group, II-VI, Inc, Saxonburg, Pennsylvania.

II-VI, Inc. is intent to become a major commercial supplier of high-quality SiC substrates. Semi-insulating 6H-SiC single crystals, doped with vanadium and vanadium-free have been grown using Advanced PVT growth technique (APVT). The APVT process incorporates synthesis of ultra-high purity SiC from semiconductor purity Si and C sources. The synthesized polycrystalline SiC demonstrates very low background contamination with impurity levels of B, Al and transition metals below their GDMS detection limits. 6H-SiC crystals grown by APVT have been extensively characterized with respect to their purity, crystal quality and electrical properties. COREMA resistivity maps showed that V-compensated boules exhibit axially and radially uniform resistivity around 1E11 Ohm-cm at room temperature. V-free undoped wafers contained residual boron and nitrogen at levels below 1E16 atoms/cm3, and demonstrated semi-insulating properties (resistivity between 1E6 and 1E11 Ohm-cm) as a result of compensation by native point defects with deep levels in the bandgap. High-quality wafers contain micropipes with their density below 10 cm-2 and dislocation density on the order of 1E4 cm-2.

J5.25

Characterization and comparison of a-plane and 8-dgree off-axis c-plane 4H-SiC homoepitaxial films and their substrates.

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Structural, microstructural, electrical and optical characterization of a- and c-plane 4H-SiC homoepitaxial films and their substrates have been conducted. The number of domains and the range of x-ray rocking curve full-width half-maxima values for a-plane wafers and films were markedly smaller than analogous values acquired from the c-plane materials. Atomic force microscopy of the surface of the as-received a-plane wafer measured a roughness of 0.52 nm RMS. Hydrogen etching of the former surface for 5 and 30 minutes reduced the RMS roughness from 0.52 nm to 0.48 nm and to 0.28 nm, respectively; the RMS value for a 30 micron film was 0.52 nm. Micropipes in the a-plane substrates did not thread beyond the film-substrate interface. Hall measurements of the a-plane films yielded a bulk mobility of 12,200 and 800 cm2̂/Vs at 100 K and 300 K, respectively, with a carrier concentration ranging from 3.1x10Î4/cm3̂ at 100 K to 7.4x10K̂14/cm3̂ at 300 K. These data indicate higher electron mobilities than reported previously for c-plane 4H-SiC films. The sharp free exciton line present in a-plane photoluminescence data indicates low impurity content. The results of additional investigations will also be presented, including structural characterization of the density and distribution of defects in these materials as well as preliminary electrical characterization of a- and c-plane PiN diodes.

J5.26

Characterization of defects generated by boron diffusion in SiC.

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The diffusion of implanted boron (B) in silicon carbide (SiC) has been studied by using secondary ion mass spectrometry (SIMS) and photoluminescence (PL) spectroscopy and imaging. The focus of this paper is using a new approach to investigate the nature of defects generated by B implantation and thermal annealing. A commercial 4H-SiC(1000) substrate with an n-type epitaxial layer was implanted with $2x10^{14}$ atoms/cm^2 B. The sample was annealed at approximately 1700°C for about 1 second. High-resolution scanning PL images were acquired to determine the doping distribution of the as-implanted and annealed samples. Following annealing, various thicknesses of the sample were removed by mechanical polishing, and low temperature PL spectrum measurements were obtained to investigate the changes in the PL spectra with depth. The thermal annealing generated a B diffusion profile measured by SIMS to extend to about 3 microns depth. PL measurements were specifically taken on the as-implanted sample, the unpolished activated sample, and the sample with the diffused B layer removed by polishing off the top 2 to 3 microns of the sample. PL measurements were also made after removing another 3 microns of material. These measurements allow us to trace the variation of the PL spectrum and further explore the nature of the defects induced by the B implantation and thermal annealing. It is found that after removing the diffused B layer, the spectral feature at 415 nm disappears, which is consistent with its previous identification as arising from donor-acceptor pairs (DAP) [1]. The D1 spectral features survive after polishing B layer off the sample, supporting previous suggestions that these features are due to the di-interstitial (C-C or Si-Si) or di-vacancy (C-C or Si-Si) defects. [1]. Y. Tanaka, et al, Materials Science Forum 338-342 (2000) 909.

J5.27

Core Structure and Properties of Partial Dislocations in Silicon Carbide p-i-n Diodes.

Seoyong Ha, Mourad Benamara and Marek Skowronski; Carnegie Mellon University, Pittsburgh, Pennsylvania.

The electroluminescence, mobility and core structure of partial dislocations bounding stacking faults in silicon carbide p-i-n diodes were investigated using optical emission microscopy and transmission electron microscopy. It is well-known that the motion of partial dislocations in diodes under forward bias is responsible for formation of stacking faults and the degradation of diodes. In order to understand this phenomenon, the mechanism of the dislocation glide should be identified. It is generally accepted that the properties of partial dislocations in semiconductors are determined by their core structure. The results presented below indicate that such relationship also exists for the partial dislocations in silicon carbide. The p-i-n diodes examined in this study were fabricated on a 35 mm diameter, 4H-SiC, n-type substrate (n=5x1018 cm-3). The substrate was off-cut by 8 degrees from the [0001] toward the [11-20] direction and the diodes were processed on the silicon-face. The low-doped (n 1015 cm-3) blocking layer (35 microns) and the p-type anode were deposited by horizontal hot-wall chemical vapor deposition method. Standard metal contacts were formed on the diode surface and substrate backside. Diode mesas were defined by reactive ion etching. Optical emission microscopy was applied to record the evolution of dislocations during the forward operation of the diodes. A liquid-nitrogen cooled, UV sensitive camera and an optical microscope mounted on a probe station were used. Pre-existing dislocations in the blocking layer could be imaged as bright spots and lines due to preferential recombination of electrons and holes along the dislocation lines. The dislocations moved and stacking faults developed during high current biasing with current densities between 0.1 and 10 A/cm2. Their bounding partial dislocations showed two distinct characteristics. Bright luminescent segments were mobile while dark invisible ones were stationary. The core nature of the different segments was determined by transmission electron microscopy. The locations of dislocation segments could be traced throughout the sample preparation by comparing the diode emission microscopy

images with the optical micrographs of the sample taken in each step of preparation. Using this technique, we could uniquely correlate each partial dislocation observed in transmission electron microscopy with it recorded in optical emission microscopy. Burgers vector analyses performed by applying different techniques indicated that the mobile segments are silicon-core 30 degrees partial dislocations while the immobile segments are carbon-core 30 degrees ones.

J5.28

Novel approach of 6H-SiC single crystal growth for diameter enlargement. Soo-Hyung Seo, Crystal Growth Division, Neosemitech Corp., Inchon, South Korea.

Silicon carbide(SiC) grown by sublimation method is considered to be on of wide bandgap materials promising for high-temperature and high-voltage power electronic device applications and optical sensors in the ultraviolet region. Low defect and large diameter SiC crystals are necessary for develpment of SiC-based devices. From an industrial viewpoint, also, the diameter of 2 inches is insufficient for device applications from now on and the enlargement of diameter from small seed to either 3 inches or 4 inches demands a long time. In this study, we demonstrate a novel approach for rapid enlargement of SiC crystal diameter. This method includes the assembling together several SiC seeds which are the precisely cut and crystallographically oriented single crystals plates along the well aligned pattern called as a mosaic arrangement. In previous works, the successful growth of SiC crystal using an alternative mosaic arrangement has not been exhibited until now and this result has not still been reported in monograph. Consequently, we present the possibility and realization to overgrow the diameter of 6H-SiC crystals using mosaic arrangement. 6H-SiC (0001)-oriented seeds were precisely cut as square of 10 x 10 mm^2 and they were attached on graphite lid as a mosaic arrangement. The various mosaic conditions were artificially considered for the evaluation of possible effects such as the widths of junction gaps, the misaligned angle, and the rotated arrangement during the process of seed attachment. The abrasive-grade SiC powder was etched in hydrogen chloride solution for removing metal impurities and was used for the source material. As-grown SiC surfaces and junction morphologies were investigated for step structures and the connected shape at junctions between seeds by using an optical microscopy with Normarski interference contrast and AFM(atomic force microscopy). The connected properties of as-grown surface at junctions were improved under low growth rate, high operation pressure, narrow junction widths, and so on. Micro-Raman spectra for analysis of polytype formation at junctions are obtained at room temperature by Renishaw micro-Raman spectrometer(Series 1000) attatched to a optical microscopy. The exitation was carried out with the Ar laser (514nm, 25mW) focused on the 6H-SiC surface and the focusing beam size is about 2μm in diameter. From Raman spectra, the polytypes except 6H-SiC were not confirmed at junctions. Furthmore, the analysis data of the crystallographic and spectroscopic properties on the overgrowth at junctions are presented though employing high-resolution XRD, photoluminescence, FE-SEM(field emission scanning electron microscopy) to elucidate the growth behavior at junctions.

J5.29

Photoluminescence at 1540 nm from erbium implanted amorphous silicon carbide films. Spyros Gallis[1], Harry Efstathiadis[1], Meng Bing Huang[1], Ei Ei Nyein[2], Uwe Hommerich[2] and Alain E Kaloyeros[1]; [1]School of NanoSciences and NanoEngineering, The Univestity at ALBANY-SUNY, ALBANY, New York; [2]Department of Physics, Hampton University, Hampton, Virginia.

Erbium (Er) implanted material systems have received significant attention, since the Er^{3+} exhibits an optical transition around 1540 nm, a wavelength falling in the window of minimal absorption for silica optical fibers used in optical communications. In particular, implanting silicon carbide (SiC) with Er can further extend the application of SiC as a light source to the technologically important wavelength of 1540 nm. In this work, we report on strong room temperature photoluminescence (PL) from Er-implanted and post-annealed amorphous silicon carbide (a-SiC:Er) films. The stoichiometric SiC films were grown by thermal chemical vapor deposition (TCVD), then implanted to Er fluences in the range of 5×10^{13} to $1\times x10^{16}$ ions/cm^2 using 380 keV implantation energy. Post-implantation annealing was carried out at the temperature range of 550°C to 1350°C in argon (Ar) ambient. The resulting SiC films were characterized by Auger electron spectroscopy (AES), Fourier transform infrared spectroscopy (FTIR), nuclear reaction analysis (NRA), x-ray diffraction (XRD), and high-resolution transmission electron microscope (HRTEM). Clear PL behavior was seen from the annealed a-SiC:Er samples, even at room temperature, with PL intensity reaching a maximum for samples annealed at 900°C. Further studies of thermal quenching of Er luminescence from a-SiC:Er samples annealed at 900°C indicated that as the sample temperature increased from 14K to room temperature, the luminescence intensity at 1540 nm dropped by a factor of 3.6. In addition, post-deposition annealing at temperatures above 1000°C was performed, leading to the formation of SiC nanocrystals within the amorphous SiC matrix. The effect of these SiC nanocrystals on Er luminescence was also investigated.

J5.30

Structural Analysis of the Carrot Defects in 4H-SiC Epilayers. Mourad Benamara[1], Marek Skowronski[1], Joseph Sumakeris[2] and Michael Paisley[2]; [1]Carnegie Mellon University, Pittsburgh, Pennsylvania; [2]Cree, Inc, Durham, North Carolina.

One of the frequent surface morphology defects in homo-epitaxial 4H-SiC layers, namely the carrot defect, has been analyzed by plan-view and cross-section transmission electron microscopy, atomic force microscopy, and KOH etching. The defect is a shallow ridge elongated along the [11-20] off-cut direction with a narrow trench in the middle. The carrot extends always the same distance indicating that its origin is at the layer/substrate interface. The trench has a different length always starting at the tip of the carrot. The entire length of the trench etches in KOH indicating that the carrot is due to the planar defect intersecting the layer surface along the trench. TEM analysis has shown that the defect consists of a {1-100} prismatic stacking fault. The fault folds many times into the basal plane for approximately 1 micron, then folds back into the prismatic plane. The displacement vector R of the fault was determined using conventional weak-beam dark-field microscopy. The (g, ng) experiments were carried out in order to extinguish the alpha fringes. The results indicate that the fault displacement vector R has a component along the c-direction. Possible formation mechanisms will presented and discussed.

J5.31

PVT Growth of 6H SiC Crystals and Defect Chararacterization. Govindhan Dhanaraj[1], Feng Liu[1], Michael Dudley[1], Hui Zhang[2] and Vish Prasad[3]; [1]Materials Science and Engineering, Stony Brook University, Stony Brook, New York; [2]Mechanical Engineering, Stony Brook University, Stony Brook, New York; [3]Mechanical Engineering, Florida International University, Miami, Florida.

The Silicon Carbide (SiC) is a potential semiconductor material to replace and out-perform the conventionally used silicon crystal in several electronic devices for high power and high frequency and high temperature applications because of its unique combination of properties such as high electric field break down strength, high electron velocity and high thermal conductivity. Due to the phase equilibrium in the Si/C system, SiC cannot be grown from melt methods. Theoretically predicted temperature and pressure for melting SiC are beyond the reach at the laboratory. The high temperature solution growth of bulk SiC using Si melt is limited because of stringent experimental conditions and the presence large of number of stacking faults and planar inclusion defects Physical vapor transport (PVT) growth, also known as seeded sublimation growth, has been the most successful method to date for growing large SiC single crystals (1). In this method, SiC powder in a semi-sealed crucible is sublimed and recrystallized on a seed crystal maintained at a slightly lower temperature. The crystal growth process of SiC is complex and difficult to optimize due to the fact that the operating temperatures are extreme (2100-2500 deg C) and monitoring and controls are difficult (2,3). Since growth process occurs in almost air-tight graphite crucible and it is not feasible to observe the growing boule or determine experimentally the exact thermal conditions in the growth zone due to high operating temperatures and the opacity of the graphite crucible. The temperature field in the hot-zone has been predicted using numerical modeling. We have grown 6H SiC crystals using PVT system designed and fabricated in our laboratory. A new seed mounting technique has been developed for holding the seed on the crucible lid. Crystals up to 50 mm diameter have been grown at temperature range 2100-2200 deg C. The seed crystals and the grown bulk crystals have been characterized using Nomarski, SWBXT and Etching techniques to understand the formation of micropipes during the growth. The details on crystal growth of 6H SiC and defects characterization will be presented. References: 1. Carter, Jr., C.H., Tsvetkov, V.F., Glass, R.C., Henshall, D., Brady, M., Muller, St.G., Kordina, O., Irvine, K., Edmond, J.A., Kong, H.S., Singh, R., Allen, S.T. and Palmour, J.A., Progress in SiC: from Material Growth to Commericial Device Development, Mater. Sci. Engg., B61-62, 1-8 1999. 2. G. Dhanaraj, X.R. Huang M. Dudley, V. Prasad and R.H. M, Silicon Carbide Crystals: Part I : Crystal Growth and Characterization, chapter 6, p181-232, in Crystal Growth Technology, Eds K. Byrappa, T. Ohachi, Springer with William Andrew, NY 2003 3. Chen, Q-S., Prasad, V., Zhang, H. and Dudley, M., Silicon Carbide Crystals: Part II:Process Physics and Modeling,Chapter 7, p 233-269, in ibid

J5.32
Atomic Force Microscope Observations of Growth and Defects on As-Grown (111) 3C-SiC Mesa Surfaces.
Philip G. Neudeck[1], Andrew J. Trunek[2] and J. Anthony Powell[3]; [1]NASA Glenn Research Center, Cleveland, Ohio; [2]OAI, Cleveland, Ohio; [3]Sest, Inc., Cleveland, Ohio.

We have previously reported the step-free surface heteroepitaxy growth technique for obtaining high yields of 3C-SiC mesa heterofilms completely free of stacking fault defects [1,2]. However, only abbreviated atomic force microscope (AFM) data of as-grown 3C mesa film surfaces have been published to date [3]. This paper presents more extensive observations of as-grown (111) 3C-SiC mesa heterofilm surfaces by AFM. In nearly all cases, the as-grown (111) 3C-SiC surface consisted of single bilayer height (0.25 nm) steps. Macrosteps (i.e., step-bunching) were almost never observed. AFM also revealed some as-grown mesa surfaces in which sub-bilayer height line features with <111> orientation were superimposed across many single-bilayer height step patterns. Thermal oxidation of a selected 3C-SiC mesa confirmed the presence of stacking fault defects exactly corresponding to where line features were previously imaged by AFM in the as-grown film surface. Other small perturbations in the step structure of the film surface are attributed to the intersection of isolated threading edge or basal plane dislocations. AFM revealed that the morphology on the top (111) surface of 3C heterofilm mesas varied as a function of growth conditions, film thickness, and film defect content. AFM of 3C-SiC film surfaces grown at temperatures below 1500 C exhibit clear evidence of two-dimensional (2D) terrace nucleation. In some regions, the terrace nucleation appears quite random. In other regions, terrace nucleation is enhanced by the presence of threading edge dislocation defects producing triangular growth hillocks on the 3C-SiC growth surface [2,3]. At higher growth temperatures, 2D nucleation on the top (111) surface becomes suppressed contributing to previously reported large differences in growth rate between mesas with and without stacking fault defects [3]. Experimental data (including AFM) suggests that 3C-SiC film growth becomes governed by growth on evolving facets at the edges of mesa crystals. Because the edge facet surfaces have higher chemical bond density than the top (111) surface, the facet surfaces are hypothesized to support more rapid crystal growth. [1] P. Neudeck, et al., Mat. Sci. Forum 389-393 (2002) p. 311. [2] P. Neudeck et al., to appear in Silicon Carbide and Related Materials 2003. [3] A. Trunek et al., to appear in Silicon Carbide and Related Materials 2003.

J5.33
Abstract Withdrawn

J5.34
Fabrication of Desk-Top type ion implanter for SiC device application.
Satoshi Furukawa[1], Toshitake Nakata[2], Yuji Horino[3], Yoshinori Hosokawa[4] and Shigehiro Nishino[1]; [1]Department of Electronics and Information Science, Kyoto Institute of Technology, Kyoto, Kyoto, Japan; [2]SIC Semicon Corp., Osaka, Japan; [3]AIST, Osaka, Japan; [4]X-ray Precision Ltd., Kyoto, Japan.

Ion implantation is a key technology for SiC devices. Generally implantation is carried out using by large scale ion implanter, however, small scale implanter has a lot of merit in the field of SiC devices. We made desk-top type ion implanter which consists of PIG ion source, small acceleration tube, mass separation by Wine filter and chamber for sample stage. We already applied this machine to 4H-SiC devices. Carrier concentration of the epilayer of the 4H-SiC substrate was 2E15 cm-3. Edge termination of SBD was made using Ar ion with acceleration voltage (Va) of 10 KeV and high resistive amorphous layer was made around Schottky barrier metal. Dose of Ar was 1E16 cm-2.Amorphous state of the implanted region was confirmed by RHEED pattern. Implanted layer was also examined by IR reflection measurement. Without edge termination, break down voltage was 600 V, but after edge termination by Ar implantation, breakdown voltage increased to 1000 V . Diameter of the metal was 0.5 mm. To make a np junction , nitrogen ion was implanted with Va of 30 KeV to p-type substrate. Carrier concentration of the p-layer was 2E15 cm-3. After high temperature annealing, pn junction was formed. Typical diode characteristics were obtained. To make a pn junction, boron ion was made using BC solid and B ion was implanted into n-type epilayer. Characteristics of the diodes is discussed.

SESSION J6: Extended Defect Characterization I
Chair: M. Dudley
Thursday Morning, April 15, 2004
Room 2009 (Moscone West)

8:30 AM *J6.1
Microstructural Aspects and Mechanism of Degradation of 4H-SiC PiN Diodes under Forward Biasing.
Pirouz Pirouz, Materials Science and Engineering, Case Western Reserve University, Cleveland, Ohio.

Devices fabricated from the wide bandgap semiconductor SiC have many advantages over those made from conventional semiconductors. Thus, performance characteristics of some 4H-SiC devices can be two orders of magnitude better than equivalent devices made from silicon. On the other hand, new and unexpected problems have crept up with the operation of some SiC devices that need to be understood and solved before further progress can be made in this area. One of the most intriguing problems has been the degradation of bipolar PiN diodes that, because of conductivity modulation and lower on-resistance, have major advantages over unipolar Schottky barrier diodes at high blocking voltages. The electrical degradation of the diodes was noticed after prolonged reliability tests and refers to a drop in voltage under extended forward current operation. The degradation appears to be associated with the appearance of stacking faults in the entire base region of the diode. In this talk, we discuss the many puzzling aspects of stacking fault formation in such diodes. Electroluminescence as well as TEM has been used to investigate the degradation problem and, based on experimental results, the formation of partial dislocations within the device, their enhanced motion under electron-hole recombination and the possible sources of partial dislocations will be considered.

9:00 AM J6.2
Thermoplastic Deformation and Residual Stress Topography of 4H- and 6H-SiC Wafers.
Robert S Okojie[1], Ming Zhang[2] and Pirouz Pirouz[2]; [1]Sensors and Electronics Branch, NASA Glenn Research Center, Cleveland, Ohio; [2]Department of Mater. Sci. & Eng.,, CWRU, Cleveland, Ohio.

Optical reflectometry was used to measure stress relaxation via thermoplastic deformation in as received 4H- and 6H-SiC substrates. The stress topology was characterized using 3D mapping features, or contour maps, to locate differences in wafer bow or wafer warp across the surface. In all cases, during thermal excursion to 900 ^{o}C in vacuum, the radii of curvature of the substrates increased (i.e., the wafers became flatter) with increasing temperature starting from 350 ^{o}C. This change in curvature corresponded to a relaxation of the residual stress in the substrates. Upon cooling down to room temperature, the radii of curvature of all the substrates retained their high-temperature (900 ^{o}C) values, thus exhibiting thermoplastic inelastic behavior. Further cyclic excursion to 900 ^{o}C did not yield any significant changes in the curvature, thus indicating that the changes from the first anneal were irreversible. The change in internal stress following thermoplastic deformation at 900 ^{o}C in vacuum was estimated to be greater than 0.7 GPa with an activation energy of deformation of 3.14±0.8 eV. Subsequent measurements of residual stresses were performed on n-type 4H-SiC epilayers with different nitrogen-doping level that were grown homoepitaxially on the n- or p-type 4H-SiC substrates relaxed by thermal anneal in nitrogen at 1150 ^{o}C prior to growth. The 3D stress measurements on the as grown epilayer on the substrate indicated the existence of compressive stresses in the epilayers. The samples were further annealed at 1150 ^{o}C in nitrogen for thirty minutes and their microstructure was investigated by transmission electron microscopy (TEM), specifically to look for the possible generation of stacking faults (SFs). TEM investigations revealed 3C-SiC bands in annealed 4H-SiC samples, which had an n-type epilayer doping as low as 5 x 10^{17} cm^{-3}. This epilayer doping level is approximately two orders of magnitude below the reported threshold value (3 x 10^{19} cm^{-3}) previously suggested for the onset of the generation of SFs in annealed epilayers. This work provides evidence for the existence of significant compressive stresses in 4H-SiC epilayers. Thus, it is possible that stacking faults and 3C bands observed in many recent experiments are due to the motion of pre-existing partial dislocations.

9:15 AM J6.3
The Driving Force of Stacking Fault Formation in Silicon Carbide p-i-n Diodes.
Seoyong Ha[1], Marek Skowronski[1], Joseph Sumakeris[2] and Michael Paisley[2]; [1]Carnegie Mellon University, Pittsburgh, Pennsylvania; [2]Cree, Inc, Durham, North Carolina.

The driving force of stacking fault formation in 4H silicon carbide p-i-n diodes has been investigated using optical emission microscopy and transmission electron microscopy. The forward voltage drop has been observed to increase with time due to expansion of single-layer Shockley-type stacking faults in the blocking layer. It has been suggested that the phenomenon is driven by a mechanical stress in the epilayer/substrate structure. The results presented below indicate that stress cannot be the driving force. The p-i-n diodes examined in this study were fabricated on 3 inch diameter, 4H-SiC, n-type substrates (n=8?1018 cm-3). The substrates were off-cut by 8 degrees from the [0001] toward the [11-20] direction and the diodes were processed on the silicon-face. The low-doped (n 1015 cm-3) blocking layer (30 ?m) and the p-type anode were deposited by chemical vapor

deposition. Standard metal contacts were formed on the diode surface and substrate backside. Diode mesas were defined by reactive ion etching. The partial dislocation motion was recorded by optical emission microscopy during the diode operation. The degraded diodes were analyzed by transmission electron microscopy in order to determine the Burgers vector and the line direction of the partial dislocations. From these dislocation characteristics one can deduce the type of the shear stress driving the fault expansion. The stress direction was determined for over 20 different partial dislocations. The partial dislocations moved as if there were positive as well as negative shear stresses in the blocking layer even in the case of single diode. We also have observed several examples of two partials with the same sign of Burgers vector moving in opposite directions within several microns of each other. This could not be explained by stress either uniform or local in nature. These observations indicate that the stacking fault expansion in diodes under forward bias is inconsistent with a stress acting as the driving force. This argument leaves the thermodynamic free energy difference between the perfect and a faulted structure as the only plausible driving force. In other words, 4H-SiC crystals are metastable at room temperature and would convert spontaneously into faulted structure. For such process to occur, however, the nucleation sites and the activation energy in the form of electron-hole recombination are needed. At this point, the best approach to elimination of the junction degradation appears to be control of pre-existing defects serving as nucleation sites.

9:30 AM *J6.4
Mechanisms of Stacking Fault Growth in SiC PiN Diodes.
R. E. Stahlbush, Naval Research Laboratory, Washington, District of Columbia.

Power devices fabricated in SiC offer many advantages over their present-day Si counterparts. However, SiC technology is not as mature and there are numerous material and processing problems that remain to be resolved. One of the most significant materials problems is the formation of stacking faults (SFs) during forward-biased operation of bipolar devices. The stacking faults degrade the minority carrier lifetime and increase the forward voltage drop, V_f. Furthermore, the formation of stacking faults is erratic. For example, PiN diodes from the same wafer can have V_f drift that varies more than order of magnitude. While some of the mechanisms of the degradation are understood, others remain unclear. It is agreed that electron-hole recombination is necessary to provide the local energy for moving the partial dislocations that bound the SFs. It is also clear that there must be nucleation sites where SF growth starts. The recombination overcomes the kinematic constraint making SF growth possible. The thermodynamic driving forces are less clear; three have been proposed. The first is lowering of the electronic energy as electrons fall into the quantum wells formed by the SFs. The second is relief of mechanical stress, and the last is the preference near room temperature for the 3C polytype over the 4H polytype. Studying the SF growth dynamics by light emission imaging provides insight into these open questions. Nucleation sites are distributed throughout the diode drift region and many of them originate from faulting of basal plane dislocations present after the epitaxial growth. The SF growth patterns can also distinguish among the possible driving forces. The electronic energy lowering can be neglected while nonuniform stress appears to play a significant role and the 3C polytype preference also may be contributing to the driving force.

SESSION J7: Extended Defect Characterization II
Thursday Morning, April 15, 2004
Room 2009 (Moscone West)

10:30 AM *J7.1
Extended Defects in SiC Substrates and Epilayers.
Marek Skowronski, Carnegie Mellon University, Pittsburgh, Pennsylvania.

The driving force behind the development of silicon carbide technology is the potential for major energy savings due to use of high voltage switching devices. The first of such devices, namely Schottky diode rated for up to 1.2 kV, is already available commercially. However, the development of high voltage bipolar devices still faces numerous challenges. From the materials point of view, this is possibly the most demanding application requiring utmost in doping control, low extended defect densities, and long carrier diffusion lengths. This presentation will focus on extended defects in SiC substrates and epitaxial layers and will describe their morphology and allude to their origin. The sources of three types of dislocations silicon carbide wafers will be discussed. The elementary screw dislocations are either inherited from the seed crystal or nucleated at the initial stages of growth on basal plane surfaces. They serve as step sources on the surfaces of boules and determine the stacking sequence. Threading edge dislocations are mostly grown-in but some evidence suggests possibility of prismatic slip. These dislocations appear to be mobile at growth temperatures and undergo partial polygonization forming low angle grain boundaries. The final type, basal plane dislocations, is introduced by plastic deformation of boules during growth. They frequently form characteristic arrays with morphology consistent with that of basal plane slip bands. SiC homoepitaxy has a major effect of dislocation distribution. The oblique off cut angle used for substrates induces significant image force acting on basal plane dislocations and results in most of them converting into threading type. In addition to dislocations propagating from the substrate, additional threading dislocations are nucleated during growth. An example of such dislocations, called pair array, will be presented. Finally, the defect characteristic of silicon carbide, the basal plane stacking fault frequently found in as-grown epilayers, will be discussed.

11:00 AM J7.2
First Direct Measurements of Dynamic Constants of Dislocations Introduced in (11-20) 4H-SiC.
Idrissi Hosni[1], Maryse Lancin[1], Joel Douin[2], Gabrielle Regular[1] and Bernard Pichaud[1]; [1]TECSEN, University III, Marseille, France; [2]LEM, CNRS-ONERA, Chatillon cedex-20, France.

Despite the essential role of dislocations and the increasing importance of silicon carbide in the high-power electronic industry, no direct experimental values on either perfect or partial dislocations velocity in SiC have been published so far, whatever their core. Nevertheless, transmission electron microscopy (TEM) observations show that partial dislocations with silicon core have a higher mobility than those with a carbon core. This is actually in contradiction with ab initio calculations which demonstrate that partials containing core Si atoms are strongly reconstructed whereas partials containing core C atoms are more weakly reconstructed indicating that the latter partials are more mobile. The purpose of this work is to derive the stress exponent m and the activation energy Q of dislocation velocity [1] from introducing and developing fresh dislocations by cantilever bending in as-received high quality (11-20) 4H-SiC. V=A $\mathrm{sr\hat{m}}$ exp(-Q/kT) [1] A is a constant and sr is the resolved shear stress in the gliding basal plane. The wafer orientation is selected because of its most suitable geometry for deformation (high Schmidt factor). The stress along the sample length is measured by determining the local radius of curvature. The plastic deformations are carried out at temperatures ranging from 823K to 1323K under neutral atmosphere. The dislocation propagation distance is measured by X-Ray transmission Topography (XRTT) or chemical etching. In addition, TEM studies are carried out to characterize the Burger's vector and the dislocation cores. XRTT observations and chemical etching reveal straight lines parallel to the basal plane with asymmetric location as compared to the position of the nucleation centres (edges or scratches of the samples). These lines correspond to faulted half loops consisting of i) one 90 Shockley partial dislocation with a silicon core, parallel to the surface and located close to the neutral plane at half the thickness of the sample and ii) two 30 Shockley partial dislocations with a silicon core, one of them emerging at the sample surface and the other linked to the 30 Shockley partial dislocation with a carbon core belonging to the dislocation source. The observed asymmetry derives from the low mobility, if any, of the 30 Shockley partial dislocation with a carbon core. We will give the first set of curves of dislocation velocities as a function of temperature and as a function of the resolved shear stress in 4H-SiC for a temperature range below 1373K.

11:15 AM J7.3
Characterization of SiC epilayers using high-resolution X-ray diffraction and synchtron topography imaging.
Xianrong Huang[1], Michael Dudley[1], Wondong Cho[1] and Robert S Okojie[2]; [1]Dept. of Materials Sci. & Eng., Stony Brook University, Stony Brook, New York; [2]NASA Glenn Research Center, Cleveland, Ohio.

A series of advanced X-ray diffraction and imaging techniques, including double-axis HRXRD, triple-axis diffraction, reciprocal space mapping (RSM), and synchrotron white-beam X-ray topography (SWBXT) are used to investigate the extremely small lattice mismatch and misorientation in n-type 4H SiC epilayers grown homoepitaxially on p-type 4H SiC. It is found that the basal planes of the doped epilayers are usually tilted against those of the substrate (around 50 seconds). Using triple-axis RSM, we successfully separate the contribution of lattice tilts from that of lattice constant variation in the diffraction pattern. The dependence of the lattice constant and crystalline quality of the epilayers on different nitrogen doping levels and annealing treatments is thus accurately obtained. The doping-induced lattice constant variation is attributed to the substitutional nitrogen incorporated preferentially in the host carbon sites. Annealing can also change the lattice parameters due to the generation of stacking faults in 4H SiC epilayer.

11:30 AM J7.4
Optical Studies of Porous GaN/SiC and GaN/porous SiC

structures. Karim Mynbaev[1], Sergey Ostapenko[2], Igor Tarasov[2], Gregory Onushkin[1] and Marina Mynbaeva[1]; [1]Ioffe Institute, St.-Petersburg, Russian Federation; [2]Nanomaterials and Nanomanufacturing Research Center, University of South Florida, Tampa, Florida.

Results of optical studies of porous GaN/SiC structures and single- and multi-layer GaN-based structures grown on porous SiC (PSC) substrates are presented. In porous GaN/SiC structures, the most remarkable feature is strong photoresponse (PS) in visible part of the spectrum. The PS demonstrates peculiarities typical of persistent photoconductivity effect in GaN, including non-exponential decay with characteristic times of thousands of seconds. Detailed PS, photoluminescence and electron microscopy studies allowed us to relate the PS to charged states localized at GaN/SiC interface in porous GaN/SiC structures. On single GaN epitaxial layers grown on PSC and SiC substrates, a PL study was performed. It appeared that layers grown on PSC substrates demonstrated increased PL intensity as related to those grown on non-porous SiC substrates. All PL bands were increased by approximately the same amount, which indicates that a mechanism of the increase is a reduction in density of non-radiative recombination centers in the layers grown on PSC. As transmission electron microscopy revealed reduction in dislocation density in GaN layers grown on PSC substrates, such centers of non-radiative recombination can be related to dislocations. Finally, results of electroluminescence (EL) measurements on a DH GaN/AlGaN LED structure grown on PSC will be presented. Luminescence properties of GaN layers and GaN-based device structures will be used to discuss the advantages of epitaxial growth on porous substrates.

SESSION J8: MOS Structures
Thursday Afternoon, April 15, 2004
Room 2009 (Moscone West)

1:30 PM *J8.1
Comparison of electrical properties for MOS structures fabricated on the 4H-SiC (0001),(11-20),(000-1) faces.
Kenji Fukuda, Power Electronics Research Center, National Institute of Advanced Industrial Science and Technology, Tsukuba, Ibaraki, Japan.

SiC MOSFET is expected to be available for next-generation switching devices. However, at present, the on resistance (Ron) of the SiC power MOSFET is much higher than the theoretical value of SiC, the performance of SiC is not sufficiently demonstrated. This is attributed to several defects at the SiO2/SiC interface compared to the SiO2/Si interface, which leads to difficulty with respect to the current flow. A channel mobility 100-200 cm2/Vs is required for the realization of the SiC power MOSFET, with the limitation of Ron for 4H-SiC. However, the inversion channel mobility is low and higher channel mobility is necessary. Gate oxide reliability is also very severe problem for the realization of SiC power MOSFET. The oxidation rate strongly depends on the surface orientation. It is considered that optimum gate oxidation condition changes with the surface orientation. We are investigating techniques by which to systematically improve the interface trap density (Dit), the inversion channel mobility, gate oxide reliability such as TZDB,TDDB, hot-carrier degradation and the Ron of lateral resurf MOSFET for the (0001) face, the (11-20) face and the (000-1) face. We have reported that the inversion channel mobility of SiC MOSFET fabricated on the (0001) face was increased using pyrogenic re-oxidation[1], that the Dit and the inversion channel mobility of MOS structures fabricated on the (11-20) face and (000-1) face was much improved using pyrogenic gate oxidation followed by hydrogen post oxidation annealing(POA),which resulting in the peak value of inversion channel mobility of 160cm2/Vs and 127cm2/Vs, respectively[2]-[4]. Hydrogen POA also suppresses hot-carrier degradation[5]. Further details regarding these techniques containing the Ron of lateral resurf MOSFET and gate oxide reliability will be reported at MRS spring meeting. [1] R.Kosugi et al.:IEEE Electron Device Lett.23(2002)136. [2] J.Senzaki et al.: Mater. Sci.Forum, 433(2003)613. [3] K. Fukuda et al.:Mater. Sci.Forum, 433(2003)567. [4] K. Fukuda et al.: to be published in Mater. Sci.Forum. [5]W.J.Cho et al.:Appl.Phys.Lett.77(2000)1215.

2:00 PM J8.2
MOS Interface Properties and MOSFET Performance on 4H-SiC{0001} and Non-Basal Faces Processed by N2O Oxidation. Tsunenobu Kimoto, Yohsuke Kanzaki, Hajime Kosugi and Hiroyuki Matsunami; Department of Electronic Science and Engineering, Kyoto University, Kyoto, Japan.

Although silicon carbide (SiC) MOSFETs are recognized as ideal power switches, SiC MOSFETs have suffered from low effective channel mobility. In recent years, N2O oxidation has been proposed to improve SiO2/4H-SiC(0001) interface properties and thereby to increase effective channel mobility of MOSFETs. Recent investigations have revealed that 4H-SiC(000-1) and non-basal faces such as (11-20) and (03-38) possess much potential to further improve the quality of MOS structure. In this study, characterization and MOSFET fabrication have been investigated on 4H-SiC(000-1), (11-20), and (03-38) by using N2O oxidation. The oxidation has been performed in N2-diluted N2O (dry) at 1300oC. The typical oxide thickness was 50-70 nm. The crystal face dependence of oxidation rate was also studied. In MOSFET fabrication, planar inversion-type MOSFETs were processed on p-type epilayers doped to 1E16 - 3E17 cm-3 to investigate the influences of p-body doping on the MOSFET performance. The source/drain regions were formed by high-dose phosphorus ion implantation followed by annealing at 1600oC. The interface state density (Dit) was estimated by low- and high-frequency C-V curves of n-type MOS capacitors. Although the Dit for the 4H-SiC(0001) MOS structure showed a rapid increase near the conduction band edge, the MOS structures on the other faces exhibited a rather flat Dit distribution: The Dit value at Ec - 0.2 eV is well below 1E12 cm-2eV-1. The effective channel mobility of the (0001) MOSFET remained 18-24 cm2/Vs. However, (000-1) and (11-20) MOSFETs showed much higher mobilities of 50-62 cm2/Vs and 74-83 cm2/Vs, respectively on lightly-doped p-type epilayers. It should be noted that the (11-20) MOSFET showed a reasonably high mobility of 56 cm2/Vs even on epilayers with an acceptor concentration of 2E17 cm-3, which is more realistic for power MOSFET fabrication. On the other hand, the mobility of (0001) MOSFET significantly decreased to 12 cm2/Vs by increasing the p-body doping. The crystal face/p-body doping dependencies of channel mobility is discussed. Although rapid progress has been made on 4H-SiC(0001) MOSFETs, power MOSFETs on (000-1) or trench MOSFETs with the (11-20) sidewalls are promising in the future.

2:15 PM J8.3
Interface Trap Defects Observed in 6H SiC Metal Oxide Semiconductor Field Effect Transistors via Spin Dependent Recombination. David J. Meyer[1], Morgen S. Dautrich[1], Patrick Lenahan[1] and Aivars Lelis[2]; [1]Engineering Science and Mechanics, The Pennsylvania State University, University Park, Pennsylvania; [2]U.S. Army Research Laboratory, Adelphi, Maryland.

We utilize a particularly sensitive form of electron spin resonance (ESR) called spin dependent recombination (SDR) to observe deep level trap defects at or very near the interface of 6H silicon carbide and the SiO_2 gate dielectric in SiC MOSFETs. We find that the SDR response is strongly correlated to SiC/SiO_2 interface recombination currents and also find that the magnitude of the SDR response is correlated with processing induced changes in interface trap density, an extremely strong indication that we are observing the dominating interface/near interface trapping defects. The SDR response is extremely large, as large as one part in 350. To the best of our knowledge, this is the largest SDR response ever reported in a semiconductor device at room temperature. To the best of our knowledge, this is the first observation of SDR in a SiC MOSFET and arguably the first direct observation via magnetic resonance of a defect certain to be involved in SiC/SiO_2 interface traps. Rotation about two axes demonstrates that the g-tensor is isotropic and g = 2.0027 for all orientations. In addition to observation of the strong center line, we also observe weaker superhyperfine and hyperfine side peaks. The superhyperfine peaks are almost certainly associated with nuclear magnetic moments of ^{29}Si; the hyperfine peaks are associated with ^{13}C. These results quite strongly suggest that the defect under study involves a silicon vacancy site. We are presently adding conventional ESR measurements as a function of gate bias to provide a fuller description of the electronic properties of these defects.

2:30 PM J8.4
Reliability of Nitrided Oxides in N- and P-type 4H-SiC MOS Structures. Sumi Krishnaswami, Mrinal Das, Anant Agarwal and John Palmour; Cree Inc, Durham, North Carolina.

One of the attractive features of MOS-based silicon carbide devices is their potential use for high temperature and high power applications. Earlier problems with high interface trap density (D_{IT}) and low mobility on (0001) 4H-SiC MOS structures have been steadily improved via nitridation annealing with D_{IT} reported as low as 1E11 $cm^{-2}eV^{-1}$ near E_C and mobility approaching 100 cm^2/V-s [1,2]. However, the use of such devices will ultimately be limited by oxide integrity and reliability. This paper presents high temperature time dependent dielectric breakdown (TDDB) results from both n-type and p-type MOS capacitors with thermal oxides grown under different nitridation conditions. Reliability measurements on n-type MOS capacitors biased into strong accumulation enable us to investigate the oxide integrity under electron injection from the semiconductor where the barrier is relatively low due to the wide 4H-SiC bandgap. This emulates the on-state mode of operation thereby predicting the maximum allowable gate voltage (i.e., the minimum on-resistance). Reliability measurements on p-type MOS capacitors, on the other

hand, predicts the maximum allowable field in the semiconductor (i.e., the maximum blocking voltage) by simulating the oxide stress during the MOSFET blocking mode of operation which is governed by hole injection. TDDB measurements of NMOS capacitor (1200 °C dry oxide with 1300 °C N2O anneal) were performed at 175 °C and 300 °C under high positive bias stress. The devices are biased into strong accumulation mode such that the field in the oxide is high enough to collect breakdown data in a reasonable period of time. We observe that at 175 °C, a 100-year MTTF is obtained if the field in the oxide is kept below 6.5 MV/cm. The TDDB measurement has also been performed at 300 °C where lifetime has been reduced by a few orders of magnitude. Recent reliability results on similarly oxidized MOSFETs have shown failures along the same trend as the n-type capacitors, indicating that MOSFETs and MOS capacitors can have similar reliability despite inherent processing and structural differences. PMOS capacitors fabricated with the aforementioned dry + N2O process as well as capacitors fabricated using the low D_{IT} nitridation techniques are currently being evaluated. [1] M.K. Das, "Recent Advances in (0001) 4H-SiC MOS Devices," International Conference on Silicon Carbide and Related Materials, Lyon, France, October, 2003. [2] G. Gudjornsson, H.O. Olafsson, E. O. Sveinbjornsson, "Enhancement of inversion channel mobility in 4H-SiC MOSFETs using a gate oxide grown in nitrous oxide (N2O)," International Conference on Silicon Carbide and Related Materials, Lyon, France, October, 2003.

2:45 PM J8.5
Extreme Service Packaging for Silicon Carbide Electronic Devices. Grant Norton[1], Maxime Guinel[1], Diego Rodriguez-Marek[1], David Bahr[1] and Robert Davis[2]; [1]School of Mechanical and Materials Engineering, Washington State University, Pullman, Washington; [2]Caldus Semiconductor, Inc, Richland, Washington.

Electronic devices based on single crystal silicon carbide represent a good choice for fast, high frequency and high power devices for use as sensors, switches, pressure devices and control electronics in high temperature applications such as inside fuel cells. The challenge is to develop a package that is resistant to thermal degradation in harsh environments. The package must protect the die and allow it to maintain functionality for durations of at least 1000 h. Elevated temperatures place severe loads on both the device and package. The thermal cycle is extreme and this all but rules out only a handful of materials and materials systems. Polycrystalline silicon carbide is the material that we have chosen to study as a suitable package and materials suitability/compatibility has been considered on several levels. The package must be able to withstand prolonged exposure to harsh environments. We have demonstrated that quenching polycrystalline SiC can reduce fracture toughness and we have used indentation methods to determine the effect of thermal cycling on the mechanical properties of SiC. Sealing the package would be accomplished using a glass. The seal must be mechanically strong and hermetic. The maximum processing temperature for package joining using SiC electronics is 1088 deg.C and the package should operate up to 1000 deg.C. These requirements together with that of thermodynamic stability place severe restrictions on the glass. We will describe our results in selecting suitable glasses for this application. Electrical connections between the device and package are required to be ohmic and long lasting. The interconnect lead wire system must be stable at high temperatures and resistant to thermal cycling. The bonding system that we will describe uses diffusion and transient liquid phase bonding. A copper interlayer is used to form a bond between the top chip level metal tungsten pads and the nickel wire lead. This method has produced some very promising results in recent long-term aging studies.

SESSION J9: Growth and Characterization
Thursday Afternoon, April 15, 2004
Room 2009 (Moscone West)

3:30 PM *J9.1
Device Critical Defects in SiC. Peder Bergman, Christer Hallin, Liutauras Storasta, Bjorn Magnusson and Erik Janzen; Department of Physics and Measurement Technology, Linkuping University, 58183 Linkoping, Sweden.

SiC devices, such as schottky barrier diodes and MESFET, are today available for different applications. Further development also in other applications requires improved material quality. Both in order to make the devices functionable, but also to improve yield and general performance. Critical defects ate today structural defects such as micropipes, stacking faults and dislocations. But also the role and influence of point defects, both impurities and intrinsic defects, remains to be understood. In this presentation we will review known properties and influence of these defects. In particularily the properties of dislocations, the properties and influence on point defects on for example carrier lifetime, and the role of intrinsic defects both as recombination centers and as responsible for semi insulating proerties of high purity material.

4:00 PM J9.2
A correlation between implantation induced defects and dopant profiles in P implanted (0001) and (11-20) oriented 4H-SiC. Jennifer Wong-Leung[1], Margareta K. Linnarsson[2] and Bengt Gunnar Svensson[3]; [1]Dept. of Electronic Materials Engineering, Australian National University, Canberra, Australian Capital Territory, Australia; [2]Solid State Electronics, Department of Microelectronics and Information Technology, Royal Institute of Technology, Kista-Stockholm, Sweden; [3]Department of Physics/Physical Electronics, University of Oslo, Oslo, Norway.

In this study, both (11-20) and (0001) n-type 4H-SiC substrates were implanted with 400 keV P and then annealed at different temperatures namely 1300C and 1700C. The various samples, both as-implanted and annealed, were studied by secondary ion mass spectrometry (SIMS), Rutherford backscattering and spectrometry (RBS-C) and transmission electron microscopy (TEM) to understand the damage evolution and defect structures resulting from different crystal orientations and different implantation damage. TEM analysis of the (0001) wafer shows the formation of basal plane dislocation loops, voids and some precipitates close to the loops. The (11-20) wafer showed some larger voids faceted on the {1-100} planes, some loops with basal plane as habit plane and other loops with the (11-20) habit plane. Some elongated loops on the (11-20) plane were also observed to be pinned by precipitates. SIMS profiles show in some cases distinct differences between the two crystal directions. A comparison between the TEM and the SIMS results suggests a relation between the accumulation of P at certain and precipitation close to dislocation loops.

4:15 PM J9.3
Comprehensive Study of Impact Ionization Coefficients of 4H-SiC. Tetsuo Hatakeyama[1], Takatoshi Watanabe[1], Kazunori Kojima[2], Nobuyuki Sano[3], Takashi Shinohe[1] and Kazuo Arai[2]; [1]Corporate R&D Center, Toshiba corporation, Kawasaki, Japan; [2]Power Electronics Research Center, National Institute of Advanced Industrial Science and Technology, Tsukuba, Japan; [3]Institute of Applied Physics, University of Tsukuba, Tsukuba, Japan.

Impact ionization coefficients are important physical properties for power devices, because avalanche breakdown caused by impact ionization limits the voltage blocking capabilities of a power device. However, our knowledge of the impact ionization coefficient of 4H-SiC is limited, and the reported coefficients differ one another. Further, anisotropy of breakdown field of 4H-SiC was reported and it was shown that there is a significant reduction of the breakdown field when the electric field is applied perpendicular to the c-direction. In order to understand avalanche breakdown behavior of a 4H-SiC power device, reliable parameter sets for the impact ionization coefficients are needed. In this talk, we present the parameter sets of impact ionization coefficients of 4H-SiC for <0001> and <11-20> directions that reproduce avalanche breakdown behavior of p+n diodes on (0001) and (11-20) epitaxial 4H-SiC wafers. The obtained impact ionization coefficients show large anisotropy; the breakdown voltage of a p+n diode on (11-20) wafer is 60% of that on (0001) wafer. We also discuss the origin of anisotropy of impact ionization coefficient of 4H-SiC based on the microscopic description of the impact ionization and the transport physics under high electric field; impact ionization coefficients can be obtained by integrating the product of impact ionization scattering rate, the distribution function and density of state. Impact ionization rate and density of state are independent of electric field. Distribution function varies according to a carrier temperature, and carrier temperature is proportional to saturation velocity and electric field. Saturation velocity varies according to the direction of the electric field, in general. Thus, the anisotropy of the impact ionization coefficients is attributable to the anisotropy of saturation velocity originated from the electronic structure of 4H-SiC. The experimental results of the anisotropic saturation velocity and temperature coefficients of impact ionization coefficients will be presented at the meeting.

4:30 PM *J9.4
Growth and Metrology of Silicon Oxides on Silicon Carbide. Andrew M Hoff, Nanomaterials and Nanomanufacturing Research Center, University of South Florida, Tampa, Florida.

Thermal oxidation of SiC by the afterglow method has opened new pathways of opportunity to address both thin film growth and defects that hinder electronic device development with this important semiconductor material. Oxide growth, with rates up to 700Å per hour, on SiC has been demonstrated using this technique over a temperature range from 600 °C to 1100 °C at 1 Torr total pressure. Electrical and physical properties of oxide films grown by conventional means or by the afterglow method were obtained with a novel,

non-contact charge-voltage (Q-V) metrology approach. This instrument employs a combination of incremental contact potential difference values obtained in response to applied corona charge generated from air. The slope of the Q-V characteristic within a bias range corresponding to accumulation of the semiconductor provides an effective dielectric permittivity value for the grown film. Effective permittivity values for afterglow oxides grown on SiC approach that of SiO_2 grown on silicon substrates whereas the values for oxides grown on SiC in an atmospheric steam oxidation process are always depressed relative to SiO_2 on silicon, indicating that the latter process always produces low-k oxides. A mechanistic discussion regarding these observed differences between the two oxidation methods is presented along with suggestions for an integrated process and metrology approach to reduce defects in oxide films on SiC.