SYMPOSIUM K

Advances in Chemical Mechanical Polishing

April 13 - 15, 2004

Chairs

Duane Boning
Dept of Electrical Engr & Computer Sci
Massachusetts Institute of Technology
60 Vassar St.
Cambridge, MA 02139
617-253-0931

Johann W. Bartha
Dept of Electrical Engr & Information Tech
Dresden University of Technology
Noethnitzer Str. 64
Mierdel-Bau, Dresden, D-01187 Germany
49-351-463-35292

Gregg Shinn
Texas Instruments
MS 3736
P.O. Box 650311
Dallas, TX 75265
972-995-9708

Ingrid Voss
IMEC
Kapeldreef 75, B-3001 Belgium
32-16-28-1891

Ara Philipossian
Dept of Chemical & Environmental Engr
University of Arizona
Room 201C
P.O. Box 210011
Tucson, AZ 85721-0011
520-621-6101

Proceedings to be published in both book form and online
(see *ONLINE PUBLICATIONS* at www.mrs.org)
as volume 816
of the Materials Research Society
Symposium Proceedings Series.

* Invited paper

SESSION K1: Copper CMP
Chair: Ingrid Vos
Tuesday Morning, April 13, 2004
Room 2007 (Moscone West)

8:30 AM *K1.1
Challenges and Rewards of Low-abrasive Copper CMP: Evaluation and Integration for Single-Damascene Cu/Low-k Interconnects for the 90nm Node. Christopher Borst, Stan Smith and Mona Eissa; Texas Instruments, Inc., Dallas, Texas.

Low-abrasive slurries for copper (Cu) chemical-mechanical planarization (CMP) have been developed to perform with removal rate and removal uniformity comparable to conventional slurries. They can improve post-CMP defectivity and allow operation at lower polish pressures that are more compatible with the low-dielectric constant (low-k) materials required for current and future high-performance interconnect schemes. Integration of these slurries into a yielding product with 9-level Cu/low-k metallization requires fundamental learning and process characterization. This paper discusses the global challenges encountered during development, integration, and qualification of a low-abrasive Cu CMP process for Texas Instruments Incorporated's 90 nm technology node with 130nm minimum dimension copper/organosilicate interconnect. As abrasive content is reduced, the slurry chemistry must play a larger role in CMP removal. More aggressive reactive chemistry requires a more effective inhibitive chemistry to keep Cu static etch rate low. As a result, Wafer-scale process and consumable interactions, die-scale planarization efficiency, and feature-scale removal rates each become more sensitive to process changes. Pressure and temperature have larger effects on removal rate/profile than conventional slurries, and complete clearing of Cu puddled over underlying topography becomes more difficult. Successful integration of these slurries, however, can achieve excellent results in dishing and erosion topography, Cu thickness uniformity, and Cu loss in small features such as vias and landing pads. Low-abrasive solutions are also more stable and easy to handle in slurry distribution vessels and lines, have lower scratch and residue defectivity, and have greatly extended margin for overpolish. As low-abrasive Cu slurry options continue to evolve to become manufacturable solutions, their benefits far outweigh the costs and challenges encountered in their successful integration.

9:00 AM K1.2
Investigation of the influence of different copper slurry systems on post CMP topography performance.
Goetz Springer, Peter Thieme and Pierre Klose; Memory Development Center, Infineon Technologies, Dresden, Germany.

Since the early days of copper CMP much research and development effort was put into formulation of new copper and barrier CMP slurries. Two major motivations for this effort are the improvement of process performance for currently used integration schemes and the preparation for new integration schemes using low-k and ultra low-k dielectric materials. In this paper the influence of different copper slurries on topography before and after removal of the barrier film is investigated. For the tested slurries blanket wafer polish rates for copper, tantalum and silicon dioxide will be presented. Measured blanket wafer selectivities had a range of about a factor of ten. The topography performance was investigated using a standard metal CMP test structure. For each copper slurry, wafers with different copper and barrier CMP overpolish margins were processed. In all cases the same barrier CMP consumable set was applied. This allowed the direct comparison of the influence of different copper CMP slurries on copper CMP topography and post barrier CMP topography as well as electrical parameters. It was found that the different blanket wafer selectivities affect directly the erosion performance of array features after copper CMP. It was also recognized that with advanced copper slurries available on the market the dishing can be reduced drastically. As a result of the post copper CMP topography investigations, a discussion of advantages and disadvantages of non-selective and selective barrier polish processes will be presented. To complete this discussion of potential topography correction during barrier CMP, an investigation of an observed pronounced dielectric erosion close to large metal features or within high metal density arrays with medium or high selective barrier CMP processes will be presented.

9:15 AM K1.3
Copper CMP Formulation for 65 nm Device Planarization.
Gregory T Stauf, Karl Boggs, Peter Wrschka, Jeffrey F Roeder, Craig Ragaglia, Michael Darsillo, Mackenzie King, Jun Liu and Thomas H Baum; ATMI, Danbury, Connecticut.

To achieve 65 nm technology node requirements, CMP processes must provide improved control of selectivity, topography, wire cross section, and process robustness. Slurries and processes must also be compatible with fragile low k materials by providing low erosion and shear forces. We will present data on a unique Step 1 bulk Cu removal slurry with high selectivity, removal rates over 8000 Å/min, and extremely low liner removal/erosion in high (90%) density structures. This is achieved through a combination of surface modified abrasives and alternative inhibitors which provide superior performance and reduced electrochemical activity compared to benzotriazole, a commonly used inhibitor. The Step 1 slurry has allowed use of polish down forces as high as 5 psi on patterned CVD deposited C-doped oxide low k materials without damage. This is combined with a Step 2 liner removal slurry that can be chemically tuned to adjust relative selectivities of Ta:oxide:Cu from the nominal ratio of 2:2:1, allowing its use with a variety of integration schemes. Results of CMP planarization experiments on 200 mm blanket and patterned test wafers will be described, including electrical data.

9:30 AM K1.4
Effect of Hydrogen Peroxide on Oxidation of Copper in CMP slurries Containing Glycine and Cu Ions. Tianbao Du, Arun Vijayakumar and Vimal Desai; Advanced Materials Processing and Analysis Center, University of Central Florida, Orlando, Florida.

This study compares the oxidative dissolution, passivation, and polishing behavior of copper chemical mechanical polishing in the presence of hydrogen peroxide, glycine and copper sulfate. High purity discs were used to study the dissolution and oxidation kinetics under static and dynamic conditions at pH 4 with varying H2O2 concentrations. Changes in surface chemistry of the statically etched copper-disc were investigated using X-ray photoelectron spectroscopy (XPS). In the presence of only H2O2, the copper removal rate reached a maximum at 1% H2O2 concentration, and decreased with a further increase in H2O2 concentration. The etched surface morphology indicates that the removal of copper is primarily the result of electrochemical dissolution of copper at low H2O2 concentrations. However, at increased H2O2 concentration, the copper oxidation rate increases, resulting in a change in the copper removal mechanism to mechanical abrasion of oxidized surface. With further addition of glycine and copper sulfate to the slurry, the copper removal rates increased significantly and the maximum removal rate showed a shift to H2O2 concentration of 3%. Electrochemical investigation indicates an enhanced dissolution of copper, which might be due to the strong catalytic activity of Cu(II)-glycine complexs in decomposing H2O2 to yield hydroxyl radicals.

9:45 AM K1.5
Experimental and Numerical Analysis of Novel Slurry for Copper CMP. yun zhuang[1], Yoshitomo Shimazu[2], Leonard Borucki[3], Zhonglin Li[1], Nobuo Uotani[2] and Ara Philipossian[1]; [1]Department of Chemical and Environmental Engineering, University of Arizona, Tucson, Arizona; [2]Showa Denko K.K., Shiojiri, Nagano, Japan; [3]Intelligent Planar, Mesa, Arizona.

A novel slurry containing a proprietary inhibitor was analyzed in terms of its frictional, tribological, thermal and removal rate attributes for copper CMP applications. Experiments were performed on a scaled polisher using an IC-1000 k-groove pad (no sub-pad) and blanket PVD-deposited copper wafers. Slurry flow rate was maintained at 80 cc/min. Wafer pressure (p) and relative pad-wafer velocity (U) ranged from 2.0 to 2.5 PSI, and 0.31 to 1.09 m/s, respectively. An IR camera was used to record the pad surface temperature along the leading edge of the wafer during the CMP process. Stribeck curve analysis showed the coefficient of friction (COF) to be relatively constant (0.31 to 0.36) as a function of Sommerfeld number, indicating the dominant tribological mechanism to be that of 'boundary lubrication'. Analysis of removal rate at various values of p*U showed highly non-Prestonian behavior with three distinct regions as follows: An 'initial region' (values of p*U ranging from 4,500 to 11,000 Pa-m/s), where removal rate increased monotonically from 90 to 350 A/min. An 'intermediate region' (values of p*U ranging from 11,000 to 15,000 Pa-m/s) where removal rate increased sharply from 350 to approximately 4,000 A/min. And a 'final region' (values of p*U ranging from 15,000 to 20,000 Pa-m/s), where removal rate increased gradually from 4,000 to 4,700 A/min. The inherent non-Prestonian behavior of the slurry was believed to be due to the presence of the proprietary inhibitor in the formulation. During polishing, the oxidant in the slurry was believed to form a softened layer on the copper surface that was protected by the inhibitor. In the 'initial region', removal rate was determined by the speed with which the inhibitor layer was removed, while in the 'intermediate region' and the 'final region' the inhibitor layer would rapidly abrade off, thus leading to a significant increase in removal rate. Based on the measured pad temperature data, a thermal model previously developed for the heat exchange between the copper wafer, the pad and the slurry was used to predict the wafer temperature during the process. The removal rate was then calculated in the 'initial region' and 'final region' using a Langmuir-Hinshelwood kinetic model with great success (R-squared values greater than 0.95 in both regions). At low values of p*U, the calculated chemical rate constant was significantly larger than the mechanical rate constant,

indicating the removal of the inhibited layer was mechanically controlled. In contrast, at high values of p*U, the chemical rate constant was significantly smaller than the mechanical rate constant, indicating that copper removal was chemically limited after the inhibited layer was abraded off the surface.

10:30 AM K1.6
Invesitigations on Novel modified fumed abrasives from the system SiO2 and Al2O3 for Cu CMP applications. Dieter Zeidler[1], Johann W. Bartha[1], Wolfgang Lortz[2] and Ralph Brandes[3]; [1]Inst. for Semiconductor- and Microsystems Technology, Dresden University, Dresden, SN, Germany; [2]Res. & Dev., Degussa AG, Hanau, HS, Germany; [3]Global CMP Application, Degussa Corp., Piscataway, New Jersey.

Due to the increasing demands in lithography, high end microelectronic processes require a constantly growing degree of global planarization. This fact in combination with an extension of the multitude of materials to be processed, created a demand for polishing slurries designed to meet very specific properties with respect to removal rate, selectivity and surface quality. Today fumed and colloidal silica as well as alumina are among the abrasives used for metal polishing. In this study novel fumed particles from the system silica / alumina have been studied. Significant differences in the removal rate as well as the quality of the polished surface have been observed for the polishing of Cu, TaN and SiO2 when applying different Al2O3 or SiO2 abrasives or mixtures thereof in slurries with identical chemical environment. When using the same abrasive concentration with similar particle size distribution and identical chemistry in the slurry, the differences in the polishing behavior have to be related to the hardness, young modulus and surface charge transfer. The most important nanoscale interactions for the CMP process are the fast formation of a thin surface layer and the mechanical abrasion of this surface film. By scanning several newly designed abrasives used in slurries with identical chemistry it was tried to assign the particle properties to the polishing behavior with respect to removal rate, planarization behavior, selectivity and roughness. In order to study the interaction between particles and the surface layer we investigated the Cu CMP process, utilizing a chemistry consisting of phthalate or glycine as complexing agent and H2O2 as oxidizer. Some of the fumed abrasives, based on SiO2 or Al2O3 have also been modified by incorporating different doping atoms. By this a modification of the mechanical properties and the particle surface charge or surface reactivity was obtained. The polishing of Cu/TaN layers revealed a significant change of the RR, the planarization behavior and the selectivity of Cu vs. TaN and TaN vs. SiO2. Besides improvements in the polishing process itself for the Cu/TaN system, the investigations with modified abrasives enable a deeper insight into the interaction mechanism between the abrasives and the surface layer. Due to the possibility to specifically design abrasives, it might be possible to tailor the particles to generate a low stress polishing, which could be useful for applications such as low-k materials.

10:45 AM K1.7
Novel Organic Abrasive Particles for Copper CMP at Low Down Force. Krishnayya Cheemalapati[1], Atanu Roy Chowdhury[1], Yuzhuo Li[1], Kwok Tang[2] and Guomin Bian[2]; [1]Chemistry, Clarkson University, Potsdam, New York; [2]Dynea, Mississauga, Ontario, Canada.

With the integration of copper as interconnect and low k materials as dielectric, the CMP community is facing an ever increasing demand on reducing defectivity without scarifying production throughput. One such strategy is to lower the polishing pressure from conventional 3-5 psi to below 1 psi. Such a move has placed tremendous challenges to the tool manufactures, consumable suppliers (especially the slurry vendors), and end-users. It is a challenge to remain the high throughput (MRR and selectivity) at low down force without using harsh abrasives. In this study a set of pure organic particles with unique bulk and surface properties are investigated for their potential applications in metal CMP. Unlike conventional abrasive particles such silica or alumina, these unique particles are designed to specifically interact with the metal surface to be polished and significantly modify the rheological behavior of the slurry. The obvious advantage of using such particles is the reduction of defects during CMP. The consequence of using such particles is also its ability to provide unsurpassed high selectivity in removal rate for copper over barrier and dielectric materials due to their weak interaction with these surfaces. The added benefit for slurry that uses such particles is to allow CMP process conducted at a lower down force without compromising the throughput. In this presentation, the physical and chemical characteristics of these unique organic particles will be presented first. Blanket and patterned wafer polishing results using slurries formulated based on these unique particles will be introduced. The potential advantages of such slurry formulation over slurries that are prepared using conventional abrasive particles will be illustrated with comparative results. Finally the potential role of these particles in the copper low k integration scheme will be examined.

11:00 AM K1.8
Nanoscale Investigation of Mechanical and Chemical Effects During Copper CMP. Su-Ho Jung[1], Seung-Mahn Lee[1] and Rajiv Singh[2]; [1]Materials Science and Engineering, University of Florida, Gainesville, Florida; [2]Microelectronics Research Center, University of Texas, Austin, Texas.

Chemical mechanical polishing (CMP) of Copper is typically achieved by the synergistic interaction of chemical and mechanical effects. The formation and removal of a chemically modified surface film controls this CMP process. There have been very few studies on the characterization of nano-scale effects during the metal polishing. In this study we have conducted a detailed investigation of the surface layer effects during the CMP process. The dynamics of the surface layer formation was determined using transient electrochemical measurements, while the mechanical properties of the surface layer were determined using nano-mechanical measurements. The effect of the chemical additives (hydrogen peroxide, benzotriazole, citric acid, and pH) on the mechanical properties of the nano-scale layer was delineated. In order to resolve the synergistic mechanical aspects, the particle size and its concentration were varied during the polishing process. A model incorporating effects of the nano-scale layer formation and its subsequent removal with respect to particle size effects is also proposed.

11:15 AM K1.9
Reactivity and Removal Mechanism of Copper with Various Organic Additives in Copper CMP Slurry. Dae-Hong Eom, Young-Jae Kang, Ja-Hyung Han and Jin-Goo Park; Metallurgy and Materials Engineering, Hanyang University, Ansan, South Korea.

The Cu CMP process is tend to apply low pressure and high rpm due to the delamination of Cu/low-k films. The role of organic passivation film grown on Cu surface becomes important to understand the CMP performance in Cu slurry. Cu removal rate during CMP process is strongly dependent on the growth of passivation film. Cu surface generally reacts with organic complexing agent in slurry and grows a passivation layer. However, the growth mechanism of passivation film in various organic complexing solutions is poorly understood. In this study, reactivity of Cu with various organic additives is evaluated and chemical and mechanical properties of passivation layer are characterized by electrochemical polisher combined with EG&G potentiostat and XPS (x-ray photo-electron spectroscopy). Organic acids, bi-carboxylic acids, oxalic acid, malonic acid and maleic acid with different C-H chain, as complexing agents and hydrogen peroxide (H2O2) as oxidant are used for the formation of passivating film. In-situ electrochemical analysis of Cu in various slurries is performed using electrochemical polisher. Also, etch and polish rates are evaluated with different composition of slurry as functions of process parameters such as pressure and rpm.

11:30 AM K1.10
Experimental Investigation of Surface Properties of Particles and Their Effects on Cu CMP. Joe J. Zhao[2], Yuzhuo Li[2], Helen G. Xu[1] and Hong Liang[1]; [1]Mechanical Engineering, University of Alaska Fairbanks, Fairbanks, Alaska; [2]Chemistry, Clarkson University, Postdam, New York.

The surface properties of nanoabrasive particles have profound influence on CMP performance. In this study, we investigated the correlation between surface properties and the frictional behavior of some silica particles under various oxidizing conditions. More specifically, the friction and wear of copper surface against a polyurethane pad have been measured in the presence of slurries that contained these abrasive particles and were formulated for Cu CMP. The surface qualities and wear mechanisms were then investigated under the scanning electron microscope. The experimental results indicated that the frictional force is not only a function of the particle surface property but also a function of the extent of copper surface modification. In this presentation, experimental design and results will be first presented. The implication of this study to the design of copper CMP slurry will also be discussed.

11:45 AM K1.11
Ultra Low Pressure Copper CMP Using Particle Based Non-Prestonian Slurries. Rajiv Singh[1], Kyo-Se Choi[2] and Deepika Singh[2]; [1]Microelectronics Research Center, University of Texas, Austin, Texas; [2]Sinmat Inc., Gainesville, Florida.

The CMP requirements for next generation copper/low K dielectrics presents several challenges such as reduction of stresses, defectivity and surface topography during polishing while at the same time reducing the process complexity. Efforts are underway to reduce the operating CMP pressures to below 1 psi, while at the same time,

maintain high polishing rates and surface planarity. The standard slurries used in the industry for polishing of copper/low K dielectrics are typically Prestonian in nature, i.e. the polishing rate increases linearly with applied pressure. The increase in removal with applied pressure has been primarily attributed to increased pad-wafer contact area with increasing pressure. To increase the polishing rates at lower pressure, more aggressive etching agents need to be added in the polishing slurries. This leads to high static removal rates and high removal rates at lower pressures (< 0.5 psi). However, to maintain high planarity, the polishing rates at low pressures (< 0.5 psi) should be kept to a minimum value. Thus the Prestonian slurries are expected to show some limitations in terms of achieving optimum performance for low stress polishing. In contrast, non-Prestonian slurries, or slurries which exhibit non-linear polishing characteristics may be better suited for low pressure polishing of copper/low k dielectrics. The non-Prestonian behavior has been attributed to their unique removal mechanism. A threshold pressure for removal of the surface modified layer exists in these systems. Below the threshold pressure, the CMP process cannot remove the surface layer. Above the threshold pressure value, substantial removal of the surface layer takes place, leading to rapid polishing. Due to this reason it is possible to achieve high planarity and high removal rates under reduced pressure polishing conditions (< 1 psi). Thus the non-Prestonian slurries are expected to be more suitable for polishing of copper/low K dielectrics in low stress environments. This talk will focus on the use of non-Prestonian slurries for copper polishing. The mechanism of material removal as well as the stress developed during the process will be discussed in detail.

SESSION K2: Metal CMP Modeling
Chair: David Stein
Tuesday Afternoon, April 13, 2004
Room 2007 (Moscone West)

1:30 PM *K2.1
The Mechanism of Metal Chemical-Mechanical-Polishing (CMP) Revisited. Frank B Kaufman, Cabot Microelectronics Company, Aurora, Illinois.

The metal CMP dynamic repassivation mechanism published at the dawn of the CMP era has played a critical role as a key reference template for describing the mechanism of that new process technology. In this invited talk we will review the current status of this mechanistic picture gathered from recent literature publications. Then we will present new CMP polish and in-process sensor data, and modeling results, obtained on both simple Cu CMP chemistry systems, and actual slurries, which will shed further light on critical aspects of the operative mechanism.

2:00 PM K2.2
A Model of Cu-CMP. Ed Paul[1], Vlasta Brusic[2], Fred Sun[2], Jian Zhang[2], Robert Vacassy[2] and Frank Kaufman[2]; [1]Stockton College, Pomona, New Jersey; [2]Cabot Microelectronics, Aurora, Illinois.

A model of copper CMP, based on a previously successful model of tungsten CMP, has been developed. The model predicts the polishing rate as a function of oxidizer concentration and of the polishing pressure and speed. Experimental data will illustrate how the model can be used to interpret trends in the polishing rate as these variables change.

2:15 PM K2.3
Dishing and Erosion Studies of Cu-CMP. Inho Yoon[1], Sum Huan Ng[2], Andres Osorno[2], Daniel Osorno[2] and Steven Danyluk[2]; [1]The School of Material Science and Engineering, Georgia Institute of Technology, Atlanta, Georgia; [2]The George W. Woodruff School of Mechanical Engineering, Georgia Institute of Technology, Atlanta, Georgia.

It is well known that the polishing of electrodeposited copper in vias represents a considerable challenge in the production of smooth, flat surfaces. The copper is subject to dishing and erosion, and scale the extent of which is related to the geometry and scale of the vias. We have studied the erosion and dishing of electro-deposited copper on specially designed patterned, (100) p-type silicon wafers. The patterns had structures with varying line-width and density. Dishing and erosion were measured as a function of the pattern geometry, location on the wafer and polishing conditions. The polishing was done on a modified laboratory-scale Struers polisher where the normal load, velocity and slurry delivery could be varied. The measured dishing and erosion were then compared to a model that included the subambient pressures at the silicon / pad interface.

2:30 PM K2.4
Coherent Chip-Scale Modeling for Copper CMP Pattern Dependence. Hong Cai[1], Tae Park[1], Duane Boning[1], Hyungjun Kim[2], Youngsoo Kang[2], Sibum Kim[2] and Jeong-Gun Lee[2]; [1]Microsystems Technology Laboratories, MIT, Cambridge, Massachusetts; [2]Hynix Semiconductor, Cheongju, Chungbuk, South Korea.

With shrinking of interconnect dimensions (both vertical and lateral) and improvements in Chemical-Mechanical Polish (CMP) processes, our previously reported copper CMP pattern dependence model, developed at the quarter micron technology node, faces accuracy limits in predicting dishing and erosion for advanced technologies. The latest CMP data shows that the model prediction errors are comparable to the reduced topographic variation, indicating that the previous model needs an improvement in accuracy. In this research, we present an improved and coherent model framework for copper bulk polishing, copper over-polishing, and barrier layer polishing. The integration of contact wear model and step-height model is more seamlessly implemented and clears inherent shortcomings in the previous model. In the new model, a local density instead of the effective density computed by using a planarization length is used, and only a contact wear coefficient characterizes the planarization capability which avoids the conflict between the planarization length and the contact wear coefficient. Another advantage of the new model is that since we are using a similar model framework for different polishing steps, it is possible to directly compare basic process characteristics, such as pad stiffness, of different polishing steps. Results with the new model show a significant improvement of the modeling accuracy to better than 100 Angstroms of root-mean square error. Furthermore, an added benefit of using the coherent model is that it can be more easily adapted to the modeling of multi-level metallization processes when combined with electroplating and dielectric deposition pattern dependence models.

SESSION K3: Planarization Equipment
Chair: Ara Philipossian
Tuesday Afternoon, April 13, 2004
Room 2007 (Moscone West)

3:15 PM *K3.1
Polish profile control using magnetic control head. Manabu Tsujimura, Executive officer, Ebara Corporation, Fujisawa, Kanagawa, Japan.

Magnetic bearing technology is widely used in various technical fields, and is particularly appreciated in the semiconductor industry, where it is applied to the turbo molecular pump and wafer transfer system due to the excellent controllability it provides, even at speeds as high as 50,000 rpm. This report discusses the adoption of magnetic bearing technology to control the wafer carrier tilt angle during polishing. When the wafer is polished on a viscoelastic pad, the wafer carrier is inclined and pressed into the pad. Therefore, the reaction force on the wafer from the pad is concentrated at the wafer edge, increasing the polish rate at the edge relative to the rest of the wafer. Modification of the tilt angle is thought to offer a possible means of normalizing the distribution of the reaction force from the pad and correcting the non-uniformity of the polish rate. The wafer carrier was confirmed to press slightly into the pad and to be tilted 18 x 10-5 rad by the viscoelasticity of the pad (without tilt angle control). Constant current control led to better control of the polish rate profile relative to feedback control. The polish rate in the outer area of the wafer was increased by tilting the carrier to the positive side, and the polish rate of the wafer center area could be reduced by tilting it to the negative side. The best profile was obtained with control current of Im = -0.4 A. When the wafer carrier was tilted in the reverse direction, the polish rate became almost zero. It was concluded that hydro-planing occurred between the wafer and the pad. Accordingly, this report demonstrates the possibility of improving the polish rate profile by maintaining the wafer carrier in a horizontal position using magnetic control.

3:45 PM K3.2
Adaptive Piezo-Controlled Carrier for CMP Processing. Johann W. Bartha[2], Christian-Toralf Weber[1], Dieter Zeidler[2] and Juergen Weiser[1]; [1]IGAM mbH, Barleben/Magdeburg, Germany; [2]IHM, TU Dresden, Dresden, Germany.

The chemical mechanical planarization is a wide-spread procedure for the production of semiconductors, however it is increasingly applicable with the production of MEMS as well as optical systems. With ever smaller structures increasingly higher demands are made on the accuracy of the planarization processes, i.e. an as evenly as possible removal rate (RR) with a low non-uniformity (WIWNU). Particularly with 12" wafers there arise non-uniformities of the removal profile not only in the boundary region, but also within the entire wafer surface. So far it was tried to adjust the special retaining rings, back pressure

as well as global convex or concave deformation of the carrier to obtain an even removal profile. The IGAM engineering company for applied mechanics Ltd. developed a piezo driven active carrier with individually controllable rings with an integrated (no collector ring) control. The dimensioning of the carrier took place on the basis of contact analyses with finite elements, whereby the pressure distribution between wafer and polishing pad was computed. Due to the high stiffness of the piezo elements the profile of the carrier and thus the pressure distribution in the polishing area can be adjusted over the entire wafer surface with a high accuracy independently of downforce. The IHM at the University of Dresden accomplished polishing attempts for the characterization of the removal behavior (SiO2 process) using a 6" variant of the system on a laboratory CMP machine Mecapol E460 manufactured by Presi. The pressure distribution of the controlled carrier measured before polishing with Tekscan flexible pressure sensor arrays between polishing pad and wafer is identical to the reached removal profile. Although only three piezo actuators acting on each ring, the results show a very even, rotationally symmetric distribution of the pressure and removal profile in circumferential direction on the wafer. The WIWNU could be improved by purposeful control of the rings in one correction step around 50%. The aim of further developments is the local (not rotationally symmetric) influence of the removal profile as well as the integration of sensor technology including the control of the process.

4:00 PM K3.3
Metrological Assessment of the Coefficient of Friction of Various Types of Silica Using the Motor Current During ILD-CMP. Harald Jacobsen[1], Eric Stachowiak[1], Gerfried Zwicker[1], Wolfgang Lortz[2] and Ralph Brandes[3]; [1]Fraunhofer ISIT, Itzehoe, Germany; [2]Degussa AG, Hanau, Germany; [3]Degussa Corporation, Piscataway, New Jersey.

For various CMP applications a large number of slurries are available on the market using abrasives, which for ILD polishing are typically either based on colloidal silica or fumed silica. Both types of slurries show a different behaviour for material removal, which can be described by Prestons Law and modifications thereof. In all equations to describe removal rate a coefficient C_p is used to describe the differences in polishing behaviour deriving from variables such as the applied pad or slurry characteristics as well as the coefficient of friction (COF) between wafer, slurry and pad. In the work presented the COF was for the first time determined metrologically for 8" PECVD-oxid blanket wafers using a CMP tool (Peter Wolters Surface Technology, PM 200) meeting the standards of production of a fab by a systematic assessment of motor currents for different products of pressure and velocity (p x v). Measuring the motor current allows a conclusion to the torsional moment M and the applied energy E, respectively which are required for the actuation of the polishing equipment (E_{Loss}) and the actual CMP process (E_{CMP}). Based on the total energy (E_{Total}) the energy E_{CMP} can be deduced by determination of the energy loss E_{Loss} ($E_{CMP} = E_{Total} - E_{Loss}$). The energy E_{Total} was determined during the production process, whereas a nearly frictionless polishing process has determined the energy loss with the system steel on ice. The COF can be evaluated from E_{CMP}. Five test slurries based on fumed silica as the abrasive with BET surface areas from 50 m^2/g to 300 m^2/g were investigated in ILD polishing. These test slurries were provided by Degussa and were dispersed by a novel high-shear milling method (wet jet mill). Two commercial standard slurries (one with colloidal silica as an abrasive and one with fumed silica) were included in the investigation for reference. With all test slurries it could be shown that the inserted energy E_{CMP} is proportional to the product of pressure and velocity (p x v). The COF of the parameter domain considered here does not depend from the inserted energy or the product of p x v in a first approximation. For all tested slurries it was demonstrated that the COF and the removal rate (RR) behave analogously (low COF $\rightarrow$ low RR). Using the expression for the friction force F_f and considering a full wafer contact on the pad allows the calculation of the shear rate γ. By measuring the viscosity η with a high-pressure capillary viscometer the dependency of the viscosity over the shear rate $\eta = f(\gamma)$ can be obtained. These measurements have shown that η is not a constant in the shear rate range relevant for CMP. Using the obtained viscosity values a maximum slurry film thickness in the range of 90 μm $-$ 145 μm could be calculated. The above investigations demonstrated that the coefficient of friction (COF) and the viscosity η in CMP have to be both considered in an equation describing removal rate.

4:15 PM K3.4
Impact of Various Oxidizing Species on Copper CMP using a Controlled Atmosphere Polishing System. Darren DeNardis[1], Toshiro Doi[1,2], Koichiro Ichikawa[3] and Ara Philipossian[1]; [1]Chemical and Environmental Engineering, University of Arizona, Tucson, Arizona; [2]Saitama University, Saitama, Japan; [3]Fujikoshi Machinery Corporation, Nagano, Japan.

A new Controlled Atmosphere Polisher (CAP) manufactured by Fujikoshi Machinery Corporation is used for CMP of copper substrates. The novel tool features a pressure-resistant chamber that hermetically contains the entire processing unit. The machine allows chamber gases to be rapidly changed during polishing. A vacuum pump or a compressor is used to maintain chamber pressure (under vacuum or pressurized conditions) at a desired set point. The objective of this research is to characterize the mechanism of copper CMP by gaining further insight into the role of various oxidizing species that affect the formation of intermediate copper complex layers crucial for subsequent abrasion. This is achieved by utilizing various high-purity gases such as oxygen, air and nitrogen during polish and by modulating their concentration in the slurry by controlling the chamber pressure. Moreover, the presence or absence of oxidants such as hydrogen peroxide, in conjunction with the above chamber conditions, is expected to shed further light into the complex interplay of various processing parameters on copper removal. In this study, the CAP was used to polish 100-mm copper discs on Rodel IC-1400 k-grooved pads. In all cases, Fujimi's PL-7102 copper slurry, flowing at 80 cc/min, was used. Wafer pressures and relative pad-wafer velocities ranged from 1.5 to 3.2 PSI, and from 0.26 to 0.52 m/s, respectively. First, the effect of chamber pressure was quantified by polishing at 1 and 5 ATM under ultra-pure air conditions. In the presence of hydrogen peroxide, chamber pressure had no effect on copper removal rate. At a chamber pressure of 5 ATM, as long as the slurry contained hydrogen peroxide, the type of gas used (i.e. air, nitrogen or oxygen) had no effect on copper removal. This suggested that the concentration of dissolved gaseous species in the slurry (in accordance with Henry's Law) were insignificant compared to the concentration of oxidizing species associated with hydrogen peroxide. The feasibility of oxidizing the copper surface (in the absence of hydrogen peroxide) using dissolved gaseous species was investigated by comparing the effect of oxygen and nitrogen chamber gases at 5 ATM. Copper removal under oxygen was considerably lower in the absence of hydrogen peroxide compared to cases where hydrogen peroxide was used. However, removal rate was higher by a factor of 4 when oxygen was used instead of nitrogen (in the absence of hydrogen peroxide). This suggests that external sources of oxygen (especially ones with lower values of Henry's constant) have the potential of reducing, or even eliminating, the need for hydrogen peroxide for copper polish.

4:30 PM K3.5
Electropolishing of Copper with High Planarization Efficiency and Low Surface Defect. Sue-Hong Liu[1], Chih Chen[1], Jia-Min Shieh[2] and Bau-Tong Dai[2]; [1]Department of Materials Science and Engineering, National Chiao Tung University, Hsinchu, Taiwan; [2]National Nano Device Laboratories, Hsinchu, Taiwan.

Planarization of copper is generally recognized as the crucial concern with damascene metallization schemes. Conventional Chemical mechanical planarization (CMP) of copper contains mechanically stress on copper films and hard abrasives that may cause damaged and scratched surfaces on copper. Copper electropolishing (EP) technology could be used as replaced methods for first-step CMP process because EP offers potential advantages such as a lower waste stream, stress-free to the copper and dielectric films, and reduced particle on copper surface. In this study, a clean and scratch-free surface was obtained after electropolishing by using phosphoric acid with various organic addtives as the electrolyte. Excellent planarization efficiency (PE) up to 96% can be obtained on high step-height copper damascenes by the mass-transport-controlled dissolution of copper at the anode under constant voltage condition. This may be due to that the diffusivities of H+ became more different between outside and inside the trenches in electrolytes when the organic additives presented. Furthermore, with appropriate ratio of addtives and phosphoric acid, significant reduction in density of etching pits on polished copper surface was realized. All the additives that can reduce etching pits and yield high planarization efficiency during EP were found to have oxyhydrogen function groups, and they were also effective in a wide range of concentration. X-ray photoelectron spectroscopy, potentiodynamic (PD) polarization, and electrochemical impedence spectroscopy were also performed to investigate the roles of these additives during polishing. This results will be presented in detailed in the conference.

SESSION K4: Poster Session
Tuesday Evening, April 13, 2004
8:00 PM
Salons 8-9 (Marriott)

K4.1
A Study on CMP Scratch Defects with Atomic Force Microscope. Guanghui Fu, Lam Research Corporation, Fremont, California.

Chemical Mechanical Polishing (CMP) has become a mainstream

process method in submicron Integrated Circuit (IC) manufacturing. With this technology, surface roughness of a polished wafer is generally below one nanometer. However, CMP processes will generate scratches on the wafer surface. Those scratches are killer defects because they may distort the pattern, lead to bridges at the metallization step and create chip reliability problem. Scratch control becomes more and more important as the IC industry works toward smaller feature size. In this paper, we use Atomic Force Microscope (AFM) to study the scratches of polished wafers. The experiments were performed on patterned Cu wafers, which were processed with Teres CMP system from Lam Research Corporation. The scratch defects were found by AIT, a dark-field pattern wafer defect inspection tool from KLA-Tencor. The tool's optical microscope was used to review the defects. The defect coordinate information from AIT was used to locate defects in AFM measurements. The paper shows the AFM measurements of a razor scratch on a 100um by 100um bond pad structure. We find the scratch depth changes rapidly along the scratching direction. This is explained by the experimental results on the nanoindentation of polycrystalline Cu thin film. Indentation load-displacement curves for Cu thin films show a number of discrete bursts in the penetration depth, and each burst happens at almost a constant load. This phenomenon is explained as a result of dislocation burst.

K4.2
A Study on the Self-Stopping CMP Process for the Planarization of the High Step Height(@step height>1.5um) Pattern. Kwang Bok Kim, Ki-Huon Jang, Hyo-Jin Lee, Joung-Duk Ko, Kyung-Hyun Kim, In-Seac Hwang, Yong-Sun Ko and Chang-Lyong Song; Semicondouctor R&D Center, Samsung Electronics Co Ltd., Youngin-City,Kyunggi-Do, South Korea.

CMP(Chemical Mechanical Planarization) process is widely used to reduce step height in semiconductor fabrication processes. As a design rule shrinks, a highly planar surface becomes inevitable within wafer scales. In order to get a high degree of a planarization, self-stopping characteristics of a ceria-based slurry should be studied and used in semiconductor process. In this study, threshold polishing pressure for a self-stopping characteristics was obtained by optimizing down pressure, pad conditioning, and mixing ratio of ceria abrasive and additive. A series of experiments were made to optimize the threshold polishing pressure in variable line & space patterns that consist of 0.8um step height and unit oxide film. As a result, self-stopping cmp process is twice batter than conventional silica-based process with respect to planarity and WIWNU. In addition, WIWNU and step height was dramatically decreased to less than 1000Å when applying to real fabrication devices over 2um step height.

K4.3
A Kinematical Study on Chemical Mechanical Polishing (CMP). Guanghui Fu, Lam Research Corporation, Fremont, California.

Most kinematical studies on Chemical Mechanical Polishing (CMP) are focused on the spatial distribution of relative velocity on the wafer surface. Under typical CMP conditions, this velocity spatial variation is small and is generally neglected. In this paper, we investigate another aspect of CMP kinematics: the trajectory on the wafer surface by an arbitrary fixed point on the pad surface. Both rotary tool and linear tool are considered in this study. The trajectory study is important in many ways. For example, it helps to pinpoint the scratch source. Wafer map with clear scratch patterns can be analyzed with this technique to locate the scratch source. Slurry distribution is an important factor on the Within Wafer Nonuniformity (WIWNU). Trajectory study is a rough estimation on how the slurry passes the wafer surface. From the simulation, different points on the pad polish the wafer in different ways. A certain point on the pad polishes any part of the wafer surface while other points polish only some parts of the wafer surface. Pad wear is related to the removal rate drop and polishing profile drift. Trajectory study can indicate the extent of pad wear at different pad locations. Insight from such study will help to improve the conditioning kinematics design and facilitate the conditioning recipe generation.

K4.4
Modeling of Pressure Non-uniformity at a Die Scale for ILD CMP. Jihong Choi and David Dornfeld; Mechanical Engineering, University of California at Berkeley, Berkeley, California.

The non-uniformity of film thickness at a die scale, after the ILD CMP process, is mainly attributed to non-uniform pressure distribution across patterns on a die. Therefore, measurement of the pressure on each pattern is the key to a study on pattern dependent CMP performance at a die scale. However, in-situ measurement for the pressure, especially at a die scale, is limited experimentally. In this study, as an alternative to the direct measurement, a finite element modeling (FEM) technique is employed to estimate pressure distribution at a die scale. Based on the assumption that the time dependent visco-elastic behavior of a polishing pad, consisting of pores, walls, and grooves, can be modeled on equivalent static material properties with the help of published data, simplified two-dimensional static FEM analysis was conducted on two different test patterns to evaluate the pattern dependent pressure distribution at a die scale. The pressure distribution calculated from the FEM analysis is compared with the effective pattern density in the pattern-density-based oxide CMP model. Since the effective pattern density on a test pattern depends on the selected weighting function and its characterization length, three different functions - square-shaped step weighting function, circle-shaped step weighting function, and elliptic integral weighting function- are used, and the characterization length of each function is set to give the best match between the pressure distribution and the effective pattern density. This FEM analysis was further taken to evaluate the effects of thickness and material properties of each layer on the degree of pattern dependant pressure non-uniformity at a die scale for a typical polishing pad made up of a hard and a soft layer. The analysis shows that the degree of pressure non-uniformity at a die scale increases with the combination of a stiff hard layer and a thick soft layer, while it decreases with the combination of a stiff soft layer and a thick hard layer.

K4.5
The Effect of Abrasive of Cu-CMP on Grobal Planarization. Yutaka Nomura, Yasuo Kamigata, Hiroshi Ono, Hiroki Terazaki and Masato Yoshida; Hitachi Chemical Co., Ltd., Hitachi city, Ibaraki, Japan.

Relationship between abrasive properties and Cu-CMP performance were investigated, in order to design a high planarity performance Cu-CMP slurry. One of the most effective properties for the global planarization was found to ζpotential in Cu-CMP slurry. ζpotential value of both abrasive and Cu-Complex layer on Cu metal greatly affected the global planarization. At the conference, mechanism of improving the planarity will be discussed in detail.

K4.6
Evaluation of the Tribological Properties and Wear Rate of Different Semiconductor Grade Plastic Materials for Contact Retaining Ring Application. William G Easter[5], Parshuram Balkrishna Zantye[1,2], Arun Kumar Sikder[2] and Ashok Kumar[1,2]; [1]Department of Mechanical Engineering, University of South Florida, Tampa, Florida; [2]Nanomaterials and Nanomanufacturing Research Center, University of South Florida, Tampa, Florida; [3]Department of Electrical Engineering, University of South Florida, Tampa, Florida; [4]Department of Chemistry, University of South Florida, Tampa, Florida; [5]Semplastic Inc., Daytona Beach, Florida.

In order to exploit the avenues available in the presently growing CMP consumable market, considerable amount of research is being carried out in the areas of the polishing pads and slurries. With the increasing implementation of the contact retaining ring in the wafer carrier head, the tribological properties and wear rate of the different semiconductor grade plastic candidate retaining ring materials need to be investigated. In this research, 1 inch coupons of commercially available semiconductor grade plastics namely EPPS, PPS and PEEK were polished in fumed silica, alumina and ceria slurry using the CETR CP-4 bench top CMP machine. A comparitive study was performed on the Acoustic Emission (AE) and Coefficient of Friction (COF) data obtained during each polishing run. The wear rate for each polishing run was calculated there by giving an estimate of the life time of the contact retaining ring made of the given material. In order to gauge the effect of the contact retaining ring surface on the polisihing pad, Atomic Force Microscopy (AFM) was performed on the 1 inch coupons after a polishing run in each type of slurry.

K4.7
Investigation of the Mechanical Integrity and its Impact on Polishing for a Novel Polyurethane Pad.
Parshuram Balkrishna Zantye[1,2], Arun Sikder[2], Raghu Mudhivarthi[1,2], Sadiya Hasan[1,2], Shenique Johnson[1,2], Ashok Kumar[1,2], Serguei Ostapenko[3,2], Julie Harmon[4] and Abhaneshwar Prasad[5]; [1]Department of Mechanical Engineering, University of South Florida, Tampa, Florida; [2]Nanomaterials and Nanomanufacturing Research Center, University of South Florida, Tampa, Florida; [3]Electrical Engineering, University of South Florida, Tampa, Florida; [4]Department of Chemistry, University of South Florida, Tampa, Florida; [5]Cabot Microelectronics, Aurora, Illinois.

There is a wide spread interest in field of CMP consumables due a lucrative existing and potential market, as the CMP process becomes widely implemented in the field of microelectronics fabrication. A non-destructive Ultra Sound Testing (UST) developed at USF has already been sucessfully used to map the variation of specific gravity in the pad. There is a need to corelate the results of the specific

gravity variation with the actual polishing results there by establishing the pad dependence on wafer to wafer non uniformity (WTWNU) and with in wafer non uniformity (WIWNU) occuring during the CMP process. Novel CMP pads developed by Cabot Microelectronics for Interlayer Dielectric (ILD) polishing have been investigated using the UST technique. The mechanical properties of the pads were evaluated using Dynamic Mechanical Analysis (DMA), pad compression test and nanoindentation. 6 inch coupons from areas of higher and lower ultrasound transmission were punched out and their tribological properties and removal rate were estimated during CMP of high density plasma ILD material. Due to the relaxation in the built in stresses that cause the non homogenity in the pad, the candidate pad coupons punched out of the regions of different specific gravity did not show much variation in mechanical and tribological properties.

K4.8
Interactions between abrasive particles and film surfaces in low down force copper CMP. Yuchun Wang, Fred Sun and Joe Hawkins; Cabot Microelectronics, Aurora, Illinois.

In copper-low k CMP for 65 nm and beyond, a robust copper CMP slurry at low down force should have high copper removal rate, efficient planarization, decent overpolishing window, and low defects. The choice of abrasive particles in conjunction with film forming species is critical to achieve good planarity and residue free Cu CMP, especially at higher level metal interconnect. This paper addresses the interactions of different particles (alumina, silica, specially treated particles) and film surfaces in copper CMP at 0.7 psi to 2 psi. The performance of low dishing erosion and smooth surface finish is discussed with the proposed mechanism.

K4.9
Effect of particle interaction on agglomeration of silica-based CMP slurries. alex tregub, Intel Corp, Santa Clara,, California.

Chemical Mechanical Planarization has become a method of choice for planarization of metal and oxide layers in microelectronics industry. A CMP process includes up to 16 variables that need to be controlled to achieve a stable CMP process. One of the major variables in CMP is related to slurry compositions. In particularly, a uniform distribution of the sizes of the abrasive particle in slurry is crucial for a stable CMP performance. It is known that, for a silica-based slurry, particle agglomerates of above 1 micron size are the major cause of the wafer defects. The agglomerates can be unstable, and depend on addition of chemical additives and shearing during the CMP process. In this work, the authors studied agglomeration of the fumed and colloidal silica-based slurries using dynamic rheometry, zeta potential tests, and an accusizer. Dynamic rheometry tests were conducted in a steady and dynamic modes, including frequency and time sweep tests. The shear rate varied in the range from 10 to 2000 1/sec, and all tests were performed at three different temperatures of 5, 30, and 50oC. Slurry viscosity, determined using a steady state rheometry, was correlated to the particle charge, characterized by zeta potential, and to the particle sizes obtained using accusizer. Additionally, rheometer was used for slurry shearing to study change of characteristics of slurries subjected to shear. The effect of adding surfactants and various pH and aging on slurry stability was also studied. It was shown that: Slurry viscosity can be correlated to the particle size distribution and particle charge; Slurry shearing causes decrease of particle repulsion and, thus, increase of sizes of particle agglomerates; Addition of surfactants diminishes the effect of shearing.

K4.10
Measurement of Electroplated Copper Overburden for Advanced Process Development and Control. Joshua Tower[1], Michael Gostein[1], Alex Maznev[1] and Koichi Otsubo[2]; [1]Philips Advanced Metrology Systems, Natick, Massachusetts; [2]Philips Advanced Metrology Systems, Tokyo, Japan.

The wafer-level and die-level uniformity of the copper electroplating process has a direct effect on the final post-polish thickness of copper interconnect lines used in advanced integrated circuits. Control of the plating process involves a complex balance between the chemical properties of the plating bath, the variable parameters of the plating machine, and the characteristics of the incoming wafer. Furthermore, post-plating thickness can depend greatly on the local feature geometry, with some process conditions resulting in excess deposition above narrow-linewidth structures. Therefore, process development and control require high-speed copper thickness metrology to provide rapid feedback of thickness over a variety of structures on the wafer. In this work, we used a non-contact metrology system based on laser-induced surface acoustic waves to evaluate the uniformity of electroplated copper. Several wafers were prepared using a variety of plating conditions to affect the copper overburden thickness. Measurements of overburden were made on line arrays of various line-width and pitch, as well as on the surrounding field dielectric. In general, the overburden was found to be thicker above the line arrays, as compared to the surrounding field. This difference in overburden thickness is referred to here as the 'array step height'. In the wafers studied, the magnitude of the array step height is very dependent on the plating process and on the position within the wafer. For example, the array step height for a 50% density line array varies from zero to 5000 Angstroms in these wafers, depending on process conditions. The large overburden non-uniformity would generally result in poor uniformity of the copper line thickness after polish (CMP). The array step height was found to be progressively lower as the copper percentage of the array decreases from 50% to 35% and to 20%. We also found that the overburden in the field area is reduced as the adjacent array step height increases, presumably because of depletion of reactant in the plating bath in the vicinity of the high overburden regions above the arrays.

SESSION K5: Polishing Pads
Chair: Greg Shinn
Wednesday Morning, April 14, 2004
Room 2007 (Moscone West)

8:30 AM K5.1
Micro Feature Pad Development and Its Performance in Chemical Mechanical Polishing. Sunghoon Lee and David A. Dornfeld; Department of Mechanical Engineering, University of California, Berkeley, Berkeley, California.

Chemical Mechanical Polishing (CMP) has been considered to be one of the most capable IC fabrication technologies to achieve planar surfaces essential for very large scale integrated circuits (VLSI). During the CMP process, a wafer is placed face side down on a pad with high pressure. The wafer and pad rotate simultaneously with slurry. High pressure, rotational speeds, and chemical-mechanical reactions enhanced by the slurry result in a planarized surface on a wafer. Generally, a pad has a wavy surface profile consisting of peaks and valleys. Real contact between the wafer and pad occurs on the crests of the pad (i.e. active region). Fresh slurry temporarily collects in the valleys (i.e. reservoir region) and is supplied to the active regions through the relative movement of the wafer and pad, traveling between the peaks and valleys (i.e. transition region). However, degradation in the pad is generated mainly by abrasion in the active region. As a result, the real contact area increases and the real contact pressure drops rapidly during the CMP process, causing the material removal rate (MRR) to decrease dramatically in the absence of a conditioning process. The pad deterioration mechanism mentioned above causes many problems such as removal rate fluctuations (process repeatability), scratches from diamond conditioning grit (pad maintenance), erosion, dishing (chip-topography dependence), and so on. A novel set of design rules is suggested in this paper for pad fabrication that satisfies the demands for a new pad with features such as constant real contact area, no-diamond conditioning, and topography independence. Experimentally, pads are fabricated using micro-molding technology, and the repeatability and chip-topography independence issues are specifically investigated with patterned wafers. The pad introduced here is composed of two layers; soft and hard. The soft material with high compressibility and compliance serves to homogenize the pressure distribution over a wafer, and the hard layer, which is backed up by the soft layer, makes contact with the wafer and is used to achieve planarity. To improve repeatability in the CMP process, constant contact area between pad and wafer should be maintained. In this pad, the hard layer is composed of evenly spaced micro scale square features. Using this design, better repeatability can be obtained. In a conventional pad, stress concentration occurs around coarse or small patterns on a wafer. This uneven pressure distribution generates polishing defects such as a wavy surface in ILD CMP, and dishing or erosion in metal CMP. The reason for these defects is related to the continuity of contact points between the hard layer and wafer. In a new pad, only the isolated hard cubes make contact with wafer. The stress is independently applied on the hard cubes and is absorbed by the soft layer. As a result, a uniform stress distribution is acquired across wafer.

8:45 AM *K5.2
Characterization of CMP Pad Surface Texture and Pad-Wafer Contact. Gregory P. Muldowney and David B. James, Advanced Research and Pad Technology Groups, Rohm and Haas Electronic Materials, CMP Technologies, Newark, DE.

Abstract Not Available

9:15 AM K5.3
Modeling CMP Transport and Kinetics at the Pad Groove Scale. Gregory P Muldowney, Advanced Research and Pad Technology Groups, Rohm and Haas Electronic Materials, CMP Technologies, Newark, DE.

Chemical mechanical planarization (CMP) of semiconductors relies on an intense confluence of micron-scale transport and kinetics. Groove design and surface texture of CMP polishing pads are two readily adjustable means of process control as planarizers are scaled to 300-mm wafers. A 3-D fluid flow and kinetics model of the full pad-wafer gap, including both grooves and land area flow properties, was developed to research the influence of these essential pad features at a scale not previously studied. A novel CMP pad characterization test was devised to determine the surface flow resistance of a textured polishing pad. Fluid pressure loss profiles under controlled flow conditions were measured across the pad while compressed by a flat instrumented plate. Experiments yielded the void fraction and characteristic length of the pad asperity layer, two physical descriptors which accurately reflected differences among pad materials and degrees of conditioning. Asymmetries in pressure profiles also revealed anisotropy in some textured surfaces at a level undetected heretofore. The experimental flow resistances enabled a computational fluid dynamics simulation to be built for a dual-axis CMP machine with a rotating pad having 131 concentric circular grooves under a rotating 200-mm wafer. Grooves were modeled as fluid regions and land areas as porous-media regions. Results revealed abrupt point-to-point variations in polish conditions between the grooves and land areas including fluid velocity, wall shear stress, and transient mixing behavior. These effects were more pronounced at higher polish pressures. Flow patterns in individual grooves were found to be highly variable from one location to another beneath the rotating wafer such that pathlines of slurry particles were dissimilar point to point even within the same concentric circular groove. Chemical reaction rates at the wafer surface were studied by including first-order kinetics for slurry activity. The effects of pad and wafer rotation, amplified by the unequal flow resistances of grooves and land areas, led to features in the steady-state concentration profile at the same spacing as the groove pitch. This unusual finding identified a direct mechanism by which polish irregularities may be formed at the scale of the grooves. Results imply unexpected directions for CMP process and consumables and improvements.

9:30 AM *K5.4
Measuring Pad Deformation During Polish.
Chris Buergin Rogers, Mechanical Engineering, Tufts University, Medford, Massachusetts.

For the past 8 years at Tufts University we have measured properties of the slurry film between the pad and wafer during polish using laser-induced fluorescence. Recently, we started making these measurements at any given instant in the process, allowing us to freeze the process. In particular, we measured the slurry film thickness at a single instant in time over a 2 cm square area under the wafer. This allows us to measure how the pad deforms around a given discontinuity (topography) in the wafer surface. In this talk I will review some of the time-averaged results in slurry thickness, temperature, and mean residence time we have taken in the past. I will spend the bulk of the talk, however, presenting the new instantaneous results of pad deformation. By measuring the slurry film thickness, we can even estimate the change in pad surface roughness under the wafer during the polishing process.

10:30 AM K5.5
High Pressure Micro-Jet Technology as an Alternative to Diamond Conditioning for ILD CMP Applications.
Darren DeNardis[1], Masano Sugiyama[1], Yoshiyuki Seike[2], Mineo Takaoka[2], Keiji Miyachi[2] and Ara Philipossian[1]; [1]Chemical and Environmental Engineering, University of Arizona, Tucson, Arizona; [2]Asahi Sunac Corporation, Owariasahi, Japan.

The efficacy of an alternative to diamond conditioning in the interlayer dielectric (ILD) CMP process was investigated. The High Pressure Micro-Jet (HPMJ) system, manufactured by Asahi Sunac Corporation, was studied to determine if the process could be used as a substitute for, or in conjunction with, conventional diamond disc pad conditioning. The system is designed to jet ultra pure water (UPW), at pressures of 5 to 20 MPa, onto the surface of the pad used for wafer polishing. In this study, the effect of using the HPMJ system for ex-situ pad conditioning was analyzed in terms of its tribological and removal rate attributes. The new process was also compared to those of in-situ diamond conditioning, ex-situ diamond conditioning and no conditioning. Experiments were performed on a scaled version of a Speedfam IPEC 472 polisher using IC-1000 perforated pads with 100-mm ILD substrates. Fujimi's PL-4217 slurry (12.5 weight percent fumed silica abrasives) was used. Slurry flow rate was maintained at 80 cc/min. The variables associated with the HPMJ system included: water jet pressure, nozzle fan angle, actuator angle, water flow rate, distance from the nozzle to the pad, and jet spray time. The effects of actuator angle and jet spray time on coefficient of friction (COF) and removal rate were investigated to optimize the HPMJ system for ILD CMP. The optimal actuator angle and jet time were found to be 25° and 30 seconds. It was found that using the HPMJ system alone resulted in higher values of COF compared to cases where no conditioning was adopted. However, the HPMJ resulted in removal rates that were similar to cases where pads were not conditioned. Ex-situ diamond conditioning and the HPMJ resulted in similar values of COF but the removal rates associated with the HPMJ were significantly lower than those associated with ex-situ diamond conditioning. In-situ diamond conditioning demonstrated greater COF and removal rate values compared to the HPMJ process. SEM analysis suggested that pad asperities existed on the pad surface after two ILD polishes for both ex-situ diamond conditioning and HPMJ conditioning, but were not apparent with no conditioning. Therefore, the lower removal rates associated with the HPMJ process were assumed to be due to the dilution of the slurry on the pad surface when HPMJ was used for conditioning. To prove this, experiments were conducted using a pilot wafer between HPMJ conditioning and the next wafer polish. The purpose of the 1-minute pilot wafer polish was to re-saturate the pad surface with slurry. The resultant average COF for HPMJ conditioning was approximately 20% less than that of ex-situ diamond conditioning (0.27 compared to 0.34). The Preston's constant associated with HPMJ conditioning was comparable to that of ex-situ diamond conditioning (6.3E-14 compared to 9.2E-14 1/Pa). Results also indicated that the lower COF associated with HPMJ conditioning has the potential of increasing pad life.

10:45 AM K5.6
Non-Destructive Evaluation Method For Psiloquest Application Specific Pads (ASP) For CMP Applications.
Parshuram Balkrishna Zantye[1,2], Arun Sikder[2], Ashok Kumar[1,2] and Yaw Obeng[3]; [1]Department of Mechanical Engineering, University of South Florida, Tampa, Florida; [2]Nanomaterials and Nanomanufacturing Research Center, University of South Florida, Tampa, Florida; [3]Psiloquest Inc., Orlando, Florida.

There is a need to develop the metrology metrics that predict the performance of the CMP pads before putting them in to service. This appears to be achievable using PsiloQuest application specific pads (ASP) in which the pad surface is tuned to match the mechanical properties of the target substrate. The ASP-pads are made up of thermoplastic foams co-extruded with condensed polyolefin. The chemical and mechanical properties pad-wafer interface is tuned by coating the pad with thin films ceramic various materials. The surface of the pads was characterized using AFM, XPS and FTIR while the hardness of the surface was measured using nanoindentation. Static coefficient of friction was measured with a hand held tribometer. Using CETR CP-4 bench top CMP tester, the pads were polished to evaluate the dynamic COF, Acoustic Emission (AE) signal and material removal rates. The COF and AE were filtered using the wavelet transform technique. Polishing experiments need to be performed on sufficiently large number of pads in order to get the statistical distribution of its tribological properties. A strong correlation was observed between the static COF, the dynamic COF and removal rate. Since the static COF and wear rate of the pad is a non destructive test, it can be used for quality control of the pads, there by considerably decreasing the pad-pad reproducibility issues commonly associated with thermoset polyurethane CMP pads. The research was supported by NSF GOALI Grant # DMI 0218141.

SESSION K6: CMP Corrosion and Cleaning
Chair: Ara Philipossian
Wednesday Morning, April 14, 2004
Room 2007 (Moscone West)

11:00 AM K6.1
Corrosion of the Copper Damascene Interconnects as a Function of the Electrochemical Plating Process Parameters.
Didem Ernur[1,2], Wen Wu[1,2], Sywert H Brongersma[1], Valentina Terzieva[1] and Karen Maex[1,2]; [1]SPDT, IMEC, LEUVEN, Belgium; [2]ESAT, K.U.L., Leuven, Belgium.

The need for high-speed microprocessors requires an increase in the number of the transistors beyond the 0.10 mm technology. This necessitates multilevel metallization together with the shrinkage in the dimensions of the Cu interconnect lines. This means repeated planarization steps with no concerns of defects and corrosion from the CMP point of view. Corrosion of the Cu damascene interconnects during CMP were addressed by several researchers [1,2]. The CMP slurry constituents, and the barrier metal were shown to play important roles on the corrosion mechanism of Cu [3,4]. In this work, we present the influence of the type of the electrochemical plating recipe and the bath chemistry on the Cu grain size evolution and its link to Cu corrosion. Organic and inorganic acid-based model CMP solutions were tested. Chips containing isolated and semi-dense single damascene Cu lines, fabricated on silicon wafers, were used. Based on the electrical and micro structural data our results revealed that the change in the plating recipe, while keeping the bath chemistry

unchanged, induced a variation in the resistance and the grain size of Cu especially in the narrow lines. The Cu etch rate also varied as a function of the plating recipe in the case of inorganic acid based solution and presented a line width dependency with the highest etch rate in the narrow lines. This is thought to originate from the preferential attack at the grain boundaries, which are higher in volume and are shown to be a function of the plating recipe in the narrow lines. Organic acid based solutions, however, resulted in lower and line width in-dependent etching. By keeping the same recipe, we further changed the plating bath chemistry. Based on our results we suggest that the differences in the additive type and concentration not only influence the Cu grain evolution, but are also shown to pose challenges in terms of Cu corrosion of especially narrow lines. Thus better understanding of the link between the ECP and CMP parameters is critical for improved performance.

11:15 AM K6.2
Prevention of Water Mark Defects in Copper/low-k CMP Process. Ja Hyung Han[2], Dae Hong Eom[1], Sang Ho Lee[1], Jin Goo Park[1], Ja Eung Koo[2], Duk Ho Hong[2], Sang-Rok Hah[2] and Kwang-Myeun Park[2]; [1]Metallurgy and Material Eng., Hanyang University, Ansan, Gyeonggi-Do, South Korea; [2]System LSI Division, SAMSUNG Electronics, Yongin-City, South Korea.

The requirement for improved speed has made copper the interconnect metal of choice for integrated circuits (ICs) for sub-0.13um technology. However, copper patterning cannot be carried out in the conventional way since dry etching of copper is difficult due to the lack of valatile halogen compound at low temperature. To pattern copper for sub-micron technologies with a large process window, chemical mechanical polishing and the damascene technology schemes are the only choices. Especially low-k material should be used as dielectric in nano era. In Cu/low-k film CMP and post CMP cleaning, major challenges can be divided into to two issues. The first issue is the delamination of low-k material due to the weak hardness of low-k material and the second issue is the formation of watermarks on the dielectric spaces and copper lines due to hydrophobic property of low-k material. This paper presents basic surface properties of low-k material, effects of CMP on surface property and effects of surfactant treatment in post CMP cleaning. Aurora film was used as a low-k dielectric and several kinds of surfactant were tested to evaluate effects of surface modification in this experiment. CMP changes surface energy and contact angle of Aurora and shows significant improvement on wettability without chemistry change in films. Addition of surfactant makes the adsorption of water easy and improves wettability of films. Thermal desorption analysis show the effects of surfactant treatments.

11:30 AM K6.3
Adhesion of Alumina Slurry Particles on Wafer Surfaces during Cu CMP. Yi Koan Hong, Ja Hyung Han and Jin Goo Park; Department of Metallurugy and Materials Eng., Hanyang Univ., Ansan, South Korea.

The adhesion and removal of alumina particles were theoretically and experimentally investigated during Cu CMP process. The adhesion force of particles on surface was measured using an Atomic Force Microscope (AFM, Park Scientific Instruments CP Research) by directly measuring the force required to remove them from a surface. The 40 m diameter sized spherical alumina particle (Micron Co.) was attached on a Si3N4 tipless cantilever. The adhesion force was measured between particle and wafer surfaces in a liquid cell. Electroplated Cu wafers, TEOS (tetraethylorthosilicate), TaN, Coral (SiOCH) and FSG (Fluorine-doped Silicate Glass) of low-k materials were used for the experiments, respectively. Cu and TaN wafers were pre-cleaned in diluted HF (DHF, 0.01 vol%) solution for 30 sec. TEOS, Coral and FSG wafers were pre-cleaned in the SPM (Sulfuric-peroxide mixture) solution and DHF solution for 5 min and 1 min, respectively. The interaction forces between the particle and wafer surfaces during Cu CMP were calculated based on the Derjaguin-Landau-Verwey-Overbeek (DLVO) theory at different pH ranges. The adhesion forces between the particles and surfaces were also experimentally measured in different pH's slurry solution. Likewise, the magnitudes of particle contamination on wafer surfaces were observed after they were polished to confirm the resulting interaction forces. The highest particle removal efficiency was observed in cleaning solutions with the lowest adhesion force. The adhesion force between particle and surface directly related to the particle contaminations on wafers during Cu CMP process.

11:45 AM K6.4
Frictional Analysis of Various PVA Brush Roller Designs for Post-CMP Scrubbing Applications. Juan Weaver[1], Weijing Li[2], Kris Bahten[2], Larry Curtis[2] and Ara Philipossian[1]; [1]Department of Chemical Engineering, University of Arizona, Tucson, Arizona; [2]Rippey Corporation, El Dorado Hills, California.

The study consisted of analyzing two designs of PVA brush rollers, manufactured by Rippey Corporation, in terms of their frictional and tribological attributes during post-CMP scrubbing. The two types of brushes were identical to one another in all respects except the first design employed a plurality of nodules on one-fourth of its outer surface while the other did not. The inner and outer radii of both types of brushes were identical (the outer radius of the brush with nodules included the 5-mm height of the nodule). Other parameters investigated in this study were the rotational velocity of the roller (10, 20, 30, 40, 50 and 60 RPM),the nominal pH of the cleaning fluid (1.1, 7.0 and 10.7), the type of substrate being scrubbed (blanket silicon dioxide wafer and STI-patterned silicon dioxide wafer), and the applied brush pressure (0.25, 0.35, 0.45 and 0.55 PSI). All tests were conducted on an isolated single-sided post-CMP cleaning machine designed especially to measure shear forces caused by the interaction between the brush and the surface of the wafer at a sampling frequency of 10,000 times per second. This data, couple with the applied brush pressure allowed the calculation of the coefficient of friction (COF) critical for establishing the frictional and tribological attributes of the system. In all cases, higher brush pressures resulted in higher values of COF. Brushes containing nodules showed higher values of COF compared to those without nodules. This difference ranged from 1.5X at low values of pH to about 3X at neutral and high values of pH. COF associated with blanket wafers was statistically the same as those corresponding to STI patterned wafers. This suggested that blanket wafers could act as suitable candidates in establishing the frictional attributes of post-CMP brush scubbing of typical industrial processes. This observation was supported by traditional Stribeck curve analysis indicating the absence of 'boundary lubrication' throughout the entire range of Sommerfeld numbers employed. Specifically, at low values of pH, regardless of the type of substrate, the tribological mechanism associated with brushes containing nodules was that of 'partial lubrication' at higher applied pressures (i.e. 0.55 and 0.45 PSI) and that of 'hydrodynamic lubrication' at the lower pressures. At neutral and high values of pH, tribological mechanism was that of 'hydrodynamic lubrication' across the entire range of applied pressures and Sommerfled numbers. Real-time frictional waveforms (in time domain) were further analyzed using spectral techniques to yield information regarding the distribution of the total mechanical energy of the process in frequency domain. The resulting 'interfacial interaction index' which was a measure of the total mechanical energy of the process due to stick-slip phenomena, confirmed the tribological results summarized above.

SESSION K7: Novel CMP Applications
Chair: Johann Bartha
Wednesday Afternoon, April 14, 2004
Room 2007 (Moscone West)

1:30 PM *K7.1
Utility of CMP in Engineered Semiconductor Substrates. Eugene Arthur Fitzgerald, Materials Science and Engineering, MIT, Cambridge, Massachusetts.

Traditional use of CMP as applied to semiconductors began with the art of polishing bulk semiconductor substrates. As the back-end of CMOS integrated circuits grew to multiple metal layers, CMP migrated to solve the problems of interconnect layer morphology. As the use of CMP has removed some performance constraints of the back-end, CMP is now playing an increasing role in the fabrication of advanced engineered substrates to improve performance of front-end transistors. CMP may also bring new device functionality into the front-end as well. In this talk, we overview the use of CMP in creating strained Si/SiGe/Si, strained Si/SiGe/OI, Ge on Si, GOI, and GaAs on Si. We also will highlight the devices which can be created on these engineered substrates, and their potential use in future systems. We conclude with a case study of the commercialization of strained Si substrates.

2:00 PM K7.2
Advances on the CMP Process on Fixed Abrasive Pads for the Polishing of SOI Substrates with high degree of flatness. Martin Kulawski[1], Frauke Weimar[2], Jari Makinen[3], Kimmo Henttinen[1] and Ilkka Suni[1]; [1]VTT Microelectronics, Espoo, Finland; [2]3M Europe, Neuss, Germany; [3]Okmetic Oy, Espoo, Finland.

When presenting the new approach of polishing silicon wafers for thick film silicon-on insulator (SOI) substrates by fixed abrasive pads in 2003 the state of development was early, however showed encouraging results. Incoming ground material of total thickness variation (TTV) of below 0,5 μm was seen able to be kept maintained under the polishing and superior surface quality was achieved under the processing. With a further developed pad the obstacles of too low removal and slow processing have been able to be addressed and an overall improved performance was shown without loosing the superior

capabilities of the first approaches. By going on in the evolution of the fixed abrasive technology and driving on the process development it has been able to reach the major specifications of a practicable manufacturing process. The further developed consumable-process solution has been applied to a variety of materials and was able to show even enhanced removal rates. Long term tests have been carried out to demonstrate the stability of the process. By integration of the process with final haze removal into enhanced grinding methods and a suitable post-CMP cleaning it can be shown that a new alternative method is achieved to manufacture highly flat SOI substrates. Results are confirmed by capacitive thickness measurements as well as atomic force microscopy (AFM). For waviness measurements optical reflection methods are used. In a comparison with conventional processing the quality of the overall process performance is demonstrated.

2:15 PM K7.3
Analysis of Nanotopography Generation in Polishing Process of Silicon Substrate. Hiromichi Isogai and Katsuyoshi Kojima; Silicon Company, TOSHIBA CERAMICS CO.,LTD., Kitakanbaragun, Niigata Prefecture, Japan.

This paper describes a new model, which can analyze the effect of polishing conditions on nanotopography of silicon (Si) wafer in chemical mechanical polishing (CMP) process. Nanotopography characterization has been affects the thickness uniformity of dielectric oxide-film on Si wafer as CMP. CMP has become increasingly important in the production of multilayer integrated circuits due to the decrease in feature size and increase in pattern density in ULSI devices. Therefore, reducing nanotopography of Si substrate is essential to obtain high-performance of Si substrate in CMP. We have developed the model based on the Prestonfs equation for calculating nanotopography change process in Si substrate polishing. In this model, various conditions of polishing relating to the structure of polish apparatus can be taken into consideration. To investigate the influence of polishing conditions, such as a pad material and a motion of substrate, nanotopography was analyzed by using this model. Thus, the mechanisms of nanotopography generation in polishing process of Si substrate were clarified during CMP process.

2:30 PM *K7.4
MEMS-based Retinal Prosthesis Electrode Array.
David J. Stein[1,2], Kurt Wessendorf[1], Murat Okandan[1], Ramona Myers[1], Tom Lemp[1] and Conrad James[1]; [1]Sandia National Labs, Albuquerque, New Mexico; [2]University of New Mexico, Albuquerque, New Mexico.

200,000 people each year go blind due to age-related macular degeneration and retinitis pigmentosa. People who suffer from these diseases lose functionality of the rods and cones - the cells in the retina that detect light. However, functionality of the nerves that transmit information from the rods and cones to the brain is not impaired. The US DOE and NIH have teamed to develop a device that will act in lieu of the rods and cones and bring limited sight back to these patients. Many challenges exist, especially that of building a device that will be placed onto the retina to stimulate the nerve endings. Our challenge is to design and build a 1,000 electrode array to allow those suffering from these diseases to see well enough to be independently mobile and to read large type. Sandia's approach is to build the device as a MEMS structure where the individual electrodes are attached to springs to compensate for the curvature and topography of the retina. This talk will give an overview of the retinal prosthesis project and describe the structure and manufacturing issues associated with the MEMS electrode array. CMP is used extensively during fabrication and these aspects will be emphasized. Sandia National Laboratories is a multiprogram laboratory operated by Sandia Corporation for the United States Department of Energy's NNSA under contract DE-AC04-94AL85000

3:30 PM K7.5
The Application of Chemical Mechanical Polishing for Nickel Used in MEMS Devices. Arun Vijayakumar, Tianbao Du, Kalpathy Sundaram and Vimal Desai; Advanced Materials Processing and Analysis Center, University of Central Florida, Orlando, Florida.

Chemical mechanical planarization has found extensive application in the fabrication of micro-electro-mechanical systems (MEMS) devices. Nickel is a promising material to realize movable structures for MEMS application. The development of CMP slurry chemistry for Ni that provides good CMP performance is the key in enabling CMP technology for MEMS device fabrication. Unfortunately, very little work has been reported in terms of the electrochemical interaction of Ni with various CMP slurry constituents such as oxidizers, complexants and inhibitors. In this study, the dissolution, passivation and polishing behavior of nickel with various slurry constituents was studied under dynamic and static conditions. Electrochemical techniques were used to investigate the interplay between the different slurry chemistries such as type of abrasives, pH, oxidizer concentration, chelating agent concentration and corrosion inhibitor. The affected surface layers of the statically etched Ni-disc were investigated using X-ray photoelectron spectroscopy (XPS) and scanning electron microscopy (SEM). The surface planarity was studied by atomic force microscopy (AFM). Preliminary results obtained with different slurry chemistries seem to indicate that the surface chemistry and electrochemical characteristic play an important role in controlling the Ni polishing behavior.

3:45 PM K7.6
CMP Modeling and Characterization for Polysilicon MEMS Structures. Brian David Tang[1,2] and Duane S. Boning[1,2]; [1]Electrical Engineering and Computer Science, MIT, Cambridge, Massachusetts; [2]Microsystems Technology Laboratories, MIT, Cambridge, Massachusetts.

The current bedrock technology for integrated circuit (IC) planarization, chemical-mechanical polishing is beginning to play an important role in microelectromechnical systems (MEMS). However, MEMS devices operate with different feature sizes in comparison to ICs. While smaller is better for circuits, MEMS features are usually found to be larger in order to fulfill mechanical functions. We present an experiment to characterize and model a polysilicon CMP process with the specific goal of examining MEMS sized test structures. We utilize previously discussed models and examine whether assumptions from IC CMP can be applied to MEMS CMP. An analysis of the data collected points to a polishing dependence on not only pattern density, but also partly on feature size. In addition to larger feature sizes, MEMS devices can have new and different kinds of layouts in comparison to IC layouts. While carrying out our characterization experiments, we discover that certain layout features relevant to MEMS can negatively impact the ability of existing CMP models to simulate polishing, motivating the need for further model development.

4:00 PM *K7.7
Planarization Issues in Wafer-Level 3D Integration.
Jian-Qiang (James) Lu, Timothy S. Cale and Ronald J. Gutmann; Focus Center - New York, Rensselaer: Interconnections for Hyperintegration, Rensselaer Polytechnic Institute, Troy, New York.

Planarization Issues in Wafer-Level 3D Integration J.-Q. Lu, T.S. Cale and R.J. Gutmann Focus Center - New York, Rensselaer: Interconnections for Hyperintegration Rensselaer Polytechnic Institute, luj@rpi.edu Wafer-level three-dimensional (3D) integration offers the potential for the highest volumetric density of signal electronics and optoelectronics with a high density of high-performance vertical interconnections. Various 3D technology platforms have been investigated, with different combinations of alternative alignment, bonding, thinning and inter-wafer interconnection technologies. Initial emphasis has been on the different wafer-to-wafer alignment strategies, bonding techniques, and inter-wafer interconnection approaches. However, wafer-level planarization requirements can be significantly different for the various 3D platforms. After a brief overview of the potential of wafer-level 3D integration and a summary of viable 3D technology platforms, this paper will focus on comparison of wafer-level planarization needs for these platforms. Particularly, planarization issues associated with wafer bonding interface, wafer thinning, and damascene patterning of inter-wafer interconnects will be addressed for the various 3D technology platforms. Inter-wafer interconnect dummy-structure needs will also be discussed.

4:30 PM K7.8
Chemical Mechanical Planarization of Ruthenium Thin Film.
Sang-Ho Lee[1], Young-Jae Kang[1], Jin-Goo Park[1] and Sang-Ick Lee[2]; [1]Metallurgy and Materials Eng., Hanyang University, Ansan, Kyunggido, South Korea; [2]Advanced Process-CMP, Hynix Semiconductor, Ichon-si, Kyunggido, South Korea.

MIM (Metal-Insulator-Metal) structure capacitor is required in the future DRAM technology because of the cell capacitance in shrinking cell size. The novel metals such as ruthenium have been suggested as the bottom electrode materials in the fabrication of the capacitor. However, there are several issues in the application of these metals for MIM structure capacitor. One of them is the difficulty of planarizing the steps of cylinder capacitor to meet the requirement of the backend scalability. The maskless planarization technology or chemical mechanical planarization has been introduced for the planarization of the metal layers after the capacitor process. In this study, the chemical mechanical planarization process of ruthenium for the formation of bottom electrode in capacitor was investigated. Ruthenium thin film was polished by nitric acid and cerium ammonium nitrate based slurry. Because ruthenium has very high resistance to chemical reaction at room temperature, it was difficult to find the chemistry that etch and polish the ruthenium surface.

Strong oxidizers such as cerium ammonium nitrate, ammonium persulfate, urea and potassium permanganate were applied to etch the ruthenium surface with and without nitric acid. From etching experiment, it was found that only the cerium ammonium nitrate or chemical mixture of cerium ammonium nitrate and nitric acid etched the ruthenium thin film slightly. However, the ruthenium thin film was not etched in the other applied chemicals. Chemical Mechanical Planarization experiments were carried out with Logitech PM5 polisher and Rodel IC 1400 pad. The carrier and platen speed was set at 30rpm. The down pressure of carrier was 6.5 psi and slurry flow rate was constant to 200ml/min during the polishing. Also, polishing time was 1 min. From the results of etching, slurry was made with nitric acid and cerium ammonium nitrate to polish the ruthenium. The removal rate of ruthenium was 85.47nm without abrasive particles. When alumina particles were added into the slurry solution from 1 to 3 wt%, the removal rate increased over 100nm and saturated. In the constant abrasive particle content, concentration of cerium ammonium nitrate was controlled. As the concentration of cerium ammonium nitrate increased, the removal rate of ruthenium was about 100nm at 6 wt% nitric acid uniformly. However, the removal rate increased linearly in the slurry containing only cerium ammonium nitrate and abrasive particles. From these results, the polishing behavior of ruthenium was dependent on the concentration of cerium ammonium nitrate when nitric acid was not added to slurry.

SESSION K8: CMP Modeling
Chair: Duane Boning
Thursday Morning, April 15, 2004
Room 2007 (Moscone West)

8:30 AM *K8.1
Modeling and Design of Consumables in Chemical Mechanical Planarization (CMP). David Dornfeld, Sunghoon Lee, Jianfeng Luo, Jihong Choi and Edward Hwang; Mechanical Engineering, University of California, Berkeley, California.

Mechanical issues such as abrasive size, distribution, composition as well as the characteristics of pads (composition, mechanical properties, surface features and texture, etc.), kinematics of the process (polishing trajectory and velocity), pressure and pad conditioning as well as chemistry effects of the slurry (pH, stability, viscosity, etc.) and, of course, wafer materials all contribute to the uncertainty in CMP performance. The understanding of the different roles played by the input values and their interactions, is critical for the optimization of cost, material removal rate, non-uniformity, micro-scratches and the control/design of CMP, [1]. Material removal models (primarily mechanical aspects) describing these interactions, which are unique do to the small pad hardness and different size scales of the pad asperity and the polishing abrasives, have been developed by [2]-[4]. This model is based on solid-solid contact mode in CMP and assumptions of plastic contact over the wafer-abrasive interface and pad-abrasive interface, a normal distribution of abrasive size and a periodic rough surface of the polishing pad. A number of important input values have been integrated into the model. MRR formulations developed based on the model as functions of down pressure and abrasive size have been presented and verified using experimental results. An important observation of both experimental researchers and those focusing on modeling has been that characteristics of the pad, slurry chemistry and abrasives (if present) - the consumables - play an important role in the success of the process. This success is measured in terms of selectivity, with-in wafer nonuniformity (WIWNU), with-in die nonuniformity (WIDNU), scratching, dishing and erosion. This paper reviews current modeling efforts and, specially with respect to the design and performance prediction of consumables, presents some novel ideas on designed consumables including specially designed pads [5]. References [1] Evans, J., et al., Material Removal Mechanisms in Lapping and Polishing, STC G Keynote, CIRP Annals, 52, 2, 2003. [2] Luo, J. F. and Dornfeld, D. A., Material Removal Mechanism in CMP: Theory and Modeling, IEEE Trans. Semiconductor Manufacturing, 14, 2, 2001, pp. 112-133. [3] Luo, J. F. and Dornfeld, D. A., Material removal regions in CMP for Submicron Integrated Circuit Fabrication: Coupling Effects of Slurry Chemicals, Abrasive Size Distribution and Wafer-pad Contact Area, IEEE Trans. Semiconductor Manufacturing, 2003, vol. 16, no. 1, pp. 45-56. [4] Luo, J. F. and Dornfeld, D. A., Effects of abrasive size distribution in chemical-mechanical planarization (CMP): modeling and verification, IEEE Trans. Semiconductor Manufacturing, 16, 3, 2003, to appear. [5] Lee, S., Kim, H., Jeong, H. and Dornfeld, D. Pad contact area characterization in CMP using micro molding technology, Proc. 18th ASPE Annual Meeting, Portland OR, Nov. 2003.

9:00 AM K8.2
Revisiting the Removal Rate Model for Oxide CMP.
Jamshid Sorooshian[1], Ara Philipossian[1], Len Borucki[2], David Stein[3], Dale Hetherington[3] and Robert Timon[3]; [1]University of Arizona, Tucson, Arizona; [2]Intelligent Planar, Mesa, Arizona; [3]Sandia National Laboratories, Albuquerque, New Mexico.

Experiments were performed on a Speedfam-IPEC 472 Avanti polisher using 150-mm blanket thermal silicon dioxide and thermally annealed LPCVD TEOS wafers. Nominal pad surface temperatures of 12, 25, 35 and 45 degrees Celsius were used to investigate the effects of pad temperature (T), wafer pressure (p) and relative pad-wafer velocity (U) on removal rate. Wafer pressures of 3, 5 and 7 PSI, and relative pad-wafer velocities of 0.31 and 0.93 m/s were examined. Consumables included Rodel's IC-1400 k-grooved pad and Cabot's D7300 silica-based slurry (12.5 percent silica by weight) at a constant flow rate of 270 cc/min. Conditioning was performed in-situ using a 100-grit diamond disc. An IR camera was used to record the pad surface temperature on 10 points along the leading and trailing edges of the wafer during the CMP process. At a given pad temperature, the relationship between removal rate and p x U showed significant deviations from Prestonian behavior for both types of silicon dioxide substrates. The greatest non-Prestonian behavior was observed when relative pad-wafer velocity increased from 0.31 to 0.93 m/s. By assuming a Langmuir-Hinshelwood kinetics model, the removal rate data at various pad temperatures were used to determine the apparent activation energy (based on the mean pad temperature) of the thermally activated step. At low values of p x U apparent activation energies were estimated to be around 0.1 eV for both the thermal silicon dioxide and TEOS oxide substrates. This value was considered to be too low (and likely incorrect) since at low values of p x U, removal was mechanically limited. At high values of p x U where the removal was thermally activated, the apparent activation energies were more realistically around 0.4 eV for both types of substrates. Based on a previously developed thermal model (albeit for a polisher using 100-mm substrates) increasing the relative pad-wafer velocity from 0.31 to 0.93 was shown to impact the heat partition function between the pad and the wafer such that 17 percent less heat dissipated through the wafer during processing. Moreover, the above model indicated that higher sliding velocities removed more heat from the wafer due to forced convection caused by the centrifugal motion of the slurry. The above two phenomena were believed to be responsible for the observed dramatic deviation in the Prestonian behavior of the process at various velocities. Studies are currently underway to extend the above thermal model to the 150-mm polisher used in these experiments. Such an undertaking would not only allow accurate determination of the wafer temperature as a function of sliding velocity, but would also help determine the actual activation energy of the process thus theoretically explaining and reconciling the observed non-Prestonian behavior.

9:15 AM K8.3
Tribological Issues and Modeling of Removal Behavior of the Doped and Undoped SiO2 Interlayer Dielectric Planarization.
Arun Sikder[2], Swetha Thagella[2], Parshuram Balkrishna Zantye[1,2], Ashok Kumar[1,2] and Jiro Yota[3]; [1]Department of Mechanical Engineering, University of South Florida, Tampa, Florida; [2]Nanomaterials and Nanomanufacturing Research Center, University of South Florida, Tampa, Florida; [3]Advanced Process Technology, Skywork Solutions, Inc, Newbury Park, California.

Understanding the tribological, mechanical and structural properties of an inorganic and organic dielectric layer in the CMP (chemical mechanical planarization) process is critical for successful evaluation and implementation of these materials with the copper metallization. In this research we will present the mechanical and tribological properties of various doped and undoped oxide low- k materials like undoped (SiO2), carbon doped (SiOC), fluorine doped (SiOF) oxides using nanoindentation and CMP tribometer. Films were deposited using both chemical vapor deposition and spin-on method. Polishing of these films was performed on a bench-top CMP tester using colloidal oxide slurry. Coefficient of friction and acoustic emission signals have significant effect on the polishing behavior. It was found that carbon and fluorine incorporation in the Si-O network weaken the mechanical integrity of the structure and behave differently in slurry selective to SiO2 films. Surface of the films are investigated before and after polishing using atomic force microscopy. Roughness and section analysis of the films after polishing show the variation in wear mechanism. A materials removal model is derived on the basis that the material removal rate (MRR) is equal to the material removed by a single abrasive and the number of active abrasives involved in material removal. A new method of calculating active abrasive particles will be presented. It is found that with the increase in pressure, the MRR increases due to increase in the number of active abrasives. The model is validated by comparing the results with experimental results.

9:30 AM K8.4
Pad Asperity Parameters for CMP Process Simulation.
Takafumi Yoshida, Dept of TCAD, YNT-jp.com, Hikari, Yamaguchi, Japan.

This paper reviews the contact mechanics between the surface of a wafer and the asperity of the polishing pad for CMP from basic asperity such as spherical, rectangular, and conical shapes to more general asperity with a height distribution. This paper also proposes a practical method to bridge a measured profile of pad asperity in microscopic scale to a set of simple parameters which describe the elastic behavior for CMP process simulation in lager scale. We show a scalable CMP simulation using the proposed pad asperity parameters.

9:45 AM K8.5
Assessment of Planarization length variation by the Step-Polish-Response (SPR) Method. Johann W. Bartha, Tilo Bormann, Kathrin Estel and Dieter Zeidler; Inst. for Semiconductor- and Microsystems Technology, Dresden University, Dresden, SN, Germany.

In spite of the fact, that the main purpose of CMP is the planarization of surfaces, most processes are optimized with respect to the removal rate. Possibly this is due to a lack in the determination of the planarization behavior. Boning has proposed the application of specific test pattern to determine the planarization length and he described the concept of convoluting a transfer function with the test pattern to obtain the shape of the finished surface. The problem in the interpretation of the data is the interaction of neighboring pattern with different pattern densities. We used the approach to apply the polish to the most simple imaginable pattern, which is a simple step with an extension of the up and down areas much larger than the planarization length. In this case the spatial derivative of the resulting contour represents directly the demanding transfer function used for the convolution. We have applied this concept (SPR Step-Polish-Response) to evaluate the polish of oxide and copper. Wafers with steps concentrically arranged around the center of the wafer in an about 1um thick SiO2 or Cu film with a terrace extension of 1 to 5 cm have been prepared. During polish the initially infinite steep step widens up, yielding the planarization length as a function of removal respectively polishing time. These experiments reveal 3 significant effects: i) The planarization length is a function of polish time respectively of the removal and reaches its equilibrium value at polish times respectively removals much larger than used in manufacturing. ii) It turned out that the transfer function is not necessarily a symmetric function, which enables to describe a different polishing behavior at the down and up area close to the step. iii) We observed transfer functions with side minima, resulting in an enhanced removal rate at the down area close to the step edge and a reduced removal rate at the up area close to the step edge. Profiles showing this behavior will be presented. Significant differences in the evaluation of the planarization length could be quantified depending on the pad, slurry and tool parameters. Surprisingly our first experiments revealed a decrease in planarization length by the addition of BTA in a copper slurry. We will present further results on the variation of additives in the slurry to study chemical effects and variations of machine parameters to study mechanical effects, that impact the planarization behavior at Oxide and Copper steps.

SESSION K9: Oxide and STI CMP
Chair: Johann Bartha
Thursday Morning, April 15, 2004
Room 2007 (Moscone West)

10:30 AM *K9.1
Cerium Oxide Abrasives - Observations and Analysis. David Russell Evans, Sharp Laboratories of America, Inc., Camas, Washington.

The use of cerium oxide (ceria) as an abrasive for dielectric chemical mechanical polishing has had a "checkered" history to say the least. Nevertheless, its use remains attractive for this purpose because of favorable polishing characteristics that are generally not obtainable using conventional fumed or colloidal silica abrasives. To be specific, large differences are commonly observed between the removal rates of thin film silicon oxide, silicon nitride, and/or polysilicon. Moreover, such rate selectivity invariably favors the removal of oxide films, which of course, is precisely what is desirable for fabrication of modern shallow trench isolation schemes. Even so, oxide CMP using ceria abrasive often exhibits unusual characteristics that cannot be explained adequately by conventional polishing models based on pad/asperity elasticity or pressure distribution over features. Most notably, non-conventional, observed behaviors can be collected under the rubric of "slow start pehnomena". In addition, a further and possibly related objectional characteristic of ceria abrasive is an enhanced tendency toward defectivity in comparison with conventional silica. In this work, the behavior of ceria abrasives within the context of CMP will be summarized and analyzed.

11:00 AM K9.2
Analysis of Ceria Slurry Particles Pre and Post Dielectric CMP. Naga Chandrasekaran, CMP, Micron Technology, Inc., Boise, Idaho.

Chemo mechanical polishing (CMP) has emerged as a primary processing step in the manufacture of semiconductor devices. With constantly reducing device dimensions and increasing density, the requirements placed on CMP process performance has increased significantly. This has led to the development of a variety of process consumables including, polishing pads, slurry, conditioner, and tool set. Among the process consumables, the primary factor affecting CMP performance is the abrasive slurry. It has been commonly accepted that in dielectric CMP, the slurry chemically modifies the dielectric surface forming a hydrated layer, which is then removed by mechanical abrasion between the slurry particles and the work surface. While several other models have also been proposed to achieve a better understanding of the material removal mechanisms in CMP, there has been limited experimental evidence in direct support of these models, primarily due to the dynamics of the CMP process. A better understanding of the particle-work surface interactions can be achieved by studying the change in abrasive particle morphology and chemistry pre and post CMP, which is the objective of this study. In this investigation, ceria slurry is used to polish two different dielectric materials, namely, thermal oxide and thermal nitride. The slurry used to polish these materials is collected post CMP and analyzed to understand the change in particle size distribution, abrasive morphology (SEM), and chemistry (XRD and TGA). It was observed that the tail of the particle size distribution exhibits a significant shift post CMP while the mean size change is relatively insignificant. This indicates that the material removal mechanism is primarily achieved by the particles in the tail regime during the initial polishing cycle. As polishing proceeds, the large particles are either embedded deeper into the film or broken down at the interface between the wafer surface and the polishing pad leading to higher particle-wafer contact area. It can be suggested that these large particles in the tail end of the slurry are the primary defect generation sources as well. Under the SEM, the particle morphology was observed to change relatively less, however, the number of larger particles was observed to be reduced. XRD and TGA analysis also suggested possible reactants on the surface of the particles. In addition, differences in the material removal mechanisms between oxide and nitride with ceria slurry were also noted. The degree of change in abrasive morphology was observed to be depend on the pad hardness. When experiments were performed on a softer pad, the material removal was observed to drop. In addition, the change in particle size and morphology was observed to be minimal compared to a hard pad.

11:15 AM K9.3
WID Rnit Variation Improvements of HSS STI CMP Process using Modified Scribe Lane Pattern Design. kwon hyuk, choi yongsoo, lee sanghwa, chung myungjin and song yongwook; Memory Research Division, Hynix Semiconductor Inc., Icheon, Kyeonggi-do, South Korea.

Recently, Ceria-based high selectivity slurry (HSS) has been used at the shallow trench isolation (STI) CMP process. This is due to HSS has proven to give much improved field oxide (Fox) dishing and thickness range, as well as nitride loss and range, compared to traditional silica based slurry. In the DRAM process, trench isolation technology normally requires characteristics that high polishing rate for field oxide layer and low polishing rate for nitride barrier layer. Therefore, high selectivity characteristics between oxide and nitride layer play an important role in STI-CMP process and usually can be achieved using Ceria-based abrasive with additives. Generally, HSS STI-CMP process consists of two polishing steps. In the first step, conventional silica-based low selectivity slurry has generally being used for the reduction of initial step height. In the second step, ceria-based high selectivity slurry is used especially for excellent nitride surface finishing and this second polishing step was developed as following 3-stage. First stage is oxide removal stage, that oxides deposited on the top of nitride are removed by ceria abrasive in the slurry. Second stage is nitride passivation stage, which has a characteristic that additives are adsorbed on the exposed nitride surface and embodies high selectivity characteristics. And third stage is over-polishing stage, in this final stage, mechanical polishing factor is more dominant than chemical factor especially in the large-pitched and low pattern density region. As a result, nitride erosion increases with over-polishing going on. In the scribe lane, which is located at the frame neighboring two chips, most of the test patterns for monitoring electrical characteristics of memory device as well as various key patterns for photo process are formed. In this area, any regions that aren't drawn at STI mask level were generally leaved as field oxide (Fox) region. For this reason, the pattern density of these regions is lower than that of the main chip area, and cause nitride erosion by dishing phenomena during HSS STI-CMP process. Nitride erosion occurred in the scribe lane region, could affect erosion

properties of cell region in main chip area, results in within die remain nitride variation and marginal fail in device characteristics. In order to prevent this problem, unit-pattern density in the scribe lane was increased by modifying some of the large Fox patterns into Active patterns. Using this modified pattern design, any possible side effects on photo key alignment process were checked. The effects of improvement in within die remain nitride variation were investigated by FIB-TEM analysis and its correlation with electrical properties were explained. Analysis results shows there weren't not any side effect on the following photo process and the range of within die remain nitride thickness decreased up to 59.2%(45Å), the range of cell Vt(Thresh hold voltage) decreased up to 13.5mV.

11:30 AM K9.4
Characterizing STI CMP Processes with an STI Test Mask Having Realistic Geometic Shapes. Xiaolin Xie[1], Tae Park[1], Hong Cai[1], Duane Boning[1], Aaron Smith[2], Neil Patel[2] and Paul Allard[2]; [1]Microsystems Technology Laboratories, MIT, Cambridge, Massachusetts; [2]National Semiconductor Corporation, South Portland, Massachusetts.

Chemical mechanical polishing (CMP) has become the enabling planarization method for shallow trench isolation (STI) of sub 0.25um technology. CMP is able to reduce topography over longer lateral distances than earlier techniques; however, CMP still suffers from pattern dependencies that result in large variation in the post-polish profile across the chips. In the STI process, insufficient polish will leave residue nitride and cause device failure, while excess dishing and erosion degrade device performance. Our group has proposed several chip-scale CMP density models [1], and methodology using designed dielectric CMP test mask to characterize CMP process. The methodology has proven helpful in understanding STI CMP, however, it has several limitations as the existing test mask primarily consists of arrays of lines and spaces of large feature size varying from 10 to 100 um. In this paper, we present a new STI characterization mask, which consists of various rectangular, L-shape, and X-shape structures of feature sizes down to submicron. The mask is designed to study advanced STI CMP processes better, as it is more representative of real STI structures. The small feature size amplifies the effects of edge acceleration and oxide deposition bias, thus enables us to study their impacts better. Experimental data from a state of the art CMP process is shown to verify the existing methodology, and these secondary effects are explored. The new mask and data guide ongoing development of improved pattern STI CMP models. [1] D. O. Ouma, D. S. Boning, J. E. Chung, W. G. Easter, V. Saxena, S. Misra, and A. Crevasse, "Characterization and Modeling of Oxide Chemical Mechanical Polishing Using Planarization Length and Pattern Density Concepts," IEEE Transactions on Semiconductor Manufacturing, vol. 15, no. 2, pp. 232-244, May 2002.

11:45 AM K9.5
Investigation and Control of Chemical and Surface Chemical Effects in Dielectric Chemical Mechanical Polishing. Jeremiah Terrell Abiade[1], Wonseop Choi[1], Vishal Khosla[1] and Rajiv K. Singh[2]; [1]Materials Science & Engineering and Particle Engineering Research Center, University of Florida, Gainesville, Florida; [2]University of Texas, Austin, Texas.

With the ever-increasing popularity of STI in microelectronic device fabrication designer slurries must be tailored to meet increasingly stringent planarity requirements. Although, dielectric polishing is primarily mechanical in nature, the chemical and the surface chemical effects can be tailored to enhance selectivity and planarity. Examples of chemical and surface chemical effects in dielectric CMP include control of slurry pH, use of reactive particles such as cerium dioxide, and addition of surfactants to modulate the particle-substrate interactions. Cerium dioxide particles are utilized due to an increase in substrate dissolution through particle-substrate bonding, which accelerates material removal of the dielectric surface. The increased efficiency of reactive particles is largely dependant on the area of contact between particle and substrate during polishing. The chemical nature of the interaction between the particles and surfactants has been investigated using AFM, XPS, and an in-situ friction force apparatus. Both the pH and cerium dioxide particles have been found to significantly affect the near surface region of the oxide film. Additionally, the use of surfactants to control the planarity and enhance selectivity will be discussed.