SYMPOSIUM B

Silicon Materials—Processing, Characterization, and Reliability

April 1 – 5, 2002

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* Invited paper

TUTORIAL

B: INTEGRATED CIRCUIT FABRICATION AND YIELD CONTROL
Monday, April 1, 2002
8:00 a.m. - 12:00 p.m.
Salon 11/12 (Marriott)

This course, starting from buying the wafer up to the final interconnect structure made by Cu damascene techniques, details in a step by step fashion how a logic chip is built and what are the associated yield control/metrology steps encountered during the build. The build basics which are applicable to any state of the art chip facility will be described in such detail that the student will understand the reason for each step, and the logic of the sequence used, as well as systematic and random defects encountered. Additionally, a discussion of an active yield control strategy is described including in line inspection techniques and points, use of CD, overlay and AFM, both now and in the near in future. Cross sections, top down defect appearance, etc., at each key step will be used to illustrate the build process and the defects found. The instructor, Professor Ernest Levine of the School of Nanosciences and Nanoengineering of the University of Albany, has spent 24 years working in the field which will be explored in this tutorial.

Instructor:
Ernest Levine, SUNY-Albany

SESSION B1: SILICON MATERIALS AND PROCESSING
Chair: Janice L. Veteran
Monday Afternoon, April 1, 2002
Salon 10-12 (Marriott)

1:15 PM B1.1
SUPPRESSION OF PARASITIC BJT ACTION IN SINGLE POCKET THIN FILM DEEP SUB-MICRON SOI MOSFETS. Najeeb-ud-Din, Aatish Kumar, Mohan V. Dunga, V. Ramgopal Rao, J. Vasi, Dept of Electrical Engineering, Indian Institute of Technology, Bombay, INDIA.

A study of parasitic bipolar junction transistor effects in Single Pocket (SP) thin-film SOI n-MOSFETs is carried out. Characterization and simulation results show that parasitic BJT action is suppressed in SP-SOI MOSFETs when compared to the conventional (CON) SOI technologies. SP-SOI MOSFETs used in this study are fabricated by the standard CMOS process, except the V_{th} implant is done after the poly-silicon gate patterning. Pocket implant is done from the source side. Both the CON and SP-SOI MOSFETs are fabricated on the same wafer with channel lengths down to 100nm, and with different silicon film thicknesses, 35, 50 and 65 nm. The gate oxide thickness for all the MOSFETs is 3.9 nm. Gate-Induced-Drain-Leakage (GIDL) current technique has been used for characterization of parasitic BJT gain. GIDL current is independent of channel length and depends on the area of gate-drain overlap region and the electric field within it. At high drain biases, when impact generation starts to occur, the impact generated electrons flow towards the drain while the holes lead to charging of the body in SOI. In long channel devices these holes recombine before reaching the source, where as in short channel devices the hole current gets amplified by the factor β (BJT gain) depending upon the base width (channel length). This amplified current gets added to the drain current. By taking the ratio of currents in short channel to long channel device, we can estimate the value of β for the parasitic BJT. The experimentally evaluated value of β for the parasitic BJT in deep sub-micron SP-SOI devices is found to be an order of magnitude lower as compared to the CON SOI technologies. The suppression of parasitic BJT effect in SP-SOI devices is also analyzed from detailed 2-D simulations and attributed to lower peak electric field near the drain junction. Further insight is gained by detailed process and device simulatios using a BJT like structure with similar technology parameters as in SP-SOI. The results obtained from simulations excellently corroborate the experimental findings.

1:30 PM B1.2
MICROSTRUCTURAL EVOLUTION AND DEFECTS IN ULTRA-THIN SIMOX MATERIALS DURING ANNEALING. Jun Sik Jeoung, Rachel Evans, and Supapan Seraphin, The University of Arizona, Department of Materials Science and Engineering, Tucson, AZ.

Ultra-thin SIMOX processes are creating increased interest as a long-term solution for ULSI due to its advantages: low cost, better heat dissipation, and short channel effect over standard SIMOX. Ultra thin SIMOX materials were prepared by implantation of the oxygen ions into p-type (100) 8-inch Si wafers at an implantation energy of 65 keV and 100 keV with a dose range of 2.0 - 8.0×10^{17} O+/cm^2 using an Ibis 1000 high-current oxygen implanter. As-implanted wafers were subsequently annealed at 1100°C,1200°C, 1300°C and 1350°C each for 0 hrs and 4 hrs in an Ar (+1%O_2) atmosphere. Microstructural evolution, oxygen redistribution and crystalline quality of the Si films of SIMOX structure after post implantation thermal ramping and high temperature annealing were characterized using a Transmission Electron Microscope (TEM), Rutherford Backscattering Spectroscopy (RBS), and Auger Electron Spectroscopy (AES). The defect microstructures and their evolution upon high temperature annealing were investigated using XTEM and PTEM. The dislocation density in the Si-thin films of ultra thin SIMOX were measured using an optical microscope after a chemical etching. Results of the microstructure analysis shows that a dose range of 3.0 - 3.5 $\times10^{17}$ O+/cm^2 at an implantation energy of 100 keV produces a silicone island-free continuous buried oxide layer (BOX) after 1350°C and 4 hrs annealing. The thickness of silicon overlayer and BOX layer was about 160 nm and 75 nm respectively. The effects of implantation energy and dose on defect density in a fully annealed SIMOX are discussed.

1:45 PM B1.3
X-RAY REFLECTIVITY STUDY OF EXOTIC MATERIALS FOR ELECTRONIC APPLICATIONS. C.H. Russell, Bede Scientific Inc., Englewood, CO.

As device size decreases, new challenges arise regarding shrinking dimensions, creating the need for thin, high k dielectric materials, low k copper interconnects and other exotic materials. This in turn creates physical and characterization issues, which cannot be resolved with traditional metrology tools. Critical physical parameters such as density, interface roughness and thickness of a layer can be resolved with x-ray reflectivity. The quickest and a very reliable method of study regarding these materials is to base work on simulations using a very robust fitting program. This work incorporates a largely theoretical study of exotic materials of interest, including SiON, low k (silia-based films) and high k dielectrics (Ta_2O_5, ZrO_2, HfO_2, $SrTiO_3$), with a few selected experimental results.

2:00 PM B1.4
ABSORPTION SPECTROSCOPY ON COPPER TRACE IMPURITIES ON SILICON WAFERS. Andy Singh, Katharina Baur, Sean Brennan, Piero Pianetta, Stanford Synchrotron Radiation Laboratory, Stanford, CA; Takayuki Homma, Waseda University, Tokyo, JAPAN.

Trace metal contamination during wet cleaning processes on silicon wafer surfaces is a detrimental effect that impairs device performance and yield. Currently, total reflection x-ray fluorescence (TXRF) using synchrotron radiation is one of the most powerful techniques for trace impurity analysis on silicon wafer surfaces and has been used to better understand the deposition mechanism of Cu trace impurities on silicon wafers. Recent studies investigating silicon wafers immersed in copper contaminated ultra pure water solutions show a strong correlation between the deposited copper concentration and the amount of oxygen present in ultra pure water. In addition, TXRF has been combined with x-ray adsorption near edge spectroscopy (XANES) on pre-contaminated silicon samples that were dipped in UPW solutions with copper concentrations ranging from 2 to 200 ppb. Results showing the oxidation state of the deposited metal will be shown for both oxygenated and deoxygenated solutions. Finally, XANES experiments using a cell with a syringe water delivery system to observe samples directly beneath a water layer were also conducted. Higher concentrations of copper were used in the solutions to overcome degraded sensitivities due to the presence of the water layer, but the deposition processes could be monitored without environmental interference.

2:15 PM B1.5
PORE SIZE DISTRIBUTIONS IN LOW-k THIN FILMS BY X-RAY REFLECTIVITY AND SMALL ANGLE NEUTRON SCATTERING. Barry J. Bauer, Hae-Jeong Lee, Christopher Soles, Ronald C. Hedden, Da-Wei Liu, Wen-li Wu, NIST, Gaithersburg, MD; Jeffrey A. Lee, Jeff Wetzel, International Sematech, Austin, TX.

New methods have been developed to measure of pore size distributions in 1 mm films deposited on silicon wafers. X-ray reflectivity (XR) and small angle neutron scattering (SANS) have been carried out on samples surrounded by a controlled partial pressure of toluene vapor. As the vapor pressure increases, increasingly larger pores become filled with toluene liquid and XR is used to measure the amount adsorbed as a function of pressure. The Kelvin equation can be used to calculate the pore size distributions from the adsorption data. SANS is carried out in various mixtures of saturated toluene and toluene-d8 in air. The SANS signal goes through a minimum at a toluene/toluene-d8 ratio which is the "match point" at which time the wall material is matched by the toluene mixture. The wall density can

be calculated from this composition directly, without assuming any particular morphology type. The match point mixture is then used to fill the pores at various partial pressures and SANS of these samples provides an independent measure of pore size distribution.

3:00 PM B1.6
LINEWIDTH DEPENDENCE OF THE REVERSE BIAS JUNCTION LEAKAGE FOR CO-SILICIDED SOURCE/DRAIN JUNCTIONS. Anne Lauwers, Muriel de Potter, Richard Lindsay, Oxana Chamirian, Caroline Demeurisse, Christa Vrancken, Karen Maex, IMEC, Leuven, BELGIUM.

At the moment Co-silicide is the preferred self-aligned silicide for sub 0.25 um CMOS technologies. To be compatible with the continuously decreasing junction depth, the Co-silicide film thickness is being scaled down to lower the Si consumption at the expense of a higher sheet resistance. To optimally balance the trade-off between silicide sheet resistance and junction leakage, it is crucial to minimise the silicide/silicon interface roughness. The interface roughness can be improved by optimising the salicide pre-clean and the thermal budget of silicidation. In this work the reverse bias junction leakage is studied for Co-silicided 100 nm deep As and B source/drain junctions defined by shallow trench isolation. Dedicated test structures were designed to study the junction leakage as a function of the junction width and spacing. The width of the silicided junctions is varied between 0.15 and 3.0 um, the trench width is varied between 0.3 and 3.0 um. The Co-silicide is formed from a Co/Ti bilayer and resulting Co-silicide film thickness is 25 nm. Different salicide pre-clean conditions are compared. The temperature of the second RTP step of Co-silicidation is varied between 800 and 850°C. The junction leakage is studied as a function of the junction width for different trench widths. The leakage current dependence on salicide thermal budget is found to be different for large square diodes and diodes with narrow linewidth.

3:15 PM B1.7
A SELF-ALIGNED SILICIDE PROCESS UTILIZING ION IMPLANTS FOR REDUCED SILICON CONSUMPTION AND CONTROL OF THE SILICIDE FORMATION TEMPERATURE. G.M. Cohen, C. Cabral Jr., C. Lavoie, P.M. Solomon, K.W. Guarini, K.K. Chan, R.A. Roy, IBM T. J. Watson Research Center, Yorktown Heights, NY.

We propose a modified self-aligned silicide (salicide) process that uses Ge implantation and a silicon cap to reduce the silicon substrate consumption by 75% as compared with a conventional salicide process. We have used Ge implants to increase the cobalt disilicide formation temperature. This forces the cobalt to react primarily with a deposited silicon cap, thus minimizing consumption from the silicon substrate. We expect this process to be useful for making silicide on shallow junctions and thin SOI films, where silicon consumption is constrained. To experimentally determine the effect of Ge implantation on silicide formation, we monitored silicide phase evolution using in-situ synchrotron x-ray diffraction. We tested different Ge implant energies having projection ranges of 5.4, 10, 15 and 20 nm. The implant dose was 3E15 cm^{-2}, which roughly corresponds to a Ge content of 6%. The obtained Ge profile and dose were verified by SIMS. Since the implant amorphizes the top portion of the silicon film, we also investigated the role of the amorphization on the silicide formation by testing the silicide process with and without a 900°C RTA re-crystallization anneal. Following the implant, a Co layer capped by a TiN film was deposited on all samples. While annealing the samples at a heating ramp rate of 3°C/s from 100°C to 1000°C, we monitored the silicide phase using x-ray diffraction. The results were compared with a control sample, which was not implanted. Our main observation is that in Ge implanted wafers the formation temperature of the $CoSi_2$ phase is 122°C higher than the control sample. There is no significant change in the formation temperature of the CoSi phase. We also found that in amorphous silicon the formation of the $CoSi_2$ phase is not retarded. Yet, if the amorphous portion of the film is thin enough so it is consumed by the CoSi phase, then the resulting formation temperature of the $CoSi_2$ phase is similar to those of fully re-crystallized wafers, and is retarded by 122°C. Based on our study we propose a new salicide process having reduced silicon consumption: (1) Implant Ge and junction dopants. (2) Re-crystallize amorphized silicon and activate dopants by RTA. (3) Deposit Co and anneal to form CoSi. (4) Etch the excess metal, and deposit a blanket Si film. (5) Anneal to form the $CoSi_2$ phase, and etch the unreacted portion of the Si cap. The second anneal temperature should be lower than the formation temperature of $CoSi_2$ in the Ge implanted Si. This limits the silicide reaction to the top silicon cap, thus reducing the silicon consumption from the substrate by 75%.

3:30 PM B1.8
THICKNESS EFFECT ON NICKEL SILICIDE FORMATION AND THERMAL STABILITY FOR ULTRA SHALLOW JUNCTION CMOS. F.F. Zhao, Z.X. Shen, Physics Department, National University of Singapore, SINGAPORE; J.Z. Zheng, P.S. Lee, Chartered Semiconductor Manufacturing Limited, SINGAPORE; C.H. Pang, School of Materials Engineering, Nanyang Technological University, SINGAPORE.

NiSi is a promising candidate for CMOS device fabrication due to its low resistivity, low formation temperature and one-step annealing. Compared with $TiSi_2$, the resistivity of NiSi remains constant down to 0.1μm, while it consumes about 20% less silicon to form a silicide film of the same thickness when compared with $CoSi_2$. These two main advantages are of crucial importance for ultra shallow junction formation and sub-quarter micron CMOS fabrication. Nickel silicide samples are formed from sputtered Ni films on (100) Si substrates with thickness between 4nm and 30nm, and annealed between 300°C and 900°C for 30s by rapid thermal annealing. Electrical measurements by four-point-probe method show that the sheet resistance of thinner films start to increase at a lower temperature, indicating that thinner films are thermally less stable and agglomeration occurs more easily. This result is confirmed by the surface roughness data from AFM micrographs. Micro-Raman spectroscopy, which is sensitive to chemical composition and structure, is applied to identify phase formation, uniformity and orientation of nickel silicide films. For thinner films, the NiSi phase forms at lower temperature than the thicker ones. For samples of the same thickness, the NiSi films formed at higher temperatures have a higher degree of epitaxy with the Si substrate. Ion channelling experiments using Rutherford backscattering spectroscopy is also used to study the orientation of the NiSi films. The interface will be characterized by cross section TEM. And thermal stability of NiSi with different thickness will be invested.

3:45 PM B1.9
SUPPRESSION OF NiSi-TO-$NiSi_2$ TRANSITION USING VERY SHORT-TIME RTA SILICIDATION. D. Ma, D.Z. Chi, W.D. Wang, A.S.W. Wong and S.J. Chua, Institute of Materials Research and Engineering, Singapore, SINGAPORE.

Nickel monosilicide (NiSi) has been demonstrated to be a potential candidate for deep sub-0.1micron CMOS devices because of its linewidth-independent sheet resistance and low consumption of Si. However, the thermal stability of NiSi is a major concern for back-end process due to the transition of NiSi to the high-resistivity disilicide ($NiSi_2$) at an elevated temperature. In this study, we have investigated the effect of RTA silicidation duration on the NiSi-to-$NiSi_2$ transition during Ni-silicidation reaction of thin Ni (20 nm thick) film on (100)Si. The NiSi-$NiSi_2$ transition temperature was increased from 700 to >800°C with decreasing the annealing time from 60s to 1s. When the annealing temperature was fixed on 700°C, the critical time for NiSi-$NiSi_2$ transition was identified as 30-40s. Agglomeration of the silicide films was observed to depend on not only the film thickness but also the annealing time. The time-dependent agglomeration phenomenon can be explained in terms of the kinetics of grain growth. Agglomeration-induced disilicide nucleation was also characterised by HR-TEM. A model considering the kinetics of nucleation and faceted-growth of disilicide has been developed, by constructing a temperature-time transformation diagram, to elucidate the important roles of the film thickness and the RTA time in determining the NiSi-$NiSi_2$ transition temperature.

4:00 PM B1.10
ANALYSIS OF SILICIDE/DIFFUSION CONTACT RESISTANCE MAKING USE OF TRANSMISSION LINE STRUCTURES. Amal Akheyar, Infineon Technologies, Munich, GERMANY (affiliated to IMEC); Anne Lauwers, Richard Lindsay, Muriel de Potter, Georg Tempel and Karen Maex, IMEC, Leuven, BELGIUM.

The performance of MOS circuits depends strongly on transistor current drive. The drive current of the transistor is determined by the total device resistance, which consists of the channel resistance and the parasitic resistances associated with diffusions and contacts. As device dimensions shrink in each new technology generation, it is expected that the contact resistance between silicide and diffusion will ultimately dominate the total device resistance. For ohmic silicide/silicon contacts the contact resistivity is determined by the barrier height and the concentration of electrically active dopants at the silicide/silicon interface. The analysis of the contact resistance of a silicided junction is complicated by the fact that part of the junction is consumed during silicidation. As a result the dopant concentration at the silicide/silicon interface decreases as the silicide thickness is increased and the sheet resistance of the remaining part of the junction increases. In this work the contact resistance of Co-silicided As and B junctions is investigated to understand the influence of implant and anneal conditions, silicide thickness and silicidation temperature. The contact resistance between silicide and diffusion is studied making use of dedicated transmission line structures. The transmission line structures consist of alternating silicided and unsilicided diffusion segments, obtained by making use of

a salicide blocking mask. The specific contact resistivity and the sheet resistance of the remaining diffusion under the silicide are extracted from resistance measurements on transmission line structures with segments of varying length.

4:15 PM B1.11
CHARACTERISATION OF NOVEL RELAXED Ge AND Si_{1-x}/Ge_x PSEUDO BUFFER LAYERS GROWN BY CHEMICAL VAPOUR DEPOSITION. Ajey P. Jacob, T. Myrberg, O. Nur, M. Willander, Physical Electronics and Photonics, Physics Department, Microelectronics Centre (MC2), Chalmers University of Technology and Gothenburg University; C.J. Patel, Y. Campidelli, D. Bensahel, STMicroelectronics, Crolles, FRANCE; R.N. Kyutt, F. Ioffe Physical-Technical Institute of the Russian Academy of Science, St Petersburg, RUSSIA.

Relaxed SiGe and pure relaxed Ge pseudo substrates have attracted global interest recently. They are of great importance for providing suitable substrates for tensile strained Si as well as for integrating III-V compound semiconductors with Si technology. We have used the strain sensitive high resolution two dimensional reciprocal space mapping (2D-RSM) tool to characterize novel high quality fully relaxed SiGe and Ge buffer layers grown on Si 001 substrates by chemical vapour deposition. Both symmetric and asymmetric reflections were used to characterize these buffer layers. The effect of the Ge layer thickness and the post-growth temperature annealing on the over all quality regarding relaxation and threading dislocation density is investigated. In addition, the advantage of growing buffer layers on low temperature grown initial Si buffer layers is also studied. The 2D-RSMs are used to extract layer tilts relaxation factors, as well as to assess the crystalline quality. The results indicate high quality fully relaxed buffer layer with low threading dislocations. We have observed improved crystalline quality with increasing layer thickness up to an epilayer of 5 micrometer. On contrary to what have been shown previously, we found no improvement regarding the relaxation and threading dislocation density reduction by using the initial low temperature Si buffer layer. The overgrowth on these relaxed buffer layers is also monitored. These measurements were complemented by secondary ion mass spectrometry (SIMS). The SIMS results shows that at the Si/Ge interface a considerable inter-mixing have taken place. This inter-mixing was also observed in High resolution rocking curves as a tail on the high angle shoulder of the Ge peak in consistence with the SIMS results.

4:30 PM B1.12
PREVENTION OF BUCKLING DURING SiGe RELAXATION ON COMPLIANT SUBSTRATES. Haizhou Yin, Rui Huang, Princeton Univ, Center for Photonics and Optoelectronic Materials, Princeton, NJ; Karl D. Hobart, Naval Research Lab, Washington, DC; Zhigang Suo, Princeton Univ, Center for Photonics and Optoelectronic Materials, Princeton, NJ; Sean R. Shieh, Tom Duffy, Princeton Univ, Dept of Geoscience, Princeton, NJ; James C. Sturm, Princeton Univ, Center for Photonics and Optoelectronic Materials, Princeton, NJ.

There has been increasing interest in compliant substrates for integration of heterogeneous epitaxial materials. In our experiments, borophosphorosilicate glass (BPSG) on silicon is used as a compliant substrate to allow the relaxation of a strained silicon-germanium (SiGe) layer initially grown pseudomorphically on Si(100) substrate and then transferred to the BPSG by a bond and etch process[1]. Buckling of SiGe during relaxation has been observed[1] and analyzed[2]. Here, we first develop a fundamental quantitative model and understanding of the tradeoff between the desired lateral relaxation and the undesired vertical (buckling) process, and then demonstrate an experimental method to overcome the buckling issue. Large and thin islands cause slower lateral relaxation, which in turn enhances the buckling rate. Relaxation and buckling are measured by Raman spectroscopy and AFM, respectively. Experiments confirmed that thin SiGe layers buckle much faster. Furthermore, lowering the viscosity of the BPSG by a factor of five lowers the time required for both the lateral relaxation and buckling process, but the amount of buckling for a given amount of desired lateral relaxation does not change. Island size is a critical parameter, however, with buckling amplitude on 60um islands of $Si_{0.7}Ge_{0.3}$ being ten times as large as that of 40um islands. To overcome buckling, samples can be made temporarily thicker with an epitaxial cap, or buckling can be removed by long anneals at 850C after the initial buckling. The buckling amplitude decreases dramatically from more than 10nm to 0.5nm (RMS). We observe that small islands flatten faster than big islands and islands flatten faster at higher temperature. In addition, flattening process slows down over time, which is explained by the fact that the flattening process is driven by the residual strain in the islands. With high temperature anneals, it should be possible to make large relaxed SiGe islands with zero dislocation density. This work is supported by DARPA(N66001-00-1-8957) and ARO (DAA655-98-1-0270). 1. K.D. Hobart, F.J. Kub, M. Fatemi, M.E. Twigg, P.E. Thompson, T.S. Kuan and C.K. Inoki, J. Electron. Mater. 29, 897 (2000).
2. N. Sridhar, D.J. Srolovitz and Z. Suo, Appl. Phys. Lett. 78, 2482 (2001).

4:45 PM B1.13
THE ROLE OF EXCESS SILICON OR FREE VOLUME AT THE GROWING OXIDE INTERFACE. Ralph Jaccodine, Lehigh University, Sherman Fairchild Laboratory, Bethlehem, PA; S.J. Kilpatrick, IBM Microelectronics Division, Essex Junction, VT.

In the seminal work on Si oxidation by Deal and Grove [D&G],the early stage of oxidation <10nm does not follow an expected simple linear relationship entailing k[linear] reaction coefficient and time. This coefficient encompasses the conversion of crystalline Si into SiO_2 with an over 2X cell size. This gives rise to the model of a large excess of Si or alternatively the need for the creation of "free volume" at the interface. One of the earliest detailed models was done by W.Tiller et al. The existence of interstial [excess] Si was given particular cogency by the sucess in explaining oxidation related phenomena like OISF, OED/ORD. This paper discusses the issues that arise when an excess Si or SiO flux is used to adjust the D&G model to the observed growth. The authors use the experience of modelling the oxidation of Si-Ge alloys with the variation of over nine orders of oxygen partial pressure as a background to the discussion. A recent simulation of the thin oxide problem by M. Uwmatsu et al. invokes the effect of "excess Si" near the interface to adjust the D&G reaction coefficient and add an additional flux to the growing oxide. This paper will assess some of the critical points in their model as well as the relation of sub-bonded Si to the oxidation mechanism. A recent proposal by Pasquarello etal.opens new insight into the way the interface adjusts to the growing oxide which challenges our previous mechanistic notions.

SESSION B2: GATE DIELECTRICS AND DEVICES
Chairs: Jane P. Chang and Veena Misra
Tuesday Morning, April 2, 2002
Salon 10-12 (Marriott)

8:00 AM B2.1
PLASMA ENHANCED ATOMIC LAYER DEPOSITION OF ZrO_2 GATE DIELECTRIC. Jaehyoung Koo, Yangdo Kim, Taehan Doh, Jiwoong Han, Sungwoo Choi and Hyeongtag Jeon, Division of Materials Science and Engineering, Hanyang Univ., Seoul, KOREA; Yunsoo Kim, Thin Film Materials Laboratory, Advanced Materials Division, Korea Research Institute of Chemical Technology, Yuseong, Daejeon, KOREA; Shi-Woo Rhee, Laboratory for Advanced Materials Processing (LAMP), Department of Chemical Engineering, Pohang University of Science and Technology (POSTECH), Pohang, KOREA.

As the gate oxide thickness of metal-oxide-semiconductor (MOS) devices is scaled down to the sub-100nm, tunneling leakage current through gate dielectrics and reliability become serious problems. Thus, the high-k gate dielectrics become one of the solutions in providing increased capacitance and reduced leakage currents without significantly increasing the actual equivalent oxide thickness (EOT) of gate dielectrics. Among the high-k materials, zirconium oxide (ZrO_2) is considered to be one of the potential replacements of SiO_2 gate oxide due to its high dielectric constant and good thermal stability in contact with silicon. In this study, we investigated the ZrO_2 gate dielectric deposited by plasma enhanced atomic layer deposition (PEALD) method using three different zirconium sources. ZrO_2 were deposited on p-type Si (100) substrate using Zr t-butoxide, $Zr(tmhd)_2(O^tBu)_2$ and $Zr(Net_2)_4$ as Zr precursor and oxygen as reactant gas. Oxygen reactant gas was introduced both as in normal gas phase and plasma state. All samples were rapid thermal annealed at 800°C for 10 seconds in nitrogen ambient. Platinum (Pt) electrode layer with the thickness of about 1000Å was deposited by e-beam evaporator and patterned to form the gate electrodes. Post-metallization annealing was carried out in $H_2 + N_2$ ambient at 450°C for 30 minutes. The physical and chemical characteristics of ZrO_2 film were analyzed by cross-sectional transmission electron microscope (XTEM), atomic force microscope (AFM), Auger electron spectroscopy (AES) and X-ray photoelectron spectroscopy (XPS). The electrical properties and reliability characteristics including EOT, hysteresis, leakage current and capacitance were analyzed by I-V and C-V measurements.

8:15 AM B2.2
ATOMIC LAYER CHEMICAL VAPOR DEPOSITION OF HAFNIUM OXIDE USING ANHYDROUS HAFNIUM NITRATE PRECURSOR. J.F. Conley Jr., Y. Ono, D.J. Tweet, W. Zhuang, W. Gao, Sharp Labs of America, Camas, WA; S.K. Mohammed, R. Solanki, Oregon Graduate Institute, Department of Electrical and Computer Engineering, Beaverton, OR.

It is generally believed that scaling of SiO_2 will not be possible much

below 1.0 nm and that a high-k replacement material for SiO_2 will be necessary. Since an EOT of less than 1.0 nm will be needed and an interfacial layer of SiO_2 can easily form during deposition, atomic scale control of the interface is critical when depositing a high-k film. Although atomic layer chemical vapor deposition (ALCVD) inherently allows for monolayer control, researchers using $HfCl_4$ as a precursor have reported difficulty initiating deposition of HfO_2 on H-terminated Si. We find that the use of $Hf(NO_3)_4$ as a precursor allows for ALCVD of HfO_2 directly on H-terminated silicon without the need for an SiO_2 layer. HfO_2 films were characterized using spectroscopic ellipsometry (SE), x-ray diffraction (XRD) and reflectivity, and x-ray photoelectron spectroscopy (XPS). CV, IV, and TDDB measurements were made on capacitors and transistors with evaporated Pt electrodes. A single cycle deposition resulted in a uniform film covering the entire sample surface, demonstrating a clear advantage of $Hf(NO_3)_4$ over $HfCl_4$. XRD analysis indicated that as-deposited films were amorphous and uniform; film structure could be altered by a post deposition anneal. Thin films remained amorphous at anneals below 700°C. XPS analysis indicated that films are oxygen rich, contain silicate, and that residual NO_3 and NO_2 from the precursor could be eliminated by an anneal. HfO_2 films had lower leakage than SiO_2 of similar EOT but also lower BD strength. For a ~4.2nm HfO_2 film, k ~10 and capacitive equivalent thickness ~1.6nm (neglecting quantum effects) was obtained. The lower than expected dielectric constant is likely due to both the presence of an interfacial layer (such as silicate) and excess oxygen.

8:30 AM B2.3
HAFNIUM SILICATE FORMATION BY THE UV-OZONE OXIDATION OF HAFNIUM SILICIDE. G. Pant, P. Punchaipetch, M.A. Quevedo-Lopez, M. El Bouanani, R.M. Wallace and Bruce Gnade, Department of Materials Science, University of North Texas, Denton, TX.

As the scaling of silicon CMOS technology continues, high-κ gate dielectrics are required to provide increased gate capacitance while reducing gate leakage current. One candidate material that is receiving considerable attention is hafnium silicate[1]. We present results on the formation of hafnium silicate using UV-ozone oxidation of hafnium silicide. Hafnium silicide films were deposited on hydrogen terminated silicon wafers at room temperature using magnetron sputtering of $HfSi_2$. The hafnium silicide films were subsequently oxidized to hafnium silicate by exposing the wafers to UV-ozone. We find evidence for an oxidation rate consistent with metal enhanced oxidation of silicon with yttrium and lanthanum, as seen by Parsons et al.[2-3]. X-ray photoelectron spectroscopy, Rutherford backscattering spectrometry, and Fourier transform infrared spectroscopy were employed to examine the extent of oxidation. The electrical behavior of the as-deposited and annealed silicate films were determined with current-voltage (I-V) and capacitance-voltage (C-V) measurements. The effect of post-annealing on electrical properties using N_2, O_2, N_2O, NO, NH_3, and forming gas will also be presented. Comparison of the UV ozone oxidized hafnium silicate films will be made with those prepared by conventional reactive sputtering techniques. This work is supported partially by the US Army Soldier Systems Command (Contract #DAAD16-00-C-9273) and the Texas Advanced Technology Program. [1]G.D. Wilk, R.M. Wallace, and J.M. Anthony, J. Appl. Phys. 87 (2000) 484. [2]J.J. Chambers and G.N. Parsons, J. Appl. Phys. 90 (2001) 918. [3]J.P. Maria, D. Wicaksana, A.I. Kingon, B. Busch, H. Schulte, E. Garfunkel, T. Gustafsson, submitted.

8:45 AM B2.4
METALORGANIC CVD OF Ru AND RuO_2 THIN FILMS FOR GATE ELECTRODE APPLICATIONS. Filippos Papadatos, Spyros Skordas, Zubin Patel, Steve Consiglio, Eric Eisenbraun, UAlbany Institute for Materials, Albany, NY.

Ruthenium-based thin films are of interest for emerging CMOS gate electrode applications owing to their low resistivity, excellent thermal and chemical stability, and suitable work function characteristics. Ru and RuO_2 films were deposited on SiO_2 by chemical vapor deposition (CVD) and low power plasma enhanced CVD (PECVD) in a 200-mm wafer deposition cluster tool using a metal beta-diketonate precursor [Bis (2,2,6,6-tetramethyl-3,5-heptanedionato) (1,5-cyclooctadiene) ruthenium (II)]. Hydrogen and oxygen were employed as the reactive gases to deposit, respectively, Ru and RuO_2. The deposition temperature used ranged from 320°C to 480°C. The resulting film properties were analyzed using cross-sectional scanning electron microscopy (CS-SEM), four point resistance probe, x-ray photoelectron spectroscopy (XPS), and x-ray diffraction (XRD). Both Ru and RuO_2 films could be deposited with minimal carbon concentration (< 5 at.%). The purity of the films was reflected in the resistivity of the as deposited films, which was found to vary from 47 to 300 $\mu\Omega$·cm, depending on processing conditions. The films were subsequently annealed in both forming gas and oxygen ambients for one hour at 650°C. It was observed that the thermal CVD-deposited RuO_2 films were stable in oxidizing ambients, and annealing in a reducing ambient resulted in significant film densification and reduction of the film resistivities by approximately 70% (to as low as 43 $\mu\Omega$·cm). On the other hand, the ruthenium films were stable only after anneals in a reducing ambient. It was also observed that the plasma deposited films were not stable after anneals.

9:00 AM B2.5
EVALUATION OF CANDIDATE METALS FOR DUAL-METAL GATE CMOS WITH HfO_2 GATE DIELECTRIC. S.B. Samavedam, J.K. Schaeffer, D.C. Gilmer, V. Dhandapani, P.J. Tobin, J. Mogab, B-Y. Nguyen, R.S. Rai, Z-X. Jiang, R. Martin, M.V. Raymond, M. Zavala, L.B. La, J.A. Smith, Motorola Digital DNA Laboratories, Austin, TX; R.B. Gregory, Motorola Digital DNA Laboratories, Mesa, AZ; S. Dakshina-Murthy, AMD-Motorola Alliance, Austin, TX.

As the MOSFET gate lengths are scaled down to 50 nm or below, the expected increase in gate leakage will be countered by the use of a high dielectric constant (high-k) material. The series capacitance from polysilicon gate electrode depletion becomes a significant fraction of the actual capacitance from the gate dielectric as the dielectric thickness is scaled down to 10 Å equivalent oxide thickness (EOT) or below. Metal gates promise to solve this problem and address other issues like boron penetration and increased gate resistance that will have increased focus as the polysilicon gate electrode dimensions are scaled down further. Extensive simulations have shown that the optimal gate work-functions for the sub-50 nm channel lengths should be 0.2 eV below (above) the conduction (valence) band edge of silicon for n-MOSFETs (p-MOSFETs). In addition to the work-function requirements, the metal gate and the high-k gate dielectric should be mutually compatible and not inter-diffuse or react at the MOSFET thermal budget. This study summarizes the evaluations of TiN, TaSiN, WN, TaN, TaSi, Ir and IrO_2 as candidate metals for dual-metal gate CMOS using HfO_2 as the gate dielectric. The gate work-functions and fixed charge induced was determined by fabricating MOS capacitors with varying dielectric thicknesses. The metal-dielectric compatibility and thermal stability was studied by annealing the capacitors at different temperatures. The gate stacks were characterized using TEM, SIMS and X-ray diffraction. Of the metals evaluated, TaSiN and TaN show most promise as candidate gate electrodes for HfO_2 n-MOSFETs. Data from Ir and IrO_2 (promising PMOS candidates) gated HfO_2 capacitors will also be reported.

9:15 AM B2.6
HIGH QUALITY HfO_2 FILM AND ITS APPLICATIONS IN NOVEL POLY-Si DEVICES. K.L. Ng, N. Zhan, M.C. Poon, M. Chan, H. Wong, Hong Kong University of Science and Technology, Dept. of Electrical and Electronic Engineering, HONG KONG.

High quality high dielectric constant (high-k) HfO_2 films have been studied and applied in novel poly-Si memory devices. 50-500 Å HfO_2 film was deposited on silicon (c-Si) substrate. Poly-Si floating gate was then deposited and patterned. A second HfO_2 film was deposited on the floating gate, followed by the poly-Si control gate deposition and the formation of source and drain contacts. The process parameters including the HfO_2 and poly-Si formation processes, film thicknesses and annealing temperatures were studied to optimise the quality of the HfO_2 film, the HfO_2/c-Si and the HfO_2/poly-Si interfaces. The new low-voltage non-volatile memory cell has lower dielectric leakage current, better oxide/Si interfaces, and better memory reliability. Moreover, the cell has lower voltage drop in the two HfO_2 films and higher voltage drop in the Si substrate. Hence the memory has better gate control on the channel, better tunnelling and higher current drive.

10:00 AM *B2.7
ADVANCED MATERIALS AND PROCESSES FOR SYSTEM ON CHIP APPLICATIONS. B.E. White Jr., R. Muralidhar, and Michael Sadd, Motorola, Austin, TX.

The semiconductor industry has experienced exponential growth over the last three decades largely due to the ability of scientists and engineers to shrink the gatelength of the workhorse device of the industry: the silicon MOSFET. As we enter the fourth decade of growth, unprecedented technology development is needed to continue on this trend. In particular, the need to combine disparate technologies to create monolithic systems is driving technology development focused not only on system performance but also ease of integration. This presentation will focus on advanced processes and technologies needed for sub-50 nm system on chip applications. In the logic arena, discussion will focus on a comparison of technologies competing to replace bulk CMOS. This will include discussion of FDSOI MOSFET, double gated FDSOI MOSFET, and Schottky source/drain MOSFET. In the memory arena, discussion will focus on unconventional device structures which are easily integrated with advanced CMOS such as nanocrystalline Si based memory.

10:30 AM B2.8
PHYSICAL CHARACTERISATION OF HIGH-k GATE STACKS.
W. Vandervorst, H. Bender, T. Conard, H. Nohira, J. Petry, O. Richard, C. Zhao, B. Brijs, M. Caymax, S. De Gendt, IMEC; V. Cosnier, J. Chen, J. Kluth, W. Tsai, E. Cartier International Sematech c/o IMEC.

The need in future devices for gates with sub-nm EOT and/or extreme low leakage implies the use of high-k dielectrics with an interfacial silicon oxide thickness as close as possible to zero because the latter thickness will directly add to the overall EOT value of the dielectric stack. Formation of these layers is pursued with various deposition techniques such as ALCVD, MOCVD, ... In addition to the intrinsic properties of the high k stack, it is essential that the interfacial layer is controlled (minimized) as good as possible. The presence of an interfacial (SiO_x) layer depends on several factors, e.g. the silicon surface preparation prior to the high-k deposition, the high-k deposition process and the post-deposition air exposure or thermal anneal. Understanding the mechanism of formation and the control of the interfacial oxide are therefore key-issues for the successful implementation of high-k dielectrics in future devices. Moreover composition, crystallization behavior, stability upon anneal and poly-deposition are all aspects which need to be looked at very carefully in order to assess the intrinsic properties of the high k stacks. The successful understanding of the layer deposition and growth mechanism (layer by layer growth, islanding, phase separation, oxygen diffusion, ..) relies on the ability to probe these layers very precisely. As no technique has the ability to fully characterize the layers with respect to e.g. layer thickness and composition, surface and interface roughness, crystallinity, contaminants and presence of an interfacial layer, a combined effort with complementary analysis techniques is required. This paper discusses the results of such an effort as applied to the characterization of high-k layer stacks based on Zr, Al and ZrAl-mixed oxides. The physical analysis is done by ellipsometry, X-ray photo-electron spectroscopy (XPS), X-ray fluorescence (XRF) and reflectivity (XRR), inductively coupled plasma optical emission spectroscopy (ICP-OES), FT-IR, time-of-flight SIMS (TOF-SIMS), Rutherford backscattering (RBS) and Elastic recoil detection, low energy ion scattering (LEIS) and transmission electron microscopy (TEM). Procedures have been developed to rapidly screen growth behavior, silicide formation, phase separation, crystallization behavior, ...

10:45 AM B2.9
DEGRADATION AND SILC EFFECTS OF RPECVD SUB-2.0NM OXIDE/NITRIDE (O/N) AND OXYNITRIDE DIELECTRICS UNDER CONSTANT CURRENT STRESS (CCS).
Yi-Mu Lee, Joon Goo Hong, Gerald Lucovsky, North Carolina State Univ, Dept of Electrical and Computer Engineering, Materials Science and Engineering, Physics, Raleigh, NC; Yider Wu, Advanced Micro Devices Inc., Technology Development Group, Sunnyvale, CA.

Constant current stress (CCS) is conducted to investigate the Stress-Induced Leakage Current (SILC) effects to clarify the influence of boron penetration and nitrogen incorporation on the breakdown of sub-2.0 nm Oxide/Nitride (O/N) and oxynitride dielectrics prepared by remote plasma enhanced CVD (RPECVD). The distortion and degradation of MOSFET characteristics which related to soft breakdown (SBD) and hard breakdown (HBD) are studied. Analog-mode gate noise and post-breakdown voltages are monitored for both gate and substrate injection during CCS up to 10k sec in order to detect SBD and HBD. The monitored gate voltages are gradually decreased during SBD, and a continuous increase in SILC at low gate voltages is shown between each stress interval. HBD was observed to result in resistive I_g-V_g characteristics and device failure, and can be detected by a significant drop in gate voltages during CCS. Compared to SILC in the thermal oxide, the reduced SILC effect of O/N and oxynitride dielectrics is observed, which is due to the suppression of positive trap generation by nitrogen incorporation at the Si/SiO_2 interface. Band bending of gate dielectrics due to charged traps is found to influence the SILC effect and degradation mechanisms. Furthermore, we also demonstrate that stacked O/N and oxynitride dielectrics show less degradation in MOSFET electrical performance and trap-assisted SILC effects because of the reduction of boron diffusion and the improved Si/SiO_2 interface and gate-to-drain overlap region.

11:00 AM B2.10
SILICON NITRIDE THIN FILM DEPOSITION FOR GATE DIELECTRICS USING SINGLE-WAFER HOT-WALL RAPID THERMAL CVD.
Yoshihide Senzaki, Yakov Brichko, Carl Barelli, Robert Herring, ASML Thermal Division, Scotts Valley, CA.

Rapid thermal processing (RTP) is an emerging technology in integrated circuit fabrication, and could be an alternative to batch furnace processing as future wafer production moves to 300mm diameter size. RTP requires shorter process time and can achieve better film uniformity than the batch process. We have recently developed single-wafer furnace RTP modules for both thermal oxidation and low pressure chemical vapor deposition (LPCVD) of silicon nitride. Uniform oxide films of sub-20Å can be grown by thermal oxidation and NO nitridation. The RTCVD system also provides consistent film deposition performance for silicon nitride thin films in terms of thickness and uniformity. This paper further extends the application of the hot-wall single-wafer RTCVD system to gate dielectric applicatons. The system provides silicon nitride films of equivalent oxide thickness below 20Å. The film deposition processes, the post-deposition anneal processes, and the electrical characterization of the gate dielectrics will be discussed.

11:15 AM B2.11
HIGH PURITY SILICON AMIDO PRECURSORS FOR LOW TEMPERATURE CVD OF GATE DIELECTRICS.
Alexander S. Borovik, Chongying Xu, Bryan C. Hendrix, Jeffrey F. Roeder and Thomas H. Baum, ATMI, Inc., Danbury, CT.

Early transition metal silicates, such as those containing zirconium and hafnium, are of great interest for use as the next generation gate dielectrics. To minimize the formation of an interfacial silicon oxide layer, a low temperature CVD process is required. Generally, metal amides are promising low temperature CVD precursors. However, until recently, their silicon analogues were not readily available in high purity, a fundamental requirement for their use in microelectronic applications. We have developed direct synthetic methods for the production of high purity $Si[N(CH_3)_2]_4$, $Si(NEtMe)_4$, $HSi(NEtMe)_3$ and $HSi(NEt_2)_3$ in high yield. These compounds were fully characterized by NMR, FT-IR, ICP-MS and IC-chlorine analysis. In this paper, we report the synthesis, characterization of the new precursors and their use for the low temperature CVD of metal silicates, gate dielectrics.

11:30 AM B2.12
METROLOGY STUDY OF SUB 20 Å OXYNITRIDE BY CORONA-OXIDE-SILICON (COS) AND CONVENTIONAL C-V APPROACHES.
Pui Yee Hung[a], George A. Brown[a], and Xiafang Zhang[b], [a]International SEMATECH, Inc, MetrologyYield Management Tools, Austin, TX; [b]KLA-Tencor Corporation, Film and Surface Technology Division, San Jose, CA.

This work aims to develop a non-contact corona oxide-silicon (COS) measurement strategy for the monitoring of sub 20 Å oxynitride gate dielectrics. The oxynitride used in this study is composed of two batches of In-Situ Steam Generated oxide (ISSG) oxide (20/16 Å) which are exposed to Remote Plasma Nitridation (RPN) for various time durations. First, the nitrogen concentration and profile of the samples are established by SIMS and nuclear reaction analysis. Then, the COS measurement using Quantox^{TM} was carried out on companion wafers, extracting the following five electrical parameters: interface trap density (D_{it}), flatband voltage (Vfb), total charge, effective charge and equivalent oxide thickness (EOT). Both the pre-anneal D_{it} and total charge are promising parameters because of their strong correlation with the nitrogen content. However, the Vfb, effective charge, and EOT measurements appear to be affected by the ambient environment or the leakage characteristics of the oxynitride. In addition, the integrity of the oxynitride is verified by measuring the COS tunneling voltage, leakage current and oxide resistivity. A comparison of the C-V/COS measurements of EOT, Vfb and current density is included; however, no simple linear relationship exists between these parameters.

SESSION B3: HIGH-k DIELECTRICS

Chairs: Roy G. Gordon and Veena Misra
Tuesday Afternoon, April 2, 2002
Salon 10-12 (Marriott)

1:30 PM *B3.1
La AND Zr-BASED ALTERNATIVE GATE DIELECTRICS: A STRUCTURAL AND ELECTRICAL INVESTIGATION.
J-P. Maria, D. Wicaksana, C. Hoffman, A.I. Kingon, North Carolina State University, Department of Materials Science and Engineering, Raleigh, NC; H. Schulte, E. Garfunkel, Rutgers University, Department of Chemistry, Piscataway, NJ; S. Stemmer, Rice University, Department of Mechanical Engineering and Materials Science, Houston, TX.

Alternative high-permittivity gate dielectrics based on lanthanum oxide and zirconium oxide for sub-1.0 nm equivalent-oxide-thickness transisitors have been investigated. Lanthanum and zirconium-based dielectrics are of interest given their large electrical polarizability and the predicted stability in contact with SiO_2 at high temperatures. This investigation is focused upon structural and electrical characterization of these dielectrics, especially in the context of post-deposition high-temperature heat treatments. X-ray diffraction

has been used to investigate crystallization behavior of metal silicates and alloys. A model describing the crystallization behavior of La and Zr-containing silicates based on sub-liquidus immiscibility will be presented. This model will be used in conjunction with a phase diagram survey of metal oxide-SiO_2 systems to categorize potential gate dielectrics for crystallization behavior. Electrical and structural characterizations have been used to optimize a dielectric and a process able to withstand temperature excursions in excess of 1000°C. In general, appropriate combinations of temperature and oxygen partial pressure can be found which minimize unwanted interface reactions, and low permittivity interface layer formation during high temperature exposure. Models for reactions between these materials will be presented in the context of oxygen rich and oxygen poor atmospheres. Specifically, a new model will be presented which attempts to describe the decomposition of oxides in contact with silicon. Finally, data will be shown comparing materials prepared with and without *in situ* deposited Ta metal gates. These results demonstrate the sensitivity of ultra-thin capacitive layers to atmospheric exposure.

2:00 PM B3.2
THERMODYNAMIC STABILITY OF HIGH-k DIELECTRIC METAL OXIDES ZrO_2 AND HfO_2 IN CONTACT WITH Si AND SiO_2. Maciej Gutowskia, John E. Jaffea, Pacific Northwest National Laboratory; Chun-Li Liu, Matt Stoker, Rama I. Hegde, Raghaw S. Rai, and Philip J. Tobin, Motorola Inc.

We present theoretical and experimental results regarding the thermodynamic stability of the high-k dielectrics MO_2 (M = Zr and Hf) in contact with Si and SiO_2. The HfO_2/Si interface is found to be stable with respect to formation of silicides whereas the ZrO_2/Si interface is not. The MO_2/SiO_2 interface is marginally unstable with respect to formation of silicates. Cross-sectional transmission electron micrographs expose formation of nodules, identified as silicides, across the polysilicon/ZrO_2/Si interfaces but not for the interfaces with HfO_2. For both ZrO_2 and HfO_2, the X-ray photoemission spectra illustrate formation of silicate-like compounds in the MO_2/SiO_2 interface.

2:15 PM B3.3
EFFECT OF TECHNOLOGY SCALING ON MOS TRANSISTORS WITH HIGH-k GATE DIELECTRICS. Nihar R. Mohapatra, Madhav P. Desai, V. Ramgopal Rao, Indian Institute of Technology Bombay, Department of Electrical Engineering, Mumbai, INDIA.

High-K materials like Al_2O_3(K 10), ZrO_2/HfO_2(K 25) and TiO_2(K 60) have received much attention recently as alternative gate dielectrics for CMOS applications. A few papers have been published recently on the effect of fringing capacitances in these high-K gate dielectric MOS transistors due to their higher physical dielectric thickness. However, no work has been done to study the effect of technology scaling parameters on the fringing field effects. In this work, we have studied the effect of gate overlap length, spacer dielectric material and other technology parameters on the device and circuit performance of aggressively scaled CMOS transistors with high-K gate dielectrics by extensive two dimensional device simulations. In high-K gate dielectric transistors, the ratio of physical thickness to channel length increases as the gate dielectric constant is increased. Thus the 2-D effects become dominant leading to poor short channel performance. For K_{gate} greater than K_{Si}, we observe a substantial coupling between source and drain regions through the gate dielectric rather than through silicon. Our results show that for an increase in K_{gate} from 3.9 to 60, I_{on}/I_{off} ratio decreases by a factor of 9 for V_d=0.5V and by a factor of 17 for V_d=1V. Also, DIBL increases by a factor 2.5 when K_{gate} is increased from 3.9 to 60. In future aggressively scaled MOS technologies the control of overlap region is going to be a major challenge. Since much of the coupling between source-drain occurs through the gate dielectric, it is observed that overlap length is an important parameter for optimizing DC performance in short channel MOS transistors. We provide extensive 2-D device simulation results to prove this point. We have also studied the effect of spacer dielectric material and channel length on the performance of high-K gate dielectric MOS transistors.

3:00 PM B3.4
Si(100) SURFACE CLEANING USING Sr AND SrO. Yi Wei, Xiaoming Hu, D.C. Jordan, Brad Craigo, Ravi Droopad, Jimmy Z. Yu, Alex Demkov, John L. Edwards Jr., W.J. Ooms, Physical Science Research Laboratory, Motorola Labs, Motorola Inc., Tempe, AZ.

A method for removing SiO_2 and producing an ordered Si(100) surface using Sr or SrO has been developed. In this technique, a few monolayers of Sr or SrO are deposited onto the as received Si(100) wafer in a ultrahigh vacuum (UHV) molecular beam epitaxy (MBE) system. The substrate is then heated to ~800°C for about 5 minutes, the SiO_2 is removed to leave behind a Sr or SrO terminated ordered Si(100) surface with a mostly (2X1) reconstruction. This Sr or SrO terminated Si(100) surface is well suited for the growth of crystalline high k dielectric $SrTiO_3$[1]. To understand the mechanism of removing SiO_2 from Si(100) using Sr or SrO, we have run temperature programmed desorption (TPD) measurements on SrO covered Si(100) substrates. The species we observed coming off the surface during the temperature cycle was mainly SiO and O, no significant amount of Sr containing species was observed. We conclude that the SiO_2 removal is due to the catalyst reaction SiO_2 + Sr (or SrO) →SiO (g) + O+ + e- + Sr (or SrO). The reaction SiO_2 + Si → 2SiO (g) at the SiO_2/Si interface is limited and the pit formation is suppressed. The main roles that Sr or SrO play during the oxide removal process are catalysts promoting SiO formation and passivating the newly exposed Si surface, preventing further etching and the formation of pits in the substrate. We have shown the Sr or SrO coverage is important to achieve a smooth, pit-free Si(100) surface. [1] Z. Yu, J. Ramdani, J.A. Curless, J.M. Finder, C.D. Overgaard, R. Droopad, K.W. Eisenbeiser, J.A. Hallmark, and W.J. Ooms, J.R. Conner and V.S. Kaushik "Epitaxial perovskite thin films grown on silicon by MBE", J. Vac. Sci. Technol. B18, 1653 (2000).

3:15 PM B3.5
Sr/Si PHASES FROM Sr AND SrO DE-OXIDATION AND THE Sr 3D5/2 BINDING ENERGY SHIFTS STUDIED BY LEED AND XPS. Xiaoming Hu, Yi Wei, B. Craigo, J.L. Edwards Jr., H. Li, D. Jordan, R. Droopad, K. Moore, and W.J. Ooms, Physical Science Research Laboratories, Motorola Labs, Tempe, AZ.

The Sr/Si templates for $SrTiO_3$ growth prepared by Sr and SrO de-oxidation processes of silicon with native oxides have been studied by LEED and XPS. The Sr or SrO de-oxidation processes involve first depositing a small amount (2-3ML) of Sr or SrO on silicon, and then anneal the sample at elevated temperatures in the range of 700-800°C. Different surface phases depending on the recipes, namely (3x2), (2x1) and (5x1) have been identified by LEED and found to be related to the Sr coverage by XPS. Shifts in binding energies of the Sr 3d5/2 photoemission peak have been observed by comparing XPS spectra from the Sr/SrO de-oxidation with those from 2ML and 6ML SrO deposited on Si. A shift of about -0.9eV in binding energy (compared to metallic Sr at 134.3eV) for the 2ML SrO/Si sample indicates a reduction of surface work function possibly due to surface polarization of the SrO layer. This implies that the SrO de-oxidation mechanism is likely through the surface work function reduction promoted SiO_2 de-composition process as opposed to the normal SiO_2 thermal de-oxidation which required higher temperature and/or longer time. The 6ML SrO/Si sample showed a binding energy shift of about -0.4eV less than that of the 2ML SrO/Si leading to the conclusion that there exists an optimum SrO thickness (a few ML) which gives the maximum surface work function change. Negative binding energy shifts for Si 2p have also been observed in the XPS indicating actually larger surface work function reductions, however, due to the complexity of surface charging effects, absolute working function reductions for each sample can not be determined during these experiments.

3:30 PM B3.6
MECHANISM OF THE SUPPRESSION OF Zr SILICIDE FORMATION IN POLY-Si/ZrON/ZrSiON/Si STRUCTURE. Masato Koyama, Akira Nishiyama, Advanced LSI Technology Laboratory, R&D Center, Toshiba Corporation, Yokohama, JAPAN; Chie Hongo, Mitsuo Koike, Yuichi Kamimuta, Masamichi Suzuki, Environmental Engineering and Analysis Center, R&D Center, Toshiba Corporation, Yokohama, JAPAN; Kyoichi Suguro, Process & Manufacturing Engineering Center, Semiconductor Company, Toshiba Corporation, Yokohama, JAPAN.

ZrO_2 is a promising material for high-k gate dielectrics for sub-100nm CMOS LSIs. However, zirconium silicide ($ZrSi_x$) formation has been widely reported in the poly-Si/ZrO_2/SiO_2/Si system, even in the case of 850°C annealing. In order to avoid this problem, we have prepared ultra-thin ZrON/ZrSiON stacked gate insulator by low temperature oxidation of ZrN and successfully demonstrated that the poly-Si/ZrON/ZrSiON/Si stack has superior thermal stability even in the case of 1000°C annealing [1]. In this study, the mechanism of the suppression of the $ZrSi_x$ formation in the poly-Si/ZrON/ZrSiON/Si structure is discussed in detail. First, we speculated that the nitrogen atom incorporated in ZrON was outdiffused during the annealing to form interfacial SiN at poly-Si/ZrON interface, stabilizing the interface. In order to check this model, we performed high temperature annealing before the poly-Si deposition and removed nitrogen from ZrON film. The absence of the silicide formation in this experiment revealed that the SiN formation at the poly-Si/ZrON interface due to the nitrogen in ZrON is not responsible for the suppression of the $ZrSi_x$ formation. On the other hand, it was predicted that the gaseous Si-O formation and diffusion at the ZrO_2/SiO_2/Si stack was essential for the silicide reaction [2]. In order to confirm this model, we have investigated the thermal stability of poly-Si/ZrO_2/Si stack by inserting SiO_2 or Si_3N_4 into ZrO_2/Si interface. It was clearly

observed that the $ZrSi_x$ formation was substantially restrained by inserting $Si_3 N_4$ instead of SiO_2. This result means that the formation and diffusion of gaseous Si-O at the stack is the dominant process promoting the reaction. Based on these experimental results, we think the thermal stability of the poly-Si/ZrON/ZrSiON/Si stack is mainly due to the nitrogen incorporation into the ZrSiON interfacial layer, in which Si-O creation as well as its diffusion is effectively suppressed. [1] M. Koyama et al., to be published in IEDM2001. [2] T.S. Jeon, J.M. White and D.L. Kwong, Appl. Phys. Lett. vol. 78, 2001, p. 368.

3:45 PM B3.7
STRUCTURE AND STABILITY OF ALTERNATIVE HIGH-k DIELECTRIC LAYERS ON SILICON. S. Stemmer, Z. Chen, Rice University, Houston, TX; D. Niu, R. Ashcraft, G.N. Parsons, D. Wicaksana, J.-P. Maria, A.I. Kingon, North Carolina State Univ, Raleigh, NC.

We use electron energy-loss spectroscopy (EELS) in scanning transmission electron microscopy with a sub-0.2 nm probe and atomic resolution transmission electron microscopy to investigate the structure and stability of Y_2O_3 grown by remote plasma chemical vapor deposition (CVD) and of ZrO_2 layers grown by reactive evaporation in a molecular epitaxy system (MBE). We investigated CVD Y_2O_3 films as a function of film thickness and pre-treatment of the silicon surfaces after post-deposition anneals. We show that thin films on clean silicon form a silicate film with a thin interfacial oxide, whereas a nitrogen plasma pre-treated Si surfaces reduces the amount of silicon away from the interface and Y_2O_3 is found as the top-most layer in a film of the same thickness (7 nm). We also show that the amount of silicon in the films determines the crystallization behavior in post-deposition anneals at 900°C and the formation of a thin interfacial oxide is difficult to avoid under atmospheric, non-capped annealing conditions. MBE-ZrO_2/Si structures were investigated before and after rapid thermal annealing (RTA) treatments at 1000°C under different oxygen partial pressures. We identified a critical partial pressure of approximately 10^{-5} torr that can preserve a thin (1 nm) interfacial silicon oxide layer for high equivalent oxide thicknesses. At higher oxygen partial pressures (about 10^{-4} torr) the interfacial oxide thickness increases through oxygen diffusion through the ZrO_2 layer and silicon consumption at the interface. At lower oxygen partial pressures (about 10^{-7} torr), silicide formation at the interface is observed. ZrO_2 films annealed at the optimal partial pressure for a thin interfacial oxide were found to crystallize and contain no silicon, whereas silicon diffusion and partial amorphization takes place at higher partial pressures. The results show the relationship between crystallization and silicon diffusion as a function of annealing atmosphere, and also show that oxide crystallization is important in determining the overall phase formation behavior. We will also discuss the application of EELS fine-structure analysis to provide an additional measure of interface composition in these very thin layers.

4:00 PM B3.8
ATOMIC LAYER DEPOSITION OF ZIRCONIUM DIOXIDE THIN FILMS USING NEW ALKOXIDE PRECURSORS. T.J. Leedham, A.C. Jones, P.A. Williams, H.O. Davies, Inorgtech Ltd, Mildenhall, UNITED KINGDOM; M. Ritala, R. Matero, M. Leskala, Department of Chemistry, University of Helsinki, FINLAND.

Zirconium dioxide has a high permiittivity and is stable in contact with silicon, making it a prime candidate as the gate dielectric in next generation MOSFET devices. Atomic layer deposition (ALD) allows the deposition of conformal films at low substrate temperatures with control of layer thickness to the monolayer level. Zirconium tetrachloride and zirconium tetraiodide have been used as precursors but halide contamination is a potential problem. Zr alkoxides may offer process advantages and Zr tetra-tert-butoxide has been investigated for the ALD of zirconium dioxide. However this mononuclear precursor contains a four coordinate unsaturated Zr(IV) centre making it moisture sensitive and susceptible to decomposition during storage and use. The use of donor functionalised alkoxide ligands containing more than one oxygen or nitrogen donor group (e.g. dimethylaminoethoxide) leads to more fully saturated and less reactive Zr-alkoxide complexes. Here we report the ALD of zirconium dioxide using a number of donor functionalised alkoxide precursors. Results are compared to conventional sources and the implications are discussed for the future design of ZrO_2 ALD precursors.

SESSION B4: POSTER SESSION
DIELECTRIC CHARACTERIZATION
Tuesday Evening, April 2, 2002
8:00 PM
Salon 1-7 (Marriott)

B4.1
CHARACTERIZATION OF Si NANOCRYSTALS ON DIELECTRIC SURFACES FOR MEMORY APPLICATIONS. Ran Liu, X.D. Wang, Q. Xie, Motorola SPS, Advanced Process Development & External Research Laboratory, Mesa, AZ; R. Rao, and B.E. White, Motorola SPS, Advanced Process Development & External Research Laboratory, Austin, TX.

One of the promising application of nanocrystalline Si materials is the nonvolatile memory using Si nanoparticles grown on dielectrics as a floating gate. The characterization of the size and density, two crucial parameters affecting the device performance, of the nanocrystals presents great challenges even to the powerful structural characterization techniques such as atomic force microscopy (AFM) and transmission electron microscopy (TEM). Since the electron and phonon structures strongly depend on the size of nanocrystal Si, optical spectroscopy can be used as nondestructive characterization and metrology tools. In an effort to correlate the optical properties with the nanocrystal structure and density, we have performed UV-Raman spectroscopy and spectroscopic ellipsometry in conjunction with AFM and TEM on thin layers of Si nanocrystals of different size and densities on dielectrics. The extremely small optical penetration depth strongly suppresses the UV-Raman signals from the Si substrate and thus allows characterization of the thin nanocrystal Si layer by correlating the phonon frequency shift to the particle size. Ellipsometry spectra have been found to be sensitive to both the size and the density of Si particles. The energy gap obtained from ellipsometry seems to increase with decreasing Si particle size, possibly due to quantum confinement effect.

B4.2
HIGH-k GATE DIELECTRIC PREPARED BY LOW TEMPERATURE WET OXIDATION OF ULTRATHIN METAL NITRIDE. Sangmoo Choi, Sanghun Jeon, and Hyunsang Hwang, Kwangju Institute of Science and Technology, Dept of Material Science and Engineering, Buk-ku, Kwangju, KOREA.

Although Ta_2O_5 has been investigated in terms of MOS gate dielectric applications, it is difficult to obtain an equivalent oxide thickness of less than 2 nm with acceptable leakage current. Since an approximately 1 nm-thick interfacial SiO_2 oxide layer is necessary to minimize interface state density and the intermixing of silicon and Ta_2O_5, the dielectric constant of Ta_2O_5 is not sufficient to obtain an equivalent dielectric thickness of less than 2 nm. Recently, we have reported an excellent electrical characteristics of TaO_xN_y prepared by nitridation and wet reoxidation of Ta_2O_5 [1]. In this presentation, we report on high-k gate dielectrics prepared by low temperature wet oxidation of TaN layers. TaN layer was directly deposited on bare silicon using RF magnetron sputtering. Wet oxidation of TaN was performed at 400°C. After the deposition of a 150nm-thick layer of Pt, MOS devices with a gate area of 9×10^{-6} cm^2 were defined. Compared with TaO_xN_y prepared by NH_3 nitridation of Ta_2O_5, TaO_xN_y prepared by wet oxidation of TaN shows excellent electrical characteristics such as equivalent oxide thickness as thin as 13Å, leakage current density of less than 100μA/cm^2 at V_{FB} ?1.5V, and acceptable interface state density which was confirmed by C-V and conductance method. The improvements of electrical characteristics can be explained by the reduction of interfacial oxide layer due to the direct deposition of metal nitride. [1] H. Jung, K. Im, D. Yang, H. Hwang, Appl. Phys. Lett., 76, 3630 (2000).

B4.3
ELECTRICAL AND MATERIALS PROPERTIES OF ALD-GROWN ZrO_2 AND HfO_2 GATE DIELECTRICS. Hyoungsub Kim, Paul C. McIntyre, Stanford Univ, Dept of Materials Science and Engineering, Stanford, CA; Krishna Saraswat, Stanford Univ, Dept of Electrical Engineering, Stanford, CA.

As MOS transistor size decreases and higher speeds are required, the gate oxide must be aggressively decreased down to 1.5nm for a 0.1μm channel length transistor. However, as the thickness of SiO_2 decreases, the leakage current across the dielectric increases enormously through direct tunneling. At present, in order to reduce the leakage current, high-k materials, including ZrO_2 and HfO_2 have been widely investigated because they offer the opportunity to scale device dimensions further, while retaining sufficient physical thickness of the dielectric to avoid direct tunneling. Among many possible deposition techniques, ALD (Atomic Layer Deposition) is drawing a lot of attention because it can produce high quality films with precise thickness control and near-perfect conformality owing to its adsorption-controlled deposition mechanism. For these experiment, we used a cold wall ALD system with $ZrCl_4/H_2O$ and $HfCl_4/H_2O$ precursors for each processes. The deposition was carried out at 250 - 300°C on a thermally-grown thin SiO_2 underlayer. Platinum gate electrodes were deposited through a shadow mask by e-beam evaporation for electrical characterization of the gate stacks. In this presentation, we will compare the electrical and microstructural

properties of ALD-grown ZrO_2 and HfO_2, using C-V, I-V, and HR-TEM. The microstructure and leakage current properties of ZrO_2 and HfO_2 will be compared before and after thermal annealing. In addition, electrical and material properties as a function of thickness will be discussed. As a possible candidate for high-k gate dielectric applications, data on ZrO_2-HfO_2 nanolaminate structures will be also presented.

B4.4
AB-INITIO MODELING OF BORON DIFFUSION IN POLY-CRYSTALLINE HfO_2 FILMS. Chun-Li Liu, Advanced Process Development and External Research Lab., Motorola, Inc, Mesa, AZ.

We present ab-initio modeling results including formation, migration, and activation energies for B diffusion through bulk and grain boundaries in polycrystalline HfO_2 films. Modeling results clearly indicate that B can penetrate through a 40 Å HfO_2 film via grain boundary diffusion, but not by bulk diffusion. SIMS analysis of B concentration profiles for polysilicon/HfO_2/Si gate stacks after different anneals showed double B peaks at the interfaces and thus confirmed the modeling prediction.

B4.5
ENHANCED OXYGEN INCORPORATION IN HIGH-k DIELECTRIC MATERIALS DEPOSITED BY AN ULTRAVIOLET-ASSISTED GROWTH TECHNIQUE. J.M. Howard, V. Craciun, C. Essary, N.D. Bassim, and R.K. Singh, Univ of Florida, Gainesville, FL.

As the search for an alternative gate dielectric for the currently used SiO_2 continues, numerous high-k materials have been investigated as possible candidates. Among them, zirconium dioxide, hafnium dioxide and barium strontium titanate have shown great promise. In a comparative study, nanometer thick samples were grown by both conventional pulsed laser deposition (PLD) and by an ultraviolet-assisted pulsed laser deposition (UVPLD) technique. In the UVPLD technique, low pressure Hg lamps were added to the PLD chamber. With the addition of the 185 nm UV radiation sources, molecular oxygen is broken down into highly reactive ozone and atomic oxygen which can incorporate more readily into the growing films. The effects of this enhanced oxygenation process resulted in higher crystalline quality, more stoichiometric films due to lower oxygen vacancies. A variety of characterization techniques were used to investigate the effects of the ultraviolet radiation. The structural properties were analyzed by transmission electron microscopy, x-ray diffraction, and x-ray reflectivity. Chemical analysis was performed via x-ray photoelectron spectroscopy and Fourier transform infrared spectroscopy. Finally, electrical characterization in the form of capacitance-voltage and current-voltage measurements was performed. In each of the cases, samples grown with and without UV illumination were compared and the oxygen content was analyzed. The main benefit of this UV-assisted process is the ability to grow higher quality films, or otherwise equivalent films but at lower processing temperatures.

B4.6
PROPERTIES OF HAFNIUM OXIDE UPON DEPOSITION METHOD. Suheun Nam, Seok Woo Nam, Jung Ho Yoo, Dae Hong Ko, Dept of Ceramic Engineering, Yonsei Univ., Seoul, KOREA; Ja Hum Ku, Siyoung Choi, Samsung Electronics Co., Ltd., KOREA.

The SiO_2 dielectrics have been a subject of intensive studies for several decades. According to the past trends in mass production, however, reliability problems were considered to limit the physical thickness of gate SiO_2. Therefore, extensive research is underway to meet the challenge of moving beyond the SiO_2 era, that is, to replace the conventional SiO_2 with high-k gate dielectrics. The advantages of HfO_2 over SiO_2 is greater density which makes it more effective barrier to a migrating impurities - its high dielectric constant, and high band gap of 5.65eV with favorable band alignment with silicon. We studied and the optimized the characteristics of hafnium oxides deposited by different kinds of methods. Generally, reactive sputtering method is used to deposit the oxide thin films. However, there exists substantial interlayer between oxide and silicon, causing serious degradation to fully achieve the potential of high permittivity. In order to testify these problems, we examined the films using simple reactive sputtering and compared the results with the other films deposited by the modified sputtering method. During hafnium sputtering, O_2 flow was modulated to control the interface quality and to suppress the additional growth of the interfacial layer. If hafnium metal is covered before going through the reactive sputtering step, it acts as an oxygen barrier; thus interlayer, which is thought to be SiO_2, reduced down to $\sim 5\AA$. Electrical properties of hafnium oxides were evaluated using capacitance-voltage (C-V) and current voltage (I-V) measurements. It shows well-behaved C-V characteristics, indicating low level of interfacial trap charge. The equivalent oxide thickness was calculated to be $\sim 10\AA$ using modified reactive sputtering method. Besides, leakage current level was quite low comparing to SiO_2 with same physical thickness, accounting for the superiorities of hafnium oxide as a gate dielectric.

B4.7
IS IT A RIGHT ASSUMPTION THAT B AND Ge ARE DISTRIBUTED RANDOMLY AFTER GROWING A STRAINED HBT-STRUCTURE? V.I. Kol'dyaev, PDF/Solutions Inc., FEOL Dept, San Jose, CA.

A comprehensive review of the main experimental features of the B and Ge segregation onto Si substrate during growing a fully strained SiGe layers is carried out. The main feature of the segregation process is that surface B and Ge clustering is observed. The simplest clusters are a couple of B or a couple of Ge atoms on the surface, but a longer 1D chains or 2D areas are also seen with some sort of symmetry. This can be explained since the surface diffusion of B and Ge is enough for collision of atoms and clustering during a layer growth. The (2*1) reconstruction regions and quasi-reconstructed surface point defects like a divacancy are precursors for such a clusterization on the H passivated surface. These observations are strongly against the assumption that B and Ge are randomly incorporated into a strained layer rather suggesting a strong correlation of B and Ge distribution. Another observation is that surface Ge atoms are considered to be responsible for the surface B segregation process. A set of original experiments is carried out showing that at certain conditions B is taking initiative and determine the Ge surface segregation process. Basic assumptions are suggested to self-consistently explain these original experimental features and what is observed in the literature. These results have a strong implication for modeling the B diffusion in SiGe where the initial conditions should be formulated accounting for the correlation in B and Ge distribution. A new assumption for the initial condition to be "all B atoms are captured by Ge" is regarded as a right one implicating that there is no any transient diffusion controlled by the B capturing kinetics.

B4.8
IMPROVEMENT OF GATE DIELECTRIC QUALITY OF MNS CAPACITOR BY HYDROGEN ETCHING ON ULTRA THIN GATE DIELECTRICS. Parag C. Waghmare, Samadhan B. Patil, Rajiv O. Dusane, V. Ramgopal Rao, Dept of Metallurgical Engg and Materials Science, IIT Bombay, INDIA.

Silicon nitride is being considered as a promising candidate to replace thermal gate oxide dielectric, as the latter is reaching its scaling limit due to excessive increases in the gate tunneling leakage current. A novel technique called, the Hot Wire Chemical Vapor Deposition (HWCVD), had shown promise to synthesize gate quality silicon nitride films at 250°C while maintaining their primary advantage of higher dielectric constant. The deposition was carried out for one minute. However it was found that the fixed charges and the interface states were of the order of 5 e12. To improve the gate quality of the device due to the increase in fixed charges and interface states, hydrogen etching is carried out. This etching is carried out for 1 min at a hydrogen flow rate of 5 sccm with 250°C as substrate temperature. Our exhaustive characterization shows the reduction in fixed charges and the interface states to about 1e12. This could be due to unbonded silicon atoms getting passivated by hydrogen atoms.

B4.9
THE CHARACTERISTICS OF SILICON NITRIDE THIN FILM BY ATOMIC LAYER DEPOSITION. Joo-Hyeon Lee, Dept of Materials Science and Engineering, KAIST, Daejeon, KOREA; Hyuk Kim, Dept of Materials Engineering, Hanbat National Univ, Daejeon, KOREA; Yeon-Seong Lee, Dept of Multimedia Engineering, Hanbat National Univ, Daejeon, KOREA; Sa-Kyun Rha, Dept of Materials Engineering, Hanbat National Univ, Daejeon, KOREA; Chong-Ook Park, Dept of Materials Science and Engineering, KAIST, Daejeon, KOREA; Won-Jun Lee, Dept of Advanced Materials Engineering, Sejong Univ, Seoul, KOREA.

Recently, atomic layer deposition (ALD) attracts much interest in silicon integrated circuit processing owing to its accurate thickness control, conformal coverage, high film quality, and lower processing temperature. Silicon nitride films have been widely used as the interlayer dielectrics (ILD), and are deposited by conventional low-pressure chemical vapor deposition (LPCVD) in the front-end processing or by plasma-enhanced chemical vapor deposition (PECVD) in back-end processing. However, high process temperature of LPCVD and poor film quality of PECVD are being expected to limit the performance and the reliability of the state-of-art IC in the near future. In the present paper, silicon nitride films were deposited by ALD, and effects of process parameters on the film properties were examined. Silicon tetrachloride ($SiCl_4$) and dichrolosilane (DCS) were compared as the silicon source gas. Ammonia (NH_3) was used as the nitrogen source gas, and nitrogen was used as the purging gas between the pulse of $SiCl_4$ and NH_3. Using silicon tetrachloride as the

precursor, silicon nitride thin films were deposited controlling process parameters, such as chamber pressure, temperature, the time and number of the precursor pulses, and the properties of deposited films were characterized by various techniques. Based upon the leakage current data, we optimized the ALD process parameters for the silicon nitride deposition.

B4.10
ARGON ANNEALING-BASED IMPROVEMENTS OF THE PROPERTIES OF ULTRATHIN OXYNITRIDES POST-NITRIDES WITH NH_3. Anindya Dasgupta, Christos G. Takoudis, University of Illinois at Chicago, Department of Chemical Engineering, Chicago, IL.

Thermally grown Si_3N_4 films in NH_3 are known to have a higher dielectric constant and a higher N concentration than silicon oxides/oxynitrides, but they incorporate hydrogen atoms that induce hot electron carriers during subsequent high temperature processing. Further, silicon nitride is difficult to grow over 6 nm thick, due to self-limiting growth. One alternative is SiO_2 and SiN_yO_z films post-nitrided with NH_3.
In this work, we study the improvement of the properties of Ar annealed nitrided oxynitrides as a function of annealing temperature and duration. Secondary ion mass spectroscopy (SIMS) study of the nitrogen profile suggests that there is increased nitrogen removal with increasing annealing time and temperature. Electrical characterizations have been performed to find out the total charge density (q/cm^2) and interface trap density ($/eV\text{-}cm^2$) at different processing conditions before and after the annealing step. A post annealing step is found to remove unwanted hydrogen atoms and improve electrical properties but at the expense of nitrogen removal. An optimization of the annealing step is, therefore, essential in designing nano-dielectrics with desired nitrogen amount and concentration profiles and in understanding related process-structure-function relationships.

B4.11
LOW TEMPERATURE METAL ORGANIC CHEMICAL VAPOR DEPOSITION OF Al_2O_3 FOR ADVANCED CMOS GATE DIELECTRIC APPLICATIONS. Spyridon Skordas, Zubin Patel, Filippos Papadatos, Steve Consiglio, Gerry Nuesca, and Eric Eisenbraun, The University at Albany Institute for Materials (UAIM), Albany, NY.

A low-temperature, metal organic chemical vapor deposition (MOCVD) process for the growth of aluminum oxide (Al_2O_3) as a potential alternative gate dielectric layer has been developed on 200-mm Si wafers. Amorphous Al_2O_3 films were deposited on (100) oriented p-type silicon (Si) samples employing an aluminum -diketonate metal organic precursor (aluminum(III) 2,4-pentanedionate) and water (H_2O) as the aluminum and oxygen sources, respectively. A design-of-experiment (DOE) approach was employed for process optimization. The chemical, microstructural, electrical, and thermal stability properties of the resulting Al_2O_3 films grown over a temperature range of 250-450°C via this route were studied by x-ray photoelectron spectroscopy (XPS), X-ray diffraction (XRD) measurements, Rutherford back-scattering spectrometry (RBS), nuclear reaction analysis (NRA) for hydrogen profiling, scanning electron microscopy (SEM), transmission electron microscopy (TEM), atomic force microscopy (AFM), capacitance-voltage (C-V) and current-voltage (I-V) measurements. An optimized processing window was defined for the growth of dense, amorphous ultrathin Al_2O_3 films with carbon incorporation as low as 1 atomic % and hydrogen incorporation as low as 3 atomic %. The corresponding films possess typical dielectric constant values of 7-10. Post-deposition annealing studies indicate that the films chemical and structural properties are stable to temperature of at least 600°C. Thickness control was demonstrated for films as thin as 1.5 nm. Various post-deposition annealing methods were employed in order to improve the electrical properties of ultra-thin films. The resulting dielectric constant was as high as 10 and the leakage current behavior was comparable to that of silicon dioxide films of equivalent electrical thickness.

B4.12
TUNING THE MATERIAL AND ELECTRICAL CHARACTERISTICS OF ZrO_2 FILM OBTAINED BY PLASMA ENHANCED CHEMICAL VAPOR DEPOSITION. Byeong-Ok Cho, Jianjun Wang, and Jane P. Chang, University of California at Los Angeles, Dept of Chemical Engineering, Los Angeles, CA.

ZrO_2 was investigated as a dielectric to replace SiO_2 for dynamic random memory (DRAM) capacitor. ZrO_2 films were deposited on p-Si (100) wafers by ECR-PECVD using zirconium tetra-tert-butoxide ($Zr(OC_4H_9)_4$) as an organometallic precursor, Ar to carry the precursor vapor, and O_2 as oxidant. We used optical emission spectroscopy (OES), Langmuir probe, and quadrupole mass spectrometry (QMS) to characterize the gas phase. Using QMS, we identified all oxidation states of Zr and found that the compositional abundance shifted from Zr metal and monoxide to Zr dioxide and trioxide with the increase in O_2/Ar flow rate ratio (O_2/Ar). Atomic force microscopy results showed that the ZrO_2 surface was very smooth with rms=1.4 $\AA$ as long as O_2/Ar was set to over one. X-ray diffraction showed that the films were amorphous. X-ray photoelectron spectroscopy (XPS) and secondary ion mass spectrometry indicated that stoichiometric ZrO_2 film was obtained with various amount of carbon incorporation depending on the electron temperature and the O_2/Ar. We obtained a linear dependence of the carbon content determined by XPS upon the OES intensity ratio of molecular carbon and atomic oxygen. High resolution transmission electron microscopy was used to observe the interfacial layer formation between the deposited ZrO_2 and the substrate Si. Fourier transform infrared spectroscopy indicated that the layer was SiO_2. The electrical properties of the as-deposited ZrO_2 were assessed by forming $Al/ZrO_2/Si$ capacitor structures. We obtained the maximum dielectric constant of 16 at O_2/Ar=1. C-V curves shifted to higher bias voltage with increasing O_2/Ar, which indicated more negative fixed charges were introduced into the film as we add more O_2 in the gas phase. We observed that the leakage current density decreased drastically with increasing O_2/Ar. ZrO_2 film at O_2/Ar=4 showed $3.3\text{x}10^{-6}$ A/cm^2 at equivalent oxide thickness of 25 $\AA$.

B4.13
ZrO_2 GATE DIELECTRICS PREPARED BY ATOMIC LAYER DEPOSITION. Juwhan Park, Bongsik Choi, Nohhon Park and Jiyoung Kim, Dept. of Materials Engineering, Kookmin University, Seoul, KOREA.

According to 1999 ITRS roadmap, ultra thin gate oxide with EOT of less than 12Å are needed for beyond 0.1mm CMOS technology. Unfortunately, SiO_2 as a gate dielectric has been facing the scaling limitation due to its direct tunneling currents and reliability problems. Therefore, alternative gate dielectric materials have been extensively investigated such as TiO_2, Ta_2O_5 and ZrO_2 because of their high dielectric constants. While TiO_2 and Ta_2O_5 have low barrier heights and they thermodynamically unstable directly on Si during dopant activation annealing, ZrO_2 exhibits good thermal stability and high dielectric constant (about 20). In this study, atomic layer deposition (ALD) was used for ZrO_2 thin film depositions because its excellent thickness controllability and uniformity due to self limiting process. At the same time, this method may avoid formation of undesirable interface layer during process due to its low process temperature and lack of any energetic atom (or ion) bombardment. Zirconium t-butoxide and water were used as Zr and oxygen sources, respectively. In addition, combinations of NH_3 and water and NH_3 and O_3 were also evaluated as a oxidizing source. The ZrO_2 films deposited on p-type (100) silicon were annealed in various ambient, top electrodes were depositied using DC sputtering and a pattened device size is $2\text{ x}10^{-4}$ cm^2 and then the microstructures of ZrO_2 and interface were investigated by ellipsometry, XRD, AFM, TEM, RBS. Also, the electrical properties were assessed by C-V and I-V measurements of Metal-Oxide-Semiconductor (MOS) capacitor structure of $Pt/ZrO_2/(100)$ silicon.

B4.14
ENHANCED THERMAL STABILITY OF NiSi FILMS ON 20KEV BF_2^+ IMPLANTED (100)Si. A.S.W. Wong, D.Z. Chi, M.E. Loomans, D. Ma, W.C. Tjiu and S.J. Chua, Institute of Materials Research and Engineering, SINGAPORE.

The thermal stability of NiSi films formed on 20 keV BF_2^+-implanted (100) Si has been investigated. Phosphorous-doped (100) Si wafers with a resistivity of 1-10 $\Omega\cdot$cm were used in this study. 20 keV BF_2^+ implantation was performed at implant doses of $5 \times 10^{13}/cm^2$ and $5 \times 10^{15}/cm^2$. Some of the wafers implanted at a dose of $5 \times 10^{15}/cm^2$ underwent rapid thermal annealing (RTA) at 850°C for 60 s in order to regrow the surface amorphous layer (<40nm thick) and activate the dopants. 30nm thick Ni films were deposited on all samples, including control samples (Si wafers without implant), by sputter deposition after standard RCA cleaning and dilute HF dipping. The samples were then subjected to 60s RTA at 500-750°C for silicidation. X-ray diffraction (XRD), scanning electron microscopy (SEM), transmission electron microscopy (TEM) and secondary ion mass spectroscopy (SIMS) were employed in the analysis of the silicide films. Significant enhancement of NiSi thermal stability by the presence of fluorine in NiSi has been observed. The disilicide nucleation temperature increases to >750°C when NiSi forms on (100) Si implanted with 20 KeV BF_2^+ at an implant dose of $5\times10^{15}/cm^2$. The NiSi films formed on BF_2^+ implanted Si also exhibit much improved morphological stability. The observed enhancement of NiSi thermal stability is attributed to the retardation of grain growth, possibly due to fluorine decoration of NiSi grain boundaries and NiSi/Si interface. The retardation in the grain growth improves the morphological stability of NiSi films and the improvement in the morphological stability, in turn, suppresses the formation of $NiSi_2$ by reducing the number of the favoured sites for $NiSi_2$ nucleation.

B4.15
COMPOSITE X-RAY WAVEGUIDE-RESONATOR AS A BACKGROUND FOR THE NEW GENERATION OF MATERIAL TESTING EQUIPMENT FOR FILMS ON Si SUBSTRATES. Vladimir K. Egorov, Evgeniy V. Egorov, IPMT RAS, Chernogolovka, Moscow Dist., RUSSIA.

Planar X-ray waveguide-resonator (PXWR) functioned on total X-ray reflection phenomenon is formed by two plane parallel polished dielectric reflectors are positioned at several tens nanometers. PXWR is characterized by a high degree of an X-ray beam compression ($P \sim 1000 \div 10000$) and by low level of its intensity attenuation. The waveguide-resonator captures an X-ray radiation in the angle spread area $\Delta\theta_{in} \leq 2\theta_c$, where θ_c is the total reflection critical angle. Classical PXWR design assume the identify of inlet and outlet waveguide angle apertures and an emergent beam is submitted to limitation $\Delta\theta_{out} \leq 2\theta_c$. Composite planar X-ray waveguide-resonator (CPXWR) with length L contained two mutual aligned waveguides separated by distance $\Delta L \ll L$ allows to decrease divergence of its emergent beam. The angle area contraction of CPXWR emergent beam without falling of its total intensity is connected with abrupt decreasing of capture angle for second PXWR inlet of the composite waveguide. There are discussed examples of CPXWR practical applications for diffractometry of polycrystal and epitaxial film structures on Si substrates, TXRF spectrometry and X-ray reflectometry of the thin film materials.

B4.16
EFFECT OF POLYSILICON ANNEAL ON GATE OXIDE CHARGING DAMAGE IN POLYSILICON GATE PATTERNING PROCESS. Daniel Chong, Won Jong Yoo, National University of Singapore, Dept of Electrical and Computer Engineering, SINGAPORE; Lap Chan, Alex See, Chartered Semiconductor Manufacturing Ltd, Technology Developement, SINGAPORE.

Polysilicon film anneal is performed prior to polysilicon gate etch in certain process flows to activate part of the implanted dopants inside the polysilicon gate electrode. This step forms the first part of a two-step annealing/activation process for the polysilicon gate electrode. The second part of this two-step annealing process is performed during the source and drain junctions anneal. The reason for having a two-step polysilicon gate electrode annealing process is such that the thermal budget required to activate the source and drain junctions can be kept relatively low without affecting the resistivity of the gate electrode. Thermal budget for source and drain junctions anneal/activation is kept low to obtain shallow junction devices. Device or transistor wafers are fabricated using the 0.15 μm technology process flow. Transistors in the test structures are n-channel devices with gate oxide thickness of 20Å. The dimension of the gate oxide is 0.15 μm x 10 μm. The thickness of polysilicon film is 2000Å and the implanted phosphorus dose is 5.5x1015 cm^{-2}. An experimental split is performed at the polysilicon film anneal step. One set of wafers undergoes this step while another set skip it. Polysilicon film anneal is carried out in N2 ambient at 800°C for a 15 minutes time duration. Our study shows that this two-step polysilicon gate electrode annealing process does have some effect on gate oxide charging damage. Gate oxide charging damage is increased with the inclusion of the polysilicon film anneal step prior to gate patterning.

B4.17
ELECTRICAL CHARACTERISTICS OF SILICON IMPLANTED NANOCRYSTAL MEMORY IN SILICON NIITRIDE-SILICON DIOXIDE STRUCTURES. T.S. Kalkur, Department of Electrical and Computer Engineering, University of Colorado, Colorado Springs, CO; Nathaniel M. Peachey, Atmel Corporation, Colorado Springs, CO.

Recently, metal-oxide-semiconductor structure field effect transistors based on silicon implanted nano-crystals are attracting the attention of many investigators for the fabrication of non-volatile memories. In this paper we are presenting the results of non-volatile memory characteristics of heavy dose silicon implanted (1e16 per cm^2) silicon nitride-silicon dioxide structures.
Polysilicon-oxide-nitride-oxide-silicon structures were fabricated with silicon implanted nano-crystals have been fabricated and were characterized by capacitance-voltage and current-voltage measurements. These structures show hysteresis in their capacitance vs voltage characteristics which might be due to charge trapping at the silicon nano crystal-silicon dioxide interface.

B4.18
DEGRADATION STUDY OF ULTRA-THIN JVD SILICON NITRIDE MNSFETS. K.N. ManjulaRani, V. Ramgopal Rao and J. Vasi, Department of Electrical Engg., Indian Institute of Technology, Mumbai, INDIA.

Jet Vapour Deposited (JVD) silicon nitride has emerged as a viable alternative to SiO_2. It has been shown that JVD silicon nitride has excellent hot-carrier capabilities. In this paper, we report the degradation due to current limited constant voltage stressing in JVD Metal-Nitride-Semiconductor FETs (MNSFETs). The devices used in this study are n-channel MNSFETs with an Equivalent Oxide Thickness (EOT) of 3.1nm. The devices were fabricated in UCLA with the JVD deposition done at Yale University. Border traps or slow traps seem to play an important role in silicon nitride MNSFETs. We have developed a simple but accurate method of characterizing border traps using hysteresis in drain current of MNSFETs. This method can be used to characterize border traps in smaller channel length devices also. We will compare these results with those obtained by variable frequency charge pumping method. In addition to the border traps, the effect of stressing on V_{th}, g_m and N_{it} are also reported. In ultra-thin MNSFETs, the effect of Stress Induced Leakage Currents (SILC) and Soft-Breakdown (SBD) also become very important. SILC causes increase in leakage currents at low fields and is especially important for JVD MNSFETs in memory applications. We have observed that the JVD MNSFETs show very little increase in SILC after stressing. Next we look at Soft Breakdown characteristics of JVD MNSFETs. Noise in the gate current(observed in the Ig-Vg characteristics) is the most widely used method to characterize SBD. In addition to this, we have also used gate current transients before and after stress at sufficiently low voltages to detect SBD. We have observed Random-Telegraph-Noise (RTN) like behaviour after soft-breakdown. In ultra-thin SiO_2 MOSFETs, it is observed that although soft-breakdown increases the noise in currents, it does not effect the device performance. We have also observed that there is hardly any affect of SBD on the device performance in JVD MNSFETs.

B4.19
EFFECTIVE DIELECTRIC THICKNESS SCALING FOR *HIGH-k* GATE DIELECTRIC MOSFETS. Krishna K. Bhuwalka, Nihar R. Mohapatra, Dept of Electrical Engineering, Indian Institute of Technology, Bombay, INDIA; Siva G. Narendra, Microprocessor Research Lab, Intel Corporation, Hillsboro, OR; V. Ramgopal Rao, Dept of Electrical Engineering, Indian Institute of Technology, Bombay, INDIA.

The use of *high-K* materials as gate dielectric has received considerable attention for CMOS scaling. For successful induction into the mainstream technology, the short channel performance of MOS transistors with *high-K* gate dielectrics must be compared with the conventional SiO_2 at identical equivalent oxide thickness. It has been shown recently that the short channel performance worsens for *high-K* dielectric MOSFETs as the physical thickness to the channel length ratio increases, even when the effective oxide thickness is kept identical to SiO_2. In this work, we have systematically evaluated using 2-D simulations the effective dielectric thickness for different K_{gate} to achieve the targeted threshold voltage (V_t), drain-induced barrier lowering (DIBL) and I_{on}/I_{off} ratio for different technology generations down to 50 nm, following the SIA roadmap specifications. Our results clearly show that the oxide thickness scaling for *high-K* and SiO_2 follow different trends and the fringing field effects must be taken into account for estimation of effective oxide thickness when SiO_2 is replaced by a *high-K* dielectric. For example, with a T_{ox} (effective) of 1.5 nm for the 70 nm technology node, V_t reduces by about 5%, DIBL increases by 28%, and I_{on}/I_{off} decreases by alomost a factor of 2 if SiO_2 is replaced by a *high-K* dielectric of dielectric constant 30. This degradation becomes even more significant for sub 50 nm technologies. This paper summarises the oxide scaling trends for *high-K* dielectrics with the help of systematic 2-D simulations for channel lengths down to 50 nm, and with gate dielectric constant varied over a wide range, keeping in mind the *high-K* dielectrics currently being investigated by various research groups.

B4.20
CHARACTERIZATION FOR HIGH-k AND POROUS LOW-k THIN FILMS BY GRAZING INCIDENCE X-RAY SCATTERING. K. Omote, A. Takase, and Y. Ito, X-Ray Research Laboratory, Rigaku Corporation, Tokyo, JAPAN.

Atomic scale structure of thin high-k gate dielectrics is essential to the properties of films. It is believed that amorphous structure is suited for the gate dielectrics. Although x-ray scattering technique is useful to characterize such a structure, it is hard to measure the diffraction peaks of ultra-thin film with thickness below 10 nm by conventional θ-2θ scan method. Grazing incidence in-plane diffraction has high surface sensitivity and able to detect film peaks even though the thickness is less than 1 nm. By using in-plane geometry, we have successfully obtained the ZrO_2 diffraction down to 1 nm film thickness and detected the structural change by thermal annealing. In addition, we have also analyzed film stacked and interfacial structure of the ZrO_2 films in sub-nanometer scale by grazing incidence reflectivity measurement (XRR). Combination of these two techniques, we could determine precise structure of ultra-thin high-k dielectric films. We

will also present the method for determining pore-size distribution in porous low-k dielectric films by grazing incidence x-ray scattering. The technique has been used to analyze porous methyl silsesquioxane (MSQ) films. The pore size distributions determined by the x-ray scattering technique agree with that of the commonly used gas adsorption technique. The x-ray technique has successfully determined small pores down to sub-nanometers in diameter, which is well below the lowest limit of the gas adsorption technique.

B4.21
KINETICS OF INTERFACIAL FORMATION DURING POSTANNEALING OF PULSED LASER DEPOSITED HIGH-k DIELECTRICS ON SILICON. C. Essary, N. Bassim, V. Craciun, and R.K. Singh, Univ of Florida, Gainesville, FL.

Current silicon transistor technologies are nearing the physical limits of miniaturization using SiO_2 as the gate dielectric, therefore alternate higher-k dielectric materials are desired. Pulsed laser deposition (PLD) is an important tool for formation of thin films of these potential alternate high-k dielectric layers on silicon wafers. However, during deposition and annealing of ZrO_2 and Y_2O_3 films by PLD, an interfacial layer formation was noted. This layer has detrimental effects on the overall capacitance properties of the film. This presentation explores the kinetics of the formation of this interfacial layer and ways to impede its formation. Samples of both ZrO_2 and Y_2O_3 films were deposited using a pulsed-laser deposition technique and were post-annealed in various atmospheres, at different temperatures, and with increasing times. Using several characterization techniques, the thickness, uniformity, and bonding environment of the interfacial layer were determined. The results were used to model the kinetics of the formation of the interface. Further comparisons were made of samples deposited on top of a thin nitride layer formed by heating in a nitrogen environment to study the nitride effectiveness in slowing the interfacial layer growth.

B4.22
REMOTE PLASMA-ENHANCED CHEMICAL VAPOR DEPOSITION OF SILICON NITRIDE AT ATMOSPHERIC PRESSURE. Greg Nowling, Steve Babayan, Vladan Jankovic, and Robert Hicks, University of California, Los Angeles, Dept of Chemical Engineering, Los Angeles, CA.

Silicon nitride is widely used in silicon microelectronics for barrier layers, packaging, isolation, and novel dielectric structures. We have deposited high-quality silicon nitride films using a novel atmospheric-pressure plasma source. This source is operated without vacuum chambers and associated hardware, and represents a low-cost alternative to the equipment currently used for semiconductor processing. The atmospheric-pressure discharge was produced by flowing nitrogen and helium through two perforated metal electrodes that were driven by 13.56 MHz radio frequency power. Deposition occurred by mixing the plasma effluent with silane and directing the flow onto a rotating silicon wafer heated to between 100 and 500 degree C. Film growth rates ranged from 90 $\pm$10 to 1300 $\pm$130 angstroms/min. Varying the nitrogen/silane feed ratio from 43,000 to 4,300 caused the film stochiometry to shift from $SiN_{1.45}$ to $SiN_{1.2}$. Minimum impurity concentrations of 0.04% carbon, 3.6% oxygen and 13.6% hydrogen were achieved at 500 degree C and an nitrogen/silane feed ratio of 17,000. The growth rate increased with increasing silane and nitrogen partial pressures, but was invariant with respect to substrate temperature and rotational speed. The deposition rate also decreased sharply with distance from the plasma. These results combined with emission spectra taken of the afterglow suggest that gas-phase reactions between nitrogen atoms and silane play an important role in this process. At the meeting, we will further discuss the properties of the films, and their potential application in Si devices.

B4.23
HfO_2 FILMS FORMED BY THERMAL AND UV ASSISTED, INJECTION LIQUID SOURCE, CVD. P.K. Hurley, B.J. O'Sullivan, NMRC, University College, Cork, IRELAND; H. Roussel, F. Roussel, J.P. Senateur, M. Audier, C. Dubourdieu, INPG, Grenoble, FRANCE; Q. Fang, I.W. Boyd, Dept. of E&EE, University College-London, London, UNITED KINGDOM; T.L. Leedham, Inorgtech, Suffolk, UNITED KINGDOM; C. Jimenez, JIPElec, Crolles, FRANCE.

In this abstract we present the first results of HfO_2 films formed by thermal and UV assisted, injection liquid source, chemical vapour deposition. Using a liquid injection system HfO_2 films have been fabricated using a Hafnium tetra-t butoxide $[Hf(C_4H_9O)_4]$ precursor in a hexane solvent. HfO_2 films with thicknesses varying from 20-100 nm were formed over a range of temperatures (320-550°C) and deposition ambients (O_2, Ar, Ar+O_2, Ar+H_2). HfO_2 films have also been formed ($\approx$ 20 nm) using UV excimer lamp (222 nm) assisted, injection liquid source, CVD. For the initial studies relatively thick films (20-100 nm) were deliberately chosen to minimise interface effect and allow analysis of the bulk film composition. In both cases the substrates were Si(100), with approximately 1 nm chemical oxide present prior to deposition. Using the liquid injection system, the HfO_2 growth rate was determined to be in the region of 0.1 nm per injection, demonstrating atomic layer control using this technique. The films were analysed physically using XRD, FTIR, SIMS, SNMS and RBS, identifying the films as HfO_2, with carbon present at 1-2 At %. Both polycrystalline (T>365°C) and amorphous films (T <320°C) were formed. The polycrystalline structure is identified as monoclinic. The deposition efficiency (deposited film thickness/precursor mass injected) is established to be a strong function of temperature, but essentially independent of ambient. Electrical characterisation was performed using either a mercury probe or aluminium dots evaporated through a shadow mask. High frequency CV analysis reveals dielectric constants in the range 16-20, with breakdown fields in excess of 5MV/cm. The effect of post deposition UV O_2 annealing (350°C), and the effect of injection frequency, will also be presented.

B4.24
ELECTROLUMINESCENCE PROPERTIES OF INDIUM-TIN-OXIDE/EMBEDDED Si NANOCRYSTALLITES IN SiO_x/P TYPE Si/METAL STRUCTURE PREPARED BY PULSED LASER DEPOSITION. Jong Hoon Kim, Kyung Ah Jeon, Jin Back Choi, Sang Yeol Lee, Department of Electrical and Electronic Engineering, Yonsei University, Seoul, KOREA.

Nanocrstalline Si (nc-Si) on p-type Si substrate and indium-tin-oxide (ITO) have been prepared by pulsed laser deposition technique using a Nd:YAG laser with the wavelength of 355 nm. Basal pressure was maintained at 1-10^{-5} Torr. Nanocrstalline Si thin films are deposited in 1 Torr helium ambient. After deposition, nc-Si has been annealed in nitrogen gas. Strong violet-indigo luminescence from Si nanocrystallites has been observed at room temperature by photoluminescence (PL). Dependence of the electroluminescence (EL) properties on various deposition factors will be discussed using ITO/nc-Si/p-type Si/metal structure.

B4.25
EVOLUTION OF SPUTTERED HfO_2 THIN FILMS UPON ANNEALING. Seok Woo Nam, Jung Ho Yoo, Suheun Nam, Dae Hong Ko, Dept. of Ceramic Engineering, Yonsei Univ., Seoul, KOREA; Ja Hum Ku, Siyoung Choi, Samsung Electronics Co., Ltd., KOREA.

We investigated the evolution of the physical and electrical properties of HfO_2 thin films deposited by the reactive DC magnetron sputtering method on the (100) silicon substrate upon annealing. The HfO_2 thin films deposited at room temperature were amorphous, while the films after annealing were poly crystalline. The crystallization temperature of the HfO_2 thin films was dependent on the annealing methods (RTP or Furnace) and ambient (nitrogen or oxygen). The microstructures of HfO_2 thin gate oxides $<15\AA$ thick were analyzed by HRTEM, XRD and AES. We also focused on the interfacial layer between HfO_2 thin films and silicon substrates. Due to its high oxygen diffusivity, any annealing led to oxygen diffusion rapidly through the HfO_2 films. The EOT decreased upon annealing due to the increased SiO_2-containing layer. The HfO_2 thin films deposited at room temperature have the undesirable interfacial states due to the surface damage by sputtering. We found that the HfO_2 thin films $<15\AA$ thick were optimized by RTP or furnace annealing.

B4.26
FLAT BAND VOLTAGE, HYSTERESIS AND BREAKDOWN of HAFNIUM SILICATE PREPARED BY PVD TECHNIQUE. Hongguo Zhang, Gaurang Pant, Manuel Quevedo-Lopez, Prakaipetch Punchaipetch, Bruce E. Gnade, Robert M. Wallace, The Lab of Electronic Materials and Device, Dept. of Materials Science, Univ. of North Texas, Denton, TX.

The shift of flat band voltage Vfb and hysteresis observed for MOS capacitors prepared by PVD techniques are examined for (100) orientation-silicon substrate. Using a Pt/Al gate C-V system, the Vfb shift can be attributed to changes in the working function of gate metals and the electronic properties of oxide layer, as had previously been reported. In addition, this work indicates that the Vfb shift results from a reduction of interface state and oxide fixed charge due to the different forming gas annealing temperatures. The obvious hysteresis shows that the existence of large amount of trapping or detrapping defects in the oxide layer. The interface state and oxide charge densities are calculated and related to the available bonds at the interfaces. The breakdown experiments confirm that the Vfb shift for the MOS samples is mainly due to a reduction of oxide fixed charge in the oxide annealed in higher temperature, and to a lesser degree, to a reduction of interface charge.

B4.27
THE METAL INDUCED LATERAL CRYSTALLIZATION OF AMORPHOUS SILICON THIN FILMS BY ALTERNATING

MAGNETIC FLUX. Sung-Gye Park, Sang-Jin Park, Seung-Eui Nam, Hyung-Jun Kim, Department of Metallurgy and Material Science, Hong-Ik University, Seoul, KOREA.

Recently, many studies in poly-Si TFT LCD and poly-Si solar cell have focused on the recrystallization at temperature without affecting the glass substrates. For the fabrication of low temperature poly-Si TFTs less than 450°, a new method is designed using alternating magnetic flux crystallization (AMFC). We confirmed that the crystallization temperature and incubation time in MIC decrease according to alternating magnetic flux. In the case of MILC, the velocity of the lateral growth was accelerated in alternating magnetic flux. The lateral growth rate as a function of alternating magnetic flux according to the applied current. We observed lateral growth from 10A to 50A at 430°. The velocity of the lateral growth was remarkably accelerated up to 1.2 um/min as a function of the strength of applied current. It is expected that the migration of $NiSi_2$ precipitates in a-Si matrix may be enhanced by selective joule heating of a-Si films using alternating magnetic flux. We formed the patterned layer by photolithography in order to acquire selective metal region. The samples were annealed at 300° to 500° for 30 min in alternating magnetic flux of 14KHz and 50A.

B4.28
THERMAL STABILITY AND DIELECTRIC PROPERTY OF STACKED HIGH-k DIELECTRICS ON SILICON Y-S. Lin and J.P. Chang, Department of Chemical Engineering, University of California-Los Angeles, Los Angeles, CA.

Recognizing the need of using novel high-k dielectric materials for the next generation microelectronic devices, this paper addresses the thermal stability and the dielectric property of metal oxides/metal silicate. The thermal stability of $ZrO_2/ZrSi_xO_y$ and $ZrO_2/ZrSi_xO_y/SiN_x$ thin films deposited by an atomic layer chemical vapor deposition process on silicon was examined by Synchrotron radiation ultra-violet photoemission spectroscopy. The deposited $ZrO_2/ZrSi_xO_y$ stack is stoichiometric, uniform, amorphous, and has an equivalent oxide thickness of ~1 nm and a dielectric constant of ~18 with low leakage current. Micro-diffraction and high resolution transmission electron microscopy showed a localized monoclinic phase of ZrO_2 and an amorphous interfacial $ZrSi_xO_y$ layer which has a corresponding dielectric constant of 11. These $ZrO_2/ZrSi_xO_y$ samples are thermally stable in vacuum up to 880°C at which the film decomposed to form $ZrSi_2$, the most thermodynamically stable metal silicide at a per zirconium atom basis, and the desorption of $SiO_{(g)}$ and $ZrO_{(g)}$ accounted for the greatly reduced oxygen and zirconium photoemission intensities. The thermal stability of $ZrO_2/ZrSi_xO_y$ is improved to 950°C when deposited on a 0.5-0.7 nm SiN_x film. The conduction mechanism is identified as Schottky emission at low electric fields and as Poole-Frenkel emission at high electric fields. The MOS devices showed low leakage current, small hysteresis (<50mV) and low interface state density (~$2x10^{11}$ cm^{-2} eV^{-1}). To integrate these high-k dielectric materials in metal-oxide-semiconductor transistors, a high density plasma etching process is developed to pattern these materials and the etching rate is found to scale linearly with the ion energy, and the etching products are predominantly ZrCl2, ZrCl3 and ZrCl4. The etching mechanism is shown to be an ion-enhanced chemical etching process, and the ion energy and plasma density controls the proportionality of etching products. Etching anisotropy and selectivity will also be discussed.

B4.29
ELECTRICAL CHARACTERIZATION OF SIMOX SOI WAFERS WITH MOSOS C-V MEASUREMENTS. C.L. Li, Y.H. Yu, M. Chen, S.C. Zou, Sh. X, Z.X. Lin, Ion Beam Laboratory, Shanghai Institute of Metallurgy, Chinese Academy of Sciences, Shanghai, PEOPLES REPUBLIC OF CHINA.

SIMOX SOI is quite attractive for IC technology because of its potential for high-speed and low power consumption. SOI wafers are required to maintain good electrical performances in the buried oxide (BOX) layers, thus it is imperative to study the electrical characteristics of the BOX layers and the interface states. C-V and I-V techniques are very frequently utilized for extracting the parameters of the Si-SiO_2 interface in bulk-silicon MOS systems. In this paper, we use a new two-terminal MOSOS (metal-oxide-semiconductor-oxide-semiconductor) structure to study the electrical characteristics of SIMOX SOI wafers. Results gained from the comparison between the experimental curves and simulation curves are presented and analyzed. We show considerable improvement in comparison with results obtained using traditional methods.

B4.30
DOPANT PROFILE IN SILICON MATERIAL PROCESSING. Kal Renganathan Sharma, Vellore Institute of Technology (Deemed University), Vellore, Tamil Nadu, INDIA.

In silicon doping in transience the Fick's law of Diffusion is not adequate representation. This is because; a) mathematically it is poorly convergent at the short time limit for surface flux and b) physically it implies a infinite velocity of mass. The hyperbolic mass wave equation can represent the finite speed of propagation of mass which is realistic. Nothing is faster than the speed of light. The "only" modification that will remove the singularity in time is the second derivative in time in the hyperbolic partial differential equation. The problem of quenching a finite slab with both the ends of 1 dimension brought to C1 the bath temperature from a initial C0. The non-dimensionalized variables X = x/sqrt(Dtou(r)) and tou = t/tou(r) and u = (C1 - C)/(C1 - C0). The symmetry boundary condition at the center of the slab yields a slope of zero. The separation of variables technique is used to get a cosine series in X with lamda(n) being (2n-1)Pi/2sqrt(alpha tou(r))/a. The time domain is represented by a second order ODE. The solution gives a complex representation whose real part yields a cosine term in tou which yields a periodicity to the temperature solution damped by a decaying exponential. This is for values of lamda(n) >1/2. The An term is solved for by integration and is (1 - (-1)n)/n. This analytical solution can be used to predict the transient heat transfer in 1-dimension.

B4.31
GRAZING-ANGLE INCIDENCE X-RAY DIFFRACTION BY THE SiGeC/Si HETEROJUNCTION WHERE THE GERMANIUM AND THE CARBON CONCENTRATIONS ARE PERIODICALLY VARYING ALONG THE FLAT LAYER SURFACE.
Hayk H. Bezirganyan (Jr.), Yerevan State Univ, Faculty of Informatics and Applied Mathematics, Yerevan, ARMENIA; Siranush E. Bezirganyan, Hakob P. Bezirganyan, Yerevan State Univ, Faculty of Physics, Yerevan, ARMENIA; Petros H. Bezirganyan (Jr.), State Engineering Univ of Armenia, Dept of Computer Science, Yerevan, ARMENIA.

Evaluation of the coherent part of x-radiation scattered by strained or relaxed crystalline, as well as amorphous flat Si(1-x)Ge(x) layer deposited on the silicon substrate is presented in [1], and it is pointed out the possibility of the direct Grazing-angle Incidence X-ray Diffraction (GIXD) experimental investigations of the long-period structured intermediate transformation states of Si(1-x)Ge(x) layer, which are emerging due to periodicity of the strain field along the substrate-layer interface. The coherent intensity evaluation was done based on the theoretical method presented in [2]. The Si-C bond length is much smaller than the bond lengths in a Si(1-x)Ge(x) alloy, therefore a small amounts of carbon atoms provided an additional design parameter in manipulating the strain (e.g. see [3]), i.e. the effect of the increase of the average lattice constant due to germanium atoms can be compensated by adding the carbon atoms in the heterostructure. While studying the influence of carbon in Si(1-x-y)Ge(x)C(y) layer, it is also important the investigation of the behavior of the tensile strained Si(1-y)C(y) layers (e.g. see [4, 5]). In this paper we present the GIXD theoretical curves of a thin flat Si(1-x-y)Ge(x)C(y) layer deposited on a thick silicon perfect-crystal substrate. The diffraction occurs due to a specific long-range order in a layer e.g. through a harmonic variations of the germanium and carbon composition coefficients in the heterostructure. References: 1. P.A. Bezirganyan (Jr.), A.P. Bezirganyan, S.E. Bezirganyan and K.O. Hovnanyan, Grazing-Angle Incidence X-ray Diffraction Curves of Si(1-x)Ge(x) Thin Layer if the Composition Coefficient (x) is Varying Harmonically Along the Flat Layer Surface, the Book of Abstracts of 16th International Conference on X-ray Optics and Microanalysis (ICXOM XVI), Vienna, Austria, 2001, p.57. 2. A.P. Bezirganyan and P.A. Bezirganyan, Solution of the Two-dimensional Stationary Schrodinger Equation with Cosine-Like Coefficient (in View of X-ray Diffraction), Phys. Stat. Sol. (a), 105 (1988) 345-355. 3. B. Dietrich, H.J. Osten, H. Rucker, M. Methfessel, and P. Zaumseil, Lattice Distortion in a Strain-Compensated Si(1-x-y)Ge(x)C(y) Layer in Silicon, Phys. Rev. B, 49(24) (1994) 17185-17190. 4. G.G. Fischer, P. Zaumseil, E. Bugiel, and H.J. Osten, Investigation of the High Temperature Behavior of Strained Si(1-y)C(y) Heterostructures, J. Appl. Phys., 77(5) (1994) 1934-1937. 5. H.J. Osten, D. Endisch, E. Bugiel, B. Dietrich, G.G. Fischer, Myeongcheol Kim, D. Kruger, and P. Zaumseil, Strain Relaxation in Tensile-Strained Si(1-y)C(y) Layers on Si(001), Semicond. Sci. Technol., 11(11) (1996) 1678-1687.

SESSION B5: DIELECTRIC CHARACTERIZATION
Chair: David O'Meara
Wednesday Morning, April 3, 2002
Salon 10-12 (Marriott)

8:00 AM B5.1
EFFECT OF CARBON AND POROSITY ON ADHESION AND DEBONDING OF CARBON-DOPED OXIDE FILMS. Dong-Ick Lee, Reinhold H. Dauskardt, Materials Science and Engineering Dept, Stanford Univ, Stanford, CA.

As the size of microelectronic devices decreases dramatically, the RC delay and power dissipation are becoming the serious problem in VLSI technology. Accordingly, huge effort is being made on the interlayer dielectrics such as carbon-doped oxides which have the lower dielectric constant than the silicon dioxides constant ~4.0. However, since the alkyl group is put into the silicon oxide backbone, the volume expands and the interface characteristics are becoming inferior. This is caused by disruption of the glass network. This phenomena leads to inferior mechanical properties such as the fracture toughness, modulus and hardness which are closely related to the reliability of the micro-electronic devices. On my study the interfacial debonding and failure between the dielectric and adjacent layers in the multi-layer stack of thin films will be focused. Those failures are driven by the thermal and residual stresses between the films. Within the Linear Fracture mechanics technique the energy, termed as the critical strain energy release rate or the interface debond energy, which is needed to debond the dielectric film from the adjacent film can be determined. This energy includes the breaking of the chemical bonds across the interface as well as the plasticity in adjacent layers. Since inorganic silicate behaves like a completely brittle material, the carbon-doped oxide film is expected to behave in the same manner. Therefore the fracture energy of the interface is sensitive to the interface chemistry and glass composition. The subcritical debonding is also concerned in terms of reliability. Under the environment of high humidity and temperature crack can be growing with much less driving forces. This can cause the problem to the microelectronic devices. Two kinds of ways of making carbon-doped oxide film are used. Those are spin-on glass and CVD method. To measure the critical strain energy release rate, 4-point bending and double cantilever beam configurations are chosen. After testing, the resulting fracture surfaces were characterized by XPS scans to determine the debonding path. From the data obtained it was clarified that the fracture toughness is decreasing with the carbon contents increasing no matter what kind of alkyl group is. Moreover the debonding interface for CVD method is mostly happened on the lower interface between dielectric and silicon nitride layers by XPS scanning. It is explained that the fracture mode is the mixed mode so that the crack is growing downward as well as forward. For future work, the various kinds of functional groups can be adjoined in the silicate and tested and moreover the subcritical cracking can be induced by many degrees of humidity and temperature situation. Finally, the relationship between the glass composition and structure and the resulting mechanical properties can be elucidated.

8:15 AM B5.2
SYNTHESIS OF ORDERED NANOPOROUS SILICA FILM WITH HIGH STRUCTURAL STABILITY. Norikazu Nishiyama, Shunsuke Tanaka, Korekazu Ueyama, Osaka University, Dept of Chemical Engineering, Osaka, JAPAN; Yoshiaki Oku, MIRAI-ASET, Tukuba, JAPAN; Akira Kamisawa, Rohm Co Ltd, Kyoto, JAPAN.

In this study we synthesized nanoporous silica films with high structural stability on a silicon wafer. The silicon wafer was coated with a precursor solution by a spin-coating. The XRD pattern of the films showed that highly ordered silica was formed on the silicon wafer. The (110) reflection peak was not observed in the XRD pattern showing that the straight pore channels were oriented parallel to the support surface. This is due probably to the orderly arrangement of surfactant molecules on the silicon wafer. However, the formation of a silicate network is thought to be insufficient because the reaction rate of the condensation of silanol groups is not high at low temperature. To complete the condensation of a silicate network, a post-synthesis treatment was carried out. Then the calcination was conducted at 673 K for 5 h to remove surfactant molecules. No peak shift of the (100) reflection was observed in the calcined silica film. The peak intensity did not decrease, indicating high structural stability of the treated silica film. The FE-SEM images of the cross section of the treated silica film showed that its thickness is about 300 nm. The periodic porous structure can be observed in the cross section of the silica film. This corresponds to the results of the XRD patterns, which indicate that straight pores were oriented parallel to the surface of the silicon wafer. Normally, the periodic ordered structure of nanoporous silica gradually collapses under water vapor in the atmosphere. In this study, the silica films were silylated with organic vapor to enhance the resistance against water vapor. The pore surface effectively increased its hydrophobicity by silylation. The ordered structure of the silylated silica film was maintained under saturated water vapor at 333 K.

8:30 AM B5.3
HIGH QUALITY ZrO_2 GATE DIELECTRIC FOR SiGe MOS DEVICES. Sangmoo Choi, Sanghun Jeon, and Hyunsang Hwang, Kwangju Institue of Science and Technology, Dept of Materials Science and Engineering, Kwangju, KOREA.

Considering high hole mobility of strained SiGe/Si heterostructure, CMOSFET with SiGe pMOSFET is promising for future high speed device. However, a conventional high temperature thermal oxidation for gate dielectric is not compatible with SiGe heterostructure because of strain relaxation and Ge segregation effect. Improvement of carrier mobility of SiGe MOSFET with silicon capping layer was reported because silicon capping layer reduces Ge segregation and interface roughness during the thermal oxidation. Recently, the ZrO_2 film was investigated as a promising alternative gate dielectric for silicon MOS devices. We report on the electrical characteristics of ZrO_2 on SiGe with silicon capping layer. Epitaxial 30nm-thick $Si_{0.8}Ge_{0.2}$ strained layer was grown on p-type silicon wafer. For comparison, 7nm-thick epitaxial silicon capping layer was grown for some samples. Various thickness of ZrO_2 layer was deposited by e-beam evaporation followed by wet vapor annealing at 280°C. After the deposition of a 150nm-thick layer of Pt, MOS devices with a gate area of $9\times10^{-6}cm^2$ were defined. The wet vapor annealing of ZrO_2 reduce hysterisis which can be explained by the reduction of oxygen vacancy of as-deposited ZrO_2. Compared with ZrO_2 directly deposited on SiGe, ZrO_2 deposited on silicon capping layer exhibits a significant improvement of electrical characteristics such as low leakage current, low fixed charge density, negligible hysterisis, and low interface state density. The improvement of electrical characteristics of sample with silicon capping layer can be explained by negligible Ge segregation.

8:45 AM B5.4
CHARACTERISTICS OF ZIRCONIUM BASED AMORPHOUS THIN FILMS FOR GATE DIELECTRIC APPLICATIONS. Chang-Bae Jeon, Seong-Ho Kong and Jiyoung Kim, Dept. of Materials Engineering, Kookmin University, Seoul, KOREA.

Considering high leakage currents of thermal SiO_2 films with thickness less than 2.0nm, development of high-k films for gate dielectric applications is necessary to scale device dimension down to 100nm. Alternative gate dielectrics should simultaneously satisfy several harsh requirements, such as a high dielectric constant, a low leakage current, a good thermal stability on Si substrate, and excellent interface characteristics, etc. Even though various high-k materials have been studied in order to replace conventional thermal oxide, most of them show a trade-off. Unary metal oxides such as TiO_2, and ZrO_2 are easily transformed from amorphous to crystalline during dopant activation annealing. Since poly-crystalline thin films have lots of grainboundaries, amorphous phase is relatively preferred. On the other hand, silicates such as $ZrSiO_4$ shows excellent thermal stability. However, the silicates have relatively low dielectric constants (10-12). In order to realize a use of the silicate as an alternative dielectric, dielectric constant should be improved. In this study, we investigate effects of composition between Zr and Si on thermal stability and dielectric constants. In addition, effect of Al and Bi as novel glass network formers are also evaluated. Amorphous thin films were deposited by reactive co-sputtering because of its easiness on compositional change. However, reactive sputtering easily causes undesirable interfacial layers. In this study, various pre-treatments, such as nitridation are employed in order to reduce the interface layer. The deposited films are annealed at various ambients and then Pt top electrodes are formed. We will extensively reports the effect of composition of Zr based glass type thin films on thermal stability and dielectric behaviors on Si substrate.

9:00 AM B5.5
MOLECULAR LAYER DEPOSITION OF ULTRATHIN ZIRCONIA FILMS ON SILICON USING POLYNUCLEAR METAL ALKOXIDE PRECURSORS. Jason Lee, Walter G. Klemperer, University of Illinois, Frederick Seitz Materials Research Laboratory and Department of Chemistry, Urbana, IL; Erik A. Mikalsen, David A. Payne, University of Illinois, Frederick Seitz Materials Research Laboratory and Department of Materials Science and Engineering, Urbana, IL.

Conventional atomic layer deposition provides a viable route to high-k dielectric films on silicon. In order to reduce the number of growth cycles required, we have investigated the use of polynuclear metal alkoxide precursors capable of depositing several atomic centers in a single reaction step. Ultrathin zirconia films have been deposited on silicon using a tetrameric zirconium alkoxide precursor, $Zr_4(OPr^n)_{16}$, in fluid solution. Films with equivalent oxide thicknesses less than 2.0 nm and low leakage currents less than 10^{-3} A/cm^2 at -2.0 V were obtained using this process.

9:15 AM B5.6
CHARACTERIZATION OF HfO_2 FILMS FOR HIGH-k GATE APPLICATION. Ran Liu, N.V. Edwards, S. Zollner, J. Kulik, P. Fejes, R. Gregory, X.D. Wang, D. Werho, S.F. Lu, Motorola SPS, Advanced Process Development & External Research Laboratory, Mesa, AZ; J. Schaeffer, D. Triyoso, and B.Y. Nguyen, Motorola SPS, Advanced Process Development & External Research Laboratory, Austin, TX.

Currently there is still no clear front runner for the next alternative gate dielectrics despite extensive efforts. Much of the material

research and integration development are focused on transitional metal oxides and silicates, rare earth metal oxides and other oxides. This paper will present some recent results on materials and physical properties HfO_2 films grown on Si by CVD and ALD. Extensive structural, compositional, and optical characterization has been carried out using TEM, AFM, RBS, SIMS, AES, XRD, XPS, and optical spectroscopy (UV-Raman spectroscopy, spectroscopic ellipsometry, and IR transmission spectroscopy). Issues related to impurities, interfacial layers, and thermal stability will be addressed. New characterization method such as tunneling AFM has also been developed to correlate electrical "hot spots" with film structures.

10:00 AM *B5.7

ALTERNATING LAYER DEPOSITION (ALD) OF METAL SILICATES AND OXIDES FOR HIGH-k INSULATORS IN GATES AND CAPACITORS. Roy G. Gordon, Jill Becker, Eric Greyson, Dennis Hausmann, Esther Kim, Seigi Suh and Ying Wang, Harvard University, Dept of Chemistry and Chemical Biology, Cambridge, MA.

New processes are studied for ALD of silicates and oxides of the metals lanthanum, zirconium, hafnium and tantalum. For deposition of metal silicates, the silicon and oxygen source is tris(tert-butoxy)silanol, $(^tBuO)_3SiOH$, and the metal precursors are metal alkylamides such as tetrakis(dimethylamido)hafnium, $(Me_2N)_4Hf$. Pulses of silanol vapor and metal amide vapor are introduced alternately and separately into the heated deposition zone where they react on the surfaces of substrates. For the deposition of metal oxides, the metal alkylamides are reacted with water vapor instead of the silanol. Each of these reactions is shown to be self-limiting within a certain range of substrate temperatures. Excellent step coverage and highly uniform thicknesses and compositions are found for films deposited within these temperature ranges. By using both silanol and water pulses in various ratios, various compositions are deposited with silicon to metal ratios ranging from zero up to about 4. The surfaces of the films are quite smooth, with rms roughness (by AFM) less than 1% of the thickness. The stoichiometry and kinetics of the surface reactions are studied with a quartz crystal microbalance. The oxide reactions are found to be remarkably fast, while the silicate reactions require a higher flux to reach saturation.

10:30 AM B5.8

CHARACTERIZATION AND ELECTRICAL PROPERTIES OF ULTRA THIN HfO_2 GATE DIELECTRICS PREPARED BY ATOMIC LAYER DEPOSITION. Taeho Lee, Jaemin Oh, Hanyang Univ, Dept of Materials Science & Engineering, Seoul, KOREA; Youngbae Kim, Duckkyun Choi, Hanyang Univ, Dept of Ceramic Engineering, Seoul, KOREA; Jaehak Jung, Evertek Corp, Sungnam-City, Kyunggi-Do, KOREA; Jinho Ahn, Hanyang Univ, Dept of Materials Science & Engineering, Seoul, KOREA.

For the future integrated circuit manufacturing, new materials and thin film deposition methods will be needed for gate dielectrics preparation. Among the various deposition methods, atomic layer deposition (ALD) is one of the most promising techniques capable of meeting the strict requirements in the future IC manufacturing. However, the evaluation of this ultra thin high dielectric film is cumbersome and sometimes difficult. In this research we have investigated the characteristics of ultra thin ALD HfO_2 films using several analytical techniques. HfO_2 films were deposited in a traveling wave type ALD reactor (Plus 200^{TM}) using $HfCl_4/H_2O$ as precursors and N_2 as a carrier/purge gas. Solid $HfCl_4$ was volatilized in a canister kept at 200°C and carried into the reaction chamber with pure N_2 carrier gas. H_2O canister was kept at 12°C and carrier gas was not used. The films were grown on 8-inch (100) p-type silicon wafer in the temperature range of 200-400°C after standard RCA cleaning. Spectroscopic ellipsometer, XRD and TEM were used to investigate the initial growth mechanism and microstructure. The chemical composition of deposited film was analyzed by RBS and XPS. The electrical properties of the film were measured and compared with the physical/chemical properties. The effects of final substrate treatment, deposition temperature, and precursor injection time on the ALD HfO_2 films will be discussed. Also, the comparison of the evaluation results from the several analytical techniques will be addressed. The effect of process condition on the electrical properties will be discussed based on the bulk and interfacial structure of the HfO_2 film.

10:45 AM B5.9

REACTION BETWEEN POLYSILICON GATE ELECTRODES AND HIGH-k La-O-Si SILICATE LAYERS. M.J. Kelly, T. Gougousi, K. Bray, W.S. Burnside, J.M. Bennett, T.L. Schmit, and G.N. Parsons, Dept. of Chemical Engineering, NC State University, Raleigh, NC.

Stability of gate electrode materials on high-k dielectrics is a critical issue for advanced gate stacks. For this study, lanthanum silicate dielectrics were prepared by oxidation of PVD La on silicon using two slightly different processes at the same temperature (900C). Process (A) resulted in film with no visible OH in the infrared absorption spectrum, and process (B) resulted in a film with a small amount of OH visible in the IR. The only difference between process A and B was the conditions of substrate preparation before dielectric layer formation, and X-ray Photoelectron Spectroscopy analysis of as-prepared films indicated no other significant difference between the two processes. Two samples of each process were prepared, and all samples showed consistent results. Thin (30-50A) amorphous silicon was deposited on all samples. AFM analysis indicated that the thickness was sufficient to achieve complete surface coverage, but the silicon was thin enough to enable analysis of the top poly/dielectric interface by XPS. XPS data was collected with the top silicon as deposited, and after several high temperature annealing steps (temperatures ranging from 650 to 1050C). When the polysilicon on the OH-free sample (process A) was annealed at high temperature, XPS showed oxidation of the exposed polysilicon surface, with no significant change in the lanthanum related features. However, for the films that contained hydroxide (process B), XPS results show significant changes in the Si 2p spectrum, suggesting that the thin polysilicon layer reacts with the dielectric layer during the anneal step leading to consumption of the polysilicon. These results are consistent with excess oxygen (in the form of water vapor) promoting a reaction between the metal oxide and silicon. Implications for stability between high-k dielectrics and polysilicon gate electrodes will be discussed.

11:00 AM B5.10

INTERFACE PROPERTIES OF YTTRIUM OXIDE HIGH DIELECTRIC CONSTANT INSULATORS DEPOSITED BY OXYGEN PLASMA ASSISTED CHEMICAL VAPOR DEPOSITION. D. Niu, R.W. Ashcraft, and G.N. Parsons, Dept. of Chemical Engineering, NC State University, Raleigh, NC.

Controlling interface and bulk chemical stability of CVD high-k dielectrics is a critical issue for advanced gate stacks, but the mechanisms that control interface structure during deposition are not well understood. We have studied deposition of yttrium-based high-k dielectrics formed by oxygen plasma assisted CVD at temperatures between 350 and 450°C using a yttrium diketonate precursor introduced downstream from a remote oxygen plasma. Physical film thickness ranged from <40A to >1000A, and films were characterized using IR, XPS, TEM, EELS, and IV and CV electrical analysis, before and after annealing at temperatures up to 1000C. XPS and TEM analysis indicate that during initial film deposition, significant mixing occurs between the initial deposited Y-containing layers and the silicon substrate, leading to a mixed Y-O-Si (silicate) layer at the interface with thickness >10A. Continued film growth result in Y_2O_3 formation on top of the interface silicate. Over a wide range of thickness, as deposited films show evidence for O-H and C-H bonds in the IR spectra, and the O-H peaks grow over time. After annealing at 900°C in N_2 (with >10-5 Torr O_2 pressure), the IR shows almost complete removal O-H and C-H bonds, and for thin (<100A) dielectric layers, XPS indicates further consumption of the substrate silicon. Thicker dielectric layers show a measurable decrease in net film thickness, also consistent with substrate consumption during post-deposition anneal. High resolution TEM/EELS analysis shows results consistent with XPS and CV analysis. While results to date do not allow unambiguous linkage between OH reduction and silicon substrate oxidation, the results suggest that post-deposition OH absorption is a critical issue for controlling interface structure and post-deposition reactivity in high-k dielectrics deposited on silicon. Approaches to control hydroxide incorporation and improve material stability will be presented and discussed.

11:15 AM B5.11

CONTROL OF A METAL-ELECTRODE WORK-FUNCTION BY SOLID-STATE DIFFUSION OF NITROGEN. R.J.P. Lander, J.C. Hooker, Philips Research Leuven, Leuven, BELGIUM; J.P. van Zijl, M.P.M. Maas, Y. Tamminga, and R.A.M. Wolters, Philips Research Laboratories, Eindhoven, THE NETHERLANDS.

Metal gate electrodes are increasingly attractive for future CMOS technologies as they eliminate poly-Si gate depletion, reduce gate resistance, improve matching behaviour etc. It is generally accepted that conventional planar CMOS will require gate electrodes with two work-functions in order to achieve suitable Vt for both n- and p-MOSFETs. The integration issues could be greatly eased if the electrode work-function at the dielectric interface could be selectively adjusted for a single metal. This would allow fine-tuning of the threshold voltages and might give the dual-work-function gate electrodes without the need to remove one metal and redeposit a second. Several groups have reported the influence of nitrogen content at the metal-dielectric interface upon the work-function of TiN metal gates. In those studies the nitrogen was selectively introduced by low energy ion implantation. In this report it is demonstrated that a substantial concentration of nitrogen can be achieved at a molybdenum-SiO_2 interface by solid-state diffusion from a deposited TiN overlayer. Patterning of this overlayer prior to diffusion is straightforward and it is shown that only moderate diffusion

temperatures (800C/30min) result in measurable nitrogen concentrations at the metal dielectric interface (from Rutherford back-scattering measurements) and substantial changes in flat-band voltage (∼0.25V from capacitance-voltage measurements).

11:30 AM B5.12
ELECTRICAL AND STRUCTURAL PROPERTIES OF ULTRA-THIN ZIRCONIA DIELECTRICS. Shriram Ramanathan, Paul C. McIntyre, Stanford University, Dept. of Materials Science and Eng., Stanford, CA; David A. Muller, Bell Laboratories, Lucent Technologies, Murray Hill, NJ.

Ultra-thin ZrO_2 films are currently being investigated as a potential candidate to replace SiO_2 in future complementary metal-oxide-semiconductor devices. In order to integrate them into future transistors, a fundamental understanding of their electrical properties is desired. This requires a thorough investigation of the microstructure and interface chemistry of these films in conjunction with studies of their dielectric behavior, which will enable better processing methods to grow high-quality zirconia films. This paper deals with studies on thin films of zirconia grown by ultra-violet ozone oxidation of Zr metal films at room temperature. The effects of oxidation time, oxygen partial pressure, the underlayer and annealing conditions have been studied in detail. It was found that partially-oxidized films exhibited significant frequency dispersion in both the depletion and accumulation regions, while fully-oxidized films showed negligible frequency dependence. A model based on the Maxwell - Wagner interfacial polarization mechanism has been used to interpret such phenomena and will be presented in detail. The electrical studies of oxygen-deficient zirconia have been complemented with detailed studies of the electronic structure using atomic resolution EELS in a STEM. It was found that the oxygen stoichiometry of the zirconia films had a significant effect on the O-K near edge structure and this will be discussed using a molecular orbital description. Studies on CV hysteresis revealed that the flatband shift scaled with zirconia thickness. It was found that the leakage current could be modeled as direct tunneling at low voltages while Poole-Frenkel mechanism dominated at higher voltages. The trap energy levels were calculated from modeling the IV data measured as a function of temperature and found to agree with values reported for ALD-grown SiO_2 / ZrO_2 stacks. It is suggested that the electrical traps in the zirconia films may be responsible for CV hysteresis. References: S. Ramanathan et al., (a) Appl. Phy. Lett. (in press, 2001), (b) Jl. App. Phy. (submitted, 2001).

SESSION B6: GATE OXIDES AND INTERFACES
Chair: David O'Meara and Jon-Paul Maria
Wednesday Afternoon, April 3, 2002
Salon 10-12 (Marriott)

1:30 PM B6.1
SUBSURFACE REMOVAL OF SiO_2 TO CREATE A DIRECT SILICATE/Si(001) INTERFACE. M. Copel, E. Cartier, V. Narayanan, S. Guha, N. Bojarczuk, P. Batson and M. Gribelyuk, IBM T.J. Watson Research Center, Yorktown Heights, NY.

In order to reduce parasitic capacitance in alternative gate dielectrics, it is quite common to remove surface SiO_2 prior to deposition of a metal oxide dielectric. A typical procedure involves aqueous HF etching to create an oxide free substrate. Using medium energy ion scattering we have investigated a novel approach, where interfacial oxide is removed after deposition by high temperature annealing in ultra-high vacuum. Surprisingly, there is a temperature window in which silicide formation does not occur, but oxygen containing species can freely migrate out through a silicate overlayer. An examination of the kinetics shows a similarity to SiO desorption from SiO_2/Si(001), suggesting that the same mechanism occurs for an SiO_2 layer embedded underneath a silicate. The results confirm stability predictions for silicate dielectrics, i.e. for the proper choice of materials, the metal-oxygen bonds have greater stability than the silicon-oxygen bonds.

1:45 PM B6.2
Sr FLUX CLEANING OF Si AND THE FORMATION OF TEMPLATES FOR $SrTiO_3$ GROWTH. Xiaoming Hu, Yi Wei, B. Craigo, J.L. Edwards Jr., J.Z. Yu, R. Droopad, K. Moore, and W.J. Ooms, Physical Science Research Laboratories - Motorola Labs, Tempe, AZ; D. Sarid, Optical Sciences Center, University of Arizona, Tucson, AZ.

The removal of native silicon dioxide using a beam of Sr atoms and the resulting Sr/Si(100) surface phases have been studied by LEED, AES and STM. The conditions for the formation of Sr/Si(100) template, namely the "2x1" phase, for epitaxial MBE $SrTiO_3$ growth [1] have been identified. It has been found that the resulting Sr/Si surface phases depend upon the substrate temperature during the Sr flux de-oxidation process, in agreement with earlier findings that the Sr/Si phases are temperature related when depositing Sr on a clean Si(100) [2]. Post annealing of a sample obtained with the substrate at a lower temperature resulted in the slow adsorption of Sr atoms from the silicon surface and a progression of Sr phases with time. Similar results can also be obtained with the silicon substrate held at higher temperatures. Sr flux cleaning of a silicon wafer pre-treated with HF has also been studied and similar Sr/Si phases can be obtained by adjusting the substrate temperatures or annealing conditions. [1] Z. Yu, J. Ramdani, J.A. Curless, J.M. Finder, C.D. Overgaard, R. Droopad, K.W. Eisenbeiser, J.A. Hallmark, and W.J. Ooms, J.R. Conner and V.S. Kaushik "Epitaxial perovskite thin films grown on silicon by MBE", JVST B18 (2000) 1653. [2] Xiaoming Hu, Z. Yu, J.A. Curless, R. Droopad, K. Eisenbeiser, J.L. Edwards Jr., W.J. Ooms, D. Sarid, "Comparative study of Sr and Ba adsorption on Si(100)", Applied Surface Science, 181 (2001) 103.

2:00 PM B6.3
THE INTERFACE CONTROL OF Gd_2O_3 FILMS GROWN ON Si(111) USING VARIOUS BUFFER LAYERS. Y.S. Roh, S.A. Park, Y.K. Kim, M.-H. Cho, C.N. Whang, K. Jeong, Yonsei Univ, Dept of Physics, Seoul, KOREA; D.-H. Ko, Yonsei Univ, Dept of Ceramic Engineering, Seoul, KOREA.

We investigated the characteristics of the gadolinium oxide thin films controlled by interfacial layers. Ultra-thin ZrO_2 and SiO_2 layers grown on Si (111) were used to modify the surface of the Si substrate. The characteristics of the films were assessed using various characterization tools such as reflection of high-energy electron diffraction (RHEED), x-ray diffraction (XRD), Rutherford back-scattering spectroscopy (RBS), atomic force microscopy (AFM) and X-ray photoelectron spectroscopy (XPS). We found out that the structural transition from cubic Gd_2O_3 to monoclinic Gd_2O_3 was occurred using buffer layers. In particular, the transition was enhanced at the existence of ZrO_2 buffer layer. The crystallinity of the films was significantly affected by whether the buffer layer was inserted or not. The interfacial reaction between Gd and Si or $Gd_{1+x}O_{2-x}$ and Si critically affected the growth. The buffer layers successfully controlled the interfacial reaction and high quality epitaxial film were grown.

2:15 PM B6.4
PREPARATION AND OH ABSORPTION IN LANTHANUM SILICATES FORMED BY OXIDATION OF PVD La ON SILICON. T. Gougousi, M.J. Kelly, W.S. Burnside, J.M. Bennett, T.L. Schmit, and G.N. Parsons, Dept. of Chemical Engineering, NC State University, Raleigh, NC.

We have prepared La-based amorphous La-O-Si alloys, i.e. "silicates", by sputter depositing La onto Si in a UHV sputter chamber, then oxidizing in N_2O at temperatures ranging from 400C to 900C. Because lanthanum is reactive in air, target preparation and handling is critical to maintain high purity La deposition. When La is deposited on Si and oxidized, X-ray Photoelectron Spectroscopy indicates that the La reacts very rapidly with the silicon, leading to predominantly La-O-Si bonding units in the film. The mechanisms are similar to those detailed previously for Y PVD and oxidation, but the rate of reaction between La and Si is significantly faster than that of Y and Si. The relative concentration of La and Si in the resulting film depends on initial La layer thickness, substrate pretreatment, and oxidation time and temperature. By controlling these parameters, we have been able to achieve La-silicate thin films with equivalent oxide thickness as small ∼15A based on capacitance voltage analysis. CV show good behavior, with evidence for positive fixed charge, similar to most other reports of metal oxide high-k dielectrics. After deposition, infrared absorption of thicker silicate films showed evidence for OH absorption from the ambient. The rate of OH absorption depended strongly on the annealing temperature, suggesting a structural compaction of the dielectric layer upon annealing, similar to well known processes in SiO_2. The presence of hydroxide in high-k dielectric layers can help promote reactions between metal oxides and silicon, resulting in unwanted lower-k layer formation at the high-k/silicon interface. Details of the material preparation and stability to OH absorption will be discussed in terms of advancing the understanding of controlling interface reactions during CVD of high-k dielectrics on semiconductor surfaces.

3:00 PM B6.5
OXIDES, SILICIDES, AND SILICATES OF ZIRCONIUM AND HAFNIUM; DENSITY FUNCTIONAL THEORY STUDY. Maciej Gutowski, John E. Jaffe, Pacific Northwest National Laboratory, Environmental Molecular Sciences Laboratory, Theory, Modeling & Simulations, Richland, WA; Chun-Li Liu, Matt Stoker, Anatoli Korkin, Advanced Process Development and External Research Laboratory, Motorola, Mesa, AZ.

It is known that the chemistries of hafnium and zirconium are more

nearly identical than for any other two congeneric elements. Thus, both zirconia, with the dielectric constant K of 21, and hafnia (K = 21) have emerged as potential replacements for silica (K = 3.9) as a gate dielectric. We have recently found that there is an important difference between the zirconia/Si and hafnia/Si interfaces. The former was found to be unstable with respect to formation of silicides whereas the latter is stable. This surprising difference prompted us to study differences between oxides, silicides, and silicates of hafnium and zirconium. The calculations were performed in the framework of density functional theory with the Perdew-Wang 91 exchange-correlation functional. The ionic compounds were found to be more stable for hafnium than for zirconium with the heats of formation of oxides and silicates being larger by ca. 0.5 eV for hafnium. The higher ionicity of hafnium compounds is also reflected by the band gaps that are larger by 0.5 (oxides) and 0.9 (silicates) eV for hafnium than for zirconium. The higher ionicity of hafnium compounds is consistent with a smaller electronegativity of atomic hafnium (1.3) than zirconium (1.4), but inconsistent with atomic ionization potentials 7.9 and 7.0 eV for Hf and Zr, respectively. The silicides were found to be more stable for zirconium than for hafnium with the heats of formation of disilicides being larger by ca. 0.3 eV for zirconium. Both mono and disilicides were found to be metallic with no quantitative differences in densities of states between hafnium and zirconium compounds.

3:15 PM B6.6
DOPANT DIFFUSION STUDIES FROM As-, B- AND P-DOPED POLYSILICON THROUGH CVD DEPOSITED Hf SILICATE THIN FILMS. M. Quevedo-Lopez, P. Punchaipetch, G. Pant, M. El-Bouanani, M. Kim, B.E. Gnade, and R.M. Wallace, Department of Materials Science, University of North Texas, Denton, TX; L. Colombo, M. Bevan, M. Douglas, A. Li'fatou and M. Visokay, Si Technology Research, Texas Instruments Incorporated, Dallas, TX.

As the aggressively scaling of CMOS technology continues, high-κ gate dielectrics become one of the solutions in providing increased capacitance without remarkable increase in gate leakage current. However, issues such as thermal stability[1] and dopant penetration[2] still require further study. Dopant penetration into the channel region from doped polysilicon is an increasingly important issue in MOSFET's. Under high temperature processing, such as dopant activation annealing, dopants can diffuse out of the doped polysilicon gate, through the thin gate dielectrics and into the Si substrate, causing a shift in the threshold and flat-band voltages of the device. Diffusion studies of boron, arsenic, and phosphorous from doped polysilicon through the high-κ gate dielectric thin film (4-5 nm) candidate $HfSi_xO_y$ into Si will be presented. The Polysilicon/ $HfSi_xO_y$/Si stack was subjected either to rapid thermal processing (RTP) or standard furnace annealing in an N_2 atmosphere. After annealing, the polysilicon and dielectric films were chemically etched prior to depth profiling using Secondary Ion Mass Spectrometry (SIMS) methods. As-deposited and annealed films were studied using X-ray Photoelectron Spectroscopy (XPS) and High resolution Transmission Electron Microscopy (HRTEM) to determine any structural changes or growth of interfacial layers. Dopant penetration after aggressive annealing was observed. Polysilicon removal and dielectric film removal issues after annealing will also be discussed.
[1] M. Quevedo-Lopez, M. El-Bouanani, S. Addepalli, J.L. Duggan, B.E. Gnade R M. Wallace M.R. Visokay, M. Douglas, M.J. Bevan, and L. Appl. Phys. Lett. 79 (2001) 2958.
[2] K. Onishi, L. Kang, R. Choi, E. Dharmarajan, S. Dopalan, Y. Jeon, C. Seok, B. Hun-Lee, and J.C. Lee. 2001 Symposium on VLSI Technology Digest of Technical Papers.
This work supported by Texas Advances Technology Program, the Semiconductor Research Corporation, and DARPA.

3:30 PM B6.7
COMPARISON OF VIABLE MOCVD PRECURSORS FOR HAFNIUM SILICATES FOR CMOS DEVICES. B.C. Hendrix, A. Borovik, Z. Wang, C-Y Xu, J.F. Roeder, T.H. Baum, ATMI, Danbury, CT; M.J. Bevan, M.R. Visokay, J.J. Chambers, A.L.P. Rotondaro, H. Bu, L. Colombo, Texas Instruments, Dallas, TX.

Hafnium silicates are leading contenders for replacing silicon oxynitride as the gate dielectric material in CMOS devices. Silicates as defined herein cover the entire composition range from SiO_2 to HfO_2 and are regarded as a homogenous mixture of the binary oxides. Silicates offer advantages over the binary oxides that include maintaining an amorphous nature (at least as-grown or during subsequent thermal processing below 1000°C) and etching comparable to SiO_2. CVD is being considered for their manufacture, and appropriate metalorganic precursors are being evaluated. This study investigates and compares the deposition of Hf silicate films from two suites of metalorganic CVD precursors. The first precursor suite has oxygen coordinated to the Si or Hf center and includes β-diketonate, alkoxide and acetoxy ligands. The second precursor suite has alkylamido ligands, which have nitrogen coordinated to the Hf or Si center. Since these amido precursors do not contain oxygen, the oxygen activity of the process is controlled independently from the precursors. The process space for deposition of silicates was evaluated to determine under what conditions the composition of the silicate can be controlled and growth rates are sufficient for a manufacturable single-wafer process. The Hf:Si ratio in the film is controlled over the entire range by changing the ratio of Hf:Si in the precursor solution. The composition of the films, including Hf:Si ratio, oxygen, carbon, and nitrogen content were measured by XPS. Both suites of precursors provide routes by which composition can be controlled in fully oxidized films with low carbon and nitrogen content. Very thin interfacial layers (HRTEM) are also shown.

3:45 PM B6.8
INVESTIGATION OF LIGHT INITIATED OXIDATION OF HYDROGEN PASSIVATED SILICON SURFACES: H_x-Si(100) AND H-Si(111). Kathleen A. Morse, Stanford University, Dept of MS&E, Stanford, CA; Piero Pianetta, Dept of Electrical Engineering, Stanford University, Stanford, CA.

Factors present in cleanroom air that may lead to contamination prior to processing need to be better understood in order to meet tomorrows requirement for atomically clean surfaces prior to gate oxidation. This paper identifies the conditions that initiate room temperature oxidation of fluoride prepared hydrogen passivated silicon surfaces by using X-ray Photoelectron Spectroscopy (XPS). Possible oxidation factors investigated include lighting conditions and gaseous ambient. Both H_x-Si(100) and H-Si(111) surfaces do not oxidize under dark lighting conditions for 100% humid and dry air ambients. These surfaces do oxidize in the dry air and 100% humid air ambients when substrate is directly exposed 250nm light. Wavelength dependence for oxidation on both surfaces is confirmed. In addition, the level of oxidation is observed to depend on substrate orientation but not dopant type.

4:00 PM B6.9
SILICON NANOSTRUCTURES THROUGH NEAR-FIELD OPTICAL LITHOGRAPHY. Yadong Yin, Younan Xia, Univ of Washington, Dept of Chemistry, Seattle, WA.

Near-field optical lithography with an elastomeric phase-shift mask has been combined with silicon-on-insulator (SOI) wafers to generate nanostructures of single crystalline silicon with well-defined shapes and dimensions. We have demonstrated the capability and feasibility of this approach by fabricating nanowires, nanorings, and interconnected triangles with lateral dimensions of ~100 nm. This dimension could be further reduced to ~20 nm by adding self-limited oxidation to this process. These silicon nanostructures are potentially useful as active components in fabricating nanoscale electronic devices. They also provide a class of good model systems to study nanoscale mechanics and electrochemistry.

SESSION B7: POSTER SESSION
DIELECTRIC CHARACTERIZATION
Wednesday Evening, April 3, 2002
8:00 PM
Salon 1-7 (Marriott)

B7.1
STUDY OF SUB-NANOMETER GATE OXIDE IN FIELD EFFECT TRANSISTORS BY ATOMIC SCALE SCANNING TRANSMISSION ELECTRON MICROSCOPY. Teya Topuria, Nigel D. Browning, University of Illinois at Chicago, Dept of Physics, Chicago, IL; Zhiyong Ma, Kevin Johnson, Intel Corporation, Hillsboro, OR.

Gate oxide is arguably the most critical part of contemporary metal-oxide-semiconductor field effect transistors (MOSFET). Continuous improvement in device performance requires further scaling of gate oxide to achieve desired drive current. Oxide thickness has reached a level where the properties of Si oxide is determined by the interfacial suboxide, which is very different from the bulk oxide in terms of structural, electrical and optical properties. Thus a good understanding of gate oxide both structurally and electronically is of paramount importance for its application in future transistors. In this work we present a comprehensive study of subnanometer gate oxide in MOSFET using atomic resolution Z-contrast imaging coupled with spatially resolved electron energy loss spectroscopy (EELS) in the scanning transmission electron microscope (STEM). Interface composition, roughness, and strain are characterized and correlated to its electrical properties and electronic structure. Here we report an existence of local interface strain between Si and SiO_2 and provide a quantitative characterization in terms of the maximum atomic displacement and the spatial extent. EELS analysis of Si $L_{2,3}$ and oxygen K edges across the ultrathin gate oxide provided information on the spatial extent of the suboxides, dielectric properties of the

oxide and leakage current. A presence of pronounced but not overlapping interfacial states were identified.

B7.2
DEVICE SCALING EFFECTS ON SUBSTRATE ENHANCED DEGRADATION IN MOS TRANSISTORS. Nihar R. Mohapatra, Souvik Mahapatra, V. Ramgopal Rao, Department of Electrical Engineering, Indian Institute of Technology Bombay, INDIA; Bell Laboratories, Lucent Technologies, NJ.

Recently enhancement of electron injection with reverse substrate bias (V_{sub}) is observed due to impact ionization feedback mechanism, which is helpful for realizing fast and low power non-volatile memories. The reduction of L_{eff} and T_{ox} of the transistor affects the internal electric field distributions and hence carrier heating and injection process. The damage creation and the resulting device degradation thus become a strong function of device dimensions and therefore merit attention. Till date, no work has been done to study the effect of device scaling on the degradation with negative V_{sub}. In this paper, we have studied the reliability issues of n-channel MOS transistors having different L_{eff} and T_{ox} for different reverse V_{sub} under identical bias and gate current (programming time for flash memories) condition. The L_{eff} dependence studies are performed on devices having T_{ox} of 9nm. The T_{ox} dependence studies are performed on devices having L_{eff} of 0.2 μm. With increase in negative V_{sub} impact ionization feedback occurs, which increases carrier heating therby gate current. Also, for higher nagative V_{sub} the injected carriers are not confined to a narrow zone but spread out. We observe an increase in ΔN_{it} and ΔG_m by 1.16 and 1.72 when the device is stressed at V_{sub}=-2V. The higher ΔG_m can be attributed to an increased spread of interface trap profile. With a decrease in L_{eff} from 0.4μm to 0.1μm, ΔN_{it}, I_{sub} and ΔG_m are increased by a factor of 4.3, 2.31 and 2.88 respectively for V_{sub}=0 and by a factor of 3.7, 3.08 and 1.98 for V_{sub}=-2V. This is because if L_{eff} of a MOSFET is reduced at a constant bias, the E_{lat} increases whereas the E_{tran} decreases due to higher SCEs. Since the injection and therby degradation at negative v_{sub} has a very strong dependence on E_{tran}, it is less sensitive to L_{eff}. With reduction in T_{ox} from 13nm to 5nm, we observe higher I_{sub} and degradation for V_{sub}=-2V. The increased I_{sub} can be attributed to large number of secondary holes in the substrate and the higher degradation is due to higher gate injection and larger spread of interface trap profile. We have also studied the degradation for different L_{eff} and T_{ox} under constant gate injection and generation efficiency.

B7.3
USE OF SMALL GATE VOLTAGE PULSES FOR THE EXTRACTION OF THE INTERFACE TRAPS DENSITIES IN MOS STRUCTURES USING THE CHARGE PUMPING TECHNIQUE. E. Lin, E. Moussy, and D. Bauza, Laboratoire de Physique des Composants Semiconducteurs, UMR CNRS 5531, ENSERG, Grenoble, FRANCE.

In MOS structures with ultrathin oxides, the determination of the interface trap densities, D_{it}, with conventional interface trap characterization techniques is difficult due to the small gate voltage excursions allowed before Fowler-Nordheim injection or direct tunneling through the insulator. Using charge pumping (CP), the most widely used technique for interface trap characterization, large gate voltage pulses imply such currents. The use of high frequencies to increase the CP current magnitude has been proposed [1]. In this paper, small gate pulses are proposed for the extraction of D_{it}. They strongly limit the leakage currents and extend the experimental conditions which can be used (the frequency can also be used to increase CP signal magnitude). For this, and as the theoretical derivations that allow the extraction of D_{it} also require large gate pulses (pulses larger than $(V_{th} - V_{fb})$, where V_{th} and V_{fb} are the device threshold and flat band voltage) [2], the extraction D_{it} is extended to the case of small gate pulses, i.e. pulses smaller than $(V_{th} - V_{fb})$. To this end, the theoretical derivations are re-considered in order to account for both emission and capture in various situations. This provides equations that 1) more accurately describe the CP current when large gate pulses are used, 2) generalize the description of the CP current to a wide range of situations including reduced high and/or low bias levels and the effect of small trap cross sections and 3) allow D_{it} to be calculated whatever the gate pulse is. These results are applied for characterizing MOS device with thick and ultrathin oxides. To this end, and with respect to the above results, the large distribution of trap time constants evidenced at the interface cannot be overlooked when using small gate pulses and only a fraction of the interface traps is expected to be probed [3]. The interface trap densities measured, effectively decrease when reducing the pulse height, especially for height values smaller than $(V_{th} - V_{fb})$, but with pulse heights as small as $(V_{th} - V_{fb})/2$, that is $\approx$ 0.6 V, the D_{it} values obtained are within a factor of two equal to those measured conventionally. This is a fully acceptable result if one accounts for all the uncertainties on the determination of D_{it} (for instance, the differences between the values obtained using different characterization techniques). [1] P. Masson, J.L. Autran, and J. Brini, IEEE Electron Device Letters 20, 92 (1999). [2] Van den Bosch et al. IEEE Trans. Electron Devices 38, 1820 (1991). [3] D. Bauza and Y. Maneglia, IEEE Trans. Electron Devices 44, 2262 (1997).

B7.4
THE SOLUTION OF GOI IMPROVEMENT ON HIGH VOLTAGE DEVICE. S.Y. Ku, H.M. Guan, Y.F. Tsay, Y.J. You, Taiwan Semiconductor Manufacturing Co. Ltd., Hsin-Chu, Taiwan, ROC.

The thicker thickness of gate oxide is required to make sure the product can work on high voltage condition. However, the traditional dry oxidation method can't meet the testing requirement. The aim of this paper is to provide a quality method to produce a high quality gate oxide for mass production. There are three process factors were studied for this gate oxide quality improvement on dual voltage product. The first gate oxide is to form a thick oxide and then a thin oxide. The brief summary on thick oxide (dominator for HV product) as list: 1) Oxidation methodology. The low temperature (850C) and three steps (dry-wet-dry) get the better VBD performance than 920C/800C or two steps (dry-wet) conditions. The mechanism is annealing, deweling bond and crystal original pits effect. 2) Stack gate formation methodology. The prior gate oxide forming method changed from oxidation to LPCVD is considered. HTO replaces dry-wet-dry oxidation will get better VBD result. It is believed COP effect. But, TEOS didn't have the similar result since carbon element impact. 3) Wafer material source. Above two experiments were done on CZ polish wafers. AR anneal wafer performance is slightly better than H2 anneal wafer, but both anneal wafers' performances are better than polish wafer. According the studying above, COP effect plays the major dominator of the gate oxide quality on high voltage devices. Oxidation method, stack gate formation and wafer material are pointed out the advantages and shortages. This paper provides some solutions on gate oxide quality improvement for mass production.

B7.5
DEGRADATION IN A MOLYBDENUM GATE MOS STRUCTURE CAUSED BY N^+ ION IMPLANTATION FOR THE WORK FUNCTION CONTROL. Takaaki Amada, Nobuhide Maeda, Kentaro Shibahara, Research Center for Nanodevices and Systems, Hiroshima Univ., Hiroshima, JAPAN.

Work function control technique of the Mo gate by annealing or N^+ ion implantation has been reported by Ranade et al.[1] with the aim of dual work function CMOS fabrication with a single metal material. We also fabricated the Mo gate MOS diodes with 5-20 nm SiO_2 gate oxides and found that the gate leakage current were increased as N^+ implantation dose and implantation energy were increased. Though work function shift was observed in C-V characteristics, the hump due to the high-density interface states was found for high-dose specimens. Nitrogen SIMS depth profile showed that nitrogen was implanted much deeper than calculated depth obtained by SRIM simulator. Channeling of the N^+ ions implanted nearly vertically (7 degrees) into columnar crystal structure Mo film is the considerable origin of this deep profile. To reduce N^+ ions that pass through the gate oxide, we have compared angled implantation with the nearly vertical one. In the case of tilt angle of 30 degrees, the gate leakage current was reduced compared with the 7 degrees case. Since the decrease in projected range of N^+ ions for the 30 degrees angled implantation is only 15%, the deep profile and gate leakage increase seems to be attributed to the channeling effect. [1] P. Ranade et al., MRS Symp., Vol. 611. 2000. C3.2. 1 Acknowledgement: Part of this work was supported by STARC (Semiconductor Technology Academic Research Center).

B7.6
ELECTRICALLY INDUCED JUNCTION MOSFET FOR HIGH PERFORMANCE SUB-50NM CMOS TECHNOLOGY. A. Dixit[a], R.O. Dusane[b], V. Ramgopal Rao[a], [a]Department of Electrical Engineering, Indian Institute of Technology Bombay, INDIA; [b]Department of Metallurgical Engineering and Materials Science, Indian Institute of Technology, Bombay, INDIA.

An electrically induced junction MOSFET (EJMOS) is different from conventional CMOS device in that the shallow source/drain (S/D) junctions are electrically induced by the gate voltage. In such a device the shallow extensions are underneath the gate and contain low doped regions of opposite conductivity as that of deep S/D. In order to turn ON the device a voltage is applied at the gate of a EJMOS, such that these low doped regions below poly gate get inverted and serve as shallow S/D extensions. Consequently, the effective channel length in this condition is the distance between these low doped regions. On the contrary, at any gate voltage less than that required to invert these regions, no S/D extensions are induced, and the effective channel length is equal to the physical separation between the deep S/D junctions. Our proposed structures also reduce the series resistance

effects when compared to the recently published devices based on a similar concept.
In this work, we compare 45nm gate length EJMOS and conventional devices using ISE-TCAD process and device simulations. In the EJMOS process, shallow extension regions under the gate are achieved by a compensation doping using a large angle tilt implant from both source and drain sides, after patterning the gate. The resulting MOSFET is symmetric in nature and can be fabricated using conventional CMOS processes.
From extensive 2-D process and device simulations, we observe over an order of magnitude increase in Ion/Ioff, improved sub-threshold characteristics, and better short-channel performance. Overall, as our simulation results show, the EJMOS structure offers significant advantages over the conventional CMOS technologies in the sub-50nm regime.

B7.7
APPLICATIONS OF AFM/SCM IN PROCESS CONTROL AND FAILURE ANALYSIS OF SEMICONDUCTOR DEVICES.
Kuo-Jen Chao, J.R. Kingsley, H. Ho, H. Shen, I. Ward, Pat Lindley, Charles Evans & Associates, Sunnyvale, CA.

As the minimum feature size of semiconductor devices continues to shrink, analyses of the engineered structures and materials of semiconductor devices are increasingly critical in manufacturing and in the development of new generation devices. Furthermore, the performance of a modern device is strongly influenced by its dopant distribution in depth and laterally. Scanning capacitance microscopy (SCM) is one of the techniques that has been developed to reveal the dopant distribution two-dimensionally. In this work, AFM/SCM was applied to both process control and failure analysis of semiconductor devices. Two types of semiconductor devices, Si based and GaAs based, were studied. In the process control area, two examples are presented. The first investigates the uniformity of an arsenic layer of a silicon substrate. This sample has a layer that is supposed to consist of uniformly distributed As. A cross-section SCM/AFM study found local non-uniformity in the As layer. In the second example, the lateral diffusion length of dopants after a thermal annealing process is evaluated. A GaAs substrate is masked and patterned by a layer of Si_3N_4, then Zn dopants are thermally diffused through a line-opening in the nitride layer into the substrate. By overlaying the AFM image on top of the SCM image, the lateral diffusion length of the Zn dopants is found to be about 2.2 μm away from the edges of the exposed GaAs region. Another important application of AFM/SCM is in device failure analysis. In this work, a failed p-channel transistor is investigated by AFM/SCM. Two levels of dopant concentration are found in the correspond-ing source and drain regions by SCM. Another approach to identify the cause of failures is to directly compare a failed device with a properly functioning one. The use of AFM/SCM to study the same N-well structures in two devices, one good and the other failed, determined that the depth of the N-well for the failed device is about 0.4 μm shorter than in the good device.

B7.8
SILICON SURFACE CHEMICAL TREATMENTS IN OXIDE/ NITRIDE DIELECTRIC STACK PROPERTIES.
David Jacques, Sebastien Petitdidier, Jorge L. Regolini, Kathy Barla, STMicroelectronics, Crolles, FRANCE.

The "oxide" terminated silicon surface may be chemically grown through several methods compatible with the ULSI technologies. These methods are not equivalent when used to grow thin oxide (SiO2)/nitride (Si3N4) stacks as a dielectric for memory cells. In the present work we studied the dielectric oxide/nitride (ON) stack electrical performances after different chemical surface treatments of the Si starting material through dielectric leakage current and charge to breakdown measurements on the ON stack on single crystal Si (<Si>)and in Poly-Si substrates. Three main steps are followed to obtain the complete ON stack: (i) the wet chemical surface treatment. Two main reasons lead us to use a chemical step before the stack deposition: surface cleaning and surface passivation. The RCA cleaning, the ozonised water DIW/O3, and the HF last were independently used. (ii) the surface nitridation. The chemical oxides have been thermally nitridated transforming the lying oxide into some SiOxNy layer over which the SiN will be deposited. (iii) the nitride deposition. SiN 5 nm thick was deposited using DCS/NH3 gas mixture, below 1 Torr total pressure and at 650°C in a batch vertical furnace. Morphological results such as stack surface roughness (Atomic Force Microscopy) and SiN incubation time for growth are comparable for all the studied cases on <Si>. However, Tof-SIMS shows different oxygen content at the Si/stack interface following the different chemical treatments. Electrical measurements show comparable C-V and I-V results, for the same Equivalent Oxide Thickness (same capacitance at strong accumulation) the different interfaces bring different interface states density with lower values for higher interfacial oxygen content. However, for DRAM applications, a clear improvement in electrical characteristics is obtained under low interfacial oxygen content conditions. Results are compared in embedded-DRAM cells for which we developed an industrially compatible dielectric deposition sequence to obtain minimum leakage current with maximum specific capacitance and no particular linking constraints.

B7.9
DEVICE QUALITY SiO_2 FILMS BY LIQUID PHASE DEPOSITION (LPD) AT 48°C.
Meenakshi Manhas, T.J. Pease, R. Cross, S.C. Bose, D.P. Oxley, M.M. De Souza, E.M. Sankara Narayanan, Emerging Technologies Research Centre, De Montfort University, The Gateway, Leicester, UNITED KINGDOM.

We describe the preparation, properties and the comparison of SiO_2 films deposited by liquid phase deposition from supersaturated solutions with both silica powder and silicic acid. From both the solutions the resulting [Si $(OH)_4$]-rich supersaturated solution, when suitably diluted with De-Ionised (DI) water deposits SiO_2 onto silicon [1]. Our work was motivated by the search for the conditions for the optimum condition for device quality oxide growth within a low (<300°C) thermal budget, for large area device fabrication, on inexpensive substrates such as glass and plastic. The net growth of the LPD oxide layer is result of competition between deposition and etching; the balance and hence the rate of growth being controlled simply and reproducibly by the addition of de-ionised (DI) water [2]. We have produced device grade SiO_2 from the solution at 48°C onto both n and p type Si substrates. Control of the oxide properties is achieved in the amount of DI water added to the super-saturated solution. Oxide layers of optimum quality being obtained by the titration of 60ml DI water to 100ml of supersaturated solution. FTIR, ellipsometery, and C-V/I-V measurements were used to characterise the films deposited from solutions of silica powder and silicic acid. The resistivity of the optimum layers from a saturated solution of silica powder was found to be in excess of $\approx 10^{11}$ $\Omega\cdot$cm with breakdown field strengths of the order of 3-5 x 10^6 V/cm. The resistivity of the optimum layers prepared using silicic acid were much higher (10^{15} $\Omega\cdot$cm), with breakdown field strengths of the order of (9$\pm$1) x 10^6 V/cm. The results approach those of thermally grown silicon dioxide, suggesting that LPD oxide have the potential of device quality insulator on large area substrate such as glass and plastic.
References [1] C.F. Yeh et. al., IEEE Electron device letters, vol. 14, No. 8, Aug. 1993. [2] Ching-Fa Yeh et. al. J. Electrochemical Soc., 141(11), pp. 3177-3181, 1994.

B7.10
DEVELOPMENT OF SPIN-ON PRE METAL DIELECTRICS (PMD) FOR 0.11UM DESIGN RULE AND BEYOND.
Zhongtao Li, Xiaobing Zhou, Dave Wyman, Mike Spaulding, Ginam Kim, Stelian Grigoras, DK Choi, Eric Moyer Semiconductor Fabrication Materials, Dow Corning Corp., Midland, MI.

Spin-on pre metal dielectric (PMD) materials are being developed for memory and logic devices at 0.11 um design rules and beyond. The stringent design rules require a PMD material with a low thermal budget, excellent gap fill capability, and etch resistance similar to that of a thermal oxide. A novel Spin-on PMD has been developed to meet these requirements as current PMD technologies of HDP CVD or BPSG are constrained by void formation and high thermal budget requirements. One common challenge that faces spin-on PMD is inhomogeneous densification, or "corner etch". In this paper EELS-STEM, FTIR, SEM and HF wet etching were used to study the mechanism of this phenomenon. Optimization of the spin-on PMD resin based on this information will be presented.

B7.11
THE OPTIMIZATION OF UNIT PROCESSES IN A INTER LAYER DIELECTRIC APPLICATION USING NOVEL POLYSILAZANE-BASED SOG.
Jung-Ho Lee, Jung-Sik Choi, Dai-Won Kang, Dong-Jun Lee, Sang-Moon Chon, Samsung Electronics Co., LTD., Material Technology PJT, Kyunggi-Do, KOREA.

Currently borophosphosilicate glass (BPSG) has been widely used to integrate the inter layer dielectric (ILD) to fill gaps between word lines. However, there are a lot of problems in using BPSG for manufacturing very large scale integration (VLSI) devices. To solve these problems, a novel polysilazane-based spin on glass (SZ-SOG) method is evaluated to apply to in ILD layer. In this paper, the unit process conditions were optimized. The main spin revolution was fixed at 1000rpm, because when the film was prepared lower than 1000rpm caused crack problem after the main bake, and the film under high rpm condition had no enough thickness margin for chemical mechanical polishing(CMP). When SZ-SOG was coated, edge bead removal(EBR) process was used to minimized micro-scratches and defects due to particles provoked from wafer bevel. The pre-bake temperature was selected in the range from 150 to 200°C to keep flowability property of neat polymer. Finally, SZ-SOG must be formed not only of perfect silica film but also a dense film through the main

bake step to successfully achieve integration in ILD layer. To prepare a dense and defect free SZ-SOG film, the furnace loading temperature must be kept below 500°C and ramping rate below 20°C/min in the main bake step. When the furnace loading temperature and ramping rate were higher than 500°C and 20°C/min, respectively, there were a crack and lifting problems due to sudden surface oxidation. Consequently, the unit processes of SZ-SOG in ILD application were successfully optimized for the first time. The proposed SZ-SOG could be attractive in applications such as future DRAM and LOGIC device because of its excellent gap-filling property and thermal oxide like film qualities.

B7.12
CHARACTERIZATION OF CVD LOW-k α-SiCO:H FILMS PREPARED FROM TRIMETHYLSILANE. Hae-Jeong Lee, Eric K. Lin, Barry J. Bauer, Wen-li Wu, National Institute of Standards and Technology, Polymers Division, Gaithersburg, MD; Byung Keun Hwang, William D. Gray, Electronics Industry & Advanced Materials Business, Dow Corning, USA.

In next generation devices, increases in propagation delay, cross-talk noise, and power dissipation of the interconnect structure become limiting factors for integrated circuits. To address these problems, new low dielectric constant (low-k) interlayer dielectric materials prepared by both spin-on and chemical vapor deposition (CVD) techniques are being developed to replace the traditional silica. Low-k CVD films have attracted interest due to their physical rigidity, superior mechanical strength, and compatibility with current Si technology. One of the candidates for CVD low-k thin films is trimethylsilane (3 MS) based carbon doped silica film (α-SiCO:H). This precursor material is attractive because films with dielectric constants ranging from 2.5 to 3.5 can be obtained using typical plasma enhanced chemical vapor deposition (PECVD) equipment with standard delivery system and process conditions that are comparable to SiH_4 based SiO_2. In this work, we characterize the structure of Dow Corning Z3MS based α-SiCO:H low-k thin films deposited with different processing conditions. Samples with dielectric constants ranging from 2.5 to 2.9 were prepared using single or dual frequency modes with different oxidants, O_2 or N_2O. X-ray porosimetry is employed to characterize the porosity, average density, wall density and density profile of the thin films. These results are compared with those from a combination of three techniques, small angle neutron scattering (SANS), high-resolution specular X-ray reflectivity (SXR), and ion scattering. The influence of the process conditions on the chemical bonding structures and electrical properties were investigated using Fourier transform infrared (FTIR) spectroscopy and electrical measurements.

B7.13
CHALLENGES IN ETCHING OF OSG LOW-k MATERIALS FOR DUAL-DAMASCENE METALLIZATION. Vladimir N. Bliznetsov, Moytreyee Mukherjee-Roy, Leong Yew Wing, Yew Wee Chuan, Institute of Microelectronics, Dept Deep Submicron Integrated Circuits, SINGAPORE; Ng Beng Teck, National University of Singapore, Dept Material Science, SINGAPORE.

Issues associated with OSG low-k dual damascene etching and in particular with trench etching in the “via first” integration scheme is the focus of this study. Usually during trench etch three basic requirements should be met simultaneously. These are profile control, selectivity to barrier layer and minimal post-etch residues. The high hydrocarbon content in OSG films makes it more difficult to achieve these as compared to conventional USG films. Moreover, if trench stop-layer is not used additional issues such as micro-trenching, across-wafer non-uniformity, micro-loading, and RIE lag may appear. This study was done mainly on Black Diamond^{TM} of Applied Materials with some comparison to Coral^{TM} of Novellus. TEL dipole-ring-type magnetron etcher was used for etch development based on $C_4F_8/N_2/Ar$ plasma. After preliminary screening experiments in-depth DOE was performed which gave the dependence of OSG etch rates, selectivity to barrier layers, sidewall slope, RIE lag, micro-loading and non-uniformity versus three key process parameters: flow rates ratio C_4F_8/N_2, plasma power, and pressure. Based on experimental outcomes, the etching process was further optimized to realize sidewall profiles of 88-89°, minimized non-uniformity, RIE lag, and micro-loading. Selectivity obtained was enough to pursue etch processes using planarizing BARC for additional via bottom protection. The BARC process was tuned using different types of BARC. Viscosity of BARC and fill depth in vias were optimized for obtaining an optimal thickness for bottom protection and generating the least amount of polymers during etch. BARC opening time was fine-tuned accordingly. Different combinations of dry/wet clean recipes were evaluated for removal of post-RIE residues without significant changes in OSG k-value. The sequence of optimized processes were successfully implemented for creating dual damascene structure complying with integration requirements for 0.13 design rules.

B7.14
ONE FORCE DRIVING Cu DIFFUSION INTO INSULATOR. T. Fukuda, H. Nishino, A. Matsuura, H. Yanazawa, H. Itoh, Environmental Process Technology Lab., Association of Super-Advanced Electronics Technologies (ASET), Yokohama, JAPAN.

This study is part of Japanese national project to develop a PFC-free and energy-saving ILD (interlayer dielectric) process. In this project, we have also been investigating novel ILD processes that do not require a barrier film to prevent Cu diffusion. Thus, a clear understanding of the mechanism by which Cu diffuses into an ILD is essential. A simulated potential energy shows that when Cu penetrates SiO2, it must be converted to Cu+. One possible driving force is Schottky defects (crystal defects). The estimated current density was less than 3 E-24 A/cm2 (Observed value > 1 E-12). From this value, it is clear that diffusion through defects is not the dominant process. The current density of a Cu-electrode/TEOS/Si structure was measured with a probe in a vacuum chamber, which allowed the ambient conditions to be controlled. The lowest current density was obtained when degassed TEOS formed by vacuum annealing was used and the I-V characteristics were measured just after deposition of the Cu electrodes. The current density was found to be the same exposed to N2, though it did increase after exposure to dry air. It should be noted that degassed TEOS film contains hardly any water or oxygen molecules. In contrast, conventional TEOS not subjected to annealing contains both, and samples made with this material exhibited the highest current density. These results demonstrate that Cu diffusion occures when TEOS is exposed to oxygen or TEOS contains oxygen molecules. Atomic Cu has a magnetic moment, and oxygen molecules exhibit strong paramagnetism. The interaction between the magnetic moments of Cu and O2 lowers the potential. That means that the interaction allows Cu to diffuse easily into TEOS. Samples made with conventional TEOS were divided into two groups just after formation of the Cu electrode. One set was kept in a magnetic field for 2 days, and the other set was kept in air. The samples kept in a magnetic field exhibited lower current densities than the others. This demonstrates that one cause of Cu diffusion into an insulator is the presence of O2 in the insulator. Acknowledgments: This work was performed under the management of ASET in a METI R&D program supported by NEDO.

B7.15
CHARACTERIZATION OF POLY(SILSESQUIOXANE) SPIN-ON FILMS FOR LOW DIELECTRIC APPLICATIONS: MICROSTRUCTURE, ELECTRICAL PROPERTIES AND MECHANICAL PROPERTIES. Jingyu Hyeon-Lee, Yi Yeol Lyu, Sang Kook Mah, Jin-Heong Yim, Hyun-Dam Jeong, Samsung Advanced Institute of Technology, E-Polymer Laboratory, Taejon, KOREA; Mong Sup Lee, Sang Youl Kim, Korea Advanced Institute of Science and Technology, Dept of Chemistry, Taejon, KOREA.

We studied the effect of porogen content on the film properties of porous poly(silsesquioxane) material. Organic/inorganic nanohybrids were prepared by using a thermally labile poly(caprolactone) as a template, and SOG silsesquioxane polymer as a matrix material. Thermal decomposition of the organic polymer resulted in nanoporous films. It is found that the dielectric constant depended on the porogen content and hardness and modulus of the thin film were affected by the porogen content. The thin films had dielectric constant of 2.2 with good mechanical strength.

B7.16
EVALUATION OF LOW-k POLYMER THIN FILM CONTAINING BORAZINE-UNIT. Masami Inoue, Takuya Fukuda, Azuma Matsuura, Hiroshi Yanazawa, ASET, Yokohama, Kanagawa, JAPAN; Yuko Uchimaru, Naoko Koda, Hiroshi Yamashita, AIST, Tsukuba, Ibaraki, JAPAN.

It was predicted that the polymers containing borazine unit were low-k materials, because a dielectric constant was simulated by both molecular polarizability and number of molecular in a unit volume through the help of the molecular orbital and band calculations. Two hybrid polymers containing borazine unit, such as borazine-carbosilane unit and borazine-siloxane unit, were evaluated on electric characteristics. These polymers were synthesized by hydrosilylation polymerization of B,B$'$,B$''$-triethynyl-N,N$'$,N$''$-trimethylborazine with p-bis(dimethylsilyl)benzene or tetramethylcyclosiloxane. Polymerization under diluted conditions gave a homogenous solution of the polymer. From an ethylbenzene solution, a thin homogeneous films of the polymer were made on a silicon wafer by spin-coating method, followed by annealing at 300~500°C under argon gas. The dielectric constants of these thin film were evaluated to be 2.8~1.8, which depend on these compositions and annealing conditions, by measurement of C-V curves from MIS structure sample. The thermal resistance was good, because the temperature of weight decreasing to

5% was 563°C by the TGA method. Therefore, it has been demonstrated that the polymer containing borazine unit is very promising as ultra low-k material. The New Energy and Industrial Technology Development Organization supported this work.

B7.17
UNUSUAL STRENGTH-POROSITY RELATIONSHIP OF NANOPOROUS MSSQ FILMS CHARACTERISED BY BRILLOUIN LIGHT SCATTERING AND SURFACE ACOUSTIC WAVE SPECTROSCOPY. C.M. Flannery, Paul Drude Institute for Solid State Electronics, Berlin, GERMANY; T. Wittkowski, Physics Department, University of Kaiserslautern, GERMANY; M.R. Baklanov, IMEC, Leuven, BELGIUM.

Nanoporous aerogel films present perhaps the best candidate for low dielectric constant materials for microelectronic interconnect with reduced RC factor. It is becoming increasingly clear that the drastically reduced stiffness properties of porous films limit their introduction for commercial purposes. Thus, a compromise must be reached between low k value and sufficient mechanical strength for the material to survive the chemical mechanical polishing process. There is also a lack of useful and accessible techniques which can accurately provide absolute values of the most important film parameters (density/porosity, Youngs modulus, pore size) suitable for process control. This work reports characterization of density/porosity and Young's modulus values of a range of polymer-based nanoporous Methylsilsesquioxane (MSSQ) films via two independent techniques, Brillouin Light Scattering (BLS) and Surface Acoustic Wave Spectroscopy (SAWS), which have not previously been applied to such films. The films had template concentrations of 1% to 30%, corresponding to porosities of 14% to 40%. These have the advantage of being hydrophobic and having a lower dielectric constant than silica-based aerogels. Excellent correlations are observed between measured density, porosity and X-Ray derived density measurements. The extracted stiffness measurements from BLS and SAWS also correlate very well. The strength dependence on porosity shows that the films are soft (E = 2 GPa) at low porosity, but that, in comparison to silica aerogels, the strength properties decrease much more slowly with increasing porosity, so that in the k<2 region they may be stronger than the silica aerogel films and therefore may be more suitable for commercial application. Thus these techniques represent reliable methods to extract absolute values of critical properties of nanoporous films and reveal unusual strength-porosity behaviour of nanoporous MSSQ.

B7.18
RELATIONSHIP BETWEEN ELECTRICAL PROPERTY AND STRUCTURE OF POROUS SiOC FILM WITH LOW DIELECTRIC CONSTANT. Yoon-Hae Kim and Hyeong Joon Kim, Seoul National Univ, School of Materials Science and Engineering, Seoul, KOREA; Hae-Jeong Lee and Jin Yong Kim, Eric K. Lin, Barry J. Bauer and Wen-li Wu, NIST, Materials Science and Engineering Laboratory, Gaithersburg, MD; Young Lee, Jusung Engineering Ltd, R&D Division 3, Kyunggi-Do, KOREA.

As ultralarge scale integrated circuits (ULSIs) are reduced in size to deeper sub-micron dimension, there has been a strong demand for low dielectric constant inter-metal dielectric materials instead of SiO_2 that is conventionally used to improve the performance of devices, such as signal propagation delay, cross talk, and power consumption. Recently, SiOC, which is hybrid between organic and inorganic materials, is very promising inter-metal dielectric, since it has higher thermal and mechanical stabilities than organic materials as well as low dielectric constant. Despite many researches, the reasons for increasing dielectric constant upon carbon incorporation remain under debate. Generally, it is accepted that the carbon incorporation in the Si-O network leads to the porous structure and the decrease of film density results in the decrease of dielectric constant. In this investigation we focused on the electrical properties affected by porosity and wall density of SiOC film. The methodology we develop is a combination of high-resolution x-ray reflectivity (HRXR), and time-of-flight elastic recoil detection (TOF-ERD) to determine important structural information about the film. X-ray reflectivity measurement provides an accurate determination of the film thickness, electron density, and average film density. The dielectric constant is calculated from capacitance-voltage (C-V) measurement at 1MHz. The (average) film density was reduced with increasing of carbon content incorporated in film, resulting in the decrease of dielectric constant of SiOC film. Though the average film density was reduced by incorporating of carbon in film, the porosity was almost unchanged. On the other hand, matrix wall density was drastically reduced with increasing of carbon content. This result indicates that low dielectric constant of SiOC film results from the decrease of matrix wall density by incorporating carbon in film.

B7.19
MODIFICATION OF LOW-k MATERIALS FOR ULSI MULTILEVEL INTERCONNECTS BY ION IMPLANTATION. Alok Nandini U. Roy, G.S. Shekhawat, R. Geer, Katherine Dovidenko, Eric Lifshin, H. Bakhru, State University of New York at Albany, Dept of Physics, Albany, NY; A. Mallikarjunan, A. Kumar, J. Fortin, T.-M. Lu, Rensselear Polytechnic Institute, Center for Integrated Electronics and Electronics Manufacturing, Troy, NY.

Thin films of xerogel and SiLK (Low-k materials) were implanted with argon, nitrogen and helium etc. with 2E15 and 1E16 doses at energies varying from 50 to 150 keV at room temperature. In this work we discuss the improvement of hardness as well as elasticity of low k dielectric materials by ion implantation. Ultrasonic Force Microscopy (UFM) and Nano indentation technique have been used for qualitative and quantitative measurements respectively. The hardness increased with increasing ion energy and dose of implantation. For a given energy and dose (fluence), the hardness improvement varied with ion species. Dramatic improvement of hardness is seen for multi-dose implantation. Characterization of xerogel and SiLK using Ion beam technique will be presented.

B7.20
STUDY OF POROUS SILICA BASED FILMS AS LOW-k DIELECTRIC MATERIAL AND ITS INTERFACE WITH COPPER METALLIZATION. I. Fisher, M. Eizenberg, Dept. of Materials Engineering, Technion-Israel Institute of Technology, Haifa, ISRAEL; M. Nault, and T. Weidman, Applied Materials, Santa Clara, CA.

The success of future gigascale integrated circuit (IC) chip technology depends critically upon the reduction of the interconnect RC delay time. This calls for the development of new low dielectric constant insulators, and on their integration with lower resistivity copper metallization. Porous silica based film prepared by surfactant templated self-assembly spin-on deposition is an attractive candidate as a low-k material. In this research we have studied the structure, the chemical composition and bonding of the film and its interface with copper metallization. The decomposition and vaporization of the surfactant in the last step of the film deposition results in a film with an amorphous structure as determined by X-ray diffraction and TEM analysis and its high porosity (35-55%) is confirmed by X-ray reflectivity measurements. XPS analysis of the Si2p transition indicates three types of bonding: Si-O, O-Si-C and Si-C. The effect of various plasma post-treatment processes (evaluated to improve hardness and adhesion) on the film topography and bonding was determined by AFM and XPS, respectively. It was found that direct H_2 plasma exposure exerted a significant effect of surface roughness of the film (rms 111Å; avr 87Å) and bonding type (higher Si-O vs. Si-C bonding percentage). The structure and properties of various PECVD deposited capping layers were also studied, as was the interface between the porous dielectric and Ta, Ta_xN (PVD deposited diffusion barriers) and Cu after annealing at 200-700°C. The 200°C and 500°C annealing treatments did not indicate any diffusion of Cu or Ta into the porous film, as determined by AES and SIMS. However the 700°C anneal resulted in complete Cu penetration into the porous film, when deposited directly on it, whereas when a thin (~50Å) Ta_xN/Ta diffusion barrier layer was interposed between the Cu and the porous film, the Cu penetration was insignificant.

B7.21
SURFACE PROPERTIES OF LOW-k HYBRID-ORGANIC-SILOXANE-POLYMER (HOSP) FILMS ETCHED WITH IONS OF DIFFERENT INCIDENT ANGLES IN CHF_3 PLASMA. Sung-Wook Hwang, Gyeo-Re Lee, Jae-Ho Min, Sang Heup Moon, Seoul National University, School of Chemical Engineering and Institute of Chemical Processes, Seoul, KOREA; Yu Chang Kim, Hyun-Kyu Ryu, Yun Seok Cho, Jin Woong Kim, Hynix Semiconductor Inc, Memory R&D Division, Kyoungki-do, KOREA.

Hybrid-organic-siloxane-polymer (HOSP), a representative spin-on-glass low-k material, was etched in CHF_3 plasma while ions were incident on the substrate surface at specified angles under the practical conditions of plasma etching. HOSP films contacting another HOSP bottom surface at different angles were placed in a Faraday cage, which allowed ions to travel in a pre-determined direction independent of the substrate alignment in the cage, and then the films were etched in CHF_3 plasma at 5mTorr while the bias voltage was varied between -100V and -400V. As a whole, the etch yield, defined as the etch rate/incident ion, showed a cosine dependency on the ion angle. However, the etch yield slightly deviated to higher values from those predicted by the cosine-dependency curve when the ion angle was lower than 80°, and fell below the cosine curve at angles higher than 80°. To understand the different behaviors of the etch yield depending on the ion angle, we analyzed the film surface after etching at two different angles, 70° and 90°, representing the low and the high angle regions respectively. Atomic force microscopy (AFM), Auger electron spectroscopy (AES), and X-ray photoelectron spectroscopy (XPS) were used for the analysis. The surface of HOSP film was rougher after etching at 90° than at 70°, and the difference

in the surface roughness increased with the bias voltage. A thick fluorocarbon surface layer was observed on the HOSP film after etching at 90°, and the layer formation was enhanced at high bias voltages due to the redeposition of particles emitted from the bottom surface. When the HOSP film etched in CHF_3 plasma was subsequently exposed to O_2 plasma for ashing, the film surface became much rougher than before the exposure, except for when the film was etched at 70° and at low bias voltages.

B7.22
POLARITY DEPENDENCE OF DEGRADATION IN ULTRA THIN OXIDE AND JVD NITRIDE GATE DIELECTRICS. Yatin Mutha, K.N. Manjularani, J. Vasi, V. Ramgopal Rao, Indian Inst of Tech-Bombay, Mumbai, INDIA.

We have studied Jet Vapor Deposited (JVD) silicon nitride MNSFETs and compared their degradation under identical field conditions with conventional MOSFETs. The devices used in this study are n-channel transistors. The thickness of the gate dielectric is 3.9 nm for MOSFETs and 3.1 nm for nitrides. The technology used for both devices is same except the dielectric deposition process. Silicon nitride is deposited using jet vapor deposition technique, whereas the oxide is thermally grown at 850°C. In this work, the evolution of the interface state density N_{it} with stress for both nitrides and oxides is systematically investigated. Charge pumping method at 1 MHz is used to calculate N_{it}. We have observed that in both oxide and nitride device, the degradation is higher under negative gate polarity. Also, in case of nitrides, the degradation in N_{it} is always lower as compared to oxides for both positive and negative stressing. The results are analyzed in detail with the well-known hydrogen transport and trapped-hole recombination models. We conclude that trapped hole recombination is the more dominant mechanism of degradation. The devices under real operating conditions are subjected to bipolar or AC stress rather than DC conditions normally used for such degradation studies. This paper presents results using AC stress experiments on these ultra thin oxide and nitride MOS transistors. The frequency, peak-to-peak voltage and offset voltage of the applied AC signal are some of the parameters that are varied. Detailed characterization results and an analysis of the same will be presented.

B7.23
SYNTHESIS AND CHARACTERIZATION OF METHYL-TRIETHOXYSILANE BASED LOW PERMITTIVITY (LOW-k) POLYMERIC DIELECTRICS. Z. Gu, Department of Chemical Engineering; R. Jeyakumar, S. Sivoththaman, A. Nathan, Department of Electrical and Computer Engineering, University of Waterloo, Waterloo, Ontario, CANADA.

Low-permittivity (low-k) polymeric dielectrics are potentially very attractive as interconnection materials in a wide range of semiconductor structures. In this work, a low-k polymeric material has been synthesized using methyltriethoxysilane as base material, and the material properties have been characterized. The material synthesis was carried out using an experimental set-up that performed refluxing, hydrolysis, agitation, and polymerization steps. The final product is a high-flowing brownish liquid, that is spin-coatable to yield uniform films after coating and curing treatments. The film properties were studied by structural and electrical characterization. Test structures on silicon were fabricated to measure the dielectric constant (k) of the material. The values of k were found to be in the range of 1.9 - 2.7 (at 1 MHz) for annealing temperatures 250C - 450C. The annealed films as well as the initial material were found to be very stable. Fourier Transform Infrared (FTIR) spectroscopy was used for the structural characterization. Prominent peaks, (Si-CH3 stretch, Si-O stretch, Si-C, etc.) are are observed and their dependence on film annealing conditions as well as material formation conditions will be discussed. In addition to the electrical and structural properties of the films, the paper will also report on integration-related issues such as planarization, film-stress, etc. (ref: Yamada et al., J. Electrochem. Soc. Vol. 147, p. 1477, 2000).

B7.24
EFFECT OF ION-ACCELERATED PLASMA HYDROGENATION AND THERMAL TREATMENTS ON HYDROGEN SILSESQUIOXANE (HSQ) LOW-k DIELECTRIC FILMS. R. Jeyakumar, L. Ren, and S. Sivoththaman, Electrical and Computer Engineering, University of Waterloo, Waterloo, Ontario, CANADA.

Hydrogen silsesquioxane (HSQ) is a very promising polymeric dielectric with a low permittivity(k). However, higher curing temperatures and presence of oxygen tend to increase the k. In this work, the effects of an ion-accelerated hydrogen plasma exposure, film annealing temperature, and annealing ambient on the permittivity and structural properties of HSQ low-k dielectric films have been investigated. Experiments were performed on test structures fabricated using spin-coated HSQ low-k films. The film curing temperature was varied from 275C to 575C. The k values were found to be increasing with increasing curing temperature, and stayed below 3.2 for temperatures up to 400C. Fourier transform infrared (FTIR) spectroscopy showed a reduction in intensity of Si-H peaks with increasing temperature. The presence of oxygen in the curing ambient was also found to have a strong influence on the dielectric constant as well as in the intensity of Si-H peaks with the reduction in Si-H peak intensities starting to occur at lower temperatures (<300C). When the cured films were subjected to an ion-accelerated hydrogen plasma treatment (250C, 13.56 MHz RF plasma, 45 minutes), a very significant reduction in k was observed for all curing temperatures. (up to 45 percent reduction in k). The paper will report on the dependence of electrical, structural, and mechanical properties of the HSQ films on different thermal and plasma treatments.

B7.25
USING CARBON NANOTUBE CANTILEVERS IN SCANNING PROBE METROLOGY OF INTEGRATED CIRCUIT STRUCTURES. Y.N. Emirov, University of South Florida, Center for Microelectronics Research; D.A. Walters, B. Metha, University of Central Florida, Physics Department; Z.P. Huang, Z.F. Ren, Boston College, Physics Department; B.B. Rossie, Agere Systems; and R. Schlaf, University of South Florida, Center for Microelectronics Research.

Carbon nanotubes (CNT) are among the candidates for atomic force microscopy probes for use in high aspect ratio critical dimension metrology (CDM). Their mechanical strength at small diameters makes them ideal high resolution probes for narrow and deep features. The synthesis of CNT has been making great progress in recent years. The use of CNT in scanning probe microscopy, however, has been limited due to a number of problems. While the CNT probes generally appear to be long lasting, the manufacture of precisely aligned CNT of defined length, diameter and number of walls poses a number of challenges. Yet, such precisely defined CNT probes appear to be required if the cantilevers are to be used for CDM. Our results demonstrate, for example, that the attachment angle of CNT with respect to the cantilever beam is crucial for their application in CDM. We report about our efforts to overcome these problems by growing well-defined CNT on standard Si cantilevers.

B7.26
A STUDY ON THE DRY THERMAL OXIDATION AND POST-ANNEALING OF A GRADED SiGe/Si HETEROSTRUCTURE. Jong Seok Jeong, Young Soo Lim, Jeong Yong Lee, Korea Advanced Institute of Science and Technology, Dept of Materials Science and Engineering, Daejeon, KOREA; Hong Seung Kim, Electronics and Telecommunications Research Institute, Microelectronics Technology Laboratory, Daejeon, KOREA; Dae Won Moon, Korea Research Institute of Standard and Science, Surface Analysis Group, Daejeon, KOREA.

Si/Ge strained heterostructures have been widely investigated for various applications in the field of electronic and optoelectronic devices due to the compatibility with well-known Si technology. We investigated the effect of dry thermal oxidation and post-annealing of a graded SiGe layer. To reduce the Ge pileup effect during the thermal oxidation, the SiGe layer was deposited with the graded composition of Ge. The composition and the microstructure of SiGe heterostructures were investigated using a secondary ion mass spectrometry (SIMS) and a transmission electron microscopy (TEM). After dry thermal oxidation at 900°C, the Ge composition in pileup layer was significantly reduced and strain relaxation by defect formation was prevented due to the graded Ge distribution. To homogenize the Ge distribution between pileup layer and remaining SiGe layer, the oxidized layers were post-annealed at 900°C, and thereby a SiO_2/SiGe interface with good structural properties was obtained. The homogenization is significantly enhanced by strain-induced diffusion, and it was confirmed by uphill diffusion of Ge. This result can propose an alternative oxidation method of strained SiGe/Si heterostructures.

SESSION B8: METALS AND INTERFACES
Chairs: Janice L. Veteran and Mehmet C. Ozturk
Thursday Morning, April 4, 2002
Salon 10-12 (Marriott)

8:00 AM B8.1
SELF-ALIGNED PASSIVATED COPPER INTERCONNECTS: A NOVEL TECHNIQUE FOR MAKING INTERCONNECTIONS IN ULSI DEVICE APPLICATIONS. Amit Chugh, Ashutosh Tiwari, A. Kvit, J. Narayan, NSF Center for Advanced Materials & Smart Structures, Department of Materials Science and Engineering, North Carolina State University, Raleigh, NC.

We have developed a technique to grow self-aligned epitaxial Cu/MgO

films on Si (100) using a Pulsed Laser Deposition Method. In this method we deposit a uniform film of Cu/Mg (5-7%) alloy over Si (100) at room temperature using TiN as an intermediate buffer layer. As a result of HRTEM (with spatial resolution of 0.18 nm) and STEM-Z investigations we observed that when this film is annealed at 500°C (in a controlled oxygen environment), in less than 30 minutes time, all the Mg segregates at the top and at the bottom surface of Cu. This is understood to be the consequence of lower surface energy of Mg. At 500°C Mg is quite sensitive to oxygen and a thin layer of MgO is immediately formed at the top surface, we also observed a thin layer of MgO at the Cu/TiN interface. Thickness of the upper MgO layer was found to be 15 nm while that of lower layer was 10 nm. Lower MgO layer acts as a diffusion barrier and inhibits the diffusion of Cu in the system. Upper MgO layer acts a passivating layer and improves the quality of copper against oxidation. Electrical resistivity measurements (in the temperature range 12-300 K) showed MgO/Cu/MgO/TiN/Si (100) sample to be highly conducting. We also observed that the resistivity of the system is insensitive to ambient oxygen environment. Self-aligned MgO (100) layer also provides a means to grow several interesting materials over it. This technique can be used to integrate high temperature superconductors like $YBa_2Cu_3O_{7-\delta}$ with silicon chip.

8:15 AM B8.2
RESISTIVITY OF AND ELECTROMIGRATION IN Cu-Ag ALLOYS. V. Bansore, K.S. Ravi Chandran, University of Utah, Department of Metallurgical Engineering, Salt Lake City, UT.

Cu has been implemented by some chip manufacturers recently for interconnects in VLSI circuits replacing traditional Al-Cu(2%) alloy. Recently there have been attempts to look beyond Cu and some Cu alloys have been proposed for future interconnects. In this study, the viability of Cu-Ag alloy as a possible interconnect is explored since it is the only alloy which gives a lower resistivity and possibly good reliability as compared to pure Cu. The sputter deposited Cu/Ag alloy films have been characterized in terms of resistivity, composition, microstructure, adhesion, electromigration lifetimes and electromigration activation energy calculations. The Cu/Ag alloy films were deposited by sputtering Cu/Ag alloy targets of different compositions. The films were annealed in-situ in vacuum at 400°C for 30 minutes. The resistivities for the as deposited and annealed films were relatively higher and lower respectively at all Ag concentrations. The microstructures of the films were evaluated and possible mechanisms for the resistivity decrease and electromigration resistance discussed. Adhesion of Cu-Ag alloy films seemed to be poor when compared to Cu on Si oxide, but showed good adhesion with a Ta under layer. Interconnect structures were etched out with Ta/Cu and Ta/Cu-Ag bilayers for electromigration reliability testing. The accelerated lifetime tests were conducted by passing high density of current through the structures while maintaining the test structures at a constant temperature by a temperature controlled hot and cold chuck system specially assembled for the purpose. The resistivity changes as a function of time at different temperatures are reported and analyzed and the activation energies for electromigration were determined.

8:30 AM B8.3
DIFFUSION STUDIES OF Cu IN Si AND LOW-k DIELECTRIC MATERIALS. K. Prasad, X.L. Yuan, C.M. Tan and D.H. Zhang, School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore, SINGAPORE; C.Y. Li, S.R. Wang, S.Y.J. Yuan, J.L. Xie, D. Gui and P.D. Foo, Institute of Microelectronics, Singapore, SINGAPORE.

The use of low-k dielectric and/or Cu metallization is chiefly responsible for the reduction in the interconnect delay time in deep submicron integrated circuits. Cu contamination during back end of line (BEOL) processing is considered a serious issue by the industry. Wafer backside Cu contamination has been shown to pose no serious problems in Cu process integration (K. Prasad et al., MRS 2000 Spring Meeting, San Francisco, USA, April 24-28 2000, Symposium D). However, there are reports of Cu contamination induced degradation of MOSFETs when a thin layer of oxide is present between Si wafer and Cu metallization (Hozawa et al., 2000 Symposium on VLSI Technology, Honolulu, USA, June 13-15 2000). It is obvious that the diffusion kinetics of Cu is very different in oxide and Si. In this work, we study the diffusion behavior of Cu in low-k dielectric materials such as Black Diamond (Applied Materials Inc.) and CORAL (Novellus Systems Inc.). MOS structures with Cu (deposited by ionized metal plasma), low-k dielectric (Black Diamond, CORAL, etc.), and Si are fabricated. For comparison purposes, MOS structures using conventional silicon dioxide and silicon nitride are also fabricated. They are subjected to thermal annealing in the temperature range typically used for BEOL processes, for various times. Cu concentration and depth profile, both in low-k dielectric material and Si substrate, are studied using SIMS and TXRF analyses. The electrical stability of MOS structures with Cu contamination is studied using I-V and C-V measurements. A correlation between Cu contamination and MOS electrical stability will be established. Diffusion properties of Cu in different low-k dielectric materials are compared and possible diffusion mechanisms in these dielectric materials will be reported. This work is supported through the award of a joint research grant from NSTB/MOE.

8:45 AM B8.4
MODELING COPPER DIFFUSION IN SILICON OXIDE, NITRIDE, AND CARBIDE. Vladimir Zubkov, Sheldon Aronowitz, LSI Logic, Santa Clara, CA; Joseph Han, Charles Musgrave, Dept of Chemical Engineering, Stanford, CA.

High diffusivity of Cu through low k and regular oxides is well established. However, nitrides and carbides exhibit effective barriers for the Cu drift. Ab initio methods and cluster approximation were applied to explore the barriers to Cu diffusion in oxide, nitride, and carbide. Since copper penetration in oxide is significantly enhanced by negative bias, copper ions are active species during copper diffusion. In this work interactions of copper cation, Cu^+, with molecular clusters modeling basic units of the silicon oxide, nitride, and carbide materials was considered. Most of the results were obtained for clusters involving one or two rings each bearing four Si atoms and four X groups where X contains O, or N, or C atom. Calculations revealed strong interactions of Cu^+ with model clusters. Copper diffusion should proceed as elementary "hops" between stable structures. Stable structures resulting from interaction of Cu^+ with the oxide, nitride, and carbide clusters were found. Estimated low bounds for activation energies for Cu^+ hops between stable structures are in agreement with experimentally observed barrier properties. Affect of spacial arrangement variations in amorphous oxide, nitride, and carbide on Cu^+ diffusion is discussed. The diffusion of neutral copper in oxide was also considered. In this case interaction of Cu with model clusters is weak and implies a high barrier for penetration of neutral Cu atoms from bulk copper into oxide. The results suggest that the barrier to copper diffusion in these materials is determined by their intrinsic properties. A possible technologically effective approach to raising the oxide barrier to Cu^+ diffusion is discussed.

9:00 AM B8.5
GROWTH MECHANISMS AND PROPERTIES OF TANTALUM THIN FILMS GROWN BY PLASMA-ENHANCED ATOMIC LAYER DEPOSITION. H. Kim, C. Cabral Jr., C. Lavoie, S.M. Rossnagel, IBM Thomas J. Watson Research Center, Yorktown Heights, NY.

Ta films were grown by plasma-enhanced atomic layer deposition (PE-ALD) at temperatures from 20°C up to 500°C using $TaCl_5$ as source gas and RF plasma-produced atomic H as the reducing agent. Post-deposition chemical analyses showed that the main impurity is oxygen, incorporated during the air exposure prior to analysis. The films had typically low Cl concentration below 1 at %. X-ray diffraction shows broad diffraction features, indicating that ALD Ta films are composed of nanocrystals. The typical resistivity of ALD Ta films was 150-180 $\mu\Omega\cdot$cm, which corresponds to that of β-Ta phase, for a wide range of growth parameters. The conformality was up to 100% in trenches with aspect ratio of 15. The thickness per cycle, corresponding to the growth rate, was measured by Rutherford backscattering spectrometry and/or quartz crystal microbalance as a function of various key growth parameters, including $TaCl_5$ and H exposure time and growth temperature. The maximum values of thickness per cycle were below 0.1 ML, due to the steric hindrance for $TaCl_5$ adsorption. Based upon these results, the basic growth mechanisms for Ta PE-ALD are discussed. The diffusion barrier properties of ALD Ta films were investigated using bilayer structures consisting of Cu films deposited by sputtering and ALD Ta of various thickness on Si. Various analysis techniques were applied during heating, including X-ray diffraction, elastic light scattering, and resistance analysis. The results were compared with Ta thin films deposited by sputtering with comparable thicknesses.

9:15 AM B8.6
THE EFFECTS OF NITROGEN ON ELECTRICAL AND STRUCTURAL PROPERTIES IN $TaSi_xN_y/SiO_2$/p-Si MOS CAPACITORS. You-Seok Suh, Greg Heuss, Jae-Hoon Lee, and Veena Misra, Department of Electrical Engineering, North Carolina State University, Raleigh, NC.

As gate oxide thickness decreases, the capacitance associated with the depleted layer at the poly-Si/gate dielectric interface becomes significant, making it necessary to consider alternative gate electrodes. The search for metallic gates faces many challenges since they must have compatible work functions, process compatibility and thermal/chemical interface stability with underlying dielectric. Most metal gate electrodes studied to date suffer from high temperature instability resulting in a degraded interface with the underlying dielectric. Our recent wok has shown that $TaSi_xN_y$ (Si >Ta) films on SiO_2 have excellent thermal stability at high temperatures and the

workfunction of $TaSi_xN_y$ is compatible with NMOS devices. In this work, $TaSi_xN_y$ films were deposited on the SiO_2 gate oxides using reactive co-sputtering of Ta and Si target. The $TaSi_xN_y$ gate electrodes with different compositions have been studied to investigate the effects of the nitrogen in the $TaSi_xN_y$ gate on the electrical and structural properties. The role of nitrogen in the $TaSi_xN_y$ gate was studied by comparing flatband voltage and the equivalent oxide thickness with nitrogen. The thermal stability of $TaSi_xN_y$ on SiO_2 stacks was studied at annealing temperatures of 700°C and 900°C in Ar. XPS and TEM analysis were performed to get the bonding information in the films and interfacial reaction between $TaSi_xN_y$ film and SiO_2.

10:00 AM B8.7
NON-DESTRUCTIVE MONITORING OF COBALT SILICIDE USING PICOSECOND ULTRASONIC MEASUREMENTS.
Amit Nangia, Texas Instruments Inc, DMOS6, Dallas, TX; Chi-Kong Cheung, University of California, Berkeley, Dept of Chemical Engineering, Berkeley, CA; Niall McCusker, Rudolph Technologies, Flanders, NJ.

Silicides in CMOS technology have historically been monitored by measuring sheet resistance at different stages of the metal-silicon reaction. Sheet resistance being destructive in nature, requires that these measurements be made on non-product wafers. As contacts continue to shrink in size with more stringent processing requirements, the use of a non-destructive technique to gauge the silicidation process directly on product devices becomes increasingly important. Elimination of non-production material also has processing cost and time reduction benefits which can be significant at 300mm diameter wafer fabrication. In this study, we investigated the use of picosecond ultrasonics to assess thickness and density of cobalt metal and silicide phases over the different stages of silicidation. An ultrafast optical 'pump and probe' technique was used to excite the film and measure change in optical reflectivity as a function of time. Samples of different thickness were measured after cobalt stack deposition, CoSi formation, cap layer strip and $CoSi_2$ anneal. Models were developed to extract the thickness and density of the films at each step, on both single crystal silicon and poly-silicon substrates. A correlation was obtained between sheet resistance and measured thickness for the different stages of the cobalt silicide formation.

10:15 AM B8.8
SINGLE CRYSTAL TaN THIN FILMS ON TiN/Si HETERO-STRUCTURE.
Haiyan Wang, Ashutosh Tiwari, Alexamder Kvit, Xinghang Zhang, Jagdish Narayan, Department of Materials Science and Engineering, North Carolina State University, Raleigh, NC.

We have successfully grown epitaxial cubic (B1-NaCl structure) tantalum nitride films on Si (100) and (111) substrate using a pulsed laser deposition technique. A thin layer of titanium nitride was used as a buffer medium. We characterized these films using X-ray diffraction, high resolution transmission electron microscopy and scanning transmission electron microscopy (Z-contrast). X-ray diffraction and high-resolution transmission electron microscopy confirmed the single crystalline nature of these films with cubic-on-cubic epitaxy. The epitaxial relations follow TaN(100)‖TiN(100)‖Si(100) on Si(100) and TaN(111)‖TiN(111)‖Si(111) on Si(111). We observed sharp interfaces of TaN/TiN and TiN/Si without any indication of interfacial reaction. We checked the diffusion barrier characteristics of these films by growing a thin layer of copper on the top and subsequently annealing the films at 600°C. Even after annealing for 30 minutes we did not observe any diffusion of copper in the system. Rutherford backscattering experiments showed these films to be slightly nitrogen deficient ($TaN_{0.9}$). High precision electrical resistivity measurements showed excellent metallic nature of these films. We also tried to deposit TaN directly on silicon, the films were found to be polycrystalline. In our method, TiN plays a key role in facilitating the epitaxial growth of TaN. This method exploits the concept of lattice matching epitaxy between TaN and TiN and domain matching epitaxy between TiN and Si. This work explores a promising way to grow high quality TaN diffusion barrier on silicon for copper interconnection.

10:30 AM B8.9
MICROSTRUCTURAL EVOLUTION OF THE INITIAL PHASE FORMATION OF COBALT SILICIDE WITH AN ULTRA-THIN TITANIUM UNDERLAYER.
Kevin D. Johnson, Julie Tsai, Zhiyong Ma, Intel Corporation, Hillsboro, OR; Kian Sin Sim, Intel Corporation, Penang, MALAYSIA.

Co silicide has been a predominant candidate for deep sub-micron process technology owing to its low resistance, process compatibility and scalability. This work investigates ultra-thin Ti underlayer assisted mediation of the phase formation for cobalt silicide and addresses the role of Ti in the various stages of the phase evolution. The Ti underlayer has been sputter deposited as a thin ($<20Å$) amorphous layer prior to Co deposition. A rapid thermal anneal (490°C-650°C) is then implemented to initiate salicidation. Although the reaction sequence for Co silicide is Co->Co_2Si->CoSi->$CoSi_2$, the introduction of a very thin Ti underlayer alters this sequence, allowing $CoSi_2$ to form directly below the Ti underlayer and a more Co-rich phase to form above the Ti underlayer. The thickness of the Ti underlayer also alters the initial phase formation and the reaction path for Co salicidation. In addition to mediating the reaction kinetics, there are practical advantages for Ti underlayer that mitigate some of the difficulties of salicide processing.

10:45 AM B8.10
A STUDY OF LEAKAGE CHARACTERISTICS IN SILICIDED SHALLOW JUNCTIONS USING TRANSMISSION ELECTRON MICROSCOPY.
Chel-Jong Choi, Tae-Yeon Seong, Dept of Materials Science and Engineering, Kwangju Inst of Science and Technology (K-JIST), Kwangju, KOREA; Key-Min Lee, Joo-Hyoung Lee, Young-Jin Park, Memory R&D Div, Hynix Semiconductor Inc, Cheongju, KOREA; Hi-Deok Lee, Dept of Electronics Engineering, Chungnam National Univ, Taejon, KOREA.

A cobalt self-aligned-silicide process has been widely used to realize high performance ultra-large-scale integrated (ULSI) circuits. As the dimension of ULSI devices continues to scale down, a junction leakage problem caused by a Co-silicidation process can be a key issue for the fabrication of next generation integrated circuits. However, the precise leakage model remains still unclear due to the complex characteristics of the junction leakage. In this work, two-dimensional (2D) junction profiling using transmission electron microscope (TEM) combined with selective chemical etching is used to investigate the junction leakage mechanism in p+/n and n+/p shallow junctions which were fabricated using the Co-silicidation and shallow trench isolation (STI) processes. To directly reveal 2D profiles in the junctions, ion-milled cross-section thin foil specimens are chemically etched using a mixture of HF, HNO_3, and CH_3COOH. TEM and TSUPREM-4 simulation results show that a decrease in the Si interstitials near the edges of the active regions causes junction profiles to bend upward near the active edges, namely, the formation of shallower junctions in these regions. Based on the TEM and electrical results, it is suggested that abnormal junction profiles near the edges of the active regions could be a main cause for the junction leakages in the silicided perimeter samples with the p+/n and n+/p junctions.

11:00 AM B8.11
ON THE MORPHOLOGY CHANGES OF Ni- AND Ni(PT)-SILICIDES.
Pooi See Lee, Dept of Materials Science, Kin Leong Pey, Dept of Electrical and Computing Engineering, National University of Singapore, SINGAPORE; Dominique Mangelinck, L2MP-CNRS, FRANCE; Jun Ding, Dept of Materials Science, Dong Zhi Chi, Institute of Materials Research and Engineering, SINGAPORE; Thomas Osipowicz, Dept of Physics, National University of Singapore, SINGAPORE; Alex See, Chartered Semiconductor Manufacturing, SINGAPORE.

NiSi is a promising silicide material due to one step low temperature formation, low resistivity and low Si consumption. To enhance the phase stability of NiSi, addition of Pt has been shown to form Ni(Pt)Si up to 900°C [1]. The application of Ni(Pt)Si onto devices at silicidation temperatures above 700°C has also been demonstrated [2]. The issue of agglomeration and layer inversion has remained critical since conductivity of thin silicide films is sensitive to the degradation of the film morphology. The purpose of this work is to study the morphology degradation that includes agglomeration and layer inversion of NiSi and Ni(Pt)Si. Rutherford Backscattering Spectroscopy (RBS), Scanning Electron Microscopy (SEM), Cross Transmission Electron Microscopy (XTEM) and electron diffraction analysis were employed. Layer inversion leads to the reversal in position of polycrystalline silicon (poly-Si) and silicide. It was found that the addition of Pt has led to an improvement in the agglomeration behavior of NiSi but have little influence on the layer inversion on the undoped poly-Si. Suppression of layer inversion was attained by silicidation on Phosphorus doped poly-Si or with the use of thin Ni(Pt) (~10 nm). The agglomeration behavior and layer inversion are discussed in terms of the controlling factors of grain boundary energy and interface energies. [1] D. Mangelinck, J.Y. Dai, J.S. Pan and S.K. Lahiri, Appl. Phys. Lett. 75 (12), 1736 (1999). [2] P.S. Lee, K.L. Pey, D. Mangelinck, J. Ding, D.Z. Chi, L. Chan, Electron Dev. Lett., to be published in Dec, 2001.

11:15 AM B8.12
AC-INDUCED DAMAGE IN Cu INTERCONNECTS.
R. Mönig, S. Orso, C.A. Volkert, R.R. Keller, and E. Arzt, Max Planck Institute for Metals Research, Stuttgart, GERMANY.

We have recently observed the formation of severe damage in Cu interconnects during in-situ testing in an SEM with 100 Hz alternating currents at room temperature. The damage appears as surface wrinkles within single grains, which grow in amplitude and extent,

and eventually lead to electrical failure of the lines. The damage bears no resemblance to typical electromigration damage generated by DC testing conditions and is probably caused by thermal fatigue. Because of Joule heating in the interconnects, the alternating currents used in these studies (rms 10-15 MA/cm^2) generate temperature swings as large as 150°C which cause thermal mechanical strain cycles and the creation of fatigue damage within as few as 10^5 cycles. The formation of the fatigue damage is not hindered by the presence of soft encapsulating films, such as a polymer-based low k dielectrics. Since the temperature swings generated by the tests are not much larger than those expected in devices during use, thermal mechanical fatigue may become a serious reliability threat in Cu-based devices with soft interlevel dielectrics. We will present results on the effect of the current density (or temperature amplitude), grain orientation, and encapsulating layers on the formation of fatigue damage and the time to cause an electrical failure. In addition, the damage accumulation process, including the formation of cracks, will be described.

11:30 AM B8.13
EXPERIMENTAL CHARACTERIZATION OF THE RELIABILITY OF 3-TERMINAL DUAL-DAMASCENE COPPER INTERCONNECT TREES. C.L. Gan[a], C.V. Thompson[a,b], K.L. Pey[a,c], W.K. Choi[a,c], F. Wei[b], B. Yu[d], and S.P. Hau-Riege[e]; [a]Advanced Materials for Micro- and Nano- Systems Programme, Singapore-MIT Alliance, SINGAPORE; [b]Department of MS&E, Massachusetts Institute of Technology, MA; [c]Department of Electrical & Computer Engineering, National University of Singapore, SINGAPORE; [d]Institute of Microelectronics, SINGAPORE; [e]Intel Corp., Portland, OR, now with Lawrence Livermore National Laboratory, Livermore, CA.

Presently, most modeling and experimental analyses for circuit-level interconnect reliability focus on straight stud-to-stud test lines. However, in reality, multiple segments of straight-lines are connected at junctions in integrated circuits. An interconnect tree has been defined as a unit of continuously connected high-conductivity metal lying within one layer of metallization. Standard reliability-assessment methods are based on analysis of individual segments, using the results from straight junction-free lines rather than trees. This method is generally inaccurate as material within an interconnect tree can diffuse freely among connected segments, and the stress evolution in different segments of a tree is coupled. Tree-based experiments and assessment methodologies have been developed for Al-based interconnects. However, experiments have not been previously carried out on Cu-based interconnect trees. Electromigration experiments have been carried out on simple Cu dual-damascene interconnect tree structures consisting of straight stud-to-stud lines with an extra via in the middle of the line. As with Al-based interconnects, the reliability of a segment in this tree strongly depends on the stress conditions of the connected segment. Beyond this, there are important differences in the results obtained under similar test conditions for Al-based and Cu-based interconnect trees. These differences are thought to be associated with variations in the architectural schemes of the two metallizations. The absence of a conducting electromigration-resistant overlayer in Cu technology, and the possibility of liner rupture at stressed vias, lead to important differences in tree reliabilities in Cu compared to Al. Although liner rupture may increase the reliability of the structure locally, it can lead to a globally reduced lifetime of the circuit. This work demonstrates that while segments are not the fundamental reliability unit for circuit-level reliability assessments for Al *or* Cu, vias, rather than trees, might be the appropriate fundamental units for assessment of Cu reliability.

11:45 AM B8.14
COMPARISON OF TiN THIN FILMS DEPOSITED BY METAL ORGANIC ATOMIC LAYER DEPOSITION (MOALD) USING TDMAT AND TDEAT. Ju Youn Kim, Sang Won Seo, Jin Yong Park, Yangdo Kim, Young Do Kim and Hyeongtag Jeon, Division of Materials Science and Engineering, Hanyang University, Seoul, KOREA.

Among the transition metal nitrides, titanium nitride (TiN) has been widely used as a diffusion barrier in ultra large scale integrated devices. Barrier layers were deposited predominantly by the physical vapor deposition (PVD) and chemical vapor deposition (CVD) techniques, but they suffer from the poor step coverage and have limited their applicability in the new generation of integrated circuits with very high aspect ratio structure and shrunken device dimension. Atomic layer deposition (ALD) is a new deposition technique to improve the combined problems of PVD and CVD methods. Many researches have been carried out to grow TiN, mainly using halide precursors, by ALD method. However, the films grown by ALD method using halide precursors has some problems such as very low growth rate and high chlorine contents which makes ALD difficult to be applied in an industrial device process. Therefore, in the recent, many experiments have been performed to alternate halide precursors with metal organic precursors. In this study, TiN films grown by metal organic ALD (MOALD) method using tetrakis-dimethyl-amino-titanium (TDMAT) and terakis-diethyl-amino-titaninm (TDEAT) as Ti precursor and NH_3 as reactant gas have been investigated. The physical, chemical and electrical properties of TiN films grown by MOALD using TDMAT and TDEAT precursors have been systematically analyzed and compared.

SESSION B9/C6: JOINT SESSION
CHARACTERIZATION USING SURFACE ANALYSIS TECHNIQUES
Chairs: Daniel F. Downey and Janice L. Veteran
Thursday Afternoon, April 4, 2002
Salon 10-12 (Marriott)

1:00 PM *B9.1/C6.1
ROUTINE DOPANT/IMPURITY AND STOICHIOMETRY CHARACTERIZATION OF SiGe AND SiON USING SURFACE ANALYSIS TECHNIQUES. Charles W. Magee, Evans East, (A Member of the Evans Analytical Group), East Windsor, NJ.

A critical technological benchmark of the SiGe HBT is its maximum oscillation frequency fmax, which is dependent on the base sheet resistance of the transistor. Reduction of the base sheet resistance results in a higher operating frequency. However, the peak boron concentration in the base is limited by boron out-diffusion. Incorporation of carbon into the SiGe has been shown to reduce this B out-diffusion.[1,2] These properties often require SIMS characterization for measuring the changes in the B distribution with growth and anneal, as well as determining the substitutional C concentration. The depth profile characterization by SIMS however, demands carefully set analytical protocols involving standards calibrated by other techniques for accurate quantification. In addition, the requirement to measure layer thicknesses or junction depths makes achieving good depth resolution during the analysis also important. A high dose C implant across the interface between an RBS-calibrated, B-doped SiGe epi layer and the Si substrate was prepared as a quantification reference material to characterize SiGeC:B epitaxial films. The protocol developed using a series of SiGe samples implanted with various elements provides concentration determinations for these elements with an accuracy of 5-10%. Several experimental conditions show that a low energy oxygen primary ion beam has to be used to measure an accurate B distribution in the sample, which is often used to determine the base layer thickness. Although Cs primary ion bombardment allows the accurate quantification of total B, C, O, P and Ge, using ion yield corrections, in a single analysis for cost effectiveness, the oxygen bombardment is necessary to obtain better depth resolution. A second part of this presentation focuses on siliconoxynitride-SiON gate dielectrics. As the thickness of these gate dielectrics is reduced, the demands on the analytical techniques used to characterize these films have increased. The characterization of the SiON films, which currently range from 1-5nm thickness and 1-25 atom% N, necessitates a combination of near surface characterization techniques and reference materials. Currently, Nuclear Reaction Analysis (NRA) is used in the calibration of reference materials; X-ray Photoelectron Spectroscopy is used measure total N concentration and thickness using these reference materials, and SIMS is used in combination with results of XPS to determine the nitrogen distribution.

[1]M.S. Carroll, J.C. Strum, T.H. Buyuklimanli, Phys. Rev. B64 August 2001.
[2]L.D. Lanzerotti, J.C. Sturm, E. Stach, R. Hull, & T.H. Buyuklimanli, C. Magee Appl. Phys. Lett. 70 (23) 3125 (1997).

SESSION B10: OXIDES AND SILICIDES
Chair: Janice L. Veteran
Thursday Afternoon, April 4, 2002
Salon 10-12 (Marriott)

1:45 PM B10.1
LPCVD OF SILICON NITRIDE USING ADAPTIVE REAL-TIME TEMPERATURE CONTROL. John Gumpher, Tokyo Electron America, Diffusion Systems, Richardson, TX; Wayne Bather, Darin Wedel, Texas Instruments, Silicon Technology Development Group, Dallas, TX.

A novel method to achieve very uniform thick silicon nitride depositions using dichlorosilane and ammonia is demonstrated in a LPCVD batch furnace system. Adaptive Real-Time Temperature control, coupled with model-based process temperature optimization, can significantly improve both wafer-to-wafer and within-wafer silicon nitride thickness uniformity. Improvement in within-wafer thickness uniformity is achieved by thermal ramping during deposition. The

resulting across-wafer thermal gradient offsets the effects of preferential edge deposition on within-wafer thickness uniformity. Accurate estimation of substrate thermal response and silicon nitride deposition rate dependence on temperature and process chemistry allow for precise calculation of temperature setpoints for best uniformity. Both of these requirements are met using Adaptive Real-Time Temperature control and associated silicon nitride deposition models. The ability of current vertical LPCVD batch reactors to precisely control process temperatures, even during ramping, insures repeatable results. Typically, additional test runs are required to qualify silicon nitride depositions and process time increases when Adaptive Real-Time Temperature control is utilized. However, Adaptive Real-Time Temperature control is intended for critical processes with very demanding film thickness specifications; where batch sizes must be reduced to achieve acceptable thickness uniformity. The use of Adaptive Real-Time Temperature control allows acceptable film thickness uniformity to be achieved over the entire furnace load area and ultimately increases process throughput.

2:00 PM B10.2
Si/SiO_2 INTERFACE ROUGHNESS STUDY BY SCANNING TUNNELING MICROSCOPY. Jixin Yu, Lequn Liu, Thomas W. Sorsch[a], William M. Mansfield[a], Gregory L. Timp, and Joseph W. Lyding, Beckman Institute, University of Illinois, Urbana, IL; [a]Agere System, Murray Hill, NJ.

There is a tremendous interest in determining the Si/SiO_2 interface roughness, which is believed to account for the degradation of the effective mobility of an inversion layer at high transverse field. Two parameters are necessary to characterize the interface roughness: the rms-roughness Δ, and the correlation length Λ. For the first time, we demonstrate that ultra-high vacuum scanning tunneling microscopy (STM) can be used to directly examine the Si/SiO_2 interface and extract Δ and Λ simultaneously from the topography. The rms-roughness Δ can be acquired from the Gaussian fit of the asperity height distribution, and the correlation length Λ is obtained from an exponential fit to the in-plane autocorrelation function. A smooth wafer and a rough wafer have been examined, both with a nominally 1nm gate oxide grown at 1000°C by standard industry procedure. We find Δ=0.111nm and Λ=2.605nm for the smooth wafer and Δ=0.285nm and Λ=2.416nm for the rough one. These results are consistent with those extracted from annular dark field scanning transmission electron microscopy data and X-ray diffraction data taken on similarly processed wafers.

2:15 PM B10.3
TRANSPORT PROPERTIES OF HETEROSTRUCTURE $ZrSiO_4$ / Al_2O_3 / $ZrSiO_4$ AND Si_3N_4 / Al_2O_3 / Si_3N_4 ON Si. Julie D. Casperson, Harry A. Atwater, California Institute of Technology, Watson Laboratory of Applied Physics, Pasadena, CA; L. Douglas Bell, Jet Propulsion Laboratory, Pasadena, CA; Brett W. Busch, Lalita Manchanda, Martin L. Green, Agere Systems, Murray Hill, NJ.

Among the main performance limitations of floating gate nonvolatile memory devices, such as flash memories and nanocrystal memories, are the long program time (~1 μs) and erase time (~1 ms) achievable via a Fowler-Nordheim tunneling mechanism for charging of the floating gate through a homogeneous tunnel barrier. An interesting alternative to homogeneous dielectric tunnel barriers is a silicon compatible layered tunnel barrier, which enables a large drop in the barrier height with applied voltage. We have correlated dielectric constants and band offsets with respect to silicon in order to help identify possible materials from which to construct these layered barriers. Based on this survey, we have determined that some of the most promising materials heterostructures are Si_3N_4 / Al_2O_3 / Si_3N_4 and $ZrSiO_4$ / Al_2O_3 / $ZrSiO_4$. We have fabricated the metal-insulator-semiconductor layered barrier structure of Si_3N_4 / Al_2O_3 / Si_3N_4 on silicon. The Si_3N_4 was made by low-pressure chemical vapor deposition at 700°C, while the Al_2O_3 was made by atomic layer deposition using sequential exposures of trimethylaluminum and H_2O at 300°C. High-temperature annealing was found to greatly reduce the leakage currents and thus enhance the barrier lowering. We have also fabricated single-layer barriers of Al_2O_3 and double barriers of Si_3N_4 / Al_2O_3. A comparison of the current-voltage (I-V) and capacitance-voltage (C-V) characteristics of these structures will be discussed. The I-V measurements that were performed on dielectrics that were deposited on degenerately doped n^+ and p^+ silicon in order to minimize band-bending. To assess the electrical performance of our layered tunnel barriers, we performed simulations with heterostructure amorphous dielectrics on Si(100). Tunneling probability simulations for layered tunnel barriers are performed using an effective-mass model. With this theory we are able to predict the I-V curves for our tunnel barriers and can determine if barrier lowering has been achieved. In addition to electrical characterization, values of the band offsets for Al_2O_3 and $ZrSiO_4$ relative to n-type silicon will be presented. These values are found by ballistic electron emission microscopy (BEEM) and by photoconductivity measurements that utilize a variable energy tunable light source.

3:00 PM B10.4
DIFFUSION CHARACTERISTICS OF COPPER IN TiN THIN FILMS. Abhishek Gupta, Alex V. Kvit, Gerd Duscher and J. Narayan, NSF Center for Advanced Materials and Smart Structures, Department of Materials Science and Engineering, NCSU, Raleigh, NC.

We have investigated the diffusion characteristics of copper in nanocrystalline, polycrystalline and single crystal TiN thin films, which is being used as a diffusion barrier for sub-quarter-micron metallization. These films were synthesized on Si $< 100 >$ substrate by first ablating amorphous TiN and then ablating amorphous copper targets using Pulse Laser Deposition. The three different crystal structures of TiN were achieved by growing the films at different substrate temperatures, where higher temperatures (~650°C) leads towards epitaxy. Then a uniform thin layer of copper was deposited at room temperature for all the three depositions above. Each sample is annealed at three different temperatures (400°C, 500°C and 600°C) to study the diffusion barrier characteristics of TiN. Study of diffusion profile and the copper concentration measurement were performed using Scanning Transmission Electron Microscopy-Z contrast (0.16nm resolution), Secondary Ion Mass Spectroscopy, Electron Energy Loss Spectroscopy and Rutherford Backscattering Spectroscopy techniques. These data were used to plot the measured concentration of copper with respect to the temperatures for the three crystal structures of TiN to calculate the diffusion coefficients and were compared to study the effect of microstructure of TiN thin film on the diffusion of copper after annealing.

3:15 PM B10.5
EFFECT OF AN APPLIED Ti LAYER ON $CoSi_2$ SALICIDE FORMATION. G.Z. Pan, E.W. Chang, S.A. Prussin and Y. Rahmat-Samii, University of California at Los Angeles, Dept of Electrical Engineering, Microelectronics Fabrication Laboratory, Los Angeles, CA.

Integration of self-aligned metal silicide into metal-oxide-semiconductor transistors in 100 nm and beyond technology nodes is crucially difficult in order to achieve low sheet/contact resistance on ultra-shallow junction source/drain as well as narrow gate. $CoSi_2$ silicide, in comparison with $TiSi_2$ and NiSi, is advantageously attractive in terms of low sheet resistivity, independent formation on narrow gate length, suitable formation temperature in control of ultra-shallow junctions and thermal stability as well as readily epitaxial growth to improve contact resistance. We studied extensively the formation of ultra thin $CoSi_2$ silicide with/without an applied Ti mediating or capping layer by using rapid isothermal and isochronal annealing in N_2 ambient. Four-point-probe sheet resistance measurements and electron microscopy were used to characterize the ultra-thin silicide films as well as their formation kinetics. We found that the formation temperature of CoSi and $CoSi_2$ as well as their existing duration are strongly influenced by the presence of an applied Ti mediating or capping layer. Under Ti capping, Co directly reacts with Si substrate in a way similar to a single layer Co silicidation. However, Ti capping favors the formation of CoSi and the diffusion of Ti from the capping layer delays the phase transformation of CoSi into $CoSi_2$ from 525°C to 675°C. An applied Ti mediating layer acting as a diffusion barrier suppresses the supply of Co so that it limits the formation of high Co concentration silicide CoSi but favors that of low Co concentration silicide $CoSi_2$ under a Co diffusion-controlled process. Electron microscopy studies indicate that $CoSi_2$ formed with an applied Ti mediating layer exhibits better epitaxial characteristics.

3:30 PM B10.6
FUNDAMENTAL BEAM STUIDES OF RADICAL ENHANCED ATOMIC LAYER DEPOSITION OF TITANIUM NITRIDE. Frank Greer, D. Fraser, J.W. Coburn, and David B. Graves, U.C. Berkeley, Dept of Chemical Engineering, Berkeley, CA.

Atomic Layer Deposition (ALD) has been proposed as one way to deposit highly conformal thin films for copper diffusion barriers due to the self-limiting, layer-by-layer growth that can be achieved with this technology. One problem with thermally activated ALD is that the deposition temperatures that are required to achieve reasonable growth rates and good quality films with low impurity concentrations can be relatively high. This may make the integration of these barrier films with temperature-sensitive films, such as organic low-k films, impossible. One potential alternative to thermal ALD is to use more reactive species such as radicals to catalyze film deposition at lower substrate temperatures. In this work, TiN films are deposited using Radical Enhanced Atomic Layer Deposition (RE-ALD) using separate, alternating pulses of TiCl4 and various combinations of hydrogen and/or nitrogen radicals with or without additional pulses

of NH3. By directing independent beams of each of these species at a given surface (in this case, silicon coated on Quartz Crystal Microbalances), kinetic parameters of interest such as the sticking and reaction probabilities of these species have been measured as a function of surface temperature, and will be used to predict the conformality of films deposited using RE-ALD in features of arbitrary aspect ratio. Ex-situ XPS analysis of the deposited films will be presented, paying particular attention to the low residual chlorine content that can be achieved with sufficient hydrogen radical exposure (~0.3%) at deposition temperatures as low as 100°C. In-vacuo Auger Electron Spectroscopy film composition measurements will be presented from different stages during the deposition process. Various measurements of the film quality will also be presented including the films' resistivity and crystallinity.

3:45 PM B10.7
NICKEL, PLATINUM and ZIRCONIUM GERMANOSILICIDE CONTACTS TO ULTRA-SHALLOW, P^+N JUNCTIONS FORMED BY SELECTIVE SiGe TECHNOLOGY FOR CMOS TECHNOLOGY NODES BEYOND 70NM. Jing Liu, Hongxiang Mo, Mehmet C. Ozturk, North Carolina State University, Department of Electrical and Computer Engineering, Raleigh, NC.

One of the key challenges for future CMOS technology nodes beyond 100 nm is formation of ultra-shallow junctions with a series resistance contribution limited to five percent of the channel resistance. The future junctions are expected to possess extremely low sheet, contact and spreading resistance values requiring fundamentally different methods for junction and contact formation. Recently, this laboratory reported a new technology based on selective deposition of doped SiGe alloys in source/drain regions isotropically etched to the desired depth, which showed promise for technology nodes down to 30 nm. Of particular interest to this paper is the smaller bandgap of SiGe resulting in a smaller metal-semiconductor barrier height, which is a key advantage in reducing the contact resistivity for future technology nodes. In this paper, we present our recent results on Pt and Ni germanosilicide contacts to p^+ SiGe. We show that both contacts can provide a resistivity near 10^{-8} ohm-cm^2 needed for technology nodes beyond 70 nm. However, the stability of the materials were found to be limited to ~550°C for Ni and ~800°C for Pt. This was attributed to Ge departure from germanosilicide to segregate either at the grain boundaries or at the contact-junction interface. Zr was proposed as an alternative germanosilicide for better stability. Another possibility, considered for the first time here is the use of a thin Zr layer as an intermediate layer between Pt or Ni and the junction. The films were characterized by four-point-probe, XRD, SIMS and AFM. The results indicate that both Zr alone or Zr with Pt and Ni are viable contact materials to p^+ SiGe. Using Zr alone results in a ternary germano-silicide with good stability at least up to 900°C. Using Zr as an intermediate layer improves the stability by retarding the Ge loss from the germanosilicide.

4:00 PM B10.8
MICROSTRUCTURE AND ELECTRICAL PROPERTIES OF Cu/TiN INTERFACE FOR CMOS COPPER INTERCONNECTION. Qi Wang, Qingguo Tao, Tong Wang and Chunmei Chen, Tongling Nonferrous Metals Shenzhen Company, Shenzhen, PRC; Xiaoman Duan, MIT, Dept of Materials Science & Engr, Cambridge, MA.

The interface between Cu and barrier layer is important key to the CMOS copper interconnection. An ideal interface of Cu/Barrier metal has to be developed to form a uniform and homogeneous copper grain layer in order to suppress the interfacial electromigration of copper. In this study, a TiN layer with a thickness of 800 Å was deposited onto a typical dielectric SiO_2 layer using conventional Physical Vapor Deposition technique. On the barrier layer, a 200 Å layer of copper was, then, sputtered at room temperature. Afterwards, low temperature annealing for Cu/Barrier metal interface was carried out at 350 to 550°C for 30 to 60 minutes in order to form a uniform interface and to reduce residual stress in the layers formed during deposition. We have systematically studied the wetting and agglomeration of copper layer on TiN substrate and the texture of Cu film using Transmission Electron Microscopy (TEM) and X-ray Diffraction (XRD). It was found that the better wetting interface and less copper agglomeration occurred during low temperature annealing, and the roughness of the Cu/TiN interface increased with the annealing temperature. It was also found that the (111) copper texture formed during deposition and the degree of the texture decreased with increasing of annealing temperature and time. The result showed that the electromigration of copper in CMOS interconnects was related with the microstructure of Cu/barrier interface, in turn, with the annealing procedures. The relationship between electromigration resistance and texture degree of copper is reported in this paper.

SESSION B11: POSTER SESSION
METALS AND MODELING
Thursday Evening, April 4, 2002
8:00 PM
Salon 1-7 (Marriott)

B11.1
MICRO-RAMAN SPECTROSCOPIC STUDY OF NICKEL SILICIDE FILMS. S.K. Donthu, D.Z. Chi, S. Tripathy[a], A.S.W. Wong and S.J. Chua, Institute of Materials Research and Engineering, Singapore, SINGAPORE; [a]Centre for Optoelectronics, Singapore, SINGAPORE.

Micro-Raman technique was used to investigate vibrational properties of NiSi thin films formed on three different substrates: unimplanted (100) Si, 20-keV BF_2^+-implanted (100) Si, and 20-keV B^+-implanted (100) Si. Nickel films, 30-nm thick, were deposited by sputtering technique and were subsequently rapid thermal annealed for 60 sec at 500-800°C for silicidation. Secondary ion mass spectroscopy was employed to study dopant redistribution during silicidation. Raman spectroscopy was performed in backscattering geometry corresponding to either $z(xx)\bar{z}$, $z(xy)\bar{z}$ or $z(yy)\bar{z}$ configuration. Raman spectroscopy was also performed on NiSi powder to identify various phonon modes associated with different selection rules of group theory. Eight characteristic phonon peaks of NiSi phase were identified of which four at 214-cm^{-1}, 288-cm^{-1}, 360-cm^{-1} and 397-cm^{-1} were assigned to A_g phonon modes, the two at 197-cm^{-1} and 332-cm^{-1} to B_{1g} phonon modes and the remaining two at 255-cm^{-1} and 314 cm^{-1} to either B_{2g} or B_{3g} phonon modes. It was found that Raman peaks of NiSi thin films formed on BF_2^+ implanted substrate were broader and shifted to lower frequency side compared to films formed on other substrates. The broadening of the Raman peaks in these films, which also exhibit much improved thermal stability, is attributed to small grains resulting probably from fluorine segregation to grain boundaries and interface. SIMS analysis showed that fluorine preferentially segregates to silicide film with an estimated concentration of about 1-3 atm %. It is proposed that in addition to grain boundary segregation, some structural modification in silicide film is induced by the presence of excess fluorine inside the grains, resulting in shift of phonon peak positions.

B11.2
Abstract Withdrawn.

B11.3
OPTIMIZATION OF ULTRATHIN ALD TANTALUM NITRIDE FILMS FOR ZERO-THICKNESS LINER APPLICATIONS. Oscar van der Straten, Yu Zhu, Eric Eisenbraun, Alain Kaloyeros, UAlbany Institute for Materials, Albany, NY.

A metal-organic atomic layer deposition (ALD) tantalum nitride process has been demonstrated for zero-thickness liner applications in advanced copper metallization schemes employing a commercial ALD reactor. This process employs a liquid tantalum source (tertbutylimido trisdiethylamido tantalum - TBTDET) and ammonia as the reactants. Key functionality data addressing the self-limiting nature of ALD film growth with respect to key process parameters including substrate surface exposures to TBTDET and ammonia will be presented. Surface roughness data as well as conformality data of ALD tantalum nitride in high aspect ratio structures as measured by atomic force microscopy (AFM) and transmission electron microscopy (TEM), respectively, will also be presented. Results of research to evaluate the barrier performance of thermally and bias stressed Cu/ALD tantalum nitride stacks using both compositional and electrical measurements will be discussed, as will limiting barrier thickness metrics and determination of the barrier failure mechanisms.

B11.4
THE USE OF C-V TECHNIQUES TO INVESTIGATE INSTABILITY MECHANISMS IN M-I-S STRUCTURES. S. Paul, W.I. Milne and J. Robertson, Engineering Department, Cambridge University Cambridge, UNITED KINGDOM.

In the field of flat panel displays, the current leading technology is the Active Matrix liquid Crystal Display; this uses a-Si:H based thin film transistors (TFT) as the switching element in each pixel. However, under gate bias a-Si:H TFTs suffer from instability, as is evidenced by a shift in the gate threshold voltage. Two possible sources of this instability are the creation of midgap states in the a-Si:H channel and charge trapping in the gate insulator. The shift in the gate threshold voltage is generally measured from the gate transfer characteristics, after subjecting the TFT to prolonged gate bias. However, a major drawback of this measurement method is that it cannot distinguish whether the shift is caused by the change in the midgap states in the a-Si:H channel or by charge trapping in the gate insulator. In view of this, we have developed a capacitance-voltage (C-V) method to measure the shift in threshold voltage. We employ Metal-Insulator-

Semiconductor (MIS) structures to investigate the threshold voltage shift as they are much more simple to fabricate than TFTs. We have investigated a large of number Metal/a-Si:H/SiO_2/Si^{+n} and Metal/a-Si:H/Si_3N_4/Si^{+n} structures using our C-V technique. From, the C-V data for the MIS structures, we have found that the relationship between the thermal energy and threshold voltage shift is similar to that reported by Wehrspohn et al in a-Si:H TFTs (J Appl. Phys, 144, **87**, 2000). The a-Si:H and Si_3N_4 layers were grown using radio-frequency plasma-enhanced chemical vapour deposition and the SiO_2 was deposited thermally.

B11.5
CHARACTERIZATION OF THE ELECTRONIC STRUCTURE OF SiC/METAL INTERFACES USING PHOTOELECTRON SPECTROSCOPY. Joern Kohlscheen, John T. Wolan, Stephen E. Saddow, Rudy Schlaf, Univ of South Florida, Center for Microelectronics Research, Tampa, FL; Gilyong Chung, Olle Kordina, Sterling Semiconductor Inc, Tampa, FL.

We are presenting results of the investigation of SiC/metal interfaces interesting for device applications. X-ray and ultraviolet photoemission spectroscopy (XPS, UPS) combined with multi-step in-situ thin film growth were used for the determination of the electronic structure and interface chemistry of these systems. In our experiments, the interface was built up in a number of deposition steps during which the metal was grown on SiC substrates. During the growth procedure, the sample surface was characterized by XPS and UPS before deposition and after each deposition step. The resulting set of spectra allowed detailed insight into the interface formation. Injection barriers, band bending and interface dipole were determined as well as the chemical structure of the interface.

B11.6
INTERFACIAL SLIDING IN BACK-END INTERCONNECT STRUCTURES AND ITS MECHANISM. K.A. Peterson, C. Park and I. Dutta, Center for Materials Science and Engineering, Department of Mechanical Engineering, Naval Postgraduate School, Monterey, CA.

High stresses can develop in back-end interconnect structures (BEIS) of micro-electronic devices during thermal excursions because of the large differences in thermal expansion coefficients (CTE) between Si, the interlayer dielectric (ILD) and the interconnect lines. These stresses may induce local plasticity, creep or interfacial sliding within the interconnect structure. These effects are expected to become more prominent with decreasing line dimensions, and increasing ILD compliance, necessitating fundamental studies of the involved deformation mechanisms. Here we report the results of atomic force microscopy (AFM) studies of plastic deformation and interfacial sliding in stand-alone copper interconnect lines on Si, and single and bi-layer Cu-low K ILD structures on Si. The AFM measurements demonstrated that plasticity of interconnect lines, accommodated by diffusionally-controlled interfacial sliding occurs in the interconnect structure, resulting in dimensional instability. Further, studies of the cross-section of a BEIS showed evidence of distortion due to thermal cycling. To understand the mechanism of interfacial sliding, creep experiments were conducted on model planar interfaces between Al and Si, where the kinetics of diffusionally accommodated sliding at an interface loaded in shear was determined. A creep law to describe this phenomenon is proposed, and the role of interfacial morphology is discussed. It is suggested that future micro-mechanical models of BEIS must incorporate interfacial sliding in order to capture all the operative deformation mechanisms. This research was supported by NSF grant #DMR 0075281 and an SPAWAR Graduate Student Fellowship.

B11.7
ELECTRONIC TRANSPORTS ACROSS POROUS/CRYSTALLINE SILICON HETEROJUNCTIONS. Md. N. Islam, Sanjay K. Ram, Satyendra Kumar, Dept of Physics, Indian Institute of Technology, Kanpur, INDIA.

The understanding of electronic transport properties of porous silicon (PS)/crystalline silicon (c-Si) heterojunctions, is crucial in improving the electroluminenscence property of metal/PS/c-Si structures. The property of a heterojunction is determined by the interplay of the band-edge offsets and the density of defect states (DOS) within the bandgap. In order to analyze the electrical behavior of PS/c-Si heterojunctios, we studied the current-voltage (I-V) characteristics of a series of PS/c-Si junctions as a function of temperature. We found that Al/PS junctions are non-rectifying and quasi-linear whereas Al/PS/c-Si junctions are weakly rectifying having rectification ratio varying from as low as 5 up to 250 at a fixed applied bias voltage for different PS samples. Thus the rectifying behavior is due to PS/c-Si heterojunction, not Al/PS junction. Fitting the I-V data to the conventional diode equation, the diode ideality factor η was found to be about 8 for bias $\leq$0.5 V (about 50 for bias $\leq$5 V) at forward bias and nearly 1 for $\leq$0.5 V at reverse bias. As the temperature decreases, η at both forward and reverse bias increases. At reverse bias, (η-1) is inversely proportional to temperature and the reverse current exceeds forward current at small biases. These results thus suggest different current transport mechanisms operating across the PS/c-Si junctions under forward and reverse biases. We found that the barrier height measured from I-V data for $\leq$0.5 V is higher for forward bias than that for reverse bias. For high reverse biases (>5 V), the reverse current increases slowly following $\ln I \propto V^{1/2}$ law. Considering the inhomogeneous nature of PS layer and large DOS distributed spatially as well as energetically, we tried to explain our I-V results on PS/c-Si junctions by a multi tunneling-recombination model for forward bias while carrier generation-recombination and barrier lowering effects for reverse bias.

B11.8
NEW TECHNOLOGIES FOR SOLAR GRADE SILICON PRODUCTION. Sergey Karabanov, Ryazan Metal Ceramics Instrumentation Plant JSC, Ryazan, RUSSIA.

The paper deals with the analysis of different methods for solar grade silicon production: - traditional silane technology, - direct carbothermic reduction of silicon from SiO_2 - chlorine free alkoxy silane technology, - silicon production from fluorides. The experimental researches resulted in the development of the technology for solar grade silicon production using the method of carbothermic reduction with the subsequent cleaning. The research results of physical-chemical properties of the silicon obtained are given. The evaluation of ecological indices of the developed technology is presented.

B11.9
PHENOMENOLOGICAL AND ELEMENTARY REACTION ANALYSIS OF POLY-SILICON CVD PROCESS. Ryosuke Shimizu, Tadashi Januma, Masaaki Ogino, Fuji Electric Corporate Research and Development, Ltd., Matsumoto, JAPAN; Yukihiro Shimogaki, Masakazu Sugiyama, Mitsuo Koshi, Univ of Tokyo, School of Engineering, Tokyo, JAPAN.

Thickness distribution of poly-silicon thin-film was investigated by phenomenological and elementary reaction analysis in a longitudinal type CVD reactor of $\phi 6''$ manufacturing scale for the first time. Sample wafers were fully charged on the quartz boat and the 100% SiH_4 and 0.8% PH_3 gases with nitrogen carrier gas were introduced from the bottom of the reactor. The deposition temperature and pressure were 550°C and 100Pa, respectively. The thickness profile was measured with a spectroscopic ellipsometer. To analyze the experimental result phenomenologically, concentration distributions of film precursors were examined by solving basic diffusion equation for the CVD system. The analytical solution was a modified Bessel function and the experimental thickness distribution can be simulated very well with this solution by optimizing η, the sticking probability of film precursors. Three kinds of film precursors with different sticking probabilities were found to contribute the poly-silicon deposition. They are SiH_4 gas with the sticking probability 1×10^{-6}, and two kinds of radical species with 7×10^{-4} and 5×10^{-2}, respectively. Subsequently, elementary chemical reaction analysis of poly-silicon CVD process was performed based on elementary reaction mechanisms using ChemKin^{TM} and two chemical species, SiH_2 and Si_2H_6, were identified as the possible candidates for the radicals. According to these analyses, the basis deposition of poly-silicon film is due to the source precursor, SiH_4, and the profile is almost flat because of its extremely low sticking probability. While the generation rate of SiH_2 from the SiH_4 gas is very low, the extraordinary deposition around the peripheral region of wafers is explained by the large sticking probability of SiH_2. This result is important not only for improving the growth rate uniformity on the wafers, but for the filling up of poly-silicon into a high aspect ratio trenches and via-holes, and will contribute to the improvement of device performances.

B11.10
PERIODIC HEATING IN SLSI. Kal Renganathan Sharma, Vellore Institute of Technology (Deemed University), Vellore, Tamil Nadu, INDIA.

The temperature of the surface of the IC chip used in VLSI/SLSI undergoes (BSL, 1960) a periodic varition by virtue of the fluctuations in the current passing through as a result of the arithmetic operations. Take the surface of the board to be a plane we find an expression for u=(T - Tavg)/(Tmax - Tavg) as a function of z, t (the time measured after T=Tmax at z=0), and w (the frequency of fluctuations that are assumed to be sinusoidal). By postulating a solution in the form of complex temperatures and using separation of variables, De Movrie's theorem the real part of the temperature may lend itself to an expression for T. However, the parabolic equations that are used in this problem imply a infinite speed of propagation of heat. This can be corrected by the hyperbolic wave propagative equations. Using the hyperbolic partial differential equations the

expression for u is derived. These solutions are compared with each other and significance discussed.

B11.11

EVALUATION OF CONTACT AND VIA STEP COVERAGE USING A NOVEL TWO-STEP TITANIUM NITRIDE BARRIER DEPOSITION PROCESS. Ardy Sidhwa, Chuck Spinner, Todd Gandy, STMicroelectronics, Inc., Phoenix, AZ; William Brown, Simon Ang, Hameed Naseem, and Richard Ulrich, University of Arkansas, Department of Electrical Engineering, Fayetteville, AR.

Aluminum plug technologies are still used for many different semiconductor device applications and are cost-effective processes. However, there are some disadvantages associated with them. The key disadvantage is aluminum junction spiking caused by aluminum diffusing down into the silicon substrate and silicon diffusing up into the aluminum plug, due to a poor titanium nitride (TiN) barrier. The tungsten plug process is mainly used for 0.5mm and smaller technologies. Titanium nitride barrier material plays an important role as an underlayer for tungsten plugs to prevent the tungsten hexafluoride (WF6) from attacking the titanium (Ti) film. The role of the TiN barrier is to retard or prevent diffusion of the materials that the TiN layer separates. All TiN barriers are not perfect and have limited thermal budgets. Some TiN barriers may not be suitable at via levels because of high deposition temperature or chemistry. In this work, the authors investigated the TiN barrier film properties with respect to nitrogen flows at two different power set points and argon gas flows. Different experiments were performed to understand the properties of the TiN film with respect to process variables. Changes in stress of different TiN barrier films were recorded for different process variables such as nitrogen gas flows, process powers, and chamber pressures. Also, the impact of Rapid Thermal Anneal (RTP) processing on the stress behavior of different TiN barrier films was analyzed. The two-step approach results in a shift of the columnar grains as a result of stopping and reinitiating the deposition process. The shift in the columnar grains acts as a trap for any inter-diffusion through the grain boundaries. Furthermore, the dual- or two-step barrier process provides a thicker sidewall and bottom TiN step coverage than a standard one-step barrier process, particularly for high aspect ratio conditions for contact and via openings.

B11.12

SOLUTION-BASED PRECURSOR DELIVERY FOR COPPER CVD. Lidong Wang, Greg Griffin, Louisiana State University, Dept of Chemical Engineering, Baton Rouge, LA.

We have measured the growth rates for copper CVD using Cu(hfac)2 dissolved in isopropanol as the precursor delivery method. This approach offers the convenience and control associated with liquid precursor delivery, while avoiding the high melting point of this precursor. The new method provides similar growth rates to those observed using conventional delivery (i.e., sublimation of solid precursor), but these rates are achieved using a much lower partial pressure of precursor in the reactor. The deposition rate is initially first-order with respect to precursor pressure, but saturates at high values. The rate is also first-order with respect to hydrogen partial pressure. Increasing the hydrogen pressure also shifts the point at which precursor saturation occurs. The isopropanol component has a smaller and more complex effect on the kinetics. Measurements of surface roughness and film resistivity indicate that the initial films are discontinuous (i.e., for film thickness less than 100 nm). The film properties also do not appear to depend strongly on the gas phase reactant composition. These results suggest that surface diffusion is primarily responsible for initial film morphology.

B11.13

POSSIBLE RELATIONSHIP BETWEEN FERMI LEVEL PINNING AND INDUCED NET CHARGE DENSITY AT NON-INTIMATE METAL/SILICON INTERFACE. Bruno Cvikl, Faculty of Civil Eng., University of Maribor, Maribor, SLOVENIA; J. Stefan Institute, Ljubljana, SLOVENIA.

It has been shown recently that the, reverse biased excess capacitance of various metal/Si Schottky junctions [1] is an direct outside manifestation of the existence of the net charge density as induced at the appropriate interface. This net charge density has been shown to be external bias dependent and its magnitude appears to be strongly related to the deposition method chosen of a given metal/ semiconductor junction formation. The induced, interfacial net charge density, provides the basis for the calculated effective density of states, EDOS, of the pertinent charge carriers, respectively. The deduced spectrum, a local quantity characterizing the charge distribution at the interface, extends over the semiconductor energy gap and is characterized by sharp spikes. The amplitude of spikes are periodically modulated and their envelopes appear as identical, lorentzian like curves. The finite number of lorentzians slightly overlap and are uniformly distributed over the energy gap, however the spikes density within each lorentzian monotonically increases on approaching the conduction band minimum. In this work the question as to what extent the above described spikes densities, specifying the local effective density of gap states at the metal/semiconductor interface, could be associated with the Fermi level pinning position in silicon will be examined. In this respect the correlation of various published values of Schottky barrier heights for Ag and Pb metal/Si junction with the peak positions of the calculated EDOS is being investigated in detail. In the study, our results as obtained by the ionized cluster beam deposition method for various values of the Ag and Pb metal ions acceleration voltages, appear to relate rather well with the peak positions of the calculated EDOS values. It is also for this reason that the findings are to be contrasted with the Drummond's [2] predictive model of various near surface defects in GaAs, claimed to be the origin of several Fermi level pining levels for this compound. Some possible applications of the findings above as related to physics of semiconductor devices will be also discussed. [1] B. Cvikl and D. Koroöak, J. Appl. Phys, to be published. [2] T.J. Drummond, Phys. Rev. B59, 8182 (1999).

B11.14

NEAR-FIELD ULTRASONIC IMAGING: A NOVEL METHOD FOR NONDESTRUCTIVE SUBSURFACE IMAGING OF IC INTERCONNECT STRUCTURES. Gajendra S. Shekhawat, Huimin Xie, Yuegui Zheng, and R.E. Geer, Univ. at Albany Institute for Materials, Albany, NY.

Nondestructive subsurface imaging is of great interest for back-end-of-line (BEOL) integrated circuit (IC) interconnect structures due to the need to quickly identify subsurface voids in damascene metal lines and mechanical defects in metal/low-k structures. Conventional acoustic microscopy has found limited application in subsurface imaging of BEOL interconnect structures due to its poor spatial resolution ($\sim$ micron). The single greatest challenge results from high-frequency transmission losses in far-field acoustic lenses that limit spatial resolution. In this work we report on the development of an alternate approach to nondestructive, nanoscale, subsurface imaging for IC interconnect structures: Near-field ultrasonic imaging. This approach utilizes a heterodyne interferometer based on a scanning probe microscope, similar to so-called heterodyne force microscopy (HFM). Ultrasonic excitation of super-resonant vibrations in an SPM cantilever probe are combined with ultrasonic waves applied to an IC interconnect test structure. Subsequent heterodyne interference between these two signals is observed assuming a nonlinear tip-sample interaction. This interference is sensitive to the relative phase difference of the two ultrasonic excitations and enables phase-sensitive imaging. Proof-of-feasibility demonstrations of this technique are presented for ultrasonic phase-imaging of Cu/low-k interconnect structures for a range of ultrasonic carrier frequencies. Spatial resolution $<$10 nm is demonstrated. These results are compared to simulations based on the Johnson-Kendall-Roberts (JKR) model for the mechanical interactions of a scanning probe tip with a surface. Calculations for depth and in-plane mechanical resolution are presented in terms of surface and subsurface contributions to the phase image for Al/low-k and Cu/low-k IC interconnect test structures.

B11.15

STUDY OF Ta_2O_5 BASED MOS CAPACITORS, WITH Ta, OXIDIZED IN O_2:NH_3 AMBIENT. Pallavi Krishnamoorthi, A.N. Chandorkar, Dept of Electrical Engineering, IIT Bombay, INDIA.

Tantalum Pentoxide, an alternative to SiO_2, as a high-k dielectric for DRAM and MOS applications, faces the problem of interface mismatch at silicon. SiO_2/Si_3N_4 interface layer were suggested to overcome the interface problem. Here we study the physical and electrical characteristics of Ta, oxidized in O_2:NH_3 ambient, and without any other interface layer. This is done to check if N/H moves to the interface, and thus improves the electrical properties. However XRD studies of the film, showed the presence of $TaSi_2$, unoxidized Ta and TaN in the film. But the intensity of these peaks decreased with the reduction of NH_3 content. Thus a higher oxygen content could probably reduce the content of TaN and unoxidized Ta. FTIR analysis however showed strong Ta=O and Si-O peaks. For the MOS capacitors, due to the presence of resistive components, the maximum capacitance was reduced, compared to that of pure Ta_2O_5 films. V_{fb} varied from 1.1-1.9V. Oxide charges in the films varied from 3-6e12/cm^2. But the traps in these films were found to be almost negligible as observed from the hysteresis of C-V characteristics. Films with N/H showed lesser oxide charges by one order of magnitude, as compared to pure Ta_2O_5 films.

B11.16

CHARACTERISTICS OF REMOTE OXYGEN AND HYDROGEN PLASMA DRY CLEANING OF FLUOROCARBON RESIDUES FORMED AT THE CONTACT HOLES. Hongkwon Youn, Sung Bae

Kim, Hyungtak Seo, Jongkook Song, Yangdo Kim, Hyeongtag Jeon, Hanyang Univ, Div of Materials Science and Engineering, Seoul, KOREA; Hyun Soh, Young Chai Kim, Hanyang Univ, Dept of Chemical Engineering, Seoul, KOREA.

Reactive ion etching (RIE) using fluorocarbon is widely used to open contact holes due to its high anisotropic and selective silicon etching characteristics. However, the RIE process induces nonvolatile and chemically stable fluorocarbon residues and these residues typically cause high contact resistance at the metal-silicon interface. Moreover, it is very difficult to remove such residues completely in high-aspect ratio structure especially with sub-micron diameter contact hole size. In previous reports, the oxidizing process followed by wet chemical stripping, dipping in hydro sulfuric acid (H_2SO_4) and hydro fluoric (HF) acid based chemicals, was the most effective method to remove fluorocarbon residues. However, a large quantity of these wet chemicals increased the process cost and caused significant environmental problems. In this study, low temperature remote plasma dry cleaning process that removes both the PR and polymer residues containing carbon and fluorine after RIE process has been investigated. The cleaning efficiencies of remote oxygen and hydrogen plasma were systematically evaluated at various conditions such as plasma power, exposure time, gas flow rate and sample temperature. Remote plasma was used to minimize plasma damage by keeping the substrate distant from discharge region. Preliminary results showed that the hydrogen plasma cleaning was necessarily required to remove the residual carbon contaminants on silicon surface after oxygen plasma cleaning. Also, two step cleaning, oxygen plasma ashing and subsequent hydrogen plasma cleaning, was very effective to remove carbon residues and polymer without forming SiO_2 layer on silicon surface after cleaning process.

B11.17
EFFECTS OF BOROPHOSPHOSILICATE GLASS DOPANT CONCENTRATIONS ON ISOTROPIC ETCH PROFILE. Chris Gibson, Bradley R. Williams, Stacey Evans, AMI Semiconductor, Inc., Pocatello, ID.

In the process of chemically etching contact openings, film characteristics of the borophosphosilicate glass (BPSG) film strongly effect the formation of an ideal contact profile. Ideal contact profiles represent a wine glass shape to provide better metal step coverage in to the contact opening in comparison to a vertical sidewall profile. The rounded shape of the wine glass is etched chemically (isotropic) allowing for etch in the vertical and horizontal direction. As the addition of dopants to the oxide film effect the etch rate, the profile of the isotropic etch will change which in turn effect electrical device properties, down stream processes and device reliability. BPSG film characteristics are the area of investigation. Characteristics of concern are weight percent concentrations of boron and phosphorus, film density and dopant concentration profiles in relation to depth. To evaluate the entire contact formation module, chemical etch characteristics including etch rate in relation to film depth for thermal oxide films were also investigated. Experimentation in the form of a response surface design was used to model effects of previously discussed BPSG film characteristics. To achieve the desired and predictable wet etch rate of BPSG in a buffered oxide etch (BOE) calculated control limits were placed on the boron and phosphorous dopant concentrations. Results showed that dopant effects on the isotropic etch process exceeded the control capability of dopant concentrations in the deposition process. In relating process control capabilities to 6s techniques, a Cpk above 1.5 is considered capable. To eliminate previously discussed defects created in the isotropic etch process, reject limits for dopant concentrations in BPSG film deposition process would need to be set well within the typical 6s giving a Cpk below 1.5.

B11.18
EPITAXIAL GROWTH OF $CoSi_2$ ON Si(100). Ryan Chong, Mark Yeadon, Shue Yin Chow and Chaw Sing Ho.

Epitaxial silicides are of interest in advanced CMOS front-end-process technology for shallow source/drain contacts of higher thermal stability and lower interfacial roughness than their polycrystalline counterparts. We report the synthesis of epitaxial $CoSi_2$ on Si(100) by a reactive deposition technique. Using real-time in-situ transmission electron diffraction and microscopy under UHV conditions (MERLION system) we observe the direct formation of $CoSi_2$ on the Si(100) surface with no intermediate phase formation. The experimental data will be compared with the deposition and anneal of Co on the clean (2x1) reconstructucted Si(100) surface. Under these conditions, the formation of polycrystalline $CoSi_2$ was observed, as expected. The mechanisms of epitaxial silicide formation were elucidated from video recordings of the growth process which will be discussed.

B11.19
Cu PATTERNING USING A SELF-ALIGNED MgO MASK Yeonkyu Ko, Heejung Yang, Jaegab Lee, Kookmin Univ, School of Metallurgical and Materials Engineering, Sungbuk-Gu, Seoul, KOREA.

Development of a Cu patterning method has been one of the most important technical processes that need to apply for the gate electrodes of thin film transistor liquid crystal display (TFT-LCD). A self-aligned surface MgO layer was used as a mask in the new process. The surface MgO layer was formed by diffusion of Mg from Cu film to free surface. Cu(4.5at%Mg) film having thickness of 4000 Å was annealed in O_2 ambient at 10 mTorr, 500° for 30min, followed by patterning of the MgO layer using photolithography and HF wet etch process. The patterned Cu alloy film was exposed to O_2 plasma ambient and H(hfac) gas was simultaneous flowed toward the film for dry etching. Total pressure of O_2 and H(hfac) in the reactor was constantly maintained at 200 mTorr (O2/H(hfac) = 1:1).
The self-aligned MgO films successfully played a role of mask for dry etching the Cu(Mg) films with a taper slope. A a-Si:H TFT was fabricated with the dry etching process. The a-Si:H TFT using the MgO mask showed good subthreshold slope, on/off current ratio, and output characteristics.

B11.20
THE EFFECT OF THE MICROSTRUCTURE OF DIFFUSION BARRIERS ON THE PALLADIUM ACTIVATION FOR ELECTROLESS COPPER DEPOSITION. Seok Woo Hong, Yong Sun Lee, Jong-Wan Park, Div. of Materials Science and Engineering, Hanyang University, Seoul, KOREA; Ki-Chul Park, Samsung Electronics, Kyungki-Do, KOREA.

Cu is being widely used in ULSI metallization process as a replacement for Al due to its lower resistivity and higher electro-migration resistance. Electroless Cu deposition is one of the candidates for Cu processing because of low cost and high quality of electroless Cu films. Copper can be deposited on a catalytic surface from an ionic solution without any external power supply by electro-less plating. The electroless copper reaction is an autocatalytic reaction. This means that once there is an initial layer of copper, the reaction continues indefinitely. Since the surface on which electroless copper is deposited is not catalytic, an activation process is usually needed to start the electroless reaction. Gold, platinum, or palladium is required as catalytic layer for reliable electroless copper deposition, so the activation process is a key process for successful copper electroless plating. In this paper, palladium activation on dc magnetron sputtered TiN and TaN as diffusion barriers for auto-catalytic electroless copper deposition has been investigated by using X-ray diffraction, sheet resistance measurement, field emission scanning electron microscopy, plan view transmission electron microscopy (TEM). The density of palladium nuclei on TaN diffusion barrier was increased with decreasing the grain size of TaN films which was caused by increasing nitrogen content in TaN films. Plan view TEM results showed that palladium nuclei formed mainly on the triple points of the grain boundaries of the TiN diffusion barriers.

B11.21
POST BLAST COMPONENT CLEANING TECHNIQUES TO REDUCE PARTICLE GENERATION IN ETCH AND DEPOSITION CHAMBERS. Ronald Burgess, Dave Laube, BOC Edwards-Kachina, Phoenix, AZ; Ardy Sidhwa, Chuck Spinner, Sanyi Zheng, Tin Bun Chew, Todd Gandy, Steve Melosky, Jerome Vetier, ST Microelectronics, Phoenix, AZ.

Particles emanating from walls, shields and other components of the chambers in which integrated circuit wafers are processed, are among factors which have been shown to contribute to the formation of defect sites on completed wafers. Typically, the generation rate of particles is influenced by the final treatment that the surfaces of these components receive prior to installation in the chamber. Quartz coupons, prepared from material characteristic of contemporary bell jar manufacture, were subjected to typical post cleaning steps. These were surface texturing, post blast etching, pressure washing and ultrasonic rinsing. The relative effectiveness of these steps was assessed with a conventional experimental matrix. The coupons were evaluated for potential particle generation by two methods. First, carbon liftoff techniques were used to evaluate relative numbers of weakly attached particles on the surface of the coupons. Secondly, cross sections were prepared to examine the depth and type of subsurface damage capable of contributing to particle generaltion. Current methods to promote adhesion of deposits to PVD shielding require increasing surface roughness by abrasive blasting. This technique is known to embed fractured grit particles into the metal substrate. Cleaning processes intended to remove micro-particles following grit blast are only marginally successful. This experiment was designed to optimize post grit blast processing for embedded grit removal. Stainless steel samples, prepared from used shield

components, were utilized in a matrix to evaluate the effectiveness of ultrasonic agitation, chemical etching, and CO_2 pellet blasting at removing embedded grit. These samples were analyzed using beta backscattered electron imaging. Subsequently, samples were subjected to thermal cycling representative of that experienced in chamber operation, to determine whether any remaining grit would be released as a result of these temperature excursions. Particle count data, obtained from actual production operations, is presented to demonstrate the effectiveness of post blast cleaning techniques.

B11.22
A NOVEL Cu/LOW-k INTEGRATION TECHNOLOGY BY Cu LINE-PILLAR PROCESS. Seiichi Shishiguchi, Takuya Fukuda, Hiroyuki Kochiya, Hiroshi Yanazawa, Association of Super-Advanced Electronics Technologies (ASET), Yokohama, JAPAN.

The Cu/low-k integration has become essential in order to reduce RC-delay of interconnect-lines. In this regard, a Cu dual-damascene process has been proposed and has actually applied to the high-end ULSIs. As the device size shrinks toward 100nm technology-node, the damascene structure will require more difficult technologies, such as the etching of low-k material and the deposition of conformal and thinner metal-layers into the smaller feature size. The need to reduce the k value of dielectrics will make the CMP process more difficult, because materials become more fragile as k becomes smaller. This paper describes a new concept of Cu/low-k integration that solves the above problems. The technology does not employ CMP, and involves the following three process steps. First, photoresist is patterned on a Cu seed-layer and photoresist spaces are filled by the electroplated Cu. Cu lines or pillars are formed by the removal of the PR/seed/adhesion layers. Second, a low-k film is transferred by STP (spin coating, film transfer, and hot pressing), which involves spin-coating a low-k material on a base film, and then transferring it to the Cu line/pillar substrate by pressing and heating in a vacuum. Gap-filling and surface-planarization are realized after the removal of the base film. Third, the top surface of the Cu line/pillar is revealed by the low-k etch back. In experiments, x-ray lithography was used for the photoresist patterning. Pulse current mode was applied for the Cu electroplating to relax the Cu plating stress. An organic low-k material (k=2.9) was used for the STP process. The formation of Cu lines and the low-k gap fill as well as the surface planarization were successfully demonstrated. This work was performed under the management of ASET in METI's R&D program supported by NEDO.

SESSION B12: LOW-k DIELECTRICS
Chairs: Jeffrey A. Lee and Paul S. Ho
Friday Morning, April 5, 2002
Salon 10-12 (Marriott)

8:00 AM B12.1
CROSS-SECTIONAL ELASTIC IMAGING OF COPPER AND LOW-k IC INTERCONNECT STRUCTURES FOR MECHANICAL ANALYSIS/METROLOGY AND DEFECT IDENTIFICATION. Lata Muthuswami, Huimin Xie, G.S. Shekhawat, Katherine Dunne, R.E. Geer, University at Albany Institute for Materials, Albany, NY.

One of the most difficult challenges in the integration of Cu and low-k materials in integrated circuit (IC) processing concerns the significant mismatch of mechanical properties (Young's modulus, shear modulus, Poisson's ratio, coefficient of thermal expansion) between metals and most low-k dielectrics. Recently, a technique based on ultrasonic force microscopy (UFM) has been developed to enable nondestructive nanometer-scale elastic imaging of as-processed structures. UFM has successfully been used to image RIE-induced hardening of patterned low-k dielectrics and mechanical modification of such dielectrics due to chemical mechanical planarization (CMP). To complement this technique we report on the development of cross-sectional elastic imaging of IC interconnect structures via cross-sectional UFM (CS-UFM). A CS-UFM protocol has been developed to successfully image the elastic profiles of cross-sectioned Al/silicon oxide, Cu/silicon oxide, and Cu/low-k interconnect structures with a spatial resolution <5 nm. CS-UFM imaging reveals mechanical defects and non-uniformities in low-k dielectrics. Specifically, intra-trench variation of mechanical response is shown. Also, subsurface compositional defects have been imaged within low-k dielectrics. Likewise, CS-UFM has been used to image voids in Cu-filled trenches/vias. The cross-sectional elastic imaging maps of the IC interconnect structures are compared to finite element analysis (FEA) models as well as empirical elastic-response models to estimate the mechanical sensitivity of CS-UFM and calibrate the nanoscale image intensity to the elastic moduli of the interconnect metal, barrier, and dielectric. A modulus sensitivity $<2\%$ is demonstrated.

8:15 AM B12.2
A CORRELATION STUDY OF THERMAL STABILITY ON POROUS LOW-k. Y.F. Chow, T.H. Foo, Y.J. Yuan, Y.H. Wang, A.Y. Du, S.Y. Wu, C.Y. Li, R. Kumar, P.D. Foo.

The thermal stability on organic porous low-k, P-SiLK with dielectric constant about 2.4, has been studied. The effects of thermal cycles on porous low-k film such as shrinkage, refractive index, dielectric constant, pore size, hardness and Young's modulus are investigated. Film is spun on silicon substrate, baked and cured in the vertical furnace for 1 hour at 430°C under N2 ambient. Thermal cured is done in the vertical furnace with oxygen level less than 10 ppm. Two curing temperatures (430°C and 450°C) are applied and compared the thermal stability after several thermal cycles. Each thermal cycle is one hour but the film is checked for every alternate cycle. We observed that after the first thermal cycle of 450°C and 430°C cured, the refractive index is increase and about 0.8% and 0.4% respectively. Dielectric constant is slightly increased after 450°C cured but that is no significant change for 430°C cured. Change in film properties are investigated and evaluated by using opti-probe, FTIR, mercury probe, nano-indentation and TEM. Organic low k material SiLK with dielectric constant about 2.8 is used as a baseline for comparison.

8:30 AM B12.3
CHARACTERISTICS OF LOW-k AND ULTRALOW-k PECVD DEPOSITED SiCOH FILMS. A. Grill, V. Patel, K. Rodbell, S. Christiansen and E. Simonyi, IBM Research Division, T.J. Watson Research Center, Yorktown Heights, NY.

We have shown previously that the dielectric constants of PECVD prepared SiCOH dielectrics can be extended to ultralow-k values of k=2.0. The reduction in the dielectric constants has been achieved by adding an organic precursor to the tetramethylcyclotetrasiloxane (TMCTS) used for the preparation of the SiCOH dielectric and annealing the films to remove the thermally less-stable organic CHx fractions from the films to add porosity and reduce the density of the films.
In order to estimate the effects of the reduction of the values of the dielectric constant on the properties of the material, the films have been characterized by RBS and FRES, FTIR, positron annihilation spectroscopy, TEM, AFN, nanoindentation measurements, stress vs temperature and photothermal deflection measurements. The obtained characteristics of the films will be presented and discussed as a function of the deposition conditions and in relation to the dielectric constants.

8:45 AM B12.4
A NEW ULTRA-LOW-k ILD MATERIAL BASED ON ORGANIC-INORGANIC HYBRID RESINS. Ben Zhong[a], Cory Bargeron[a], Ken Weidner[a], Herman Meynen[b], Paul Schalk[a], Alan Peck[a], Stephane Mailhouitre[c], Marleen Van Hove[c], Karen Maex[c]; [a]Dow Corning Corporation, Midland, MI; [b]Dow Corning Corporation, Seneffe, BELGIUM; [c]IMEC, Heverlee, BELGIUM.

A ULK material based on a siloxane resin has been developed that can be coated on silicone wafers by spin-coating, and both cured and rendered porous by a simple thermal treatment in an inert atmosphere. The chemical bonds between the resin and porogen groups prevent the phase separation of the porogen from the resin during curing and lead extremely small pores. The highly hydrophobic thin films made from this material displayed Dk of 1.8, breakdown voltage of 4 MV/cm, a cohesive strength $>$ 60 MPa, excellent crack resistance, and an average pore size of 2.2 nm by PALS and 2.5-3.0 nm by EP. In this presentation, our strategy for designing low-k materials, the material properties and integration results for this new material will be discussed.

9:00 AM B12.5
A NEW APPROACH OF THIN-FILM X-RAY REFLECTANCE/SCATTERING ANALYSIS FOR ULTRA-LOW-k DIELECTRICS WITH PERIODIC PORE STRUCTURES. N. Hata, MIRAI-AIST, Tsukuba, JAPAN; Y. Oku, K. Yamada, MIRAI-ASET, Tsukuba, JAPAN; Y. Azuma, I. Kojima, NML-AIST, Tsukuba, JAPAN; T. Kikkawa, MIRAI-AIST and Hiroshima Univ., Higashi-Hiroshima, JAPAN.

We propose and demonstrate experimentally a new structural characterization technique for ultra-low-dielectric-constant thin films with periodic porous structures by employing a new analytical approach to X-ray reflectance / scattering data. The analytical approach which we propose here takes specular reflection, incoherent scattering from random distribution of, and coherent scattering from periodically modulated distribution of electron density into account. Thin-film measurements by reflectance and scattering of X-ray are known for their advantages in sensitivity and non-intrusiveness. Interlayer dielectrics with dielectric constant (k) less than 1.5 will be required in future integrated circuit technology for high enough transmission speed of signal and for low enough energy consumption. On the other hand, candidate materials ever been studied, do not

show k values well below 2 without inclusion of pores or open volume structures in them. As the pore volume fraction is increased for lower k value, pore connectivity increases for random distribution of pores, resulting in increase of average (connected) pore volume and hence in deterioration of film mechanical properties. Efforts to introduce periodicity in pore structure are undertaken to resolve the problem. Once the periodicity is introduced, however, the above-mentioned X-ray measurement techniques start to suffer from the signal associated with the anisotropy and coherent scattering or diffraction from the periodic modulation of electron density, and new approaches become needed to obtain information not only about the periodic structure itself, but also about the residual random structure in the "wall" material as well as about the overall structural disorders; all those parameters are important in assessing relationship between k and such essential properties for integration as mechanical properties, stability and reliability. By comparing the experimental data taken under specular reflection and off-angle scattering both in out-of-plan and in-plain geometries with the proposed model calculation, the contributions from the origins are successfully separated.

9:15 AM B12.6
NOVEL PERIODIC NANOPOROUS SILICATE GLASS WITH HIGH STRUCTURAL STABILITY AS LOW-k THIN FILMS. Yoshiaki Oku, MIRAI-ASET, Ibaraki, JAPAN; Norikazu Nishiyama, Shunsuke Tanaka, Korekazu Ueyama, Osaka Univ, Dept of Chemical Engineering, Osaka, JAPAN; Nobuhiro Hata, MIRAI-AIST, Ibaraki, JAPAN; Takamaro Kikkawa, MIRAI-AIST, Ibaraki, JAPAN and Hiroshima Univ, Research Center for Nanodevices and Systems, Hiroshima, JAPAN.

Reduction of interconnect parasitic capacitances has become more important issue to fabricate high-speed ULSIs for 100 nm technology node and beyond. In order to meet with this requirement, various intermetal dielectric films with low dielectric constant (low-k films) have been developed. Introducing pores (air) into dielectric materials is an efficient method to fabricate low-k film with dielectric constant less than 2.0, because the dielectric constant of air is 1.0. Conventional porous films, however, did not have enough mechanical strength and electrical properties as expected. Therefore, pore formation technology in dielectric film must be improved for development of low-k (k=1.5) for 70 nm technology node. We have developed a novel periodic nanoporous silicate glass with high structural stability as a low-k thin film by spin-coating method. Conventional porous silicate glass films have caused structural shrinkages (10-20% or more) by calcination of the spin-coated films. In this investigation we adopt special treatment before calcination. Our novel nanoporous film shows no shift of XRD peak position after calcination at 673K, indicating that both the ultimate mechanical strength and the minimization of stress at the interface between the prepared film and the underlying substrate can be achieved. Such a shrinkage-free periodic nanoporous silica film can possess higher V_{BD} (break down voltage) and lower I_{LEAK} (leak current). In this study we evaluated electrical properties (dielectric constant, V_{BD} and I_{LEAK}) by IV and CV measurements, structural properties (including information on pores) by XRD, XRR, TEM, and mechanical properties (hardness and Young's modulus) of this special-treated novel nanoporous silica film. The dielectric constant was evaluated to be around 1.5 at 1MHz.

10:00 AM B12.7
POROUS METHYLSILSESQUIOXANE LOW-k DIELECTRIC FILMS: MECHANICAL BEHAVIOR, MOISTURE SENSITIVITY, AND RELIABILITY. Dan Maidenberg, Stanford Univ, Dept of Materials Science and Engineering, Stanford, CA; Robert Miller, Willi Volksen, IBM Almaden Research Center, San Jose, CA; Reinhold Dauskardt, Dept of Materials Science and Engineering, Stanford, CA.

Methylsilsesquioxane (MSSQ) films are primary candidates to replace silica as the interlayer dielectric in future generations of micro-electronic devices. More importantly, the dielectric constant of MSSQ is continuously tunable with the incorporation of porosity at the nanometer length scale. However, before integration is possible it is necessary to understand and quantify the mechanical and fracture behavior of these thin films. Specifically, the addition of porosity may have detrimental effects on many of the required mechanical properties, which will reduce survivability during CMP and lower the resistance to electromigration back stresses during operation. The effect of porosity on a range of salient mechanical properties including inherent fracture resistance, adhesion, and elastic modulus will be addressed for several resin formulations. Various other factors, including surface modification with UV-ozone, will be presented. The implications of different matrix microstructures and pore architectures are discussed.

10:15 AM B12.8
THERMAL STABILITY STUDIES ON 2,4,6,8-TETRA-METHYLCYCLOTETRASILOXANE (TMCTS). Chongying Xu, Alexander S. Borovik, Ziyun Wang, Jose Arno and Thomas H. Baum, ATMI, Inc., Danbury, CT.

2,4,6,8-Tetramethylcyclotetrasiloxiane (TMCTS) is being considered as a precursor for CVD of low dielectric constant (k) thin films as interlayer dielectrics in an integrated circuit. Recently, it was reported that TMCTS polymerizes in delivery lines in a CVD process tool. To combat this problem, we conducted a series of chemical studies on TMCTS thermal behaviors under various process conditions. For instance, TMCTS was heated in the presence of 316L stainless steel, acids, bases, water and various drying agents. The TMCTS then was studied by NMR, FT-IR and GC-MS. Our results indicate that TMCTS is readily polymerized in the presence of moisture with acids and bases. We have developed an ultra-dry TMCTS and a new method to determine water content in TMCTS that allows us to control TMCTS quality. In this paper, we will report our results on TMCTS thermal stability studies.

10:30 AM B12.9
ELECTROMIGRATION IN SUBMICRON DUAL-DAMASCENE Cu/LOW-k INTERCONNECTS. Ki-Don Lee, Xia Lu, Ennis T. Ogawa, Hideki Matsuhashi, and Paul S. Ho, The University of Texas at Austin, Microelectronics Research Center, Austin, TX; Volker A. Blaschke, and Rod Augur, International SEMATECH, Austin, TX.

Electromigration (EM) lifetime characteristics and failure mechanism have been investigated for Cu/SiLK and Cu/porous MSQ interconnects as compared to Cu/oxide interconnects. SiLK is an organic polymer developed by the Dow Chemical Company with k of 2.7 and Porous MSQ is a spin-on porous silicate with k of 2.4. The activation energies were found to be 0.97 eV for SiLK and 0.80 eV for the porous MSQ, similar to that of oxide. This range of activation energies suggests a similar mass transport mechanism, interfacial diffusion. The current exponent of SiLK and oxide were found to be 1.1 and 1.2, respectively. Using focused ion beam (FIB) microprobe, distinct failure mechanism for Cu/low-k interconnects due to lateral Cu extrusion at the anode under the cap layer has been observed and it seems to be related to thermomechanical properties of low-k materials. The short lifetime characteristics of low-k interconnects can be attributed to a smaller back stress due to smaller confinement effect. The critical length effect has been found to be smaller for Cu/low-k than for Cu/oxide. Results obtained in this study indicated that thermomechanical properties of low-k interconnects, including interfacial adhesion, failure mode of low-k material, joule heating, mechanical strength (E) and CTE are important parameters in controlling EM reliability of Cu/low-k interconnects.

10:45 AM B12.10
EFFECT OF ULTRA-VIOLET ANNEALING ON PHYSICAL AND ELECTRICAL PROPERTIES OF HIGH PERMITTIVITY DIELECTRICS DEPOSITED BY PHOTO-ASSISTED CHEMICAL VAPOUR DEPOSITION. B.J. O'Sullivan, P.K. Hurley, NMRC, University College, Cork, IRELAND; Q. Fang, J.Y. Zhang, I.W. Boyd, Dept of E&EE, University College-London, London, UNITED KINGDOM; J.P. Senateur, INPG, Grenoble, FRANCE; T.L. Leedham, Inorgtech, Suffolk, UNITED KINGDOM; C. Jimenez, JIPElec, Crolles, FRANCE.

The results of an experiment designed to investigate the effects of post deposition ultra-violet (UV) assisted O_2 annealing on the properties of high-permittivity (κ) films on silicon are reported. Although previous work has demonstrated low temperature (350-400°C) post deposition UV O_2 annealing can improve the physical and electrical properties of high-κ films [1], the mechanism is not fully understood. The high-κ film chosen for the experiment was Ta_2O_5 fabricated by UV assisted Injection Liquid Source Chemical Vapour Deposition (UVILS-CVD) on Si(100) substrates. The UVILS CVD technique allows the high-κ deposition and post deposition annealing to be performed in the same reaction chamber. Leakage current densities are reduced by up to six orders of magnitude as a result of a 350°C post deposition UV O_2 anneal. The anneal step increases both the refractive index (2.01 to 2.21) and film stoichiometry (Ta:O, 1:2 to 1:2.47). From SIMS analysis, this improvement has been attributed to the removal of Si, N and C from the bulk of the dielectric layer during the anneal. The UV anneal in O_2 creates oxygen free radicals and ozone (the O_2 bond strength is 5.17 eV; the UV photon energy is 5.68 eV). It is proposed that these contaminants are removed in the gas phase (CO, CO_2, SiO, NO, N_2O...), following a reaction with oxygen free radicals. In addition, the UV O_2 irradiation provides O free radicals to the as-deposited suboxide, which is evidenced by the increase in the stoichiometry of the film after the 350°C UV O_2 anneal. Results will be presented on post deposition UV anneal experiments performed in vacuum conditions, which support this theory. The technique is currently being extended to alternative high-κ dielectrics, including HfO_2 and mixed Ta_2O_5-TiO_2 layers, formed using carbon based metal-organic precursors. [1] J. Zhang et. al., J. Phys. D: Appl Phys, 32, L91, (1999).

11:00 AM B12.11
POROSITY EFFECT ON THERMOMECHANICAL PROPERTIES OF ORGANOSILICATE FILMS. Dongwen Gan, Junjun Liu, Paul S. Ho, The University of Texas at Austin, Microelectronics Research Center, Austin, TX; Willi Volksen and Robert D. Miller, IBM Almaden Research Center, San Jose, CA.

Degradation of the thermal and thermomechanical properties with porosity is a key concern regarding the implementation of ultra low dielectric constant (low-k) porous materials. In this study, a bending beam technique designed to measure thermal stress, biaixal modulus, coefficient of thermal expansion (CTE) and Poissons ratio of thin films[1] was used to investigate the thermomechanical behavior of the porous Methylsilsesquioxane (MSSQ) films prepared by incorporation of macromolecular "porogens"[2]. The stress of the films with a porosity range from 0% to 50% was measured during thermal cycling at a ramping rate of 2°C/min. It was shown that the stress decreased linearly with the increase of temperature and decreased with porosity at any given temperature. As a function of the biaxial modulus and CTE the film, the slope of the temperature-stress curve was calculated as a function of porosity. It decreased with porosity and a sharp drop appeared around 20% porosity. Compared with the thermal conductivity measured by the 3ω technique[3] and the dielectric constant of the films, the modulus demonstrated a much more profound transitional behavior. It is suggested that the sharp drop is due to a transition in pore morphology from closed cell to interconnected open cell structure at the percolation limit.
[1] Zhao, Jie-Hua et al., Journal of Applied Physics, Vol. 88 (5), 3029, September 1, 2000.
[2] R.D. Miller et al., Mat. Res. Soc., Symposium Proceeding, Vol. 565, p.3 (1999).
[3] C. Hu et al., Mat. Res. Soc. Symposium Proceeding, Vol. 565, p. 87 (1999).

11:15 AM B12.12
INTERFACIAL ADHESION STUDY OF POROUS LOW-k TO CVD BARRIER LAYERS. Caroline C. Merrill, Paul S. Ho, Univ. of Texas, Microelectronics Research Center, Austin, TX; Jeffrey A. Lee, Jeffrey T. Wetzel, International Sematech, Austin, TX.

The drive for smaller and faster microelectronic devices has led to the introduction of Copper metallization and low-permittivity (low-k) dielectric materials for interconnect structures. The weak thermo-mechanical properties of low-k dielectrics cause serious concerns on reliability and integration of Cu/low k interconnects. Indeed, during fabrication, thermal stresses arise due to mismatching in coefficients of thermal expansion (CTE) and elastic properties of the materials. The interfacial adhesion of thin films becomes critical to the integration and reliability of low-k materials. This paper will present the results from an application of the 4-point bending technique to characterize the adhesion strength of ultra low-k dielectric materials to CVD barrier layers. Adhesion energy between an ultra low-k dielectric material and a barrier layer was measured as a function of porosity ($2.0 < k < 2.3$). It was found that the fracture energy decreases with the dielectric constant which correlates with mechanical properties such as Young's modulus and hardness. Adhesion measurement data were also obtained for different low-k / Barrier layer interfaces. The independence of energy on the type of interface suggests that the fracture is actually occurring in the low-k material and not at the interface. In addition, the very low fracture energies ($G < 3$ J/m^2) confirm the weak mechanical properties of such materials. Results will be illustrated with failure surfaces analysis using Auger electron spectroscopy and scanning electron microscope.

11:30 AM B12.13
NANOINDENTATION OF SILICATE LOW-k DIELECTRIC THIN FILMS. Joseph B. Vella, Alex A. Volinsky, Indira S. Adhihetty, Motorola, Digital DNATM Labs, Process and Materials Characterization Lab, Mesa, AZ; William W. Gerberich, University of Minnesota, Dept. of Chem. Eng. and Materials Science, Minneapolis, MN.

Due to the radical compromise in thermal and/or mechanical properties that the migration from silicon dioxide to novel low-k dielectric films necessarily incurs, the IC industry is motivated to better understand the failure modes of low-k dielectric films. These failure modes include thermal instability, poor mechanical strength, and chemical-mechanical polishing (CMP) failure due to low cohesive and adhesive fracture toughness. Studies performed at SEMATECH have indicated that CMP reliability of low-k can be correlated with the elastic modulus of the film. However, we believe that the modulus is only of many compromised mechanical properties that stem from the films interrupted silicate interatomic network or nano-porosity. Silica-based porous films typically have low elastic modulus of 1 to 10 GPa and relatively high hardness of 0.5 to 1.5 GPa. With the high hardness to modulus ratios low fracture toughness can also be expected. In this study we outline other properties of silica-based low-k films that must be better understood for proper low-k dielectric film screening. CVD deposited low-K films of different thicknesses were deposited on Si wafers. Film mechanical properties were measured with nanoindentation. An indentation method utilizing a cube corner indenter was used to induce radial cracks in these low-K films. Based on the indentation load and radial crack length, measured optically, fracture toughness of thin films was calculated. Film fracture was also observed during nanoindentation adhesion testing. These tests were intended to measure interfacial fracture toughness, however interfacial cracks kinked into the film itself, indicating that adhesive and cohesive failure mechanisms will compete in the event of device failure. Given that the crack propagates through the low-K and based on resultant strain energy release rate calculations, film toughness on the order of 0.05 MPa*m$^{1/2}$ is estimated. This is corroborated by strain energy release rate calculations based on spontaneous film fracture due to residual film stress at a critical film thickness of 3 microns.

11:45 AM B12.14
LOW-k THIN FILMS DEPOSITED BY PECVD USING DECAHYDRONAPHTHALENE AND TETRAETHYL-ORTHOSILICATE AS THE PRECURSORS. Sanghak Yeo, Jaeyoung Yang, Cheonman Shim and Donggeun Jung, Department of Physics, Brain Korea 21 Physics Research Division and Institute of Basic Science, Sungkyunkwan University, Suwon, REPUBLIC OF KOREA.

Plasma enhanced chemical vapor deposition (PECVD) using a mixture of decahydronaphthalene (DHN) and tetraethylorthosilicate (TEOS) as the precursors was used to deposit low dielectric constant plasma polymer thin films. The films were referred to as plasma polymerized decahydronaphthalene:tetraethylorthosilicate (PPDHN:TEOS) films. Properties of PPDHN:TEOS thin films were dependent significantly upon the plasma power. The deposition power was varied from 30 to 90 W. As the plasma power increased, except for the film deposited at 70 W, the relative dielectric constant k decreased, thermal stability degraded, and leakage current decreased. The PPDHN:TEOS thin film deposited at 70W showed the minimum k value, the poorest thermal stability, and the minimum leakage current among the PPDHN:TEOS films deposited with the plasma power of 30, 50, 70, and 90 W. We investigated the chemical structure of PPDHN:TEOS by Fourier transform infrared (FT-IR) spectroscopy. FT-IR absorption analysis revealed that as the content of DHN-related species increases and the content of TEOS-related species decreases in the PPDHN:TEOS films, the k value decreases, and thermal stability degrades. The thin film deposited at 70 W showed leakage current of $\sim 5 \times 10^{-8}$ A/cm^2 at 1 MV/cm. In order to improve the k-value and thermal stability of the 70W-deposited PPDHN:TEOS films, we performed the post deposition in-situ heat treatment. After the heat treatment at 450°C, the relative dielectric constant of the film decreased from 3.1 to 2.7. The 450°C-heat treated PPDHN:TEOS film has higher thermal stability than the not-treated film. Removal of reactive species in the film and increase of cross-linking among film-forming species by heat treatment are thought to contribute to the decrease of k-value and improvement of the thermal stabilities, respectively.

SESSION B13: RELIABILITY
Chairs: Stefan P. Hau-Riege and Paul S. Ho
Friday Afternoon, April 5, 2002
Salon 10-12 (Marriott)

1:30 PM *B13.1
TECHNIQUES FOR LOCALIZATION OF IC INTERCONNECTION DEFECTS. Edward I. Cole Jr., Sandia National Laboratories, Albuquerque, NM.

The advances in integrated circuit technology has made failure site localization extremely challenging. Charge-Induced Voltage Alteration (CIVA), Low Energy CIVA (LECIVA), Light-Induced Voltage Alteration (LIVA), Seebeck Effect Imaging (SEI) and Thermally-Induced Voltage Alteration (TIVA) are five recently developed failure analysis techniques which meet the challenge by rapidly and non-destructively localizing interconnection defects on ICs. The techniques take advantage of voltage fluctuations in a constant current power supply as an electron or photon beam is scanned across an IC. CIVA and LECIVA are scanning electron microscopy (SEM) techniques that yield rapid localization of open interconnections. LIVA is a scanning optical microscopy (SOM) method that yields quick identification of damaged semiconductor junctions and determines transistor logic states. SEI and TIVA are SOM techniques that rapidly localize open interconnections and shorts respectively. LIVA, SEI, and TIVA can be performed from the backside of ICs by using the proper photon wavelength. Each technique will be described in terms of the physics for signal generation, sample preparation requirements, and advantages over existing analysis methods. Examples of each technique will be shown demonstrating its utility in locating defects.

2:00 PM B13.2
EBIC AND XTEM ANALYSIS OF HIGH VOLTAGE SMOS RELIABILITY FAILURES. Larry Rice, Motorola, Inc., Process and Materials Characterization Laboratory, Mesa, AZ.

Microscopists are faced with many challenges in locating and examining failure sites in the ever-shrinking semiconductor device. The site must be located using electrical characterization techniques like electron beam induced current (EBIC), photo emission microscopy (PEM) or liquid crystal (LC) then cross-sectioned with a focused ion beam (FIB). Both PEM and LC require the semiconductor circuit to be at near operating conditions which has been observed to locally melt the area of interest frequently destroying evidence of the failure mechanism. In contrast, EBIC typically can be accomplished at low or no applied voltage eliminating further damage to the circuit. EBIC has been applied to locate leakage sites in high voltage metal oxide semiconductor (MOS) electro static discharge (ESD) reliability failures. In addition to a brief revisit of the basic principles of EBIC and describing a technique to successfully cross section 'hot spots' for transmission electron microscopy (TEM) observation, focus will be placed on a case study of the reliability testing failure analysis of ESD power transistors using EBIC, scanning electron microscopy (SEM), FIB, and transmission electron microscopy (TEM).

2:15 PM B13.3
LENGTH EFFECTS ON THE RELIABILITY OF DUAL-DAMASCENE Cu INTERCONNECTS. F.L. Wei, Massachusetts Institute of Technology, Department of Materials Science and Engineering, Cambridge, MA; C.L. Gan, Singapore-MIT Alliance, Advanced Materials for Micro- and Nano- Systems Programme, SINGAPORE; C.V. Thompson, Massachusetts Institute of Technology, Department of Materials Science and Engineering, Cambridge, MA, and Singapore-MIT Alliance, Advanced Materials for Micro- and Nano- Systems Programme, SINGAPORE; J.J. Clement, Sandia National Laboratory, Albuquerque, NM; S.P. Hau-Riege, Intel Corp, Portland, OR, now with Lawrence Livermore National Laboratory, Livermore, CA; K.L. Pey, W.K. Choi, Singapore-MIT Alliance, Advanced Materials for Micro- and Nano- Systems Programme, and National University of Singapore, Department of Electrical & Computer Engineering, SINGAPORE; H.L. Tay, B. Yu, M.K. Radhakrishnan, Institute of Microelectronics, SINGAPORE.

We have carried out experiments on dual-damascene Cu interconnects with different lengths. We find that, like Al-based interconnects, the reliability of Cu-based interconnects improves at short lengths. Like Al, some short Cu lines do not form voids that cause failure before back-stresses cause void growth to stop. However, unlike Al-based interconnects, there does not appear to be a minimum current density-line length product (jL) for which all lines are immortal. It is thought that this is related to the absence of a conducting refractory overlayer in Cu-technology that can shunt current around small voids, as conducting anti-reflection coating layers do in Al-technology. Also unlike Al, we find that for Cu interconnects, both the median time to failure and the deviation in the time to failure increase for longer lines. A sub-population of long lines survive for very long times. It is thought that this is the result of rupture of the thin refractory metal liner at the base of the dual-damascene Cu vias. As a consequence of this complex behavior, there are intermediate line lengths with minimum median lifetimes *and* minimum lifetime variations in Cu metallization.

3:00 PM B13.4
EFFECT OF METALLIC CONTAMINATION ON INTERFACE PROPERTIES AND OXIDE RELIABILITY. Elena Oborina, Center for Microelectronics Research, University of South Florida, Tampa, FL; Scott Campbell, Department of Chemical Engineering, University of South Florida, Tampa, FL; Drew Hoff, Center for Microelectronics Research, University of South Florida, Tampa, FL; Richard Gilbert, Department of Chemical Engineering, University of South Florida, Tampa, FL; Eric Persson, Darrell Simpson, Agere Systems, Orlando, FL.

New and emerging process technologies are creating contamination control challenges for current and future generations of integrated circuits. Damascene interconnect, metal gate and metal silicide processes are representative of many potential sources of metallic contamination to wafer structures. In this work, we studied contamination of oxidized silicon wafers by several metals of industrial importance including copper, cobalt, sodium, iron and nickel. Contamination in the range of 20 to 500 ppb was introduced by spin-coating. These levels are representative of exposure in chemical processes such as CMP cleans. Contaminating ions were driven into the oxide layer by corona temperature stress (CTS). The presence of incorporated metallic species within the oxide was determined using VPD-ICPMS and SIMS. The effects of contamination on interface and oxide reliability were quantified by non-contact COCOS (Corona Oxide Characterization of Semiconductor) and SILC (Stress Induced Leakage Current) techniques. We discuss the relationships identified between surface analysis results and the non-contact measurements of oxide reliability and interface properties.

3:15 PM B13.5
MECHANICAL-STRESS-CONTROLLED SILICIDE INTER-CONNECTIONS FOR HIGHLY RELIABLE SEMICONDUCTOR DEVICES. Hiromi Shimazu, Hideo Miura, Hitachi, Ltd., Mechanical Engineering Research Laboratory, Ibaraki, JAPAN.

Silicidation is one effective way of reducing contact resistivity between a metal and silicon. Titanium silicide is one of popular material for interconnect applications. Titanium film is deposited on poly-Si plugs, which are embedded in a silicon dioxide layer, and annealed at about 800°C to form titanium-silicide between the poly-Si plug and the metal interconnect. The first reaction from Ti to TiSi starts at about 500°C, and the second reaction from TiSi to $TiSi_2$ starts at about 600°C. However, this silicidation causes higher tensile stress than 1 GPa in the reacted silicide film due to volume shrinkage during the silicidation; thus, it sometimes causes delamination between the reacted silicide and the remaining silicon. The stress developed near the interface between the poly-Si and the reacted silicide film was analyzed using a finite element method by considering the silicidation-induced stress. The developed stress near the interface strongly depends on both the thickness of the newly grown silicide and the diameter of the contact. It increases with increasing thickness of the silicide and decreasing the contact diameter. The developed stress reached the critical stress for delamination at the interface when the thickness of $TiSi_2$ was thicker than 75 nm and the diameter of the contact was smaller than 0.3 μm. it is, therefore, very important to minimize the thickness of the silicide in order to eliminate delamination at the interface. Increasing the annealing temperature for the silcidation higher than 800°C is another effective way for reducing the stress, because the developed stress relaxes due to viscoelastisity of the silicide film. We have made clear the stress developing process during titanium-silicide formation and an effective design rule for the highly reliable silicide interconnection.

3:30 PM B13.6
A ROBUST MULTI-LEVEL INTERCONNECT MODULE FOR ULSI CMOS INTEGRATION. Zhibo Zhang, Dept. of Electrical and Computer Engineering, NC State University, Raleigh, NC; J.-S. Huang, M. Twiford, E. Martin, N. Layadi, A. Salah, B. Bhowmik, D. Vitkavage, and S. Lytle, VLSI Technology Lab., Agere Systems, Orlando, FL; E.C.C. Yeh and K.-N. Tu, Dept. of MS&E, UCLA, Los Angeles, CA.

Aluminum-wire/tungsten-plug based multi-level interconnect technologies remain as the mainstream back-end-of-line technology for VLSI circuits in the semiconductor industry. The early interconnect failure in the W-plug via structure has been recognized as a generic phenomenon. In this work, we present detailed studies of two integration schemes for such a multi-level ULSI interconnect module for sub-quarter-micron CMOS technologies, and discuss the benefits and drawbacks of each of them primarily from a process integration point of view. We demonstrate that an etch stop integration scheme in which the via etch stops on the TiN cladding layer could result in significantly improved via electromigration performance compared to an over etch integration scheme in which the via is over etched into the underline Al(Cu). We also identified several highly detrimental early failure modes associated with the over etch structure, and showed that such early failure modes could be prevented in the etch stop integration scheme. All test structures were processed using manufacturing tool sets at a state-of-the-art eight-inch silicon Fab of Agere Systems. Detailed information regarding metalization compositions for metal wires and via liners, electromigration failure distributions, FMAs (failure mode analysis) of early interconnect failures, via contact resistances, metal sheet resistances, interconnect yields, and their correlations to the different integration schemes will be presented. Even though there are some small penalties in the device performance in the etch stop integration scheme, the benefits in the reliability and the better tolerance to manufacturing process variation clearly justify the adoption of this robust multi-level ULSI interconnect module for sub-quarter-micron CMOS technologies.

3:45 PM B13.7
INTERFACIAL ADHESION OF PATTERNED INTERCONNECT STRUCTURES. Christopher S. Litteken and Reinhold H. Dauskardt, Department of Materials Science and Engineering, Stanford University, Stanford, CA.

Recent studies of the adhesion of blanket thin-film interconnect structures have established that plastic energy dissipation in thin metal and polymer films, such as copper and low-k dielectrics, is related to the thickness of the relevant ductile layer. However, there is currently little understanding of how the geometry and size of

interconnect features utilized in technologically relevant structures will influence plasticity and hence the fracture resistance of such patterned structures. Accordingly, to investigate the role of feature size and shape, selected patterned structures containing arrays of polymer and metal lines with varying aspect ratios have been investigated. Macroscopic adhesion values were determined by measuring the critical strain energy release rate, G_c, for debonding of a selected interface. The significant contribution to G_c values from local plastic energy dissipation in the polymer and metal lines was examined and used to demonstrate the effect of patterned structure geometry on interfacial adhesion. Trends in adhesion and fracture behavior related to the patterned structures will be discussed in terms of the prevailing plastic deformation mechanisms and form the basis from which simple design rules for improved mechanical reliability may be developed.