SYMPOSIUM C

Si Front-End Junction Formation Technologies

April 2 – 4, 2002

Chairs

Mark E. Law
Dept of Electrical & Computer Engineering
Univ of Florida
535 NEB
Gainesville, FL 32611-6130
352-392-6459

Alain Claverie
CEMES-CNRS
Toulouse, F-31055 FRANCE
33-5-62257900

Daniel F. Downey
Varian Semiconductor Equipment Assoc
Gloucester, MA 01930-2297
978-282-2226

Michael J. Rendon
Advanced Products R&D Lab
Motorola Inc
MD-K10
Austin, TX 78721
512-933-5650

Symposium Support
Applied Materials, Inc.
Fujitsu, Ltd.
Intel Corporation
Verdant Technologies

Proceedings to be published in both book form and online
(see *ONLINE PUBLICATIONS* at www.mrs.org)
as Volume 717
of the Materials Research Society
Symposium Proceedings Series

* Invited paper

SESSION C1: ALTERNATE ANNEALING TECHNOLOGIES
Chairs: Daniel F. Downey and Michael J. Rendon
Tuesday Morning, April 2, 2002
Salon 14/15 (Marriott)

8:00 AM *C1.1
LOW TEMPERATURE SHALLOW JUNCTION FORMATION FOR 70NM TECHNOLOGY NODE AND BEYOND. John O. Borland, Varian Semiconductor Equipment Associates, Newburyport, MA.

Ion implantation shallow junction formation by high temperature (>1000C) RTA spike or flash annealing (sub-melt) techniques for oxide or oxynitride/polysilicon electrode gate stack structures can be extended down to 100nm technology node (2003) and is limited to <8E19/cm^2 boron electrically active dopant level due to boron solid solubility limit in silicon. If using higher temperature anneals such as laser melting (1200 to 1400C) this can be extended to 35nm technology node (2009) where boron solid solubility limit is increased up to 5E20/cm^2. However, if high-k dielectric/metal electrode gate stack structures are to be used starting at 70nm node and beyond (2005) for low power CMOS then low temperature (<750C) annealing must be used for shallow junction formation. Using low temperature SPE (solid phase epitaxial regrowth) annealing in the 550 to 650C for short times of 5 minutes we have realized 50nm technology node (2007) implanted shallow junctions 8.0 to 22.5nm deep with up to 2.5E20/cm^2 boron electrical active dopant level.

8:30 AM C1.2
MILLISECOND PULSE ANNEALING OF ULTRA-SHALLOW BORON PROFILES IN SILICON BY FLASH LAMP IRRADIATION. T. Gebel[a,b], M. Voelskow[a], W. Skorupa[a,b], G. Mannino[c], V. Privitera[c], F. Priolo[d], E. Napolitani[e], A. Carnera[e]; [a]Forschungszentrum Rossendorf, GERMANY; [b]Nanoparc GmbH, Dresden-Rossendorf, GERMANY; [c]CNR-IMETEM, Catania, ITALY; [d]INFM and University of Catania, Catania, ITALY; [e]INFM and University of Padova, Padova, ITALY.

Higher integration in semiconductor technology causes the need for ultra-shallow junctions. Because common RTP techniques are limited in their temperature ramping speed, alternative methods for ultra-short time annealing are of great interest. In this paper flash lamp annealing (FLA) is applied for that purpose. Si (100) wafers were implanted at ultra-low energies (500eV-1keV) with boron ions to fluences of 10^{14}-10^{15} cm^{-2}. Subsequently, FLA was carried out at temperatures in the range 1100-1200°C with a pulse time of 2-20ms using a bank of xenon flashlamps. Preheating of the samples from the rear side was performed at 250°C by halogen lamps. Using this combined heating technique, the final temperature is reached within some milliseconds. For comparison, conventional RTP was performed at 1100°C and 1200°C for the shortest reliable time of 1s and longer times up to 80 sec. The mechanical stress induced to the samples due to the heat shock was investigated with X-ray techniques. The boron diffusion and the dopant activation were investigated by SIMS and SRP. The activated doses after FLA were as high as 20% of the implanted dose confined in a layer of only 60nm.

8:45 AM C1.3
ELECTROMAGNETIC INDUCTION HEATING FOR THE 70 NM CMOS TECHNOLOGY NODE. Keith Thompson, John Booske, Yogesh Gianchandani, University of Wisconsin, Dept of Electrical Engineering, Madison, WI; Reid Cooper, University of Wisconsin, Dept of Materials Science and Engineering, Madison, WI.

The 70 nm CMOS technology node requires source/drain regions as shallow as 20 nm with sheet resistances of 500 ω/square. Optimal operation of these devices occurs when this profile is as box-shaped as possible, preferably with a surface concentration greater than 10^{20}/cm^3 and a profile slope greater than 5 nm/decade. [1] Obtaining these junctions requires sophisticated rapid thermal activation techniques that restrict the thermal budget, limiting the diffusion of the implanted species, while activating a significant percentage of the dopants. Current spike anneal technology (ramp rates of 425°C/sec in a low ppm oxygen ambient) while satisfying the 100 nm technology node [1] appears to have reached its limit. To achieve further reductions in junction depth, anneal techniques that can achieve higher levels of activation (compared to current techniques) at a given temperature must be investigated.
Dopant activation through electromagnetic induction heating, EMIH, offers an alternative that may satisfy the 70 nm technology node. Using radiation in the RF and microwave frequency regimes (1 MHz - 10 GHz), silicon wafers have been directly heated, without the use of a susceptor, to temperatures greater than 1000°C. This technique has satisfied the 100 nm technology node outside of a controlled ambient, and it is suspected that the presence of high frequency radiation has enhanced the activation rate [2].
New research results that include investigations of the effects of a controlled oxygen ambient and evaluation of methods that improve the temperature uniformity have allowed for the optimization of electromagnetic spike annealing. These optimizations along with spike anneal data will be discussed.

1. W. Lerch, B. Bayha, D.F. Downey, E.A. Arevalo. in Proc. of the Electrochemical Society (March 2001).
2. K. Thompson, J.H. Booske, Y. Gianchandani, R. Cooper, "RF and Microwave Annealing for Ultra Shallow Junction Formation" in Proc. of the Electrochemical Society (March 2001).

9:00 AM C1.4
STUDY OF THE EFFECTS OF A TWO-STEP ANNEAL ON THE END OF RANGE DEFECTS IN SILICON. Renata Camillo-Castillo, Kevin Jones, Univ of Florida, Dept of Materials Science and Engineering; Mark Law, Univ of Florida, Dept of Electrical and Computer Engineering, Gainesville, FL; Leonard M. Rubin, Axcelis Technologies, Beverly, MA.

Investigations have been conducted where a two step anneal is performed on Ultra Low Energy (ULE) implantations in order to determine the effect on the Transient Enhanced Diffusion (TED). The procedure consists of a low temperature anneal in the range of 500-600°C in which Solid Phase Epitaxial Regrowth (SPER) occurs, followed by a Rapid Thermal Anneal (RTA) at 1000°C. The experimental data indicates that there may be a significant reduction in the TED when the pre-annealing step is applied to an ULE implant thus resulting in remarkably reduced junction depths. This has been attributed to the reduction in the end of range (EOR) defects on application of the pre-anneal. There is no experimental data which explores the evolution of the EOR defects and this warrants further investigation. In order to prove or disprove it's validity a study is underway which examines whether this pre-anneal step has any measurable effect on the evolution of the end of range (EOR) defects for a range of implant energies (10-30keV). Two scenarios are the subject of our study. One in which a RTA is applied after implantation; the second scenario the pre-anneal is applied after the implantation followed by a RTA.

9:15 AM C1.5
532NM MULTI-PULSE NONMELT LASER ANNEALING AND POST-PROCESSING OF HEAVILY-DOPED, BORON IMPLANTED SILICON. Susan Earles, Jackie Frazer, Mark Law, Kevin Jones, SWAMP Center, University of Florida; Somit Talwar, Verdant Technologies, San Jose, CA.

The effects of multiple nonmelt laser pulses on silicon heavily doped with boron has been studied and ultra-shallow, heavily-doped layers created. High-dose, non-amorphizing boron implants of 1E15/cm^2 at 500eV and 2E15/cm^2 at 5000eV were used. The implants were annealed with between 1 and 1000 20ns long laser pulses. The laser operated at 532 nm with the pulse frequency at 10 Hz. The results were post-processed with and compared to conventional spike and furnace anneals. SIMS, Hall effect, and TEM were used for analyses. Results show that nonmelt laser annealing produces shallower junctions with lower resistivity and higher mobility than conventional annealing and offers junction characteristics suitable for the 2007 65nm ITRS technology node.

9:30 AM C1.6
MICROWAVE ANNEALING OF ULE B IMPLANTED Si. Robert Crosby, K.S. Jones, M. Puga-Lambers, J. Chen, Dept of Materials Science and Engineering, Gainesville, FL; D. Downey, VSEA, Gloucester, MA.

A reasonant 915 MHz microwave furnace in conjunction with spike annealing was studied as a method of annealing implantation damage and activating dopants for junction formation in ion implanted silicon. B implants with energies of 250 eV and 500 eV and doses of 3 x 10^{15} cm^{-2} and 1 x 10^{15} cm-2 respectively were pre-annealed at 650°C, 700°C, and 750°C in both a microwave furnace and a conventional furnace for comparison. Afterwards, spike anneals varying between 950°C and 1100°C were carried out in an RTA to activate the B. Hall effect measurements were used to compare the electrical properties of the microwave-assisted anneals against the conventional-assisted anneals. SIMS analysis was conducted to monitor the junction depths of both conditions as well. We relate the differences in sheet resistivity, hall concentration, and mobility of the two annealing procedures to the increased ionization arising from the electro-magnetic energy supplied by the microwave pre-anneals.

10:15 AM C1.7
ULTRA-SHALLOW, ABRUPT AND HEAVILY-DOPED p+/n JUNCTION FABRICATED BY LASER DOPING AND ANNEALING OF PREAMORPHIZIED Si ON n-TYPE Si(100). Jong Won Moon, Myung Geun Han, Seonghoon Lee, Kwangju Institute of Science and Technology, Department of Materials Science and Engineering, Kwangju, KOREA.

Ultra-shallow, heavily-doped and boxlike boron doping profiles were formed by laser doping and annealing of preamorphized Si on n-type Si(100) wafer. We have investigated the effect of the thickness of pre-amorphized layer on a shallow p+/n junction depth. In order to obtain the optimized conditions, we also studied the effects of experimental parameters such as laser energy density, doping gas pressure, and number of laser pulses. We irradiated a 248nm KrF excimer laser beam on samples under the following conditions: doping gas pressure (3% B2H6 + 97% N2) in the range of 10 torr to 400 torr, laser energy fluence in the range of 0.2 J/cm^2 to 1.0 J/cm^2, and number of laser pulses from 1 to 20 pulses. Atomic force microscope were used to investigate the surface roughness. The sheet resistance measured by von der Pauw's method using a hall measurement instrument was 100 $\Omega/\square$. Using a high-resolution cross sectional transmission electron microscope, we confirmed the thickness of the preamorphized Si layer and observed that the amorphous silicon was transformed into single crystalline silicon without any defects through a liquid phase epitaxial growth after laser doping and annealing. Boron depth profile was analyzed using secondary ion mass spectrometry. Through this experiment, we have fabricated ultra-shallow (x∼320Å), heavily doped (>1x{10^{21}} atoms/cm^3), and boxlike p+/n junction.

10:30 AM C1.8
SINGLE-SHOT ELA AND IN-PROCESS ANALYSIS FOR USJ. Takashi Noguchi, Gurwan Kerrien, Thierry Sarnet, Dominique Debarre, Jacques Boulmer, Institut d'Electronique Fondamentale, UMR CNRS 8622, Universite Paris-Sud, Orsay, FRANCE; Miguel Hernandez, Dorian Zahorski, Christophe Defranoux, Sopra, Bois-Colombes, FRANCE; Cyrille Laviron, M.-N. Semeria, CEA-DRT-LETI/DTS-CEA/GRE, Grenoble, FRANCE.

The sub-0.1μm transistor has been studied extensively, because it will play a leading role in ULSIs. ELA (Excimer Laser Annealing) is a candidate process as an advanced RTA (Rapid Thermal Annealing) for realizing the sub-0.1μm CMOS FETs with USJ (Ultra-Shallow-Junction) which suppresses the SCE (Short Channel Effect). In order to form an optimised shallow-junction efficiently, effective in-process analyses are required in place of conventional destructive or contact analysis such as SIMS (Secondary Ion Mass Spectroscopy) or 4-points probe method. Si wafers were implanted with B^+ or BF_2^+ at a dose of 2E15 /cm^2 (less than 5 keV). Subsequently, the surface was annealed using UV beam of excimer laser with a wavelength of 308 nm by changing the pulse energy density or the number of shots. During a pulse, the depth was measured by monitoring an in-situ transient reflectivity at 675 nm of laser diode. Abrupt p^+/n junction can be expected after ELA because of instantaneous melting the Si surface. The surface has been analysed using non-contact SE (Spectroscopic Ellipsometry) in IR (Infra-Red) and conventional 4-points probe. Similar trend has been obtained for the sheet resistance and for the depth from the different analysis. By increasing the pulse energy density, the resistivity decreased corresponding to the activation of the Si surface. Higher crystallinity was confirmed for the B+ Implanted surface by analysing with SE in UV region as well as by using Backscattering Kikuchi Diffraction in the scanning electron microscope. Sheet resistance lower than 200 ohm/sq. has been obtained with less than 10 shots. The lowest resitivity under optimised energy condition has been obtained for a junction shallower than 30 nm by single-shot ELA both for B^+ and for BF_2^+ implanted samples.

10:45 AM C1.9
EFFECTS OF LASER THERMAL PROCESSING ON POINT DEFECT POPULATIONS AND BEHAVIOR IN SILICON.
Erik Kuryliw, Kevin S. Jones, University of Florida, Department of Materials Science and Engineering, Gainesville, FL; David Sing, Motorola/International Sematech, Austin, TX; Somit Talwar, Verdant Technologies, San Jose, CA.

Laser Thermal Processing (LTP) involves laser melting of an implantation induced preamorphized layer to form highly doped ultra shallow junctions in silicon. In theory, a large number of interstitials remain in the end of range (EOR) just below the laser-formed junction. There is also the possibility of quenching in point defects during the rapid solidification of the melt region. Since post processing anneals are inevitable, it is necessary to understand both the behavior of these interstitials and the nature of point defects in the recrystallized-melt region. In this study, an amorphizing 15 keV 1 x 10^{15} /cm^2 Si^+ implant was done followed by a 1 keV 1 x 10^{14} or 3 x 10^{15}/cm^2 B^+ implant. Some samples received a pre-LTP furnace anneal at 450°C to smooth the amorphous-crystalline interface. The surface was then laser melted at laser powers between 0.38 and 0.68 J/cm^2 using a 532 nm excimer-laser. It was found that laser powers above 0.52 J/cm^2 melted past the amorphous-crystalline interface. Post-LTP furnace and rapid thermal anneals were performed at temperatures ranging from 700°C to 1000°C. Transmission electron microscopy was used to analyze the defect formation after LTP. Secondary ion mass spectrometry measured the initial and final boron profiles. It was found that EOR extend defect evolution was quite different compared to conventional material. Small dislocation loops were observed to form, reach peak density after 30 minutes at 750°C, and then mostly dissolve by 120 minutes. However, samples that received pre-anneals exhibited a much more stable loop population. Despite the reduction in extended defect formation, enhanced diffusion after post-LTP anneals was observed for all laser powers. These phenomena are investigated and discussed.

11:00 AM C1.10
THE PROCESS WINDOW OF BORON IMPLANTED SILICON FOR LASER THERMAL PROCESSING. Kevin A. Gable, Kevin S. Jones, Univ of Florida, Dept of MS&E, Gainesville, FL; Mark E. Law, Univ of Florida, Dept of Electrical & Computer Engr, Gainesville, FL; Lance S. Robertson, Texas Instruments, Dallas, TX; Somit Talwar, Verdant Technologies, San Jose, CA.

One alternative to conventional rapid thermal annealing (RTA) of implants for silicon (Si) ultra-shallow junction formation is that of laser annealing. Laser thermal processing (LTP) incorporates a solid-state pulsed laser capable of melting the near surface region of the substrate. The melt depth is dependent upon the energy fluence supplied by the laser and the melting temperature of the substrate surface. LTP is able to produce similar junction depths over a range of laser irradiation energies due to the melting temperature depression associated with pre-amorphization of the substrate surface. Additional differences in the melting temperature may be realized through the introduction of a high concentration of impurities. It is the focus of this research to investigate the process window of germanium (Ge) pre-amorphized, boron (B) doped Si. (100) n-type Si wafers were pre-amorphized via implantation with 12 keV - 36 keV Ge to $1 \times 10^{15}/cm^2$ - $1.6 \times 10^{16}/cm^2$ and subsequently implanted with 1 keV B to $1 \times 10^{15}/cm^2$ - $9 \times 10^{15}/cm^2$ resulting in B concentrations of $3.33 \times 10^{20}/cm^3$ - $3 \times 10^{21}/cm^3$. All wafers were laser annealed from 0.30 J/cm^2 to 0.68 J/cm^2 using a 532 nm wavelength Nd:YAG irradiation source. Plan-view and cross-sectional transmission electron microscopy (TEM) and secondary ion mass spectroscopy (SIMS) were used to determine the process window for each implant condition and correlations between process window shift and melting temperature dependence were made.

11:15 AM C1.11
LASER THERMAL PROCESSING OF ALTERNATE DOPANTS IN SILICON. Mark H. Clark, Kevin S. Jones, University of Florida, Department of Material Science and Engineering, Gainesville, FL.

Laser Thermal Processing (LTP) is a promising candidate for producing ultra-shallow, highly-activated junctions required for future semiconductor technology nodes. Specifically, a 30 nm junction with a sheet resistance as low as 70 ohms/sq. has been reported for LTP. The low sheet resistance achieved by LTP opens the door to dopants that have historically been excluded due to low activation. The goal of this study is to determine the viability of using LTP to activate unconventional dopants in silicon. Active carrier concentration for unconventional dopants of ^{14}N, ^{209}Sb (n-type) ^{27}Al, ^{70}Ga and ^{115}In (p-type) is compared to the more conventional dopants of ^{75}As and ^{11}B respectively, after LTP and post-LTP thermal processing. Dopants were implanted into $< 100 >$ silicon wafers of opposite background concentration that had been amorphized to a depth of approximately 300 angstroms by a 15 keV $^{28}Si^+$ implant with a $1x10^{15}/cm^2$ dose. An energy of 5 keV was sufficiently low to confine all implant species to the as formed amorphous layer except for B, which required an energy of 2 keV. Each species was implanted at nominal doses of $1x10^{14}$, $5x10^{14}$ and $1x10^{15}$ ions/cm^2. After LTP and post-LTP thermal processing the electrically active carrier concentration was measured by Hall Effect. Additionally, Secondary ion mass spectrometry (SIMS) was used measure the depth of the resulting dopant profiles. LTP increased the electrically active carrier concentration of several unconventional dopants well above solid solubility limits.

11:30 AM C1.12
THE INFLUENCE OF LOW TEMPERATURE PRE-ANNEALING ON THE DEFECT REMOVAL AND THE REDUCTION OF JUNCTION DEPTH IN EXCIMER LASER ANNEALING.
Sungkweon Baek, Taesung Jang, Hyunsang Hwang, Dept of Materials Science and Engineering, Kwangju Institute of Science and Technology, Puk-gu, Kwangju, KOREA.

The scaling of a MOSFET device channel length for high-speed device applications requires an ultra-shallow junction depth in order to suppress the short channel effect. By reducing the implantation energy and the thermal budget, an ultra-shallow junction can be formed. Plasma doping method is considered as a good candidate for achieving ultra-shallow junction profiles because its ultra-low energy, high throughput and room temperature operation. In addition,

through the excimer laser annealing, the abrupt, highly activated and ultra-shallow junctions can be obtained. It was known that the only laser annealing cannot remove all defects formed by implantation and pre-annealing is required for the complete removal of defects. In this paper, we fabricated high quality ultra-shallow p^+/n junction formed by plasma doping and excimer laser annealing and investigated the low temperature pre-annealing effect on the physical and electrical properties of the junctions. An ultra-shallow junction was formed by plasma ion implantation using B_2H_6(3%) gas diluted with H_2 gas. After plasma doping, KrF excimer laser annealing was performed. The excimer laser annealing was performed in the energy 500700mJ/cm^2 at pulse 1. The pre-annealing temperature was 300°C to 500°C for 5min in nitrogen ambient. The junction depth of as implanted sample was 10nm. Through the laser annealing at 500mJ/cm^2, the junction depth of 40nm was obtained. However, through the annealing at 300°C prior to laser annealing, 20nm junction depth was obtained. Based on XTEM analysis, we observed the complete removal of defects formed by plasma doping in the pre-annealed sample at 300°C followed excimer laser annealing. Up to date, it was not reported that the pre-annealing at this low temperature can affect the removal of defects and the reduction of junction depth. In addition, to investigate junction leakage current, we fabricated junction diode. The leakage currents of the excimer laser annealed diodes were low enough to comparable to those of rapid thermal annealed diodes. The pre-annealed diode following the excimer laser annealing shows low and uniform leakage current. In summary, by optimizing plasma doping, excimer laser annealing, and the pre-annealing temperature, the high quality p^+/n junction as shallow as 20nm can be obtained.

11:45 AM C1.13

THE STABILITY OF Sb AND P IN SILICON UPON POST LASER THERMAL PROCESS RAPID THERMAL ANNEALING. J.G. Erie, K.S. Jones, J. Chen, University of Florida, Dept of Materials Science, Gainesville, FL; S. Talwar, Verdant Technology, San Jose, CA; D. Sing, Motorola, International Sematech, Austin, TX.

Laser thermal processing (LTP) is considered one of the potential processes that could help the semiconductor industry meet the challenges in shallow junctions formation. One of the key advantages of LTP is that supersaturated electrically active dopant concentrations can be achieved during solidification of the molten surface. This paper investigates the activation of P and Sb achieved by exposing the samples to a 532 nm wavelength laser with energy varying from 0.30-0.68 J/cm^2. The effect of post LTP RTA at temperatures of 700, 800, 900, 1000°C was studied as a function of: preamorphization conditions and dopant concentrations. SIMS, TEM and Hall Effects were used respectively to measure junction depth, to view extended defects evolution and to measure electrical characteristics. Active Sb concentrations of 4 x 10^{20}/cm^3 were observed after LTP however further electrical characterization suggests the Sb and P are highly unstable upon post LTP annealing.

SESSION C2: DEVICE ENGINEERING OPTIONS

Chairs: Mark E. Law and John Ogawa Borland
Tuesday Afternoon, April 2, 2002
Salon 14/15 (Marriott)

1:30 PM *C2.1

OPTIMIZATION OF JUNCTIONS FORMED BY SOLID PHASE EPITAXIAL REGROWTH FOR 65NM CMOS. Richard Lindsay, IMEC, Leuven, BELGIUM; Bartek J. Pawlak, Peter Stolk, Philips Research Leuven, BELGIUM; Karen Maex, IMEC, Leuven, BELGIUM.

For the 65nm CMOS node, it is anticipated that conventional implantation and spike annealing approaches, even with pre-amorphisation and co-implantation, are unlikely to provide pMOS junctions consistent with the ITRS requirements. Here the junction performance is limited by equilibrium solid solubility. As laser annealing and in-situ doping techniques currently have unsolved integration problems, there is a renewed interest in using solid phase epitaxial regrowth (SPER) to form ultra-shallow metastable junctions. Such junctions have the potential to have an active dopant profile similar to the as-implanted profile. This offers above equilibrium solid solubility and abrupt profiles compatible with 65nm and even 45nm nodes. However there are concerns about residual defects, deactivation, dopant migration, lateral straggle and uniformity. In this paper we demonstrate the applicability of ultra-shallow junctions formed using SPER for sub-65nm CMOS nodes. We show how the Ge pre-amorphising implant, along with F co-implantation, can be optimised for B or BF2 junctions. There is latitude for higher doses and energies than conventional implants, however results show that this may lead to clustering causing enhanced deactivation. For the crystalline regrowth, increasing the annealing temperature from 550C, 40s to 900C, 1s increases the resistance from 330ohms/sq to 1610ohms/sq. The rate of deactivation is seen to be similar for temperatures between 550-700C. Increasing the time from 40s to 160s at 550C causes an 18% increase in resistance. TEM results show how a low temperature pre-anneal of 400C affects the roughness of the amorphous interface and hence the uniformity of the junctions. The effectiveness of post annealing between 650-1100C is described in reducing the number of residual defects for good junction leakage while avoiding dopant deactivation. With this approach, p-type junctions having a sheet resistance of 330ohms/sq and depth of 21nm are realised which are compatible with 65nm and potentially 45nm CMOS nodes.

2:00 PM *C2.2

S/D ENGINEERING FOR SUB-100 NM MOSFET USING ULTRASHALLOW JUNCTION FORMATION TECHNIQUE, ELEVATED S/D STRUCTURE AND SALICIDE TECHNIQUE. Kazuya Ohuchi, Kanna Adachi, Akira Hokazono and Yoshiaki Toyoshima, System LSI Research & Development Center, Toshiba Corporation Semiconductor Company, Kanagawa, JAPAN.

Suppression of short channel effect (SCE) by utilizing the technology of formation of ultrashallow junctions is one of the important issues. The annealing process of implantation-damage that induces transient enhanced diffusion during a subsequent thermal process such as low-pressure chemical vapor deposition (LPCVD) should be optimized. Moreover, high sheet resistivity due to dose loss degrades drive current of pMOSFET, especially. Key technology to solve this problem is optimization of the process of resist removal, formation of screen oxide and gate sidewall. To pursuit high performance of MOSFETs, parasitic resistance must be reduced with scaling. On the other hand, it is difficult to decrease the parasitic resistance in the region of contact junction, which is a function of physical constant such as Schottky barrier height of silicide materials and solid solubility of dopant. The elevated source/drain structure reduces parasitic resistance of contact junction due to reduction of resistance of diffusion beneath salicide materials. Cobalt salicide is widely used till 100nm node. However, cobalt salicide has disadvantage in the thermal budget for shallow junction and quantity of silicon consumption during silicidation. Nickel salicide is one of the candidates for successor of cobalt salicide to 70 nm node or above, because of its characteristics of low formation temperature, small amount of silicon consumption and low contact resistivity on p+ junctions. In this paper, S/D engineering will be discussed from the viewpoint of the process integration of sub-100 nm physical gate length complementary metal-oxide-semiconductor field-effect transistor (CMOSFET) device.

2:30 PM C2.3

TAILORING OF DOPANT PROFILES IN ADVANCED NMOS TRANSISTORS. A. Lebedev, M. Posselt, Forschungszentrum Rossendorf, Institute of Ion Beam Physics and Materials Research, Dresden, GERMANY; T. Feudel, AMD Saxony Manufacturing GmbH, Dresden, GERMANY; N. Variam, Varian Semiconductor Equipment Associates, MA.

The properties of advanced CMOS transistors are strongly influenced by the dopant distribution in the transition region between the source (drain) and the channel. The tailoring of this distribution is achieved by appropriate halo and extension implants and subsequent annealing. Process and device simulations are performed to investigate the influence of the corresponding process parameters. The boundary condition used throughout the simulations is to keep the threshold voltage V_{Tsat} for the nominal nMOS transistor (sub-70 nm gate length) at 0.2 V. The following process conditions are studied: (i) B^+ halo implant: energy below 10 keV, tilt 45°, rotation 4×90°, dose varied to achieve V_{Tsat}= 0.2 V (ii) As^+extension implant: 0.5, 1.0, 2.0 keV, tilt 0°, 10^{15} cm^{-2} (iii) RTA after both implants with special emphasis on soak and spike anneals (950...1100°C) The model parameters employed in the simulation of the formation of the ultra-shallow extension profiles are calibrated using SIMS profiles of as-implanted and annealed samples, and sheet resistance data. The V_{Tsat} vs. L_{Tsat} curve of the nMOS transistor is calculated. The dependence of the roll-off and roll-on behaviour on the process conditions considered is discussed.

3:15 PM C2.4

CHARACTERIZATION AND MONITORING OF SILICON-ON-INSULATOR FABRICATION PROCESSES BY HIGH-RESOLUTION X-RAY DIFFRACTION. G.M. Cohen, P.M. Mooney, H. Park, C. Cabral Jr., and E.C. Jones, IBM T.J. Watson Research Center, Yorktown Heights, NY.

High-resolution x-ray diffraction (HRXRD) was used to monitor silicon-on-insulator (SOI) processing steps. The use of HRXRD is attractive since it is non-destructive and can be applied directly to product wafers. We show the usefulness of this technique for the characterization of amorphizing implants for shallow junctions, solid phase re-crystallization of implanted junctions, cobalt-silicide

formation and oxidation - all critical processes for CMOS fabrication on SOI. The idea behind the use of HRXRD to monitor SOI processing is straight forward. Oxidation, silicide formation and amorphizing implants reduce the single crystal SOI film thickness, which is easily and accurately measured by HRXRD. For example, oxidation would convert the top part of the SOI film into SiO_2. Similarly, silicidation reacts a metal (such as Co) with the top portion of a SOI film to form a silicide (such as CoSi and $CoSi_2$). The phase of the silicide that is formed can be determined from the amount of Si consumed. In the case of an amorphizing implant a portion of the SOI film is converted from single crystal silicon to amorphous silicon. Post-implant annealing (typically carried out by RTA) re-crystallizes the amorphous portion of the film and restores the SOI film thickness. Accurate measurement of the SOI film thickness is essential for tight monitoring of these processes. We used HRXRD to characterize amorphizing and non-amorphizing Ge implants, and Si and boron implants. The implanted wafers were annealed by RTA, and HRXRD was used to record the changes in the SOI film. The HRXRD data showed the re-crystallization of the amoprhized portion of the SOI, while in the case of the boron implanted wafers a change in the sign of the strain was recorded when the boron assumes a substitutional site. By comparing the rocking curve data to a calculated curve, the strain profile and implant damage profile in the SOI film was extracted. The obtained HRXRD results were found to be in good agreement with TEM data. We also investigated double-bonded SOI substrates having two stacks of buried oxides and SOI films. Diffraction maps were recorded. Analysis of the map provides the thickness, tilt, and rotation of each SOI layer with respect to the handle substrate. This demonstrates the potential of the technique for future 3D integration and processing.

3:30 PM C2.5
SILICON SELF-INTERSTITIAL CLUSTER FORMATION AND DISSOLUTION IN SOI. Antonio Saavedra, Dena Wrigley, Jackie Frazer, Kevin Jones, Department of Materials Science and Engineering, University of Florida, Gainesville, FL; Erin Jones, IBM Research Division, T.J. Watson Research Center, Yorktown Heights, NY.

Silicon-on-insulator (SOI) is a promising alternative to bulk silicon as ultra shallow junction depths shrink below 10 nm. This study examined the effect of the SOI surface silicon/buried oxide interface on {311} defect evolution after Si^+ ion implantation. SOI wafers were produced such that the SOI surface silicon thickness varied from 300Å to 1600Å. Non-amorphizing Si^+ implants ranging from 5 keV to 40 keV with a fixed dose of $2\times^{14}$ were done into the wafers. Furnace anneals were performed at 750°C from 5 minutes to 4 hours and quantitative transmission electron microscopy (QTEM) was used to study the implant damage evolution. It was observed that as the surface silicon layer was thinned down a small decrease in the initial concentration of trapped interstitials occurred. The dissolution rate of extended defects also slightly increased as the surface silicon layer was thinned. However, recombination at the Si/buried oxide interface did not appear to be significant unless the implant profile overlapped or was within 100Å to 200Å of the Si/buried oxide interface.

3:45 PM C2.6
ULTRA SHALLOW DOPANT PROFILES IN THIN SOI AND BULK. Omer Dokumaci, Paul Ronsheim, Atul Ajmera, Joyce Mayo, Ralph Young, Carol Heenan, Daniel Uriarte, K. Paul Muller, IBM SRDC, Hopewell Junction, NY; Robert J. Miller, IBM Research, Yorktown Heights, NY.

SOI (silicon-on-insulator) technology has garnered a lot of interest lately because of the device performance improvements over bulk technology. Particularly for thin SOI layers it is worthwhile to study the dopant profiles in order to see if the presence of a buried oxide causes any change in the diffusion mechanism. In this study, arsenic, boron and BF2 diffusion were investigated in both 500A SIMOX and bulk wafers. After preamorphization with Ge, arsenic was implanted at 1.5 keV, boron at 0.75 keV and BF2 at 3.4 keV, all with a dose of 1e15 cm^{-2}. The samples were annealed in an RTA system between 1s to 15s at 1000C. Arsenic and boron profiles were obtained with SIMS. There were no significant differences in arsenic profiles between the bulk and SOI wafers. The presence of the SOI/SIMOX interface did not have a significant effect on the annealing of point defects created by implantation nor did it have a significant effect on inert diffusion of high concentration arsenic. In the boron implanted wafers, there was not a significant difference in the boron profiles between SOI and bulk after the 1s anneal except close to the SOI/SIMOX interface. Boron segregation was observed around the SOI/SIMOX interface. After the 15s anneal, boron was virtually flat in the SOI sample. Boron profiles in the BF2 samples were also virtually the same in the SOI and bulk wafers except close to the SOI/SIMOX interface. All the results point out that the SOI/SIMOX interface does not have any significant effect on diffusion with respect to the front interface for ultra-shallow implants. However, segregation into the SIMOX interface can be important when the dopant profile gets close to the SIMOX interface. Simulation results of the effect of the front and SIMOX interfaces on diffusion and segregation will also be discussed.

SESSION C3: DOPING ACTIVATION

Chairs: Alain Claverie and Kazuya Ohuchi
Wednesday Morning, April 3, 2002
Salon 14/15 (Marriott)

8:00 AM *C3.1
CURRENT UNDERSTANDING AND MODELING OF BORON-INTERSTITIAL CLUSTERS. Peter Pichler, Fraunhofer- Institut für Integrierte Schaltungen, Bauelementetechnologie, Erlangen, GERMANY.

Scaling of devices as predicted by the International Technology Roadmap for Semiconductors (ITRS) requires structures with ever increasing charge carrier concentrations. Current attempts for boron as the acceptor element with the highest solubility aim at taking advantage of non–equilibrium situations in which the electrically active concentration exceeds even the solid solubility of the dopant. A major obstacle to such high electrical activities are clusters involving boron and self–interstitials, the so–called boron–interstitial clusters for which the abbreviation BICs became customary. First reports of such clusters came from electron irradiation studies where their structure was inferred mainly from infrared spectroscopy, but also from ion beam analyses and photoluminescence studies. BICs attracted the interest of the semiconductor community especially after it became clear about 15 years ago that they may reduce electrical activation and retard diffusion during post–implantation annealings even at concentrations significantly below solid solubility. Complementary investigations showed that the clusters do involve boron and self–interstitials. Since BICs were never observed by TEM it can be concluded that they are either very small or that they do not strain the matrix. Further information like binding energies or ionization levels came from theoretical investigations, especially those based on *ab–initio* methods. However, because of their still limited accuracy for excited states, "minor modifications" of the predicted values were suggested in a variety of reports. In the presentation the contemporary knowledge of the properties of BICs will be discussed and their impact on semiconductor processes will be highlighted.

8:30 AM *C3.2
DIRECT OBSERVATION OF SINGLE DOPANT ATOMS AND DEACTIVATING DEFECTS: PROBING THE LIMITS ON FREE-CARRIER DENSITIES IN 2D- AND 3D-DOPED Si. P.H. Citrin, D.A. Muller, P.M. Voyles, J.L. Grazul, H.-J. L. Gossmann[a], and P.A. Northrup, Bell Labs, Lucent Technologies, Murray Hill, NJ; [a]Agere Systems, Murray Hill, NJ.

For Si device structures to continue shrinking, we must understand the inherent limitations on the highest possible free-carrier densities. Doping Si with high concentrations of Sb is known to lead to a saturation of free carriers, the values of which depend strongly on whether the Sb atoms are distributed in 3D (bulk-doped) or 2D (δ-layer doped). We report the direct, atomic-scale observation of individual dopant atoms in Si using annular dark-field scanning transmission electron microscopy. With an Sb detection efficiency of almost 100%, the structure, size, and distribution of electrically deactivating defects responsible for the saturation of free carriers in 3D-doped Si have been determined. This is the first time individual atoms still bonded inside their crystalline host environment have been unambiguously resolved. Simple counting of Sb clusters shows that the deactivating defects cannot comprise three or more atoms, which means that Sb_3V or Sb_4V defects cannot be the primary source of deactivation in these samples. Instead, the images show that pairs of dopants are the dominant deactivating species. There are two competing models for creating Sb-pair defects: One involves the interaction of two nearby Sb donor atoms to form a particular set of structures called donor-pair defects, while the other involves two Sb atoms surrounding a vacancy to form Sb_2V defects. Both result in creating pairs of 3-fold coordinated, electrically neutral Sb dopants (the models also apply to P and As), but they differ in how the fundamental limits to free carrier concentrations are reached. The observed increased electrical activity in 2D, for example, has been explained by the frustrated formation of donor-pair defects. New 2D-doped samples demonstrate that the maximum effective dopant concentration of Sb is as high as $\sim 5\times 10^{21}$ cm^{-3} with an electrical activity of ~65%. Antimony diffusion, deactivation, and precipitation upon thermal annealing of these 2D-doped samples are directly observed using x-ray absorption and scanning transmission electron microscopy.

9:00 AM C3.3
DEPENDENCE OF B CLUSTER DISSOLUTION ON THE TYPE

OF ANNEALING AMBIENT. Lj. Radic, A.D. Lilak, M.E. Law, Swamp Center, Department of Electrical and Computer Engineering, University of Florida, Gainesville, FL.

Ion implantation is preferred method of introducing dopants into silicon substrate. Boron is the species of choice for making p-type doped substrates. Creation of highly doped shallow junctions poses problems of clustering and deactivation of implanted B. Activation of B is studied for implant energies of 5, 10, 20 keV, and doses of 1e14, 2e14, 4e14 cm^{-2}, respectfully. Annealing is performed in two steps: 30 min inert anneal at 750°C, followed by 10, 20, 30, 60 min oxidizing and inert anneal at 850°C. Boron interstitial clusters form during first anneal step and deactivate significant part of the dose. Second anneal is used to determine the influence of annealing ambient on cluster formation or dissolution. Clustering effects are investigated via secondary ion mass spectroscopy and Hall-van der Pauw measurements. Hall effect measurement show oxidizing ambient has adverse effects on activation. Samples annealed in an inert ambient have consistently higher activation over implant conditions and anneal times studied.

9:15 AM C3.4
ELECTRICAL ACTIVITY OF B AND AS SEGREGATED AT THE $Si\text{-}SiO_2$ INTERFACE. J. Frühauf, Infineon Technologies, Munich, GERMANY (affiliated to IMEC); R. Lindsay, W. Vandervorst, K. Maex, IMEC vzw, Leuven, BELGIUM; A. Bergmaier, G. Dollinger, F. Koch, Technische Universität München, Physik-Department, Garching, GERMANY.

During spike annealing of ultra-shallow junctions, large fractions of the dopants segregate to the interface between silicon and the screening oxide layer, creating a pile-up of partially active dopants. To avoid an increase in sheet resistance to meet the requirements of the ITRS roadmap, it is important to understand the behaviour of dopants at the interface and to optimise their activation. In this paper, we show results of sheet resistance, SIMS (Secondary Ion Mass Spectrometry) and high resolution ERD (Elastic Recoil Detection with a depth resolution <1nm) measurements to investigate the behaviour of B and As dopant atoms at the interface. The sub-40nm junctions were implanted through a 2nm thermal oxide or oxynitride and annealed in various spike and soak anneals with different oxygen ambients. Our results show that the fraction of dopants segregated to the interface is as high as 20-25% for both B and As, but is dose and anneal dependent. Concentrations of up to 7e20cm^{-3} of mainly active dopants are found on the Si side of the interface. The presence of nitrogen in the oxide at the interface causes a higher and sharper pile-up. Results indicate that an even sharper pile-up is expected for As. Further experiments show that immediately after removing the screening oxide in an HF dip the sheet resistance for B decreases sharply due to carrier accumulation, then raises quickly to about 6-9% above the initial level depending on the oxide and implant dose. This is shown to be due to subsequent native oxide growth consuming the dopants in the highly doped surface peak. The sharp decrease in resistance is not observed for As. For B, BF_2 and As ultra-shallow junctions, care should be taken to avoid the removal of oxide after junction anneal, as the subsequent native oxide growth consumes a highly active interfacial dopant peak.

10:00 AM C3.5
DOPANT DEACTIVATION IN HEAVILY Sb DOPED Si(001): A HIGH RESOLUTION X-RAY DIFFRATION STUDY. Yayoi Takamura, Arturas Vailionis[a], Peter B. Griffin, James D. Plummer, Center for Integrated Systems, [a]Laboratory for Advanced Materials, Stanford University, Stanford, CA.

Laser annealing is being studied as an alternative annealing technique used in the formation of ultrashallow, low resistivity junctions required in future generations of integrated circuits. This method benefits from the ability to create uniform, box shaped dopant profiles with concentrations that can exceed equilibrium solubility values. These super-saturated dopant concentrations, however, exist in a metastable state and deactivate upon subsequent thermal processing. During the deactivation of Sb, it is believed that the substitutional dopant concentration decreases as the inactive dopant forms precipitates. As deactivation occurs, HR-XRD is used to monitor the lattice strain caused by the substitutional dopant atoms. This XRD data in conjunction with electrical measurements and SIMS profiles show that for Sb doped Si(001) layers, the precipitate model is only valid at moderate concentrations where $C_{Sb} < 6\times 10^{20}$ cm^{-3}). At extremely high concentrations, the Sb layers become unstable against deactivation. We propose that under these conditions, inactive Sb exists in a new type of bonding configuration within the Si matrix.

10:15 AM C3.6
THE LOCAL STRUCTURE OF ANTIMONY IN HIGH DOSE ANTIMONY IMPLANTS IN SILICON BY XAFS AND SIMS. M.A. Sahiner, S.W. Novak, Evans East; J.C. Woicik, NIST; Y. Takamura, P.B. Griffin, J.D. Plummer, Stanford University.

One of the important challenges in semiconductor industry is to sustain high concentration of dopant atoms electrically active in very small areas. In investigating the optimum post implantation treatment methods that will help to attain these conditions, the local structural information around the dopant atom is crucial. In this study, we have used secondary ion mass spectroscopy (SIMS) and x-ray absorption fine structure spectroscopy (XAFS) to obtain the concentration depth profiles and the local structural information around the Sb atom in Sb implanted Si wafers. Pre-amorphized Si wafers were implanted with Sb between doses $1.6\times 10^{15}cm^2$ and $2.0\times 10^{16}/cm^2$. The wafers were laser thermal annealed (LTA) after the implantation. Using experimental and calculated XAFS standards for Sb-foil and substitutional form Sb in Si, the local structural changes in the Sb complexes were probed for different implant doses and LTA conditions. The results on these structural variations will be discussed and quantitative information such as the ratio of the precipitated versus susbtitutional Sb will be presented.

10:30 AM C3.7
MODELING OF DIFFUSION AND ACTIVATION OF LOW ENERGY ARSENIC IMPLANTS IN SILICON. S. Chakravarthi, Chidambaram PR, C. Machala, Amitabh Jain, Xin Zhang, Silicon Technology Development, Texas Instruments, Dallas, TX.

The achievement of ultra-shallow n-type source/drain extensions require low energy high dose implantation of arsenic into silicon. Subsequent to implantation, solid phase epitaxy (SPE) can lead to highly meta-stable arsenic concentrations. The presence of meta-stable concentrations of arsenic has been found to result in a rapid release of interstitials coupled with arsenic deactivation (e.g. annealing of laser annealed arsenic samples). Atomistic calculations have indicated the presence of various As-V complexes. Previous work by different groups has focussed on explaining these data, based on a range of discrete arsenic vacancy clusters. However, incorporation of a large number of clusters is numerically complex and reduces the effectiveness of TCAD simulators. In this work, we attempt to model the anomalous diffusion observed during annealing of low energy arsenic. We have used the understanding from atomistic calculations as the basis to develop a simple model for arsenic vacancy clustering. Our model uses a single arsenic vacancy cluster that forms by the release of silicon self interstitials. We find, this can account for the activation/deactivation and diffusion of low energy arsenic during processing. This model is calibrated over a range of energies (500eV–5keV As), dose (6×10^{14}–2×10^{15} cm^{-2}) and annealing temperatures. We also find good match to electrical data (e.g. sheet resistance) and incorporated in our full-flow process simulations.

10:45 AM C3.8
KINETIC LATTICE MONTE CARLO SIMULATIONS OF ARSENIC DIFFUSION IN SILICON. Zudian Qin, Scott T. Dunham, University of Washington, Dept of Electrical Engineering, Seattle, WA.

We simulate point defect-mediated arsenic diffusion in silicon using the Kinetic Lattice Monte Carlo (KLMC) method, based on defect-arsenic interaction from first principle calculations. With an acceleration algorithm implemented, we are able to significantly reduce computing time to achieve statistically sound results. Considering As/V interactions up to third nearest neighbor (3NN), we have found that vacancy-mediated arsenic diffusivity is linear with arsenic concentration at low dopant concentration and increases dramatically as dopant concentration exceeds 2×10^{20} cm^{-3}. These features agree qualitatively with experimental observations, but underestimate the abrupt increase of diffusivity at high dopant concentration. We performed additional simulations with As/V interactions extended up to 6NN. We found the longer-range interaction has little effect on arsenic diffusivity at low dopant concentration, since AsV pair diffusion prevails in this case and is limited by separation to 3NN distance. As dopant concentration rises, however, the longer-range interaction gives a much larger diffusivity increase at high doping level due to interaction of vacancies with multiple As atoms, consistent with experiment data. We also extended our KLMC simulations to include ejection of silicon atoms from As_nSi configurations, resulting in As_nV cluster formation. As_nSi forms via random interstitial-mediated As diffusion and thus the kick-out process accelerates further deactivation. These simulations allow us to model transient diffusion and activation of arsenic at the atomic scale.

11:00 AM C3.9
STRESS DEPENDENCE OF THE SOLID SOULUBILITY OF SOPANTS IN Si, Ge, AND SiGe ALLOYS. Babak Sadigh, Lawrence Livermore National Laboratory, Livermore, CA; Thomas Lenosky, Finisar Corporation, Livermore, CA; Scott Centoni, Stanford University, Redwood City, CA; Andrew A. Quong and Tomas Diaz de la Rubia, Lawrence Livermore National Laboratory, Livermore, CA.

One of the important challenges to the semiconductor industry today is to enhance the solid solubility of several dopants, in particular boron, in silicon. We have developed a formalism to calculate the equilibrium thermodynamic solubility of charged impurities in Si, Ge and SiGe alloys from first-principles. We apply our scheme to the case of boron in silicon-based substrates and study the effect of bi-axial stress on its solubility limit. We investigate the role of the dopant charge in its solubility, and study is coupling to stress.

11:15 AM C3.10
FIRST-PRINCIPLES SOLUBILITY ENHANCEMENT OF IMPURITIES NEAR THE FREE (100) SURFACE OF SILICON. Scott Centoni, Stanford University, Dept of Materials Science and Engineering, Stanford, CA; Babak Sadigh, Maria-Jose Caturla, Andrew Quong, Tomas Diaz de la Rubia, Lawrence Livermore National Laboratory, Livermore, CA.

One of the most pressing requirements for semiconductor fabrication to keep to Moore's Law is getting high concentrations of active dopants in thin layers near the wafer surface. Tersoff's empirical potential calculations suggest a greatly enhanced solubility of carbon in the first few layers beneath the (100) surface of silicon due to strain effects. We have performed first-principles calculations to study the relative formation energy, and thus the solubility enhancement, of several impurities near the Si (100) free surface. These methods correctly account not just for strain energies, but also for Coulombic and electronic structure effects. Impurities include carbon and germanium, which can clarify the role of strain, as well as charged dopants such as boron. Our results are of relevance in analyzing the epitaxial growth of heavily doped silicon.

11:30 AM C3.11
DOPANT SEREGATION AND CHARGE CARRIERS AT SILICIDE/SILICON INTERFACE CHARACTERIZED BY Z-CONTRAST IMAGING AND LOW LOSS EELS. Teya Topuria, Nigel D. Browning, Univ of Illinois at Chicago, Dept of Physics, Chicago, IL; Zhiyong Ma, Kevin Johnson, Intel Corporation, Hillsboro, OR.

Formation of ultra shallow junction and precise control of dopant distribution are very critical steps for todays transistor fabrication. Front-end processing modules can potentially disturb the desired junction profile and cause dopant redistribution. Self-aligned silicidation process is one of such examples where dopant is being pushed out due to limited solid solubility of dopant in silicide, resulting in significant dopant segregation. Precise characterization of dopant redistribution behavior and its electronic impact on device performance are critically needed for process improvement and control. In this work we used a comprehensive approach involving Z-contrast imaging, electron energy loss spectroscopy (EELS) and energy dispersive X-ray spectroscopy (EDS) to study dopant segregation and charge carriers at the silicide/silicon interface. Both Co silicide/Si and Ti silicide/Si interfaces were investigated for As-doped MOS transistors. Similarly prepared but undoped silicide/Si interfaces were also characterized for comparison. Our results clearly show electrically active arsenic segregating within a few monolayers beneath the Co silicide/Si interface. A detailed low loss EELS study of the doped and undoped devices revealed that arsenic remains electrically active and supplies additional charge carriers at the interface. These results are consistent with the electrical measurement showing a decrease in contact resistance for the transistors. Similar results were also obtained for Ti silicide source/drain region.

11:45 AM C3.12
ION IMPLANTATION CHARACTERIZATION OF SILICON WAFERS BY A MODIFICATION OF THE INFRARED PHOTOTHERMAL RADIOMETRY. Felipe Rabago, Instituto de Fisica, Universidad Autonoma de San Luis Potosi, San Luis Potosi, MEXICO; Andreas Mandelis, Photothermal and Optoelectronic Diagnostics Laboratories, Mechanical and Industrial Engineering, University of Toronto, Toronto, CANADA; Alex Salnik, Therma Wave Inc., Fremont, CA.

In the present contribution a study of ion implanted silicon wafers is presented. B, P and As were the ion implanted atoms in a very close doses differences. With a modification of the Infrared Photothermal Radiomery called Common-Mode-Rejection-Demodulation (CMRD) it was possible to get a resolution. The conventional frequency scan was unable to resolve these small ranges. The CMRD technique offer a better control of the ion implantation process. Results of both, conventional frequency scan and CMRD techniques, for B, P and As silicon wafers are presented here.

SESSION C4: EPITAXIAL TECHNIQUES, FLUORINE, DEFECT FUNDAMENTALS
Chairs: Peter Pichler and Masashi Uematsu
Wednesday Afternoon, April 3, 2002
Salon 14/15 (Marriott)

1:30 PM *C4.1
SELECTIVE SILICON-GERMANIUM SOURCE/DRAIN TECHNOLOGY FOR NANOSCALE CMOS. Mehmet C. Ozturk, N. Pesovic, J. Liu, I. Kang, H. Mo and S. Gannavaram, North Carolina State University, Department of Electrical and Computer Engineering, Raleigh, NC.

Future CMOS technology nodes bring new challenges to formation of source/drain junctions and their contacts. To avoid MOSFET performance degradation with scaling, series resistance contribution of each junction must be limited to five percent of the device channel resistance. This requires ultra-shallow junctions with extremely low sheet, spreading and contact resistance values. In this paper, we present an overview of the SiGe junction technology recently proposed by this laboratory for future technology nodes down to 30 nm. The technology is based upon selective deposition of boron or phosphorus doped SiGe in source/drain regions isotropically etched to the desired junction depth. Since the dopant atoms naturally occupy the substitutional sites during growth, the need for an activation anneal is completely eliminated limiting the maximum process temperature to 750°C for phosphorus doping. For boron doping, the process temperature is less than 550°C. In this temperature range, dopant diffusion is virtually eliminated resulting in extremely abrupt doping profiles Furthermore; the process is compatible with the thermal stability needs of future high-K gate dielectrics. Our results indicate that the technology can be used to form boron or phosphorus doped junctions that meet the junction depth - sheet resistance requirements of technology nodes down to 30 nm. Another key advantage of the technology is its ability to provide a lower bandgap material under the metal contact, which effectively reduces the metal-semiconductor barrier height. Very low resistivity SiGe films and smaller barrier height at the contact enable the technology to achieve contact resistivities down to 10^{-8} ohm-cm^2. We have shown that both Pt and Ni germanosilicides are able to provide contact resistivity values in this range. In summary, our results indicate that the technology is a highly promising candidate for source/drain junctions of future technology nodes.

2:00 PM C4.2
ARSENIC INCORPORATION IN Si AND SiGe MOLECULAR BEAM EPITAXY. Xian Liu, Qiang Tang, James S. Harris, Stanford Univ, Solid State and Photonics Lab, Stanford, CA; Ted I. Kamins, Hewlett-Packard Laboratories, Palo Alto, CA; Gary R. Mount, Charles Evans and Associates, Surface Science Laboratories, Sunnyvale, CA.

As MOSFETs scale to the deep-submicron scale, there has been an increasing demand for silicon-based epitaxy with sharp, high resolution doping profiles. From this nanoscale-device point of view, arsenic, with its small diffusivity and high solid solubility, makes a better N-type dopant than conventionally used phosphorous. Yet in Si and SiGe epitaxy using gas sources, arsenic tends to segregate to the surface, making high-level incorporation with abrupt profiles difficult. There are two mechanisms contributing to this phenomenon: memory effects associated with hydride decomposition, and atomic segregation of arsenic which reduces surface free energy. In this paper we report the results of arsenic incorporation in Si and SiGe alloys deposited by molecular beam epitaxy with a unique combination of disilane gas, elemental Ge, and a valved arsenic cracker which could supply both As_2 and As_4 vapors with low fluxes suitable for doping. The use of elemental arsenic eliminates the hydride decomposition step, therefore enhances incorporation and provides a means to study the true atomic segregation mechanism. Arsenic profiles were characterized with SIMS, SSR (spreading sheet resistance), and germanium profiles with SIMS, RBS and XRD. Epitaxial quality is evaluated by Hall measurements and cross-section TEM. It is shown that the degree of segregation is temperature dependent and suppressed in SiGe alloys compared with that in Si, resulting in much improved incorporation. Experimental data will be presented which systematically examines the effects of Ge concentration, growth rate and growth temperature on arsenic segregation and incorporation. These effects are attributed to changes in segregation energy and surface hydrogen coverage.

2:15 PM C4.3
SUBSTITUTIONAL CARBON INCORPORATION FAR ABOVE SOLID-SOLUBILITY IN SiC AND SiGeC BY CHEMICAL VAPOR DEPOSITION USING DISILANE. M.S. Carroll, Agere Systems, Murray Hill, NJ; J.C. Sturm, Dept. of Electrical Engineering, Princeton University, Princeton, NJ; E. Napolitani, D. De Salvador, and M. Berti, INFM and Dept. of Physics, University of Padova, Padova, ITALY.

The incorporation of high concentrations of carbon in SiGe heterojunction bipolar transistors (HBT) is used to engineer the base dopant profile, significantly improving the device performance [1]. However, because interstitial carbon is identified as a deep level that can degrade device characteristics, unlike substitutional carbon [2], great care is taken to insure that the incorporated carbon is substitutional. To incorporate such high carbon concentrations, several orders of magnitude above solid solubility ($\sim10^{17}$ cm^{-3}), special epitaxial growth conditions are required. One identified critical growth condition that enhances substitutional carbon incorporation is a rapid growth rate at relatively low growth temperature [3]. Because the growth rate of silicon and SiGe by rapid thermal chemical vapor deposition (RTCVD) is strongly dependent on the choice of silicon source gas and disilane is known to produce significantly higher silicon growth rates compared to the typical silicon source gases used for SiGe epitaxy (silane and dichlorosilane), disilane is a good candidate for enhanced substitutional incorporation of carbon and throughput of SiC and SiGeC layers. In this paper we characterize SiGeC and SiC grown between 550-625°C using a mixture of 10% disilane in hydrogen as the silicon source gas. The layers were characterized using secondary ion mass spectrometry (SIMS), X-ray diffraction (XRD), Fourier Transform Infrared (FTIR) absorption, and transmission electron spectroscopy (TEM). Growth conditions are described to obtain high carbon concentrations that are 100% substitutional in either $Si_{1-x}C_x$ or $Si_{0.93-x}Ge_{0.07}C_x$ epitaxial layers. More than enough substitutional carbon (0.8%) is incorporated into the $Si_{0.93-x}Ge_{0.7}C_x$ layer to compensate the strain produced by the lattice mismatch of the SiGe layer demonstrating that completely strain compensated SiGeC layers may be grown for the first time by RTCVD. The thermal stability of the $Si_{0.996}C_{0.004}$ and $Si_{0.926}Ge_{0.07}C_{0.004}$ layers is also examined after annealing at 850°C for 2-10 hours in nitrogen. The substitutional carbon is very stable (XRD) and a significant reduction of carbon outdiffusion from the $Si_{0.926}Ge_{0.07}C_{0.004}$ layer compared to the $Si_{0.996}C_{0.004}$ layer is observed. [1] H.J. Osten, G. Lippert, P. Gaworzewski, and R. Sorge, "Impact of low carbon concentrations on the electrical properties of highly boron doped SiGe layers," Appl. Phys. Lett., vol. 71, pp. 11, 1997. [2] G. Davies and R.C. Newman, "Carbon in monocrystalline Silicon," in Handbook on Semiconductors, T.S. Moss, Ed., 1994, pp. 1558. [3] T.O. Mitchell, J.L. Hoyt, and J.F. Gibbons, Appl. Phys. Lett., vol. 71, pp. 1688, 1997.

2:30 PM C4.4
STRUCTURE AND OPTICAL PROPERTIES OF Si/Ge MULTILAYER STRUCTURE GROWN BY MBE. N.D. Zakharov, P. Werner, G. Gerth, U. Gösele, G. Cirlin, V.A. Egorov, B.V. Volovik, Max Planck Inst of Microstructure, Physics, Halle, GERMANY.

Multilayer structures containing Ge submonolayers in Si matrix were grown by MBE on Si substrates at different temperatures. An additional peak at 1.068 eV was observed in photoluminescence spectra (PL) from the samples grown at T=600°C, 650°C and 700°C, whereas it was absent in specimens grown at 750°C. Electron microscopy structure investigations show a high density of coherent Ge inclusions in sample grown at 650°C, whereas they were not formed at 750°C. This fact indicates that observed PL peak is unambiguously related to Ge inclusions. High temperature growth at 750°C results in formation of modulated structure where the composition changes sinusoidally with periods 1.2 nm and 0.44 nm along $< 113 >$ and $< 112 >$ directions, respectively. This results in distortion of the cubic symmetry and misfit stress a relaxation. The influence of compositional modulations on optical properties of grown layers is discussed.

3:15 PM C4.5
AB-INITIO CALCULATIONS TO MODEL ANOMALOUS FLUORINE BEHAVIOR. Milan Diebel, Scott T. Dunham, University of Washington, Dept of Physics, Seattle, WA; University of Washington, Dept of Electrical Engineering, Seattle, WA.

Implanted fluorine has been observed to behave unusually in silicon, manifesting apparent uphill diffusion [1]. We are further motivated to understand the behavior of implanted fluorine in silicon by experiments which suggest that fluorine reduces boron diffusion and enhances boron activation in shallow junctions [2]. In order to investigate fluorine behavior, we calculated the energy of fluorine defect structures in the framework of Density-Functional-Theory (DFT). Besides identifying the ground-state configuration of a single fluorine atom in silicon, a set of energetically favorable fluorine defect structures were found. The latter strongly suggest a distinct fluorine diffusion mechanism. In its ground-state, a single fluorine prefers to reside in a tetrahedral interstitial site. The interstitial site is preferred by 0.81 eV over the lowest substitutional site, and DFT calculations show interstitial F to be highly mobile ($E^m_{F_i} = 0.7$ eV) [3]. However, we found F_nV_m structures to have a rather high binding energy, suggesting decoration of vacancies by fluorine. In fact, for two or more F atoms, these structures are favored over the interstitial configuration, and for four or more F atoms, clusters are even stable in the presence of interstitials. Due to the entanglement of the fluorine atoms with the surrounding silicon lattice, we believe these defects to be immobile. The evolution of F_nV_m clusters is particularly important during implant anneals due to the high point defect concentrations. We also investigated pairing of F_i with I and F_i. DFT predicts interstitial F_2 to be unstable, as the fluorine prefers to take on valence band electrons rather than forming a F_2 bound-state. F_i binds to I with an energy of 1.09 eV. Thus these structures can affect fluorine diffusion in the presence of I supersaturation. These calculations provide insight into F behavior in silicon and we use this information to develop continuum models which we compare with experimental results. [1] S.-P. Jeng, T.-P. Ma, R. Canteri, M. Anderle, and G.W. Rubloff, Appl. Phys. Lett. **61**, 1310 (1992). [2] T.H. Huang, and D.L. Kwong, Appl. Phys. Lett. **65**, 1829 (1994). [3] C.G. Van de Walle, F.R. McFeely, and S.T. Pantelides, Phys. Rev. Lett. **61**, 1867 (1988).

3:30 PM C4.6
EFFECT OF FLUORINE ON THE DIFFUSION OF BORON IN AMORPHOUS SILICON. Jeannette Jacques, Kevin Jones, University of Florida, Dept. of Materials Science & Engineering, Gainesville, FL; Lance Robertson, Texas Instruments Inc., Dallas, TX; Mike Rendon, Motorola, Austin, TX; Joe Bennett, International SEMATECH, Austin TX.

Fluorine and boron co-implantation within amorphous silicon is being studied in order to meet the process challenges regarding P+ ultra-shallow junction formation. Previous experiments have shown that fluorine can reduce boron TED (Transient Enhanced Diffusion), enhance boron solubility and reduce sheet resistance. In this study, boron diffusion characteristics prior to solid phase epitaxial regrowth (SPER) of the amorphous layer in the presence of fluorine are addressed. Samples were pre-amorphized with Si+ at a dose of 1e15 ions/cm2 and energy of 70 keV, leading to a continuous amorphous surface of approximately 1500 Å. After pre-amorphization, B+ was implanted at a dose of 1e15 ions/cm^2 and energy of 500 eV, while F+ was implanted at a dose of 2e15 ions/cm^2 and energies ranging from 3 keV to 9 keV. Prior to annealing, SIMS profiles demonstrated that boron concentration tails broaden with increasing fluorine implant energy. This effect will be discussed. Furnace anneals for the F+ implant energy of 6 keV were conducted at 550°C, for times ranging from 5 minutes to 260 minutes. It was observed that during the boron in samples co-implanted with fluorine exhibited significant enhanced diffusion within amorphous silicon. After crystallization, the boron diffusivity was dramatically reduced. Boron in samples with no fluorine did not diffuse during SPER. The role of fluorine implants on both the as-implanted and annealed boron profiles will be further discussed.

3:45 PM C4.7
AB-INITIO PSEUDOPOTENTIAL CALCULATIONS OF PHOSPHORUS DIFFUSION IN SILICON. X.-Y. Liu, Motorola, Computational Nanoscience Group, Los Alamos, NM; W. Windl, Ohio State Univ, Dept of Materials Science and Engineering, Columbus, OH; K. Beardmore, and M.P. Masquelier, Motorola, Computational Nanoscience Group, Los Alamos, NM.

In traditional models of P diffusion in Si, vacancy assisted diffusion mechanism has been assumed. More recently, experiments have determined that for intrinsic P diffusion in Si, the interstitial assisted diffusion mechanism dominates. We have performed ab-initio pseudopotential calculations to study P diffusion in Si. Special care is taken with regard to structure minimization, charge state effects and corrections. We found that for intrinsic P diffusion, the interstitial assisted diffusion mechanism dominates, in agreement with recent experimental observations. We calculated the defect formation energies and migration barriers for the various competing interstitial-P complex diffusion mechanisms for low concentration P region, as well as the energetics of different charge states vacancy-P complex diffusion. Comparison of theoretical predictions with experiments is given and discussed.

4:00 PM C4.8
DETERMINATION OF SILICON POINT DEFECT PROPERTIES FROM VARIOUS DATA SOURCES. Heidi Meyer, Scott T. Dunham, University of Washington, Dept of Materials Science and Engineering, Seattle, WA; University of Washington, Dept of Electrical Engineering, Seattle, WA.

To effectively predict complex phenomenon such as transient enhanced diffusion (TED) and atomic-scale diffusion mechanisms, it is important to have correct point-defect parameters. Different types of experiments are more or less sensitive to specific aspects of point-defect properties (e.g. $D_I C_I^*$ product, D_V). Thus, to most accurately characterize point-defect parameters, we considered metal diffusion, silicon self-diffusion, and transient enhanced diffusion (TED) experiments. To successfully complete the aforementioned

objectives, we examined Bracht *et al.'s* metal and silicon-self diffusion, Ural *et al.'s* silicon self-diffusion, and TED experiments by Solmi and Packan, all of which produced varying parameter values. To accurately determine a set of parameters and confidence limits, we fit multiple temperatures, data sources, and process conditions simultaneously, using a non-linear optimizer.

SESSION C5: DEFECT AND DIFFUSION MODELS
Chairs: Mark E. Law and Alain Claverie
Thursday Morning, April 4, 2002
Salon 14/15 (Marriott)

8:00 AM ***C5.1**
SIMULATION OF TRANSIENT ENHANCED DIFFUSION IN SILICON TAKING INTO ACCOUNT OSTWALD RIPENING OF DEFECTS. Masashi Uematsu, NTT Basic Research Laboratories, Atsugi, JAPAN.

The transient enhanced diffusion (TED) of dopants in silicon is a central issue in silicon device processing because TED is a limiting factor in the scaling down of device size. End-of-range (EOR) defects form at the amorphous/crystalline (a/c) interface following amorphizing implantation. EOR defects act as both a sink for and source of self-interstitials (I), depending on temperature and annealing time, and hence affect TED. In addition, Ostwald ripening of EOR defects reduces their efficiency as a source of self-interstitials, which further complicates TED. In this study, TED of high-dose implanted P is simulated taking into account Ostwald ripening of EOR defects. Our simulation is integrated step-by-step beginning with simpler diffusion phenomena so that the simulation is done in a unified manner. First, we integrated a basic diffusion model based on the simulation of in-diffusion, where no implanted damages are involved. Second, from low-dose implantation, we developed a model for TED due to {311} self-interstitial clusters involving Ostwald ripening and the dissolution of {311} clusters. Third, from medium-dose implantation, we showed that P-I clusters should be taken into account, and during the diffusion, the P-I clusters are dissolved to emit self-interstitials that also contribute to TED. Finally, from high-dose implantation, EOR defects are modeled, and for Ostwald ripening of EOR defects, we derived a formula to describe the time-dependence based on the model by Claverie et al. The simulation results indicate that Ostwald ripening of EOR defects is more significant at higher temperatures and longer annealing times. The simulation satisfactorily predicts the TED for annealing conditions, where the calculations overestimate the diffusion without taking Ostwald ripening into account.

8:30 AM **C5.2**
A MODEL FOR BORON TED IN SILICON: FULL COUPLINGS OF DOPANT WITH FREE AND CLUSTERED INTERSTITIALS.
F. Boucard, PHASE/CNRS, Strasbourg, FRANCE and SILVACO France, Montbonnot, FRANCE; D. Mathiot, PHASE/CNRS; P. Rivallin, LETI, Grenoble, FRANCE; and E. Guichard, SILVACO France.

Ion implantation is the common technique used for doping advanced silicon devices in microelectronics. This technique induces a huge supersaturation of point defects in the Si crystal which leads to an anomalous broadening of the dopant profile during the high temperature activation anneals. This phenomenon, known as transient enhanced diffusion (TED) of dopant, is very noticeable for boron diffusion. It is also now well established that TED is strongly correlated with the evolution of the self-interstitial supersaturation governed by the nucleation and evolution, during the high temperature anneal, of a variety of extended defect structures like Boron Interstitial Clusters (BIC) or Interstitials Clusters (IC). Thus, predictive process modeling, needed for deep submicron MOSFET technologies, requires the development of accurate diffusion models taking into account the full set of interactions between the dopant and the point or extended defects. The purpose of this contribution is to present such a model based on the pair diffusion mechanism including non-equilibrium reactions between the dopant and the free point defects, taking into account their various charge states. In addition to, and fully coupled with the dopant diffusion, we simulate the IC's and BIC's behavior. The IC's evolution is described according to the model proposed recently by C.J. Ortiz et al.[1] for the nucleation and growth of {311} defects based on thermodynamic and kinetic consideration, while the BIC's kinetics and charge states are chosen according to a recent ab-initio calculation [2]. The model developed in this work is shown to be able to simulate a very large set of experimental conditions, from conventional predeposition steps, up to RTA after low energy implantation. [1] C.J. Ortiz and D. Mathiot, Mat. Res. Soc Symp. Proc. Vol 669, Paper J.5.6, (2001) [2] J. Lenosky et al., Appl. Phys. Lett 77, 1834 (2000).

8:45 AM **C5.3**
COMPUTATIONALLY EFFICIENT MODELING OF TED KINETICS AT LOW AND HIGH TEMPERATURES BASED ON THE ANALYSIS OF SMALL SELF-INTERSTITIAL CLUSTERS IN SILICON. Pavel Fastenko, Scott T. Dunham, Electrical Engineering Department, University of Washington, Seattle, WA; Srinivasan Chakravarthi, Electrical and Computer Engineering Department, Boston University, Boston, MA.

In this work, we describe our approach to the modeling of transient enhanced diffusion in silicon after implantation and annealing at both low and high temperatures based on a "merged" small cluster/ moment-based model. Cowern and co-workers measured TED of B-doped marker layers to determine the transient interstitial supersaturation during interstitial cluster formation and growth. They used inverse modeling to derive the binding energy versus size relationship for self-interstitial clusters from the interstitial supersaturation. They found two energetically stable small clusters at sizes four and eight while near-constant behavior was assumed for large (n>15) rod-like defects. Cowern et al. derived their model based on the assumption that compact self-interstitial clusters grow and transform into {311} type defects. However, more recent theoretical studies have not found any energetically favorable transition pathways between small compact structures and elongated {311} defects.
Our model is based on the assumption that compact clusters and rod-like defects form two independent populations interacting only via the supersaturation of free interstitials and di-interstitials. Following ab-initio calculations results by Kim et al., we assume that three energetically favorable compact clusters exist (size 2, 3, 4). Based on MD results, the energy of {311} defects is described as a simple power law function of size, so that the system (clusters and 311s) has only 5 free parameters. To derive our model, the full set of rate equations is first solved on a single grid point and the expressions for evolution of the moments of the size distribution are parameterized. The reduced coupled moment-based/small cluster model is derived based on the results of the full model and is compared to the experimentally measured supersaturation of interstitials, as well as to the interstitial density in {311} defects. The resulting model allows accurate prediction of TED kinetics over the full range of thermal budgets.

9:00 AM **C5.4**
COMPLETE SUPPRESSION OF THE TRANSIENT ENHANCED DIFFUSION OF B IMPLANTED IN PREAMORPHIZED SILICON BY INTERSTITIAL TRAPPING IN A SPATIALLY SEPARATED C-RICH LAYER. E. Napolitani, A. Coati, D. De Salvador, A. Carnera, INFM and Dept. of Physics, Padova, ITALY; S. Mirabella, S. Scalese, F. Priolo, INFM and Dept. of Physics and Astronomy, Catania, ITALY.

A method for completely suppressing the transient enhanced diffusion (TED) of boron implanted in preamorphized silicon is demonstrated. Boron is implanted in a molecular beam epitaxy (MBE) grown silicon sample that has been previously amorphized by silicon implantation. The sample is then annealed in order to epitaxially regrow the amorphous layer and electrically activate the dopant. The back-flow of silicon interstitials released by the preamorphization end-of-range (EOR) damage is completely trapped by a carbon-rich silicon layer interposed by MBE between the damage and the implanted boron. No appreciable TED is observed in the samples up to complete dissolution of the EOR damage. Optimized annealing conditions for the solid phase epitaxy and dopant activation result in the complete activation of boron with negligible diffusion, the tail shift of the B profile being less than 3 nm with respect to the as implanted sample. The method is highly promising for the realization of ultra shallow junctions by ultra low energy implantation for the far future CMOS technology nodes.

9:15 AM **C5.5**
INTERACTION BETWEEN SELF- INTERSTITIALS AND SUBSTITUTIONAL C IN SILICON: INTERSTITIAL- TRAPPING AND C- CLUSTERING MECHANISM. S. Mirabella, S. Scalese, S. Pulvirenti, A. Terrasi, and F. Priolo, INFM and Dept of Physics and Astronomy, Catania, ITALY; A. Coati, D. De Salvador, E. Napolitani, A. Mattoni, G. Bisognin, M. Berti, A. Carnera, and A.V. Drigo, INFM and Dept of Physics, Padova, ITALY.

In this work the Si self-interstitials - carbon interaction has been experimentally investigated and modeled. The interactions between self-interstitials, produced by 20 keV silicon implantation, and substitutional carbon in silicon have been studied using a $Si_{1-y}C_y$ layer grown by molecular beam epitaxy (MBE) and interposed between the near surface self-interstitials source and a deeper B spike used as a marker for the Si- interstitials concentration. The C atoms, all incorporated in substitutional sites and with a C- dose range of 7 • 10^{12} - 4 • 10^{14} at/cm^2, trap the self-interstitials in such a manner that the $Si_{1-y}C_y$ layer behaves as a filtering membrane for the interstitials flowing towards the bulk and, consequently, strongly

reduces the boron enhanced diffusion. This trapping ability is related to the total C dose in the $Si_{1-y}C_y$ membrane. Substitutional carbon atoms interacting with self-interstitials are shown to trap Si-interstitials, to be removed from their substitutional sites, and to precipitate into the C-rich region. After precipitation, C atoms are not able to further trap injected self-interstitials and the interstitials generated in the surface region can freely pass through the C- rich region and produce B enhanced diffusion. The atomistic mechanism leading to Si-interstitial trapping has been investigated by developing a simulation code describing the migration of injected interstitials. The simulation takes into account the surface recombination, the interstitial diffusion in our MBE grown material, and C traps. Since the model calculates the amount of interstitials that actually react with C atoms, by a comparison with the experimental data it is possible to derive quantitative indications on the trapping mechanism. It is shown that one Si-interstitial is able to deactivate about two C traps by means of interstitial trapping and C-clustering reactions. The reactions causing trapping and deactivation are tentatively described.

9:30 AM C5.6
MODELING OF SELF-INTERSTITIAL DIFFUSION IN IMPLANTED SILICON CONTAINING INTERSTITIAL TRAPS.
D. De Salvador, A. Mattoni, E. Napolitani, A. Coati, G. Bisognin, M. Berti, A. Carnera, and A.V. Drigo, INFM and Dept. of Physics, Padova, ITALY; S. Mirabella, S. Scalese, S. Pulvirenti, A. Terrasi, and F. Priolo, INFM and Dept. of Physics and Astronomy, Catania, ITALY.

The quantification of the number of silicon self-interstitials (I) injected into the bulk by implant and subsequent annealing is a debated matter. This is a crucial problem since the interstitials injected into the bulk control important physical processes such as the dopant diffusion and the formation of I-dopant and I-impurity clusters. A proper solution involves the knowledge of many non-trivial physical processes: i) the dissolution dynamics of the I-clusters produced by the implant; ii) the evaporation of interstitials through the surface; iii) the interaction of the interstitials with interstitial traps present in intrinsic MBE silicon or intentionally incorporated during growth. The model consists in a set of rate equations describing the interstitials diffusion in a trap-containing medium with the addition of terms describing the interstitials injection and the surface evaporation. We found an approximated analytical solution of the model providing a simple understanding of the interplay between the physical parameters involved and a straightforward comparison with experimental data obtained by the broadening analysis of boron delta doping arrays. The calculations allow to demonstrate that the I injected into the bulk at the end of the I-clusters dissolution do not depend on the detailed time evolution of the I-clusters, but only on the total amount of I produced by the implant. Fit to experimental data allows to quantify important physical parameters such as the I evaporation length at the surface and the intrinsic trap density. Several applications of the model will be shown in the case of MBE materials intentionally doped with interstitial traps such as B and C. The model successfully predicts the TED suppression by I-traps and quantitatively describes the formation of I-trap clusters (C-I and B-I clusters) and their average composition. Extension of the model to a 2-dimensional diffusion case will be shown.

10:15 AM *C5.7
THERMAL EVOLUTION OF EXTRINSIC DEFECTS IN ION IMPLANTED SILICON: CURRENT UNDERSTANDING AND MODELLING.
Fuccio Cristiano, LAAS/CNRS, Toulouse, FRANCE; Benjamin Colombeau, Bernadette de Mauduit, Caroline Bonafos, Gerard Benassayag, Alain Claverie, CEMES/CNRS, Toulouse, FRANCE.

Ion implantation in silicon results in the creation of large concentrations of interstitials and vacancies which, upon annealing, tend to condense to form defects of various types. The interactions between these defects and the implanted dopants are at the origin of the transient enhanced diffusion (TED) phenomenon, one of the major problems in the realisation of future integrated circuits. As a consequence, the understanding and the physical modelling of defect evolution during annealing have become crucial issues. In this paper, we will recall the structure of the various types of extended defects as a function of annealing conditions and present an extensive study of their thermal behaviour on the basis of TEM analysis. We will show that, in most cases, all these defects are of extrinsic character and that their kinetics can be described by an Ostwald ripening process whereby the defects exchange Si atoms and evolve in size and type to minimise their formation energy. Because of this interchange, the region where the defects are located is oversaturated with Si interstitial atoms, therefore providing the source for TED. We will also recall recent experiments showing the role of the surface in the defect evolution. Finally, we will present a physically based model to predict the evolution of these extrinsic defects during annealing. Our model makes use of the combined physical concepts of non-conservative Ostwald ripening and defect formation energy and calculates the time evolution of defect densities, size distributions, number of clustered interstitials and free-interstitial supersaturation. We will present some applications of our model to a variety of experimental conditions and we will give an example of its predictive capabilities. In summary, we demonstrate that the modelling of defect evolution during annealing in a variety of technological conditions can be achieved using the combined physical concepts of Ostwald ripening and formation energy of extrinsic defects.

10:45 AM C5.8
ANNEALING BEHAVIOR OF LOCALLY CONFINED DISLOCATION LOOPS UNDER INERT AND OXIDIZING AMBIENT.
C. Tsamis, D. Skarlatos, I. Raptis, D. Tsoukalas, Inst. of Microelectronics, NCSR 'Demokritos', Aghia Paraskevi, GREECE; B. Colombeau, A. Claverie, CEMES/CNRS, Toulouse, FRANCE.

Dislocation Loops (DL's) are two-dimensional extended defects, formed in the silicon crystal after annealing of an amorphizing implant and their presence in specific areas of modern semiconductor devices strongly degrades the device performance. On the other hand, DL's have been used as point defect detectors to study point defect injection processes and to extract point defect parameters in silicon. In all these studies DL's exist as a 2-D "band" of defects, while no work has been reported for the growth of DL's when these are laterally confined in the silicon crystal. The behavior of the defects under such conditions would be much more representative of situation encountered during S/D formation in a real device. In this work, we report data for the growth kinetics of DL's organized within lines of controlled dimension and periodicity. DL's were created by Si-implantation, through openings in mask windows and annealing. The width of the lines was 1 μm while the distance between adjacent lines ranged from 0.2 to 5 μm. The growth kinetics of the DL's were investigated using TEM and compared both under inert and oxidizing conditions. During oxidation, the loops within the lines grow faster than within a continuous layer of DL's. A striking result is observed at 900°C after 2h dry oxidation, where the DL's placed within lines 5 μm apart, grow so fast that the perfect dislocation loops disappear and the Frank loops intercept the surface and have semi-circular shape. Such phenomena are observed in continuous loop layers at much higher interstitial injection (f.e. 950°C for 2h). It is also observed that, as the distance between the loop lines increases, the number of atoms bounded within the loops increases. These experiments are efficient in mapping the 2-D distribution of interstitials and allow, when combined with simulation, the extraction of parameters relevant for the description of lateral diffusion of point defects in silicon.

11:00 AM C5.9
MODELING DISLOCATION LOOP NUCLEATION AND EVOLUTION IN GERMANIUM, ARSENIC AND BORON IMPLANTED SILICON.
I. Avci , M.E. Law, Swamp Center, Department of Electrical and Computer Engineering, University of Florida, Gainesville, FL.

Ion implantation is mainly used to introduce impurity atoms into the silicon substrate. Implant species play an important role on the defect formation and and defect evolution. Light ions usually form {311}'s and dislocation loops around the projected range. Meanwhile, arsenic and germanium are heavy ions and they usually produce amorphous layers which leads to end of range defects. Previously, we presented a loop nucleation and evolution model in silicon implanted silicon. In this study, the model is extended to predict the EOR and projected range defect nucleation and evolution due to different ion implant species. The model assumes that all the nucleated loops come from {311} unfaulting and the loop density and average loop radius follow a log normal distribution. Ostwald ripening becomes dominant when excess interstitial density drops to the values close to equilibrium interstitial concentration. The model is verified with the experimental data obtained from literature for various implant species (i.e. germanium, arsenic, boron) and implant doses and energies. Modeling results are in agreement with the experimental results.

11:15 AM C5.10
ROLE OF DIFFUSION AND CLUSTERING MECHANISMS IN THE EVOLUTION OF CARBON CONCENTRATION PROFILES IN SILICON.
N.E.B. Cowern, School of Electronics, Computing and Mathematics, Surrey University, UNITED KINGDOM; P. Meunier and P.A. Stolk, Philips Research Laboratories and IMEC, Leuven, BELGIUM; F. Roozeboom, Philips Research Laboratories, Eindhoven, THE NETHERLANDS; W. Lerch, Mattson-Steag, GERMANY.

Carbon (C) is emerging as a key impurity for use in diffusion control for ultrashallow, highly activated junctions, as well as in specialized applications such as SiGeC-based devices. Recently a number of experimental and modeling studies have looked at the diffusion and clustering of C at high concentrations in silicon, and the resulting suppression of diffusion and deactivation of implanted dopants like B

and P. Up to now, however, there has been no definitive experimental study on the basic mechanisms of C diffusion. This is urgently needed in order to understand and control C-assisted USJ formation and to enable predictive TCAD. Such basic insights can be achieved by diffusion studies involving injection of excess interstitials and excess vacancies, provided that competing effects such as C clustering can be eliminated. The latter can then be investigated as an additional effect occurring at higher C concentrations.
In this paper we report experiments on the diffusion of lightly ($2 \times 10^{18}/cm^2$) C-doped and moderately ($2 \times 10^{19}/cm^2$) C-doped impurity spikes in high-quality CVD-grown silicon. Samples from as-grown wafers were processed by RTP under inert, oxidizing and reducing ambients, and Si ion-implanted samples were processed by RTP in inert ambient, in the temperature range 600-1000 C. Dopant concentration profiles were measured by SIMS.
In our analysis of the data, the measured profiles for lightly C-doped samples are fitted to extract the substitutional-interstitial migration distance and migration frequency of C in silicon, and thereby determine the contributions of the kick-out and Frank-Turnbull diffusion mechanisms. SIMS profiles for the moderately C-doped samples are fitted to extract separately the additional effects arising from C clustering. The paper clarifies fully, for the first time, the separate roles of C diffusion and clustering in the suppression of interstitial-mediated diffusion in silicon.

SESSION C6/B9: JOINT SESSION CHARACTERIZATION USING SURFACE ANALYSIS TECHNIQUES

Chairs: Daniel F. Downey and Janice L. Veteran
Thursday Afternoon, April 4, 2002
Salon 10-12 (Marriott)

1:00 PM *C6.1/B9.1

ROUTINE DOPANT/IMPURITY AND STOICHIOMETRY CHARACTERIZATION OF SiGe AND SiON USING SURFACE ANALYSIS TECHNIQUES. Charles W. Magee, Evans East, (A Member of the Evans Analytical Group), East Windsor, NJ.

A critical technological benchmark of the SiGe HBT is its maximum oscillation frequency fmax, which is dependent on the base sheet resistance of the transistor. Reduction of the base sheet resistance results in a higher operating frequency. However, the peak boron concentration in the base is limited by boron out-diffusion. Incorporation of carbon into the SiGe has been shown to reduce this B out-diffusion.[1,2] These properties often require SIMS characterization for measuring the changes in the B distribution with growth and anneal, as well as determining the substitutional C concentration. The depth profile characterization by SIMS however, demands carefully set analytical protocols involving standards calibrated by other techniques for accurate quantification. In addition, the requirement to measure layer thicknesses or junction depths makes achieving good depth resolution during the analysis also important. A high dose C implant across the interface between an RBS-calibrated, B-doped SiGe epi layer and the Si substrate was prepared as a quantification reference material to characterize SiGeC:B epitaxial films. The protocol developed using a series of SiGe samples implanted with various elements provides concentration determinations for these elements with an accuracy of 5-10%. Several experimental conditions show that a low energy oxygen primary ion beam has to be used to measure an accurate B distribution in the sample, which is often used to determine the base layer thickness. Although Cs primary ion bombardment allows the accurate quantification of total B, C, O, P and Ge, using ion yield corrections, in a single analysis for cost effectiveness, the oxygen bombardment is necessary to obtain better depth resolution. A second part of this presentation focuses on siliconoxynitride-SiON gate dielectrics. As the thickness of these gate dielectrics is reduced, the demands on the analytical techniques used to characterize these films have increased. The characterization of the SiON films, which currently range from 1-5nm thickness and 1-25 atom% N, necessitates a combination of near surface characterization techniques and reference materials. Currently, Nuclear Reaction Analysis (NRA) is used in the calibration of reference materials; X-ray Photoelectron Spectroscopy is used measure total N concentration and thickness using these reference materials, and SIMS is used in combination with results of XPS to determine the nitrogen distribution.
[1]M.S. Carroll, J.C. Strum, T.H. Buyuklimanli, Phys. Rev. B64 August 2001.
[2]L.D. Lanzerotti, J.C. Sturm, E. Stach, R. Hull, & T.H. Buyuklimanli, C. Magee Appl. Phys. Lett. 70 (23) 3125 (1997).

SESSION C7: CHARACTERIZATION TECHNOLOGIES

Chairs: Michael J. Rendon and Daniel F. Downey
Thursday Afternoon, April 4, 2002
Salon 14/15 (Marriott)

1:45 PM C7.1

HIGH RESOLUTION MULTI-DIMENSIONAL DOPANT PROFILING BY SCANNING TUNNELING MICROSCOPY. Lequn Liu, Jixin Yu, and Joseph W. Lyding, Beckman Institute, University of Illinois, Urbana, IL; Frankie Liu, and James D. Plummer, Department of Electrical Engineering, Stanford University, Stanford, CA.

Due to the random nature of ion implantation, dopant diffusion, and other processes involved in the doping of silicon devices, the dopant number in shallow junctions and short channels is subject to stochastic variations, which translate directly into variations in device behavior. Nanometer scale resolution dopant profilers are needed to properly measure these dopant fluctuations. In this paper, we use scanning tunneling microscopy (STM) and spectroscopy (STS) to measure dopant profiles with nanometer scale resolution across PN junctions of Si devices. The Si surface is passivated by hydrogen in order to eliminate surface states. STM topographical images, dI/dV images and current image tunneling spectroscopy (CITS) are acquired across PN junctions. Two-dimensional dopant and carrier profiles are extracted from the CITS data. Moreover, individual P and N type dopant induced features are observed on the hydrogen-passivated surface. The amplitudes of the dopant induced features depend on the dopant type, dopant density, sample bias, and the depth of the dopants. Based on the depth dependence of the amplitudes, the position of the individual subsurface dopants can be identified, and thus three dimensional subsurface dopant map can be generated. This work reveals the real physical picture of randomly distributed dopants and can be used to verify and calibrate TCAD simulators.

2:00 PM C7.2

PROFILE CHANGES AND SELF SPUTTERING DURING LOW ENERGY ION IMPLANTATION. W. Vandervorst, T. Janssens, B. Brijs, R. Lindsay, IMEC; E.J.H. Collart, David A. Kirkwood, Applied Materials, Implant Division, UNITED KINGDOM; G. Mathot, G. Terwagne, Univ. Namur, LARN, Namur, BELGIUM.

Due to the reduction in primary beam energy, self sputtering during low energy ion implantation has become an important factor influencing the retained dose. Since sputtering is directly proportional with the near surface concentration, high resolution SIMS has been used to analyze low energy B, BF2, As and Sb-profiles. Dose retention has been monitored using nuclear reaction analysis and RBS. At low energies the retained dose becomes considerably less than the nominal implant dose and reaches a steady limit for doses as small as 5e15 - 1e16 at/cm^2. At that point the self sputtering yield is equal to one. The dose saturation at these low fluences is at variance with theoretical predictions (based on standard theory for ion retention in combination with sputtering) and computer models which were originally developed for the simulation of SIMS profiling. Both predict a saturation only for doses as high 1e17 at/cm^2. The explanation can be found by analyzing the drastic changes in the profile which occur during the implantation process itself. For most elements a strong surface segregation, during the implant process itself, can be seen which of course does increase the self sputtering yield drastically. These observations are reminiscent of the observations in SIMS whereby also an enhanced mobility of B during ion irradiation can be observed leading to the anomalous B-surface peak in many SIMS profiles. In particular for B, the amount of surface segregation is dose dependent which suggests that the thermodynamic driving force might be concentration dependent. Whereas the surface segregation explains the rapid dose saturation, the component sputter yield which can be derived from the SIMS profiles in combination with the retained (and sputtered) appears to be 2-5 higher that the matrix sputter yield. An explanation must probably be sought in a weak bonding of the segregated species leading to a reduced surface binding energy and thus enhanced sputtering yield.

2:15 PM C7.3

JUNCTION AND PROFILE ANALYSIS USING CARRIER ILLUMINATION. T. Clarysse, W. Vandervorst, R. Lindsay, IMEC; P. Borden, E. Budiarto, J. Madsen and R. Nijmeijer, Boxer Cross Inc.

Carrier Illumination (CI) is an optical technique for non-destructive in-line monitoring of post-anneal junction depth and pre-anneal PAI depth and dose. This work presents a systematic study of CI response to a wide variety of post- and pre- anneal implant processes, varying parameters including species, implant energy and dose, annealing condition, and surface preparation. The aim is to characterize CI over a range of processes and develop new uses, for example, to extend the technique to exploit profile sensitivities. For annealed profiles, samples

containing B, BF2 and As-implants with and without Ge PAI layers, with junction depths between 10-2000 nm, were measured. CVD-grown layers were also fabricated and measured to obtain comparison to near-ideal box-like profiles. Whereas for the abrupt CVD profiles, CI primarily samples the junction position with sub-nm resolution, it is shown for more graded implant + RTA layers that the best SIMS junction depth correlation is a function of generation laser power. The concentration level at which the correlation is made, can be adjusted over a concentration range of approximately 3x1018 to 2x1019/cm3 implying that the CI measurement has profile sensitivity. This behaviour is expected, and is due to the dependence of the induced photo-generated carrier profile at the junction edge on the profile shape and generation laser power. A discussion of simulations supporting these results is provided. For un-annealed profiles, as-implanted B, BF2, As and Sb-implants have been analyzed as a function of energy and implant dose. A very steep decrease of the CI signal with increasing dose is observed in the regime below amorphization. This behaviour is consistent with the model of implant-induced point defects acting as recombination centers. In this region a sensitivity as high as 1-5 e4 mV/decade can be observed implying a sensitivity of 0.5-1% at an assumed noise level of about 75 mV. Additional details of this response and its correlation to a vacancy model wi! ll be presented.

2:30 PM C7.4
CALIBRATION OF PHOSPHORUS IMPLANTATION DOSE IN SILICON BY RADIOCHEMICAL NEUTRON ACTIVATION ANALYSIS. Rick L. Paul, David S. Simons, Chemical Science and Technology Laboratory, National Institute of Standards and Technology, Gaithersburg, MD.

The U.S. semiconductor industry relies on secondary ion mass spectrometry (SIMS) for characterization of the depth distribution of dopants such as boron, arsenic, and phosphorus in silicon. To assist the industry in achieving high accuracy measurements, Standard Reference Materials (SRMs) of boron and arsenic implants in silicon have been developed by NIST as SIMS calibration standards. Plans are underway to develop a phosphorus implant in silicon SRM, to be certified by radiochemical neutron activation analysis (RNAA). RNAA was chosen because other techniques lack the necessary sensitivity, chemical specificity and matrix independence to measure phosphorus at implantation levels. During RNAA, ^{31}P undergoes neutron capture to form ^{32}P. The ^{32}P is then separated and purified of other radionuclides before quantification by beta counting. Preliminary measurements, carried out on six pieces of a phosphorus-implanted silicon wafer previously used in a round-robin study of SIMS measurement repeatability, yielded a mean and standard deviation of $(8.35 \pm 0.20) \times 10^{14}$ atoms cm^{-2} (relative standard deviation = 2.35%), in agreement with both the nominal implantation dose (8.5 x 10^{14} atoms cm^{-2}) and a consensus value of $(8.23 \pm 0.33) \times 10^{14}$ atoms cm^{-2} determined from the SIMS investigation. The expanded uncertainty of the measurements was evaluated at 4.6 %. Modifications to the original procedure as well as refinements in the processing and measurement of silicon blanks have resulted in better precision and lower uncertainties. Measurement of twelve additional samples of the implanted silicon using the improved procedures yielded a mean and standard deviation of $(8.32 \pm 0.11) \times 10^{14}$ atoms cm^{-2} (relative standard deviation = 1.3%), and an expanded uncertainty of about 3%. Based on this work, it should be possible to determine the implanted phosphorus dose in silicon with an expanded uncertainty of 3% or better, which is acceptable for this SRM.

3:15 PM C7.5
FOCUSED ION BEAM PREPARED TEM SAMPLES FOR 2-D DOPANT PROFILING. Y.C. Wang, X. Da, E. Van Cappellen, FEI Company, Hillsboro, OR; Hui-Chen Chang, TSMC, Hsin-Chu, TAIWAN; M. Weschler, M. Darus, and M. Bernas, FEI Company, Hillsboro, OR.

Typical dopant levels (10^{15} to 10^{20} cm^{-3} well concentrations) will not alter the amplitude term of the incident electron wave sufficiently to depict visible contrast in the conventional TEM (Transmission Electron Microscopy) mode. However, the electric fields across the dopant area will modulate the phase term of the incident electron wave and this will be visible in the reconstructed holographic phase image. Electron holography offers us the ability to image and quantify the electric field in two dimensions that is inaccessible to detection by other analytical techniques. TEM samples for 2-D dopant profiling were prepared by the FEI Dualbeam Workstation with the sample ranging from 200 to 350 nm. If the sample is thicker than 400 nm, the holographic fringe contrast will be deteriorated and give rise to a seriously wrapped phase image. The use of FIB will provide site-specific capabilities for TEM sample preparation as well as the reproducible thickness of the sample and the electrically inactive layers. However, the electrically inactive layers on both side of the FIB prepared TEM samples could be removed by about 50% using the low kV ion beam cleaning with appropriate tilting angles toward the ion beam. Milling deeper at the region of interest could mitigate the curtaining effects generated by the different sputtering rate of different materials. A thin carbon layer coating could also remove the charging on the surface of the dopant profiling samples. A vacuum area near the region of interest (dopant area) is necessary to normalize and quantify the reconstructed phase image. Preliminary results of the low magnification Holography using Lorentz lens on FEI Tecnai series FEG TEM will be discussed. The spatial resolution of the Lorentz lens holography set up is about 2 nm and the holographic field of view ranges from 0.5 to 1 μm.

3:30 PM C7.6
2-D P-N JUNCTION PROFILING IN CMOS DEVICES BY ELECTRON HOLOGRAPHY. M.A. Gribelyuk, IBM Microelectronics Div, Hopewell Junction, NY; M.R. McCartney, Center for Solid State Science, Arizona State Univ, Tempe, AZ; J. Li, Dept of Physics and Astronomy, Arizona State Univ, Tempe, AZ; C.S. Murthy, P. Ronsheim, B. Doris, J.S. McMurray, IBM Microelectronics Div, Hopewell Junction, NY; S. Hegde, IBM T.J. Watson Research Center, Yorktown Heights, NY; D.J. Smith, Center for Solid State Science and Dept of Physics and Astronomy, Arizona State Univ, Tempe, AZ.

Quantitative 2-D maps of the electrostatic potential in 0.13μm and 0.35μm pFET devices were produced with a spatial resolution of 6 nm and precision of 0.17 V using off-axis TEM electron holography. These results were directly compared to SIMS and process simulations. In particular, the close match of the depth dependence of dopant diffusion to those derived by SIMS and process simulations was established without any consideration of "dead layers", which simplified the electron holography experiment and made its application more robust. The consistency of the results of electron holography has been proved by comparison of devices subjected to the same processing conditions. Increase of electrostatic potential was observed near Si surface in the source and drain regions of the device. In this regard process simulation has evaluated the relative importance of B deactivation, B segregation and surface charging effects. Our direct comparison of electron holography, SIMS and process simulation results has demonstrated that electron holography can be used to assess the accuracy of the process simulation models. These results indicate that electron holography could become an effective method for quantitative 2-D analysis of p-n junctions in deep-submicron devices.

3:45 PM C7.7
PULSED FORCE-SCANNING SPREADING RESISTANCE MICROSCOPY (PF-SSRM) FOR HIGH SPATIAL RESOLUTION 2D-DOPANT PROFILING. Pierre Eyben, Marc Fouchier, Pierre Albart, Jeremy Charon-Verstappen, Wilfried Vandervorst, IMEC vzw, Leuven, BELGIUM.

The biggest disadvantage of the AFM-based Scanning Spreading Resistance Microscopy (SSRM) electrical measurement technique is the necessity to use a high force between the tip and the sample to obtain a good electrical contact. This force is responsible for the fast damaging of the tip (and of the sample) while scanning. Tip damage is mainly due to the shear force occurring while scanning in contact mode at high forces leading to breakage (cleavage) of sharp tips or rapid increase of tip radius (wear). The latter prevents the use of metallic probes and affects the accuracy of the electrical measurements, as the contact radius is a determining parameter for quantification. The high force also prevents the simultaneous acquisition of high quality topography data. We have solved those problems by introducing the Modulated Force Principle (MFP) for AFM-based electrical measurement. MFP consists in applying a variable (e.g. pulsed) force while scanning reducing the force during the lateral movement of the tip and synchronizing the electrical measurements with force peaks. The latter results in lower lateral forces and introduces a quasi multi point contact mode. MFP also allows to obtain a better topography image by synchronizing the topography measurement with the low force part of the force cycle. Our new technique has shown drastic reductions of surface and probe damaging. Simultaneous acquisition of a good spreading resistance and topography during one scan has also been realized.

4:00 PM C7.8
DAMAGE AND DOPANT DISTRIBUTIONS PRODUCED BY ULTRA SHALLOW B AND As IMPLANTS INTO Si AT DIFFERENT TEMPERATURES CHARACTERIZED BY MEDIUM ENERGY ION SCATTERING. J.A. van den Berg, D.G. Armour, S. Zhang, S. Whelan, M. Werner, University of Salford, Joule Physics Laboratory, Salford, UNITED KINGDOM; E.H.J. Collart and R.D. Goldberg, Applied Materials, Horsham, UNITED KINGDOM; P. Bailey and T.C.Q. Noakes, CLRC Daresbury Laboratory, Daresbury, UNITED KINGDOM.

Medium energy ion scattering (MEIS), operated at sub-nm depth resolution in the double alignment configuration, has been used to

examine implant and damage depth profiles formed in Si substrates irradiated with 1 keV B^+ and 2.5 keV As^+ ions. Samples were implanted at 150°C, 25°C and 300°C to doses ranging from 3×10^{14} to 1×10^{16} cm^{-2}. MEIS measurements of the B implants indicate the formation of two distinct damage regions each with a different dependence on implant dose, the importance of dynamic annealing for implants at room temperature and above, a point defect trapping effect at the Si/oxide interface competing with dynamic annealing and the movement of point defects from the deeper damage layer to the surface upon annealing to 900°C. Low temperature B^+ implants result in the formation of an amorphous layer, the epitaxial regrowth of which at 600°C is arrested by the presence of defect clusters containing B. MEIS studies of the damage formation and annealing (RTA) due to As^+ implants also showed different damage effects depending on the implant temperature. Following epitaxial regrowth at 600°C, approximately half of the As was observed to be in substitutional sites, consistent with the reported formation of As_nV complexes ($n \leq 4$), while the remainder became segregated to and become trapped within a narrow, 1.1 nm wide layer at the Si/oxide interface. Notably different B and As distributions were measured by SIMS in the samples implanted at different temperatures following RTA up to 1100°C. The observed dependence of the dopant transient enhanced diffusion (TED) on implant temperature is discussed in terms of different dynamic annealing and defect agglomeration conditions during implantation.