SYMPOSIUM G

Materials for Flexible Electronic Displays and Devices

April 2 – 4, 2002

Chairs

Paul S. Drzaic
Alien Technology Corp
Ste 150
Morgan Hill, CA 95037
408-201-7435

Thomas N. Jackson
Center for Thin Film Devices
Pennsylvania State Univ
216 Electrical Engineering West
University Park, PA 16802-2701
814-863-8570

Dalen E. Keys
DuPont iTechnologies
Wilmington, DE 19880-0030
302-992-3465

Tatsuya Shimoda
Seiko-Epson Corp
Nagano-ken, 398-8502 JAPAN
81-266-52-8063

Symposium Support
Army Research Laboratory
Defense Advanced Projects Research Agency
Eastman Kodak Company

* Invited paper

SESSION G1: FLEXIBLE ELECTRONIC DEVICES AND COMPONENTS I
Chair: Thomas N. Jackson
Tuesday Morning, April 2, 2002
Golden Gate C1 (Marriott)

8:00 AM G1.1
EXPERIMENTAL CHARACTERIZATION AND PHYSICAL MODELING OF LOW TEMPERATURE a-Si:H TFTS.
Peyman Servati, Denis Stryahilev, Arokia Nathan, Andrei Sazonov, Electrical & Computer Engineering Department, University of Waterloo, Waterloo, Ontario, CANADA.

This paper investigates the effect of low temperature (120°C) fabrication processes on the key device parameters of amorphous silicon (a-Si:H) inverted staggered thin-film transistors (TFTs). The TFTs are fabricated on glass and plastic substrates and incorporate amorphous silicon nitride, intrinsic a-Si:H, and n^+ silicon layers grown at 120°C using conventional PECVD equipment. The key device parameters include threshold voltage, subthreshold slope, contact resistance, mobility, and leakage current, which we have systematically extracted from measurement data of a variety of specially designed TFT test samples fabricated in-house. Physically based simulation models have been developed that establish the relationship between TFT characteristics and physical parameters such as the density of interface states, insulator fixed charge, slope of the band tails in the a-Si:H, and the density of defects in both the a-Si:H and associated dielectric layers. These parameters are in turn strongly influenced by the low temperature process conditions and subsequent material integrity. The paper examines the behavior of these device parameters, along with the underlying physics, in relation to their higher temperature counterparts.

8:15 AM G1.2
LOW THRESHOLD VOLTAGE AMORPHOUS SILICON JUNCTION FIELD EFFECT TRANSISTOR: SIMULATION AND EXPERIMENT. Domenico Caputo, Giampiero de Cesare, Francesco Lemmi, Fabrizio Palma, University of Rome "La Sapienza", Dept. of Electronic Engineering, Rome, ITALY; Mario Tucci, ENEA Research Center, Portici, Naples, ITALY.

Hydrogenated amorphous silicon thin film transistors (TFT) are commonly used as switching devices of in flat panel displays. However, analog applications of a-Si:H, either using bipolar transistor or MOS structures, are limited by the very small minority carrier diffusion length or the low channel conductance, respectively. In this work a Junction Field Effect Transistor (JFET) based on a-Si:H is presented. The drain-source contacts are made on top of the n-layer of a glass/metal/p^+-i-n^- structure. The channel conductivity can be modulated by a reverse voltage applied to the junction, which varies the width of the depletion region. In amorphous based devices, however, the depletion of doped layers is hampered by the high defect density induced by the doping process. Based on the link between dopant concentration and defect density, presented in a previous work, we studied the depletion of the n-doped layer in a p-i-n amorphous silicon junction by using a one-dimensional finite element simulation program. We described the free electron concentration as a function of reverse applied bias, dopant concentration and thickness of the intrinsic layer. The n-channel conductivity has been obtained by integrating the free electron concentration along the drain-source direction. Pinch-off regime is achieved when the n-layer is fully depleted. The threshold voltage can then be defined. Based on simulation results we fabricated a JFET with W/L=200/40 μm and obtained transistors with threshold voltage around -3 Volt and transconductance values in the order of 10^{-5}A/V. These results represent a strong improvement respect to our previous report (MRS 2000) and make the device suitable for applications in linear circuit. In particular, unlike TFTs, JFETs do not require high-temperature, high-quality dielectric layers. As a result, the presented device is extremely attractive for process on plastic substrate.

8:30 AM *G1.3
POLY-SILICON TFTS ON PLASTIC SUBSTRATES.
Dharam Pal Gosain, Yokohama Research Center, Sony Corporation, Yokohama, JAPAN.

Electronics on a plastic substrate is attractive, because, of the lightweight, flexibility and robustness. In the long term it may also allow realization of a roll-to-roll fabrication process. To fabricate electronics on a plastic substrate, at a temperature compatible with the substrate thermal budget, which is much lower than glass, there are a number of challenges, one of which is the fabrication of poly-Si TFTs including crystallization of a-Si. The Short-pulse laser-crystallization technique has allowed the fabrication of poly-Si thin film transistor on a low temperature plastic substrate. The status of the poly-Si and a-Si:H TFTs on plastic substrates is reviewed. Our work on a-Si crystallization, characterization and thin-film transistor fabrication on a plastic substrate will be reported. It will be shown that TFTs with high mobility can be fabricated on a plastic substrate, hence electronics on a plastic substrate is possible.

9:00 AM G1.4
P-CHANNEL AND N-CHANNEL THIN FILM TRANSISTORS OF NANOCRYSTALLINE SILICON DEPOSITED AT 150°C.
I-Chun Cheng, Sigurd Wagner, Department of Electrical Engineering, Princeton University, Princeton, NJ; Sanghoon Bae, Alpha Industries, Sunnyvale, CA; Stephen J. Fonash, Nanofabrication Facility, Pennsylvania State University, University Park, PA.

CMOS capable thin film transistors that can be made on plastic foil are attracting great interest for fully-integrated, non-breakable, flexible, transparent and low cost large area electronics. We fabricated both p-channel and n-channel thin film transistors (TFTs) of nanocrystalline silicon (nc-Si:H) at a substrate temperature of 150°C on glass substrate. Our results suggest that CMOS capable transistor technology on plastic may be accessible through directly deposited silicon, in an approach that is compatible with present a-Si:H thin film technology. The TFTs are fabricated in a staggered top gate, bottom source/drain geometry. Both the intrinsic and the doped source/drain nc-Si:H layers are deposited at 80 MHz excitation frequency. Small amounts of dichlorosilane were added to the silane/hydrogen source gas for undoped nc-Si:H to obtain intrinsic conductivity of 10^{-6} to 10^{-7} S·cm^{-1}. A 230-nm intrinsic PECVD nc-Si:H seed layer is deposited first, followed by a 50-nm thick evaporated Cr bottom source/drain contacts, and a 50-nm thick PECVD p^+ or n^+ nc-Si:H layer. After patterning the contact layer to define the source/drain, the 50-nm thick intrinsic nc-Si:H channel layer is deposited. This channel layer is grown on top of the seed layer to promote the nucleation and structural evolution of nc-Si:H. Either 235-nm thick electron cyclotron resonance SiO_2 deposited at 140°C or 370-nm thick PECVD SiO_2 deposited at 150°C are the gate dielectrics. Contact holes are opened by wet chemical etching and 200-nm Al is thermally evaporated for contacts and then is patterned. The highest process temperature for n-channel TFTs is 150°C, while for p-channel TFTs all process temperatures are 150°C or less, except the p^+ layer deposition temperature, where we experimented with 150°C and 280°C for comparison. The n-channel TFTs reach an electron mobility μ_e of 12 cm^{2}V^{-1}s^{-1}, and the p-channel TFTs hole mobilities μ_h of 0.05 cm^{2}V^{-1}s^{-1} (150°C p^+) and 0.16 cm^{2}V^{-1}s^{-1} (280°C p^+). These mobilities suggest that directly deposited nc-Si:H is an attractive candidate for CMOS capable transistor electronics made on plastic substrates. We acknowledge support by DARPA and the Princeton Plasma Physics Lab.

9:15 AM G1.5
NANOCRYSTALLINE SILICON BY ECR FOR FET'S. Lihong Teng and Wayne A. Anderson, State University of New York at Buffalo, Department of Electrical Engineering, Amherst, NY.

In this work, the inverted staggered thin film transistors were fabricated on directly deposited hydrogenated nanocrystal silicon (nc-Si:H) and amorphous silicon (a-Si:H) from argon and silane (2% SiH_4 in He) gases by an electron cyclotron resonance microwave (2.45GHz) plasma chemical vapor deposition method. At the substrate temperature of 250°C and without H_2 dilution, the amorphous silicon films were obtained. At the substrate temperature of 400°C and with H_2 dilution, the nanocrystal silicon films were obtained. The microwave power used was 600W.The depositions were monitored by an in-situ residual gas analyzer (RGA). The total pressure during the deposition was kept below 70mTorr. The deposited Si films were analyzed by TEM and XRD. The nanocrystal size was ~50nm, which was obtained from TEM. Under these conditions, the dark and photo conductivities of the deposited Si films were 3.13×10^{-9} S/cm and 8.69×10^{-5} S/cm, respectively, for the a-Si:H case and 4.97×10^{-9} S/cm and 1.95×10^{-4} S/cm, respectively, for the nc-Si:H case. Thin film transistors with both nc-Si:H and a-Si:H as active layers were fabricated and characterized. For a typical nc-Si:H transistor, at V_{DS}=5V, the threshold voltage was 5.2V; the field effect mobility was 112 cm^2/Vs; the on-current was 3.9×10^{-5} A at V_{GS}=9V and the off-current was 1.6×10^{-11} A at V_{GS}=-1V. The ON/OFF current ratio was 2.4×10^6. The presentation will include the effect of H_2 dilution and the different gate designs on the TFT characteristics.

9:30 AM G1.6
LOW TEMPERATURE a-Si:H TFT FABRICATION PROCESS FOR PLASTIC SUBSTRATES: EFFECT OF MATERIAL PROPERTIES ON DEVICE PERFORMANCE. D. Stryahilev, A. Sazonov, P. Servati and A. Nathan, Department of Electrical and Computer Engineering, University of Waterloo, CANADA.

Amorphous silicon (a-Si:H) thin-film transistor (TFT) technology on glass substrates is widely used as backplane electronics technology for displays and imaging. Recently, polymer plastic substrates have

attracted much attention due to their mechanical flexibility and lightweight compared to traditional rigid glass counterparts. However, fabrication of TFTs on plastic must take into account the low glass transition temperature and high temperature expansion coefficient of a polymer substrate. Thus low temperature processing is required without compromising the properties of thin film materials and TFT performance. This paper reports the successful fabrication of a-Si:H TFTs at 120°C in which all semiconductor and insulator layers have been deposited in a standard parallel-plate 13.56 MHz PECVD equipment. We describe the structural and electrical properties of our thin film materials and analyze the effect of silicon nitride dielectric layers and contact processing on transistor performance. Tri-layer inverted staggered a-Si:H TFTs have been fabricated on glass and plastic substrates. The TFTs demonstrate field effect mobility of 0.85-1.0 cm^2/Vs and ON/OFF-ratio $\sim 10^7$. The fabrication process is evaluated in terms of intrinsic channel characteristics, source and drain series resistance, and leakage current behavior.

9:45 AM G1.7
LOW TEMPERATURE DEPOSITION AND POST-PROCESSING OF AMORPHOUS SILICON ON FLEXIBLE HIGH PERFORMANCE POLYMERS. Luigi Nicolais, Eugenio Amendola, Italian National Research Council, Institute of Composite Materials Technology, Napoli, ITALY; Dario Della Sala, Antonio Imparato, Carlo Privato, and Gaetano Contento, Italian Agency for New Technologies Energy and the Environment, Portici Research Center, Portici, ITALY.

Weight reduction and mechanical robustness are the main advantages expected from the replacement of glass with polymeric substrates. Thin film technologies on polymer substrates will benefit the rapidly growing market of portable, light-weight and cheap electronic appliances (new multimedia telephones, hand-held computer, digital cameras). Nowadays, high performance polymers are commercially available, featuring maximum processing temperature in the range of 200-250°C (even higher for specialty and niche polymeric materials). The development of semiconductor processing technology allows deposition of amorphous silicon films at temperatures consistent with polymeric materials that can be re-crystallized at low temperature. To prevent the complete thermal degradation of the polymer substrate, a short laser pulse is used, and inorganic coating should be deposited between semiconductor layer and polymeric substrate to prevent contamination and peeling-off of the film during the rapid melting event. We report about the deposition and laser crystallization of amorphous silicon film on polymeric substrates. Intrinsic amorphous films, of 1500 $\AA$ thickness, have been deposited on Polyetherimide (PEI), Polyethersulphone (PES) and Polycarbonate (PC) substrates by PECVD technique in the deposition temperature range of 120-200°C. Dehydrogenation and crystallization of thin films have been obtained by high energy (10 J) XeCl pulsed excimer laser with flat top homogenized beam of very large area (130 x 13 mm^2). The laser source and homogenization optics have been designed by ENEA. The irradiation conditions have been varied in order to study their influence on dehydrogenated and crystallized material properties. Electrical and optical properties of as-deposited and crystallized films have been determined. Structural characterization has been performed to evaluate average grain size and distribution. Preliminary data of crystallization realized at 270 mJ/cm^2 point out a distribution of grain size in the 200-600 $\AA$ range. Further investigation is under way in order to improve the excimer laser crystallization process by optimizing the homogenization optics.

10:30 AM G1.8
THIN FILM TRANSISTORS ON 3-D SHAPES: ELECTRICAL PERFORMANCE UNDER MECHANICAL STRAIN. P.I. Hsu, H. Gleskova, R. Bhattacharya, Z. Xi, Z. Suo, S. Wagner, J.C. Sturm, Center for Photonics and Optoelectronic Materials, Princeton University, Princeton, NJ.

There is a growing interest in the application of large area electronics on curved surfaces. Our approach towards realizing this goal is to fabricate amorphous silicon thin film transistor (TFTs) on a planar, thin plastic foil substrate, and then permanently deform the thin foil to a spherical dome subtending a 66° field-of-view (one steradian). The difficulty of such spherical deformation results from the fact that the substrate deformation introduces excessive force on the device structure and fractures inorganic semiconductor materials and metal interconnects. Furthermore, the dependence of carrier transport properties of amorphous silicon on strain is not well known. Previous work has shown that by patterning uniform amorphous silicon and silicon nitride layers into isolated islands on "soft" plastic substrates, amorphous TFTs can be made to withstand the deformation without fracture as we expand the substrate to a spherical dome, whose average tensile strain in the substrate exceeds 5% [1]. In this work, we report the relationship between the mechanical residual strain in the TFT islands and the device electrical characteristics after deformation. The strain in the device islands after deformation is a function of the island geometry and substrate material properties. Though the substrate is plastically expanded to a spherical dome, device islands can experience either tension or compression depending on the deformation conditions. Our preliminary results show that the electron mobility might increase or decrease by up to 10% after deformation. We will present both modeling and experimental methods to demonstrate how the spherical deformation affects the device performance. The results of interconnecting devices into circuits will also be discussed. [1] P.I. Hsu, H. Gleskova, Z. Suo, S. Wagner, and J.C. Sturm, "Amorphous Si TFTs on plastically-deformed substrates with 3-D shapes," Proc. of the 59th Device Research Conference, June 2001.

10:45 AM G1.9
CADMIUM SULFIDE THIN FILM TRANSISTORS FABRICATED BY LOW TEMPERATURE CHEMICAL BATH DEPOSITION. Curtis Voss, Hewlett-Packard Co., Corvallis, OR; Chih-hung Chang, Oregon State University, Dept of Chemical Engineering, Corvallis, OR; Mani Subramanian, Oregon State University, Electrical and Computer Engineering, Corvallis, OR.

The digital revolution has brought information to every corner of our daily life. Inexpensive and flexible integrated circuits are needed for this continuing revolution. Silicon technology, the current workhorse of microelectronic industry, is far from inexpensive and flexible. Researchers are taking several different routes to achieve this goal. Amorphous silicon is the current material of choice for low cost thin film transistors (TFT). They are relatively cheap compared to their single crystal silicon cousin. Organic (molecular crystals or polymeric semiconductors) electronics with the advantages of flexibility and compatibility with low cost plastic substrates are the other major candidate. Another promising alternative is to fabricate compound semiconductor devices by low temperature (plastic compatible) processing technology. In this work, a solution based low temperature processing method known as Chemical Bath Deposition (CBD) was explored to fabricate thin film transistors. CBD is an aqueous analog of Chemical Vapor Deposition (CVD). The constituent ions are dissolved in a water solution, and the thin films are produced through a heterogeneous surface reaction at low temperature ($\sim$80°C. It is known that CBD is capable of producing an epitaxial layer (e.g., CdS) on single crystal surface. In this paper, we report the first working TFT using a CBD deposited CdS semiconductor layer. A $\sim$1000 $\AA$ thick CBD CdS film was deposited on thermally grown SiO_2 at the surface of a heavily antimony doped (n+) silicon wafer. Twenty and forty micron transistors were fabricated by conventional photolithography using Al deposited on CdS as source and drain contacts. Thus, the device is essentially an inverted gate thin film MOS transistor with n+ Si wafer serving as the gate. It has clearly demonstrated transistor action as shown from the I-V measurements. More importantly, the device characterization data and modeling shows that the CdS film is n-type with a doping concentration of $\sim 10^{17}$ cm^{-3} and an effective carrier mobility of $\sim$2 cm^2/Vxs. This performance is comparable to most amorphous Si (0.1 to 1 cm^2/Vxs) and better than a typical organic thin film transistor (10^{-2} cm^2/Vxs). The interface state distribution at the CdS-SiO_2 interface was also determined by C-V measurements. We are currently working on extending this process to fabricate a MESFET on a plastic substrate.

11:00 AM G1.10
LOW TEMPERATURE DEPOSITION OF ZIRCONIUM AND HAFNIUM SILICATE GATE DIELECTRICS FOR FLEXIBLE DISPLAY APPLICATIONS. P. Punchaipetch, G. Pant, M.A. Quevedo-Lopez, M. El Bouanani, H. Zhang, R.M. Wallace and B. Gnade, Dept of Materials Science, University of North Texas, Denton, TX.

Hafnium and zirconium silicate are being studied as potential candidate materials to replace SiO_2 as the gate dielectric in scaled silicon transistors due to their relatively high dielectric constant and high thermal stability [1]-[2]. In this work, we examine the properties of hafnium and zirconium silicate films produced under low temperature processing conditions for the fabrication of transistors on plastics substrates. The low glass transition temperature of most plastic substrates limits the device processing temperature to <150°C. Zirconium and hafnium silicate films were prepared by reactive sputtering of zirconium silicide ($ZrSi_2$) and hafnium silicide ($HfSi_2$) targets at room temperature with Ar/O_2 sputter gas mixtures. Rutherford backscattering spectrometry (RBS) and X-ray photoelectron spectroscopy (XPS) are used to determine the composition and chemical bonding of the film. Capacitors using shadow mask deposited top Pt electrodes are used to examine the electrical behavior of the as-deposited and annealed silicate films. We will present results on the effect of several processing parameters, including; 1) the effect of varying the sputter gas mixture, 2) the effect of surface preparation for hydrogen-terminated silicon vs. a UV-ozone oxidized surface, and 3) the effect of post-annealing at low temperature using N_2, O_2, N_2O, NO, NH_3, and forming gas. This

work is supported partially by the US Army Soldier Systems Command (Contract #DAAD16-00-C-9273) and the Texas Advanced Technology Program. [1] G.D. Wilk, R.M. Wallace, and J.M. Anthony, J. Appl. Phys. 87 (2000) 484. [2] G.D. Wilk, R.M. Wallace, Appl. Phys. Lett. 74 (1999) 2854.

11:15 AM G1.11
PECVD DEPOSITION OF HIGHLY CONDUCTIVE MICRO-CRYSTALLINE SILICON THIN FILMS UNDER 120°C ON POLYMERIC SUBSTRATE. A.M. Nardes[a], E.A.T. Dirani[a,b], J.A.R. Neves[a], J.P.H. Lima[a,d], R. Muccillo[c], E.N.S. Muccillo[c], A.M. de Andrade[a] and F.J. Fonseca[a]; [a]LME, Dept. Eng. Sist. Eletr., Escola Politecnica da USP, Sao Paulo, SP, BRAZIL; [b]Dept. de Eng Eletr. - PUCSP, Sao Paulo, SP, BRAZIL; [c]CMDMC, CCTM, IPEN, Sao Paulo, SP, BRAZIL; [d]EEM, CEUN - Inst. Mau de Tecnologia, Sao Caetano do Sul, SP, BRAZIL.

In this paper we present the results on doped n-type hydrogenated microcrystalline silicon (μc-Si:H) films deposited in a conventional plasma enhanced chemical vapor deposition (PECVD) in the temperature range of 70 to 120°C on low cost polymeric substrates. The interest of these films arise from the fact that they combine the high optical absorption of amorphous silicon and the electronic behavior of the crystalline silicon, making them interesting for the production of large electronic devices such as solar cells, image sensors and thin film transistors. It is well known that thin films obtained at low temperatures presents poor electronic characteristics when compared to thin films deposited at temperatures above 200°C. Nevertheless, for new applications such as devices produced on substrates susceptible to be damaged when overheated (PET-Poly Ethylene Teraphtalate and other polymers) the temperature parameter is of crucial importance. We show that highly conductive n-type μc-Si:H can also be obtained even at low temperature deposition, under 120°C (σ = 2.9 S/cm). The structural properties of the films have been studied by Raman and Infrared spectroscopy that allowed to calculate the crystalline fraction and hydrogen contents, respectively. Electrical measurements were performed by AC Impedance Spectroscopy, Hall Effect and Dark Conductivity. The impedance plots in the form of half circles indicates that the films can be modeled as a parallel RC circuit, each one linked to one phase of the material. Good electrical features were obtained in this deposition set-up; sample deposited on kapton at 90°C (σ = 0.03 S/cm, μ = 1,56 cm^2/V Hall measurements) shows the possibility to develop polymer substrate based devices. Some conclusions regarding to the correlation between the electrical and structural properties are presented for the considered temperature range.

11:30 AM G1.12
ELECTRODEPOSITION OF COMPOSITE THIN FILMS OF METAL AND LUMINESCENT Si NANOPARTICLES. A. Smith, G. Belomoin, M.H. Nayfeh, Univ of Illinois, Dept of Physics, Urbana, IL; T. Nayfeh, Cleveland State Univ, Industrial Engineering, Cleveland, OH.

We report on a procedure for deposition of a composite thin film of metal and ultrasmall ultrabright Si nanoparticles using an electrochemical plating process. A tank of an aqueous alcohol solution, in which the particles and metal (Al, Ni) salts are dissolved, operates at a current flow between the two electrodes. As in metal plating, metal-Si particle plating occurs at the cathode. Thin film composites on metal, silicon substrates, foils, or conducting polymer films are tested. Auger material analysis confirms that the film is a composite of particles and metal, and optical spectroscopy shows that the film is still highly luminescent. The process is discussed in terms of the formation of complex metal ions with the silicon particles tagging along. These results have implications to flexible particle-based displays.

11:45 AM G1.13
ROLE OF THE LAYER COMPOSITION AND THICKNESS ON THE OPTOELECTRONIC PROPERTIES OF p-i-n AND p-i-n-p-i-n a-SiC:H HETEROJUNCTIONS. P. Louro, Yu. Vygranenko, M. Fernandes, R. Schwarz, M. Vieira, Electronics Telecommunications and Computer Dept, ISEL, Lisbon, PORTUGAL.

The aim of this work is to describe the results of experiments and to discuss the usefulness of a-Si alloy materials in the improvement of large area (4×4 cm^2) single (ZnO:Al/p (SiC:H)/i (Si:H)/n (SiC:H)) and stacked (ZnO:Al/p (SiC:H)/i (Si:H)/n (SiC:H)/ p (SiC:H)/i (SiC:H)/n (SiC:H)) image and colour transducers. It concerns the structural, electrical and optical characterisation of the a-$Si_{1-x}C_x$:H films deposited by PECVD at low temperature (100°C) needed to use flexible substrates. The efforts are focused mainly on doped n- and p-type layers at high and low doping levels with and without carbon, as well as in the intrinsic layer thickness and composition. Junction properties, carrier transport and photogeneration are investigated from dark and illuminated current-voltage characteristics. The collection efficiency is evaluated from spectral response measurements under different applied bias voltages. A systematic research on the optoelectronic properties of the layers and related devices under dark and different light illumination conditions was performed to understand its role on the output performance of the a-SiC:H based transducers. Transport and optical modelling give insight into the internal physical process. Results show that the photocurrent collection depends on the illumination conditions and applied voltage. The transport mechanism under low-level illumination is based mainly on field-aided drift while under strong illumination it will depend mainly on the diffusion of minority carriers. The turning point in the conduction mechanism depends on the flat band voltage, which in the single junctions is highly influenced by the composition of the doped layers and in the stacked ones by the i-layer thickness and composition. When high resistivity and wide band gap doped layers are used the biasing light level controls the transport mechanism. This is the basis for using these devices as optical transducers.

SESSION G2: FLEXIBLE ELECTRONIC DEVICES AND COMPONENTS II
Chair: Thomas N. Jackson
Tuesday Afternoon, April 2, 2002
Golden Gate C1 (Marriott)

1:30 PM *G2.1
SURFACE FREE TECHNOLOGY BY LASER ABLATION/ ANNEALING (SUFTLA) AND ITS APPLICATIONS FOR FLEXIBLE ELECTRONIC DISPLAYS AND DEVICES. Satoshi Inoue, Sumio Utsunomiya, Takayuki Saeki and Tatsuya Shimoda, Seiko Epson Corporation, Technology Platform Research Center, Nagano, JAPAN.

A new technology, which enables the transfer of thin film devices from an original substrate to another substrate using laser irradiation, has been developed in order to realize flexible displays and devices. This technology has been termed SUFTLA, which stands for surface free technology by laser annealing / ablation. We attempted to transfer low-temperature polycrystalline-silicon thin film transistor liquid crystal displays (poly-Si TFT-LCDs) onto plastic films. The display area of the TFT-LCDs is 0.7-inch diagonal and the number of pixels is 428 x 238. Four x-drivers and two y-drivers are integrated into the panels. Each data driver consists of a 107-stage static shift register, and clock frequency is 1.3MHz. Each y-driver consists of a 119-stage static shift register and 238-NAND gates, and clock frequency is 4.0kHz. In the SUFTLA TFT-LCD fabrication process, an a-Si film is deposited as an exfoliation layer on a conventional glass substrate (original substrate), and a low temperature poly-Si TFT array with integrated drivers is fabricated onto it. Next, the substrate is glued onto another glass substrate (the first transfer substrate) using a water-soluble adhesive, and a XeCl excimer laser is irradiated from the rear of the original substrate. At this stage, hydrogen from the exfoliation layer evolves and causes the detachment of TFTs from the original substrate. Then, the first transfer substrate, on which the TFTs are transferred, is glued onto a plastic film using non-water-soluble adhesive. The first transfer substrate with plastic film is cut, and soaked in water. When the water-soluble adhesive dissolves in water, the TFTs can be transferred onto the plastic substrate. Finally, the LCD module was assembled using a standard LCD assembly process. As a result, we were able to transfer SUFTLA TFT-LCDs onto plastic films, becoming the first in the world to see display images using this technology.

2:00 PM *G2.2
TOWARDS A LOW-COST RADIO FREQUENCY IDENTIFICATION TECHNOLOGY. Hagen Klauk, Infineon Technologies, Polymer Materials & Technology, Erlangen, GERMANY.

One of the first commercial applications for flexible organic electronics will be in low-cost radio frequency identification (RFID) systems. These are wireless interrogation systems designed for non-contact, non-line-of-sight reading and consequently are effective in many environments unsuitable for barcode labels and optical readout techniques. Today's conventional RFID systems rely on transponders (RFID tags) that are built around silicon-based microchips and are typically encapsulated in plastic or ceramic packages. Over the past 20 years, RFID has established itself in a wide range of markets, including manufacturing, transportation, security, inventory control, and livestock identification, where a need for automatic tracking of moving or stationary objects exists. By far the largest market projected for RFID is as a replacement for barcode labels in retail stores - a market that is expected to total more than 10 billion units per day. By replacing barcode labels, RFID systems will eliminate the need for laser scanners and conventional check-out registers, and provide additional features such as Electronic Article Surveillance

(EAS) and automatic inventory control at little or no extra cost. Because RFID systems will make retail operations more efficient and more convenient, the cost of outfitting every retail item with a transponder does not necessarily have to be as low as the cost of applying barcode labels; a somewhat higher cost per RFID tag will likely be acceptable. Nevertheless, the projected minimum cost for silicon-based transponders is still about an order of magnitude too high for retail tagging. Flexible organic thin film electronics, on the other hand, especially when combined with large-scale roll-to-roll processing, inexpensive printing lithography, novel materials, and innovative device and circuit concepts, may provide a much cheaper and more easily scalable route to fabricating billions of transponders per day, particularly passive transponders, where circuit complexity and dynamic performance requirements are comparatively low.

2:30 PM *G2.3
FLEXIBLE ELECTRONIC DEVICES AND DISPLAYS.
Roger Stewart, Alien Technology Corporation, Morgan Hill, CA.

Flexible display media have been available for more than 30 years but have so far failed to trigger any significant development of flexible displays. This is because fabricating practical flexible electronic devices requires much more than just developing flexible electro-optic display materials. Widespread use of flexible devices and displays also requires that the cost be reduced; that power dissipation be dramatically reduced; and that the ubiquitous interface electronics system servicing these devices be made much more compact and flexible. These three factors will govern the future success or failure of flexible devices and displays. Although in many applications the continuing integrated circuit revolution has reduced cost to the point where we can almost ignore it, displays and RFID devices haven't fully benefited from "Moore's Law" due to packaging limitations. While transistor costs have been reduced by a ratio of almost 100:1 over the past 10 years, the cost of a minimum-priced packaged IC has hardly been reduced at all and still hasn't broken through the 10-cent barrier. The cost of current display systems are limited more by their pin count than by their transistor count, and these costs aren't being reduced fast enough to open up large markets for portable displays. Also, flexible display applications require them to be either portable, large, or both. Even if they could be made flexible, the 100-800 mW/in2 power dissipation of existing CRT, plasma, or backlit AMLCD displays is many times higher than acceptable in any practical flexible display system. Beam-powered RFID devices often have to operate on a power budget of only 1 microamp. This paper will describe a new approach to building flexible devices and displays based on ultra-miniaturized NanoBlock IC electronics that are used to reduce cost, power dissipation, and bulk.

3:30 PM G2.4
GROWTH OF ITO FILMS ON POLYMERIC SUBSTRATES FOR ELECTRONIC APPLICATIONS. R. Scott McLean, Peter F. Carcia, Michael H. Reilly and Zhigang Li, Dupont Co., Central Research Department, Wilmington, DE; Lawrence Pillione and Russell F. Messier, Pennsylvania State University, University Park, PA.

Transparent conductive coatings are an integral part of device structure for a number of electronic applications. Currently, low resistance transparent coatings are commercially available on glass substrates. If, however, electronic devices could be made on flexible polymeric substrates in a reel-to-reel process, this would reduce cost, improve ruggedness, and reduce weight. However, to achieve success on plastic substrates, low resistance transparent coatings are needed for efficient electro-optical performance. Polymeric substrates present certain challenges such as considerably lower working temperature and rougher surfaces as compared to glass substrates. Important properties needed for processing transparent conductive coatings on plastic are, low resistivity, low film stress, a smooth microstructure and a low temperature process. In this paper we investigate the relationship of the polymeric substrate and its surface morphology to the properties and structure of inorganic thin films, as examined by atomic force microscopy. Conducting ITO films were grown by rf magnetron sputtering. ITO films, as deposited on unheated PET and PEN substrates, with sheet resistance of only ~15 ohms/square, have a very small microstructure and are considerably smoother than commercially available ITO on polymeric substrates. These films were relatively thin (120-180 nm thick) with low stress and high optical transparency in the visible, and they were also good barriers to oxygen transport. In addition electrical properties of these films will be discussed.

3:45 PM G2.5
DEPOSITION OF ZnO FILMS BY USING AN ATMOSPHERIC PRESSURE COLD PLASMA GENERATOR. Yoshifumi Suzaki, Seiki Ejima, Kagawa Univ, Department of Advanced Materials Science, Takamatsu, JAPAN; Tomokazu Shikama, Takamatsu National College of Technology, Department of Electrical and Computer Science Engineering, Takamatsu, JAPAN; Osamu Tanaka, Takahiro Kajitani, Okura Ind. Co. Ltd., Research Laboratory, Marugame, JAPAN; Hideomi Koinuma, Tokyo Institute of Technology, Frontier Collaborative Research Center, Yokohama, JAPAN.

Transparent electrical conductive zinc oxide (ZnO) films have generated much attention as low-cost transparent electrodes for solar cells. ZnO films are usually prepared by methods such as MOCVD, CVD and SP. Most of these however require sophisticated and costly apparatus making it unsuitable for large area production. Recently, the homogeneous nonequilibrium plasma was generated by an rf excitation of flowing He gas at 1 atm. Under normal atmospheric pressure, arc discharge is the most commonly observed phenomenon. However, the plasma generator we developed using Al as the cathode has a thin coating of alumina resulting from a process using natural oxidation that enables glow discharge to occur instead of arc discharge. Using this cold plasma, ZnO films were prepared. The plasma generator composed of Al orthorhombic cathode and Al plate anode. A slit (5 mm × 20 mm) was drilled into the cathode (about 30 mm × 50 mm) for purpose of introducing He gas into the gap between cathode and anode. Also the anode moves with a glass substrate in a perpendicular direction to the slit, in order to get flat films. Plasma was generated by flowing He plasma gas (1800 sccm) and He carrier gas (200 sccm) through the inner space of the cathode down to the gap, where it was excited by a 50 - 110 W radio frequency. Bis-dipivaloylmethanato Zinc (DPM_2Zn) was vaporized and carried by the He flow for introduction into the plasma generated at the gap. Transparent flat films (about 150 nm thick) were successfully deposited directly under the slit made into the cathode. The transmittance of the films was more than 80%. X-ray diffraction measurement revealed that ZnO films had polycrystalline structure. By mixing O_2 gas into He, grain size of the ZnO crystalline became larger.

4:00 PM G2.6
TRANSPORT PROPERTIES OF INDIUM TIN OXIDE CONDUCTIVE FILMS DEPOSITED ONTO ANISOTROPIC FLEXIBLE TRANSPARENT CELLULOSIC SUBSTRATES.
A. Amaral, C. Nunes de Carvalho, Centro de Fisica Molecular, IST/UTL, Lisboa, PORTUGAL; P. Brogueira, L.V. Melo, Dep. Fisica, IST/UTL, Lisboa, PORTUGAL; G. Lavareda, M.H. Godinho, Dep. Ciencia dos Materiais, FCT/UNL, Monte de Caparica, PORTUGAL.

Hydroxypropylcellulose (HPC) systems have been actively investigated as flexible transparent substrates for use in LCD technology. HPC solid films (20-60 micron), obtained from aqueous liquid crystalline solutions, present tunable topography. The need for transparent back contact in working electronic devices leads to the study of the properties of indium tin oxide (ITO) deposited on this flexible substrates. Substrates obtained from a 30% w/w solution of HPC in water were found to be isotropic with a roughness (Ra) of 18.4 micron as measured by atomic force microscopy (AFM). Anisotropic substrates were obtained from a 65% w/w HPC solution. AFM measurements show a Ra = 29.1 micron. Two kinds of peridiocities can be observed in the anisotropic substrates. A primary set of large bands, perpendicular to the shear direction is characterized by a periodicity of 1.8-2.1 micron and an average peak-to-valley height of 74-87 nm. This first set of bands lies under a secondary set of smoother band texture with a periodicity of 0.35-0.40 micron and an average peak-to-valley height of 2.9-4.4 micron. Transport properties of ITO deposited on isotropic substrates show a resistivity around 0.1 ohm.cm independent of orientation. ITO films deposited on to the anisotropic substrate shows a resistivity which depends strongly on the current direction by more than one order of magnitude. The resistivity measured along the shearing direction is 0.1 ohm.cm and along a perpendicular direction is 1.9 ohm.cm. In order to understand the origin of the observed effect we study different anisotropic substrates by means of AFM, polarizing optical microscopy (POM) and optoelectronic measurements. The results obtained will be discussed and compared with those reported in literature.

SESSION G3/P5: JOINT SESSION
ORGANIC DISPLAYS AND DEVICES
Chairs: Sue Anne Carter and Paul S. Drzaic
Wednesday Morning, April 3, 2002
Franciscan II/III (Argent)

8:00 AM *G3.1/P5.1
HYDROSTATIC PRESSURE DEPENDENCE OF THE ELECTRICAL PROPERTIES OF PENTACENE AND TETRACENE.
Zhenlin Rang, P. Paul Ruden, and Marshall I. Nathan, University of Minnesota, Department of Electrical and Computer Engineering, Minneapolis, MN; Reid J. Chesterfield and C. Daniel Frisbie, University of Minnesota, Department of Chemical Engineering and Materials Science, Minneapolis, MN; Paul F. Baude and Dawn Muyres, 3M Company, St. Paul, MN.

Pentacene and tetracene exhibit unusually high mobilities for organic semiconductors. However, the transport mechanisms that give rise to these mobilities is not understood. Moreover, the achievable values of the mobilities are not known. Therefore, a study of mobility as a function of molecular separation or pressure appears to be useful. Pentacene and tetracene show readily observable photoconductivity when illuminated with light in the blue part of the visible spectrum. We measured the change of photoconductivity with hydrostatic pressure in single crystal samples of both materials. Possible mechanisms for the observed increase in photoconductivity with pressure are discussed. We conclude that a carrier mobility increase under pressure is most likely to cause the increase in photo-conductivity in the case of pentacene. For tetracene, changes in the absorption spectrum in the range of the excitation wavelengths may also be significant. We observe a phase transition near 0.3GPa in tetracene, in agreement with previous results. We have also studied the effect of pressure on the electrical characteristics of organic (pentacene) field effect transistors (OFETs). From the OFET measurements we obtain field effect mobility. The results from the photoconductivity measurements and the OFET measurements will be compared.

8:30 AM G3.2/P5.2
PENTACENE THIN FILM TRANSISTORS AND CIRCUITS: INFLUENCE OF PROCESSING AND DEVICE DESIGN.
Dietmar Knipp, Robert A. Street, Brent Krusor, Jackson Ho, Xerox Palo Alto Research Center, Palo Alto, CA.

The electronic transport of thermal evaporated pentacene TFTs and circuits on neutral substrates will be presented. Since organic TFTs fabricated on thermal oxide are not of particular interest for large area and/or low cost applications, alternative dielectrics and processing methods consistent with thin film technology have been investigated. The influence of the dielectrics on the structural and electronic properties of pentacene films and TFTs will be discussed. For all applied dielectrics, we observed a strong correlation between morphology and structural properties of the pentacene films and the mobility of the TFTs. In the case of inorganic dielectrics like plasma enhanced chemical vapor deposited (PECVD) silicon nitride and silicon oxide the growth of pentacene is mainly determined by the roughness of the dielectric. The roughness inhibits the ordering of pentacene molecules on the surface. However, by optimizing the fabrication process of the dielectrics, we have achieved similar pentacene mobilities on PECVD dielectrics and thermal oxide (0.4 cm^2/Vs), without employing self-assembled monolayers like octadecyltrichlorosilane (OTS). With an OTS treatment of oxide based dielectrics the mobility increases by a factor of 2-3 up to $>1cm^2/Vs$ for thermal oxide. Despite the high mobility for inorganic dielectrics, organic dielectrics are more attractive because the dielectric can be spin coated or inkjet printed. We have studied the growth of pentacene on poly-vinyl phenol (PVP) and bisbenzo-cyclobutene (BCB). The films on organic dielectrics are highly ordered, which is confirmed by structural and transport measurements. For pentacene films on inorganic and organic dielectrics we find similar mobilities of 0.3-0.5cm^2/Vs and high on/off ratios between 10^6 and 10^8. Different device designs will be discussed towards all-organic circuits on flexible substrates.

8:45 AM *G3.3/P5.3
POLYMER LED DISPLAYS BUILT ON PLASTIC SUBSTRATES.
Marie O'Regan, Mark Sellars, Blanca Lopez, Michel Dubeau, Naparat Juanko, Ralph Martinez and Alan Heeger, UNIAX Corporation, Santa Barbara, CA.

Emissive displays built on plastic substrates provide some major advantages to the display industry over glass-based displays, specifically in terms of weight, ruggedness, profile and form factor. Polymer LED (PLED)displays are being developed at UNIAX/ DuPont; we have successfully built and demonstrated prototype displays on plastic substrates. Progress in the development of flexible PLED displays will be summarized. This talk will focus on some of the remaining challenges, including barrier properties and substrate patterning.

9:15 AM G3.4/P5.4
A NOVEL APPROACH FOR ADDRESSING PRINTED, ALL-POLYMER ELECTROCHROMIC DISPLAY CELLS.
Thomas Kugler, Linkoping University, Dept. of Science and Technology, and Acreo AB, Norrkoping, SWEDEN; Tommi Remonen, Anna Malmstrom, Jessica Hall, Bjorn Knuthammar, Lars-Olov Hennerdal, Acreo AB, Norrkoping, SWEDEN; Magnus Berggren, Linkoping University, Dept. of Science and Technology, and Acreo AB, Norrkoping, SWEDEN.

We report on a completely novel approach for addressing the electrochemically active elements in conducting polymer-based devices. The principle is illustrated with our latest results on printed, all-polymer electrochromic displays realized on flexible substrates such as paper or plastic foil. The displays are based on lateral patterns of poly(3,4-ethylenedioxythiophene) (PEDOT) doped with poly(styrene sulfonic acid) (PSS), which is used both as conducting and electrochromic material. The key feature in our displays is the fact that the electrochromic material is not in direct contact with a conducting electrode. Instead, at least two, remote electrodes are used to apply an electric field across a slab of electrolyte interfacing an electrochromic element consisting of PEDOT-PSS. Based on the fact that PEDOT-PSS is conducting in the oxidized, optically transparent state, the presence of the electric field results in a polarization of the electrochromic element and the onset of electrochemistry: the edge adjacent to the (remote) cathode is oxidized further, whereas the edge adjacent to the (remote) anode is reduced to deep blue, neutral PEDOT. The concomitant reduction in conductivity results in a deep blue coloration front advancing from the negatively polarized edge towards the center of the electrochromic element. By modifying the ionic conductivity within the electrolyte along the electrochromic element, both dynamic and bi-stable switching can be realized. The displays operate at low voltages in the range 1-5 V, depending on geometrical parameters and the ionic conductivity of the electrolyte. Both gelled water-based and solid electrolytes have been tested. We will present different basic device architectures for realizing printed electrochromic display cells together with the factors determining the switching speed, coloration intensity, and lifetime of these devices.

9:30 AM G3.5/P5.5
POLYMER LIGHT-EMITTING DIODE DISPLAYS DRIVEN BY INTEGRATED NANOBLOCK IC DRIVERS.
Jan Bernkopf, Yijian Shi, Diane Choquette, Alien Technology Corporation, Morgan Hill, CA.

Polymer light-emitting diode (PLED) displays can be operated in either passive matrix or active matrix mode. Passively-addressed displays, while suitable for many applications, are limited in pixel count and in size. Active matrix displays can achieve higher pixel densities, but require high quality and expensive polysilicon circuitry. Here, we describe an alternative addressing approach for PLEDs, using high quality, inexpensive CMOS circuitry. The single crystal silicon circuitry is built onto a wafer using standard CMOS foundries, and then converted to numerous small, square (360 microns on one side) NanoBlock ICs. These NanoBlock ICs are assembled onto glass sheets using Alien Technology Fluidic Self Assembly process. In this approach, the tiny NanoBlock IC drivers are uniformly distributed (and embedded) into the display backplane. Each driver is driving the nearest eight pixels locally (each pixel receives a maximun of 180 μA of current). In this paper, we will demonstrate the successful synergy of NanoBlock IC/FSA process with light emitting polymers as basis for high-performance emissive displays. Material compatibility between the NanoBlock IC process and the PLED fabrication process is demonstrated. NanoBlock ICs can be deployed into many types of substrates, including plastic, showing a path for high quality silicon to drive future PLED displays on plastic.

10:15 AM *G3.6/P5.6
ORGANIC BISTABLE DEVICE AND MEMORY CELLS.
Liping Ma, Jerry Liu, Seungmoon Pyo, Faye Xu, Yang Yang, Univ of California-Los Angeles, Los Angeles, CA.

Electrical bistability is a phenomenon in which a device exhibits two states of different conductivities, at the same applied voltage. In this presentation, we report a novel organic electrical bistable device (OBD) comprising of a thin metal layer embedded within the organic material, as the active medium. The performance of this new device makes it attractive for memory cell type of applications. The two states of the OBD differ in their conductivity by about 107 and show remarkable stability, i.e. once the device reaches either state, it tends to remain in that state for a prolonged period of time. More importantly, the high and low conductivity states of an OBD can be precisely controlled by the application of a positive voltage pulse (to write) or a negative voltage pulse (to erase), respectively. One million writing-erasing cycles for the OBD have been achieved in ambient conditions without significant device degradation. These discoveries pave the way for newer applications, such as low-cost, large-area, flexible, high-density, electrically addressable data storage devices.

10:45 AM *G3.7/P5.7
PLASTIC ORGANIC LIGHT EMITTING DISPLAYS.
P.E. Burrows, W.D. Bennett, C.C. Bonham, G.L. Graff, M.E. Gross, M.G. Hall, E.S. Mast, P.M. Martin, D.W. Matson and M.R. Zumhoff, Pacific Northwest National Laboratory, Richland, WA; M.S. Weaver, J.A. Silvernail, A.B. Chwang, R.H. Hewitt, S.Y. Mao, L.A. Michalski, T. Ngo, M.R. Nugent, K. Rajan, M.A. Rothman, and J.J. Brown, Universal Display Corporation, Ewing, NJ.

Rapid degradation of organic light emitting devices (OLEDs) is observed in the presence of even low concentrations of moisture. In most conventional OLED displays described to date, this problem is addressed by encapsulating devices grown on glass or silicon using a glass or metal lid sealed to the substrate by means of an adhesive, typically a UV-curable epoxy product. Desiccant is often added to the package to absorb both residual moisture from the fabrication process and moisture diffusing through the epoxy seal. Pixels with > 10,000 hours of operating lifetime at video brightness have thereby been demonstrated. If we are to utilize the advantages of plastic substrates, however, this type of encapsulation approach is flawed due to the high moisture permeability of the substrate itself. In this paper, we describe a process to deposit transparent, flexible, organic-inorganic multilayer thin film barriers onto commercially available polymers by a hybrid process of cryo-condensation and polymerization of an organic precursor from a flash evaporation source followed by vapor deposition of a nanoscale barrier layer. The multilayer hybrid barrier restricts moisture and oxygen permeation rates to levels not measurable by conventional technology while retaining a high degree of flexibility and transparency. Residual permeation is dominated by pinholes rather than bulk diffusion, rendering large area permeation measurement techniques such as MOCON difficult to interpret. We will present further results of work to quantify a spatially resolved permeability of ultrabarrier plastic substrates by observing the degradation of thin films of reactive metals. Furthermore, we will present operating lifetime results from various high efficiency electrophosphorescent small molecule OLEDs grown on moisture barrier substrates and show that better than 3,000 hours of operation is achievable at display brightnesses. Based on our results, we project that video-brightness plastic displays with better than 10,000 hours of operating lifetime are achievable.

11:15 AM G3.8/P5.8
POLYMER LIGHT EMITTING DISPLAYS AND PHOTOVOLTAICS ON FLEXIBLE SUBSTRATES. H. Tillmann, H.-H. Hoerhold, University of Jena, Institute for Organic and Macromolecular Chemistry, Jena, GERMANY; S. Tuttle, Add-Vision Inc., Scotts Valley, CA; M.A. Kreger, T. Omabegho, S.A. Carter, University of California Santa Cruz, Dept of Physics, Santa Cruz, CA.

Polymer light-emitting diodes, light-emitting electrochemical cells and photovoltaics on flexible substrates have been fabricated and their electrical and optical properties have been characterized. Various device structures are discussed with reference to cost effective construction, optimum performance and display stability. Electrical properties and electroluminescence spectra have been measured for poly phenylene vinylene (PPV) and polyfluorene (PF)-based materials on several different flexible substrates, including PET and flexible glass, and compared with similar devices on thick glass. Stability of polymer light emitting devices has been monitored in both a dry nitrogen atmosphere and on encapsulated devices in air atmosphere. Aging-dependent Current-Voltage-Radiance measurements, complimented by atomic force and fluorescent microscopy images, allow us to determine the primary device degradation mechanisms, which may include electrode delamination, irreversable chemical reactions, air/water migration at impurities and defects, and polymer chain breakage. We also will present our work on the performance of photovoltaics consisting of conjugated PPV-based polymers cast on TiOx sol gel and nanoparticle layers on flexible substrates. The stability of the polymer layer to photobleaching under solar condition and the effect of the TiOx morphology on polymer stability and performance will also be addressed. We will conclude by discussing the optimization of polymer-based optoelectronic devices for manufacturing inexpensive printable large-area displays and detectors on flexible substrates.

11:30 AM *G3.9/P5.9
CHARGE INJECTION AT THE METAL-ORGANIC INTERFACE. J. Campbell Scott, Luisa. D. Bozano and Amelia R. Span, IBM Almaden Research Center, San Jose, CA.

The performance of virtually every type of organic electronic device depends on the efficiency of charge injection from metallic electrodes into the semiconducting organic material. In the cases where there is no chemical reaction between the metal and the organic, it has been shown that the injected current is proportional to charge carrier mobility in the organic layer, with a field dependence that is dominated by Schottky barrier lowering. The net injected current can be described theoretically as the difference between the injection current (metal to semiconductor) and the surface recombination current (semiconductor to metal). The charge density on the interface layer of organic molecules is given by a thermal occupation probability, provided that the net current flow is low compared to the surface recombination term. We describe additional experimental tests of this description using chemical modification of the metal surface to alter the nature of the interface states.

SESSION G4/P6: JOINT SESSION
ORGANIC TRANSISTORS
Chairs: Paul S. Drzaic and Sue Anne Carter
Wednesday Afternoon, April 3, 2002
Franciscan II/III (Argent)

1:30 PM *G4.1/P6.1
DIRECT PRINTING OF POLYMER TRANSISTOR CIRCUITS. Henning Sirringhaus, University of Cambridge, Cavendish Laboratory, Cambridge, UNITED KINGDOM.

Polymer transistor circuits offer new opportunities for the controlled manufacturing of active electronic circuits by a combination of solution processing and direct printing. Control over the morphology of the polymer semiconductor is obtained by making use of self-organisation mechanisms, such as liquid-crystalline phase behaviour. Accurate definition of the transistor channel and other circuit components is achieved by high resolution printing techniques such as surface energy-assisted inkjet printing. Here we will discuss recent progress towards new architectures and the controlled definition of high performance polymer transistors.

2:00 PM G4.2/P6.2
JET PRINTING FOR THE FABRICATION OF ORGANIC-BASED THIN FILM TRANSISTORS. Kateri E. Paul, William S. Wong, Steve Ready, Michael L. Chabinyc, Raj B. Apte, Xerox Palo Alto Research Center, Palo Alto, CA; Beng S. Ong, Ping Liu, Yiliang Wu, Xerox Research Centre of Canada, Mississauga, Ontario, CANADA.

The expense and difficulty of fabricating large-area thin-film transistor (TFT) arrays for applications such as flat panel displays or imager arrays has led to the development of alternative fabrication methods including direct-write methods such as jet printing. The spatial control of jet printing makes it an ideal technology for direct writing of materials. We fabricated a-Si:H TFTs using printed wax masks in place of conventional lithography. Bottom-gate TFTs with source-drain contacts overlapping the channel were created using a printed three-mask process. These TFTs have I-V characteristics comparable to photolithographically patterned devices, with mobility of 0.6-0.9 cm^2/Vs, threshold voltage of 2-3 V, and on/off ratios exceeding 10^7, for devices with channel lengths below 50 μm. We are exploring the efficacy of jet printed organic semiconductors. Using conventional semiconductor processing techniques we have fabricated TFT devices using regioregular polythiophenes as the semiconductor; preliminary device characteristics show mobility on the order of 10^{-3} cm^2/Vs. We will describe a method for fabricating organic semiconductor-based TFTs by jet printing, discuss the critical parameters in the printing process that affect feature size and resolution, and compare the organic TFTs fabricated by jet printing with devices fabricated by other methods.

2:15 PM G4.3/P6.3
THE INVESTIGATION OF USING CONTACT AND NON-CONTACT PRINTING TECHNOLOGIES FOR ORGANIC TRANSISTOR FABRICATION. Jie Zhang, Paul Brazis, Abhijit Roy Chowdhuri, John Szczech, Dan Gamota, Motorola, Schaumburg, IL.

Low-cost and high-volume manufacturing processes are envisioned for solution processable organic semiconductor integrated circuits fabrication. The organic IC may be the low-cost solution for driving communication devices, i.e., smart cards, RFID tags, flexible displays, and personal-area and body-area networks. This study is investigating the use of commercially-available contact and non-contact printing technologies to fabricate organic transistors in a non-clean room manufacturing environment without the use of vacuum processing. The contact printing technologies investigated were pad printing and screen printing; the non-contact printing technologies were ink jetting and micro dispensing. The material system selection for transistor structures and layers was based on printing technology requirements and commercial availability. The materials were polymer thick film conductors and insulators, conductive nanoparticle suspensions, and organic polymer systems. A series of material property characterization and printing process development were conducted. As a result, several OFET designs were fabricated and the all-printed organic transistors were repeatably shown to be functional. The electrical performance was evaluated and will be discussed.

2:30 PM G4.4/P6.4
EFFECT OF DIELECTRIC SURFACE ON CARRIER MOBILITY IN POLYMER SEMICONDUCTORS. A. Salleo, M.L. Chabinyc, W.S. Wong, K.E. Paul, R.B. Apte, and R.A. Street, Xerox Palo Alto Research Center, Palo Alto, CA; B.S. Ong, P. Liu, Y. Wu, L. Jiang, Xerox Research Centre of Canada, Mississauga, Ontario, CANADA.

The use of semiconducting polymer films in transistor devices has become increasingly interesting as their carrier mobilities approach 1 cm^2/Vs. In general, mobility in polymers is found to increase with

interchain ordering. Because they can be solution-processed, polymers are appealing for large-area applications. Deposition methods include spin-coating, dip-coating and jet-printing. However, since none of these operations is carried in vacuum, the processing history of the dielectric surface prior to the deposition of the semiconductor has a large effect on carrier mobility in the polymer. In this study we characterize promising semiconducting polymers (e.g. polyfluorene and regio-regular polythiophene). Both inorganic and organic dielectrics are tested. When possible, the dielectric/semiconductor interface is modified by adsorption of functionalized monolayers. The flexibility of this approach allows to control surface energy and can be used to promote specific chemical interactions with the semiconductor. For instance alkylation of the oxide surface leads to an increase in carrier mobility in F8T2 from 3.10-4 cm^2/Vs to approximately, 6-8.10-3 cm^2/Vs, higher than the reported mobility of isotropic F8T2 [3-5.10-3 cm^2/Vs]. As most samples show bias stress effects a pulsed bias technique is used to measure transistor characteristics. The deposition process is expected to play a role in the ordering of the polymer as well. Therefore, the interplay of surface preparation and deposition technique in optimizing carrier mobility for FET devices will be explored.

2:45 PM G4.5/P6.5
CRITICAL CONSIDERATIONS IN POLYMER TFT DIELECTRICS. Munira Raja, Giles Lloyd, Naser Sedghi, Bill Eccleston, Department of Electrical Engineering and Electronics, University of Liverpool, Liverpool, UNITED KINGDOM; Raffaella Di Lucrezia, Simon Higgins, Department of Chemistry, University of Liverpool, Liverpool, UNITED KINGDOM.

Gate dielectrics form a critical part in the design of TFTs for integration into displays and other circuits. Obviously the use of thermally grown SiO_2 is impractical in real devices, as is used for the majority of test devices. It remains, however, the standard to which most dielectrics are compared. There is an increasing demand, as TFT properties improve, to find a more suitable dielectric for large-scale integration of polymer TFTs. Such a dielectric needs to be compatible with fabrication procedures and not prone to high leakage, as SiO_2 is known to be in polymeric devices. We propose the use of anodised aluminium as the gate dielectric. Anodisation as opposed to gaseous deposition allows for complicated growth procedures such as oxide growth on a vertical wall. This is essential for production of ultra-fast vertical channel TFTs. Presented is a comparison of aqueous and plasma anodisation techniques of aluminium and their performance in electronic devices compared with that of SiO_2. Particular emphasis is placed on the I-V and C-V analysis of the oxides. Oxide leakage current is observed to increase by up to 4 orders of magnitude with deposition of the polymer onto the oxide. This is also observed in SiO_2 dielectrics with polymer as the semiconductor. Leakage currents are also observed to increase when the polymer is doped with DDQ. C-V analysis shows good oxide formation giving reasonable quality MOS structures in all cases. A frequency dependence of the accumulation layer is observed for all oxides. It has been suggested that this is a relaxation effect of charge carriers in the polymer. These relaxation effects are believed to be associated with charge carrier dynamics and analysis enables charge carrier mobility to be determined.

3:15 PM G4.6/P6.6
MODELING OF I-V CHARACTERISTICS IN ORGANIC TFTS. A.R. Völkel, R.A. Street, D. Knipp, Xerox Palo Alto Research Center, Palo Alto, CA.

Recent interest in organic electronics has led to the development of a wealth of organic semiconducting materials suitable for making thin film transistors (TFT). While experimental methods can reveal many valuable insights into the properties of these transistors, it is often hard to extract definite answers on the distribution of potential barriers and/or trap states without the knowledge of an appropriate physical model. We have developed a computer model that allows us to study the impact of various trap state distributions on the transport properties of thin film MOS structures. Though this model describes only some aspects of a complete transistor structure, it allows us to explicitly study the correlation of threshold and onset voltages, as well as the shape of I-V curves, on concentration and distribution of inter-band states. In particular, we compare our results to experiments performed on poly-crystalline pentacene TFT's which were thermally evaporated onto a bottom gate structure with a CVD grown dielectric. Our calculations show that we can describe many of the experimentally observed I-V curves very well with two different sets of low-lying inter-band states: (1) a narrow (0.1 eV) exponential distribution of donors and (2) a broader (0.5 eV) Gaussian distribution of acceptors. The donor states account for the shift of the threshold voltage and are most likely due to some residual disorder in the pentacene film. The acceptor states account for the current onset at positive gate voltages and the model also suggests that these states are localized near the dielectric interface. The model is used to analyze the changes in the penracene TFT characteristics that are induced by illumination and bias-stress effects. The analysis of data from transistors based on polymeric organic materials will also be discussed.

3:30 PM *G4.7/P6.7
ORGANIC MATERIALS FOR MULTIFUNCTIONAL TRANSISTOR-BASED DEVICES. H.E. Katz, T. Someya, B. Crone, X.M. Hong, A. Dodabalapur, A. Gelperin, Bell Laboratories-Lucent Technologies, Murray Hill, NJ.

For many applications of organic transistor-based electronics, properties other than semiconductor mobility may be more important than mobility itself. In this work, we consider four applications: an electrophoretic pixel switch, a complementary inverter, a simple nonvolatile memory element, and a chemical sensor array, and discuss the particular device and material properties that need to be optimized for each one. The pixel switch requires minimal off current, the inverter depends on an ambipolar transistor pair, the memory depends on a dielectric-semiconductor pairing in which both charge storage and threshold voltage adjustment occur, and the sensor is based on reversible and selective chemical interaction between an analyte and the semiconductor. Achievements reported here include a dynamic range >10 for the inverter and memory element, and sensory discrimination between organic functional groups such as alcohols and ketones. Deposition of semiconductors including thiophene/phenylene co-oligomers and NTCDIs from solution and device operation in the presence of air and solvents are emphasized.

4:00 PM G4.8/P6.8
STRATEGIES FOR ORGANIC INTEGRATED CIRCUITS - NOVEL SURFACE MODIFICATIONS FOR HIGH PERFORMANCE DEVICES. Tommie W. Kelley, Dawn Muyres, Dennis Vogel, Kim Vogel, Paul Baude, Mark Pellerite, Tim Dunbar, Larry Boardman, Todd Jones, Terry P. Smith, 3M Company, Science Research Center, St. Paul, MN.

We show novel and selective means to modify the dielectric surfaces in organic TFTs. Modification schemes include alkyl phosphonic acid monolayers which have a strong affinity for alumina surfaces. Monolayers form robust, extremely uniform thin films and are deposited through simple washing with a dilute solution of the monolayer precursor in solvent. Adding monolayers to organic TFTs has resulted in polycrystalline devices with mobilities nearly equal to single crystal values, while maintaining other device parameters (for example, threshold voltage, on/off ratio and subthreshold slope) required for fully functional integrated circuits.

SESSION G5: FABRICATION OF FLEXIBLE ELECTRONIC DEVICES
Thursday Morning, April 4, 2002
Golden Gate C1 (Marriott)

8:30 AM *G5.1
THE DEVELOPMENT OF A ROLL TO ROLL MANUFACTURING PROCESS FOR POLYMER LIGHT EMITTING DISPLAYS. Jeffrey G. Innocenzo, E.I. DuPont, Towanda, PA.

The author will present an overview of the progress to date in developing a roll to roll manufacturing process for polymer light emitting displays. The topics covered will include substrate selection, barrier development, film coating, photolithographic and other patterning steps, material handling, and defect control.

9:00 AM G5.2
HIGH-PERFORMANCE, FLEXIBLE POLYMER LIGHT-EMTTING DIODES FABRICATED BY CONTINUOUS BAR-COATING PROCESS. Jianyong Ouyang, Tzung-Fang Guo, Jie Liu, Yang Yang, University of California-Los Angeles, Los Angeles, CA; Hiroyuki Higuchi, Masahiro Yoshioka, Tatsuki Nagatsuka, Nitto Denko Corporation, Osaka, JAPAN.

A major advantage of using conjugated polymers for the organic light-emitting diodes is that it permits solution processing. Bar-coating process, which is a continuous process, has been developed for coating polymeric thin films on flexible substrates to fabricate polymer light-emitting diodes. This novel process shows advantage over spin-coating in several aspects. It uses polymer very efficiently and enables a continuous coating of polymer on large-area substrate. A flexible device, using poly(2-methoxy-5-(2′-ethyl-hexyloxy)-1,4-phenylene vinylene (MEH-PPV) as the light emitting layer, exhibits high performance: luminance of 300 cd/m2 at 3 mA and efficiency of 1.2 cd/A. This performance is comparable to that of good devices fabricated by traditional spin-coating process. This

opens a new direction for fabricating polymer light-emitting diodes and possible other organic devices with a low cost.

9:15 AM G5.3
SLOT COATING FOR POLYMER LED DISPLAY FABRICATION. Scott Herrmann, Jan Bernkopf, Alien Technology Corporation, Morgan Hill, CA.

The use of roll to roll technology for the production of small plastic polymer LED displays has the potential to greatly reduce the manufacturing cost for monochrome displays and lighting applications. As an initial step in this direction, we have successfully constructed polymer LED devices using slot die coating of both the hole emissive layer and light emitting polymer layer. On glass substrates, device I-V characteristics and efficiency are similar to that achieved in our labs through spin coating. The internal efficiency of the devices measured up to 2.3 Cd/A. Thickness non-uniformity of less than 6% was achieved on coatings averaging 800 angstroms thick. Functional PLED devices were also fabricated on plastic substrates. The coatings were accomplished on a roll to roll coating line with speeds up to 20 fpm.

9:30 AM G5.4
FLEXIBLE, HIGH-PERFORMANCE POLYMER LIGHT-EMITTING DIODES FABRICATED BY A LOW TEMPERATURE LAMINATION PROCESS. Tzung-Fang Guo, Seungmoon Pyo, Shun-Chi Chang, Gufeng He, Yang Yang, University of California at Los Angeles, Department of Materials Science and Engineering, Los Angeles, CA.

A flexible, high-performance polymer light-emitting diodes (PLEDs) using a low temperature plastic lamination process is successfully demonstrated. Blue-, green-, and red-emitting PLEDs were fabricated by laminating different luminescent polymers and organic compounds together to form the active media. This unique approach enables the selection of the most suitable materials to fulfill the device requirements for the multi-layer PLEDs without the worrisome processing compatibility. In addition, a template activated surface process (TAS) has been successfully applied to generate an optimum interface for this low temperature lamination process. The atomic force microscopy analysis reveals a distinct difference in the surfaces created by the TAS and the spin-coating process. The evidence for the high surface area interface is further enhanced by the impendence study. This observation coupled with the device data confirms the importance of the activated interface in the lamination process.

9:45 AM G5.5
INKJETTED GOLD CONDUCTORS FOR ELECTRONICS ON PLASTICS. Daniel C. Huang, Frank Liao, and Vivek Subramanian, Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA.

Alkanethiol gold nanoclusters have low melting and sintering temperatures, which make them attractive for use as contact metallization in low-cost electronics and display applications on flexible substrates such as plastic, cloth, and paper. Low resistance gold conductors can be produced by inkjetting or screen-printing gold clusters on arbitrary substrates and heating to temperatures below 150 degrees Celsius, fully compatible with conventional plastic substrates. To date, little work has been done on optimizing the structure of these clusters for inkjetted conductor applications. Most gold nanocluster processes reported to date require temperatures that are incompatible with plastic, or result in conductor lines with unacceptably high resistance due to poor microstructure and cracking. We have found that substantial improvements in resistivity and process compatibility can be achieved by optimizing the size, encapsulation, and deposition processes of the nanoclusters. These results indicate that alkanethiol gold nanoclusters may be used to form low-resistance interconnects, high-Q inductors, and high quality contact layers to low-cost electronic devices such as organic transistors and TFTs. We report on studies performed on the effect of annealing process on conductor microstructure and resistivity. We also report on the effect of optimization of the alkanethiol capping chemistry on the annealing requirements of the nanoclusters, and the resulting effect on conductor properties. Finally, we describe the effect of nanocrystal size on the same. Using these optimization techniques, we demonstrate low-resistance inkjet-printed gold conductors with excellent electrical properties suitable for use in low-cost electronics and display applications.

10:30 AM G5.6
CONTACT PRINTING FOR MICROELECTRONIC FABRICATION: GUIDELINES FOR PATTERN FIDELITY AND RESOLUTION. Scott M. Miller, Sandra M. Troian, Microfluidic Research and Engineering Laboratory, Department of Chemical Engineering, Princeton University, Princeton, NJ; Sigurd Wagner, Department of Electrical Engineering, Princeton University, Princeton, NJ.

Contact printing methods offer an attractive approach to patterning large area electronics on flexible substrates. Printed materials can be used, for example, as etch resists to pattern underlying material layers. The ink transfer process relies on low liquid viscosity, but this compromises pattern fidelity and resolution. Since post-printing spreading ultimately determines the maximum resolution achievable, patterns are usually fixed by raising the viscosity through cooling, solvent evaporation, or polymerization. Using a combination of experiment and numerical simulations, we have investigated the spreading behavior of micron scale polymer structures to establish design rules for resolution and pattern fidelity. Experimental results are compared to simulations of capillary driven spreading for geometric patterns relevant to microelectronics applications. Studies of isolated square islands and long lines, as well as intersections and corners, reveal that pattern distortion is worse for smaller feature sizes and thicker films. In addition, exterior corners advance slowly while interior corners spread more rapidly, ultimately leading to undesirable rounding. Distortion also occurs more quickly for liquids of higher surface tension and low viscosity. The initial polymer conformations for these studies were obtained by energy minimization simulations; future studies could use initial conditions from AFM measurements of actual surface profiles. The design rules derived from our studies are applicable to structures obtained by many different printing methods in which the distortion is controlled by capillary and viscous forces. The authors gratefully acknowledge support from the DARPA Molecular Level Printing program and the New Jersey Commission on Science and Technology program on Large Area Electronics. SMM is supported by a graduate fellowship from the Eastman Kodak Company.

10:45 AM G5.7
NANO-METER SIZED COMPOUND SEMICONDUCTOR STRUCTURES AND DEVICES EMBEDDED IN THIN POLYMER FOILS. Jie Chen, Rolf Engelhardt, Rolf Könenkamp, Hahn-Meitner Institut Berlin, Berlin, GERMANY.

We report the growth of semiconductors within nano-meter sized volumes in thin polymer foils. The experimental techniques allow us to prepare devices like resistors, diodes and transistors embedded robustly within the polymeric matrix. Since the matrix is soft compared to the inorganic semiconductor material, mechanical forces due to shear flex and strain motion are minimal, resulting in extremely stable electronic device operation. Nanometer-sized voids are produced by high energy heavy ion irradiation of the foils and subsequent etching of chemically sensitized areas (1). Semiconductor deposition involves solution growth and electrodeposition at low temperatures to prepare conformal coatings or void-filling deposits in volumes with a minimal size of $\sim$30 nm. Devices can be prepared as embedded structures or as free-standing structures when the polymer matrix is dissolved after the semiconductor growth process. (1) R. Engelhardt and R. Knenkamp, J. Appl. Phys. 90, 4287 (2001).

11:00 AM G5.8
NANOTECTONICS: DIRECT FABRICATION OF ALL-INORGANIC LOGIC ELEMENTS AND MICRO-ELECTRO-MECHANICAL SYSTEMS FROM NANOPARTICLE PRECURSORS. Eric J. Wilhelm, Brent Ridley, Joseph Jacobson, Massachusetts Institute of Technology, Media Lab, Cambridge, MA.

The reduced melting point and high solubility of inorganic nanoparticles have been shown to be useful in the low-temperature solution-based fabrication of semiconductor devices. These inks have been patterned using various techniques to form inorganic logic elements and multi-layer structures. Here we report advances in the printing and syntheses of such nanoparticle inks.

11:15 AM G5.9
3-COLOR PIXEL PRINTING VIA STAMPING AND CONTACT DYE DIFFUSION. Kenneth R. Carter, Jesse R. Salem, J. Campbell Scott, Sally A. Swanson, IBM Almaden Research Center, San Jose, CA.

Full-color polymeric light emitting diode (PLED) displays can be realized by using a single blue PLED emitting layer and converting either internally by doping or externally by color conversion. In order to fabricate the red/green/blue subpixels, the materials set must be patternable on the desired length scale. We present an approach that uses blue emitting polymers as a base layer into which we selectively apply novel small molecule fluorescent red and green dyes via patterned contact dye diffusion. We entered into this study with the goal of demonstration and development of technology enabling creation of three color pixels in an PLED device. Additionally, the technology must be extendible to high resolutions (>5 um subpixels) and be amenable to large area flat panel screen production. In the process a dye pattern is transferred from a dye transfer plate (PDMS-based) into a receiving layer (blue LED polymer) on a

substrate by bringing the dye transfer plate into contact with the receiving layer. The pattern of the dye is maintained upon transfer and any subsequent diffusion steps. Preferably, the method is repeated to provide a three-color pattern in the receiving layer. This talk will outline the materials and process conditions used to successfully create patterned 3-color (red, green, blue) PLED devices with pixels sizes appropriate for high resolution PLED displays. Characterization of actual devices will be presented. The process was designed with large areas screens in mind and will find importance in the efficient and low-cost manufacture of flexible PLED displays.

11:30 AM G5.10
FABRICATION OF A METAL INTERCONNECT MATRIX ON A SPHERICAL SURFACE. Rabin Bhattacharya, Pai-Hui Iris Hsu, James C. Sturm and Sigurd Wagner, Department of Electrical Engineering and POEM, Princeton University, Princeton, NJ.

We show that a circuit matrix on a spherical surface can be interconnected by metal with low fracture strain. Fabricating integrated circuits on spherically curved surfaces requires extensive deformation of planar circuits, because no techniques exist for the direct fabrication of ICs on spherical substrates. Our approach is to (1) fabricate rigid circuit islands on plastically deformable substrates, (2) deform these structures to spherical surfaces, and (3) apply the interconnect wiring on the spherical surface. The island/substrate structure is designed such that the inter-island regions of the substrate take up most plastic deformation. Because this strain in the inter-island substrate region exceeds the critical strain of the thin-film metals used in IC metallization, the interconnects can be applied only after spherical deformation. However, at least three mask levels are needed for the X-Y addressing of a circuit matrix. We circumvent this requirement for several successive levels of patterning on the spherical surface by building crossovers into the circuit islands as part of step (1). Then, before deformation, while the substrate is still flat, a plastically deformable sacrificial pattern is overlaid on the entire surface. In step (2) this pattern is deformed along with the islands and the substrate. In step (3) the pattern serves as the mask for metal deposition onto the spherical surface by liftoff. To date we have made 2-micrometer wide X-Y interconnects between islands, where the two levels are isolated by the pre-fabricated crossovers. We describe island and crossover design and fabrication, experiments with the sacrificial layer, alignment of metal lines to the circuit islands, and electrical results. This work is supported by the MLP program of DARPA.

11:45 AM G5.11
CdS AND PbS FILMS ON FLEXIBLE SUBSTRATES FOR APPLICATIONS IN ELECTRO TEXTILES. M.S. Shur, Rensselaer Polytechnic Institute and Biomedical and Information Technologies, Inc.; R. Gaska, Sensor Electronic Technology; S. Rumyantsev, B.Q. Wei, R. Vajtai, and P.M. Ajayan, Rensselaer Polytechnic Institute.

We report on structural and electrical properties of CdS films deposited at temperatures below 90°C from citrate solutions containing complex cadmium ions and tiorea. We demonstrated deposition on a variety of flexible substrates, including viewfoils, cloth, and threads and fabricated devices on the deposited films including solar cells, stress sensors, and photoconductive sensors. TEM and SEM data show that the films consists of nanocrystalline grains (of several nanometer sizes) separated by grain boundaries. The X-ray diffraction curves identify crystalline CdS with hexagonal structure. The relative intensity of the peaks in the X-ray diffraction spectrum shows that the crystallites must be oriented and, therefore, the film might have pyroelectric properties. The nanostructure of the CdS films results in a giant reproducible sensitivity to stress (tension) under UV illumination. We will also report on the properties of CdS deposited on a viewfoil with a layer of carbon nanotubes. This composite material has the same energy gap as CdS but exhibits several orders of magnitude lower resistivity. Finally, we discuss the device applications for photovoltaic cells on fibers and cloth and report on the measured characteristics of the CdS photovoltaic cell fabricated on a fiber.

SESSION G6: DISPLAYS, POWER, AND COMPONENTS
Thursday Afternoon, April 4, 2002
Golden Gate C1 (Marriott)

1:30 PM *G6.1
FLEXIBLE LCD WITH RUGGED IMAGE STORAGE. Guy Bryan-Brown, Alistair Graham, Emma Wood, Pete Brett, ZBD Displays Ltd, Malvern, UNITED KINGDOM.

The use of plastic instead of glass substrates in LCD manufacture is seen as a key step in improving display portability by reducing weight and thickness and also reducing screen breakage. Furthermore thin plastic substrates lead to clearer text in reflective LCDs by removing parallax and also allow the display to conform to curved surfaces. Two technologies dominate current LCD products; supertwisted nematic and active matrix twisted nematic. Both these show difficulties in migrating to plastic. Supertwist requires very tight control of cell gap and pretilt in order to achieve high multiplexing and good contrast. These aspects are harder to control on a plastic substrate. Active matrix displays require multi step high resolution photolithography and so are harder to make on plastic due to dimensional changes (induced by absorption or temperature variation) as well as the low maximum working temperature. An alternative approach to plastic LCDs is to use a bistable display mode which has a well defined threshold and so can be infinitely multiplexed without an active matrix. In recent years a number of approaches have been developed for adding bistability to an LCD. The ZBD (zenithal bistable display) is an example of a bistable nematic LCD which is unique in relying on surface rather than bulk bistability and makes it the only bistable LC technology which can retain a written image after the application of mechanical shock. An 83x90 pixel matrix addressed ZBD prototype has been made using polyethersulphone (PES) substrates one of which incorporates photodefined spacer pillars to ensure a uniform cell gap. This shows good reflective optical properties and can be flexed and compressed without loss of the written image. Matrix addressing of this display confirms that the technology can be extended to displays with many thousands of lines allowing large area images with paper-like resolution.

2:00 PM *G6.2
NOVEL FLEXIBLE ELECTRO-OPTICAL DEVICES USING FERROELECTRIC LIQUID-CRYSTALLINE POLYMER AND PLASTIC FILM SUBSTRATES. Hitoshi Kuma, Toshihiro Iwakuma, Masahiko Fukuda, Takashi Sekiya, Idemitsu Kosan Co. Ltd, Central Research Laboratories, Chiba, JAPAN.

A novel flexible LCD was developed by combining plastic film substrates with a FLCP mixture. Its optical response time was improved by using a newly developed FLC polymer, particular polysiloxane typed structure. Using a FLC mixture based on the FLCP, wide temperature range of chiral Smectic C phase in the range from -20 to 80°C and short electro-optical response time of 0.4ms at 25°C was achieved. Additionally, good toughness against external shock was achieved by arranging columns of UV-cure resin in the FLC layer. The FLC layer was 2μm thick. The manufacturing process of this LCD has great advantages because it is possible to produce LCD by roll-to-roll process with high productivity and low plant investment. This technology was applied to two typical applications. One was a prototype of the electric-paper. The display part was B5 size (VGA) and B/W reflection type. High-contrast ratio, wide viewing angle and clear flickerless images was achieved due to the bistable memory effect of FLC. After the display part was removed from the controller, contents remained without any power supply. The other was a high-speed and large-area LC shutter, which was obtained by putting one or more polarizers on the LCD. This LC shutter could be used for a 3D imaging monitor or a field sequential-type high-resolution monitor. Because of the short response time of FLC, the direction of polarization could be changed uniformly in the large area. In the application for LC shutter, the refractive index of UV-cure resin was adjusted to the average refractive index of LC molecules. Therefore, the intensity of scattered light was minimized at the interface between UV-cure resin and LC domain, and high contrast ratio more than 100 was achieved.

2:30 PM G6.3
FABRICATION OF FIELD EMISSION DISPLAY ARRAY ON FLEXIBLE SUBSTRATE USING NANOTECHNOLOGY. A.H. Jayatissa, S.T. Cheng, Materials Science and Engineering Program, CMD Department, Western Michigan Univ, Kalamazoo, MI; A.C. Jayasuriya, Dept of Chemical and Bio-chemical Engineering, Rutgers Univ, Piscataway, NJ; A. Choudhury, Industrial and Manufacturing Department, Western Michigan Univ, Kalamazoo, MI.

We have fabricated multipurpose flexible circuit array devices using Cu/Polymer and Al/Polymer as the starting substrate for display applications. Array was fabricated using chemical etching and electroplating. Surface and electrical properties were studied with the aim of minimizing metal thickness for a given line width without affecting the electrical properties. Metal array size was changed from diameter of 5-20 μm. Interconnect area was completed with line widths of 10 and 20 μm. Ni layers were used as the surface finishing of Cu and Al lines which provide better surface barrier for mechanical scratching, moisture absorption and oxidation. Advantages of this method include growth of nanomaterial layers on Ni surfaces, which can be used for field emission display as well as electron gun applications. We demonstrated latter possibility with electrophoresis coating of diamond nanoparticles on Ni surfaces. It is found that proposed material selection is an ideal way to fabricate multipurpose flexible circuits such as emission region of field emission display, interconnect, and wiring.

2:45 PM G6.4
LIGHT EMITTING DEVICES MADE FROM AMORPHOUS III-NITRIDES ON FLEXIBLE SUBSTRATES. Hugh H. Richardson, Daniel R. Richardson, Paul G. Van Patten, Ohio Univ, Dept of Chemistry and Biochemistry, Athens, OH; Martin E. Kordesch, Ohio Univ, Dept of Physics and Astronomy, Athens, OH.

Light emitting devices can be fabricated from amorphous AlN hosts and flexible polymers substrates. The phosphor layer is an amorphous AlN host with lanthanide ion luminescent centers and is activated by oxygen contamination during growth. Ordinarily, rare-earth III-Nitride materials must be activated at elevated temperatures (∼1000K) before appreciable luminescence can be observed. We have shown that oxygen contamination is an effective alternative to thermal activation. For example, in AlN:Eu3+ a study of the CL intensity versus oxygen incorporation indicate that luminescence turns on if the oxygen content in the sputtering plasma exceeds a few percent. In fact, oxygen incorporation appears to have a greater impact (>600-fold) on luminescence than does thermal activation (100-fold). Using this approach an alternating current thin-film electroluminescence (ACTFEL) device was constructed using a polymer substrate and an amorphous AlN:Tb3+ film as the phosphor. A stripe of light 0.6 mm x 14 mm emanating from the top electrode emits when the device is operated AC with a frequency of 1 kHz at 170 V rms. The EL spectrum from the device is very similar to the CL and PL spectrum and the lifetime of the excited state is relatively long (850 microseconds) and single exponential.

3:30 PM *G6.5
NEW REDOX-ACTIVE COMPOUNDS WITH HIGH CAPACITY: SULFER CONTAINING HETEROCYCLIC COPOLYMERS FOR LITHIUM SECONDARY BATTERIES. Hiroshi Uemachi, SENSA Co. Ltd, Ishikawa, JAPAN; Yoshihiro Iwasa, Tohoku Univ, Inst for Materials Research, Sendai, JAPAN; Tadaoki Mitani, JAIST, Tatsunokuchi, JAPAN.

Polymer batteries are key devices for flexible electronics due to their plasticity, ease of manufacturing, and low cost. Conducting polymers and organosulfur compounds have been investigated for cathode materials for battery applications. Particularly, organosulfur compounds, which contain disulfide (S-S) bonds in polymer main chains, are the most promising cathode materials for lithium secondary batteries. In this paper, we report a new class of redox system, polymers consisting of aromatic ring and unsaturated five-membered heterocyclic ring including the S-S bond. The advantages of this system are (1) the high theoretical capacity, (2) fast redox rate, (3) electrical conductivity, and (4) cycle life extension. A copolymer, composed of 1,2,4-dithiazolium ring and benzene, exhibited a reversible cyclic voltammogram with three redox peaks and electrical conductivity. A discharge test showed a capacity of 420 Ah/kg, which is about 3∼4 times higher than those of other conventional cathode materials. The high capacity is possibly ascribed to successive redox reactions of an S-S bond and a seven-π-electron unsaturated five-membered ring. Another new redox copolymer, consisting of 1,2,4-dithiazolium ring and *p*-phenylenediamine, showed a capacity of 259 Ah/kg with excellent cycleability.

4:00 PM G6.6
POLYMERIC NANOSCALE ALL-SOLID STATE BATTERY. Steven E. Bullock, Sufi R. Ahmed, Department of Materials and Nuclear Engineering; Peter Kofinas, Department of Chemical Engineering, University of Maryland, College Park, MD.

We have taken advantage of the nanoscale self-assembly of an A/B/C triblock copolymer for the fabrication of an all-solid state nanoscale polymer lithium battery. The advent of polymer electrolytes has provided a promising route to an all solid state polymer battery. Current battery configurations typically involve a metal anode, a solvent-plasticized polyelectrolyte, such as poly (ethylene oxide) (PEO), and a composite cathode. The block copolymer was derived using Schrock's catalyst for ring-opening metathesis polymerization (ROMP). Self-assembly of block copolymers provides nanodomains whose morphology can be controlled. These domains then act as a template for the formation of nanoclusters containing metals and other inorganic moieties. The polymeric battery was synthesized with the "A" block as the anode, the "B" block as the electrolyte and and the "C" block as the cathode by forming the A/B/C triblock whose microphase separation results in lamellar domains. These nanodomains contain cobalt oxide, and a spinel phase $LiMn_2O_4$ as the anode and cathode material, respectively. The first block provides the source for the electrochemical reaction to begin. The second block is polyethylene oxide derived from an unsaturated crown ether, and is used for its high ionic conductivity. The third block contains $LiMn_2O_4$, which is currently being investigated as a potential cathode material because of its low toxicity and ease of preparation. All monomers and polymers were analyzed by ^1H and ^{13}C NMR and FTIR to determine their composition and structure. The metals confined within the blocks of the copolymer were characterized by XPS and X-ray diffraction. In addition, GPC of the homopolymers of each of the blocks and triblock polymer was performed to verify the molecular weight and molecular weight distribution of each of the blocks.

4:15 PM G6.7
THE GROWTH OF PENTACENE ON Au. F.-J. Meyer zu Heringdorf, L.L. Kosbar[a], R.M. Tromp, IBM T.J. Watson Research Center, Yorktown Heights, NY; [a]present address: Colorado School of Mines, Golden, CO.

Pentacene ($C_{22}H_{14}$) is one of the most promising materials for use in organic semiconductor devices. Polycrytalline layers of pentacene with large grains and excellent electronic properties can be grown on a variety of substrates. For devices, however, these films need to be contacted to terminals. While Au films deposited on pentacene are widely used, it would be advantageous to use bottom contact geometries, where predefined Au contacts are overgrown by pentacene. We used Low Energy Electron Microscopy and Atomic Force Microscopy to compare the growth of pentacene on Si(111) and SiO_2 with the growth on different types of Au films on Si(111). At low coverages, Au forms a (5×2) reconstruction on the Si(111) substrate, and pentacene is observed to grow in the thin film phase, similar to growth on clean silicon or SiO_2. At coverages beyond 3/4 ML Au, however, a $(\sqrt{3} \times \sqrt{3})$ reconstruction is formed that causes the orientation of the pentacene crystal to rotate by almost 90°. The same result is found for thicker Au films. The adsorption of organic self-assembled monolayers (SAMs) prior to deposition of pentacene has been reported to improve the electrical contact between Au and pentacene. Here we show that pentacene growth on thiol SAMs on Au restores the growth mode and crystal orientation seen on Si and on SiO_2. A comparison with pentacene growth experiments on cyclohexene covered Si shows that carefully chosen organic substrate termination layers are likely to play a key role in the development of organic thin film semiconductor technology.