SYMPOSIUM L

Materials, Technology, and Reliability for Advanced Interconnects and Low-k Dielectrics

April 16 – 20, 2001

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*Invited paper
Advanced microelectronic interconnection structures make use of high-conductivity copper conductors with low dielectric-constant insulators at extremely small dimensions. As a consequence, issues arise in the characterization and reliability of these structures that are not found in the well-characterized aluminum-silicon system. Differences appear in the microstructure of the copper metallization and the changes induced in it by processing, thermal loading and electromigration; the mechanical characteristics of the surrounding dielectric, and the resulting interdependence of the reliability of the interconnection structure and the changes in the metal microstructure as constrained by the dielectric. This tutorial will cover these topics, introducing participants to the issues involved and the fundamental reliability concerns for both the metallization and the dielectric encapsulant. Advanced methods for characterizing electromigration behavior (especially that of copper), mechanical properties of dielectrics (especially those of low-k materials), and metallization microstructure (by X-ray diffraction) will be described.

Instructors:
Du Nguyen, IBM Microelectronics
Robert Cook, University of Minnesota
Stuart R. Stock, Georgia Institute of Technology

SESSION L1: Cu/LOW-k INTEGRATION AND PROCESSING
Chair: Robert D. Miller
Tuesday Morning, April 17, 2001
Golden Gate B2 (Marriott)


Back End Of Line (BEOL) interconnect performance improvement requires the reduction of resistivity and capacitance. IBM introduced copper metallization for the 0.22 mm technology node and a lower permittivity fluorocarbonate glass for the 0.18 mm technology node. For the 0.13 mm technology generation, a low-k thermosetting polymer, SILK(TM), was selected for use as a replacement copper and implemented into manufacturing. This will be the first true low-k dielectric to be fully integrated with copper wiring. The selection of SILK(TM) and the challenges of low-k integration will be described.

9:00 AM L1.2 ADHESION STUDY BETWEEN MATERIALS FOR COPPER AND INORGANIC LOW-k DIELECTRICS. Filip Landemans*, S.H. Breyersma, S. Poortmans, T. Conard, H. Bender, E. Beyne, K. Moeke, IMEC, Leuven, BELGIUM, "also at E.E. Dept., K.U.-Leuven, BELGIUM."

Copper and low-k materials are chosen to replace aluminum/silicon dioxide based interconnects for improving the density and the performance of interconnects. A main challenge regarding reliability is the adhesion between the various materials used in the back end of the line. In this work, shear testing is used to quantitatively determine the adhesion strength. The focus is put on the interfaces between several inorganic low-k dielectrics, hard mask materials and metals (copper and barriers). The inorganic materials form an important class among the low-k dielectrics. A distinction can be made between chemical vapor deposited SiOxNy-based materials (kn3) and porous silicon dioxide based spin-on dielectrics (kn2). Besides silicon dioxide, silicon carbide and nitride are used as hard mask materials. The test structure itself consists of a stack of circular copper dots placed on top of different layers. During shear testing, a needle pushes laterally against the copper dot until failure occurs at the weakest interface (adhesive failure) or within the weakest material (cohesive failure). The maximum failure force is monitored. By changing the presence or the sequence of the different materials in the test structure, several types of interfaces can be evaluated. The influence of different heat treatments and size of the copper dots is discussed. X-ray photoelectron spectroscopy, scanning electron microscopy and auger electron spectroscopy provide a deeper understanding of the failed interface, and are necessary to explain the measured shear force.

9:15 AM L1.3 CMP GOVERNING PROPERTIES OF POROUS SILICA ILD FILM (ALCAP(TM)). Hisayuki Hanabashi, Takasumi Itoh, Kiku Miyamoto, Sune Kurosawa, Akiko Kagaya, Tatsuo Tanabe, Asahi Chemical Industry Co., Ltd, Central Technology Laboratory, Shinya Matsumo, Asahi Chemical Industry Co., Ltd, Analytical and Computational Laboratory, Shizuoka, JAPAN.

The porous silica ILD films (ALCAP(TM)) whose dielectric constants went in range of 1.7-2.8 were successfully prepared via organic polymer/silica hybrid and an attempt was made to correlate the basic properties such as Young’s modulus, hardness, and cohesive strength with CMP compatibility. In addition to these properties the effect of the film thickness was also studied. Main issues in CMP are reported to be cohesive failure as well as delamination between the film and a cap layer, however, the former can be avoided when the cohesive strength becomes >60 MPa, evaluated by the modified Step-pull test) and the latter by an increase in Young’s modulus and hardness without hysteresis loss. Surprisingly, results on a tape-pull test were found to be affected by the modulus and hardness and could be a measure of delamination at CMP. With decreasing the film thickness below 0.5 µm, the film tends to be more compatible, exhibiting an apparent increase in the modulus and hardness by the substrate effect.


Low-dielectric constant materials (k < 3) have found widespread application in recent years in the semiconductor industry. Films comprised of SiOxCy materials are deposited by CVD due to their low dielectric constants in the region of 2.6 to 2.9. Organic (poly(methacryloyl) ether) and silicone polymers are spin deposited and have a dielectric constant between 2.5 and 2.8. Nanoporous silicon films are also spin deposited and have dielectric constants in the 1.9 to 2.4 regime. Typically these low-k materials are integrated with etch-stop and hardmask layers such as SiNx (k ~ 8) and SiO2 (k ~ 5) which increase the effective dielectric constant of the combined stack. In addition SiNx and SiO2 are typically plasma-deposited and can damage low-k materials, thereby further increasing the effective dielectric constant of the stack. This paper presents an alternate integration scheme through the substitution of SiNxF and SiOx etch-stop and hardmask layers with low-k spin-on dielectric and hardmask layers. The experimental results are consistent with simulations indicating that this scheme can be demonstrated in both low-k etch-stop layers can be substantially lower than stacks containing conventional plasma-deposited etch-stops. Thermal and electrical data, including thermal stability, adhesion, hardness, and elastic modulus are also reported. Integration issues such as etch selectivity and exposure to standard Cu CMP conditions will also be discussed.

9:45 AM L1.5 VIA POISONING-FREE DUAL DAMASCENE ETCHING FOR ORGANIC LOW-k MATERIAL INTEGRATION. Yu-Chang Kim, Min Chul Kim, Yui Seok Cho, Jin Woong Kim, Hee-Koo Youn, Hyundai Electronics Industries, Memory R&D Div, Ichon, KOREA.

Dual damascene processes have been investigated in the integration of organic low dielectric constant (low-k) material such as SILK-H (k = 7.7). Among the dual damascene scheme, via dual damascene full etch (VFD-F) scheme has the advantages in the process performance and process reliability over any other dual damascene scheme in oxide and also low-k dual damascene schemes. But we found that the integration of SILK-H using VFD-F scheme has problems such as via poisoning and non-uniform UV photoresist (PR) vias-filling, at trench mask patterning. The former induces cylindrical defects over via openings and the latter causes via openings into the trench hard mask (HM) oxide etch. The latter causes etch-through of underlayer metal etch barrier and attack of underlying metal in some damascene pattern because of the use of metal etch barrier. The solution to such process issues relating SILK-H VFD-F scheme was driven to look
for. We etched SiLK-H with oxidizing gas, O$_2$/N$_2$, using ECR etch with high-density plasma source. And then we developed trench HM oxide etch with low selectivity to DUV PR to remove trench HM oxide and via overhang. DUV PR simultaneously. Also VFD etched 
that SiLK-H at via is etched partially was employed. VFD/P-D scheme offers the advantage over VFD/P scheme 
with respect to DUV PR viafilling, inhibiting back-end of the metal etch barrier as a result. The combination of trench HM 
oxide etch with low selectivity to DUV PR and VFD/P-D scheme promises well-defined SiLK dual damascene integration excluding process issues above mentioned in SiLK/P VFD/P scheme.

SESSION I-2: CVD LOW-k DIELECTRICS
Chair: Andrew J. McKerrow
Tuesday, April 17, 2001
Golden Gate B2 (Marriott)

10:30 AM #L2.1
INTEGRATED CVD LOW-k TO 0.10µm AND BEYOND.

This paper discusses the integration aspects of chemical-vapor deposited low-k dielectric films in copper dual damascene structures, starting with an FSG/SiN dielectric/Cu diffusion barrier baseline at the 0.10µm technology node and transitioning to Black Diamond™ and BLOK™ in more advanced 0.15-0.10-µm devices. In FSG/SiN structures, reliability testing demonstrated that interface delamination is a function of the hydrogen content in the nitride. This finding has key implications for the development of low-k/damascene dielectric. Furthermore, a correlation between the deposition chemistry of the PECVD FSG and the stability of the film is demonstrated. Fluorine was found to outdiffuse to adjacent layers when deposited using silicon precursors and it remains bound in the FSG film when deposited using TEOS-based chemistry. Hence, fluorine in silane-based FSG is not tightly bound to the silicon even at very low concentrations (1% at 5%). Indeed, this fluorine outdiffusion is responsible for observed catastrophic failure of the FSG low-k/hydrogen nitride structures when subjected to furnace anneal. No failure was observed with TEOS FSG. For these reasons, the combination of TEOS FSG/low-k SiN is more appropriate as first generation dielectric films for copper dual damascene structures.

For ≤0.13-µm Cu damascene, ILD and barrier/etch step k reduction were achieved by substituting Black Diamond™ FSG and BLOK™ SiN: SiO for BLOK™ SiO: SiN, being a CVD hydrocarbon amorphous silicon carbide, showed similar electrical leakage and Cu diffusion performance to the low hydrogen SiN with an added advantage of a lower k. Prior to SiN or BLOK™ deposition, copper oxide needs to be removed since CuO can reduce electromigration lifetimes, increase via resistances, and cause poor adhesion at the Cu/dielectric interface. However, CuO removal can result in the formation of copper silicide and hillocks. It is demonstrated that these side effects can be eliminated through the control of the kinetics of the amorphous nitride treatment process. Black Diamond™ BLOK™ dual damascene integration showed an etch selectivity >10:1 and a 35% reduction in capacitance relative to oxide/SiN:SiO control without a significant etch stop. Good adhesion properties and compatibility to CuM™ have also been achieved. Black Diamond™ has been successfully integrated in an eight-level metal-dual damascene structure while maintaining reliability standards. The extension of CVD low k to ≤0.10-µm generation was demonstrated with a Black Diamond™ film of k less than 2.5. Single damascene integration results of this film will be described.

11:00 AM #L2.2
PATTERNING OF LOW-k CVD FILMS. Hilton G. Price Lewis, Koren H. K. Glenser, Project L.D. Heritage Institute of Technology, Dept. of Chemical Engineering, Cambridge, MA; Gino L. Weibel, Christopher K. Ober, Dept. of MSE, Cornell University, Ithaca, NY.

Thin films produced by chemical vapor deposition (CVD) show promise as materials capable of undergoing patterning by lithographic means. In this paper, we consider the use of fluorocarbon and organosilicon films deposited by hot filament CVD (HFCVD) for producing nanometer-scale features. HFCVD is a new plasma technique which offers the ability to tailor the chemistry of films with polymers-like structure. Both fluorocarbon and silicon-containing polymeric materials are under consideration as candidates in next-generation microelectronics technologies. Their transparency makes them ideal resist candidates for 157-nm lithography, and their low dielectric constant makes them strong contenders as interconnect materials. As one part of this paper, we present a collaboration aimed at merging the role of resist and low-k dielectric. Specifically, we are investigating a direct dielectric patterning process in which a material is deposited by CVD, exposed using UV, and then etched using UV, HM oxide and via overhang. DUV PR simultaneously. Also VFD partial etch (VFD/P-D) scheme that SiLK-H at via is etched partially was employed. VFD/P-D scheme offers the advantage over VFD/P scheme with respect to DUV PR via filling, inhibiting back-end of the metal etch barrier as a result. The combination of trench HM oxide etch with low selectivity to DUV PR and VFD/P-D scheme promises well-defined SiLK dual damascene integration excluding process issues above mentioned in SiLK/P VFD/P scheme.

12:15 PM #L2.3
PECVD DEPOSITED SiCOH FILMS WITH REDUCED DIELECTRIC CONSTANT. A. Grill, V. Patel, IBM T.J. Watson Research Center, Yorktown Heights, NY.

Carbon doped oxide low-dielectric constant (low-k) materials comprised of Si, C, O and H (SiCOH films) prepared by plasma enhanced chemical vapor deposition (PECVD) have been demonstrated previously with dielectric constants of about 2.7-2.8. These k values appear to be almost independent of the deposition tool or process parameters. However, the dielectric constant of SiCOH films can be further lowered by enhancing the atomic level porosity. This nano-porosity enhancement can be achieved by depositing multilayer films containing at least one thermally unstable phase and annealing the films to remove this volatile phase from the material. Dual phase materials have been studied in the present study by PECVD from mixtures of SiCOH precursors with hydrocarbons. The films have been characterized as-deposited and after thermal anneals up to 8 hours at 1000°C by Rutherford backscattering (RBS) and forward recoil elastic scattering (FRES) and by FTIR. The dimensional stability of the materials has been determined by measuring the size of the step heights produced in the films. The electrical properties have been measured on metal-insulator-silicon (MIS) structures. The dimensions were found that, after an initial anneal resulting in a significant loss of CH and some SiH bonds, accompanied by a thickness increase of up to 40%, the films stabilized. Depending on the deposition conditions, choice of the hydrocarbon, and its concentration in the feed gas the dielectric constant of the stabilized films reached values significantly lower than previously reported. These results indicate the feasibility potential of the carbon doped oxide PECVD dielectric to future generation of ULSI chips.

12:30 PM #L2.4
IMPROVEMENT OF THE PROPERTIES OF LOW DIELECTRIC CONSTANT PLASMA POLYMERIZED DECAHYDRONAPHTHALENE THIN FILMS BY THE POST-DEPOSITION HEAT TREATMENT. Joelyong Yang, Cheonman Shin and Dong-Seun Jung, Department of Physics, Brain Korea 21 Physics Research Division and Institute of Basic Science, Sungkyunkwan University, Suwon, SOUTH KOREA.

Effects of post-deposition heat treatment on the properties of plasma polymerized decahydro-naphthalene (PPDHN) thin films have been studied. For the PPDHN thin film with as-deposited relative dielectric constant k of 2.51, as the heat treatment temperature increased from 150°C to 350°C, k decreased from 2.45 to 2.13. With the increase of the temperature of heat treatment, thermal stability of the PPDHN thin film improved. Changes of the k value and thermal stability were related to changes of C=H, C=O and O-H group density.

1:45 PM #L2.5

Integration of copper interconnects with a low-k dielectric requires a thin dielectric barrier used to terminate each damascene layer after chemical mechanical polish (CMP), known as the "post-CMP" or the Amorphous SiNitride and SiCarbide are candidate for the post-CMP. We report here on amorphous Si, C, H alloy (aSiCH) films deposited by PE CVD from mixed volatile precursors, and on the addition of NH3 to the deposition chemistry to produce Si, N, C, H alkyles ["SNCH"]. Film properties for these films [k, LV curves, hardness, modulus] will be discussed. Investigations of the Cu barrier properties of these materials using electrical [transmission voltage sweep] and analytical [SIMS profile] methods will be presented.
SESSION L3: SPIN-COATED LOW-k DIELECTRICS
Chair: Filip Stefaniak; Lockman
Tuesday, April 17, 2001
Golden Gate B2 (Marriott)

1:30 PM #L3.1
NANOPOROUS, LOW DIELECTRIC CONSTANT ORGANOSILICATE MATERIALS DERIVED FROM INORGANIC/ORGANIC POLYMER BLEND WITH Wolkens, Robert Miller, Teddie Muggibing, Craig Hawker, James Hestek, Elbert Huang, Mike Toney, Phil Rice, Robert Zafirn, IBM Almaden Research Center, San Jose, CA; Ken Rodbell, Steve Cohen, Michael Lance, IBM T. J. Watson Research Center, Yorktown, NY, Kelvin Lynn, Mihail Petkov, Mark Weber, Washington State University, Pullman, WA; Paul Ho, Michael Kene, University of Texas, Austin, TX; Matthew Stein, Oberlin College, Oberlin, OH.

The approach of introducing porosity to lower the dielectric constant of known dielectric materials is most readily realized for silicones. Within this class of material, the organosilicates, which exhibit significantly lower dielectric constants as compared to SiO₂, can be readily converted into nanoporous coatings by a variety of approaches. One such approach, reported previously, utilizes inorganic/organic polymer hybrids derived from a thermally decomposable organic component dispersed in an organosilicate matrix. Nanoporous coatings are then formed by heating spin-coated thin films of the inorganic/organic polymer blends to elevated temperatures. The proper selection of hybrid components with respect to pore generator architecture, molecular weight of both organic and inorganic polymers as well as formulation solvent are critical in being able to reproducibly generate nanoporous structures. Formulation, consideration of processing conditions, selection stability and coating quality, as well as coating characterization with respect to mechanical, electrical, thermal and structural aspects will be presented.

2:00 PM L3.2
DESIGN OF ULTRA LOW-DIELECTRIC CONSTANT ORGANOSILICATES USING BLOCK POLYMER AS TEQPLATES. Shi Yang, C.-S. Pui, Peter Mirans, Om Nathans, Elan Reichmanis, Bell Laboratories, Lucent Technologies, Murray Hill, NJ; Yaw S. Oheng, Bell Laboratories, Lucent Technologies, Orlando, FL; Eric Lin, National Institute of Standards and Technology, Gaithersburg, MD; David Gidle, Dept. of Physics, University of Michigan, Ann Arbor, MI.

As device features in next generation integrated circuits (1C) continue to shrink to increase processor speed, RC greatly limits chip performance and reliability by increasing power dissipation and wire cross-talk in multilevel interconnects. A low dielectric constant (k) material needs to be identified, which must have good thermal stability (above 400°C), low coefficient of thermal expansion (CTE), low moisture uptake, high glass transition temperature (Tg), strong mechanical properties, high electrical breakdown field, good thermal conductivity and good adhesion to various substrates. A new class of organosilicate has been developed that can attain an ultra low-dielectric constant, k (less than 2.0), while exhibiting good mechanical strength. A series of triblock polymers, poly(ethylene oxide)-poly(propylene oxide)-poly(ethylene oxide)(PEO(140)-PPO(100)-PEO) are used as sacrificial materials in poly(methyl siloxane) (MSQ) to generate porous MSQ matrices when heated above 400°C. Dielectric constants equal to or less than 2.0 have been achieved with high dielectric breakdown strength (> 2 MV/cm) when more than 30 wt% loading of triblock porogen. It is confirmed by both small angle neutron scattering (SANS) and positron annihilation lifetime spectroscopy (PALS) that these materials have extremely small pores, 3.4 nm. Spectral X-ray reflectivity (SXR) measurement reveals that the density decreases from 1.3 g/cm³, the density of MSQ, to 0.8-0.9 g/cm³, in porous MSQ. Additionally, the modulus of film is found to be strong, ~3 GPa for a material with a dielectric constant of ~2.0.

2:15 PM L3.3
ZEOLITE LOW-k DIELECTRICS. Zhengfong Wang, Hunning Wang, Yushan Yan, Department of Chemical & Environmental Engineering, University of California at Riverside, Riverside, CA.

Ultra low-k materials are needed for the future generation microprocessors as device dimension continues to scale down [1-2]. One major class of low-k materials that has been intensively studied is porous silica by sol-gel method [2]. Sol-gel silica offers low-k but has concerns of low electrical conductivity, wide pore size distribution, and hydrophilicity [2]. Recently, surfactant-templated mesoporous materials are also studied [3, 4]. But due to their nonporous nature, mesoporous materials may face similar concern as polymeric blends in mechanical strength and hydrophilicity. Here we show that nanoporous crystalline pure-silica zeolites (e.g., silicalite with uniform pores of size 5.5 Å angstrom) offer a promising alternative as low-k materials (e.g., low-k = 2.1) because of their high mechanical strength, high heat conductivity, uniform pore size, and hydrophobicity. Two types of silicate films on silicon wafer (low-k = 2.1, high-k = 4.0, nitride covered) were prepared. The films were made by in-situ crystallization using a synthesis solution 0.32TPAOH:TEOS:15H2O. The second type was prepared by spin-coating of silicate nanocrystals (1.5-5 nm) followed by heat treatment. In-situ crystallization produces continuous films (thickness: 0.2 to 0.4 μm, modulus: 30-40 GPa by nanoindentation, k: 2.7-3.0 in 1 MHz, k stability: fairly stable in ambient air RH=60%, water adsorption: none by IR, CMB compatibility: easily polished to a smooth finish).


3:00 PM L4.1
VOID FORMATION AT TWIN BOUNDARIES IN Cu THIN FILMS DURING THERMAL CYCLING. Atsuko Sekiguchi, Junichi Koike, Kouichi Maruyama, Tohoku Univ, Dept of Material Science, Sendai, JAPAN.

SESSION L4: COPPER THIN FILM MICROSTRUCTURE
Chair: Stefan P. Haus-Riege; Lockman
Tuesday, April 17, 2001
Golden Gate B2 (Marriott)

3:30 PM L4.1
VOID FORMATION AT TWIN BOUNDARIES IN Cu THIN FILMS DURING THERMAL CYCLING. Atsuko Sekiguchi, Junichi Koike, Kouichi Maruyama, Tohoku Univ, Dept of Material Science, Sendai, JAPAN.
Cu thin films have attracted much attention as a new on-chip interconnect material because of its high electrical conductivity and good reliability. Stress-induced phase formation has been reported in Cu thin films and is a major reason for device failure during processing. The present work aimed at understanding the void formation mechanism during thermal cycling. Copper thin films of 500 nm in thickness were prepared on a pseudo-TMS/Co (20 nm)/SiO₂/1700 nm/Co (300 nm) substrates. Stress change was determined by measuring sample curvature. The calculated mechanism map was compared with stress-temperature curves. The microstructure was examined by TEM, and the stress distribution of a void region was calculated using a three-dimensional finite element method (FEM). A computer code. Actual crystallographic orientations of twins were determined by Kikuchi pattern analysis and FEM calculation. The results were compared with TEM and X-ray diffraction analysis. The deformation mechanism map revealed that local stress-glide creep is a major deformation mechanism leading to void formation during thermal cycling. A TEM observation showed that void formation occurred in the twin/dislocation boundary. The FEM simulation revealed that local misorientation of neighboring twin variants caused a large shear stress concentration at twin interfaces accompanying voids. The calculation was consistent with TEM observation that dislocation density was high along twin interfaces accompanying voids, while it was low along twin interfaces without voids. Based on these results, it is shown that shear stress concentration causes the twin interfaces to act as preferential dislocation glide planes, leading to dislocation pile up and void formation at the intersections.

3:45 PM L4.2
EFFECTS OF SEED THICKNESS AND BARRIER STRESS ON MICROSTRUCTURE AND STRESS EVOLUTION IN ELECTROPLATED Cu FILMS VIA PULSED-LASER INDUCTED MELTING AND SOLIDIFICATION
Mark T. Gregory, Saeed Akhavan, John H. Gau, and Paul S. Ho, University of Texas, Dallas, TX.

The development of Cu electroplating in damascene technology has highlighted an interesting phenomenon: room-temperature microstructure evolution. This process involves grain growth, texture development, and changes in resistivity and stress strongly dependent upon deposition conditions and initial state of the deposited film. The plating process and microstructure evolution are further complicated by the interconnect trench geometry. With subsequent device scaling, better understanding of the electroplated (EP) stack must be determined, especially with regard to seed thickness, which will be limited in narrower trenches. With this in mind, we have characterized the seed thickness dependence in blanket films to provide a foundation required to understand the microstructure and plating characteristics in damascene trenches. Our results show a strong dependence of sheet resistance, stress microstructure evolution of the EP. Cu film on seed layer thickness, with an increased rate of room temperature recrystallization with decreasing seed thickness. The microstructure changes include an increase in grain size, a decrease in [111] texture strength and the development of a small [200] texture component over time. However, the changes in the film do not occur at the same rate: the change in log f decreases with the change in seed thickness. The microstructure changes include an increase in grain size, a decrease in [111] texture strength and the development of a small [200] texture component over time. However, the changes in the film do not occur at the same rate: the change in log f decreases with the change in seed thickness. The microstructure changes include an increase in grain size, a decrease in [111] texture strength and the development of a small [200] texture component over time. However, the changes in the film do not occur at the same rate: the change in log f decreases with the change in seed thickness.
because these impurities hamper grain boundary motion. Additionally, the stress decrease from tensile values to close to zero at room temperature indicates a description in terms of the elimination of grain boundary volume, which should give a change towards a more tensile film. Thermal cycling of these layers shows a significant desorption of several C-O-H compounds between 85 and 120 °C accompanied by a stress reduction. This data, combined with a study on the evolution of grain morphology and shear resistance at elevated temperatures for various plating conditions has now led to a detailed understanding of the changes that occur during grain growth in our Copper layers. Apparent discrepancies with other groups will also be discussed.

**4:45 PM L4.6**
PROPERTIES OF SPUTTERED BILAYER WN/W DIFFUSION BARRIERS BETWEEN Si AND Cu. Kevin D. Leddy, Air Force Research Laboratory, Sensors Directorate, Wright-Patterson AFB, OH. M.J. O’Keefe, E.J. Dodelgen, University of Missouri-Rolla, Dept. of Metallurgical Engineering, Rolla, MO. J.T. Grant, Research Institute, University of Dayton, Dayton, OH.

Copper interconnect metallizations in next generation integrated circuits will require thin diffusion barrier layers (<20 nm) between the Cu and low-k dielectric which may also function as seed layers for subsequent material depositions. One possible structure entails an adherent lower resistivity film deposited directly on the intended diffusion barrier, such as W on WN. In this study, sputtered WN/W bilayer thin films were investigated as diffusion barriers between Si and Cu. The total thickness of the WN/W bilayer was fixed at 20 nm while the WN thickness was varied from 0 to 20 nm. After deposition of the barrier films, a 100 nm thick Cu film was sputtered over the W and amorphous WN bilayer. The as-deposited WN/W/Cu film structure was found to be strongly dependent on the relative amount of WN and W present. The influence of temperatures in the range of 450°C and 650°C was also investigated. X-ray photoelectron spectroscopy of the films was used to characterize the as-deposited and transformed phases.

**SESSION 5.5: DIFFUSION BARRIER & METAL THIN FILMS - DEPOSITION & INTEGRATION**
Chair: Mihal E. Gross and Ivo Ranjnumsers
Wednesday Morning, April 18, 2001
Golden Gate B2 (Marriott)

**8:30 AM *L5.1**
ADHESION AND MECHANICAL BEHAVIOR OF BARRIERS IN INTERCONNECT SYSTEMS. Jon H. Dinsmore, Department of Materials Science and Engineering, Stanford University, Stanford, CA.

The drive towards smaller length scales and complexity of device structures and their packages has led to significant challenges with regard to mechanical reliability for microelectronic technologies. Debonding of interfaces, fracture of brittle dielectric layers, stress-corrosion cracking and thermomechanical fatigue phenomena may occur at all levels of processing, during prototyping, or even in-service. Problems have been compounded by the implementation of new porous low-k dielectric materials, new Cu metallization schemes, and the barriers that separate them. These issues are discussed for a number of typical materials found in current interconnect structures. The effect of barrier elastic properties and thickness on the deformation of adjacent ductile metal and polymer layers will be discussed. Molecular simulations involving interface decohesion and attendant deformation of adjacent materials will be described. Model describing the kinetics of subcritical debonding including the effects of environment and temperature are reviewed.

**9:00 AM L5.2**
FUNDAMENTAL BEAM STUDIES OF RADICAL ENHANCED ATOMIC LAYER CHEMICAL VAPOR DEPOSITION OF NITRIDE DIFFUSION BARRIERS. Mary A. Dinsmore, Frank Greer, John Colburn, David Fraser, David Gravas, U.C. Berkeley, Dept. of Chemical Engineering, Berkeley, CA.

As device dimensions continue to shrink and aspect ratios continue to increase in microelectronics manufacturing, it will become increasingly difficult to deposit highly conformal thin films for applications such as copper diffusion barrier layers. Atomic Layer Chemical Vapor Deposition (ALCVD) has been proposed as one way to achieve these highly conformal thin films due to the layer-by-layer growth that is possible when a metallic precursor and a stable reactive species, such as ammonia, are introduced sequentially into a deposition chamber. One problem with conventional ALCVD is that the deposition temperatures that are required to achieve reasonable growing rates and good adhesion properties with low temperature-sensitive materials are too high, and may turn out to be incompatible with integration of these barrier films with temperature-sensitive films such as organic low-k materials. It has been recently proposed that by using a more reactive species like atomic hydrogen, the deposition rate at lower temperatures may be possible. This work focuses on investigating the feasibility of performing Radical Enhanced Atomic Layer Chemical Vapor Deposition (REAL CVD) of titanium nitride at low surface temperatures using TICl, atomic hydrogen and hydrogen radicals. By directly independent beams of each of these species at a given surface (in this case, silicon and silicon dioxide coated on Quartz Crystal Microbalances), deposition parameters of interest such as the sticking probability and reaction probability of these species have been measured as a function of surface temperature and surface preparation. By using these parameters, and a simplified model of reactive species transport, the feasibility of REAL CVD nitride depositions will be discussed. Various measurements of the film quality and composition including XPS and AES analysis of the deposited films will also be presented, paying particular attention to the residual chlorine content of the films.

**9:15 AM L5.3**

Atomic Layer Deposition (ALD) is an emerging ultrathin film deposition technique for advanced microelectronics applications. Enabling features of ALD are precise control over film thickness, excellent conformity and relative insensitivity to wafer size. Additionally, ALD allows interface and film engineering that can be utilized to maximize device performance within the minimum real estate requirements. In this work we report the results for ALD tantalum nitride films with an emphasis on film engineering. Tantalum nitride is deposited by sequential surface reactions of tantalum and nitrogen precursors. Film engineering is achieved by manipulating the surface species distribution and type following the nitrogen precursor reaction. The electrical and structural properties of these tantalum nitride films have been thoroughly characterized. Formation of several metastable phases of tantalum nitride is identified and correlated with a wide range in nitrogen incorporation and film resistivity. In this presentation we will discuss our strategy and data that aim at metastable useful Ta(N) films with target resistivity in the range of 50-200 µm ohm-cm. For example, ultrathin Ta(N) films are found to exhibit sharp interfaces, high density and 100% step coverage over aggressive topography. Specifically, applications for copper interconnect barrier and SiN capacitor electrodes will be addressed.

**9:30 AM L5.4**
CVD TANTALUM AND TANTALUM NITRIDE DIFFUSION BARRIER FOR COPPER METALLIZATION. Cory Wijbma, Joe Hillman, Steve Caliendo, Gene Xu, TEL, Gilbert, AZ.

As feature sizes shrink and aspect ratios grow for IC copper metallization, the need for an alternative to conventional PVD tantalum based copper diffusion barriers will arise. Inorganic CVD of tantalum and tantalum nitride diffusion barriers using TaF₅ as the tantalum precursor has been demonstrated to have good step coverage, good copper barrier properties, low impurities content, low resistivity, and a low deposition temperature. This work presents a modulated CVD tantalum and tantalum nitride film stack deposited by CVD using TaF₅ as the precursor. The modulated tantalum and tantalum nitride stack consists of thin, alternating layers of plasma enhanced CVD tantalum and thermal CVD tantalum nitride. The modulated structure provides the benefits of high step coverage and copper diffusion barrier layers to prevent thermal CVD tantalum nitride with the low resistivity of PECVD tantalum. A warm wall, parallel plate CVD reaction chamber was used on a 200 mm cluster tool with a pre-coated chamber and an ionized PVD copper chamber, enabling fully integrated CVD tantalum barrier and PVD copper processing. The CVD deposition temperature was 350°C, and the pressure was 2 torr. Deposition films were analyzed for sheet resistance, step coverage (TEM), nitrogen to tantalum ratio and fluorine content (RHEE) crysotallinity, surface roughness and density (XRD and XRFT), fluorine depth profile (SIMS), and adhesion (tape tests, stud pull tests, and CMF after copper seed and electroplating). The modulated barrier has a resistivity less than 500 µm ohm-cm, 8500 µm sidewall coverage, 10% surface coverage of 95% percent as measured by SIMS depth profile. Excellent copper diffusion barrier performance of 20 nm thick barrier films has been demonstrated, IPVD copper seed morphology and electroplating performance has also been investigated.
Atomic layer deposition method is one of the new deposition method to grow nano scale thin films. This method has a lot of unique advantages over other conventional chemical vapor deposition method such as a good uniformity in film deposition, good control of film thickness, good control of film coverage, low pin hole density and complete elimination of particle generation. In this experiment, we deposited the TiN and TiAIN films by this ALD method with using organometallic precursors of tetraakis(ethylmethylsilane)dimethylaluminum hydride-one ethyl piperidine(TEMAH-EP) and NH₄Ti. Al sources and NH₃ reactant gas were separately supplied and Ar gas was purged between each reactant gas to supply to suppress the reaction. The Ti and TiAIN films were grown at process pressures about 2 Torr and at various temperatures (163-300°C). The growth rate of these thin films were measured and exhibited the linear relationship with the number of process cycles. The step coverage of these films were examined by scanning electron microscopy(SEM).

And the other physical properties such as the chemical composition, crystallinity and the interface morphology were examined with Auger electron spectroscopy(AES), X-ray photoelectron spectroscopy(XPS), and transmission electron microscopy(TEM). The and the diffusion barrier characteristics was measured after depositing the Cu layer on the top of TiN and TiAIN films. Each x-ray test and AES analysis were conducted to examine the breakdown of the diffusion barrier characteristics and the diffusion of Cu through the diffusion barrier films. With these results we will compare the characteristics of these diffusion barriers of TiN and TiAIN and discuss the growth mechanism of TiN and TiAIN thin film which were deposited by an atomic layer deposition method.

10:30 AM L5.6

MOS CHARACTERISTICS AND THE PROPERTIES OF DIFFERENT IMP Ta, TaN, AND MT-LAYER Ta/N/TaN AS DIFFUSION BARRIERS FOR Cu METALLIZATION: He Lei 1, C. Y. Liu 2, J. J. Wei 3, Y. Qian 3, Kangoo Lee 1, Z. Q. Zeng 2, H. D. Liu 3, Joseph Xie 1*, 1Singapore-MIT Alliance, Advanced Materials Program, Singapore, SINGAPORE, 2Institute of Microelectronics, IME, Singapore, SINGAPORE, 3Nanyang Technological University, School of Material Engineering, Singapore, SINGAPORE, 4Rudolph Technologies Inc., Pauders, NJ.

We report a study on the properties of Ionized Metal Plasma (IMP) Ta, TaN, and multilayer Ta/N/TaN based on a comparative evaluation of their performance as diffusion barriers in Cu based metallization. In this study we are IMP Cu(200A)/IMP Ta(200A)/Ta(150A), IMP TaN(250A)/Ta(150A)/Si, IMP Cu(200A)/IMP Ta/N(150A)/Ta(150A)/Si, and IMP Cu(200A)/IMP Ta/N(150A)/Ta(150A)/Si. The samples were annealed in N₂ ambient at 500°C, 550°C, 600°C and 650°C, respectively. The barrier behavior and film properties of these barriers were examined using Metal-Pulse, Film Stress measurement (FSM), Four-point probe (FPP), X-ray diffractometry (XRD), Rutherford backscattering spectrometry (RBS), Atomic Force Microscopy (AFM), Transmission electron microscopy (TEM). It has been observed clearly from the sheet resistance measurements that thickness of TaN and Ta barriers thickness in 500°C, 550°C and 600°C, respectively, whereas the multilayer Ta/N/TaN could still survive from the annealing up to 550°C. Evidence showing the formation of Cu-Si in the failed film stacks was found from XRD spectra. Based on our studies, two kinds of diffusion mechanisms coexist in Cu migration through barrier layers into the Si substrate, leading to barrier failure; and the other is atomic intermixing between Cu and Ta, which does not cause the barrier failure. Depending on the barrier’s microstructures, the dominant diffusion mechanism is different, and the multilayer Ta/N/TaN has appeared to be the most robust one among the three barriers made in between the Cu layer and Si substrate.

10:45 AM L5.7

EFFECT OF SILICON CONCENTRATION IN CVD Si/TiN THIN FILMS FOR DIFFUSION BARRIER APPLICATIONS AGAINST COPPER IN INTEGRATED CIRCUITS. Dhawer Anjum, Suraj Okeybroski, Eric Eisenman, Ahim Kakkottu, Univ at Albany-SUNY, Albany, NY.

Ultrathin (~1.2 nm thick) TiN films were deposited by a chemical vapor deposition (CVD) process at 370 and 420°C using ammonia, silicon tetrachloride, trimethyl tetradecane and hydrogen chloride. To evaluate the influence of silicon content on the film properties, a series of films with different Si/Ti ratio were deposited. Using the X-ray photoelectron spectroscopy (XPS) Si concentration in the films were found to increase from 0 to ~24% as Si to Ti precursors flow ratio was increased from 0 to 30 sccm, respectively. Four-point probe results were consistent with XPS observations and showed a gradual growth of the resistivity, from 2 m Ohm to 48 m Ohm. Transmission electron microscopy (TEM) analysis of these films revealed a reduction of the grain size (~8 nm to ~1.5 μm) with increasing Si content. Rutherford backscattering spectrometry (RBS) of annealed Cu/TiN/Si stacks confirmed the Cu diffusion through the TiN barrier at 500°C annealing temperature. However, the failure was found to be the worst for pure TiN film relative to Si containing films. Cross-sectional TEM of these stacks showed Cusilicide formation at the interface of pure TiN barrier, while for Si containing films silicide formation was observed only at 500°C. The results prove the efficiency of the acrylonitrile TiSBN thin film barriers provide a significant advantage in the barrier reliability.

11:00 AM L5.8

THE INFLUENCE OF MICROSTRUCTURE IN ELECTROLESS DEPOSITED COBALT BARRIER LAYER ON DIFFUSION BARRIER INTEGRITY IN COPPER METALLIZATION. Amit Kohl, Moshe Eisenberg, Technion - Israel Institute of Technology, Dept. of Materials Engineering, Haifa, ISRAEL, Yosi Sharon, Shimshon, Tel-Aviv University, Dept. of Physical Electronics, Ramat-Aviv, ISRAEL.

Electroless deposited cobalt based thin films were investigated as diffusion barriers for copper metallization. Electrochemical deposition can be dominated by reaction kinetics resulting in a nanocrystalline or amorphous metallic layer. This microstructure is suitable for application as a diffusion barrier as it eliminates the direct, fast diffusion path via the grain boundaries. In the electrochemical deposition of cobalt, nanocrystalline h.c.p. cobalt grains were obtained by incorporation of phosphorus and tungsten. When this non-equilibrium structure was subjected to thermal treatments, TEM and XRD studies revealed phenomenal structural evolution such as microcrystallization, grain growth along a preferred basal plane (0002) orientation, and phase transformation. The diffusion barrier quality was evaluated by capacitance versus voltage and capacitance versus time measurements of MOS structures and compared to SIMS depth profiles. These evaluations indicate that 30 nm thick films of Co₆₉/₉ W₆₆/₉ P₃₀, Co₉₆, P₆₁ and Co₉₆ W₆₄ cm function as effective barriers against copper diffusion up to 450°C. The relative quality of the various cobalt films as diffusion barriers shows a J ohnston lifetime as a function of thermal treatment temperature and time and are explained based on the mechanisms of microstructural evolution.

11:15 AM L5.9

A LOW COST Cu SEED LAYER DEPOSITION FOR ULSI METALLIZATION. Ching-Hin Jan, Xu-Ming Wang, and Fan-Shian Huang, Institute of Electronic Engineering, National Tsing Hua University, Hsin-Chu, TAIWAN.

A novel method of Cu seed layer deposition for ULSI metallization is reported. We deposited tantalum (Ta) film as a barrier layer on SiO₂. Low Pressure Chemical Vapor Deposition (LPCVD) tantalum films with various thickness were then coated on Ta. A mixture solution of hydrofluoric acid and cupric sulfide saturated aqueous solution was used to form Cu nucleus on polysilicon surface. Through several electrochemical reactions, the Cu nuclei grow and replace poly-silicon layer. The rapid thermal annealing at temperature 350°C in N₂ ambient was adopted in order to improve the adhesion between Cu and Ta film. The copper film with thickness 10000Å was then electroplated on the Cu seed layer. Furthermore, Auger, SECM cross section of via, and XRD were measured to understand the composition profile near the interface, step coverage on the via, and texture of the grains. The thermal stability was studied by the G-V measurement of the capacitor (Cu/Ta (500Å)/SiO₂/Si) sintered at temperature from 300°C to 550°C. We found the thermal stable upper limit is up to 450°C. SIMS depth profiles give the consistent results with data from the above electrical test.

11:30 AM L5.10

SUPERCONFORMAL ELECTRODEPOSITION OF COPPER IN 500 TO 75 NANOJETTER FEATURES. Daniel Jaoel, Thomas Moffat, John Bonechi, William Huber, Gery Swafford and David Kelly, National Institute of Standards and Technology, Gaithersburg, MD, Andrei Stanislavskiy, Institute for Plasma Research, Department of Physics, University of Maryland, College Park, MD.

We identify an electric yield superconformal electrodeposition of copper in trenches ranging from 500 to 90 nm in width (all 500 nm deep), a unique hysteretic response in the current-voltage (I-V) data, and characteristic of the "superfilling" electrolyte, and 23% of the resistivity of the electroplated copper in less than one day at room temperature. Trenches as small as 75 nm wide and 250 nm deep were also filled. Superconformal electrodeposition was accomplished using an acid cupric chloride electrolyte containing dichloroethane (Cl), polyethylene glycol (PEG), and 3-mercaptopropyltrimethoxysilane.
(MPSA). In contrast, deposition from additive-free electrolyte, electrolytes containing the binary combinations Cl-PES or Cl-MPSA, or simply benzotriazole yielded a continuous void within the centers of the trenches. A large hysteresis in the I-E deposition characteristic is associated with the “superfilling” Cl-PES-MPSA electrolyte and can be utilized to monitor and explore additive efficacy and consumption. Resistivity measurements performed on corresponding blanket films were used to quantify the relationship between the extent of additive incorporation and its influence on microstructural evolution. The films deposited from the “superfilling” Cl-PES-MPSA electrolyte exhibit room-temperature resistivity results that result in a 29% decrease in resistivity within a few hours of deposition. Reduction of void volume formed during conformal deposition from the nonfilling electrolytes through combination of geometrical leveling effect for trench with sloping sidewalls and chemical passivation of trench openings is also demonstrated. This is relevant because some studies have used trenches with sloping sidewalls because they were the best materials available. However, it is perhaps of greater interest as an intentional method for obtaining improved filled films and vias, e.g., from electrolytes that do not provide perfect fill but might be desirable for other reasons.

11:45 AM L5.11
REACTIVE DEPOSITION OF CONFORMAL METAL FILMS FROM SUPERCRITICAL CARBON DIOXIDE SOLUTION
James J. Watkins, Jason M. Blackburn, David P. Long, University of Massachusetts, Dept. of Chemical Engineering, Amherst, MA.

The fabrication of devices of increasing complexity and decreasing dimensions is placing stringent demands on metal deposition technologies. These include conformal coverage of complex surfaces, complete filling of narrow, high aspect ratio structures, reductions in the thermal budget during fabrication, and mitigation of the negative environmental impacts of current processes. Chemical fluid deposition (CFD) is a novel approach to metal deposition that can meet these challenges. CFD involves the chemical reduction of organometallic compounds in supercritical carbon dioxide to yield high purity deposits at low temperature. Since supercritical CO2 can exhibit densities that approach those of a liquid solvent while retaining the transport properties of a gas, the technique is essentially a hybrid of chemical vapor deposition (CVD) and electroless plating. One advantage of the CFD approach is the elimination of precursor volatility constraints. In CFD precursor transport occurs in solution at low phase concentrations several orders of magnitude above those employed in CVD, which precludes mass transfer limitations and promotes high precursor utilization. Here, we describe the deposition of high purity films of Cu, Pt, Pd, Ni and Au and their alloys by hydrogen reduction of appropriate precursors in CO2. We also demonstrate that the conditions employed provide complete filling of high aspect ratio, sub-100 nm wide trenches etched in Si wafers. Moreover, since aqueous plating baths are avoided and the process efficient contains only CO2, light hydrocarbons and excess H2, this approach offers considerable environmental advantages relative to current practice.

SESSION L6: COPPER ELECTROMIGRATION
Chair: Paul S. Ho and Masahiro Murakami
Wednesday Afternoon, April 18, 2001
Golden Gate B2 (Marriott)

1:30 PM L6.1
ELECTROMIGRATION IN DUAL-MA SCENE COPPER INTERCONNECTS
Kenichi Yama, Masayuki Kusunoki, Ken Shono, Kenichi Watanabe*, Shinji Osakai, Shingo Sugawara*, LSI Quality Assurance Division, “Technology Development Division, Fujitsu Limited, Me JAPAN.

Electromigration lifetime of Cu interconnects has been studied. The lifetime has been found to increase with reduction of line width, even if the grain is bamboo structure. This result indicates the diffusion path is not grain boundary but SiN/Cu or Cu/TiN interface. E was about 1eV, for both stripe and LDEM pattern. Cu films were prepared using dual damascene process and conventional electroplating system. Thickness of Cu film was 0.5 μm. Barrier metal was sputtered TiN (0.3 μm thick). Interlevel dielectric was 0.8 μm thick and cover layer was SiN/SiO2 of 0.7 μm thickness. Via size was 0.27 μm. Two types of test structures were prepared for this study. One was a single level stripe pattern (stripe pattern) that is 1500 μm long. The other was a two-level via pattern (LDEM pattern) that had the metal segment length changing from 2 μm to 200 μm. Electromigration test was done at the temperature from 250°C to 350°C, for activation energy (Ea) estimation. The stress current density was from 1.45×10⁶ A/cm² to 4.0×10⁶ A/cm². Metal width was reduced from 0.27 μm to 8.0 μm to examine the line width effect. The failure sites were inspected using SEM and TEM. In stripe pattern, similar activation energy was obtained between 2 μm and 0.27 μm widths. Those activation energies were 0.98eV and 1.06eV. Current acceleration factor n was 2.07. In LDEM pattern, the activation energy was 1.06eV (0.27μm). Current acceleration factor n was shown 1.72. Failure analysis was conducted on some samples. For the narrow lines (w=0.27μm), voids were seen at the cathode side. In addition, some hillocks were seen at the node side. The failure sites were found in SiN/Cu interfaces. In the LDEM pattern, voids are formed at the interface of Cu beneath via and SiN/Cu interfaces near vias at the cathode side. The median grain size of Cu was about 1μm observed by TEM.

2:00 PM L6.2
REAL TIME OBSERVATION OF ELECTROMIGRATION BY OPTICAL AND SCANNING ELECTRON MICROSCOPY
Fumio Ishimori, Slade Cargill, Department of MSE, Lehigh University, Bethlehem, PA.

We have used optical and scanning electron microscopes to observe electromigration in Al and Cu (lines). The samples have been either pure Al (with 2.5% grain boundary particles) or Cu (with 0.7 μm Si3N4 passivation layer) or Al-0.25 at% Cu (width 10 μm, length 100 μm with a 1.5 μm SiO2 passivation layer). The optical microscope was used with a CCD camera, heating stage, current source and voltmeter. For SEM observations, the same heating stage and electronics were used and the passivation layers were removed by reactive ion etching. In some cases Cu concentration was monitored by energy dispersive x-ray analysis. During electromigration the line resistance was monitored and images were recorded at regular intervals to observe void growth and other morphological changes. Relationships between void growth, Cu concentration, current density and temperature will be discussed.

2:15 PM L6.3

Cu interconnects are increasingly being used in high performance microelectronic circuits. They are believed to have better reliability than Al interconnects, but the reasons for this improvement is still not clear. In this study, we have investigated the electromigration behavior of Bledzki-type test structures fabricated by a damascene process. In-situ measurements of void formation in SiN4 passivated electroplated Cu segments were performed using back-scattered electrons in an SEM at a temperature of 370°C. The segments varied in length from 10 μm to 100 μm and in width from 0.3μm to 5 μm. We observed the existence of a critical current below which no void formation occurred. Above this critical current, voids formed after an incubation period, grew, and eventually saturated. The voids could be closed by reversing the current and new voids formed near the opposite end of the segment. We will also present results on the current density dependence of the rate of void growth as well as on the microstructure and damage morphology which were characterized using focused ion beam microscopy.

2:30 PM L6.4
EFFECT OF CURRENT CROWDING ON VACANCY DIFFUSION AND VOID FORMATION IN ELECTROMIGRATION
Eugene C.Y. Yeh, C.Y. Liu, K.N. Tu, Dept. of MSE, UCLA, Los Angeles, CA; Chih Chen, Dept. of MSE, National Chiao Tung Univ, Hsinchu, TAIWAN.

In multilevel interconnects, current crowding occurs when the current changes direction, such as when passing through a via. We postulate that point defects such as vacancies and solute atoms have a lower probability of occurring in high-density regions than in low current-density regions. Therefore, besides the electron wind force, we propose that in current crowding, the current-density gradient can exert an additional driving force to cause excess vacancies (point defects) to migrate from high to low current-density regions. As a consequence, the voids tend to form in low current-density regions which is contrary to intuition. The magnitude of the current gradient, which changes to a driving force when a potential in the gradient is defined, was simulated. The current gradient force is found to be high enough to affect the atomic rearrangement during electromigration. As the line width scales down, the effects of current gradient force become more and more significant. Also, the current density gradient due to current crowding exists under both dc and ac load conditions.

2:45 PM L6.5
EFFECT OF DIFFUSION BARRIER ON THE ELECTROMIGRATION RELIABILITY OF Cu/OXIDE AND Cu/Low-k DAMASCENE INTERCONNECTS
Dual damascene Cu interconnects require a thin diffusion barrier inserted between Cu and dielectric films. While its primary function is to prevent Cu diffusion through dielectric films under thermal and electrical stress, the architecture and the microstructural property of the barrier can significantly affect the electromigration reliability of Cu. For example, the microstructure of the Cu film is often influenced by that of the underlying barrier film. Also, the characteristic of resistance variation (dR/dt) when electromigration depletes Cu depends on the resistivity and the thickness of the barrier film that may control the current-shunting effect. In order to understand the effect of barrier thickness and properties on the electromigration reliability of Cu, we have studied various Cu/oxide and Cu/low-k damascene interconnects that incorporate several different combinations of Ta and TaN. The results show that the electromigration lifetime and the activation energy of failure widely vary as a function of barrier type and property. It appears that the difference in electromigration performance is associated with a few factors that affect the integrity and the microstructural property of the Cu interconnect, including the barrier and the barrier-dielectric interfaces. The electromigration results were examined also using a thermoelectric finite element model that can solve resistance variation and Joule heating as a function of electromigration-induced voiding.


An electromigration (EM) study has determined the lifetime characteristics and failure behavior of multi-level, dual-damascene Cu/oxide interconnects under a variety of temperature and current conditions. Through the use of multiply-linked interconnect ensembles, statistical evidence of two distinct ("weak" and "strong-mode") failures in dual-damascene Cu/oxide interconnects is noted. A combination of single and repeated (N = 1, 10, 100) serial chains of nominally identical interconnects (0.5 μm wide, 300 μm long) are used in conjunction with statistical analysis based on "weak-link" concepts. So far, more than 10,000 interconnects have been evaluated with the multi-link methodology. The scaling behavior of interconnect clustering shows that the presence of a bimodal distribution of failures has significant impact on interconnect lifetime characteristics. These differences are shown to be potentially important for evaluating interconnect lifetime in very large interconnect arrays similar those in functional ultra-large scale integration (ULSI) devices, especially for the study of early failures. Through focused ion beam analysis, two distinct failure locations are identified that impact reliability within a metallization level containing dual-damascene interconnects: [1] cusp-via bottom voiding; [2] cusp-end trench voiding above the via. Of the two modes, bottom voiding is probably more susceptible to process variation. This variability may show pronounced differences in the relative population of failure types and would certainly be an issue for optimal process flow as device scaling continues. In addition, multi-level voiding is less than about 1.0 μm - consistent with interfacial transport - while accurate stronger mode determination is somewhat hindered by its longer lifetime. Also, mode exchange damage may also have impact when level-to-level reliability is considered. In addition, results on the short length or Bielek effect in dual-damascene interconnects will be discussed.


The results of a study of stress void formation in wide passivated copper lines will be presented. Heat treatment of the lines was carried out using a hot stage optical microscope. This allowed direct observations of void closure and formation to be made at temperature during an annealing cycle. We find that even under conditions where overall stress in the lines is predominantly biaxial void nucleation and growth still occurs. Based on the observations we suggest that localized regions of hydrostatic stress can arise at grain boundaries in wide copper lines due to the microstrastic properties of copper and localized shear processes such as grain boundary sliding.

4:15 PM L6.8 IN SITU X-RAY MICRODIFFRACTION OBSERVATION OF STRAIN WAVES IN DAMASCENE COPPER LINES UNDER THE INFLUENCE OF ELECTROMIGRATION ON 9 MICRON SCALE. R. Spolenak, N. Tamura, B. C. Valek, D. L. Burr, M.D.


In contrast to the knowledge base that has been acquired for Al interconnects over the past 30 years, the investigations of electromigration in Cu damascene interconnects are still relatively new. One of the major issues that has been faced for Al interconnects, whether the local microstructure of Cu has a direct influence on electromigration. In this study, we utilized the newly developed facility for microdiffraction at the Advanced Light Source (ALS) at Lawrence Berkeley National Labs. The triple-3D small angle line along a conducting line can be determined to an accuracy of 2x.4. The spatial resolution is better than 0.8 μm. This technique was applied to the Bielek type Cu damascene interconnects in-situ at 250°C at current densities between 0.5 and 2 mA/cm². The segment lengths ranged from 10 to 100 μm and the line widths from 0.8 to 2 μm. The lines were passivated with 300 nm of Si₃N₄ and showed a critical product (current density x segment length) of between 3000 and 5000 A/cm². Voiding was observed to occur at the Cu/Si₃N₄ interface, not only at the cusp end but also at specific locations along the entire length of the line. The correlation between the void sites, the local microstructure and the local strain/stress state will be demonstrated.


We have characterized the electromigration performance of copper damascene interconnects using moderately accelerated tests at package level. Two metalizations have been studied: CVD copper-deposited on CVD TaN ECD copper deposited on CVD TaN using 90 nm of CVD copper as a seed-layer. All metalizations were passivated using SiO₂. Two line widths have been characterized: 0.6 and 4 microns. Scanning Electron Microscope (SEM) observations provided qualitative information on the microstructure of the tested lines. The wide and narrow lines are respectively polycrystalline and quasi-bamboo for CVD copper, quasi-bamboo and bamboo for ECD copper. For wide lines, we obtained the same activation energy (En) for both metalizations (0.65 eV). For narrow lines, the Ea value is 0.286 eV for CVD copper whereas it is as high as 1.286 eV for ECD copper. For wide lines of both metallizations, failure analysis performed with a SEM gives clear evidences that microstructural gradients have a strong impact on voids and extrusions formation (i.e. that grain boundaries are the active diffusion paths in spite of the low Ea values). For the narrow lines, the Ea value is believed to be related to the width of the extrusion diffusion path on the basis of SEM observations. From the reliability point of view, the extrapolated lifetimes of the metalizations including ECD copper are much higher (1 to 2 orders of magnitude depending on the line width) than for CVD copper. This work has been carried out in the framework of the CCMI agreement between ST Microelectronics, CEA-LETI and France Telecom CNET.

4:45 PM L6.10 INVESTIGATION ON MASS TRANSPORT IN DUAL-DAMASCENE COPPER INTERCONNECT. Hidiki Matsushige, Amun Ramamurthi, Alex Bierwag, K-D. Lee, Patrick Justman, Ennis T. Ogawa and Paul S. Ho, University of Texas, Microelectronics Research Center, Austin, TX; Vallee, A.; Blidnick and Robert Haeussmann, International SEMATECH, Austin, TX.

Electromigration (EM) testing has been performed to investigate the mass transportation phenomenon in Cu/Oxide two level dual-damascene interconnects. The test modules used in this EM testing consist of N number of identical line element connected in series. The numbers of N included in this study were 1, 10 and 100. The lengths of the element are 100 and 300 μm. The line widths were 0.25 and 0.5μm. Average drift velocity in dual-damascene copper interconnects under various testing conditions are estimated from the rate of resistance increase, assuming the voiding that causes the resistance increase proportional to depletion of copper at voiding site. The analysis of resistance change showed that the rate of resistance increase per unit time is mostly proportional to number of N. This result is consistent with the mass transport caused by transport current happened throughout the test module. The failure sites were found to distribute evenly. Focused ion beam of the failure sites analysis revealed that the mass transport occurs primarily at the interface between the copper layer and the barrier metal, and its statistical characteristics will be presented.
SESSION L7: POSTER SESSION
LOW-K DIELECTRICS
Claire R. Cook, Mihajlo J. Gruev, Paul S. Ho, Robert D. Miller and Masoud Marzani

Wednesday, April 18, 2001
8:00 PM
Salon L7 (Merritt)

L7.1 CHARACTERIZATION OF PECVD CARBON-DOPED SiO2
LOW-K THIN FILMS PREPARED FROM TETRAMETHYL-
SILANE. Liengh M. Hsi, N. Balasubramanian, P.D. Foo, Institute of
Microelectronics, SINGAPORE, Si-Sheng Pan, Institute of
Materials Research & Engineering, SINGAPORE, Jianou Shi,
Novellus Systems, Inc., San Jose, CA.

Carbon-doped SiO2 low k thin films were prepared by radio-frequency
[RF] plasma enhanced chemical vapor deposition at 400°C from
polymerization of tetramethylsilane (4MS) and copolymerization of
tetramethylsilane and silane (SiH4) precursor, with nitrogen oxide
(N2O) as co-dopant gas. It is found that carbon film thin films from 4MS
and SiH4 precursor show much higher deposition rate than polymer
thin film from 4MS, while keeping all the other parameters same.
The addition of SiH4 can significantly promote the plasma polymerization
of 4MS molecules. The chemical structure and composition of these
films were characterized using Fourier transform infrared (FTIR) and
X-ray photoelectron spectroscopy (XPS). The two kinds of films have
different chemical composition and structure. It is also found from
FTIR spectra that chemical composition and structure of the films
varied progressively with 4MS flow rate. The characteristic peak
Si-CH3, which is a mechanism giving lower dielectric constant,
increased with 4MS flow rate. On the other hand, film porosity, which
can be characterized by SiO2 cage structure peak at higher
wavenumber, decreased with 4MS flow rate. Five different SiON (n=0
- 4) moieties were identified by XPS and it is found that the dominant
Si moiety is SiO2. The physical properties of the films, such as
dielectric constant, refractive index and thermal stability, have been
investigated and related to the Si-CH3 and cage structure of the films.
The higher the Si-CH3 and Si-O cage structure content, the lower the
dielectric constant. The above two mechanisms compete with each
other resulting in a minimum for the variation of dielectric constant
with 4MS flow rate. The film as prepared shows excellent thermal
stability at temperature as high as 400°C and has a dielectric
constant of about 3, indicating its potential as a low-k dielectric for
advanced interconnect applications.

L7.2 RESIDUAL STRESS AND THERMAL EXPANSION BEHAVIORS
IN DIELECTRIC THIN FILMS PREPARED FROM
POLYALKYLSELICOXANE SPIN-ON GLASS MATERIALS.
Monchul Lee, Wee-Swee Oh, Jong-Hol Lee, and Byungchul Lee, Dept.
Chemistry, Center for Integrated Molecular Systems, and BK-21
Functional Polymer Thin Film Group, POSTECH, Pohang, SOUTH
KOREA.

Polyalkylsiloxanes and their compositions in thin films were
prepared by various process protocols. Their curing process was
in-situ examined by FT-IR spectroscopy, thermogravimetry, and
residual stress analysis. And, thermal expansion coefficients were
calculated in the temperature range of the out-of-glass phase. Optical
and dielectric properties were measured by prism coupling and
nullification ellipsometry. In addition, morphological structure in
thin films were characterized by synchrotron X-ray scattering and
reflectance techniques. Optical and dielectric properties were measured
by prism coupling and nullification ellipsometry. Structures and
properties will be discussed in detail with considering chemical
structure, curing reaction kinetics, and pore. [This study was
supported in part by the Ministry of Science & Technology and the
Ministry of Industry & Resources [Korean Collaborative Project for
Excellence in Basic System IC Technology [SB-B4-CR 04-01-01]] and by
the KOSEF via the Center for Integrated Molecular Systems.]

L7.3 COPPER DIFFUSION INTO LOW DIELECTRIC CONSTANT
PLASMA POLYMERIZED CYCLOHEXANE THIN FILMS
DEPOSITED ON DIELECTRIC ENHANCED THERMAL VAPOR
DEPOSITION. Cheonman Shim, Jayoung Choi, and Deoggun Jung,
Department of Physics, Brain Korea 21 Physics Research Division and
Institute of Basic Science, Sungkyunkwan University, Suwon, SOUTH
KOREA.

Copper (Cu) diffusion into low dielectric constant plasma polymerized
cyclohexane (CPCHex) thin films deposited plasma enhanced
copper vapor deposition upon annealing was investigated. Cu
diffusion was analyzed by current-voltage (LV) measurement, Rutherford
backscattering spectroscopy (RBS), and transmission electron microscopy
(TEM). From LV measurement and TEM analysis, it was revealed that CPCHex thin films were resistant to Cu
diffusion up to 400°C, while there was a notable amount of Cu
diffusion from the CPCHex thin films after 400°C annealing. RBS was
not sensitive enough to detect a small amount of Cu diffused into the
CPCHex films. Improved Cu diffusion resistance of our CPCHex thin films compared to thin films of chemically synthesized polymers is
thought to be due to high cross-linking among film-forming species of
plasma polymers.

L7.4 VAPOR PHASE DEPOSITED TOTAL X-RAY FLUORESCENCE
AS A MEANS TO STUDY COPPER DRIFT DIFFUSION IN LOW-K
DIELECTRICS. Filip Lindemans*, S. Armaras, K. Møse, IMEC,
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Reliable copper integration requires a study of the copper diffusion behavior in low-k dielectrics in order to assess the barrier
requirements. For oxide it is found that copper drift diffusion under the influence of an electrical field is annealing at temperatures
as low as 200°C. A common method to electrically investigate copper drift diffusion in dielectrics is by using high thermal
stressing in combination with capacitance voltage techniques [1]. An analytical determination of copper diffusion in dielectrics
is difficult because most methods lack a high sensitivity. An exception is vapor phase deposited total X-ray fluorescence (VPD-RIXRF).
VPD-RIXRF is primarily used to detect contaminants with a similar sensitivity as capacitance voltage measurements (nA-10
5 A/cm). The technique is applied to investigate copper diffusion through a low-k dielectric. Si/thermal oxide/low-k dielectric/3000
nm copper capacitor structures are prepared and stressed under different fields at various time and temperatures. After stressing,
both the metal and low-k dielectric are etched and the copper present in the thermal oxide is detected by VPD-RIXRF. This technique involves evaporating the thermal oxide in HF vapor resulting in a deposition of the contaminants present in the oxide on the silicon surface. Subsequently these metals are collected in
an aqueous drop. The drop is put on a Si wafer, evaporated and the copper concentration is measured with TXRF. Two types of low-k
dielectrics are examined: organic [k=2.9] and porous inorganic
[k=2.0] materials. The effective diffusion barrier between the copper
and the dielectric is investigated in a similar way. Starting from the
measured concentration of copper in the oxide, a model is presented
to estimate the copper mobility in the low-k dielectric. A good
agreement of the mobility is found between this analytical method and an electrical evaluation technique [capacitance voltage]. [1] F.
Lindemans, W. Vandervorst, K. Møse, AMC 99, pp.489-495

L7.5 EFFECTS OF CURING TEMPERATURE AND THICKNESS ON
THE THERMAL CONDUCTIVITY OF HYDROGEN
SILSESQUIOXANE THIN FILMS. Hsin Wang, High Temperature
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As the minimum geometry in integrated circuits (ICs) continues to
shrink to the 0.18-0.35 μm range, low k dielectric materials have to be
implemented to reduce the delay due to the line-to-line cross talk, and
to increase the signal propagation speed. Among the available low k
materials, materials are either containing pores in the films or having
less polymer groups in their structure to achieve lower k. While
implementing porous low k materials in the IC devices, one of the
reliability concerns for these materials is thermal conductivity because
porous low k have lower thermal conductivity than those of
non-porous films do. Hydrogen silsesquioxane (HSQ), which has k >
2.9 due to its porous structure, has been successfully integrated in
manufacturing processes. The chemical structure of HSQ is
[HS(OCH)2]n before cured and the Si-H bond in HSQ dissociates and
its cage-like structure is rearranged into a network structure when
thermally processed. It has been reported that the HSQ film
properties are strongly dependent on curing temperature and process
temperature. Therefore, it is very important to understand the
relationship between structure and thermal conductivity to ensure the
reliability of HSQ in IC manufacturing. In this study, 3-omega
method was used to measure the thermal conductivity of HSQ films
cured at different temperatures. The impact of HSQ structure change
on thermal conductivity and other properties will be reported.

L7.6 LOW-K DIELECTRICS FROM PULSED-PLASMA CVD OF
ORGANOSILICONE PRECURSORS. David D. Burley, Karen K.
Gleason, Massachusetts Institute of Technology, Dept. of Chemical
Engineering, Cambridge, MA.

Thin films produced by pulsed-plasma CVD of organosilicone
precursors are promising candidates for use as low dielectric
materials. In this paper, we consider the use of a variety of precursors and
mixtures for the production of low-k organosilicon (OS,
SiO:C:H) thin films. Specifically, we examine the effect of duty cycle (plasm on time/total time) and precursor identity on the final film structure and optical properties. Pulses-alone control over the film composition as compared to continuous plasma CVD. We have deposited films under both pulsed-plasma conditions and continuous plasma conditions at the same equivalent power. Films deposited under continuous plasma conditions often exhibit a higher degree of powder formation as well as structural moieties, such as methylene groups, that are not present in films deposited under equivalent conditions. Pulsed-plasma CVD also allows the retention of some of the original molecular structure in the films. The sensitivity of the deposited films to temperature and plasma power was tested using a Fourier Transform Infrared Spectroscopy (FTIR) and 29Si Nuclear Magnetic Resonance (NMR) analysis. Additionally, it has been observed that the sticking coefficient in the film varies linearly with the duty cycle for these precursors. Growth rates for the films varied linearly with duty cycle, up to the point at which powder formation became appreciable. Index of refraction of the films varied between 1.43 and 1.47, depending upon the nature of the precursor. Another aspect of this study is the stability of the deposited films. Thermal stability was tested in a custom-built apparatus that heated the films to approximately 400°C under nitrogen for one hour. Thickness changes were measured using interferometry. Film retention rates, as measured by ellipsometry pre- and post-anneal, ranged between 80% and 98%, and were strongly related to precursor identity.

L7.7 NOVEL METHOD OF ESTIMATING DIELECTRIC CONSTANT FOR LOW-k MATERIALS: Tatsuya Fukuda, Nobuko Ao, Azuma Matsuura, Hiroshi Matsuura, Sumitsu, Association of Super-advanced Electronics Technologies, Yokohama, JAPAN.

This study is part of a five-year Japanese national project to develop multi-level interconnect processes using ultralow-k materials. Before the material design is tackled, it is important to obtain an estimate of the dielectric constant for novel materials. A theoretical treatment of dielectrics has been devised. The dielectric constant can be broken down into three components: electronic, ionic and orientational. For L16, the frequency of interest is less than a few GHz. So, all three components must be considered in estimating the dielectric constant. Here, the key point is to treat materials as collections of oscillators and ions. The electronic component is described in terms of the molecular polarizability. Since the ionic polarization is based on ionic oscillations, it must be described in terms of the sum of the oscillation strengths, \( E_j \), which in turn are related to the derivative of the dipole moment with respect to a normal coordinate. Therefore, \( E_j \) must be related to the absolute IR intensity of the band. In order to treat the condensed phas e, a correction is needed for the local electric field. Here we assume that: the component terms are independent; the temperature is high enough; the frequency of interest is \( \sim 1 \text{ GHz} \times (0.03 \text{ cm}^{-1}) \) and is much lower than the angular frequency of the oscillators. To obtain the relationship between the absolute IR intensity and the oscillation strength, we take the imaginary part of the dielectric constant. The integral of the imaginary part is written in terms of the absolute intensity, \( A_j \). On the other hand, the integral of the imaginary part can be written in terms of oscillation strength. Based on the above assumptions and procedures, a theoretical expression for the component terms is written. The electronic component is obtained by sum of atomic or bond refractions, ionic component is obtained by IR intensities and orientational component is obtained by sum of dipole moments. The data are found in many places in the literature. The sum of these contributions was found to be in good agreement with the value determined by C-V measurement. This demonstrates the validity of our estimation method. Acknowledgments: This work was performed under the management of ASET in a MITI R&D program supported by NEDO.

L7.8 THE EFFECT OF POST-PLASMA TREATMENT ON THE PROPERTIES OF FLUORINATED AMORPHOUS CARBON FILMS AND THE CRYSTALLINITY OF Cu AND Ta IN Cu/Ta/A-C4F/Si MULTILAYER. Sung-Hoon Yoon, Seok Woo Hong, Hanyang University, Division of MSE, Seoul, KOREA; Chong-Hee Shin, Hanyang University, Division of Nano-Structure Semiconductor Engineering, Seoul, KOREA; Jong-Woo Park, Hanyang University, Division of MSE, Seoul, KOREA.

The effect of post plasma treatment on the properties of fluorinated amorphous carbon (A-C4F) films and the crystallinity of Cu and Ta in Cu/Ta/A-C4F/Si multilayer. In this study, A-C4F films were prepared by an electron cyclotron resonance chemical vapor deposition (ECR-CVD) system, and Cu and Ta on the pre-deposited 500Å thick hydrogenated amorphous carbon (A-C) film. The post-plasma treatment of A-C4F films was carried out using H2 plasma with various plasma treatment powers (150~700 W) and times (0~300s) after deposition with a turbo molecular pump. During the plasma treatment, 20sccm H2 gas was introduced into a plasma chamber. Diffusion barrier of tantalum with a thickness 200Å and 300Å copper seed layer were sputtered on the A-C4F film. Copper was electrodeposited on Cu and Ta film by another CVD X-ray photoelectron spectroscopy (XPS) was taken to investigate changes in surface chemical composition. The leakage current density and the dielectric constant of the A-C4F films were investigated UV and C-V characteristics using in an FC structure. The capacitance of Cu and Ta films were obtained using a four-point probe measurement. The X-ray crystallographic orientations of Ta and Cu films were measured using an X-ray diffractometer (XRD). The surface energy of A-C4F films was evaluated by contact angle measurement in deionized water. From this study, it was found that the plasma treatment of A-C4F films produce more reactive surfaces and affect the fluorine concentration of the surface, the structure of chemical bonding and electric properties.

L7.9 EFFECT OF STRESS STATE ON THE ADHESION OF A POROUS LOW-k DIELECTRIC. Michael W. Lane, Kenneth P. Rodbell and Kenneth Wu, IBM T.J. Watson Research Center, Yorktown Heights, NY; Wilf Volkson and Robert D. Miller, IBM Almaden Research Center, San Jose, CA.

The drive for faster interconnects dictates that dielectric materials which separate the active metal lines must have a dielectric constant, \( k \), approaching that of air \((k = 1.0)\). To this end, dielectrics which contain embedded voids have been proposed. The net effect of these voids is to average the dielectric constant of air and the matrix material. An outstanding issue when considering these porous dielectrics is how they will behave under different stress conditions. Stress states arise in interconnect device structures due to mismatches in the coefficient of thermal expansion and elastic properties of the materials. These factors, along with the complex geometries employed in interconnects and the processing steps required to obtain devices (such as chemical mechanical polishing), may lead to complex stress states that vary from point to point in the device dependent on the local geometry. Therefore, no single adhesion value will characterize the material as it is likely to experience stress states ranging from pure shear to pure tension. Accordingly, a fracture mechanics based test methodology has been implemented to measure the adhesion of porous MSQ films from pure shear to pure normal loads. The reaction path was determined by changing the stress state from pure shear to pure tension. Furthermore, the delamination path was found only to depend on the type of stress (normal or shear) but also the sign of the shear stress (positive or negative). Fracture paths were characterized by AFM and EBD.

L7.10 INVESTIGATION OF N2 PLASMA EFFECTS ON THE DENSITY PROFILE OF HYDROGEN SILSESQUIXASNE THIN FILMS. H.J. Lee, E.K. Lin, W.L. Wu, B.M. Farnoni, National Institute of Standards and Technology, Polymer Division, Gaithersburg, MD; J.K. Lin, Y.L. Cheng, Y.L. Wang, Taiwan Semiconductor Manufacturing Co., Hsin-Chu, TAIWAN; H.C. Liu, Semiconductor Fabrication Materials KKC, Dow Corning, Miiland, MI; M.S. Feng, C.C. Chao, National Chiao-Tung University, Hsin-Chu, TAIWAN.

Materials with low dielectric constant (low-k) have attracted much interest because they can reduce RC delay, which becomes a limiting factor in improving device performance. One of the low-k candidates is the commercially available silicone-based hydrogen silsesquioxane (HSQ) resin because of its excellent planarization and gap fill capabilities. However, the integration of both copper lines and low-k dielectrics still has several technical problems such as reducing copper diffusion, decreasing the leakage current, suppressing water uptake, and avoiding damage during patterning in IC applications. Many of these problems can be addressed through processing modifications to increase the surface density of an HSQ film. Although this addresses some problems, a densified surface layer also increases the effective dielectric constant of film. To this end, both the semiconductor industry would like to precisely control the thickness of the densified dielectric layer. To reach this goal, it is essential to develop an accurate analytic technique to measure the thickness of the densified dielectric layer. In this work, we demonstrate the use of specular X-ray reflectivity (SXR) as a powerful tool to measure the density profile of HSQ films treated with N2 plasma varying processing and exposure time. The importance of the N2 plasma treatment on the chemical bonding structures is also investigated using Fourier transform infrared (FTIR) spectroscopy. The SXR data indicated that the density profile of an untreated HSQ film is not uniform. Plasma treatment results in a densified surface layer film and an increase in surface roughness. The thickness of the densified layer increased with both plasma power and plasma exposure time. The SXR data show that the plasma converts the HSQ structure into a SiO:H structure and are consistent with the densification observed in the SXR measurements.
L7.11 CORRELATIONS BETWEEN STRUCTURAL CHARACTERISTICS AND PROCESS CONDITIONS OF HSQ BASED POROUS LOW-k THIN FILMS. Hoo-Jeong Lee, Eric K. Lin, Howard Wang, Wen-Ji Wei, National Institute of Standards and Technology, Polymer Division, Gaithersburg, MD, Thomas A. Denk, Semiconductor Fabrication Materials RCI, Dow Corning, Midland, MI.

One of the current challenges in semiconductor processing is to improve device performance while keeping the cost low. The main limiting factor in improving device performance is the signal delay through metal interconnects from the resistance, $R$, in the metal lines and the capacitance, $C$, between adjacent lines. Lowering the resistivity of the metal lines and increasing the separation of the interlayer dielectric (ILD) material could reduce this RC delay. The National Roadmap for Semiconductors indicates a need for materials with dielectric constants of 1.5 - 2.0 for dimensions below 0.13 um. Dielectric constants are effective in a material as reduced to values below 2.2 by incorporating voids (dielectric constant of 1) in the material. Several types of porous materials are being developed to replace the current ILD, silicon dioxide. Among them, hydrogen silsesquioxane (HSQ) based porous materials have been evaluated extensively because of their potential compatibility with conventional Si technology and the high strength of the backbone silicon network. The pore structure in porous thin films can seriously affect the thermo-mechanical and electrical properties of the thin film. Structural information such as the film porosity, pore size, wall density, and pore connectivity of thin films as a function of process conditions is important to improve and optimize the properties of low-k thin films. In this work, we provide results on the correlations between processing conditions of HSQ based porous low-k thin films and the resulting structural properties. Samples with different Si-H contents ranging 30% to 52% and different dielectric constant ranging from 1.8 to 2.2 were prepared. We performed the measurements of the structural properties such as porosity, average pore size, and wall density, average film density, and pore connectivity using small angle neutron scattering (SANS), high-resolution specular X-ray reflectivity (XRR), and kink scattering techniques.

L7.12 COMPOSITIONAL AND MECHANICAL STUDY ON THE LOW DIELECTRIC CONSTANT SiOC FILM. Young-Hwa Kim, Moo Sung Hwang, Hyung Joon Kim, Seoul National University, School of MSE, KOREA, Young Lee, Jeungsung Engineering Ltd, KOREA

As ultralarge scale integrated circuits (ULSIs) are reduced in size to deeper sub-micron dimension, there has been a strong demand for low dielectric constant inter-metal dielectric materials instead of SiO$_2$ that is conventionally used to improve the performance of devices, such as signal propagation delay, cross talk, and power consumption. Recently, SiOC, which is hybrid between organic and inorganic materials, is very promising inter-metal dielectric, since it has higher thermal and chemical stability than organic materials as well as low dielectric constant. Despite many researches, the reasons for increasing dielectric constant upon carbon incorporation remain under debate. Generally, it is accepted that the carbon incorporation [-CH$_3$] in the Si-O-C network results to the possibility of more and more decrease of film density results in the decrease of dielectric constant. In this investigation we focused on the fundamental relationships among the film density, composition and dielectric constant. As carbon contents incorporated in film increased, the film density and dielectric constant decreased. Also, there was the shift of G-S-O stretching mode peak in the infrared spectra of the SiOC film and we could see the similar phenomena in the fluorinated silicate glass (FGS) film. Spectroscopic ellipsometry, electronic balance, and elastic recoil detection (ERD) were used for calculation of film density. Compositions of the films were investigated by Fourier transform infrared (FTIR), x-ray photoelectron spectroscopy (XPS), and ERD. The microstructure of the SiOC films fabricated by trenching and electron microscopy (TEM) and the dielectric constant was calculated from capacitance-voltage (C-V) measurement.

L7.13 GAP FILLING AND DIELECTRIC STABILITY OF FLUORINATED SILICON DIOXIDE (FGS) IN ALUMINUM-FSG INTERCONNECTS. Young Woong Tae, Terence K. S. Wong, Nanyang Technological University, School of Electrical and Electronic Engineering, SINGAPORE, John I. Sadjino, Also See, Hung Lin, Technology Development Department, Chartered Semiconductor Manufacturing Ltd, Woodlands, SINGAPORE

For each IC generation, the continuing reduction of the metal pitch requires taller aluminum conductors so as to maintain the same resistance. This makes dielectric gap filling very challenging as the aspect ratio between the gap and the width of the metal line is gradually increased. The first generation low-k dielectric. However, the extendibility of FSG to future generations depends not only on a reduction of the FSG k value but also on its ability to fill gaps with increasingly high aspect ratio. In this paper, the gap fill capability of FGS by HDP-CVD is studied by varying the ratio of source gas flow rates, RF bias power and the deposition pressure. Aluminum lines with different heights and pitch spacing are used to study the effect of aspect ratio for different plasma conditions. The quality of the gap fill is characterized by cross section SEM and analyzed by step coverage analysis. The HDP-CVD gap fill capability is closely related to the deposition to sputter (D/S) ratio. An optimum D/S ratio allows good gap fill capability. For FGS, the gap fill consists of sputtering by argon as well as chemical etching by fluorine in the plasma. Thus, the fluorine containing gas flow can affect the D/S ratio and hence the gap fill characteristics. The reduction of gap fill is known to improve the step coverage of FSG films. The gap fill capability of the proposed gap fill process on FSG film fabrication remains unknown. FTIR and SIMS are used to evaluate the stability of FSG films deposited at low pressures.


Nanoporous inorganic materials have been extensively studied to develop the ultra low dielectric materials ($k < 2.0$) for the next generation logic chips. Poly(methylsilsesquioxane) (PMSSQ) has been one of the most promising materials. Organic/inorganic hybrids were prepared by using as received poly(cyclosiloxane) as a matrix template. Nanoporous PMSSQ films were obtained by thermally decomposing the organic polymer (porogen) in the nanolambrdics. Nanolambrdics were prepared by spinning the solution of PMSSQ and porogen in methyl isobutyl ketone (MIBK) or propylene glycol monomethyl ether methyle acetate. The compatibility between the porogen and inorganic materials is a key controlling factor to obtain the uniform size and distribution of pores in the inorganic materials. Thus, PMSSQ copolymers were synthesized and their interaction with the porogen was controlled. Dielectric properties and refractive indices ($n$) of the pure and nanoporous PMSSQ were measured by LCR meter, respectively. Dielectric constants of nanoporous PMSSQ linearly decreased with increasing amount of porogen added and the calculated porosity also showed a good correlation with the amount of porogen added. The effect of PMSSQ copolymer composition and surface treatment effect on the electrical properties will be presented.

L7.15 A NOVEL RECESSSED GATELINE EMPLOYING AN AIR-GAP LINE CROSSOVER WITH DECREASED SIGNAL DELAY IN AM-LCD PANEL. Jin-Woo Park, Wo-Jin Nam, Cheon-Hong Kim, Min-Chool Lee and Min-Koo Hie, Seoul National University, School of Electrical Engineering, Seoul, KOREA.

The large size AM-LCD requires high speed driving circuits because the signal delay of the data line due to RC delay is increased and the quality of display image is degraded. To decrease the delay of the data line, a considerable effort has been made to reduce signal delay in AM-LCD panel as well as various FPDs (Flat Panel Display). Most of previous works are concentrated to reduce resistance rather than capacitance. The purpose of our work is to report a new low-dielectric air-gap structure which decreases the capacitance between gate and data line considerably. Our new structure planarizes the air-bridge panel in order to sustain the mechanical durability of the structure without sacrificing the capacitance. The planarization is rather important in AM-LCD because rubbing or spacer processes in AM-LCD fabrication may induce the mechanical stress. The proposed structure was successfully fabricated. The key process steps are as follows. After trenching transparent quartz substrate onto metal was evaporated without photore sist stripping. The metal on photore sist was eliminated by the lift-off process in order to forming photore sist on the bottom of the oxide trench. A new photore sist layer formed by the backside-exposure technique is the sacrificial layer for forming the air-gap. It enables align the sacrificial photore sist on the recessed gate-line exactly without any microphotolithography mask. The sacrificial layer photore sist was then formed by thermal dehydrating for performing the high temperature plasma process such as a metal sputtering on the organic photore sist. The inter-layer oxide and the data-line metal was deposited on sacrificial photore sist and patterned. Finally, the sacrificial and data-line patterning photore sist was eliminated by oxygen plasma simultaneously. After fabricating, it was observed that recessed airbridge was successfully formed in the oxide trench. The planarized panel surface prevents the airbridge from coming into contact with the mechanical stress. Our experimental signal delay data shows that the proposed structure reduces the delay time by about 9 times compared with the conventional structured panel. The
proposed low-air-gap structure in the oxide trench reduces the capacitance corresponding to the low-dielectric material. The proposed processed structure that is almost plasmaized is immune to the mechanical stress.

L7.16 CORRELATION BETWEEN SURFACE MODIFICATION OF HSQ FILMS AND PHASE TRANSFORMATION OF Cu/WN BILAYERS DEPOSITED ON THE NH3 PLASMA TREATED HSQ FILMS. Dong Joung Kim, Hyun Sung Kim, Jong-Won Park, Hanyang University, Daejon, KOREA; Yong Tae Kim, Seong-H Kim, Chuan Kuan Kim, Korea Institute of Science and Technology, Semiconductor Materials Laboratory, Seoul, KOREA.

After NH3 plasma treatment of HSQ films, W+N and Cu thin films are deposited on the NH3 plasma treated HSQ films. As a result, surface roughness of W-N film becomes smoother and adhesion of the W-N to the HSQ is also stronger than that of the W-N to the non-plasma treated HSQ. Contact angle of the W-N film on the HSQ film increases 2 times from 21 to 61° after the NH3 plasma treatment. Therefore, it is concluded that surface modification of the HSQ film by the NH3 plasma treatment causes the wet-ability on the surface of HSQ film, resulting in the improvement of surface morphology and adhesion of W-N thin film. Also, a texture of the Cu is preferred oriented to [111] when the Cu film is deposited on the W-N/the NH3 plasma treated HSQ thin film. After annealing the Cu/W-N/HSQ interconnect structure at 400 °C, we have found that the Cu/W-N/HSQ Plasma treated HSQ structure is agglomerated at 600°C and the phase transformation of W-N film is significantly occurred at 700°C. However, in the case of NH3 plasma treated HSQ thin film is not agglomerated at 600°C and the W-N phase is also remained at 700°C. These results suggest that the surface of HSQ thin film modified by the NH3 plasma treatment forms a passive Si-N layer between W-N and HSQ. This passive Si-N layer acts as a diffusion barrier against inter-diffusions of N and H atoms from the W-N and HSQ films, respectively.

L7.17 LOW-DIELECTRIC CONSTANT FUNCTIONALIZED SILICA XEROGELS. Rosa A. Orozco-Torres, Haifang Dong, Jodi A. Roepach, Dennis W. Mueller, and Richard F. Reddy, Department of Materials Science, University of North Texas, Denton, TX.

Silicon thin film xerogels have excellent potential as interlayer dielectric materials needed for the next generation of electronic devices. Silicon xerogel films exhibit extremely low dielectric constants; however, thermal and chemical stabilities of these dielectric constants during semiconductor processing are of some concern. Effective low-k materials have hydrophobic surface groups that exhibit low polarizability. Adsorption of water can increase polarizability and remove low polarizable functional groups. Many silica-based xerogel systems require "capping" steps to create hydrophobic surfaces. To avoid these additional process steps in device fabrication, efforts have been made to identify single-step" xerogel precursors. One advantage of these systems is the relatively straightforward and inexpensive integration into current fabrication methods. Studies have been conducted on two systems: triethoxycyanuric acid (TEOS) and methyltrimethoxysilane (MTMS). TEOS (Methyltriethoxysilane) for low k dielectric applications because of low polarizability of the fluorine surface atom and small particle size of polymerized FTES. However, TEOS gels very rapidly and traps unreacted hydrolytic hydroxyl groups thus presenting difficulties due to water adsorption and in spin coating processing. Another hydrophobic precursor, MTMS, gels at more controlled rates; consequently, offers some control of gel nanostructure. However, the particle size of MTMS can increase rapidly during the aging and drying periods; therefore, care must be taken to prevent particle sizes from approaching IC feature sizes. Hybrid systems of TEOS and MTMS provide a balance among gel time, hydrophobicity, and dielectric properties. In addition, samples have been removed as Surface modification agents to determine if further reductions in dielectric constant can be attained. To determine which systems are best suited for IC dielectric applications, gas adsorption, FTIR, SEM, ellipsometry, and impedance measurements have been employed to describe the structures, chemical and thermal stabilities, and dielectric constants of thin film xerogel xerogels.

L7.18 NANOINDENTATION OBSERVATIONS OF POROUS MATERIALS. Eva E. Simonoy, K.P. Reddell, J.C. Hedrick, IBM Research, Yorktown Heights, NY; A. Jain, Bensalem Polytech Institute, NY.

Manufacturing of low dielectric constant thin insulating layers present a special challenge for the microelectronics industry. One of many approaches is to use porous materials. This paper discusses hardness and Young's modulus ranges for porous materials, which range from zero to 60% porosity. As an example metasiliconoxane (dendrimers) and tetraethylorthosilicate (TEOS) will be discussed. Correlations with pore size distributions will also be shown.

L7.10 EVALUATION AND COMPARISON OF TRIBOLOGICAL AND MECHANICAL PROPERTIES OF LOW-DIELECTRIC MATERIALS. A.K. Siddier, J. Mark Anthony, Center for Microelectronics Research, College of Engineering, University of South Florida, Tampa, FL.

As the minimum geometry of microelectronic devices continues to shrink, new materials with low dielectric constant are demanded by the semiconductor industry. These are mainly used as an interlayer dielectric to improve the performance of ICs by reducing parasitic delays and power requirements. Mechanical characterization of low-K materials has shown that lower K typically also means lower elastic modulus and hardness. Also the major challenges involves in chemical mechanical polishing (CMP) of these films due to the reduced modulus and cohesive strength of many low-K materials. Parallel with the improvement of the lower dielectric constant it is utmost necessary to evaluate the mechanical and tribological properties in order to successful implementation of low-k (LKD) material. The purpose of this study is to provide a comparative study of mechanical and tribological properties of low-K dielectric materials [SILK, Porous silicon, Doped silicon oxides FLARE, and others]. Mechanical properties were evaluated using MTS Nanoindenteter XP with a Berkovich indenter. Universal Micro-Tribometer was used to study the tribological properties of these films. Surface morphology and roughness of the films were also characterized by atomic force microscopy. Mechanical and tribological characteristics along with surface characterization are equally important along with the chemical and mechanical performance testing to implement low-K materials in the device.

L7.20 A METHOD OF IMPROVING DIELECTRIC CONSTANT AND ADHESION STRENGTH OF MTHYL SILSESQUIOXANE BY USING A NH3 PLASMA TREATMENT. Hyun Sung Kim, Young Tae Kim, Semiconductor Materials Laboratory, Korea Institute of Science and Technology, Cheongyoung, Seoul, KOREA; Dong Joung Kim, Hyoeyng Jeon, Division of Materials Science and Engineering, Hanyang Univ, Seongdongku, Seoul, KOREA; Sung-Hyun Cha, Kookheon Chir, School of Chemical Engineering, Seoul National Univ, Seoul, KOREA.

Low dielectric and porous thin films, such as hydrogen silsesquioxane (HSQ) and methylsilsesquioxane (MSQ) thin films, have been intensively studied as an interlayer dielectric (ILD) material for multi-level interconnection since RC time delay can be reduced by low-k. In this work, we have synthesized a MSQ material that has a relatively low k (k=2.7-3.0), an intrinsic hydrophobicity, good mechanical hardness and good thermal stability (up to 500°C). However, it is well known that generally the MSQ has poor adhesion to Cu metal and diffusion barrier thin films. Therefore, we have tried to modify the surface of MSQ films by NH3 plasma treatment to improve the adhesion. As a result, the effects of NH3 plasma treatment on electrical and physical properties of methyl silsesquioxane (MSQ) have been investigated. After the NH3 plasma treatment, the dielectric constant of the MSQ was decreased by about 20%, and the adhesion of MSQ to W diffusion barrier thin film was also improved. However, leakage current density of the treated MSQ films was increased depending on plasma treatment conditions and as increasing the plasma treatment temperature from 150 to 350°C, the leakage current density of the MSQ increased as high as three order of magnitude. In this work, we will discuss the effect of nitrogen atom bombardment to the MSQ films on reducing the dielectric constant and reactivity on the surface of the MSQ film.

L7.21 EVALUATION OF SIN AND SiC AS COPPER DIFFUSION BARRIERS. Xiaomei Bu, Liang M. Han, Joseph Xie, Wei Qin, Zhigang Mo, Jielin Xie, Shuri Wang, Be Yu, P.D. Fox, Institute of Microelectronics, SINGAPORE.

The dielectric barrier is needed to prevent copper diffusion in copper dual-damascene technology. Silicon nitride (SiN) is currently employed for this purpose. Amorphous silicon carbide (a-SiC), a new promising thin film, is being evaluated as a potential barrier to replace SiN due to excellent barrier properties that maintain high thermal stability, and low dielectric constant.

The dielectric constant of a-SiC thin film has been prepared by plasma deposition of methylsilane precursor. RI, dielectric constant and FTIR of SiCN films have been measured. Significant copper signals were detected by TAP measurement for the surface of a-deposited SiC and SiCN thin films on Cu substrates. It was confirmed that the copper contamination on the surface of a-deposited dielectric solely comes
then hit either a pre-activated surface, or the droplets themselves are activated at the surface. The subsequent chemical reaction yields the desired chemical composition in the deposited feature, which is either a neat liquid of a precursor material or volatile solutions containing the precursor enabling low temperature decomposition and giving off volatile byproducts during the conversion reaction. These are removed using vacuum or a constant flow of inert carrier gas. Feature sizes, material morphology, rheology, electrical performance, and morphological and chemical stability are controlled by the choice of material, inkjet delivery parameters, and the chemistry involved in the conversion process. Surface chemical and microscopic analyses of the printed deposits are also presented. Our findings represent an important step towards the manufacture of electronic devices by entirely non-photographic means.

L8.3 ELECTROLESS COPPER DEPOSITION FOR SEEDING LAYER FOR COPPER INTERCONNECT METALIZATION OF ULSI THIN FILMS

Wang Ling Ge, Kee Taha Tan, Min Sin Tan, Ku Yu Lu, Nanyang Technology University, School of Electrical and Electronic Engineering, Microelectronics Center, Micro-Fabrication Laboratory, SINGAPORE.

PVD technologies are widely used for Cu seeding layer deposition but the step coverage on deep via/trench is questionable for sub-0.15um technology. CVD Cu deposition technology is thus in active research to replace the PVD methods for Cu seeding layer formation. We propose the ElectroleSS (EL) copper technology as an alternative deposition technology to CVD Cu for seeding layer formation. The resistivity, morphology, texture, grain size, roughness, microstructure and adhesion of the electrosseed Cu seeding layer was studied. Excellent step coverage is achieved with the EL-Cu technology. EL-Cu with very high (111) texture can be obtained using Cu flash layer. A comparative study was also performed to study the properties of Cu seeding layers deposited by the CVD and EL methods. Cu and EL-Cu Seeding Layers are quite comparable in term of physical properties like grain size (0.15-0.2um), roughness (<15nm) and resistivity (~2 uOmega). Unlike the CVD-Cu seeding layer process to which is known for very poor adhesion to most substrate, we demonstrate that EL-Cu film has good adhesion on barrier. ElectroleSS copper deposition method has great potential as a copper seeding scheme for ULSI copper metallization due to very low low cost (much lower than CVD Cu) and excellent step coverage (comparable to CVD process). Being a wet process, EL-Cu technology offers the advantage of easy integration with existing Cu plating process and allows both EL-Cu seeding and EP (electropless) Cu plating processes to be integrated on the same platform. Moreover, EL-Cu is deposited at a much lower temperature of around 70 deg, compared to the typical CVD process temperature of 200-300deg. The low temperature processing in EL-Cu technology enables compatibility with most lowk dielectric.

L8.4 H-Assisted Plasma CVD Using Cu(hfac)2 and Cu/EDMDI2 Mixtures

M. Shiratani, Masahiro Shiratani, Hiroki Jin, Isao Okawa, TohokuUniversity, Sendai, Japan.

Full composition of high-purity copper in submicrometer-size particles is a key requirement in formation of metal interconnects carrying signals in ULSI. For this interconnection application, we have developed an H-assisted plasma CVD reactor (HAPCVD) which is equipped with an H atom source. The H atom reactor can realize the control of quality and conformity in Cu film deposition, since H irradiation is effective in purifying the Cu films, increasing the grain size, and reducing the surface roughness, while the decrease in dissolution degree of Cu source materials leads to realize conformal deposition in fine tresses. When using Cu(hfac)2 as the source materials, Cu(hfac) is identified as the radical mainly contributing to the deposition. Based on a series of our results, we propose a model in which Cu(hfac) is and H react on surface Cu to form Cu(hfac)2 and H2, which have demonstrated conformal deposition of smooth high-purity Cu films (about 100%) of 30 nm in thickness and 1.9a.m.c in resistivity in trenches using the HAPCVD.

Moreover, we use new Cu source of Cu(EDMDI)2 which does not contain undesirable element P for obtaining good adhesion to barrier metal such as TaN and W. Films deposited using Cu(EDMDI)2 shows better adhesion strength than those obtained using Cu(hfac)2.


The properties of electroplated copper films have been found to alter along the time after the plating. This phenomenon is called self-annealing. A new phenomenon associated with microstructure changes and tensile stress release. Effects of DC and pulse current with the use of different barriers on the self-annealing behavior of the ECP Cu films have been investigated. The thickness of Cu films was deposited using different DC process with plating current density of 7, 18, 35, and 65mA/cm², or using pulse current. They were also grown on different barriers (Ti, TaN, and Ta/TaN) for comparison. After the deposition, the properties of these Cu films were investigated with FEM, four-probe probe, AFM, MetalPULSE and SEM for analyzing their stress, sheet resistance (Rs), surface topography, thickness, roughness and grain size. The results indicate that Rs had a most distinct change for all the wafers during the self-annealing process, which declined greatly strongly on the employed plating current profile. When using DC current, applying higher current density lead to that Rs began to decrease earlier in a faster rate and to a larger percentage. When using pulse current, however, the measured Rs decreased much slower and only reduced by about 3% in one week after the deposition. The effects of different barriers on the self-annealing, on the other hand, show that Rs decreased exhibited a similar trend as in the case of applying higher DC current density. These changes, based on SEM analysis, can be attributed to the increase of the Cu grain sizes.

**L8.8**

**HIGHLY (111) ORIENTED AI THIN FILMS BY ION-PLATING METHOD USING DISCHARGE PLASMA** Shin Masui, Kinio Kinoshita, Suamii Sakuragi, Toshihiko Kudo, Nihon University Center, JAPAN, Shuji Takayama, Hosei Univ. Dept of System and Control Engineering, Koganei, Tokyo, JAPAN.

Ion plating (IP) method using arc discharge plasma was applied to deposition of Al thin films for interconnects. The high energy electron beam in this discharge plasma heats Al metal, vaporize and highly ionize. The resultant AI ions are accelerated toward a glass substrate due to the plasma potential and Al this films are formed with energetically impinging of AI ions on the substrate. In this method highly oriented Al(111) films were obtained. The characteristics of IP-Al films are shown comparing with those obtained by magnetron sputtering (MS). According to X-ray diffraction (XRD), the (111) peak intensity of IP-Al films is 10 times higher than that of MS-Al films at least, and except for the (111) peak other peaks were observed in the XRD pattern of IP-Al films. In ion bombardment as a pre-treatment was found to be effective for narrowing the half-width (down to 2.4 deg) of rocking curve at the (111) peak. Whereas, the MS-Al films have several weak XRD peaks and broad rocking curves. Furthermore it was found that the surface roughness of IP-Al films (Ra=2.9nm) is smaller than that of MS-Al films (Ra=2.9nm) under AFM observation and the IP-Al films have much more resistance to abnormal grain growth with the post-treatment of the furnace annealing up to 620°C. In order to prevent the abnormal grain growth and abnormal grain growth in interconnects, the advantage of the (111) preferred orientation have been reported by many papers. IP-Al films have vast potential for this purpose but the mechanism of the growing film has not clarified yet. We will discuss the use of (111) oriented IP-Al films in terms of the ion energy and plasma irradiation during deposition.

**L8.7**

**INDEPENDENT MEASUREMENT OF COPPER FILM THICKNESS AND RESISTIVITY BY OPTO-ACOUSTIC TRANSIENT GRATING TECHNIQUE** A.A. Martin, I. Gostein, Philips Analytical, Natick, MA, John A. Rogers, Glen Kovacs, Bell Laboratories, Lucent Technologies, Murray Hill, NJ.

Conventional techniques for electrical resistivity measurements such as four-point are not non-destructive, and are not independent of the sheet resistance i.e. the product of the resistivity and film thickness. In this presentation, we show that a non-contact and non-destructive optical technique called Impulse Stimulated Thermal Scattering (ISTS) is capable of measuring film thickness and resistivity independently. In this technique, lasers are used to impulsively generate and detect both surface acoustic waves and cold thermally-induced displacement pattern at the sample surface. The measurement is acquired by the film's thermal properties and mechanical properties while the decay time of the thermal grating is dependent on the film's thermal diffusivity. The latter is well correlated with the electrical conductivity in good conductors such as copper. Thus by measuring the optical frequency and thermal grating decay time one can extract both thickness and resistivity of a copper film. The concept has been demonstrated on a set of physical vapor deposited (PVD) Cu samples fabricated under different deposition conditions. The results obtained with the opto-acoustic technique correlated well with resistivity and thickness data obtained by a combination of four-probe and grating-incidence X-ray reflectivity measurements.

**L8.8**

**SPUTTERED Ta-Si DIFFUSION BARRIER IN Cu/LowK METALLIZATION** Shih-Chun Huang*, Yu-Jen Chen**, Ling-Jung Guo**, and Fen-Shan Huang**, Institute of Electronics Engineering, National Tsing-Hua University, TAS, Science Center, National Tsing-Hua University, Hsin-Chu, TAIWAN.

As the low k dielectrics will be used in ULSI process, the fabrication temperature will reduced, so the requirement of the thermal stable ability of diffusion barrier. In this report, sputtered Ta-Si amorphous film was investigated as a barrier material. The TaSi film was deposited by sputtering of TaSi target in Ar gas. The resistivity of the TaSi film was about 200 ohm.cm, 20%, and they were used for understanding the crystalline structure, chemical structure, and atomic composition. The thermal stability can be studied from C-V test. The MOS capacitors of sputtered Cu or electroplating Cu/Ta-Si(35nm)/methylsilaneoxide film were annealed at the temperature from 350°C to 500°C for 30 min in nitrogen ambient. The MOS and porous SiO2 films with thickness 200 nm were spin-coated on the Si wafer. The dielectric constant of these films was about 2.6. From the flat band shift and the variation of inversion capacitance, the diffusion performance can be evaluated. The thermal stable temperature can be up to 450°C. We also compare the barrier properties of amorphous Ta-Si film with that of poly-TaSi film. Finally, SIMS profiles of the above MOS capacitors are correlated to the electrical test.

**L8.9**

**BEHAVIOUR OF ELECTROPLATED COPPER FILM IN THE EPCu/IMPt/Cu/IMPt/SiO2/S MULTILAYER STRUCTURE** Khim Nhuong Le**, Y. K. Lee**, H. L. Song**, O. Oskowicz** School of Materials Engineering, Nanyang Technological University, SINGAPORE, School of Physics, National University of Singapore, SINGAPORE.

Electroplated Cu film on a thin seed layer of IMPt deposited Cu has been investigated in the EPCu/IMPt/Cu/IMPt/SiO2/S multilayer structure. Khim Nhuong Le**, Y. K. Lee**, H. L. Song**, O. Oskowicz** School of Materials Engineering, Nanyang Technological University, SINGAPORE, School of Physics, National University of Singapore, SINGAPORE.

Electroplated Cu film on a thin seed layer of IMPt deposited Cu has been investigated in the EPCu/IMPt/Cu/IMPt/SiO2/S multilayer structure. Khim Nhuong Le**, Y. K. Lee**, H. L. Song**, O. Oskowicz** School of Materials Engineering, Nanyang Technological University, SINGAPORE, School of Physics, National University of Singapore, SINGAPORE.

Electroplated Cu film on a thin seed layer of IMPt deposited Cu has been investigated in the EPCu/IMPt/Cu/IMPt/SiO2/S multilayer structure. Khim Nhuong Le**, Y. K. Lee**, H. L. Song**, O. Oskowicz** School of Materials Engineering, Nanyang Technological University, SINGAPORE, School of Physics, National University of Singapore, SINGAPORE.
backscattering spectroscopy (RBS) from films deposited on glassy carbon, was around WN$_2$O$_8$. The oxygen arises from impurities in the deposition chamber and its concentration is being reduced by the addition of purifiers and a lock-tap. The growth rate (number of atoms deposited per unit area and unit time), also found from RBS, increased with the flow rate of ammonia. In the absence of ammonia, no film was detected. The thicknesses and step coverage were determined by scanning electron microscopy. The step coverage was essentially 100% in both aspect ratio of 5:1. The films were amorphous by X-ray diffraction. Electrical resistivity measurements and copper diffusion barrier properties will be reported.

L8.15
COMPARATIVE GRAIN SIZE DISTRIBUTION AND GRAIN ORIENTATION DISTRIBUTION MEASUREMENTS FROM EBSD AND A NEW XRTECHNIQUE ON COPPER FILMS AND INTERCONNECT LINES. Kris Kozak, Dave Kurtz, Roger Martin, HyperNex, Inc., Stone College, PA.

In recent years electron backscatter diffraction (EBSD) has emerged as a highly useful technique for quantitative analysis of grain orientation distribution and grain size distribution in thin films. However, the sequential grain-by-grain analysis protocol, combined with the requirement for carefully polished, unscraped samples places some limits on large-scale analysis with EBSD. An XRTE technique has been developed which can simultaneously monitor grain size distributions and grain orientation distributions on a microscale (20-300 micron diameter beam) compared to EBSD (sub-micron beam diameter) without the need for over-layer removal. The technique relies on the fact that continuous Deluge rings transition to discontinuous spots as a smaller beam size is used to illuminate fewer grains. Multiple partial Deluge rings that are discontinuous (spotty) can be collected from an area detector and used to generate an orientation distribution function from which texture volume fractions can be redisplayed. The grain size distribution is determined from the intensity distribution of the diffraction spots, each spot representing one grain. Comparative measurement examples for NbN and the XRTE technique will be provided. Good correlation for both grain size and grain orientation has been demonstrated between the two techniques.

L8.16
X-RAY POLE FIGURE ANALYSIS OF PREFERRED IN-PLANE ORIENTATION IN INLAID COPPER INTERCONNECT LINES. Paul R. Besner, Technology Development Group, Advanced Micro Devices, Inc., Austin, TX; Denise Winter, Richard Ortega, AMI Laboratories-Rigaku, The Woodlands, TX; and Ehrenfried Zscheischler, Werner Blum, Advanced Micro Devices Szony Manufacturing GmbH, Dresden, GERMANY.

The crystallographic texture of inlaid Cu lines has been quantified by X-rays (111), (110) and (100) pole figure analysis using X-Ray diffraction as a function of anneal temperature. Cu lines were 0.45 μm deep and 0.35, 0.7, and 1.0 μm wide were produced using conventional fabrication techniques for inlaid Cu lines. The crystallographic texture is predominantly (111) out-of-plane with sidewall-muscovitated grains in narrow lines. It will be shown that the (111) grains nucleated from the trench bottom have a preferred in-plane orientation with the [110] direction parallel to the sidewall, and that the sidewall-muscovitated grains have a preferred in-plane orientation as well, with the normal direction parallel to the trench bottom. The preferred in-plane orientation results from a reduction in the surface energy by the Cu grains. A 5 degree splitting of the X-ray diffraction peaks from sidewall-muscovitated grains will be shown, suggesting that the sidewall-muscovitated (111) grains are tilted by 5 degrees with respect to normal to the trench bottom. It will be shown that the 5 degree tilt results of the non-vertical trench sidewalls. Ako, the texture will be shown to be independent of when the annal is done (pre or post CMP) and the anneal temperature.

L8.17
A ROLE OF INTERFACE IMPURITIES ON ADHESION BEHAVIOR OF CuV COPPER FILMS. Young Sik Kim and Yukihiko Shimokogi, Department of Materials Engineering, University of Tokyo, Tokyo, JAPAN.

Chemical Vapor Deposition (CVD) is considered an important technology for the deposition of copper (Cu) thin films during the fabrication of future ULSI devices primarily due to excellent step coverage. In the near future, Cu-CVD process will be combined in seed or filling layer fabrication with electroplating. However, CVD Cu films deposited on common barrier layers have a poor adhesion, which influences chemical mechanical polishing (CMP) process, reliability problem and contact resistance. Thus, reliable interfacial bonding of Cu seed layer deposited by CVD is a critical factor for future application. We describe the adhesion characterization of CVD Cu films deposited on various barrier layers depending on the type of substrate, the barrier preparation process, the interface residual and the surface roughness. Adhesion strength of the Cu films on CVD TiN prepared by laser ablation due to the formation of Cu(OH)$_2$ at the interface. The X-ray photoelectron spectroscopy (XPS) results revealed that the formation of Cu(OH)$_2$ was considered to improve the adhesion strength and to be facilitated by unstable intermediate components such as Cu$_2$O on the interface. Increased surface roughness of CVD TiN films were considered to
Cu hillocks have often been observed as a consequence of electromigration in Cu damascene interconnects passivated with SiO₂. In this study, we have compared, for the first time, lifetimes deduced from hillock formation with that obtained by lifetime to voiding. The Cu damascene lines are fabricated with CVD copper deposited on CVD TiN (10 nm), encapsulated with SiN (40 nm) and passivated with SiO₂ (1 μm). The test structure used a straight stripe (test line, length 400 μm), with voltage and current contact pads at both ends. Two line widths (3 μm and 0.5 μm) provided respectively polygrain or quasi-bamboo Cu microstructure. The test line was surrounded on both sides, at the same and at upper metal levels, by other metal lines acting as extraction detectors. The failure criterion for void formation was set to 10% test line resistance increase while failure criterion for hillock formation was the occurrence of a 0.1 mA current flowing in the extraction detector circuit subjected to 2 V bias. For all test conditions (oven temperatures set to 250, 300 and 350°C and current densities set to 4 and 6 MA/cm²), extrusion failure mode always occurred significantly before void failure. The time to failure of each mode was compared with the Black methodology using Weibull analysis. Activation energy of void formation was 0.82 eV [resp. 1.03 eV] for wide lines [resp narrow lines]. These values are consistent with SEM observation showing grain boundary diffusion in polygrain microstructure and interface diffusion in quasi-bamboo microstructure. Moreover, for both linewidths, activation energy of hillock formation was lower than the value obtained for voids formation. FIB cross-section showed the typical shape of hillocks and help us to propose hypothesis to explain this failure mechanism. It is concluded that hillock's failure mode should be taken into account in electromigration design rules because it provided extrapolated lifetimes 10 times lower than the value calculated with void failure mode. This work has been carried out within the CCMC consortium between CEA-LETI and STMicroelectronics.

10.4 INVESTIGATING THE MICROSTRUCTURE-RELIABILITY RELATIONSHIP IN Cu DAMASCENE LINES. David P. Field, Washington State University, School of Mechanical and Materials Engineering, Pullman, WA; Dietmar Borrmann, Huntsville (Jonathan H.) Tong, Connect Systems, Inc., Newport Beach, CA.

The continuing performance increase of integrated circuit structures has necessitated the implementation of Cu in interconnect material. The present work focuses upon characterizing the microstructure of Cu damascene lines and investigating the reliability of the test structures as a function of microstructural characteristics. The lines were fabricated using various processing paths including self-annealing and high temperature annealing. The microstructures were characterized using focused ion beam imaging, transmission electron microscopy and orientation imaging microscopy techniques. The differences in microstructure were correlated with reliability of the test structures as determined from accelerated electromigration tests. It is apparent that the microstructure of Cu damascene lines can be altered substantially by changing the fabrication process. The grain morphology is of primary importance in predicting reliability from the microstructure. This will be discussed in connection with defining microstructural parameters for use in modeling the electromigration behavior of Cu damascene structures.

10.5 FORMATION OF A STRONG (011) TEXTURE IN THERMALLY CYCLED COPPER THIN FILMS. M. Wada, J. Koike, K. Murayama, Tohoku University, Dept. of Materials Science, Sendai, JAPAN.

Cu is a new interconnect material for semiconductor devices. Electromigration (EM) has been known to be a major reliability problem during device operation. In the case of Al interconnects, less than 1% crystalline films were more resistant against EM because of the possible formation of special grain boundaries with low atomic diffusivity. However, Cu thin films, little information is available for textiles and grain-boundary structure. The aim of our study is to study the formation of this texture by various heat treatments. Samples were composed of the layers of Cu 5000 nm / Ta 20 nm / Si (110) wafer. The Ta and Cu layers were deposited by RF magnetron sputtering. Some samples were heated to 725 K immediately after deposition, while others were kept at room temperature for one month before thermal cycling was performed. Texture information and grain-boundary structure type were determined by EBSP. Microstructure was observed by SEM and TEM. The as-deposited films had a texture <111> texture. When thermal cycling was performed immediately after deposition, large grains of the <110> orientation were formed in the most part of the film. Thermally processed for 30 minutes. In addition, approximately 95% of all grain boundaries of this film was either small-angle boundaries or special boundaries of a low atomic diffusivity. The recrystallization of the <110> grains was found to occur by twinning of the <221> grains. The subsequent selected growth of the <100> grains was attributed to much smaller biaxial elastic strain energy for the <100> grains than for other low-index grains. In contrast, the <111> texture was stabilized in the samples kept at room-temperature. Only small portion of the <992> was converted to the <110> grains by subsequent thermal cycling. The present work offers a possibility of producing new Cu interconnects with excellent EM and SM resistance.

10.6 EFFECTS OF CONTACT RESISTANCE ON CURRENT

Ryu, W.G. Lee, Hyundai Electronics Industries Co., Ltd., SYSTEM IC R&D Center, Cheongju, KOREA.

Dependence of the electromigration, electrical resistance and reliability of aluminum interconnections on the wide range of values is investigated. Aluminum metal stack structures are investigated using the CVD Cu. The Cu was deposited to examine the effect of impurities more clearly. The adhesion characteristic will be discussed with using XPS in detail.
CROWDING AND CRITICAL PRODUCT OF ELECTRO-MIGRATION IN BLECH STRUCTURES. Everett C. C. Yeh, K.N. Tu, Dept. of Materials Science and Engineering, UCLA, Los Angeles, CA.

In using Blech structures to study electromigration, current density has been assumed to be the same in the similar sets of short strips deposited on an under-layer. But this is not true owing to the existence of contact resistance between the strips and the under-layer. It has been shown experimentally that the contact resistance between strips and under-layer is very sensitive to the fabrication process. High contact resistance reduces the maximum current in the strip. Also, it diffuses the current decaying between the strip and under-layer on a wide spreading window. In other words, the spreading of the current in the direction perpendicular to the current flow is uniform in Blech structures. In this work, we simulate these phenomena of current reduction and spreading in terms of contact resistance and film thickness, both of which are key factors controlling current distribution in a Blech structure. We explore their effects on back stress and incubation time of void formation in short strips. We demonstrate these effects by the discrepancy in critical product measurements found in experiments using similar Blech structures.

L0.7 INTEGRATION AND ELECTROMIGRATION RELIABILITY OF CuPVD ALUMINUM INTERCONNECTS. Won Jun Lee, Jong Joo Kim, Suk Jee Lee, Jong Yoon Yoon, Heung Lok Park, Hyundai Electronics, Memory R&D Div, Kyonggi-do, KOREA; Sik Kyun Rha, Theion National Univ of Technology, Dept of Materials Engineering, Theion, KOREA.

CuPVD Al process is promising as the metallization method in low-cost dynamic random access memory (DRAM) manufacturing, because it forms plugs and wires simultaneously. In this study, the CuPVD AI process was successfully integrated into a 4-gigabit DRAM process flow, and its electromigration reliability was compared with that of the conventional W plug process. The multilayer film of MoCVD Ti/TiN/AlN/PVD Ti was used as the underlayer of CuPVD Al from dimethylaluminum hydride (DMAH), and thin CuPVD Al film functioned as an effective wetting layer for the subsequent PVD Al reflow. Sub-quarter-micron via with high aspect ratio (up to 10) was completely filled at temperatures below 400°C. The CuPVD Al plug process exhibited a via resistance lower than that of the conventional W plug process. The effect of process parameters on via resistance was examined. The CuPVD Al plug process showed different electromigration behavior than that of the W plug process. Most electromigration failures were catastrophic and they occurred as the Al plugs for the CuPVD Al samples, whereas the resistance of the electromigration test structure increased gradually until the failure time and voids were observed at the Al wires underneath the W stud for the W plug samples. The difference in the electromigration behavior of the Al plug samples and the W plug samples was explained by the structural and geometrical difference between them. Finally, the application of CuPVD AI process to the dual damascene Al process flow will be also presented.

L0.8 COMPARISON OF GRAIN BOUNDARY DIHEDRAL ANGLE DISTRIBUTIONS IN Cu AND Al THIN FILMS FABRICATED BY VARIOUS DEPOSITION METHODS. Jong-Min Paik, Min-Seung Yoon, Young-Chang Joo, Seoul National University, School of Materials, Seoul, KOREA; Young-Joon Park, Korea Institute of Science and Technology, Seoul, KOREA.

In electroplated copper films used in ULSI interconnects, the evolution of microstructure at room temperature known as self-annealing has been observed. Since self-annealing is not observed in the metal films fabricated by CVD or PVD methods, self-annealing seems to be related to the inherent characteristics of electroplated copper. In order to understand the characteristics of electroplated copper, we compared the distribution of dihedral angles at the grain boundary triple junctions of electroplated copper films with those of sputtered copper and aluminum films. Textures and grain size distributions were analyzed as well. For electroplated copper films, FWHH (Full Width at Half Maximum) of dihedral angle distribution was significantly larger (67.3°) than those of annealed electroplated copper (41.9°), sputtered copper (42.6°) and aluminum (35.5°). Simulation on dihedral angle distribution shows that the exceptionally large FWHH of electroplated copper films is due to the large deviation in the grain boundary energies, and this may suggest grain boundaries of electroplated Cu films are in the singular states. In a system where singular grain boundaries exist, abnormal grain growth has been observed as in the case of self-annealing. The detailed observation of grain boundaries of electroplated Cu films and the possible origin for singularity in grain boundaries are discussed.

L0.9 EFFECTS OF BOUNDARY CONDITIONS AND ANISOTROPY ON SAMPLES LOADED IN FOUR-POINT BENDING. S.K. Kakkar, Columbia University, Department of Applied Physics and Applied Mathematics, Program in Materials Science, New York, NY; I.C. Noyan, IBM Research Division, Yorktown Heights, NY.

Four-point bending, a technique often employed for loading specimens to known stress levels, is especially appropriate for testing brittle samples which are difficult to pull in uniform tension. This method has found application in the field of electromigration. The problem of the electromigration of voids is the loading of single crystal specimens for VLSI. Typically, in these problems, 1-D bending solutions which assume material isotropy are employed [1]. Semiconductor test samples, however, are generally anisotropic and possess dimensions that make it difficult to determine whether beam or plate solutions are more appropriate [2]. We describe a finite element model of SI single crystal substrates loaded in a four-point configuration and report the effects of boundary conditions, sample dimensions, and uniaxial stress on the model. Finally, we compare our modeling results to experimental data. [1] P. Scardi, Y.H. Dong, S. Setti, and V. Fontanari, Proceedings of the Sixth International Conference on Residual Stress, Oxford, UK, Vol. 1, pp. 67-70 (2000); [2] S.K. Kakkar and I.C. Noyan, Proceedings of the SEM IX International Congress on Experimental Mechanics, Orlando, FL, pp. 806-811 (2000).


3:00 AM L10.1/NG.1 CHARTER AT METAL/POLYMER INTERFACES FOR ELECTRONICS. RL. Opil, Bell Labs, Lucent Technologies, Murray Hill, NJ.

Interfaces between metals and polymers are of increasing importance in electronics. Applications that use polymers include electronics packaging, Cu and low-k dielectrics, and-display that utilize semiconducting polymers. We have used electron spectroscopy to study chemical reactions between a variety of metals (Cu, Ti, Ta, Cr, Al) and polymers (polyimide, PPV, and various low-k dielectrics). While greater metal reactivity with the polymer may yield greater initial adhesion, often the reliability degrades with time. In addition, adhesion is only one of the factors that must be considered in the role of barrier layers as conductors and/or diffusion barriers must also be considered. Great insight into the chemistry of these systems has been gained by studying the adhesion of metals onto thin-films of self-assembled monolayers on Au. We have used novel applications of photoelectron spectroscopy and x-ray absorption spectroscopy to study the evolution of the buried interfaces, and thus the long-term performance of the system. Extensions of these studies to contacts with semiconducting polymers will be discussed.

9:00 AM L10.2/NG.2 ESTIMATION OF THE INTERFACE FRACTURE ENERGY OF METAL/POLYMER SYSTEM IN MICROELECTRONIC PACKAGING: J.W. Song, S.I. Cho, Jin Yu, Center for Electronic Packaging Materials, Korea Advanced Institute of Science and Technology, Taejon, KOREA.

In the microelectronic packaging, reliability of the metal/polymer interface is an important issue and many test methods have been used to measure the adhesion strength of the interfaces. In the present work, we measured the adhesion strength of flexible two layer tapes made of Cu/Or/Polyimide(P1) using the T-peel test. The steady state peel strengths(P) were measured along with the peel angle and maximum root curvatures(K_R) behind the peel front, which were directly measured by using an optical camera. Then, effects of the bimetal plula pretreatment and the metal layer thickness on the T-peel strength were investigated, and the energy deduced by plastic bending (Ψ) were deduced based on the elastic/plastic analysis and measured root curvatures. The interface fracture energy(Γ) was the subtraction of Ψ from P. It was found that the peel strength and the plastic bending work increased with the peel angle and then saturated, and the same was true of Γ. The metal layer thickness, P and Ψ showed maximum due to the balance between crystal volume effect and compliance. However, interfacial fracture energy, Γ = P - Ψ, was more or less independent of the metal layer thickness, suggesting it to be an interface material parameter.
interfacial fracture energies deduced from the peel test. Another method used to measure the interfacial fracture toughness of the Cu/Cr interface was the indentation test using an indentation test at the W superlayer sputter-deposited on Cu film, which induced the interfacial delamination. Effects of the W superlayer thickness and residual stresses in the Cu and W films on the interfacial fracture toughness were also investigated.

9:15 AM L10.3/N6.3
FINITE ELEMENT ANALYSIS OF COPPER ADHESION TO POLY(VINYL ALCOHOL) FILM AT LEPIDIOVIR BANCO, ON Semiconductor Philippines, Inc., Technical Operations Department, Cagayan, Cagayan, PHILIPPINES.

Finite element analysis is used to analyze the button shear test. Through the use of experimental data, the adhesion strength of interfaces involved in test are characterized. It was found that adhesion strength of each interface could be characterized by dimensionless parameters. The purpose of this study was to understand and the delamination occurring in the interface of the encapsulating molding compound (EMC) and the back of the die-strap (BDF), which is made of copper. Through this adhesion strength of the EMC-BDF interface is identified and compared with various vapor pressures to see if the interface will delaminate at a given reflow temperature. Furthermore, the adhesion strength of the intervening layer of oxide is identified, which is very difficult to do in an actual experiment.

9:30 AM L10.4/N6.4
ADHESION MECHANISMS OF SILANE ADHESION PROMOTORS IN MICROELECTRONIC PACKAGING. Muna Jenkins, Jeffrey Snoeklugs, Gary Lees, Robert Small, John O. Brammell, Stanford University, Dept of Materials Science and Engineering, Stanford, CA.

Silane adhesion promoters are seeing increasing use in microelectronic packaging interfaces. For example, they are currently used to adhere the passivating polymer over oxide, and these materials are being investigated as surface treatments for silicon particles in underfill epoxy resins. To understand the exact mechanism of adhesion promotion postulated. In this paper, we present detailed studies of silane adhesion promoters on the silicon oxide surface. Two common promoters (aminopropyltrimethoxysilane and vinyltrimethoxysilane) as well as a non-functional silane are investigated. It was found that without a functional end group, long chain carbon silanes can severely degrade adhesion, resulting in interfaces weaker than if no silane is used. Several spin-coat solution formulations are used in depositing these films. Resulting surface coverage is examined and quantified with the help of AFM and XPS. Then, the behavior of various promoter films are tested in sandwich structures using a fracture mechanics approach. Finally, spin-coat solution concentration, surface coverage, and interface fracture energy are compared for the amine functional promoter.

9:45 AM L10.5/N6.5
METAL/POLYMER INTERFACE AND SOLDER JOINT RELIABILITY OF A WAFER LEVEL CSP. H. Hsu, D. Lee and J. S. Park, Dept. MSE, Center for Electronic Packaging Materials, Korea Advanced Institute of Science and Technology, Taejon, KOREA.

As microelectronic devices get smaller and higher I/O densities are required, various chip scale packages (CSP) are adopted, and wafer-level chip scale package (WLCSP) combined with flip chip technology has the highest potential. In doing so, it is necessary to redistribute peripheral bond pads and relax the thermal stress in the WLCSP. Here, we use a low modulus polymers as the stress buffer layer (SBL) to relieve the thermal stress generated at the solder joint and studied the reliabilities of the metal/SBL interface and solder joint using peel tests and ball shear tests, and effects of the polymer surface pretreatments by the RF plasma and reflow process were investigated. Results showed that the adhesion strength of the metal/SBL interface depended on the RF power density ($p$) and runner metal structure. The peel strength ($P$) was very low for $p < 0.27 W/cm^2$ but increased up to $p = 0.3 W/cm^2$ and tended to saturate around 1000gf/cm. Then failure locus analyses were conducted using AFM, AES, and XPS. The peeling locus of peel test and the failure locus of solder ball shear test were dependent on the Ni layer in the under bump metallurgy (UBM) and also on the thickness of the runner metal, particularly the thickness of Cu layer. Depending on the metal deposition condition, metal films over SBL were delaminated or buckled due to the residual stress in the metal film, which was measured using the laser curvature method. Additionally, strain fields and crack propagation and propagation behaviors around the solder joint were analyzed using micro-photograph and the correlated to the process parameters and package structures. Then, implications to the package processes and designs were discussed.

10:30 AM L10.6/N6.6
HIGH TG LOW DIELECTRIC CONSTANT AROMATIC BENZOXAZOLES CONTAINING ALKYLETHER PENETRANT GROUPS FOR USE IN MICROELECTRONIC PACKAGING. Max D. Alexander, Jr., Thuy D. Dang, Christina E. Speckler, Marlene Houtz, R.J. Spry, and Fred E. Arnold, Air Force Research Laboratory, Materials and Manufacturing Directorate, Polymer Care Technology Area, Wright-Patterson Air Force Base, OH.

Next generation microelectronic packaging requirements are driving the need to produce increasingly lower dielectric constant materials while maintaining high thermal stability and ease of processing. Polymer candidates with low dielectric constant (<2.6-2.4), high thermal stability (degradation temperature > 400°C), high glass transition temperature (>350°C), low water uptake (<1%), solubility in selected organic solvents, low thermal expansion coefficient and the capability for undergoing post-polymerization chemistry to impart insolvability after processing have been successfully synthesized and characterized by our research group. Highly flexible ring structures, formed via intramolecular hydrogen bonding, were utilized for the enhancement of the glass transition temperature. Lowering of the dielectric constants of these polymer structures was accomplished by the incorporation of perfluorocarpropyl groups along the polymer backbone. The design of post-polymer reactions to impart insolvability to select polymer candidates was based on the methodology of attachment of cross-linking sites to the polymer backbone along with pendant alkyl ether groups were synthesized from the parent structures. Upon heating, the polymer would undergo an intramolecular rearrangement reaction (chain scission rearrangement), resulting in a Tg enhancing the necessary high water uptake and dimensional stability of the polymer system. Efforts are underway to control the crosslinking density of the polymer system by partial alkylation of the hydroxyl groups attached to the aromatic benzoxazole group. Several general issues relating to integration of these polymeric materials into current processes and how we have tackled our systems, to address issues such as back etching, adhesion, dimensional stability, and conformal coating of small feature sizes.

10:45 AM *L10.7/N6.7
MOLECULAR INTERACTIONS AND ADHESION FOR INTERFACES RELEVANT TO FLIP CHIP ASSEMBLIES. Raymond A. Pearson, Lehigh University, Dept of Materials Sci. & Eng., Bethlehem, PA.

Debonding is a common wear-out mechanism in flip-chip assemblies that utilize organic substrates. The large mismatch of the thermal expansion coefficients of the silicon, chip and the organic substrate generates significant stress during thermal cycling. These thermally induced stresses promote debonding at several interfaces and debonding at the underfill-passivation interface can occur. This paper focuses on developing an understanding between the interface molecular interactions and adhesive strength in an effort to engineer reliable interfaces. The experimental approach consists of studying the adsorption of model epoxy systems onto polyimide and borosilicate surfaces using a flow microcalorimeter and separating these interfaces using double cantilever beam specimens. Acid-base theory is utilized to explain the trends in adhesion strength.

11:15 AM *L10.8/N6.8
THERMO MECHANICAL RATCHETING IN INTERCONNECTS. Z. Suo, M. Huang, Mechanical and Aerospace Engineering Department and Materials Institute, Princeton University, Princeton, NJ. Q. Mo and H. Fujimoto, Intel Corporation, Santa Clara, CA. J. He, Intel Corporation, Components Research, Hillsboro, OR.

Temperature cycling has been used as an accelerated reliability test to qualify new electronic products. Many commonly observed failure modes, however, are poorly understood that the extrapolation of the test results to service lifetime is empirical, loosely based on historical records of similar products. This lack of convenient understanding is particularly discouraging when new interconnect materials are being explored. We have initiated a program to study mechanisms of failure modes under temperature cycling. In this talk, we present our recent study on cracking in the SiN film. The SiN film has been widely used as a passivation layer in micro-electronic devices. It has been known for over a decade that the SiN film cracks after packaged devices are thermally cycled. While engineering solutions have been proposed on the basis of trial and error, a basic understanding of the cause of cracking has been identified before. In this talk, we show that the cyclic temperature, coupled with the shear stress at the die corner, causes the
interconnect pads underneath the SiN films to undergo plastic
ratcheting. Consequently, in the SiN films the stress builds up as the
temperature approaches to cracks. We compare the effects of
copper and aluminum interconnects. Implications for design rules and
qualification tests are discussed.

11:45 AM LI0.9/N9.6
DIELECTRIC PROPERTIES OF FERROELECTRIC
CERAMICS-POLYMER COMPOSITE FILMS. C.K. Chiang, L.P.
Sing and J. Obrutz, National Institute of Standards and Technology,
Gaithersburg, Maryland

The ferroelectric ceramic-polymer composite thin-film is one of
important electronic packaging materials. The dielectric constant of a
polymer composite thin film follows an empirical logarithmic
mixing rule where the powder is dispersed uniformly. The low
dielectric polymer matrix usually dominates the dielectric constant of
the composite. For example, a composite containing 30 volume
percent of barium titanate powder in an acrylic polymer shows the
dielectric constant about 31 at 1 kHz. This value is much less than
that of ceramic powder in the composite. Further increasing the
concentration of the filler has only limited effect on the increase of the
dielectric constant. In this study, XPS characterization and optical
microscopy to examine the distribution of particles. The
thin-line/case of the thickness of the order of one micron and
reconstructed 3D image from them allowed us to visualize the
relaxation by a kink-particle in any polymer interface between
them non-destructively. These data may correlate to the dielectric
constant of composite thin-films from different processing conditions.

SESSION L11: LOW-k DIELECTRICS - INTEGRATION AND MECHANICAL PROPERTIES
Chair: Robert F. Cook and Michael W. Lane

Tuesday Afternoon, April 19, 2011
Gold Gate B2 (Marriott)

1:30 PM L11.1
PO-CVD LOW DIELECTRIC CONSTANT MATERIALS
Andrew J. McKerrow, J.S. Martin, K.J. Taylor, A.K.R. Rashot, T.
Tsai, D. Morris, G. Xing, H. Hong, and J.D. Luttmer, Silicon
Technology Research, Texas Instruments Inc., Dallas, TX.

Improvements in transistor performance with scaling place increasing
dependence on interconnect performance and thereby necessitates
fundamental changes in its architecture. This includes replacing
deposition aluminum metallization with copper, the introduction of
interconnect resistance delays. At the same time or a subsequent
technology node most SC manufacturers are also replacing the
canonical silicon dioxide, SiO2, insulator with materials that are
characterized by a lower dielectric constant. The transition from
these low dielectric constant materials, or low-k materials, is intended
to improve the interconnect capacitance delay. PO-CVD deposited SiO2
is characterized by a dielectric constant of 4.1-4.2. There are a
number of materials that are deposited by PO-CVD, or similarly, that
are characterized by a lower dielectric constant and could potentially
replace SiO2 in high performance interconnects. Candidate materials
include fluoro-doped SiO2 or FSG, k = 3.5-3.8, organosilane glass or
GSGs, k = 2.7-2.9, and even lower constant materials, k =
2.2-2.9. In the k < 3 regime there are a number of
candidate materials that are deposited via spin coating, i.e. spin-on-
low-k materials. This presentation will focus on those materials
deposited by plasma methods, HDP and PECD, and that likely to be
integrated at the 0.18 or 0.13 μm technology nodes. Process
technology improvements and material characterization of HDP-FSG
films that led to the development of production worthy FSG films will be
discussed (e.g., A. L. Johnson et al., American Vacuum Society, 47th
International Symposium, Oct. 2010). This presentation will include a
discussion of the materials properties of GSG films that affect their
integration in high performance interconnects including stress
corrosion cracking and patterning using chemically-amplified resists.

2:00 PM L11.2
THE EFFECT OF CARBON ON THE ADHESION AND
DE-BONDING OF LOW-k DIELECTRIC ORGANOSILICON FILMS
(SiO-H:C) IN MULTI-LAYER THIN-FILM STRUCTURES
Jae Eun Rim, Frank Shi, Reinhold Dasakardt, Stanford Univ, Dept of
MSE, Stanford, CA.

Incorporating organic carbon groups such as methyl groups into the
Si-O network of silicon dioxide is one way of lowering the dielectric
constants of ILDs in integrated circuits. However, in general, this has
a detrimental effect on the mechanical properties of the dielectric film.
Particular of interest in this regard is the interfacial
adhesion between the dielectric and adjaing films in the multi-layer
stack. In this study, the effect of increasing carbon content on the
adhesion to adjacent materials and the intrinsic fracture resistance is
addressed. Thin film fracture mechanics techniques were employed to
test these multi-layer thin-film ILD structures containing silicon
films [Si-O-H:C] prepared by both spin-on glasses (SOG) and CVD
methods. XPS scans at the resulting fracture surfaces were used to
characterize the weak microstructural paths to failure. Adhesion and
fracture mechanisms will be discussed in terms of the organosilicon
glass network structure.

2:15 PM L11.3
PREDICTION ON LOWER LIMITS OF DIELECTRIC CONSTANT
FOR LOW-k DIELECTRICS RESTRICTED BY A MECHANICAL
STRENGTH. Nebiu Aci, Takuya Fukuda and Hitomori Matsunaga,
Environmental Process Technology Laboratory, Semiconductor
Technology Research Department, Corporate Research and
Development Division, Hitachi, Ltd., Yokohama, Japan.

By decreasing film density, dielectric constant can be reduced.
However, simultaneously mechanical strength of the films drastically
becomes weaker. Therefore, there may exist some restrictions of
lowering dielectric constant of dielectric films arising from
degradation of mechanical strength. Some estimations of such limit are our
major concern. We evaluated elastic modulus of various inorganic low-
k films and inorganic porous ones and that of various organic low-k by
means of a nano-indentation. Relations of modulus vs. density for
various low-k films exhibited linear dependencies having positive
slopes with negative intercepts for inorganic porous, inorganic,
and organic low k groups, respectively. This fact indicates that
reduction of dielectric constant of low-k films realized by lowering film
density will be confronted with a physical limitation caused by
degradation of mechanical strength. According to the relation, which bases on
the assumption that density reduction of films is caused by a
homogeneous dispersion of fine spherical pores in films, dependencies
of dielectric constants of various low-k films upon film density can be
described. From the relations between modulus versus film density, and
between dielectric constant versus film density, new relations
between modulus and dielectric constant can be obtained. From the
relations, it is concluded that modulus of inorganic low-k films decreases
abruptly with decrease of dielectric constant in comparison with moderate decrease of organic low-k ones. The values
of modulus for organic low-k films becomes lower than those of
inorganic ones in the region of dielectric constant lower than ca. 2.5,
in the region of dielectric constants lower than 2.0, modulus of
inorganic porous low-k films become larger. This work was performed under
the management of ASET in Ministry of International Trade and Industry (MII)
and New Energy and Industrial Technology Development Organization (NEDO).

2:30 PM L11.4
COMPARATIVE STUDY OF MECHANICAL PROPERTIES AND
INTERCONNECT PROCESS PERFORMANCE FOR
NANOPOROUS SILICA FILMS OF VARIOUS POROSITY
Hui-Jun Wu, Pan Zhong, Jessie Chen, Teresa Romanos, Rob Roth,
David Smith, Lisa Brengardt, Denise Dury, Victor Lu, Ha Lei, Alphon Nguyen, Jude Donne, and Jim Drage, Honeywell
International, Honeywell Electronic Materials, Sunnyvale, CA

Successful development of ultra low dielectric constant (k) insulating films is a critical part of the semiconductor industry technical
terrain map. This industry is considering the use of insulating films with a
k value in the 2.5 to 1.5 range for the 0.13 um to 0.07 um device
generations; in these device generations, lower dielectric constant films would be
part of a multi-level interconnect structure with Cu as the conductor metal. Nanoglass™ E films, a form of nanoporous silica, can be
made with k values that cover this range. In this paper we describe the
experimental results using Nanoglass™ E films which cover a range of
porosity values. For these films we report general physical and
chemical properties and results from interconnect module tests. Key
physical properties of the films (such as k, refractive index, average
capilarity, pore size distribution over a surface area, characteristic
of the film) and the overall film properties) are reported. The films are also compared for their performance in various
modules which are used in fabricating Cu damascene structures. These processes include CMP performance (polish rate, defect density). The work shows that Nanoglass™ E films can tolerate the typical CMP conditions which are used for
removal of excess Cu in damascene structures.

2:45 PM L11.5
PROCESSING OF XLR™ SPIN ON DIELECTRIC MATERIALS
FOR NEXT GENERATION INTERCONNECT TECHNOLOGY.
Jeffrey N. Bremmer, Eric Moyer, Tom Dea, Les Carpenter, Todd
Bridgewater, Wei Chen, Akihiko Kobayashi, Mike Bournina, Dow
Corning Corporation, Auburn, MI.

A new dielectric material has been developed to meet the emerging
needs of advanced interconnects beyond the 0.18 μm technology node.
Dow Corning XLR dielectric is a porous spin on material based on
Porosity Effect on Thermal Conductivity of Organosilicate Glass Films.

JunJun Liu, Chun Hu, Michael Kenna, Paul S. Ho, Michael Miller, and H. M. Almaden Research Center, San Jose, CA.

The introduction of porous materials as interlayer ultra-low K dielectrics from a network of pore-filled organosilicate glass is an attractive approach to improving the thermal properties of the film. This allows for the formation of a porous network that can enhance the thermal properties of the film. The formation of this network of pores is important in order to achieve the desired properties.

The effect of porosity on the thermal conductivity of organosilicate glass films was studied. The results indicate that the thermal conductivity of the film is significantly affected by the presence of pores. The dependence of thermal conductivity on porosity was investigated. The study showed that the thermal conductivity decreases as the porosity increases.

Environmental Effects on Stress-Corrosion Cracking of Organosilicate Glass (OSG) Low-k Dielectric Films.

Ms. Dylan Morris, Ting Tsai, Andrew McKeever, Department of Chemical Engineering and Materials Science, University of Minnesota, Minneapolis, MN.

Low dielectric constant materials of a wide variety are currently being evaluated as replacements for silicon dioxide in high performance interconnects. In all cases the mechanical properties (modulus, hardness, and fracture toughness) of such low-k materials differ considerably from those of SiO2. Therefore, it is necessary to determine the effect of porosity on the stress corrosion cracking behavior of these materials. A process that requires a tensile driving force and chemical bonding in the film that can be hydrolyzed at the crack tip.

The effect of porosity on the stress corrosion cracking behavior of low-k materials was studied. It was observed that moisture absorption reduces the film residual stress and crack velocity significantly. The pH of the reactive environment is shown to have a discernable effect on the stress-corrosion cracking velocity. The relationship between the physical properties of the film and the corresponding resistance to stress-corrosion cracking will be discussed.

Effects of Microstructure and Molecular Weight of Poly-siloxanes on Mechanical and Dielectric Properties of Thin Films.

J. K. Kim, E. S. Re, E. K. You, D. Y. Youn, School of Chemistry, K. Chae, School of Chemical Engineering, Seoul National University, Seoul, Korea; H. W. Rhee, Dept of Chemical Engineering, Sungkyunkwan University, Seoul, Korea.

We have prepared poly-siloxanes with systematically varying organic moieties (methyl, ethyl, propyl, and phenyl) and molecular weights of the polymer structures, and investigated their microstructures and physical properties of thin films. The local microstructures as determined from the MALDI-TOF and FT-IR data as function of the polymerization time change markedly with the nature of organic moieties, forming hedgehog-like, cupcake or highly branched structures through the varying extent of intermolecular and/or intramolecular interactions. The local microstructures in turn are found to strongly influence the mechanical properties (hardness and crack resistance). It is also noted that a small effect is seen for the dielectric properties.

Adhesion and Reliability in Methylsilsesquioxane Dielectrics.

D. A. M. Madden, Stanford University, Dept. of Materials Science and Engineering, Stanford, CA; Will Volkert, Robert Miller, IBM Almaden Research Center, San Jose, CA; Reinhold Draskard, Stanford University, Dept. of Materials Science and Engineering, Stanford, CA.

Methylsilsesquioxane (MSQ) is an important new interlayer dielectric. It is an attractive candidate for the replacement of silicon dioxide due to its low loss and the reduced cost. The control of porous morphologies, however, is necessary to understand the adhesion and inherent crack growth resistance of the material before full-scale integration. This study investigates the inherent toughness of MSQ as well as its adhesion to a variety of layers. The measurements were made using fracture mechanics techniques that eliminate the effects of residual stress. This is crucial, because CMP and thermal mismatch with other layers in the structure create stresses in addition to natural stresses in the film. The effect of salient compositional and microstructural factors such as porosity, connectivity, and porogen remnants was examined. In addition, the effect of adhesion promoters and surface modification via UV-Ozone and electron beam techniques will be described. The implications of such microstructural and surface modifications on fracture and adhesion mechanisms are discussed. Of special interest is the discovery that some of the porogen does not fully decompose in the porous material. In some instances, however, this is helpful rather than detrimental to the interfacial adhesion.

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The development of new organic low-k materials has provided an opportunity to examine plastic energy dissipation in thin polymer films. Unlike most brittle oxides and organic hybrids, polymer low-k materials have been observed to be ductile and more resistant to interfacial debonding. Microscopic adhesion was determined by measuring the critical strain energy release rate (Ge) of a stable metal located within a thin film structure comprised of the polymer, metal, and barrier layers. The plastic energy dissipated in the polymer layer was controlled by varying the thickness of the layer and the distance between the layer and the debond. The benefit of such plastic energy dissipation is often not observed for thin metal layers such as Al and Cu due to strengthening mechanisms. Alternately, polymer yield properties are not sensitive to layer thickness over similar length scales and offer the possibility of being controlled with chemistry and curing cycles. Finally, the yield properties and plastic energy dissipation can also be manipulated by changing the stress state of the ductile layer. Interfacial adhesion was measured for thin film structures that included patterned channels with selected aspect ratios and dimensions of the order of the ductile layer thickness. Results will be discussed in terms of the prevailing mechanism of deformation in the polymer channel.

SESSION L12: POROUS LOW-k DIELECTRICS - CHARACTERIZATION

Chair: Shu Yang and Kenneth P. Rodbell
Friday Morning, April 20, 2001
Golden Gate B2 (Marriott)

8:30 AM L12.1

Low-k, Porous Methylsilsesquioxane for Interlevel Dielectric Applications.

James M. Padovani, Hyoungjin Jeong, Sue Ann Biehow, and Paul A. Koll. School of Chemical Engineering, Georgia Institute of Technology, Athens, GA.

This project focuses on the development, characterization, and optimization of the properties of siloxane-based, porous, low dielectric constant materials for use as interlevel dielectrics. The goal is to modify a commercially available spin-on-glass (methylsiloxane) and introduce porosity into the film to lower the effective dielectric constant of the siloxane by the incorporation of air. The pores are created by adding a sacrificial polymer (substituted norbornene polymer) to the siloxane matrix. The sacrificial polymer is then thermally decomposed to form microcavities (<= 5 nm) within the film to result in the formation of a uniform pore size and distribution, chemical bonding of the sacrificial polymer to the spin-on-glass, mechanical and optical properties, and the permeability of decomposition products through the siloxane matrix will be reported. Transmission electron microscopy and small angle X-ray scattering experiments were performed to investigate the pore size distribution as a function of polymer molecular weight, concentration and type of functional groups within the polymer, and...
polymer loading level. NMR and FT-IR spectroscopies were used to probe the bonding of the polymer to the glass prior to curing and pore formation. Chemical probes were used to determine size and shape. Nano-indentation techniques were used to determine surface roughness. In general, it was shown that the porous films had superior fracture toughness (resistance to cracking) compared to those without pores. The moisture absorption and optical properties of the porous silicone films were characterized.

8:45 AM LI2.2

NANOPOROUS LOW DIELECTRIC CONSTANT ORGANOSILICATES PREPARED FROM ORGANIC/INORGANIC NANOCOMPOSITES. EFFECT OF MACROMOLECULAR ARCHITECTURE ON STRUCTURE DEVELOPMENT.

James L. Hedrick, Robert D. Miller, Craig J. Hawker, Willi Volkert, IBM Research, Almaden Research Center, San Jose, CA.

A general route to organic-inorganic hybrids with nanophase morphologies has been elaborated with the objective of ultimately tailoring nanophase morphologies and homogenization. The controllability of the organic template and the selectivity of the sol-gel conversion can be varied over a broad range of compositions by adjusting the chemistry and the processing. Poly(organosilicate) is ideally suited for such applications since it is thermally stable and compatible with many end groups. Novel synthetic routes allowed dendritic, hyperbranched and dendrimer-linear hybrid architectures to be prepared. These polymers were readily soluble initially in the organic solvent and the polymerization of the organosilicates (PMSSQ) was induced by thermal treatment, producing a nanophase inorganic structure. The size and shape of the pores are identical to those of the original hybrid morphology (< 1000 A), and the effect of the macromolecular architecture on the morphology is significant. A reduction in the dielectric constant was achieved by simply replacing a portion of the glass matrix with air which has a dielectric constant of 1.0.

9:00 AM LI2.3

CHARACTERIZATION AND Cu METALLIZATION OF MOLECULARLY TEMPELATED NANOPOROUS SILICA DIELECTRICS. F.M. Pau, T.G. Tsen, B.W. We, National Nano Device Laboratory, Taiwan, TAINAN, TAIWAN; A.P. Cho, C.M. Yang, J.C. Chien, Department of Chemistry, National Tsing Hua University, Hsinchu, TAIWAN; I.D. Chao, Department of Materials Science and Engineering, National Tsing Hua University, Hsinchu, TAIWAN.

Molecularly templated nanoporous silica films have an ordered pore structure and uniform size distribution. The dielectric constant and mechanical strength of the nanoporous silica films can be controlled by changing the silica composition, thickness and, therefore, they have a great advantage over aerogel and mesoporous silica films in terms of being a potential intermetal dielectric material for sub-130 nm technology nodes. In the study, we have prepared nanoporous films by sedimenting on the silica substrate, with the various organic template molecules were mixed, on silicon wafers. The nanoporous silica films have a porosity of ~70%, and the pore size is estimated to be about 4.5 nm according to X-ray adsorption and desorption isotherms. Cu/TEOS and TEM results also clearly show that the porous films have an ordered microstructure. MIL capacitor structure was fabricated to measure the electrical characteristics of the nanoporous silica films. The nanoporous silica films exhibit an ultra low k and value over a range of 1.5-2.0 depending on film modification methods, such as hexamethyldisilazane (HMDSO) vapor exposure or plasma treatments. A leakage current density in the order of 10^-7 A/cm² can be readily obtained for the silica films under a stress of 2MV/cm. With TEOS and FTIR, the polymer and the characterisation, the nanoporous films demonstrate very good thermal and dielectric stabilities. Copper and tantalum nitride films have been deposited on bare or in situ CVD coated nanoporous silica film. The TaN film behaves as a very good diffusion barrier for Cu diffusion up to an annealing temperature above 400°C. The Cu/TaN deposited nanoporous silica film was subjected to the chemical-mechanical polishing process and the selectivity of the silica film over the metal due to mechanical stress during CMP was not observed. The study shows that molecularly templated nanoporous films are very compatible with contemporary 10k processing technology.

9:15 AM LI2.4

STRUCTURE AND MICROMECHANICAL CHARACTERIZATION OF NANOPOROUS ORGANO-SILICATE THIN FILMS. K. Choo, S.-H. Lee, D. Yoon, Department of Chemistry, Seoul National University, Seoul, KOREA; J.-K. Lee, H.W. Ro, D.Y. Yoo, and D.Y. Yoon, Department of Chemistry, Seoul National University, Seoul, KOREA; M.Y. Jin, Advanced Material Division, Korea Research Institute of Chemical Technology, Taejon, KOREA; S.K. Kim, Department of Chemistry, Seoul National University, Seoul, KOREA; J.-H. Hahn, Korea Research Institute of Standards and Science, Taejon, KOREA.

As the feature size in advanced ULSI microelectronic devices continues shrinking, it is expected that low-k interlayer dielectric materials with k lower than 2.5 would be needed around 2003. A continued reduction of the dielectric constant k is also believed to be possible only by incorporating porous nanocomposites filled with a void fraction f = 0.8 to 1.0 into the electrically insulating matrix such as poly(methyl silsesquioxane) (PMSSQ). Micromechanical properties of the nanoporous ultralow-k thin films becomes more important than ever since the films are required to withstand severe mechanical conditions imposed by the chemical mechanical planarization (CMP) processes and the thermal expansion mismatch of multilevel BEOL films. Whenever air is incorporated into ultrathin films for lowering k, the mechanical strength is inevitably reduced. To quantify this effect, the pores should exist in the film as closed cells in nanometer scale. In this study, nanoporous ultra-low-k films were prepared with PMSSQ and star-branched poly(organosiloxane) (PCL), both of which were synthesized to control molecular weight and functionality. Nanoporous structures including size, shape, and distribution of pores across the film were investigated using field emission scanning electron microscopy, cross-sectional transmission electron microscopy, atomic force microscopy and high-resolution X-ray reflectivity. Micromechanical characteristics were also carried out, using a microindenter and a microvoider, to measure hardness, modulus and crease toughness. A strong correlation of the nanoporous thin films, showing a strong correlation between structure and micromechanical properties.

9:30 AM LI2.5

NEW METHOD FOR PRODUCING NANOPOROUS DIELECTRIC FILMS. Bashir I. Ithlahi, Xupeng Chen, Xuejun Wang, Shabbari Ganapathy, Department of Physics, Texas Tech University, Lubbock, TX; Jiansu Sun, Prathamesh Dodhi, and Sandeep L. Sinha, Department of Chemical Engineering, Texas Tech University, Lubbock, TX.

We have prepared amorphous silicon carbide (a-SiC:H) films using a liquid source in a plasma enhanced chemical vapor deposition (PECVD) system. The dielectric constant of the films ranges from 3 to 5 and depends strongly on process parameters. We are working on a novel method for introducing porosity in a-SiC:H films. In this method, nanopores are introduced by seeding the film with inert supercritical CO₂ and subsequently depressurizing the gas to form nanoporous structures. The film thickness and refractive index were measured using a prism coupler and the dielectric constant was measured using mercury probe technique. Our preliminary work shows that when a-SiC:H film with dielectric constant of 3.0 was swelled at 1500 psi CO₂ pressure for two hours followed by rapid depressurization, the film thickness increased by 2.1 ± 0.1% and the refractive index decreased by 3.7 ± 0.1%. The density was reduced by 6.0 ± 0.2% (from 3.0 to 2.8). Increasing CO₂ pressure is anticipated to increase the CO₂ desorption in the films, thereby further reducing the dielectric constant. The effect of CO₂ processing temperature and pressure on the porosity and dielectric constant of films prepared under various PECVD conditions will be discussed.

10:15 AM *LI2.6

POROSITY CHARACTERIZATION OF MESOPOROUS DIELECTRIC THIN FILMS USING POSITRON ANNOTILATION SPECTROSCOPY. M.P. Peckova, M.H. Weber, K.G. Lynn, Dept. of Physics, Washington State University, Pullman, WA; K.P. Reddell, IBM T.J. Watson Research Center, Yorktown Heights, NY; W. Volkert, R.D. Miller, IBM Almaden Research Center, San Jose, CA.

Beam based Positron Annihilation Spectroscopy (PAS) is a recent addition to the spectrum of non-destructive tools available for the characterization of low-dielectric constant (low-k) thin films. Using the annihilation signatures of positronium (Ps; H-like positron-electron atom), PAS provides information on total porosity, pore size, pore size distribution and void interconnectivity (percolation) as a function of film depth. In this paper, we show examples of the utility of various PAS techniques to characterize porous MMSQ films as a function of porogen load (5.50 wt %). PALS, 3gsPs annihilation, and Doppler Broadening were used to obtain a global picture of film porosity. We report results from measurements of mesoporous MMSQ spin-on films (~6 um thick), in which the porosity was created using a sacrificial porogen approach. The PAS results are subsequently compared to more traditional characterization techniques including CV, AC conductivity, FE-SEM, FTIR, TGA, ellipsometry, and hardness measurements.

10:45 AM LI2.7

POROSITY AND STIFFNESS OF AEROGEL FILMS
Density/porosity is the most important parameter determining properties of porous films, however it is difficult to measure. This work reports characterization of density/porosity and Young’s modulus values of a range of nanoporous silicon aerogel films via dispersion of laser-generated wideband surface acoustic waves. The technique shows the relations between dielectric constant, porosity and Young’s modulus. Density and Young’s modulus of submicron thickness aerogel thin films have been measured from dispersion of laser-generated wideband surface acoustic waves. The films had porosities of 20% and Young’s modulus between 1.2 GPa. Both density/porosity and Young’s modulus show a strong correlation with film dielectric constant. Young’s modulus is shown to reduce drastically with porosity, providing valuable information about material stiffness which is of vital importance with respect to ability to withstand mechanical-polishing. The technique provides absolute values of density and Young’s modulus, rather than relative. Porosity can be measured to better than 1%. The technique is rapid, relatively cheap and non-destructive, and has the potential to provide density measurements quicker and more accurately than other techniques. The additional ability to assess stiffness is a further advantage. Use of the method can provide valuable process control to develop and standardize nanoporous silicon film properties, the lack of such a technique has severely hindered development of such films.

11:00 AM L12.8 POROSITY IN TOW-DIELECTRICS: EFFECTS OF THE TRANSITION FROM CLOSED TO OPEN CELL POROSITY. Michael W. Lane and Kenneth P. Rodbell, IBM T. J. Watson Research Center, Yorktown Heights, NY; Willi Volkamer and Robert D. Miller, IBM Almaden Research Center, San Jose, CA.

The drive for faster interconnects dictates that materials with a dielectric constant, k, lower than that of SiO₂ (k ≈ 3.9) must be incorporated into future device technologies. A number of candidates ranging from organic to inorganic films have emerged. However, the general consensus is that solid films will not be able to provide the ultra low dielectric constant (k < 2.0) needed for future applications. To this end, dielectrics which contain embedded voids have been proposed to lower the dielectric constant towards that of air (k ≈ 1.0). While inserting voids into a material may produce favorable results in regards to electrical properties, it may have deleterious effects on the mechanical properties of the material. Accordingly, this work focuses on characterizing the effects of porosity on the electrical and adhesive properties of porous MSQ. Positron annihilation studies are used to quantify the porosity in the films and identify the transition from closed cell to open cell porosity. Four-point flexure and shear measurements were made and the fracture path was characterized by AFM and EDX. The adhesive properties of the porous MSQ were found to depend strongly on the transition from closed to open cell porosity.

11:15 AM L12.9 PROBING BARRIER INTEGRITY ON POROUS LOW-K THIN FILMS USING POSITRONIUM ANNihilation LIFETIME SPECTROSCOPY. Jinming Sun, Terry L. Dull, Albert F. Yee, MS&E Dept., Univ. of Michigan, Ann Arbor, MI; David W. Gidley, William E. Friesen, Dept. of Physics, Univ. of Michigan, Ann Arbor, MI; Todd Ryan, Simon Lin and Jeff Watson, STEMALECH, Austin, TX.

Positronium annihilation lifetime spectroscopy (PALS) has been used to investigate the continuity and thermal stability of thin barrier layers designed to prevent Cu diffusion into porous silica low dielectric constant (k) films. Honeywell Nanoglass™ R2.3-A10C, a porous organosilicate film, is determined to have interconnected pores with an average diameter of 6.8±1.4 nm, assuming the pores are tubular in shape. Cu deposited directly on the A10C films is observed to diffuse into the porous structure. The minimum necessary barrier thickness for stable continuity of T < 550°C. T < 550°C is determined by detecting the signal of positronium (Ps) escaping into vacuum. It is found that the 25 nm thick layers do not form continuous barriers. This is confirmed by the presence of holes observed in such films using a transmission electron microscope (TEM). Although 35 nm and 45 nm T < 550°C and T < 550°C layers perform effectively at room temperature as Ps barriers, only the T < 550°C samples are able to withstand heat treatments up to 500°C without breakdown or penetration into the porous film. T < 550°C diffusion into the silica pores is indicated by the reduction of the Ps lifetime after high annealing temperatures. The procedures to standardize the testing of barrier layer integrity and thermal stability using PALS are proposed. Progress in extending this method to probe barrier integrity in realistic trenches or vias will be presented.

11:45 AM L12.10 A NEW X-RAY SCATTERING METHOD FOR DETERMINING PORE-SIZE DISTRIBUTION IN LOW-K THIN FILMS. Kazushige Momoe, X-Ray Research Laboratory, Rigaku Corp, Tokyo, JAPAN; Shinjiro Kawamura, Technology Development Center, Tokyo Electron Ltd, Yamashita, JAPAN.

Lowk dielectrics are extensively interesting for producing ultrahigh density integrated circuits. Nanometerized pores are introduced into thin silicon, polymer or their hybrid thin films for reducing the dielectric constant of the materials. The structure of the pore and its size distribution are very closely related with physical properties of the material. Thus, a rapid and simple method is important for determining the pore size distribution in submicron films on thick substrates. The use of gas adsorption analysis, neutron scattering, and positron annihilation lifetime spectroscopy has been reported previously. In our laboratory, we tried to use x-ray scattering, which is a very common and simple technique for determining nanometer-size structures. However, the transmission geometry used in x-ray small angle scattering is not applicable since x-ray photons can not transmit the substrate material. Furthermore, the conventional specular reflection geometry can not be used because of strong x-ray reflection from the substrate. We, therefore, have developed a new method for avoiding specular reflected x-rays in measuring small angle scattering patterns only from the porous thin films. It is important to correct for refraction and reflection at the surface because it interferes with the small angle scattering data. The pore size distribution of a film is determined by a comparison of a simulated x-ray small angle scattering pattern with that of the observed data. We also compared the results of our method with that from the gas adsorption analysis. A good agreement has been obtained, even though the analytical models of both methods are different.