SYMPOSIUM M
Chemical-Mechanical Polishing Advances and Future Challenges
April 18 – 20, 2001

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*Invited paper
9:45 AM *M14
ROTATIONAL AVERAGING OF MATERIAL REMOVAL DURING CMP: David R. Evans, SHARP Laboratories of America, Camas, WA; Michael T. Oliver, Rock Inc., Newark, DE.

At present, several different competing mechanical configurations are used in chemical mechanical polishing. These range from classical rotary designs to orbital and linear systems as well as the more recent work on non-rotatory designs. Invariably, wafer rotation in these systems is used to average out gross material removal rates. To the uninformed, this would perhaps seem to be so obvious that no further investigation is necessary. However, the interaction of polishing pad microstructure, along with whatever abrasive material might be present is in reality quite complex. In addition, fluid transport between wafer and pad surfaces is strongly affected by pad microstructure and relative motion of the two surfaces. In the present work it has been found that in the absence of rotational averaging correlated variations in material removal rate can be observed downstream from patterned features on the wafer surface. Furthermore, the correlation length is quite long and can be related to micro and macrostructural viscoelastic properties of the polishing pad material. Specifically, relaxation time for decompression of pad anisotropy is a major determinant of the correlation length. It should be emphasized that this is an entirely separate issue from "planarization length" as commonly defined. Also, in the absence of rotational averaging, very strong "leading edge effect" is often observed. This is characterized by very high material removal rates at the leading edge of the wafer. In contrast, at the trailing edge removal rates are very low and may even vanish altogether. In addition to the usual process variables (down force, slurry flow, etc.), this behavior is governed by the angle of attack of the wafer relative to the pad.

Obviously, rotation of the wafer during polishing converts any leading to trailing edge gradient in material removal rate to radial non-uniformity. In normal operation, this will be confounded with additional sources of radial non-uniformity due to slip, vibration, back pressure, etc. In the present work these effects can be separated and quantified.

10:45 AM *M15

A long-lasting CMP related yield/reliability puzzle, thickness spike, frequently appearing at the wafer center after CMP operation, was studied. Optical film thickness measurements for pre-and post-CMP film were combined with surface topography profiling. Wafer surface profile was also studied after the oxide film was HF-etched out. It was found that the post-CMP thickness spike is not caused by CMP removing silicon however originating from a specific film type and occurs when the bare silicon wafer has a narrow dip-like defect in its center. The scenario of the "anti- spike" formation could be portrayed as: 1. Bare silicon wafer comes with a dip-like defect in its center. 2. Oxide deposition, having high step coverage properties, follows the profile of the bare silicon wafer and fills the dip. Optical thickness measurements tools, being insensitive to the height variances, are not capable to detect the dip. 3. CMP, doing its planarization job and flattening the surface, creates a local thickness bulge, actually an "anti-spike" pattern filling the bare silicon dip in the wafer center. The higher is the CMP planarization efficiency and the narrower and deeper is the bare silicon dip, the more pronounced is the pattern. An uniformed material layer under the topography copying film is transformed by CMP into a planarized flat-top film with inevitable thickness variations (thin elevated sections and thick elevated sections), which is exactly what planarization technique is supposed to produce. The center spike generation scenario explains the appearance of the film thickness spike in the wafer center reveals the root cause of this phenomenon: bare silicon dip-like defect located exactly in the wafer center, which most probably is originated to the specificity of the silicon crystal growth. This scenario also indicates that yield failures related to the center spike problem supposed to be associated with underetched plug holes and, as a result, electrical opens. It also explains why the photo lithography operation also experiences problems in these cases and what is the nature of the problems. Surface flatness obviously causes so-called "Focus depth" problems in this case, which finally results in numerous electrical and functional failures. The thickness of the dip normally is about 4 mm in diameter, which may affect either 1 or 4 dies depending on wafer layout approach. The origin of the dip in
the bare silicon wafer center is under investigation. Up to this point it was found that the dip is not originated to the thermal shrinkage of the silicon in the wafer center. The centrosymmetric phenomenon could be considered as an example of extremely long-range CMP related integration interaction of a narrow dip-like microdefect at the bare silicon wafer surface and high planarization efficiency of the CMP process.

11:00 AM M16
EFFECTS OF MICRO-SCALE ABRASIVE SIZE ON THE CHEMICAL MECHANICAL POLISHING OF SiO2, Chunhong Zhou, Lei Shan, Rob Hight, Steven Dvanikul, the George W. Woodruff School of Mechanical Engineering, Georgia Institute of Technology, Atlanta, GA; S.H. Ng, GISTIC Institute of Manufacturing Technology, Singapore; Andrew J. Prakaswini, Chemical Products Corporation, Carterville, GA.

This paper addresses the influence of the size of the abrasive in a slurry while polishing a thermally-grown silicon dioxide deposited on 100 mm diameter [100] p-type single crystal silicon wafers. The sizes of the abrasive particles (colloid silica) were 10, 20, 50, 140, and 100 microns. The slurries contained 30% by weight abrasive particles stabilized with KOH. Experimental results demonstrate that the polishing rate and surface roughness are sensitive to the particle size and there exists an optimum abrasive particle size in terms of removal rate. A “nano-film” theory based on the pad roughness is used to explain the phenomenon. Keywords: Abrasives, Material Removal Rate; Chemical Mechanical Polishing; Surface Finish.

11:15 AM M17
POLYURETHANE PAD DEGRADATION AND WEAR DUE TO TUNGSTEN AND OXIDE CMP, Amy L. Moe and Joseph Cecchi, University of New Mexico, Chemical and Nuclear Engineering Department, Albuquerque, NM; Dale Hetherington and David Stein, Sandia National Laboratories, Albuquerque, NM.

Chemical Mechanical Polishing (CMP) of both silicon dioxide and tungsten films utilizes Rodel FC140 polyurethane polishing pads and alumina (tungsten) and silica (oxide) abrasives. The purpose of this research is to examine the structural, chemical, and mechanical property changes due to CMP of tungsten and oxide films. The physical and chemical properties of a polishing pad are not well understood. These property changes due to polishing will affect the removal rate, wafer uniformity, and pad life. The degradation of the pad has been examined using Electron Microprobe, Confocal, SEM, TEM, DTA, TMA, XRD, FTIR, and Raman analyses. Tungsten and oxide polishing mechanisms are very different. Tungsten polishing is more a combination of chemical and mechanical abrasion, whereas, oxide polishing is more mechanical than chemical. Based on the FTIR spectra, the oxide polishing resulted in only one detectable structural change in the polyurethane hard segment. Tungsten polishing, however, resulted in various structural chemical changes as well as the displacement of various elements such as C, Al, and Cu in the pad. The properties of the polyurethane are dependent on the ratio of the isocyanate hard and the polyol soft segment, which change due to CMP. The result of the reduction in the isocyanate hard segment and the formation of the carbonyl group may increase the pad hydrophilicity. The swelling of the polyurethane pad during polishing is due to the increase absorption of water from the slurry system into the pad. The presence of the slurry abrasive in the pad after polishing may affect the performance of the pad. The “hot spot” formation occurs at a faster rate without conditioning for both oxide and tungsten polishing and affects polishing performance. Conditioning effectively roughens the surface of the polyurethane pad and increases the contact area between the pad, wafer, and slurry. Without conditioning, there are less pad areas for slurry transport and decreased rough areas for effective abrasion.

11:30 AM M18

In spite of being a historically ancient technology, chemical mechanical polishing (CMP) has attracted enormous attention recently because of its applicability in planarizing the dielectrics and metal films used in the silicon integrated circuit fabrication. Continued miniaturization of the device dimensions and the related need to lower the cost of processing number of devices on a single wafer led to building multilevel interconnection on planarized levels. In CMP very thin materials (≤ 5 μm) has to be removed very precisely maintaining the precise control on the remaining thickness. Because CMP occurs at an atomic level at the wafer surface and the wafer interface, stresses and pads play a critical role in the successful implementation of this process. Surface roughness, elastic and viscoelastic properties, thickness, pore sizes play important role in this process. Unfortunately mechanical properties of polyurethane polishing pads used in CMP are poorly understood. In this study we have studied the mechanical properties and surface morphology of CMP pads using the state-of-the-art nano-indentation technique along with tapping mode atomic force microscopy. Elastic, viscoelastic, modulus, and hardness, and surface roughness have been evaluated. Tribological properties of the pad have been evaluated using Universal Micro-Tribometer. Direct correlation between pad properties and polish performance is not yet determined to correlate the properties and performance of the pads.

11:45 AM M19
A TECHNIQUE FOR ENGINEERING THE PLANARIZATION PROPERTIES OF A CMP POLISHING PAD, Peter Rentel, Linn Research Corp, Fremont CA; Brian Lombardo, Madison CMP, Wilminton, DE.

In CMP, long-range planarization - planarization occurring over a lateral distance of greater than, say, 400 microns - is controlled primarily by the mechanical properties of the polishing pad, i.e. thickness and stiffness. One measurement of long range planarization can be made by polishing structures of graded lateral dimension and fixed step height. When the wafer is polished, the remaining normalized step height can be plotted as a function of feature size. Doing so results in a sigmoidal shaped curve transitioning from zero (perfect planarity) to unity (zero planarity). We describe the planarization length “L” as the distance at which the curve crosses 0.5. L is proportional to S 0.5, where S is the standard deviation of the grain size which is the derivitive of the sigmoid. While longer planarization length is generally desirable and easily achievable, a large S often results in too much planarization, where the ultimate planarity of the silicon surface is challenged, and an undesirable effect of “grain cheese” occurs as the polishing planarizes the silicon substrate itself. Decreasing L can eliminate this effect, but only at the expense of long range planarity, a desirable output. The challenge, therefore, is to engineer a polishing pad with a large S, but a very short L. This can be achieved by cutting grooves into the surface of the polishing pads, effectively decoupling L from S. By cutting the grooves in such a way as to create islands on the pad surface, these features serve to create a planarization length of the order of red limited to the island size, i.e. causing S to be very small. By changing the size of the islands, L and S can be engineered to achieve optimal planarization for the given structure to be planarized and quality of silicon substrate available. Planarization results are presented to show the effect of actively engineered planarization pads, and how the grove pattern can be optimized for a given planarity requirement and substrate quality. The results are followed by a discussion of the expected vs. the achieved results.

SESSION M2: CMP ABRASIVES I / CMP ABRASIVES II
Chairs: Kenneth C. Caden and Rajeev Bajaj
Wednesday Afternoon, April 18, 2011
Golden Gate A1 (Marriott)

1:30 PM M2.1
PREPARATION AND EVALUATION OF CHEMICALLY MODIFIED ABRASIVES FOR CMP. R. Parvath, N. Barney, H.Y. Wang, K. Gribbs and A. Bafel, Clarkson University, Dept of Chemistry, Center for Advanced Materials Processing, Potsdam, NY.

Abrasives particle size, shape and composition in CMP slurries are known to be among several variables that control polishing rate and generation of defects during wafer planarization. In order to meet new generation standards, particle sizes are being reduced and composition used to control abrasive hardness and provide selectivity in polishing different wafer surfaces. In recent years advances have been made in technologies for surface functionalization, including many of many types of particular matter. This expertise is now being applied to the preparation of powders for use in CMP. Presented in this paper will be methods developed by the authors to selectively improve for use in CMP slurries the surface of several micro and nano sized metal oxide particles. The treatments include coating individual cores with a continuous shell of inorganic or organic material; or, coating attachment of chemical functionalities on the core surfaces capable of imparting chemistry at the particle surface and the wafer. Preliminary polishing data using the described treated abrasives will be discussed.

2:00 PM M2.2
AN EVALUATION OF THE EFFECTS OF NEWLY DESIGNED ABRASIVES IN CMP SLURRY. Nobuo Kawanishi and Masayuki Hattori, JSR Corporation, Fine Electronic Research Laboratory, Yokohama, JAPAN.
Newly designed abrasives with various particle morphology and components have been prepared and evaluated in terms of CMP polish efficiency. Polymer spheres with uniformed particle size and special functional groups were prepared by soap-free emulsion polymerization. CMP slurries with these polymer abrasives indicated decreased dishing, erosion, and defectivity for metal and dielectric surfaces. This study has also been conducted with a preparation of composite particles consisting of a polymer core covered with inorganic composition such as silicon monoxide, titanium compound, AlOx, etc. The controlled hydrolysis and hetero-coagulation systems were proposed as preparation methods of composite particles. The thickness, morphology and state of the deposited layer could be altered by adjusting concentrations of the reactant and nucleus of metal compounds, pH of the aqueous solution, aging temperature, silane coupling agents, etc. These composite particles were particularly useful in preventing scratching of low dielectric material surfaces during a CMP process.


The presentation describes the evolution of a single-step Cu CMP slurry/formulation. Descriptions range from procedures for screening chemical components to analysis used in final optimization of a commercial product to process simulation on a CMP polisher. Emphasis is on the relative importance of individual parameters. The content of this presentation is based on the fundamental methods of chemical analysis, including UV/Vis and FTIR spectroscopy, pH/conductivity measurements, 1CP/OES elemental analysis, ion exchange chromatography and DC electrochemistry. Information includes insights on surface chemistry of metal oxide abrasives and how it affects metal removal, removal of metal complexes in aqueous mixtures, issues of galvanic interaction between Cu and barrier materials and to what extent pattern density becomes a factor. A comparison of laboratory results with process simulation on a CMP polisher is shown with data including performance metrics such as removal rates, dishing, erosion, and thinning.

24:45 P M M.4 HIGH PERFORMANCE CMP SLURRY WITH INORGANIC/RESIN ABRASIVE FOR Al/Low k DAMASCENE, Hisayuki Yone, Yukimaru Matsui, Gaku Minamisawa, Toshiba Corporation, Semiconductor Company, Yokohama, JAPAN; Nobuo Kurosashi, Masayuki Hitori, JSR Corporation, Fine Electronic Research Laboratories, Yokohama, JAPAN.

Damascene is an attractive wiring process for wire-level integration and yield enhancement. But CMP still has many issues like scratch, planarity and corrosion. Meanwhile low dielectric constant (low k) material is going to be introduced as interlayer dielectrics (ILD) to improve device performance. However, the mechanical strength of low k material increases concerns like scratch and planarity. So, a new concept is introduced to the CMP slurry abrasive.

The new abrasive is composed of resin particle coated with inorganic particles. Therefore, the properties of resin/Resin and resin/inorganic are mainly come from the elasticity of the resin. The soft resin particle behaves as a cushion and prevents the scratch caused by agglomerated inorganic particles and foreign material. The springy feature of the resin particles absorbs the selectivity and erosion on the via and contact portions for laminate and high-k materials. Furthermore, the pressure is loaded to high k film surface effectively through the resin particle and high k CMP rate can be achieved even without chemicals like oxidizers. This chemical free polishing would be the advantageous in preventing the corrosion of Al.

In this paper, the polishing mechanism of Inorganic/Resin abrasive and the results of Al/Low k Damascene will be presented.

3:00 P M M.5 OXIDE POWDERS FOR CMP PRODUCED BY CHEMICAL VAPOR SYNTHESIS. Hermann Sieger, Markus Winterer, Horst Hake, Darmstadt University of Technology, Materials Science Department, Thin Films Division, Darmstadt, GERMANY.

Ultra-fine, non-agglomerated oxide powders are produced by chemical vapor synthesis (CVD). In the CVD process volatile metallic precursors are decomposed in a hot wall reactor with a well defined reaction zone at reduced pressures forming nano-sized powders with a narrow size distribution. An inherent advantage is the modular design of the growth chamber which enables the production of Al2O3, doped and coated silicon powders with improved volume and surface properties, e.g. dielectric constant, dielectric constant, hardness, chemical reactivity or dispersibility. In order to correlate CVD product characteristics with CMP performance, powders are investigated by nitrogen adsorption, TEM, XRD, aqueous dispersions by zeta potential and size measurements and polished surfaces by HRSEM and AFM.


Slurries containing silica abrasive produced by varying processes are compared for polishing performance. The relationship between the physical and chemical character of silicas and polishing performance with copper, tantalum, and oxide were examined. The effects of morphological parameters and surface chemistry on removal rates, selectivity, stability, and post-polishing cleaning will be discussed.

4:00 P M M.7 SYNTHESIS OF ALUMINA SLURRIES FOR DAMASCENE POLISHING. Byung-Chen Lee, David J. Duquette, Ronald J. Gutmans, Remscheid Polytechnic Institute, Center for Integrated Electronics and Electronics Manufacturing, Troy, NY.

Model alumina slurries have been synthesized using fundamental electrodissolution and surfactant adsorptions, along with characterization of blanket copper wafers after chemical-mechanical planarization (CMP) processing. A model slurry was established containing 3 wt% alumina (50 nm nominal size), 2 wt% potassium dichromate and 1 vol% DOWFAX 2A9, as abrasive, oxidizer, and amionic surfactant, respectively, which resulted in copper removal rates of 120 nm/min with smooth, low-defect, high-K dielectric surfaces without aggressive post-CMP cleaning. When used with a model silica abrasive to remove the Ta liner, well-defined damascene patterned structures were achieved with low-particle defect densities. The principal techniques used in developing the model alumina slurry include the following: open circuit potential measurement, potential dynamic polarization, capillary hydrodynamic fractionation (CHDF) particle size analysis, surface tension measurement, and zeta potential measurement. The paper will include variations obtained with alternative alumina abrasives, alternative oxidizers and alternative surfactants to illustrate the synthesizing principles. The use of this approach in developing a slurry for the Ta liner will also be described.

4:30 P M M.8 THE IMPACTS OF ADDITIVES ON IODINE-BASED SLURRY ON COPPER CHEMICAL MECHANICAL POLISHING. Seung-Mahn Lee, Zhan Chen, and Rajiv K. Singh, Department of MSE and Engineering Research Center for Particle Science and Technology, University of Florida, Gainesville, FL.

Copper CMP has now been recognized and accepted as the process that is capable of providing the planarity to build multilevel interconnects schemes with below quarter-micron lines. One of the key issues in copper CMP is the development of slurries which can provide high removal rates, good planarity and high selectivity. In our previous presentation, the possibility of the use of iodine slurry for copper CMP was introduced. Iodine slurry showed the highest removal rate and relatively good planarity. In this presentation, we have investigated the effects of additives in iodine slurry in order to control the removal rate of copper and surface quality. Since BT and TaN/SiO2 are well known as high and selectivity surface, respectively, both additives can be used to retard the surface reaction rate and dissolution rate of copper and to enhance the surface quality. From the results, it is observed that Cu-BTA layer is formed uniformly on the surface, which protect the further corrosion of copper. In addition, surfactants were very effective to control the removal rate and surface quality. Then, for better understanding of the high removal rate of copper in iodine based slurry, friction force measurements and nano-scratch tests in solutions were conducted. These results were compared to hydrogen peroxide based slurry.

4:45 P M M.9 SELF-ASSEMBLED SURFACTANT MEDIATED DISSOLUTION OF NANOPARTICULATE SYSTEMS FOR CHEMICAL MECHANICAL POLISHING (CMP). Pankaj K. Singh, Joshua J. Adler, Bahar Basim, Yakov I. Rubinovich, and Brj M. Moudgil, Department of Materials Science and Engineering and Engineering Research Center for Particle Science and Technology, University of Florida, Gainesville, FL.

The current interest in using different types of ultrafine (nano-sized) powders for Chemical Mechanical Polishing (CMP) under severe conditions such as high salt, chemical additives, and high pressure, puts a high demand on suspension processing. Traditional dispersing methods such as sonication and polymeric dispersants may not perform adequately under the conditions encountered in CMP. Surfactant solutions can provide a feasible alternative for stabilization
of ultrainfared particles. The barrier to aggregation in presence of surfactants was measured using atomic force microscopy and the barrier height determined through a size analysis to find that the barrier was several orders of magnitude higher in presence of micelle-like self-assembled surfactant aggregates, as compared to barrier expected from electrostatic interactions. The results indicate the presence of barrier due to the adsorbed micelles on the surface, the strength of the barrier increasing with increasing strength or compactness of the adsorbed micelle. The origin of these forces was explored through techniques such as adsorption, contact angle, and potential measurements. Attributed to Total Reflection Fourier-Transform Infra-Red Spectroscopy (ATR-FTIR). In previous studies, unstable slurries were observed to cause significant surface deformation during silica CMP. Polishing was carried out using silica slurries and a specific slot stack to minimize surface damage and maintain a reasonable material removal rate. The size of particle and polishing pressure was also examined.

SESSION M3: COPPER CMP / SPI AND PLANARIZATION I
Chair: James G. Byrne, Ronald J. Gutman
Thursday Morning, April 19, 2011
Golden Gate A1 (Marriott)

8:30 AM M3.1
INTERPLAY BETWEEN COPPER ELECTROPLATING AND CHEMICAL MECHANICAL PLANARIZATION I: Akihiko Hongo, Yasuake Chikamori, Tassuyu Kohama, Koji Shimizu, Norio Kimura, Elbara Corporation, Fujisawa, Japan; David K. Watanabe, Elbara Technologies, Inc., San Jose, CA.

The introduction of Chemical Mechanical Polishing (CMP) into semiconductor device processing brought a significant need for wet chemical research and development in this industry. With the transition from aluminum to copper for advanced interconnect metallization came a tremendous amount of electrochemical research towards developing a production worthy copper CMP process capable of meeting the stringent specifications of dual damascene integration. In addition, the dual damascene integration scheme introduced copper deposition challenges that brought significant activity in developing another wet chemistry process, electroplating. These two sequential, chemical processes have been shown to have significant interaction that has created significant challenges in process integration. We present here some of the copper electroplating and copper CMP results from development efforts at Elbara that highlight the process integration challenges between these two processes. For example, a non-uniform copper plating pattern observed during copper CMP can be compensated for in the CMP process but may be indicative of non-uniform deposition, or demonstrate the need for a post deposition anneal that gives a more uniform distribution of copper microstructure across the wafer. Compositional changes to copper electroplating bath chemistry can achieve high aspect ratio, high copper voids/pits, or transient changes in copper structural and compositional properties, will be presented and discussed.

9:00 AM M3.2
EFFECT OF COPPER FILM SURFACE PROPERTIES ON COPPER CMP REMOVAL RATE: Yi-Chun Wang, Rajeev Bajaj, Gary Lan, Yaewli Dorai, Doyle Bennett, Fuyun He, Applied Materials, CMP Division, KU, Santa Clara, CA.

It has been observed that CMP (chemical mechanical polishing) removal rate of copper varies for films from different sources. While the film hardness and their wet etch rate in absence of inhibitor are similar, the wet etch rate in presence of inhibitor are significantly different. Analysis by AFM, XPS, and ion beam sputtering showed the film roughness and surface composition are different within the range of 110 angstroms deep. The different CMP removal rates are synergistic effect of copper film roughness (grain size), surface composition, and effective adhesion of inhibitor. Once polishing is initiated by an aggressive polishing step, removal rate of the remaining copper films becomes less different. Based on these findings, the polishing slurry and process were further optimized.

9:15 AM M3.3
COPPER CMP FOR DUAL DAMASCENE TECHNOLOGY: SOME CONSIDERATIONS ON THE MECHANISM OF Cu REMOVAL: David Wei, John M. Boyd, Hugh Li, Yehiel Gotsis, Stephen Jee, Joseph Li, KY. Ramanjaney, and Rodney Kistler, Lam Research Corporation, Fremont, CA.

Copper Dual Damascene (Cu2D) technology becomes the process of choice in semiconductor manufacturing. The Cu2D sequence includes multiple use of CMP both for dielectric planarization and for shaping planarized wires. The Cu2D CMP ability to remove Cu CMP burden materials leaving the wafer surface as flat as possible. The planarization task in Cu-CMP is more challenging than in other CMP processes due to larger topography variations, and it has to be accomplished twice: while the planarization Cu CMP process deposits thin film of Cu into the intermetallic Cu/CuCl layers generated by the reaction of Cu and planarization Cu CMP slurries. The H2O2 concentration determines the mechanical and chemical properties of surface oxide species and their removal. High concentration of H2O2 is required for the oxidation of remaining Cu surface films, and then decreases again. The values of open circuit potential plotted in the pH-pH diagram clearly show that the surface Cu2O is formed at lower H2O2 concentration and CuO at higher ones. The formation of different Cu-oxides was confirmed by XPS analyses.

9:45 AM M3.5
ANALYSIS OF COPPER TO TANTALUM TRANSITION IN COPPER CMP J.M. Kang, Shaoyu Wu, T. Selviah, and P.D. Foo, Institute of Microelectronics, DSIC-MD Department, SINGAPORE.

The evolution from Cu to Ta surface during Cu CMP has been investigated. As a first step of Cu CMP, removing excess Cu on field area to Ta often gives rise to topography issues such as dishing or erosion. The exposure of Ta is detected by in-situ reflectance measurement, where the downward slope start indicates the start of Ta exposure. For blanket wafers, the minimum remaining Cu thickness at slope start increases with initial Cu thickness. Applying lower polishing pressure and slower speed, so-called soft polishing, near the Cu-Ta transition stage results in thinner remaining Cu. In patterned wafers, Ta exposure starts near high pattern density areas such as field lines. This, contrary to blanket wafers, remaining Cu thickness at slope start cannot be correlated simply with initial Cu thickness. In this experiment, with increasing initial Cu thickness, remaining Cu thickness at slope start decreases. The amount of dishing is largely proportional to the initial Cu thickness. Applying soft polishing results in thicker remaining Cu than polishing without soft polishing in blanket wafers. However, polishing without soft polishing causes more dishing. Total-idealized range (maximum remaining Cu thickness
maximum distance on 100 pm trench) after first step ranges from 8-26 to 1457 A according to the initial Cu thickness, over polishing and whether soft feature has been applied or not.

10:50 AM *M3.6* ANALYSIS OF CMP PLANARIZATION PERFORMANCE FOR STI PROCESS: Manabu Tsujimura, Ebara Corporation, Tokyo; JAPAN; Masanori Mutsui, Hiroki Hiyama, Ebara Research Co., Tokyo; JAPAN; Masahiro Ota, Tokyo Metropolitan University, Tokyo; JAPAN.

CMP has now been adopted not only for ILD and W-plug, but also for Cu metal and STI. In the STI CMP process, the wafer has some defined wafer, and it has recently been reported that this wafer can significantly affect the planarization results. The principle purpose of CMP is to planarize relatively large rather than relatively small topography. Therefore, there may be a range of wafer topography in which the wafer pattern may be overpolished, depending on its peak-to-valley and freehand measurements. The second region is referred to as the "wafer material region." In this region, uniform polish is required. The third region is referred to as the "non-uniform material region." In this region, the planarization of the wafer is required. The principle purpose of CMP is to planarize the wafer, which is in turn calculated by FEM. In this analysis, CMP is defined as four types of regions. The first is the "wafer material region," the planarization performance of which is required.

11:00 AM *M3.7* A STUDY ON STI AND DAMASCENE CMP USING CHIP LEVEL SIMULATION: Kyung-Hyun Kim, Yoo-Hyun Kim, Chang-Kong Moon, Moon-Hyun Yoo, Jeong-Lim Nam, Jeong-Taek Kong and Sung-In Lee, Semiconductor R&D Center, Samsung Electronics Co. Ltd., Korea.

Modeling and simulation of Chemical Mechanical Polishing (CMP) are essential not only for understanding the physical mechanisms, but also for optimizing the process integration. Notwithstanding the prevalence of data regarding the planarization performance of CMP, it has been shown that a single material, e.g., an oxide film, that is dual type of material can be more complicated. The depth of knowledge of the effective polish rate in patterned regions and the effect of the material on pattern erosion in a CMP of STI/Damascene structure, in fact, raises the level of complexity in both the modeling and the numerical analysis based on chip level simulation. In this work, we present a methodology that describes the effective polish rate in patterned regions and the effect of the material on pattern erosion in a CMP of STI/Damascene process, and show that the above method can be used to predict the pattern erosion under various process related factors, such as, wafer selectivity, wafer selectivity, wafer selectivity, wafer selectivity, and wafer selectivity.

11:15 AM *M3.8* CONTINUOUS INVESTIGATIONS INTO THE PECULIARITIES OF CMP: USE OF CHEMICAL-DEPOSITION LAYERS: David J. Beek and Dale L. Hetherington, Sandia National Laboratories, Albuquerque, NM; Michael R. Oliver, Rodol, Inc., Newark, DE.

Previous work has discussed a novel ILD deposition technique which, when used with an experimental cerabased slurry, produces a self-regulating CMP process that minimizes pattern density effects. Specifically, the ILD deposition process involves varying the silicon content of the film as a function of the film thickness. The ILD process is based on the assumption that, if a low silicon content film is deposited on top of a high silicon content film (which is deposited directly on the metal), the high content film will stop the CMP process. Specific data that was presented included the polish rate of these films using both an experimental cerabased slurry and a standard fumed silion CMP slurry. Other data showed the chemical differences between the various ILD films, showing the potential of the films before and after CMP, and nano-indentation studies of the ILD films. Ceria particles of various sizes and iso-electric points were investigated using both the silicon-rich films described above and thermally grown silicon dioxide films. The dramatic differences in polish rate were found to be not only a function of the silicon content of the oxide but also the iso-electric point of the ceria particles and the pH of the slurry. The secondary particle size was also found to have an effect. Polish rate data will be presented. Precision indentation measurements between ceria and silicon particles and various oxide surfaces and pad materials obtained from in-situ lateral and adhesive atomic force microscopy experiments will also be presented and discussed.

11:45 AM *M3.9* CHARACTERIZATION AND CONTROL OF COPPER CMP WITH OPTOELECTRONIC METROLOGY: Michael Gostein, Michael Jeffe, Alex A. Maznev, Philips Analytical, Natick, MA; Paul Lefever, International SEMATECH, Austin, TX.

The silicon IC industry is rapidly moving to adopt copper as the material of choice for circuit interconnects. Because of the lack of etching processes to remove copper, these interconnects must be patterned with a Damascene process, in which copper is deposited over a film with trenches etched in an insulating material and the excess copper is then removed with chemical-mechanical polishing (CMP). The challenge for developers of copper CMP processes is to obtain a process that polishes the film uniformly across 200-300 mm wafers, minimizes copper dishing and dielectric erosion, and polishes uniformly on structures with widely varying density of copper-filled trenches. Optoelectronic metrology provides a valuable tool for CMP process development and control, by enabling non-contact metrology of copper thickness on both the back and the front of the wafer. Unlike profilometry, which measures only surface topography, the optoelectronic technique measures metal thickness. It can be used at all stages of polishing, from measuring the uniformity of wafers prior to polishing, measuring removal rates at intermediate polishing stages, and measuring final post-polish thickness of test pads and arrays of submicron trench. In this presentation, we will demonstrate that optoelectronic metrology provides unique process control, e.g. determination of planarization length and measurement of remaining film at intermediate stages of polishing. The rapid (~1 second per site), non-contact measurement is also ideally suited for in-line control of copper CMP process uniformity.
CME USING MESA™, Thomas Laursen, Inki Kim, Jim Schuster, SpeedFam-IPEC Incorporated, Chandler, AZ; Scott Rammels, Scott Rammels Consulting, San Antonio, TX.

MESA is a feature-scale planarization model developed by SpeedFam-IPEC (SFI), in conjunction with Southwest Research Institute, for describing the chemical mechanical polishing (CMP) process used in IC manufacturing. This model has previously been applied to the poly of inter-level dielectrics and copper CMP. The present study is part of an experimental validation for shallow trench isolation (STI). STI is a technique for creating air gaps between the underlying wafer and the阻挡 layer below the silicon level. The PD effect is evident in both cases, and a comparison between the two pads shows less PD effect and improved planarization with the single IC 1000 pad. MESA has been shown to predict the details of the topographical evolution for STI CMP on the feature scale. When validated by fitting the pad constants, k1 and k2, to describe the planarization, MESA is expected to provide accurate predictions for the polish of any oxide pattern structure as long as the same CMP process is used.

2:15 PM M4.3 MODELING POST-PATTERN DEPENDENCIES IN MULTI-LEVEL COPPER CHEMICAL-MECHANICAL POLISHING PROCESSES. Tamba E. Taghavae, Tae H. Park, Duanne S. Boning, Microsystems Technology Laboratories, MIT, Cambridge, MA; Paul Letier, SEMATECH, Austin, TX; Lawrence Camilletti, Comenius Systems, Newport Beach, CA.

Chemical mechanical polishing (CMP) has become a necessary process step in fabricating multilevel copper interconnects. Copper CMP is recognized to suffer from pattern dependent problems such as polishing, erosion, which cause increased line resistance and non-uniformity within the die, for a given metal level. The non-uniformity increases with metal level one that is caused by the post-CMP pattern-dependent thickness in multilevel copper CMP. The model is an extension of our earlier model for single level metal CMP processes [1]. It is built on the premise that copper CMP processes are more enhanced on the polished surfaces and views copper CMP processes as comprising of three intrinsic stages: bulk copper removal, barrier removal, and overpolish stage. The model takes into account the initial long-range electroplated copper topography, the pattern density, and the initial depth of the wafer. It is calculated that the PD effect is considerable and could lead to complicated polishing and erosion after CMP on metal level two. This will degrade the attainable planarity on higher metal levels, and will certainly cause integration and manufacturing problems.

Predictive pattern dependent models of copper CMP processes are therefore highly desirable for use in optimization of a manufactural flow, as well as for developing interconnect design rules, among other things. We have derived a mathematical model that determines the post-CMP pattern-dependent thickness in multilevel copper CMP. The model is an extension of our earlier model for single level metal CMP processes [1]. It is built on the premise that copper CMP processes are more enhanced on the polished surfaces and views copper CMP processes as comprising of three intrinsic stages: bulk copper removal, barrier removal, and overpolish stage. The model takes into account the initial long-range electroplated copper topography, the pattern density, and the initial depth of the wafer. It is calculated that the PD effect is considerable and could lead to complicated polishing and erosion after CMP on metal level two. This will degrade the attainable planarity on higher metal levels, and will certainly cause integration and manufacturing problems.

Chemical mechanical polishing (CMP) is an essential process for achieving a high degree of planarization. The planarity after CMP depends on the pad surfaces, the pad density, the mechanical properties of polishing pads and the polishing process properties. In order to simulate the topography after CMP, a numerical model with the pad surface soft layer had been proposed. The model should be very useful not only for the topography simulation, but also for the development and the evaluation of new processes, i.e., new CMP pads and new polishing pads. Based on the good agreement between the numerical model and the physical model, its applications for oxide CMP and metal CMP will be presented in this paper. Application for the newly based skry process, which has a non-linear dependence of the polishing rate and a self-stopping property, and application for the metal CMP with high selectivity will be discussed.
In a previous MIP model, the effects of both chemical and abrasive slurry concentration on the polishing rate were well explained, for constant polishing pressure and velocity. This model is extended here to consider specific descriptions of mechanical abrasion, including Preston and non-Preston expressions. Predictions of behavior are compared to literature results, leading to an improved understanding of the abrasive process in CMP.

4:30 PM M4.9
WATER NANOGRAPHOPY EFFECTS ON CMP: EXPERIMENTAL VALIDATION OF MODELING METHODS
Brian Lee, Dusan Boring, Massachusetts Institute of Technology, Dept of Electrical Engineering, Cambridge, MA; Winstone Bayles, BayTech Group, MA; Noel Poyada, The Hester, ADE Corporation, Westwood, MA; John Valley, Chris Kolipolus, ADE Corporation, Phase-Shift, Tucson, AZ, Dale Hetherington, Sundia National Laboratories, Albuquerque, NM; Hong-Jiang Sun, Philips Semiconductors, Albuquerque, NM; Michael Lacy, Lam Research, Fremont, CA.

NanoGRAPHOPY refers to 1.4-1.6lbfm surface height variations that exist on a lateral millimeter length scale on patterned silicon wafers. Chemical mechanical polishing (CMP) of deposited or grown films (e.g., oxide or nitride) on such wafers can generate undesirable film thickness variations, which can be of substantial concern in shallow trench isolation manufacturability. Proper simulation of the effect of nanoGRAPHOPY on post-CMP film roughness is needed to help in the measurement, analysis, diagnosis, and correction of potential problems. Our previous work has focused on modeling approaches that seek to capture the thinnest and post-CMP film thickness variations that are affected from nanoGRAPHOPY. Analysis has been performed using a density and step-height-based CMP model, as well as our previously published model. The importance of these height scale of the CMP process used (planarization length) to the length scale of the nanoGRAPHOPY on the wafer (nanoGRAPHOPY length) has been investigated. In this paper, we report on experimental experiments using sets of 300mm epi wafers with a variety of nanoGRAPHOPY signatures (i.e., different nanoGRAPHOPY lengths). Sets include single-sided and double-sided polished wafers, upon which a 1 micron oxide film is thermally grown. These wafer sets have been polished using different CMP processes, and the effects of varying nanoGRAPHOPY lengths are included in each wafer set. Extracted planarization lengths using these wafers ranged from 1.5mm to nearly 10mm. Experimental results indicate a clear relationship between the relative scales of planarization length vs. nanoGRAPHOPY length: when the planarization length is less than the nanoGRAPHOPY length, little thinning occurs; when the CMP process has a large planarization length, surface height variations are transferred into thin film thickness variations. In addition to presenting these experimental results, modeling of the nanoGRAPHOPY effect on dielectric CMP processes will be reviewed, and measurement data from the experiments will be compared to model predictions.

4:45 PM M4.10
SLURRY DETECTION AND TRANSPORT DURING CHEMICAL-MECHANICAL POLISHING OF COPPER
Ying Li, Sarah Namikawa, S.V. Babu, Dept of Mechanical and Chemical Engineering, Center For Advanced Materials Processing, Clarkson University, Potsdam, NY.

Although significant progress has been made in slurries development and process optimization, one important issue, i.e., the slurry transport between the wafer and the pad during polishing, still needs in-depth investigation. The slurry transport not only affects directly the chemical reactivity of the slurry by influencing the steady state concentration of the various chemicals and abrasives between the pad and the wafer, but also the efficiency of mechanical abrasion of the particles. This work investigates the retention and transport of chemical species and abrasive particles during copper CMP. "Slurry step-flow" experiments, in which the concentration of the chemicals and abrasives in the slurry are altered in a step change during polishing, are conducted with slurries containing different chemicals, such as ferric nitrate, hydrogen peroxide and potassium iodide. Results from these experiments that shed light on the role of abrasives and chemicals during the polishing will be presented.

SESSION M5 POSTER SESSION
Thursday, April 19, 2011 8:00 PM
Salon I.7 (Marriott)

M5.1
IN SITU LATERAL FORCE MEASUREMENT DURING CHEMICAL-MECHANICAL POLISHING
Wonseop Choi, Seung-MuHun Lee, Rajiv K. Singh, Department of MSE and Engineering Research Center for Particle Science and Technology, University of Florida, Gainesville, FL.

A variety of in-situ measurement techniques were developed and employed in CMP. However, despite the availability of these measurement techniques, the in-situ measurement of frictional forces has not been developed to monitor mechanical effects in CMP environment under solid loading conditions and the need to understand the fundamental aspects of the process is also important. In our previous work, the frictional force of stationary wafer without solid loading has been studied. In this talk, frictional forces under real CMP conditions with solid loading and rotational wafer have been investigated. An in-situ lateral force measurement apparatus was modified to be suitable for real CMP condition. This apparatus measures frictional force at the surface of the wafer sample and the polishing pad under different solid loading conditions. Experiments were done in polishing of silicon wafer using silicon slurry and polishing of copper wafers using alumina slurry. The friction force measurements, which were a function of time and process parameters, were correlated with the change in surface characteristics of the polished wafers. Atomic Force Microscopy (AFM), Ellipsometry, and Four-point probe were used to characterize the samples before and after the experiments. The results showed the better understanding of the frictional force mechanism occurring at the wafer-pad interface under different solid loading conditions during CMP.

M5.2
CMP-RELATED AND CMP REVEALED SHORT- AND LONG-RANGE INTERACTION INTERACTIONS IN COPPER DUAL DAMASCENE TECHNOLOGY
Yuchun Gokids and Rodney Kistler Lam Research Corporation, CMP/CELNTechology Division, Fremont, CA.

More than 3 years passed since IBM made their official announcement on Copper Dual Damascene (Cu2D) technology, drawing the semiconductor world in the Cu2D rush. Nowadays, more than 3 years of extensive R&D work, the EOL yields are still too low, and a lot of process integration work still has to be done to make it FAB ready. At this phase the key to success is to link the problem to its root cause, which is frequently located at remote operation and it takes more efforts to discover the link than to fix the problem. CMP is one of the most, if not the most, critical yield affecting operation in Cu2D technology. Going through all metal deposits and touching the dielectric, CMP is performing a kind of reversed processing. In this sense it could be considered also as a quality control procedure, capable to reveal problems related to other process steps. Additionally to known Cu/oxide losses and form particular defectivity, other CMP-related or CMP-revealed yield affecting issues are discussed in details scratching, micro-etching, corrosion, non-removed residuals, voids and pits, barrier integrity damage, oxide, depressions/dislocations. Cu is a very soft material. In addition to slurry agglomerates and tool debris, two new classes of scratches, inorganic treated flakes and "rolling stones", leading in some cases to extremely repeatable regularly shaped effects, and so-called shallow "chemical" scratches, are observed. Copper is a polycrystalline material, that is a new challenge for CMP, and micro cracking at the intergran boundaries is discussed particularly in detail. Rough estimation of the number of intergran separations in a chip per one Cu level leads to a number as high as about one billion. Intergran boundaries are extremely mechanically and chemically vulnerable. Scratch forces and chemically aggressive media media in CMP process can be chemistry-assisted intergran cracking and stress-induced intergran corrosion. Irreversibly exposed of processed layers to corrosive conditions is inherent part of the CMP game. There are some specific spots of the Cu layer (pin-holes, micro-cracks, true- and pseudo-scratches, intergran boundaries, hidden stressed spots, voids, glnichemically active spots etc), demonstrating enhanced vulnerability to corrosion. What should be done to prevent corrosion damage in such conditions? In summary it is concluded that extensive work still has to be done to tune design rules, deposition, annealing and CMP to make the whole Cu2D back-end cluster self-consistent.

M5.3
A PLANARIZATION MODEL IN CHEMICAL MECHANICAL POLISHING OF SILICON OXIDE USING HIGH SELECTIVE CeO2 SLURRY
Jong-Wan Lee, Bo-Uk Yoon, SungRak Hah and Joo-Hee Min, IMC/SE Center, Samsung Electronics Co., Ltd., Kyungki-Do, KOREA.

As the design rule of IC device decreases high selective chemical mechanical polishing process for shallow trench isolation is becoming more important. One of the most promising slurry for high selective CMP is ceria based slurry. However, in the high selective STI CMP process on the real pattern wafer, unexpected increase in polishing time results due to the removal rate drop in specific areas. In this study, mechanism of planarization for the CMP of silicon oxide
using high selectivity ceria slurries was explored. A comparison study on silica, ceria, and high selectivity ceria CMP processes was carried out. At the onset of polishing, with slurry containing high selectivity ceria, the removal rate and fettling depth were higher than the bulk removal rate. As the surface of the oxide becomes planarized, removal rate exponentially decreases and converges to the bulk removal rate. However, in the high selectivity ceria case, the removal rate of silicon oxide in high area is constant and does not depend on the polishing time. This implies that the oxide polishing rate does not increase on the raised areas for high selectivity ceria. Polishing behavior is a function of the solid content of ceria and the removal rate for high selectivity were investigated. Although the removal rate increases with increase in solid content similar removal rate drop phenomena was observed. In the case of non-selective ceria slurry without the chemical additive, the reduction of removal rate was not observed. Therefore it is proposed that the ceria abrasive which is coated by chemical additive passivates the oxide of recessed area that removes the removal rate. On the basis of the result, it is known that the removal rate drop phenomena in ceria slurries is not caused by solid content but caused by chemical additive.

**M5.4 LAYOUT PATTERN DENSITY AND OXIDE DEPOSITION**

PROFILE EFFECTS ON DIELECTRICS CHEMICAL-

**MECHANICAL POLISHING.** Young-Bae Park, J.Y. Yoon, J.Y. Kim, W.G. Lee, Hyundai Electronics Industries Co., Ltd., SYSTEM IC R&D Center, Cheongju, KOREA.

Based on experimentally obtained interaction distance, new test masks for characterizing and modeling pattern dependent variations of the remaining thickness after chemical mechanical polishing (CMP) are designed. Using these masks, we characterize polishing behavior with layout pattern density and pitch variations. Also deposition profile effects are compared between PETEOS (Plasma Enhanced Tetra-Ethyl Ortho-Silicate) and HDP (High Density Plasma) oxide in STI (Shallow Trench Isolation) CMP. Both remained silicon nitride thickness and expected oxide pattern density considering deposition profile effects were in good correlation with respect to pitch variation for a constant layout pattern density. And the relation between the remained silicon nitride thickness and the true layout pattern density are deduced. Also, the remained thickness increases nearly linearly with the layout pattern density for a constant layout pitch, which can be explained from the simple pattern density model.

**M5.5 A CMP NUMERICAL MODEL COMBINING DIE SCALE AND FEATURE SCALE POLISHING CHARACTERISTICS.**

Stephanie Delage, Frank Meyer, Goetz Springer, Infineon Technologies, Munich, GERMANY.

Chemical Mechanical Polishing (CMP) has emerged as the leading process for global and local planarization in silicon integrated circuits fabrication. However, there remains a large number of variation and effects due to layout pattern, equipment, and process dependencies that are still poorly understood. An accurate characterization of the CMP modeling methodology is needed to facilitate the assessment and reduction of such variations. Several works have proposed models for Chemical Mechanical Polishing to provide various benefits. But most of them relate to the single process description (wafer/die/feature) and a lack of multiscale models remains. In this paper, a new numerical model combining die scale and feature scale polishing characteristics for oxide and ceria CMP is proposed. This work is based on the analytical effective density model proposed by D. Boning and al. [1], that takes into account a die scale pad deformation. We extend this model to include the description of the removal rate. A topography discretization allows us to describe the polishing in down areas more accurately, depending on the down area width. The physical parameters considered include the deformation of the polishing pad (die scale and feature scale), the removal rate of a blank areas under the same conditions, and the removal rate in down areas for small polishing times. Comparison of simulated results with MIT teststretches experiments is performed and evaluated. [1] D. Boning et al., “Pattern dependent modeling for Chemical Mechanical Polishers” JSSP Symposium P, Chemical Mechanical Polishing, San Francisco, CA, Apr. 1999

**M5.6 PRINTING BLANKET TO PATTERNED WAFER PERFORMANCE IN COPPER CMP.** S. Hymes, D. Traball, S. Chang, I. Butcher, B. Buyer, S. Storch, Ashland Specialty Chemicals, Dublin, OH.

A basic connection between blanket and patterned wafer performance is presented using a single fundamental assumption on the role of step height. Using idealized rate responses to downforce, the blanket wafer response of idealized slurries (both Prestonian and non-Prestonian) is used to develop expressions for planarization efficiency and dishing susceptility of patterned films directly applicable to traditional and Damascene CMP. Results for real Cu CMP slurries are then compared to the model in order to demonstrate the link between composition, blanket and patterned wafer performance.

**M5.7 CHARACTERIZATION OF A NEW CLEANING METHOD USING ELECTROLYTIC IONIZED WATER FOR POLY Si CMP PROCESS.** Naoto Miyashita, Meiji Univ., Dept. of Electrical and Electronic Engineering, Kawasaki, JAPAN; Toshiba Co., Semiconductor Company, Yokohama, JAPAN; Shin-Ichiro Oekusa, Meiji Univ., Dept. of Electrical Engineering, Kawasaki, JAPAN; Masako Kodera, Yoshitaka Matsui, Toshiba Co., Semiconductor Company, Yokohama, JAPAN; Satozuka Betts, Takashi Nishikawa, Mechanical Systems Laboratory, Toshiba Corporation, Suwakani, Kawasaki, JAPAN.

Recently, trench isolation technology has been developed and applied to bipolar LSI production. Especially, play-Si Chemical-Mechanical Polishing (CMP) technique has made much improvement on deep trench isolation. Major issues of the process integration for that purpose have been the post CMP cleaning process. In general, the wafer surface after a conventional CMP is contaminated with silicon particles and chemical impurities. These contaminations produce some unexpected patterns and crystal defects in the wafer surface layer after oxidation. It is difficult to remove them by the conventional cleaning technique. Therefore, we have established the new post CMP cleaning method, using the electrolytic ionized water containing chemical additive of a small quantity. The anode water has the cleaning effect for the metal and organic contamination, and the cathode water has the removing effect for the particles and the etching surface. For this new cleaning process, it is important to avoid the chemical mechanical damages on the surface and control the surface roughness. Our experimental work has been focused on the numbers of the remaining particles, the contamination concentration, and the surface roughness using AFM. We herein report the properties of the electrolyzed water and the examined results of poly-Si surface after CMP process. It was found that the electrolyzed water is effective for surface control, and the new cleaning process is useful for CMP process.

**M5.8 ENGINEERED POROUS AND COATED SILICA PARTICULATES FOR CMP APPLICATIONS.** K.S. Choi, R. Vermaat, J. Grey, N. Bnaim and R.K. Singh Department of Materials Science and Engineering and Engineering Research Center for Particle Science and Technology, University of Florida, Gaineville, FL.

The aim of this study has been to synthesize the micro porous silica spheres and to coat m-synthesized SiO2 with CeO₂ for CMP applications. First, spherical micro porous silica powders with a narrow size distribution have been prepared by precipitation technique involving the hydrolysis reaction of silica alkoxide in ethanol. The interparticle microporosity has been created by adsorption of an organic compound (glycerol). The presence of glycerol during the synthesis affect considerably the precipitation mechanism and its effect on the particle size will be discussed. The synthesis of silica micro porous spheres of narrow size distribution yielded the preparation, by varying particle size and porosity, of a wide range of aqueous silica slurries. The influence of particle size, particle size distribution, porosity and particle concentration will be discussed in chemical mechanical polishing applications. Although silica particles show large plastic deformation than the bulk materials, very good glass polishing rates are obtained due to the plastic deformation of the silica layer during CMP. Silica particles are suitable candidates for application in CMP because silica particles can be directly precipitated as monodisperse spheres, their narrow size distribution being an important requirement in CMP applications. Secondly, m-synthesized silica particles were coated with the cerium dioxide particles having hexagonal shape, which were precipitated by decomposition of the complex particles. For this study, three coating processes were introduced to investigate the best coating parameters. Improvements in CMP of glass were also obtained by coating silica particles with cerium oxide nanorods.
While the minimization of device size in integrated circuits promotes greater integration densities and packing densities, it also introduces problems with increased resistance-capacitance delays due to the high resistance of the small dimension metal lines, and the increased interline capacitance. Efforts to reduce the delay have resulted in the move to copper interconnects, as well as the development of new low k dielectric materials to reduce line to line capacitance and cross talk noise. The novel properties of the latter materials have resulted in significant challenges in their integration into these small interconnects. This paper will report on the challenges and advances in the chemical mechanical polishing of low k organic and inorganic interlayer dielectric materials. Particular emphasis will be placed on the dependence of the polishing behavior of these materials on the chemical parameters of the slurry, such as the type and size of the abrasive particles.

9:00 AM M6.2 CHALLENGES IN DEVELOPMENT OF MANUFACTURABLE COPPER AND LOW k DIELECTRIC CMP PROCESS. Yongik Moon, David Msi, Kupina Whicoek, Fritz Redeker, Rajvej Bajaj. Applied Materials, CMP Product Business Group, Santa Clara, CA.

As the feature size of microelectronic devices shrinks down to sub-0.18 micrometer, the clock speed delay caused by resistance (R) and capacitance (C) of the interconnection is higher than the gate delay. This interconnection concern requires new materials for multilevel and dielectrics to reduce RC delay and Copper (Cu) and lowk dielectrics become the possible candidates to meet this demand. This study focuses on the development of manufacturable and robust CMP process for Cu and lowk material needed in Cu damascene process. There have been many challenges in implementing Cu and lowk CMP for manufacturing advanced microelectronic devices. High density and low density Cu surface damage and absence of post-CMP cleaning process of lowk materials. The main cause of high density and low density Cu and lowk integrated devices is the high dielectric damage loss during CMP due to the weak material property of lowk dielectrics. In this study, different copper and barrier removal slurries were evaluated. Each slurry combination was evaluated for topography and defectivity. Cu and barrier removal slurries were tested in Cu and lowk integrated pattern wafer polishing. Both processes offer different trade-offs in topography and defectivity. Due to the weak material property of lowk dielectrics, substantial amount of surface damage is created during CMP. This surface damage causes bonding failure of the following deposited layer and eventually results in the unreliability of microelectronic devices. The surface damage appears mostly along the edges of the wafer due to the high friction force by the direct wafer-pad contact. By using differentiated pressure distribution on and around the wafer surface, the surface damage along the wafer edges has been dramatically decreased. This is the result of the reduced contact between the wafer edges and the polishing pad surface. Post-CMP cleaning of low k dielectric materials is challenging because of its hydrophilic nature. A proprietary cleaning recipe was used to completely wet the low k dielectric material after CMP and keep the surface hydrophilic. The solution cleans both the dielectric and copper surface without leaving any residue or damage to copper surface. This study will detail the development challenges associated with the development of a multi-level Cu/Low k process. Future areas of development and improvement are identified.


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9:30 AM M6.4 CHEMICAL MECHANICAL POLISHING OF STEEL BY CARBON-CONTAINING THIN FILMS. Stephen J. Harris, Gordon G. Kranas, Ford Research Labs, Chemistry Dept., Dearborn, MI.

The material removal rate during polishing of steel by diamondlike carbon (DLC) and boron carbide (B4C) films falls by as much as four orders of magnitude during the course of several thousand polishing cycles. We provide quantitative information that describe the abrasion kinetics. Not only the steel but also the DLC and B4C films are polished in the process, even though the films are at least 3-3 times harder than the steel. AFM analysis shows that the B4C coating becomes atomically smooth over regions of 100 nm by 100 nm as it polish the steel. The polishing ability of the films is closely related to their nanoscale morphology but not to their microscale morphology. We provide evidence that the polishing of the films by the steel is primarily a chemical process, while the polishing of the steel by the film is primarily a mechanical process.

9:45 AM M6.5 CONTROL OF PATTERN SPECIFIC CORROSION DURING ALUMINUM CHEMICAL MECHANICAL POLISHING. Hyunjeong Kim, Paniki Kwon, Sukjye Lee, Hyung-Hwan Kim, Sungook Lee, Chul-Woo Nam, Seo-Young Song, Memory R&D Division, Hyundai Electronics Industries Co. Ltd., Icheon, KOREA.

A pattern specific corrosion of aluminum wires was found during aluminum chemical mechanical polishing process. This paper presents and discusses the particular pattern dependency of the corrosion behavior and effective control methods in order to reduce the corrosion. An aluminum single damascene structure on silicon dioxide thin film was prepared and the effects of process variables and pattern configuration on corrosion behavior were investigated. It was demonstrated that corrosion of aluminum wire was associated with the cleaning media and pattern configuration. Two approaches were made for preventing the pattern specific aluminum corrosion: by changing CMP consumables and post polish treatments, and by modifying pattern configurations. An optimized process condition was successfully evolved from such approaches and resulted in corrosion-free aluminum damascene structure. Electrical data was also collected and correlated with corrosion phenomena.

10:00 AM M6.6 DETECTION AND CLUSTERIZATION OF PARTICLE DYNAMICS IN MODEL CMP GEOMETRIES. Claudia Zettler and Minami Yoda, Georgia Institute of Technology, School of Mechanical Engineering, Atlanta, GA.

Chemical mechanical polishing (CMP), used to planarize silicon wafers, involves shearing an abrasive particle laden slurry between a rotating polishing pad and the wafer. The chemical and mechanical properties of the slurry, which consists of sub-micron colloidal particles suspended in a liquid lubricant, can greatly affect wear rates and material selectivity in CMP. The particle dynamics in a model CMP geometry were studied experimentally in this work. A technique for directly measuring the particle concentration near to the wafer surface was developed and used to evaluate how various particle properties affect this concentration. We hypothesize that increasing this particle concentration by manipulating both chemical and mechanical particle properties increases their tendency to stick to the wafer surface and hence CMP material removal rates. Evanescent waves were used to illuminate a roughly 300 nm thick region next to a solid glass surface. The surface, simulating the wafer, is fully filled with an aqueous dilute silica slurry. Simultaneous measurement of particle concentration next to the glass surface can be measured simply by counting particles. The effect of process properties such as particle size (diameters of 200 vs. 300 nm) and selectivity (polymer vs. silica particles), the presence or absence of van der Waals forces and shear rate on particle concentration will be investigated. The effect of pad roughness on the particle dynamics will also be studied by comparing results for smooth and periodically textured rotating silicon surfaces.
MODELING OF CHEMICAL-MECHANICAL PLANARIZATION (CMP) AND DEPOSITION PROCESS
Rajiv K. Singh, Zhen Chen, and Sung-Mo (Steve) Lee, MSOE, University of Florida, Gainesville, FL.

Although chemical-mechanical planarization (CMP) has successfully been employed in semiconductor device fabrication, the lack of comprehensive and quantitative understanding of CMP mechanism continues to hamper the development of efficient CMP processes. In this paper, we present a new model on CMP process, in which we emphasize on the role of the chemically modified layers on the wafer surface. We realize that the removal rate is a function of the formation and removal of the chemically modified layer. The chemistry in the slurry defines the formation rate of the chemically modified layer, while the removal rate is coupled with the abrasive wear and chemical reaction interaction. The obtained removal rate is thus the balance of formation and removal of the chemically modified layer under certain chemical and mechanical conditions. We categorized the real CMP mechanism into two categories: mechanically controlled, chemically controlled, and intermediate CPMs. The effects of chemistry, pressure, particle loading and particle size in different categories are discussed. The application of this model on tungsten CMP and copper CMP are also discussed in this paper.

A MODEL FOR EFFECT OF COLLOIDAL FORCES ON CHEMICAL-MECHANICAL POLISHING
Ali R. Manzheri and Goodarz Ahmadi, Department of Mechanical and Aeronautical Engineering, Clarkson University, Potsdam, NY.

It is well known that the variation of slurry pH can significantly affect the Chemical-Mechanical polishing Process. In this study, the mechanical model of the CMP process is extended by including the colloidal forces. It is shown that the double layer interaction and repulsion could overwhelm the other surface forces such as Van der Waals force, and thus, play a major role in Chemical-Mechanical Polishing (CMP) processes. It is found that the magnitude and sign of the zeta potentials of the surface and the abrasive particles significantly affect the removal rate. The results show that the removal rate increases sharply in the case of less zeta potential on the surface and abrasive particles have opposite sign. On the other hand, the removal rate decreases the zeta potentials have the same sign. The findings are compared with the available data and qualitative agreement was observed.

EFFECT OF ELECTROCHEMICAL INTERACTIONS ON REMOVAL RATES AND PLANARITY IN COPPER CMP
Dapeng Zhao, Vincent Hynes, Song Chong, Ben Beyer, Ionica Butea, and Wolves Sterte.

Copper CMP involves complex interplay between chemical and mechanical effects. In this study, we evaluate the performance of a number of slurry chemistries using a DOE approach and correlate the CMP performance to the chemical and mechanical interactions between the slurry and copper surface. The chemical interactions between the copper surface and the slurry are evaluated by static etch rate measurements and electrochemical measurements.

Parameters such as temperatures generated in the polishing, the ratio of removal rate to static etch rates and the slope of removal rates vs. polishing pressure were used to characterize the CMP performance. The results obtained on all of the conditions are successfully applied to understanding the CMP performance on patterned wafers.
semiconductor devices are scaled down, the number of manufacturing processes increases and the number of cleaning processes increases as well. The conventional RCA cleaning process consumes very large amounts of chemicals and ultra pure water (UPW). From environmental and commercial view points, it is clear that the cleaning process must reduce consumption of chemicals, UPW, and production costs. In this study, Si wafers contaminated with particles and metallic impurities were cleaned using the electrolyzed water (EW). Properties of generated EW such as oxidation-reduction potential (ORP), pH, and lifetime were measured. In order to compare the characteristics of anode water (AW) with those of cathode water (CW) of EW on DHF treated Si wafer surface, contact angles were also measured. pH and ORP of AW and CW were measured to be 4.7 and +1050 mV, and 9.8 and 750 mV, respectively. AW and CW were determined as oxidizing and reducing, respectively, and maintained their characteristics for more than 40 minutes. Contact angles of UPW, AW, and CW on DHF treated Si wafer surfaces were measured to be 65°, 66.5°, and 56.8°, respectively. Therefore, it was understood that CW was prone to wetting on hydrophilic-terminated surface. AW was effective for Cu removal, while CW was more effective for Fe removal. The particle distribution after AW and CW cleaning showed the applicability for 0.1 μm particle removal. It is hence promising that this cleaning technology will be very effective for promoting environment, safety, and health (ESH) issues in semiconductor manufacturing.

2:00 PM M7.3 POLISHING AND CLEANING OF LOW k DIELECTRIC MATERIAL FOR HD AND DAMASCENE. Yuchun Wang, Rajeev Bujajj, Yonguk Moon, David Msi, Kapila Wijesek, Yufei Chen, Fritz Redeker, CMP Division, Applied Materials, Santa Clara, CA; Dan Sager, L. Qu Xin, EVD Low K Division, Applied Materials, Santa Clara, CA.

This paper describes CMP challenges in development of Cu-low k technology. As copper-Tos/FGS schemes are being implemented successfully in early manufacturing, development focus has shifted to Cu-OSG integration development. Cu-OSG presents unique challenges with CMP integration, as these films tend to have much lower hardness than silicon dioxide. Significant process challenges have to be overcome prior to successfully implementing CMP process which does not mechanically damage the softer films and at the same time can achieve planarization requirements expected from CMP process. In addition, the OSG films tend to be hydrophobic leading to a need for developing improved cleaning processes/consumables. It was determined that AMAT ElectropolishingTM barrier sputter is extendable to OSG films. Good removal rate and removal profile can be achieved with ElectropolishingTM. A proprietary cleaning solution reduced defect counts by 2 orders of the magnitude on SurfScan S50200 on blanket and hydrophobic wafers. The same cleaning solution can be applied to copper-low k damascene patterned wafers to clean both copper and dielectric surface. Polished Black Diamond films have RMS roughness less than 2 angstroms and copper surface roughness about 5 angstroms with good surface finish. Process performance using the Cu-FGS process was used to highlight capability gaps in the process. Process enhancements were then integrated into the new process. Blanket and patterned wafer results are presented to demonstrate final capability. Future directions for process enhancement are identified.

2:15 PM M7.4 MECHANISMS OF POST-CMP CLEANING. Emannuel Estrang, Hong Liang, Dept of Mechanical Engineering, Univ of Alaska Fairbanks, Fairbanks, AK; Kristan Bukten, Dan McMillan, Rippey Corporation, El Dorado Hills, CA.

There has been a great interest in understanding post-CMP cleaning mechanisms. From the view point of CMP engineers, this means to know the relationship between applied load, relative surface speed, resulting friction, and effectiveness of particle removal. Inevitably, this is to maintaining the optimum water film thickness between a brush and the wafer/disk. This work simulates the cleaning conditions using a laboratory model system. Comparing with the classic lubrication concept as presented in a measured Striebeck curve, we have concluded that the cleaning process is bounded by elastohydrodynamic process that involves a constant contact between a brush and wafer/disk.

2:30 PM M7.5 A STUDY OF CMP MULTI HEAD CMP TOOL EFFECT ON BPSG FILM FOR ADVANCED DRAM APPLICATIONS. David A. Hansen, Gerry Moloney, Cybex Nano Technologies, San Jose, CA; David Whitus, Ebara Technologies, San Jose, CA.

With the maturity of CMP processes and consumables most of the major IC fabrication companies are now investigating CMP tool designs that will help without loss of process control with a corresponding reduction in CoO. In the past most of the retention was directed at multihead polishing tools as a means of attaining these goals. However most of the early multihead polishing tools produced severe Head-To-Head Thickness Variation (HTTV) and resulting Wafer-To-Wafer Thickness Variation (WTWTV). In fact some of the reported WTWV measurements were as high as 7%, which could be tolerated by some earlier products. However for all new advanced device products this high WTWV could not be tolerated and hence the drive toward multihead polishing tools faded. With new advanced CMP consumables and techniques it might be a good idea to revisit a multihead polishing tooling to see if the above issues may be addressed. In this work we have carried out a study of CMP multihead CMP tool and its effect on BPSG film for advanced DRAM applications by using the Cybex Nano Technologies IP-8000 Dry-In/Dry-Out multihead CMP tool. Once the process recipe was optimized on blanket BPSG wafers, 64 BPSG device wafers were run. Analysis of planarized wafers was carried out and the WTVTi (1σ) and HTTV (1σ) of 0.09% and 0.88%, respectively, were obtained. Furthermore the average measured WTWV and average post-step height was 2.43% and 45 Å, respectively. These results demonstrate the vast improvement that has been made by using advanced consumables and process techniques combined to early work using multihead CMP tools. In this paper we will detail how the use of the advanced consumable, i.e. tighter manufacturing specifications, and process techniques, i.e. novel pad dressing methods, have dramatically improved the viability of the multi-head CMP tool.