SYMPOSIUM M
Chemical-Mechanical Polishing Advances and Future Challenges
April 18 – 20, 2001

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SESSION MI - CMP: RECENT DEVELOPMENTS / PADS AND RELATED ISSUES

Chair: Suryendu DasBhabha and Akanei Daigumara Wednesday Morning, April 18, 2001
Golden Gate A1 (Morrill)

8:30 AM *MI1
RECENT ADVANCES IN CMP TECHNOLOGY. Malcolm Grief, Randy Harwood, Eric Woods, Sajay Banak, Padi Elkhob, Jim Schuetz, Mark Ferron, Dan Trojan and Sakti Chaddah, Speedfam-IPEC, Chandler, AZ.

Chemical Mechanical Planarization (CMP) has become an essential unit process for fabricating state-of-the-art devices. A CMP system is not used for dielectric applications. The purpose of dielectric CMP was to increase the process yield. However, the ring selectors cannot operate without exceeding the depth of focus budget. Dielectric CMP continues to evolve with With-in-Wafer Non-Uniformity (WINU) as the primary metric for improvement. Dielectric CMP was followed by WY applications for definition of plugs, contact and via. Primary motivation for W CMP was defect density reduction. Development efforts in W CMP are focused towards improving oxide erosion and plug reflow. Small Trench Isolation (STI) was adopted as a CMP application starting at the 0.35-0.25 micron technology nodes. STI reduced real estate usage while defining effective isolation of devices. Development efforts are primarily focused on direct STI and therefore in reducing overall variation (WINU, WIWNU, & WIWDU). Notably, etched copper interconnects. Copper CMP challenges are well known and primary drivers for development are oxide erosion, oxide loss, doping, and dielectrically. Finally, there are an increasing number of integration schemes for definition of High K gates requiring CMP on Interconnects. This paper will discuss advances in CMP technology that address key drivers of different CMP applications. These advances include better in-situ End point detection, superior carrier technology, and the combination of advantages of different forms (right phonon) with those of orbital platform (kinematics and through the pad shurry delivery). State of the art results from Speedfam-IPEC's new MomentumTM platform for copper, tungsten and oxide/STI will also be shown. There are three basic types of tools available in the marketplace: Rotary, Linear, and Orbital. This paper will discuss key differences and the ramifications on the total variation: With-in-Wafer Non-Uniformity (WIWNU) and With-in-De Non-Uniformity (WIWDU).

9:00 AM *MI2
A NOVEL OXIDE CMP FOR DAMASCE GATE FORMATION. Hyung-Won Kim, Sang-Kil Lee, Hyung-Kim Kim, Seung-Jung, Tae-Kyun Kim, Yeong-Joo Noh, Jee-Hong Kim, Jee-Hong Lee, Chul-Woo Nam, Samsung Electronics Co. Ltd., Icheon, KOREA.

A damascene or replacement gate process has been drawing an intensive interest due to its capability to avoid thermal or plasma damage occurred during conventional RIE process. This replacement gate process normally adopts poly-silicon dummy gate. Source/drain oxidation is performed self-aligned to the dummy gate, followed by replacing the dummy gates with W or Al metal gates. To replace dummy gates with metal gates, the top surface of the dummy gate needs to be exposed by removing the overlapping inter-level dielectric. CMP using conventional CMP process. Exposed dummy gates are removed by wet etching. In this study, ceria-based slurry was used for ILD CMP and compared with conventional ceria-based slurry. Since the ceria slurry shows high polishing selectivity of oxide to polysilicon as well as to nitride, poly-silicon dummy gates could be successfully acted as a stopping layer during ILD CMP process. As a result, process window could be significantly enlarged and final gate height could be maintained very uniformly compared with the case using conventional silicon base slurry. However, TEM examination showed that very thin layer was formed on top of poly-silicon dummy gate after polishing with ceria base slurry. It was found that this thin film made subsequent wet etching of dummy gate impossible. In order to avoid this issue, we developed a new process and possible mechanism on the formation of this blocking layers was proposed.

9:15 AM *MI3
WHAT ABRAISIVE FREE Cu SLURRY IS PROMISING? Yasuo Kikuma, Yasushi Kurita, Kazuyuki Maseha, JMS Amakura, Masako Yoshida, Hitachi Chemical Co., Ltd., Research & Development Center, Tokyo 157, JAPAN; Hitachi Chemical Co., Ltd., Electronic Devices Materials Operations Division, Tokyo JAPAN.

To reduce the number of micro-scrapes and the number of polishing particles in the fabrication of Copper interconnection circuits, we developed "Abrasive Free Polishing Slurry". By applying this newly developed slurry, we were able to achieve improved values of polishing and chemical properties in the CMP process. Using "Abrasive Free Slurry" in the damascene CMP process, excellent results of microstructure, surface flatness of the Cu film, and the topography and electrical characteristics obtained using this slurry will be discussed.

9:45 AM *MI4
ROTATIONAL AVERAGING OF MATERIAL REMOVAL DURING CMP. David R. Evans, SHARP Laboratories of America, Camarillo, CA; Michael T. Oliver, RedChip, Inc., Newark, DE.

At present, several different competing mechanical configurations are used in chemical mechanical polishing. These range from classical rotary designs to orbital and linear systems as well as the more recent wafer rotation designs. Invariably, wafer rotation is used in all of these systems to average out gross material removal rates. To the uninformed, this would perhaps seem to be so obvious that no further investigation is necessary. However, the interaction of polishing pad microstructure, as well as whatever abrasive pad and chemical solutions might be present in reality quite complex. In addition, fluid transport between wafer and pad surfaces is strongly affected by pad microstructure and relative motion of the two surfaces. In the present work it has been found that in the absence of rotational averaging correlated variations in material removal rate can be observed "downstream" from patterned features on the wafer surface. Furthermore, the correlation length is quite long and can be related to micro and macro-structural viscoelastic properties of the polishing pad material. Specifically, relaxation time for decoupling of pad anisotropies is a major determinant of the correlation length. It should be emphasized that this is an entirely separate issue from "planarization length" as commonly defined. Ako, in the absence of rotational averaging, very strong "leading edge effect" is often observed. This is characterized by very high material removal rates at the leading edge of the wafer. In contrast, at the trailing edge removal rates are very low and may even vanish altogether. In addition to the usual process variables (down force, slurry flow, etc.), this behavior is governed by the angle of attack of the wafer relative to the pad. Obviously, motion of the wafer during polishing converts any leading to trailing edge gradient in material removal rate to radial non-uniformity. In normal operation, this will be confounded with additional sources of radial non-uniformity due to surface finish, bulk pressure, etc. In the present work these effects can be separated and quantified.

10:45 AM *MI5
DE-PULVERIZING THE ORIGIN OF A CMP-ASSOCIATED "CENTER SPIKE" YIELD/RELIABILITY ISSUE. IS CMP TO BE BLAMED FOR IT'S APPEARANCE? Yehiel Geckin, David Wei, John Boyd and Rodney Kister, Lam Research Corporation, CMP/Clem Division, Fremont, CA.

A long-terming CMP related yield/reliability puzzle - thickness spike, frequently appearing at the wafer center after CMP operation, was studied. Optical film thickness measurements for pre- and post-CMP film were combined with surface topography profiling. Wafers' surface profile was also studied after the oxide film was HF-etched out. It was found that the post-CMP thickness spike is not caused by CMP masking however originated from a specific film type and occurs when the bare silicon wafer has a narrow dip-like defect in its center. The scenario of the "anti-spike" formation could be portrayed as: 1. Bare silicon wafer comes with a dip-like defect in its center. 2. Oxide deposition, having high step coverage properties, follows the profile of the bare silicon wafer and fills the dip. Optical thickness measurements tools, being insensitive to the height variations, are not capable to detect the dip. 3. CMP doing its planarization job and flattening the surface, creates a local thickness bulge, actually an "anti-spike" pattern filling the bare silicon dip in the wafer center. The higher is the CMP planarization efficiency and the narrower and deeper is the bare silicon dip, the more pronounced is the "anti-spike" pattern. An uniformity of the film thickness underlying topography copying film is transformed by CMP into a planarized flat-top film with negligible variations (thin silicon layers and thick elevated sections), which is exactly what planarization technique is supposed to produce. The center spike formation scenario explaining the appearance of the film thickness spike in the wafer center reveals the root cause of this phenomenon: high film dip-like defect located exactly in the wafer center, which most probably is originality to the specificity of the silicon crystal growth. This scenario also indicates that yield failures related to the center spike problem supposed to be associated with unetched plug holes and, as a result, electrical opens. It also explains why the photolithography operation also experiences problems in these cases and what is the nature of the problems. Surface flatness obviously causes so-called "Focus depth" problems in this case, which finally results in numerous electrical and functional failures. The thickness of the dip normally is about 4 mm in diameter, which may affect either 1 or 4 dies depending on wafer layout approach. The origin of the dip in
the bare silicon wafer center is under investigation. Up to this point it was found that the dip is not originated to the thermal shrinkage of the silicon in the wafer center. The centrosymmetric phenomenon could be considered as an example of extremely long-range CMP related integration interaction of a narrow dip-like microdefect at the bare silicon wafer surface and high planarization efficiency of the CMP process.

11:00 AM M1.6
EFFECTS OF MICRO-SCALE ABRASIVE SIZE ON THE CHEMICAL MECHANICAL POLISHING OF SiO₂. Chunhong Zhou, Lei Shan, Rob Hight, Steven Danyuk, the George W. Woodruff School of Mechanical Engineering, Georgia Institute of Technology, Atlanta, GA; S.H. Ng, Gnostic Institute of Manufacturing Technology, Singapore; Andrew J. Praszkowski, Chemical Products Corporation, Cartersville, GA.

This paper addresses the influence of the size of the abrasive in a slurry while polishing a thermally-grown silicon dioxide deposited on 100 mm diameter (100) p-type single crystal silicon wafers. The sizes of the abrasive particles (colloidal silica) were 10, 20, 80, 140, and 1.1 μm of 80/140 μm. The slurries contained 30% by weight abrasive particles stabilized with KOH. Experimental results demonstrate that the polishing rate and surface roughness are sensitive to the particle size and there exists an optimum abrasive particle size in terms of removal rate. A “nano-film” theory based on the pad roughness is used to explain the phenomenon. Keywords: Abrasives, Material Removal Rate; Chemical Mechanical Polishing; Surface Finish.

11:15 AM M1.7
POLYURETHANE PAD DEGRADATION AND WEAR DUE TO TUNGSTEN AND OXIDE CMP. Amy L. Moyer and Joseph Cecchi, University of New Mexico, Chemical and Nuclear Engineering Department, Albuquerque, NM; Dale Hetherington and David Stein, Sandia National Laboratories, Chemical Mechanical Polishing, Albuquerque, NM.

Chemical Mechanical Polishing (CMP) of both silicon dioxide and tungsten films utilizes Mode I (1410) polyurethane polishing pads and aluminas (tungsten) and silicon (oxide) slurries. The purpose of this research is to examine the structural, chemical, and mechanical property changes due to CMP of tungsten and oxide films. The physical and chemical properties of a polishing pad are not well understood. These property changes due to polishing will affect the removal rate, wafer uniformity, and pad life. The degradation of the pad has been examined using Electron Microprobe, Confocal, SEM, TEM, DMA, TM, XRD, FTIR, and Raman analyses. Tungsten and oxide polishing mechanisms are very different. Tungsten polishing is more a combination of chemical and mechanical abrasion, whereas, oxide polishing is more mechanical than chemical. Based on the FTIR spectra, the oxide polishing resulted in only one detectable structural change in the polyurethane hard segment. Tungsten polishing, however, resulted in various structural chemical changes as well as the displacement of various elements such as Cl, A1, and I in the pad. The properties of the last degree of the pad are dependent on the degree of the isocyanate hard and the polyol soft segment, which change due to CMP. The result of the reduction in the isocyanate hard segment and the formation of the carbonyl group may increase the pad hydrophilicity. The swelling of the polyurethane pad during polishing is due to the increase in absorption of water from the slurry into the pad. The presence of the slurry abrasive in the pad after polishing may affect the performance of the pad. A first layer or “first glass” formation occurs at a faster rate without conditioning for both oxide and tungsten polishing and affects polishing performance. Conditioning effectively roughens the surface of the polyurethane pad and increases the contact area between the pad, wafer, and slurry. Without conditioning, there are less pad areas for slurry transport and reduced roughness areas for effective abrasion.

11:30 AM M1.8

In spite of being a historically ancient technology, chemical mechanical polishing (CMP) has attracted tremendous attention recently because of its applicability in planarizing the dielectrics and metal films used in the silicon integrated circuit fabrication. Continued miniaturization of the device dimensions and the related need to forming number of devices on a chip has led to building multileveled interconnection on planarized layers. In CMP very thin materials (≤5 μm) has to be removed very precisely maintaining the precise control on the remaining thickness. Because CMP occurs at an atomic level at the polymer/interfacial layer, scratches and pores play a critical role in the successful implementation of this process. Surface roughness, elastic and viscoelastic properties, thickness, pore sizes play important role in this process. Unfortunately mechanical properties of polyurethane polishing pads used in CMP are poorly understood. In this study we have studied the mechanical properties and surface morphology of CMP pads using the size-of-the-art nano-indentation technique along with tapping mode atomic force microscopy. Elastic, viscoelastic, modulus and hardness, and surface roughness have been evaluated. Tribological properties of the pad has been evaluated using Universal Micro-Tribometer. Direct correlation between pad properties and polish performance is not yet determined to correlate the properties and performance of the pads.

11:45 AM M1.9
A TECHNIQUE FOR ENGINEERING THE PLANNERIZATION PROPERTIES OF A CMP POLISHING PAD. Peter Rentel, Linn Research Corp., Fremont CA; Brian Lombardo, Madison CMP, Wilmington, DE.

In CMP, long-range planarization - planarization occurring over a lateral distance of greater than, say, 400 microns - is controlled primarily by the mechanical properties of the polishing pad, i.e. thickness and stiffness. One measurement of long range planarization can be made by polishing structures of graded lateral dimension and fixed step height. When the wafer is polished, the remaining normalized step height can be plotted as a function of feature size. Doing so results in a sigmoidal shaped curve transitioning from zero [perfect planarization] to unity [zero planarization]. We describe the planarization length “L” as the distance at which the curve crosses 0.5. For a prediction of the standard deviation of the planarization which is the derivative of the sigmoid. While longer planarization length is generally desirable and easily achievable, a large “L” often results in too much planarization, where the ultimate planarity of the silicon surface is challenged, and an undesirable effect of “scripto cheese” occurs as the polish planarizes the silicon substrate itself. Decreasing L can eliminate this effect, but only at the expense of long range planarization, a desirable output. The challenge, therefore, is to engineer a polishing pad with a large “L” but a very short S. This can be achieved by cutting grooves into the surface of the polishing pads, effectively decoupling L from S. By cutting the grooves in such a way as to create islands on the pad surface, these features serve to create a planarization length on the order of the line thickness of the island size, i.e. causing S to be very small. By changing the size of the islands, L and S can be engineered to achieve optimal planarization for the given structure to be planarized and quality of silicon substrate available. Planarization results are presented to show the effect of actively engineered planarization pads, and how the groove pattern can be optimized for a given planarization requirement and substrate quality. The results are followed by a discussion of the expected vs. the achieved results.

SESSION M2: CMP ABRASIVES I / CMP ABRASIVES II
Chair: Kenneth C. Cotton and Rajeev Bajaj
Wednesday Afternoon, April 18, 2001
Golden Gate A1 (Marriott)

1:30 PM M2.1
PREPARATION AND EVALUATION OF CHEMICALLY MODIFIED ABRASIVES FOR CMP. R. Parrish, N. Barney, B.Y. Wang, K. Grifiths and A. Babel, Clarkson University, Dept. of Chemistry, Center for Advanced Materials Processing, Potsdam, NY.

Abrasive particle size, shape and composition in CMP slurries are known to be among several variables that control polishing rate and generation of defects during wafer planarization. In order to meet next generation standards, particle sizes are being reduced and composition used to control abrasive hardness and provide selectivity in polishing different wafer surfaces. In recent years advances have been made in technologies for surface functionalization of many types of particulate matter. This expertise is now being applied to the preparation of powders for use in CMP. Presented in this paper will be methods developed by the authors to selectively improve for use in CMP slurries the surface of several micro and nano sized metal oxide particles. The treatments include coating individual cores with a continuous shell of inorganic or organic material; or, coating attachment of chemical functionalities on the core surfaces capable of imparting chemistry at the particle/surface interface, the wafer. Preliminary polishing data using the described treated abrasives will be discussed.

2:00 PM M2.2
AN EVALUATION ON THE EFFECTS OF NEWLY DESIGNED ABRASIVES IN CMP SLURRY. Nobuko Kawashima and Masayuki Hattori, JSR Corporation, Fine Electronic Research Laboratory, Yokohama, JAPAN.
Recently designed abrasives with various particle morphology and components have been prepared and evaluated in terms of CMP polish efficiency. Polymer spheres with uniform particle size and special functional groups were prepared by soap-free emulsion polymerization. CMP slurries with these polymer abrasives indicated decreased wafer dishing, erosion, and defect formation for metal and dielectric surfaces. This study has also been conducted with a preparation of composite particles consisting of a polymer core covered with inorganic composition such as silicon nitride, titanium compound, silicon carbide, and AlOx. Controlled hydrolysis and hetero-coagulation systems were prepared as preparation methods of composite particles. The thickness, morphology, and state of the deposited layer could be altered by adjusting concentrations of the reactant and nucleus of metal compounds, pH of the aqueous solution, aging temperature, silica coupling agents, etc. These composite particles were particularly useful in preventing scratching of low-k dielectric material surfaces during a CMP process.

2:30 PM M.3.3
CMP OF COPPER. EVOLUTION OF A SLURRY. Wieland Prey, Jian Wang, and E. B. Davis, Intermetal Dynamics, Inc., Bethel, CT.

The presentation describes the evolution of a slurry for copper CMP that has been developed over the years. It includes lessons learned and the many advances that have been made. The slurry composition and processes are highlighted to demonstrate the changes in technology.

2:45 PM M.3.4
HIGH PERFORMANCE CMP SLURRY WITH INORGANIC/RESIN ABRASIVE FOR Al/Low-k DAMASCENE. H. Awaya, Y. Yokozawa, M. Minamihama, Toshiba Corporation, Semiconductor Company, Yokohama, JAPAN; N. Kumaishi, M. Horiuchi, JSR Corporation, Fine Electronic Research Laboratories, Yokohama, JAPAN.

Damascene is an attractive wiring method for process simplification and yield enhancement. But CMP still has many issues like scratch, planarity, and corrosion. Meanwhile low dielectric constant (low-k) material is going to be introduced as the interlayer dielectrics (ILD) to improve device performance. However, the mechanical strength of low-k material increases concerns like scratch and planarity. So, a new concept is introduced to the CMP slurry abrasive. The new abrasive is composed of resin particle coated with inorganic particles. The strength characteristics of Resin/Resin and Resin/Inorganic mainly come from the elasticity of the resin. The soft resin particle behaves as a cushion and prevents the scratch caused by agglomerated inorganic particles and foreign material. The spring feature of the resin particle is used to selectively polish metal portions and concave portions. Furthermore, the pressure is loaded to the Al film surface effectively through the resin particle and higher CMP rate can be achieved even without chemicals like oxidizers. This chemical-free polishing would be the advantage in preventing the corrosion of Al.

In this paper, the polishing mechanism of Inorganic/Resin abrasive and the results of Al/Low-k Damascene will be presented.

3:30 PM M.3.5
OXIDE POWDERS FOR CMP PRODUCED BY CHEMICAL VAPOR SYNTHESIS. Hermann Sieg, Markus Winterer, Horst Hake, and Helmut Hahn, Darmstadt University of Technology, Materials Science Department, Thin Films Division, Darmstadt, GERMANY.

Ultra-fine, non-agglomerated oxide powders are produced by chemical vapor synthesis (CVS). In the CVS process volatile metalorganic precursors are decomposed in a hot wall reactor with a well defined reaction zone at reduced pressures forming nano-sized powders with a narrow size distribution. An inherent advantage is the modular design of the gas phase which enables the production of well defined, doped and coated silicon powders with improved volume and surface properties, e.g. dielectric constant, silica potential, hardness, chemical reactivity or dispersability. In order to correlate CVS product characteristics with CMP performance, powders are investigated by nitrogen adsorption, TEM, XRD, aqueous dispersions by zeta potential and size measurements and polished surfaces by HRSEM and AFM.

3:45 PM M.3.6
SLICA ABRASIVES IN POLISHING APPLICATIONS. S.D. Helfring, C.P. McNamara, PPG Industries, Inc., Pittsburgh, PA; S.Y. Bahadur, Nanyang University, Department of Chemical Engineering and Center for Advanced Material Processing, Potsdam, NY.

Slurries containing silica abrasive produced by varying processes are compared for polishing performance. The relationship between the physical and chemical characteristics of silica and polishing performance with copper, tantalum, and oxide were examined. The effects of morphological parameters and surface chemistry on removal rates, selectivity, stability, and post-polishing cleaning will be discussed.

4:00 PM M.3.7
SYNTHESIS OF ALUMINA SLURRIES FOR DAMASCENING COPPER. Byung-Chin Lee, David J. Duquette, Ronald J. Gittman, Remsensie University, Remsensie Polytechnic Institute, Center for Integrated Electronics and Electronics Manufacturing, Troy, NY.

Model alumina slurries have been synthesized using fundamental electrochemical concepts and surfactant additives, along with characterization of blanket copper wafers after chemical-mechanical planarization (CMP) processing. A model slurry was established containing 3 wt% alumina (50 nm nominal size), 2 wt% potassium dichromate and 1 vol% DowFA 2000, as abrasive, oxidizer and amionic surfactant, respectively, which resulted in copper removal rates of 120 μm/min with smooth, low-contrast, dielectric surfaces without aggressive post-CMP cleaning. When used with a model silica abrasive to remove the Ta liner, well-defined damascene-patterned structures were achieved with low-particle defect densities. The principal techniques used in developing the model alumina slurry include the following: open circuit potential measurement, potentiodynamic polarization, capillary hydrodynamic fractionation (CHDF) particle size analysis, surface tension measurement, and zeta-potential measurement. The paper includes variations obtained with alternative alumina abrasives, alternative oxidizers and alternative surfactants to illustrate the synthesizing principles. The use of this approach in developing a slurry for the Ta liner will also be described.

4:30 PM M.3.8
THE EFFECTS OF ADDITIVES IN IODINE-BASED SLURRY ON COPPER CHEMICAL MECHANICAL POLISHING. Seung-Min Lee, Zhen Chen, and Rajiv K. Singh, Department of Materials and Engineering Research Center for Particle Science and Technology, University of Florida, Gainesville, FL.

Copper CMP has now been recognized and accepted as the process that is capable of providing the planarity to build multilevel interconnects schemes with below-quarter-micron lines. One of the key issues in copper CMP is the development of slurries which can provide high removal rates, good planarity and high selectivity. In our previous presentation, the possibility of the use of iodine slurry for copper CMP was introduced. Iodine slurry showed the highest removal rate and relatively good selectivity. In this presentation, we have investigated the effects of additives in iodine slurry in order to control the removal rate of copper and surface quality. Since BT and TiN film can be well and surfactant added rate and surfactant, respectively, both additives can be used to retard the surface reaction rate and dissolution rate of copper and to enhance the surface quality. From the results, it is observed that Cu-BTA film is formed uniformly on the surface, which protect the further corrosion of copper. In addition, surfactants were very effective to control the removal rate and surface quality. Then, for better understanding of the high removal rate of copper in iodine based slurry, friction force measurements and nano-scratch tests in solutions were conducted. These results were compared to hydrogen peroxide based slurry.

4:45 PM M.3.9
SELF-ASSEMBLED SURFACTANT MEDIATED DISPERSION OF NANOPARTICULATE SYSTEMS FOR CHEMICAL MECHANICAL POLISHING (CMP). Pankaj K. Singh, Joshua J. Adler, Bahar Basim, Yakov I. Rubinsonovich, and Brij M. Moudgil, Department of Materials Science and Engineering and Engineering Research Center for Particle Science and Technology, University of Florida, Gainesville, FL.

The current interest in using different types of ultrafine (nanosized) particles for chemical mechanical polishing (CMP) under severe conditions such as high speed, chemical additives and high pressure, puts a high demand on suspension processing. Traditional dispersing methods such as ultrasonic and polymeric dispersants may not perform adequately under the conditions encountered in CMP. Surfactant solutions can provide a feasible alternative for stabilization
of ultralight particles. The barrier to aggregation in presence of surfactants was measured using atomic force microscopy and the barrier height and sintered to sinter the barrier. It was found that the barrier was several orders of magnitude higher in presence of micelle-like self-assembled surfactant aggregates, as compared to barrier expected from electrostatic interactions. The results indicate the presence of a surface barrier due to the adsorbed micelle on the surface, the strength of the barrier increasing with increasing strength or compactness of the adsorbed micelle. The origin of these forces was explored through techniques such as adsorption, contact angle, zeta potential and surface tension measurements. 

Fourier-Transform Infra-Red Spectroscopy (ATR-FTIR). In previous studies, unstable slurries were observed to form significant surface deformation during silica CMP. Polishing was carried out using a silica surfactant or a blended silica surfactant on the wafer surface quality while maintaining a reasonable material removal rate. The effect of particle size and polishing pressure was also examined.

**SESSION M3: COPPER CMP / STI AND PLANARIZATION I**
Chair: James G. Byrne, Ronald J. Gutman Thursday Morning, April 19, 2011
Golden Gate A1 (Marriott)

8:30 AM M3.2 INTERPLAY BETWEEN COPPER ELECTROPLATING AND CHEMICAL MECHANICAL PLANARIZATION. Akiko Hongo, Yasuake Chikamori, Tatsuya Kohama, Koji Mishima, Norio Kimura, Elbara Corporation, Fushawara, JAPAN; Daniel K. Watte, Elbara Technologies, Inc., San Jose, CA.

The introduction of Chemical Mechanical Polishing (CMP) into semiconductor device processing brought a significant need for wet chemistry research and development in this industry. With the transition from aluminum to copper for advanced interconnect metallization came tremendous amount of electrochemical research towards developing a production worthy copper CMP process capable of meeting the stringent specifications of dual damascene integration. In addition, the dual damascene integration scheme introduced copper deposition challenges that brought significant activity in developing another wet chemistry process, electroplating. These two sequential, chemical processes have been shown to have significant interaction that has created significant challenges in process integration. We present here some of the copper electroplating and copper CMP results from development efforts at Elbara that highlight the process integration challenges between these two processes. For example, a non-uniform copper depositing pattern observed during copper CMP can be compensated for in the CMP process but may be indicative of non-uniform deposition, or demonstrate the need for a post deposition anneal that gives a more uniform distribution of copper microstructure across the wafer. Compositional changes to copper electroplating bath chemistry can achieve high aspect ratio, 'bottom-up' trench fill, but can present local, pattern dependent, challenges for CMP. Critical issues between these two processes, such as global uniformity, local morphology variation, post-CMP voids or pits, or transient changes in copper structural and compositional properties, will be presented and discussed.

9:00 AM M3.3 EFFECT OF COPPER FILM SURFACE PROPERTIES ON CMP REMOVAL RATE. Yuchun Wang, Rajeev Bajaj, Gary Lee, Yeazi Dando, Doyle Bennett, Prateek Banerjee, Applied Materials, CMP Division, KU, Santa Clara, CA.

It has been observed that CMP (chemical mechanical polishing) removal rate of copper varies for films from different sources. While the film hardness and their wet static etch rate in absence of inhibitor are similar, the static etch rate in presence of inhibitor are significantly different. Analysis by AFM, XPS, and ion beam sputtering showed the film roughness and surface composition are different within the range of 160 angstroms deep. The different CMP removal rates are synergistic effect of copper film roughness (grain size), surface composition, and effective adsorption of inhibitor. Once polishing is initiated by an aggressive polishing step, removal rate of the remaining copper films becomes less different. Based on these findings, the polishing shurry and process were further optimized.


Copper Dual Damascene (Cu 2D) technology becomes the process of choice in semiconductor manufacturing. The Cu 2D sequence includes multiple use of CMP both for dielectric planarization and for shaping planarized wires. The Copper CMP ability to remove copper burden materials leaving the wafer surface as flat as possible. The planarization task in Cu-CMP is more challenging than in other CMP processes due to the CuCLU layer, which has a higher toughness than other dielectric layers, and while polishing heterogeneous surface during barrier removal. Electrophoretic additives adsorbed at the grain surface affect the intergranular bonding forces, layer properties and CMP response, causing considerable pattern sensibility. Typical CMP process is multi-step/multi- consumable. High planarization efficiency and absence of the intergran boundary damage is a critical requirement and it is directly linked to the CuCLU interaction mechanism. Fast formation of passivating surface films prevents Cu from direct chemical dissolution, converting a chemically driven process into a pseudo-mechanical one with high planarization capability and self-inhibiting action, minimizing the intergran boundary damage. Normally, H2O2 added to Cu-CMP slurries. The H2O2 concentration determines the mechanical and chemical properties of surface oxide species and as result the all aspects of the CMP process. In this study the effect of H2O2 concentration on Cu removal rate and the type of surface films formed were investigated and Cu removal mechanisms discussed. It was found that Cu removal rate is extremely low in the absence of H2O2, it increases up to ~40nm/min. Then the rate quickly drops and then decreases again. The values of open circuit potential plotted in the Ei-pH diagram clearly show that the surface Cu2O is formed at lower H2O2 concentration and CuO at higher ones. The formation of different Co-oxides was confirmed by XPS analyses.

9:45 AM M3.5 ANALYSIS OF COPPER TO TANTALUM TRANSITION IN COPPER CMP. J.M. Kang, Shuyou Wu, T. Selvaj, and P.D. Foo, Institute of Microelectronics, DSC-MD Department, SINGAPORE.

The evolution from Cu to Ta surface during Cu CMP has been investigated. As a first step of Cu CMP, removing excess Cu on field area to Ta often gives rise to topography issues such as dishing or erosion. The exposure of Ta is detected by in-situ reflectance measurement, where the downward slope start signifies the start of Ta exposure. For blanket wafers, the minimum remaining Cu thickness at slope-start increases with initial Cu thickness. Applying lower polishing pressure and table speed, so-called soft landing, near the Cu-Ta transition stage results in thicker remaining Cu. In patterned wafers, Ta exposure starts near high pattern density areas such as wide lines. In this case, contrary to blanket wafers, remaining Cu thickness at slope-start cannot be correlated simply with initial Cu thickness. In this experiment, with increasing initial Cu thickness, remaining Cu thickness at slope-start decreased. The amount of dishing is largely proportional to the initial Cu thickness. Applying soft landing results in thicker remaining Cu than polishing without soft landing in blanket wafers. However, polishing without soft landing results in more dishing. Total-incident range (maximum remaining Cu thickness
CMP USING MESA™, Thomas Launzen, Inki Kim, Jim Schueter, SpeedFam-IPEC Incorporated, Chandler, AZ; Scott Rannels, Scott Rannels Consulting, San Antonio, TX.

MESA is a feature-scale planarization model developed by SpeedFam-IPEC (SPI), in conjunction with Southwest Research Institute, for describing the chemical mechanical polishing (CMP) process used in IC manufacturing. This model has previously been applied to the polish of inter-level dielectrics and copper CMP. The present study is part of an experimental validation for shallow trench isolation (STI). The study was carried out using silicon substrates with a single 1C (1000/1400) pad and a test section designed to determine the dependence of planarization length on CMP consumables such as slurry and pad, and on process settings such as down force and relative speed [1]. S. Hymes et al., CMP Symposium, MEMS Spring Meeting, April 1999.

2:15 PM M4.5
A MECHANICAL WEAR MODEL FOR CHEMICAL-MECHANICAL POLISHING PROCESS, Dobran Abbasi, Aliena Manzari and Xu Xin, Department of Mechanical and Aeronautical Engineering, Clarkson University, Potsdam, NY.

Abrasive particle-surfacer interactions are studied and the surface removal process by adhesive and abrasive wear mechanisms during chemical-mechanical polishing (CMP) are analyzed. The mechanical contact theory is used and a model for interactions of pad asperities with abrasive particles and wafer is developed. Tests were carried out on 8 inch wafers using different pads and slurry and the results show that the abrasive particle adhesion affects the CMP process. The effect of non-sphericity of slurry particles on the CMP performance was also studied.

3:30 PM M4.6
A CONTACT-MECHANICS BASED MODEL FOR DRESSING AND ELIMINATION IN CHEMICAL-MECHANICAL POLISHING, Joost J. Vlasak, Harvard University, Division of Engineering and Applied Sciences, Cambridge, MA.

In this presentation, we describe a new model for dressing and elimination during chemical-mechanical polishing. According to the model, dressing and elimination is controlled by the local pressure distribution between features on the wafer and the polishing pad. The model uses a contact mechanics analysis based on the work by Greenwood to evaluate this pressure distribution and it allows us to take the compliance of the pad as well as its roughness into account. Using the model, it is straightforward to evaluate the effect of pad density, line width, applied down force, selectivity, pad properties etc. on both dressing and elimination. The model can be applied to CMP used for oxide planarization, metal damascene or shallow trench isolation. The model is implemented as an algorithm that quickly calculates the evolution of the profile of the wafer surface during the polishing process. With proper calibration of the selectivities, it can be used as a tool in optimizing the CMP process and implementing CMP design rules.

3:45 PM M4.7

Chemical mechanical polishing is an essential process for achieving a high degree of planarization. The planarization after CMP sensitively depends on the pattern scales, the pattern densities, the mechanical properties of polishing pads and the polishing process. In order to simulate the topography after CMP, a numerical model with the pad surface soft layer had been proposed. The model should be very useful not only for the topography simulation, but also for the development and the evaluation of new processes, i.e. new dressers, new polishing pads. Based on the good agreement between the numerical model and the physical model, its applications for CMP and metal CMP will be presented in this paper. Application for the slurry based slurry process, which has a non-linear dependence of the polishing rate and a self-stopping property, and application for the metal CMP with high selectivity will be discussed.
In a previous CMP model, the effects of both chemical and abrasive slurry concentration on the polishing rate were qualitatively explained, for constant polishing pressure and velocity. This model is extended here to consider specific descriptions of mechanical abrasion, including Preston and non-Preston expressions. Predictions of behavior are compared to literature data in an attempt to give an improved understanding of the abrasive process in CMP.

4:30 P.M. M4.9 WAFER NANOPOGRAPHY EFFECTS ON CMP: EXPERIMENTAL VALIDATION OF MODELING METHODS
Brian Lee, Duane Boving, Massachusetts Institute of Technology, Dept of Electrical Engineering, Cambridge, MA; Winthrop Bajles, BayTech Group, MA; Noel Pallas, the Hester, ADE Corporation, Woodstock, MA; John Valley, Chris Kolopicus, ADE Phase Shift, Tucson, AZ; Dale Hetherington, Sandia National Laboratories, Albuquerque, NM; Hong-Jung Sun, Philips Semiconductor, Albuquerque, NM; Michael Lacy, Lam Research, Fremont, CA.

Nanochemistry refers to 10-1000nm surface height variations that exist on a lateral millimeter length scale on unpatterned silicon wafers. Chemical mechanical polishing (CMP) of deposited or grown films (e.g., oxide or nitride) on such wafers can generate undesirable film thickness variations that can result from different levels of polishing pressure. Proper simulation of the effect of nanotopography on the CMP film thickness is needed in help the understanding of process control and in the development of improved CMP models. Our group has developed unique modeling approaches that seek to capture the thickness of the CMP film thickness variation that results from nanotopography. This paper describes these measurements and analyzes the results to determine the impact of nanotopography on the CMP process.

Wayned P. M4.10 SLURRY DETECTION AND TRANSPORT DURING CHEMICAL MECHANICAL POLISHING OF COPPER. Ying Li, Sarah Nenney, S.V. Bubu, Dept of Mechanical and Chemical Engineering, Center For Advanced Materials Processing, Clarkson University, Potsdam, NY.

Although significant progress has been made in slurry development and process optimization, one important issue, i.e., the slurry transport between the wafer and the pad during polishing, still needs in-depth investigation. The slurry transport not only affects directly the chemical reactivity of the slurry by influencing the steady state concentration of the various chemicals and abrasives between the pad and the wafer, but also the efficiency of mechanical abrasion of the particles. This work investigates the retention and transport of chemical species and abrasive particles during copper CMP. "Slurry step-flow" experiments, in which the concentration of the chemicals and abrasives in the slurry are altered in a step change during polishing, are conducted with slurries containing different chemicals, such as ferric nitrate, hydrogen peroxide and potassium iodide. Results from these experiments that shed light on the role of abrasives and chemicals during the polishing will be presented.

SESSION M5 POSTER SESSION
Thursday, April 19, 2010 8:00 A.M.
Salon 1/L (Merriott)

M5.1 IN SITU LATERAL FORCE MEASUREMENT DURING CHEMICAL MECHANICAL POLISHING. Wonseop Choi, Seung-Min Lee, Rajiv K. Singh. Department of MSE and Engineering Research Center for Particle Science and Technology, University of Florida, Gainesville, FL.

A variety of in situ measurement techniques were developed in metal and silicon CMP. However, no in situ techniques have been developed to monitor mechanical effects in CMP environment under solid loading conditions and the need to understand the fundamental aspects of the process is also important. In our previous work, the frictional force of stationary wafer without solid loading has been studied. In this talk, frictional forces under real CMP conditions with solid loading and rotational wafer have been investigated. An in situ lateral force measurement apparatus was modified to be suitable for real CMP condition. This technique measures frictional forces between the surface of the wafer sample and the polishing pad under different solid loading conditions. Experiments were done in polishing of silicon wafer using silica slurry and polishing of copper wafers using alumina slurries. The frictional force measurements, which were a function of time and process parameters, were correlated with the change in surface characteristics of the polished wafers. Atomic Force Microscopy (AFM), Ellipsometry, and Four-point probe were used to characterize the samples before and after the experiments. The results showed the better understanding of the frictional force mechanism occurring at the wafer-pad interface under different solid loading conditions during CMP.

M5.2 CMP RELATED AND CMP REVEALED SHORT- AND LONG-RANGE INTEGRATION INTERACTIONS IN COPPER DUAL DAMASCENE TECHNOLOGY. Yehiel Goldis and Rodney Kistler Lam Research Corporation, CMP/CLEN Technology Division, Fremont, CA.

More than 3 years passed since IBM made their official announcement on Copper Dual Damascene (Cu2D) technology, drawing the semiconductor world in the Cu2D rush. Nowadays, after more than 3 years of extensive R&D work, the FDL yields are still too low, and a lot of process integration work still has to be done to make it fab ready. At this phase the key to success is to link the problem to its root cause, which is frequently located at remote operation and it takes more effort to discover the link than to fix the problem. CMP is one of the most, if not the most, critical yield affecting operation in Cu2D technology. Going through all metal deposits and touching the dielectric, CMP is performing a kind of reversed processing. In this sense it could be considered also as a quality control procedure, capable to reveal problems related to other process steps. Additionally to the known Cu oxide losses and formal particle defectivity, other CMP-related or CMP-revealed yield affecting issues are discussed in details: scratching, micro-cracking, corrosion; non-removed residuals; voids and pits; barrier integrity damage; oxide depressions/dislocations. Cu is a very soft material. In addition to scratching agglomerates and tool debris, two new classes of scratches, i.e., nc-Cu treated flakes and "rolling stones", leading in some cases to extremely repeatable regularly shaped effects, and so-called "chemical" scratches, are discussed. Copper is a polycrystalline material, that is a new challenge for CMP, and micro cracking at the intergran boundaries is discussed particularly in details. Rough estimation of the number of intergran separations in a chip per Cu level leads to a number as high as about one billion. Intergran boundaries are extremely mechanically and chemically vulnerable. Shutter forces and chemically aggressive CMP media, resulting in chemistry-assisted inter-grain cracking and stress-induced intergran corrosion. Inevitably exposed of processed layers to corrosive conditions is inherent part of the CMP game. There are some specific spots of the Cu layer (pin-holes, micro-cracks, true- and pseudo-scratchers, intergran boundaries, hidden stressed spots, voids, gullwingly active spots etc.), demonstrating enhanced vulnerability to corrosion. What should be done to prevent corrosion damage in such conditions? In summary it is concluded that extensive work still has to be done to tune design rules, deposition, annealing and CMP to make the whole Cu2D back-end cluster self-consistent.

M5.3 A PLANARIZATION MODEL IN CHEMICAL MECHANICAL POLISHING OF SILICON OXIDE USING HIGH SELECTIVE CoO2 SLURRY. Jong-Won Lee, Bo-Us Yoon, SangRok Hah and Jou-Hee Min. SEMI Technology RD Center, Samsung Electronics Co. Ltd., Kyungki-Do, KOREA.

As the design rule of IC device decreases high selective chemical mechanical polishing process for shallow trench isolation is becoming more important. One of the most promising slurry for high selective CMP is ceria based slurry. However, in the high selective CMP environment, which is expected to increase in future, the removal rate decreases by the recession area. In this study, mechanism of planarization for the CMP of silicon oxide
using high selective ceria slurries was explored. A comparison study on silica, ceria, and high selective ceria CMP processes was carried out. As the onset of polishing with silica slurries, the removal rate of ceria active areas are higher than the bulk removal rate. As the surface of oxide becomes planarized, removal rate exponentially decrease and converges to the bulk removal rate. However, in the high selective CMP case, the removal rate of silicon oxide in high area is constant and does not depend on the polishing time. This implies that the oxide polishing rate does not increase on the raised areas for high selective CMP. Polishing behaviors as a function of the solid content of ceria and ceria slurries and high selective ceria were investigated. Although the removal rate increases with increase in solid content, the removal rate of ceria active areas was not observed. Therefore, it is proposed that the ceria abrasive which is coated by chemical additive passivates the oxide of recessed area that reduces the removal rate. On the basis of the result, it is known that the removal rate in the oxide of etched areas is not caused by solid content but caused by chemical additive.

M5.4 LAYOUT PATTERN DENSITY AND OXIDE DEPOSITION PROFILES EFFECTS ON DIELECTRICS CHEMICAL MECHANICAL POLISHING: Young-Bae Park, J.Y. Yoon, J.Y. Kim, W.G. Lee, Hyundai Electronics Industries Co., Ltd., SYSTEMIC R&D Center, Cheongju, KOREA

Based on experimentally obtained intersection distance, test masks for characterizing and modeling pattern dependent variation of the remaining thickness after chemical mechanical polishing (CMP) are designed. Using these masks, we characterize polishing behavior with layout pattern density and pitch variation. Also deposition profile effects are compared between PETEOS (Plasma Enhanced Tetraethyl Orthosilicate) and HDP (High Density Plasma) oxide in STI (Shallow Trench Isolation) CMP. Both remained silicon nitride thickness and expected oxide pattern density considering deposition profile effects show good correlation with respect to pitch variation for a constant layout pattern density. The reason that the remaining silicon nitride thickness and the true layout pattern density are deduced. Also, the remaining thickness increases nearly linearly with the pattern density of a constant layout pitch, which can be explained from the simple pattern density model.

M5.5 A CMP NUMERICAL MODEL COMBINING DIE SCALE AND FEATURE SCALE POLISHING CHARACTERISTICS: Stephanie Delage, Frank Meyer, Goetz Springer, Infineon Technologies, Munich, GERMANY

Chemical Mechanical Polishing (CMP) has emerged as the leading process for global and local planarization in silicon integrated circuits fabrication. However, there remains a large number of variation and effects due to layout pattern, equipment, and process dependencies that are still poorly understood. An improved characterization and modeling methodology is needed to facilitate the assessment and reduction of such variations. Several works have proposed models for Chemical Mechanical Polishing to provide various benefits. But most of them relate to a single process description (wafer/die/feature) and a lack of multiscale models remains. In this paper, a new numerical model combining die scale and feature scale polishing phenomena for oxide or ceria CMP is proposed. This work is based on the analytical effective density model proposed by D.Bening et al. [1], that takes into account a die scale pad deformation. We expand this model to include the description of the removal at the feature scale. A topography discretization allows us to describe the polishing in down areas more accurately, depending on the down area width. The physical parameters considered include the deformation of the polishing pad (die scale and feature scale), the removal rate of a blank, the removal rate of the same layout conditions, and the removal rate in down areas for small polishing times. Comparison of simulated results with MIT test wafers experiments is performed and evaluated. [1] D.Bening et al. “Pattern dependent modeling for CMP optimization”, Proc. ITRS Symposium P: Chemical Mechanical Polishing, San Francisco, CA, Apr. 1999.

M5.6 FUSING BLANKET TO PATTERNED WAFER PERFORMANCE IN COPPER CMP: S. Hymes, D. Trambak, S. Chang, I. Butcher, B. Bayer, S. Storch, Ashland Specialty Chemicals, Dublin, OH.

A basic connection between blanket and patterned wafer performance is presented using a single fundamental assumption on the role of step height. Using idealized rate responses to downforce, the blanket wafer response of idealized slurries (both Prestonian and non-Prestonian) is used to develop expressions for planarization efficiency and polishing susceptibility of patterned films directly applicable to traditional and Dimencene CMP. Results for real Cu CMP slurries are then compared to the model in order to demonstrate the link between composition, blanket and patterned wafer performance.

M5.7 CHARACTERIZATION OF A NEW CLEANING METHOD USING ELECTROLYTIC IONTIZED WATER FOR POLY Si CMP PROCESS: Naoto Miyahiti, Meiji Univ., Dept. of Electrical and Electronic Engineering, Kawasaki, JAPAN; Tohoku Co., Semiconductor Company, Yokohama, JAPAN; Shin-Iehiro Oekawa, Meiji Univ., Dept. of Electrical and Electronic Engineering, Kawasaki, JAPAN; Masaki Kedema, Yoshitaka Matsu, Tohoku Co., Semiconductor Company, Yokohama, JAPAN; Satoko Betu, Takeshi Nishikawa, Mechanical Systems Laboratory, Tohoku University, Sendai, KAWA, JAPAN.

Recently, trench isolation technology has been developed and applied to bipolar LSI production, especially, poly-Si Chemical-Mechanical-Polishing (CMP) technique has made much improvement on deep trench isolation. Major issues of the process integration for that purpose have been the post-CMP cleaning process. In general, the wafer surface after a conventional CMP process is contaminated with silicon particles and chemical impurities. These contaminations produce some unexpected patterns and crystal defects in the wafer surface layer after oxidation. It is difficult to remove them by the conventional cleaning techniques. Therefore, we have established the new post-CMP cleaning method using the electrolytic ionized water containing chemical additive of a small quantity. The anode water has the cleaning effect for the metal and organic contamination, and the cathode water has the removing effect for the particles and the existing surface defects. For the new cleaning process, it is important to avoid the mechanical damages on the surface and control the surface roughness. Our experimental work has been focused on the numbers of the remaining particles, the contamination concentration and the surface roughness using AFM. VPD1+CP/MS. We herein report the properties of the electrolyzed water and the examined results of poly-Si surface after CMP process. It was found that the electrolyzed water is effective for surface control, and the new cleaning process is useful for CMP process.

M5.8 ENGINEERED POROUS AND COATED SILICA PARTICULATES FOR CMP APPLICATIONS: K.S. Choi, R. Voraay, J. Grey, N. Bnsam and R.K. Singh Department of Materials Science and Engineering and Engineering Research Center for Particle Science and Technology, University of Florida, Gainesville, FL.

The aim of this study has been to synthesize the micro porous silicon spheres and to coat insynthesized SiO2 with CeO2 for CMP applications. First, spherical micro porous silicon powders with a narrow size distribution have been prepared by a precipitation technique involving the hydrolysis reaction of a silicon alkoxide in ethanol. The interparticle microporosity has been created by adsorption of an organic compound (glycerol). The presence of glycerol during the synthesis affect considerably the precipitation mechanism and its effect on the particle size will be discussed. The synthesis of silica micro porous spheres of narrow size distribution yielded the preparation, by varying particle size and porosity, of a wide range of aqueous silica slurries. The influence of particle size, particle size distribution, porosity and particle concentration will be discussed in chemical mechanical polishing applications. Although silica particles show large plastic deformation than the bulk material, very good glass polishing rate are obtained due to the plastic deformation of the silica layer during CMP. Silicon particles are suitable candidates for application in CMP because silicon can be directly precipitated on monodispersed spheres, their narrow size distribution being an important requirement in CMP applications. Secondly, insynthesized silica particles were coated with the cerium dioxide particles having hexagonal shape, which were precipitated by decomposition of cerium alkoxide. For this study, three coating processes were introduced to investigate the best coating parameters. Improvements in CMP of glass were also obtained by coating silica particles with cerium oxide nanoparticles.
While the minimization of device size in integrated circuits promises greater design flexibility and packing density, it also presents challenges with increased resistance-capacitance delays due to the high resistance of the small dimension metal lines, and the increased interline capacitance. Efforts to reduce the delay have resulted in the move to copper interconnects, as well as the development of new low-k dielectric materials to reduce line to line capacitance and cross talk noise. The novel properties of the latter materials have resulted in significant improvements in their integration into these small-scale interconnects. This paper will report on the challenges and advances in the chemical mechanical polishing of low-k organic and inorganic interlayer dielectric materials. Particular emphasis will be placed on the dependence of the polishing behavior of these materials on the chemical parameters of the slurry, such as the type and size of the abrasive particles.

9:00 AM M6.2 CHALLENGES IN DEVELOPMENT OF MANUFACTURABLE COPPER AND LOW-K DIELECTRIC CMP PROCESS. Yong-Suk Moon, David Msi, Kangil Wijekoon, Fritz Redeker, Rajeev Bajaj. Applied Materials, CMP Product Business Group, Santa Clara, CA.

As the feature size of microelectronic devices shrinks down to sub-0.18 micrometer, the clock speed delay caused by resistance (R) and capacitance (C) of the interconnection is higher than the gate delay. Interconnect delay is a critical issue for high performance microprocessors. The high density of interconnects in microprocessors has increased resistance and capacitance of the interconnects. This in turn increases the delay of the interconnects. The delay due to interconnects becomes a significant issue in high performance microprocessors. The increase in the delay due to interconnects is due to the increase in the resistance and capacitance of the interconnects. The increase in the resistance and capacitance of the interconnects is due to the increase in the number of interconnects and the decrease in the feature size of the interconnects. The increase in the number of interconnects is due to the increase in the number of transistors in the microprocessor. The decrease in the feature size of the interconnects is due to the use of smaller lithography tools.

The surface damage appears mostly along the edges of the wafer due to the high friction force by the direct wafer-pad contact. By using different mixed pressure distribution of the polishing pad, the surface damage along the wafer edges has been dramatically decreased. Post CMP cleaning of low-k dielectric materials is challenging because of the hydrophilic nature. A proprietary shearing agent completely removes the low-k dielectric material after CMP and keeps the surface hydrophilic. The solution cleans both the dielectric and copper surface without leaving any residue or damage to copper surface.

9:30 AM M6.4 CHEMICAL-MECHANICAL POLISHING OF STEEL BY CARBON-CONTAINING THIN FILMS. Stephen J. Harris, Gordon G. Krass, Ford Research Labs, Chemistry Dept., Dearborn, MI.

The material removal rate during polishing of steel by diamondlike carbon (DLC) and boron carbide (B4C) films falls by as much as four orders of magnitude during the course of several thousand polishing cycles. We provide quantitative trends that describe the abrasion kinetics. Not only the steel but also the DLC and B4C films are polished in the process, even though the films are at least 3-3 times harder than the steel. AFM analysis shows that the B4C coating becomes atomically smooth over regions of 100 nm by 100 nm as it polishes the steel. The polishing ability of the films is closely related to their nanoscale morphology but not to their microscale morphology. We provide evidence that the polishing of the films by the steel is primarily a chemical process, while the polishing of the steel by the film is primarily a mechanical process.

9:45 AM M6.5 CONTROL OF PATTERN SPECIFIC CORROSION DURING ALUMINUM CHEMICAL MECHANICAL POLISHING. Hyungjin Kim, Ponki Kwon, Sukje Lee, Hyung-Hwan Kim, Sungdok Lee, Chul-Woo Nam, Seo-Young Sung, Memory R&D Division, Hyundai Electronics Industries Co., Ltd, Ichon, KOREA.

A pattern specific corrosion of aluminum wires was found during aluminum chemical mechanical polishing process. This paper presents and discusses the particular pattern dependency of the corrosion behavior and effective control methods in order to reduce the corrosion. An aluminum single damascene structure on silicon dioxide thin film was prepared and the effects of process variables and pattern configuration on corrosion behavior were extensively explored. It was demonstrated that corrosion of aluminum wire was associated with cleaning media and pattern configuration. Two approaches were made for preventing the pattern specific aluminum corrosion: by changing CMP consumables and post polish treatments, and by modifying pattern configurations. An optimized process condition was successfully evolved from such approaches and resulted in corrosion-free aluminum damascene structure. Electrical data were also collected and corroborated with corrosion phenomena.

10:30 AM M6.6 DIGITAL VISUALIZATION OF PARTICLE DYNAMICS IN MODEL CMP GEOMETRIES. Claudia Zettler and Masami Yoda, Georgia Institute of Technology, School of Mechanical Engineering, Atlanta, GA.

Chemical-mechanical polishing (CMP), used to planarize silicon wafers, involves shearing an abrasive particle laden slurry between a rotating polishing pad and the wafer. The chemical and mechanical properties of the slurry, which consists of sub-micron colloidal particles suspended in a liquid lubricant, can greatly affect wear rates and material selectivity in CMP. The particle dynamics in a model CMP geometry were studied experimentally in this work. A technique for directly measuring the particle concentration near the wafer surface was developed and used to evaluate how various particle properties affect this concentration. We hypothesize that increasing this particle concentration by manipulating both chemical and mechanical particle properties could increase their influence on the wafer surface and hence CMP material removal rates. Evanescent waves were used to illuminate a roughly 300 nm thick region next to a solid glass surface. The surface, illuminating the wafer is fully flooded with an aqueous dilute particle suspension. The particle concentration near the glass surface and a rotating silicon surface textured with periodic micro-scale asperities, simulating the pad. Since the evanescent wave only illuminates a layer about one particle diameter thick next to the glass surface, the abrasive particle concentration near the glass surface can be measured simply by counting particles. The particle dynamics near the wafer surface will be studied by comparing results for smooth and periodically textured rotating silicon surfaces.
Although chemical-mechanical planarization (CMP) has successfully been employed in semiconductor device fabrication, the lack of comprehensive and quantitative understanding on CMP mechanism continuously hampered researches to establish CMP models. The existing CMP models help predict the rate and uniformity of the chemically modified layers on the wafer. We realize that the removal rate is a function of the formation and removal of the chemically modified layer. The chemistry in the slurry defines the formation rate of the chemically modified layer, while the removal rate is caused by the chemical and mechanical interaction. The observed removal rate is thus the balance of formation and removal of the chemically modified layer under certain chemical and mechanical conditions. We categorized the real CMP process into three categories: mechanically controlled, chemically controlled, and intermediate CMPs. The effects of chemistry, pressure, particle loading and particle size in different categories are discussed. The application of this model to tungsten CMP and copper CMP are also discussed in this paper.

11:40 AM M6.8

PARAMETERS AND PROCESS CONTROL FOR CMP MACHINES: A COMPARISON OF PRODUCTION WITH R&D DATA

We compared published data on CMP machines from R&D laboratories with production data to assess the performance of commercial equipment.

11:40 AM M6.9

A MODEL FOR EFFECT OF COLLOIDAL FORCES ON CHEMICAL-MECHANICAL POLISHING

A model is presented to predict the effects of colloidal forces on the CMP process. The model takes into account the interaction between the colloidal particles and the wafer surface, and how these interactions affect the removal rate.

11:50 AM M6.10

EFFECT OF ELECTROCHEMICAL INTERACTIONS ON CMP WASTE WATER TREATMENT

The effect of electrochemical interactions on the treatment of CMP waste water is examined. The findings show that electrochemical processes can significantly improve the treatment efficiency.

11:50 AM M6.10

ENVIRONMENTALLY-BENIGN CLEANING FOR GIGA DRAM USING ELECTROLYZED WATER

A new method of cleaning for Gigascale DRAM using electrolyzed water is introduced. The method is environmentally friendly and more effective than traditional cleaning methods.
semiconductor devices are scaled down, the number of manufacturing processes increases and the number of cleaning processes increases as well. The conventional RCA cleaning process consumes very large amounts of chemicals and ultra pure water (UPW). From environmental and commercial view points, it is clear that the cleaning process must reduce consumption of chemicals, UPW, and production costs. In this study, Si wafers contaminated with particles and metallic impurities were cleaned using the electrolyzed water (EW). Properties of generated EW such as oxidation-reduction potential (ORP), pH, and lifetime were measured. In order to compare characteristics of anode water (AW) with those of cathode water (CW) of EW on DHF treated Si wafer, contact angles were also measured. pH and ORP of AW and CW measured to be 4.7 and +1050 mV, and 9.8 and 750 mV, respectively. AW and CW were determined to be electron-donating and maintaining their characteristics for more than 40 minutes. Contact angles of UPW, AW, and CW on DHF treated Si wafer surfaces were measured to be 68.5°, 65.5°, and 56.8°, respectively. Therefore, it was understood that CW was prone to wetting on hydrophilic-terminated surface. AW was effective for Cu removal, while CW was more effective for Fe removal. The particle distribution after AW and CW cleaning showed the applicability for 0.1 μm particle removal. It is hence promising that this cleaning technology will be very effective for promoting environment, safety, and health (ESH) issues in semiconductor manufacturing.

2:00 PM M7.3 POLISHING AND CLEANING OF LOW k DIELECTRIC MATERIAL FOR HDI AND DAMASCENE. Yuchun Wang, Rajeev Bhatnagar, Yongsook Moon, David Mo, Kapila Wijesekera, Yufei Chen, Fritz Redicker, CMP Division, Applied Materials, Santa Clara, CA; Dan Sagrista, Le Quan Xia, EVD Low K Division, Applied Materials, Santa Clara, CA.

This paper describes CMP challenges in development of Cu-low k process technologies. As copper-Tesla FSG processes are being implemented successfully in early manufacturing, development focus has shifted to Cu-OSG integration development. Cu-OSG presents unique challenges with CMP integration, as these films tend to have much lower hardness than silicon dioxide. Significant process challenges have to be overcome prior to successfully implementing CMP process which does not mechanically damage the softer films and at the same time can achieve planarization requirements expected from CMP process. In addition, the OSG films tend to be hydrophobic leading to a need for developing improved cleaning processes/consumables. It was determined that AMAT ElectropolishTM barrier sputter is extendable to OSG films. Good removal rate and removal profile can be achieved with ElectropolishTM. A proprietary cleaning solution reduced defect counts by 2 orders of the magnitude on SurfScan S60200 on blanket hydrophobic wafers. The same cleaning solution can be applied to copper-low k damascene patterned wafers to clean both copper and dielectric surface. Polished Black Diamond films have RMS roughness less than 2 angstroms and copper surface roughness about 5 angstroms with good surface finish. Process performance using the Cu-FSG process was used to highlight capability gaps in the process. Process enhancements were then integrated into the new process. Blanket and patterned wafer results are presented to demonstrate final capability. Future directions for process enhancement are identified.

2:15 PM M7.4 MECHANISMS OF POST-CMP CLEANING. Emmanuele Estragnon, Hong Liang, Dept of Mechanical Engineering, Univ of Alaska Fairbanks, Fairbanks, AK; Kristian Bokten, Dan Mckell, Rippey Corporation, El Dorado Hills, CA.

There has been a great interest in understanding post-CMP cleaning mechanisms. From the view point of CMP engineers, this means to know the relationship between applied load, relative surface speed, resulting friction, and effectiveness of particle removal. Inevitably, this leads to maintaining the optimum water film thickness between a brush and the wafer/disk. This work simulates the cleaning conditions using a laboratory model system. Comparing with the classic lubricating concept as presented in a measured Striebeck curve, we have concluded that the cleaning process is bounded with an elastohydrodynamic process that involves a constant contact between a brush and wafer/disk.

2:30 PM M7.5 A STUDY OF CMP MULTI HEAD CMP TOOL EFFECT ON BPSG FILM FOR ADVANCED DRAM APPLICATIONS. David A. Hansen, Gerry Moloney, Cybeq Nano Technologies, San Jose, CA; David Whites, Ehren Technologies, San Jose, CA.

With the maturity of CMP processes and consumables most of the major IC fabrication companies are now investigating CMP tool designs that will help improve throughput while maintaining control with a corresponding reduction in COO. In the past most of