SYMPOSIUM N
Microelectronics and Microsystem Packaging
April 16 – 19, 2001

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*Invited paper
TUTORIAL

ST L/N/EE: ADVANCED TECHNIQUES FOR MATERIALS CHARACTERIZATION AND RELIABILITY TESTING

Monday, April 16, 2001
130 p.m. - 5:00 p.m.
Salon 10/11 (Marriott)

Advanced microelectronic interconnection structures make use of high-conductivity copper conductors with low dielectric-constant insulators at extremely small dimensions. As a consequence, issues arise in the characterization and reliability of these structures that are not found in the well-used aluminum-silicon system. Differences appear in the microstructure of the copper metallization and the changes induced in it by processing, thermal loading and electromigration; the mechanical characteristics of the surrounding dielectric; and, the resulting interdependence of the reliability of the interconnection structure and the changes in the metal microstructure as constrained by the dielectric. This tutorial will cover these topics, introducing participants to the issues involved and the fundamental reliability aspects of dielectrics (especially those of low-k materials), and metalization microstructure (by X-Ray diffraction) will be described.

Instructors:

Du Nguyen, IBM Microelectronics
Hari Babu Direen, IBM Microelectronics
Robert F. Cook, University of Minnesota
Stuart R. Stock, Georgia Institute of Technology

SESSION N1: PLASTIC ENCAPSULATION AND UNDERFILL

Chair: Anthony A. Gallo
Tuesday, April 17, 2001
Golden Gate A3 (Marriott)

8:30 AM N1.1 GREEN MOLDING COMPOUNDS

Anthony A. Gallo, Dexter Electronic Materials, Olean, NY.

New molding compounds for encapsulation of integrated circuits are required in the future because the bromine-containing dielectric retardants and antimony oxide flame retardant synergists, which are commonly used in present day molding compounds, are thought to be potentially unsafe to the environment. Phosphorus-containing compounds, have been proposed as flame retardants. Although they are less hazardous, molding compounds containing these compounds generally possess undesirable properties such as high moisture absorption. New molding compounds have been developed that are substantially bromine-free, antimony-free, phosphorus-free and yet pass UL94V-0 at 3.2 mm bar thickness. These molding compounds contain either two transition metal oxides with either standard epoxy cresyl novolac or diphenyl resin or a combination of a single transition metal oxide with highly aromatic epoxy resins or hardeners. Both molding compound types were found to give good moisture and high temperature electrical reliability for ICs encapsulated with these materials. Molding compounds with transition metal oxides have the potential for less health and environmental concerns because these metal oxides are suggested by the American Conference of Governmental Industrial Hygienists to be less hazardous than antimony trioxide.

9:00 AM N1.2 EVALUATION OF THERMO-MECHANICAL PROPERTIES OF GREEN MOLDING COMPOUNDS

Leonardo G. Saida, Ramah Lai, and Noel Lapar, On Semiconductor Philippines Inc., Cainta, PHILIPPINES

In an attempt to reduce and eventually eliminate the use of potentially hazardous halogenated compounds, On Semiconductor Philippines Inc. has evaluated the thermo-mechanical properties of select non-halogenated molding compounds (common name: green molding compounds or GMCs). The study included evaluation of thermal stability, adhesion properties, manufacturability and reliability of GMCs, as compared to conventional halogenated molding compounds. The data obtained from thermogravimetric analysis (TGA) revealed higher decomposition temperatures for GMCs containing magnesium hydroxide or phosphorized compounds as flame-retarders, relative to the decomposition temperatures for existing halogenated molding compounds. A preliminary study on the decomposition products of culls and runners, considered as waste products from the molding process, was conducted using TGA coupled with Fourier Transform Infrared (FTIR) spectroscopy and using Gas Chromatography-Mass Spectroscopy (GC/MS). Identified spectra for decomposition products for GMCs based on inorganic halogenated compounds were primarily acetone, cresols and phenols. Culls and runners from existing high-efficiency molding compounds yield methanol, phenols and acrylonitrile upon thermal decomposition. No significant and simple trend in adhesion property was observed in the resin type and flame-retardant variety in the different molding compounds. Thermomechanical FE model showed lower internal stress levels for the GMCs. Their manufacturability and reliability were found comparable to the conventional molding compounds. This paper discusses the relative thermomechanical stability of the green molding compounds and its potential impact on package robustness and on environmental concerns of the industry.

9:15 AM N1.3 PACKAGE CHARACTERIZATION AND FINITE ELEMENT ANALYSIS

Edgardo L. Buzon and Doris M. Asia, ON Semiconductor Philippines Inc., Cainta, Cainta, PHILIPPINES

The direction towards environment friendly manufacturing has triggered the semiconductor companies to source out materials and processes that eliminate the use of lead, antimony, bromine and other toxic packaging and process materials. On Semiconductor has initiated a corporate wide strategy to make our manufacturing meet or converge to a lead-free and green mold compound environment.

Study showed that lead-free solder requires 260°C-reflow temperature to optimize mounting of the surface mounted package on PCB’s. In this direction, characterization is done on the Ni/PnAu preplated 260JSP TSSOP at 260°C. The HI-reflow test and cold immersion test at same moisture sensitivity level 1 (MSL1) are done on this. Degree of delamination is measured each test, before and after preconditioning. Results are compared with the 265°C reflow requirement. Furthermore, finite element study was forthcoming to analyze package robustness on both 265°C and 260°C reflow temperatures.

9:30 AM N1.4 HYDROSCOPIC- SWELLING AND Sorption CHARACTERISTICS OF EPOXY MOLDING COMPOUNDS USED IN ELECTRONIC PACKAGING

Haleh Ardabili, General Electric Company at Corporate Research and Development, Schenectady, NY; Eun Young Kang & Michael Pecht, CALCE Electronic Products and Systems Center, University of Maryland at College Park, College Park, MD.

Moisture induced swelling mismatches between different materials in a microelectronic package can cause stresses that lead to underfill that inadequate failure driving force. In this study, the swelling coefficients of four types of epoxy molding compounds used in electronic packaging were measured. The samples were subjected to thermal and dimensional changes were measured using a thermo-mechanical analyzer. The moisture sorption characteristics of the four different types of molding compounds at 85°C/85% RH were determined from weight gain and moisture content. The effect of the moisture sorption temperature on the swelling coefficients was investigated by comparing swelling coefficients at 85C, 55% and 23°C. The molding compound characteristics including percentage fillers, TG and swelling density were examined in elucidating the swelling coefficients and the moisture sorption behavior of the four different types of epoxy molding compounds. The significance of swelling from reliability perspective for the four types of molding compounds was also determined.

9:45 AM N1.5 EFFECTS OF HYDRO-THERMAL AGING ON THE DIELECTRIC PROPERTIES OF EPOXY MOLDING COMPOUNDS

Patrice Guen, Alain Sylvestre, Lab for Electron & Dielectric Materials, University of Grenoble, FRANCE; Jerome Teysseire, Christoph Priore, STMicroelectronics, Corporate Package Development, Grenoble, FRANCE

During service IC packages are subjected to the combined effects of moisture (ambient) and thermal aging (soldering process, high-temperature applications). Such hydro-thermal aging is well known to be the origin of some mechanical failures (delamination, popcop cracking...). These effects have been well characterized in the past years. On the other hand, less data are available regarding the effects of hydro-thermal aging on the dielectric properties of packaging materials. Since dielectric characteristics -dielectric constant and dissipation factor- are key parameters for package design and modeling, it is important to understand the influence of humidity and temperature on these characteristics. In the present work we studied industrial epoxy molding compounds currently used for microelectronic packaging (polyfunctional epoxies loaded with 90 wt% silica). We measured the dielectric constant and the loss factor between 100 Hz and 100 kHz, as a function of hydro-thermal aging. Long term aging was simulated using Joint Electron Device
Engineering Council (JEDEC) standard procedures. In order to
distinguish between the effects of moisture and temperature the
humidity exposure and thermal stressing were varied separately.
In addition, to study the influence of cooling density on aging, the
study was performed for resins having different initial levels of curing.
We observed important variations in the dielectric properties as a
function of temperature and humidity on the adhesion performance of underfill material. The adhesion strength
(measured by die shear test on 2 mm by 3 mm) between the underfill and passivation does not show significantly after thermal
cycling test (−55°C for 10 min, 125°C for 10 min per cycle) for 1000
cycles. The adhesion strength of underfill material decreases with the
increase of test temperature above room temperature. The sharp
decrease occurs at a temperature below the glass transition
temperature of underfill material, as the decrease in adhesion strength versus temperature is due to the decrease in modulus of underfill and
decrease of interfacial interaction with the increase of temperature.
Adhesion strength of underfill with different passivation materials
decreases after aging in high temperature and high humidity
environment (pressure cooker test at 121°C, 2% RH, 50% relative
humidity for 24 hours, or 85°C/85% relative humidity for 500 hours).
The adhesion degradation after aging in high temperature and high
humidity environment is strongly dependent on the hydrophilicity of the
passivation material, which is characterized by contact angle of water
on the surface. Hydrophilic passivation such as SiO2 and SiN shows much
more severe adhesion degradation than the hydrophobic passivation
such as benczocyclooctetene (BCH) and polyimide (PI). Kinetics of
moisture diffusion into die shear sample is monitored by studying
moisture pickup of a 2 mm by 2 mm long orthogonal underfill sample.
Although the degradation of adhesion strength is due to the moisture
diffusion into the underfill, the rate of adhesion degradation of die
shear sample during aging in an 85°C 85% relative humidity environment is not controlled by moisture diffusion. The model on
adhesion degradation will be described. It will be demonstrated that
the adhesion stability for hydrophilic passivation can be successfully
improved by use of coupling agent such as organofunctional silane
that introduces stable chemical bond at interface.

11:00 AM N1.7
EFFECT OF COMPOSITION AND HEAD SETTLING ON
DEBONDING OF UNDERFILL LAYERS. Lorraine C. Wang
and Reinhold H. Dauskardt, Stanford University, Department of
Materials Science & Engineering, Stanford, CA.

With the increased complexity of microelectronic devices and a
general trend towards making chip packages smaller, the need for
reliable high-speed flip chip packaging is increasingly important.
In these packages, epoxy underfills are often used to surround a solder
ball grid array in order to help support both mechanical and thermal
stresses. The adhesion problems of the most critical issues that arise
in these systems involves the adhesion between the underfill and chip
passivation. Factors such as the incorporation of inorganic particles
within the epoxies and exposure to moisture can greatly affect this
adhesion. This research focuses on determining the mechanisms that
cause debonding between underfill systems and SiN passivation.
A fracture mechanics approach was used to test two model underfills,
one based on an anhydride epoxy, and the other based on a bisphenol F
epoxy. The underfills were exposed to temperature and humidity
conditions between silane substrates and constructed in a double cantilever beam (DCB) configuration. Interestingly, these two underfills, which are similar
mechanically, appear to show very different critical and subcritical
trends. The high adhesion strength under cyclic displacement, behavior typically seen in interface systems, while the bisphenol F underfill surprisingly shows little
susceptibility to stress corrosion. Although both underfills show evidence of multiple cracking, one has opposing effects on their critical adhesion values. The effects of varying filler content in
these underfills as well as environmental effects on the critical and
subcritical behavior of these systems will be examined.

11:15 AM N1.8
INVESTIGATIONS OF UNDERFILL FLOW OF MODEL
SUSPENSIONS AND INDUSTRIAL ENCAPSULANTS.
Thomas Dreier, Patricia N. Shannon, Eric Greiner, Binghamton
University, Dept of Physics, Binghamton, NY; Drew Davidson, Gary Lehman,
Binghamton University, Dept of Mechanical Engineering, Binghamton, NY.

In Direct Chip Attach (DCA), a critical step in manufacturing is the
underfill process. This procedure is necessary for minimizing stresses
that result from the mismatch between the coefficient of thermal
expansion (CTE) of the underfill materials and the microelectronic device
interconnects, etc. involved. The underfill process involves the
capillary flow of solid/fluid mixtures into flow passages that are
typically smaller than 1.27 microns. The underfill material consists of
spherical (generally silica) particles suspended in a high viscosity
(epoxy resin). Modeling this underfill flow process is difficult and
further complicated by the presence of the filler particles necessary to
achieve the desired CTE, particularly since the particles can be
comparable in size to the underfill gap spacing. Our modeling of the
underfill process, however, treats the material as a homogeneous fluid
(i.e. no particles) with measured fluid properties (e.g. surface tension, viscosity, etc.). Our research has concentrated primarily on a
parameter study and flow of model suspensions and an industrial
encapsulant. Wetting and rheological properties were measured for
purposes of modeling the flow behavior. The average flow front
position of the model suspensions and for industrial encapsulants is
computed from the change in capacitance as the underfill material
flows into the flow cell. Comparisons of flow distances and dynamics
and contact angle measurements between model calculations and
experiments are made.

SESSION 2: LEAD-FREE SOLDER AND
CONDUCTIVE ADHESIVES
Chair: Abhijeet Dua Gupta
Tuesday Afternoon, April 17, 2001
Golden Gate A3 [Merrill]

1:30 PM N2.1
MICROTHERMOMECHANICAL ANALYSIS OF LEAD FREE
SOLDER JOINTS. Abhijeet Dau Gupta, Peter Haskell, CALCE
Electronic Products and Systems Consortium Mechanical Engineering
Department, University of Maryland, College Park, MD.

This paper presents a micro-mechanical approach for modeling
fatigue damage initiation due to cyclic plasticity and cyclic creep in a
Pb-free solder. Such loading results in a complex stress and strain
cycling of electronic assemblies. Experimental measurement of fatigue
behavior is reported in this paper, under different temperature and strain rates. Fatigue damage due to cyclic plasticity is modeled
with dislocation mechanics. A conceptual framework is provided to
quantify the influence of temperature on fatigue damage due to
cyclic plasticity. Damage mechanics due to cyclic creep is modeled with a
void nucleation model based on micro-structural stress fields.
Micro-structural stress states are estimated using viscoplastic
phenomena like grain boundary sliding and its blocking at 2nd phase
particles, and dislocation creep relaxation. A conceptual framework
is provided to quantify the creep-fatigue damage due to
thermo-mechanical cycling.

2:00 PM N2.2
ELECTROMIGRATION OF FLIP CHIP SOLDER BUMPS ON
Cu/Si(N)/Al THIN FILM UNDER-BUMP-METALLIZATION.
Wojcieh Choi, Everett C.C. Yeh, and K.N. Tu, Dept. of Materials
Science and Engineering, UCLA, Los Angeles, California; Peter Elekans,
Haluk Balkan, FlipChip Technologies, Phoenix, AZ.

The electromigration of flip chip solder bump (eutectic SnPb) has been
studied at temperatures of 100, 125 and 150°C and current densities of
1.3 to 2.75 ×10^10 A/cm^2. The under-bump metallization on the
chips is thin film Al/Ni/V/Cu and on the board side is thick
electroless Ni coated with 30 μm of Au. Stressed at the highest current
density, the Mean-Time-To-Failure (MTTF) was found to decrease much
faster than what we expect from the published Black equation.
At one point where voids formed, the Ni/ V intermetallic layer was not
found. We note that this Ni/ V intermetallic layer has been found to be
very stable under multilevel reflows, but it disappeared in electromigration after a
high current stressing. In addition, the Cu/ Sn intermetallic compounds formed during the reflow is known to adhere well to the
thin film UBM, but they also detached from the UBM after current
stressing. Therefore, the UBM itself could be part of the reliability
problem of the flip chip solder joint under electromigration. By
simulating the current distribution in the sample, we found that the
current crowding occurs at the chip side where the current enters the
solder ball. We are able to match this simulation to the real
electromigration damage in the sample. The experimental result
showed that voids initiated from the position of current crowding and
propagated outward. This phenomenon of current crowing in flip
chip solder joints can increase MTTF.
The electromigration of eutectic SnPb and SnAg3.5Cu0.7 solder bumps on electroless Ni Under Bump Metallurgy (UBM) were characterized after current stressing at 125°C for several days at 10^4 to 10^6 A/cm^2 where the solder was cross-sectioned before current stressing. The marker motion on the cross-sectioned surface was used to calculate the rate of electromigration and the effective charge number of the solder. For eutectic SnPb, the effective charge number was between 6 and 8. After 10^5 A/cm^2, electromigration SnAg3.5Cu0.7, the marker movement was negligible so it was not possible to measure the effective charge number even after 200 hrs current stressing. The atomic flux of current stressing in SnAg3.5Cu0.7 was less than that in eutectic SnPb. Voids were observed in both solders on the cathode side of the joint. The growth of the intermetallic compound (IMC) between the Ni and the solders during current stressing is 10 to 100 times faster than the growth during solid state annealing. Dissolution of electroless Ni was observed. The dissolution of electroless Ni was affected by the Ni-Cu-Sn compound formation adjacent to the electroless Ni UBM. In Cu UBM on PCB side, no Cu dissolution was observed and there was no enhanced growth of Cu-Sn compounds during electromigration.

TEXTURED GROWTH OF Cu-Sn INTERMETALLIC COMPOUNDS. Kithan Prakash Hariharan, Thirumurthy Srinathan, Nanyang Technological University, School of Materials Engineering, SINGAPORE.

Rectangular sections of an extruded rod of Cu were reacted with Sn-Pb solder alloys of different composition over a range of temperatures above their liquidus temperatures to study the growth behavior of Cu-Sn intermetallic compounds (IMC) at the Cu-Sn solder interface. X-ray diffraction studies were carried out on the IMC layers in the reacted samples after selectively etching away the excess solder. The resulting diffractionograms consisted of very strong (101) and (102) peaks of α-Cu6Sn5 precipitate phase. The (101) peak height was high at all temperatures. In the low Sn solder (27Sn-73Pb), the α-peak peaks were absent at the two highest temperatures in the present study, but the (121) α-peak (Cu6Sn5) peak was prominent. Since many major peaks of these compounds listed in JCPDS cards were either absent or small, a crystallographic texture was suspected in the IMC layers. Hence, pole figures were constructed using the conventional texture goniometer. For the (101) pole figures, and for the α-phase (102) pole figures were constructed. They confirm a strong texture in these phases normal to the surface of substrate Cu. The growth directions were identified to be <110> and <102> for α- and <112> and <103> for α-phase. The growth directions do not change with extract time and temperature although the layer thickness and morphology undergo substantial changes. The morphology of the α-phase layer varies gradually from a cellular film with rugged interface to a dense film with scalloped interface as the Pb content and temperature increase. The α-phase was dense and planar. It is expected that the textured growth of the IMC layer would give rise to anisotropy in properties such as electrical resistivity and mechanical properties of the joint.

COMPARISON OF SOLID STATE AGING AND WETTING REACTION OF EUTECTIC-TIN-LEAD AND LEAD-FREE SOLDER ON COPPER. T.Y. Lee, W.J. Choi and K.N. Tu, Univ. of California Los Angeles, Dept. of MSE, Los Angeles, CA; J.W. Jang, S.M. Koo, J.K. Lin and D.R. Freer, Motorola, Interconnect System Laboratory, Tempe, AZ.

The intermetallic compound (IMC) growth of four different solders — eutectic SnPb, SnAg3.5, SnAg3.5Cu0.7 and SnCu0.7 — on Cu Under Bump Metallurgy (UBM) during solid state aging and wetting reaction was studied. The four solders were refloved twice on Cu at 240°C for 2 min and followed by solid state aging at 125°C, 150°C and 170°C for 500 hrs, 1000 hrs and 1500 hrs. The morphology and the growth mechanism of the IMC layers were studied. The specific growth rate is diffusion-controlled growth, respectively. The activation energy was 0.94 eV for eutectic SnPb, 1.03 eV for SnAg3.5, 1.01 eV for SnAg3.5Cu0.7 and 1.05 eV for SnCu0.7. However, the activation energy of the wetting reaction was between 0.2 and 0.3 eV and the morphology was scalloped-type. The growth mechanism was ripening-controlled. The rate of IMC growth is 10^4 times different between the reactions, i.e. 1 μm/min for wetting reaction and 10^2 μm/min for solid state reaction. Even though the Gibbs free energy changes per mole at 240°C and 170°C are not significantly different, the rate of Gibbs free energy change is significantly different.

Therefore, the scallop morphology during the wetting reaction is stable due to the high rate of Gibbs free energy change, even though the reaction type has much higher surface energy than the solid state type. During the solid state reaction, the slow change in Gibbs free energy causes the IMC to change from the scallop type to the layer type.

INTERFACIAL PHASE FORMATION IN Sn-Ag-Cu SOLDER JOINTS ON Ni/Au COATED BOARDS. Keisuke Nishida, Masahiro Ono, Hiroshi Aikawa, Shinji Kashiwamura, Osaka University, Japan.

Ni/Pt/Au coatings have been extensively used as a finish system on PCB pads because Ni coating provides flat and uniform surface and also serves as a diffusion barrier between solder and copper. However, nickel phosphide intermetallic compounds between Ni-Au and SnPb showed a problem of joint reliability. Au-Sn re-deposits at interface after thermal cycling or aging. Phosphorus is accumulated between Ni-Au and nickel phosphide intermetallic compounds. This interfacial structure greatly degrades the mechanical properties of the joints. Pb will be eventually eliminated from electronic products and Sn-Ag-Cu alloy has been considered as the most promising substitute for the Sn-Ag-Cu solder. Interfacial reaction of the Sn-Ag-Cu solder with Ni(Pt)/Au finish on board has been investigated in this work. Transmission electron microscopy and scanning electron microscopy were employed to analyze the interfacial microstructure. The intermetallic compound Cu6Sn5, containing a small amount of Ni, was found to preferentially form on the Ni coating. This compound layer served as a barrier for the reaction of Sn with the Ni coating. On the Ni(Pt) side, a nickel phosphide was identified. Thermodynamic modeling of the Cu-Ni-Sn system was carried out to rationalize the segregation of Cu at the solder/finish interface. Effects of the interfacial reaction on joint reliability are discussed.

FATIGUE AND INTERMETALLIC FORMATION IN LEAD FREE SOLDER DIE ATTACH. Patrick McCasker, Craig Hallman, and Zheng Yang, University of Maryland, College Park, MD.

With the advent of many new lead-free solder materials, it is important to understand their reliability as die attach. However, little information is available in the literature on the fatigue properties of thin films of these materials. The fatigue is critically needed to evaluate the lifetime of power electronic modules. In this paper, we will discuss analytical, semi-analytical, and numerical methods for assessing the fatigue behavior of large area solder die, the use of mechanical testing as a way of determining the fatigue coefficients and the validation of these methods against thermal cycle testing. Furthermore, most of the Pb free solder candidates being considered for moderate to high temperature applications, such as Sn95.5Ag0.5Cu0.7, consist of small amounts of alloying elements added to Sn. The abundance of tin assists in surface wetting by promoting intermetallic reaction with the underlying plating materials. However, it is this same tendency of tin to form intermetallics that raises a long standing reliability concern regarding high tin solders. The brittle intermetallic is prone to fracture, especially in the presence of voids created by symmetric interdiffusion. We will discuss experiments developed to model and address intermetallic reliability concerns.

CERTIFICATION AND SOLDERING OF ORGANIC SOLUTION MODIFIED ALUMINUM THIN FILMS AND BOND PADS. Rui Feng, Eric Dahlgren, Matt O'Keefe, Tom O'Keefe, University of Missouri-Rolla, Dept of Mechanical Engineering and Materials Research Center, Rolla, MO; Wu-Sheng Shih, Brewer Science, Rolla, MO; Dan Grumet, Motorola, Schaumburg, IL.

The use of solder connections on integrated circuits with aluminum bond pads for applications such as direct chip attach, or to form grid arrays and chip scale packages is increasing. In order to have a weatable surface and reliable solder joint, under bump metallization (UBM) is deposited onto the aluminum bond pad prior to solder deposition. The UBM is usually deposited by sputtering, deposition, photolithography and etching, as is the case for copper, or by electroless plating directly onto the bond pads, as is done for Ni/Au. In this study an immersion plating process using organic solutions containing copper and palladium is described. Even though the film quality is lower than that of thick Pd-interlayer and passives the surface of thin film aluminum surfaces and bond pads for subsequent electrodeless copper deposition and solderability tests. It was demonstrated that the copper and palladium particles deposited from the organic solution onto spatter deposited aluminum thin films were able to act as nuclei sites for the subsequent build up of adherent, continuous copper films from formic/hyphosphoric electroless plating baths. In addition, the metal deposition from organic solution process was found to be effective on patterned test vehicles and integrated circuits as metal deposition
4:15 PM #2.0
FUNDAMENTAL ISSUES IN ELECTRICALLY CONDUCTIVE ADHESIVES. James E. Morris, State Univ of New York at Binghamton, Dept of Electrical Engineering, Binghamton, NY.

Electrically Conductive Adhesives (ECAs) offer significant advantages over solders for both surface mount and flip chip interconnection, including no lead content, improved flux pitch performance, greater compliance, and lower process temperature leading to lower thermomechanical stress and better reliability. Nevertheless adoption has been slow, other than for niche applications, with impact resistance remaining the primary obstacle. This paper will review the status of inorganic Conductive Adhesive (ICA) technology concentrating on recent research results, and on the new directions they suggest.

4:45 PM #2.10
SIMULTANEOUS MEASUREMENTS OF ELECTRICAL RESISTIVITY AND RAJAN SCATTERING FROM CONDUCTIVE DIE ATTACH ADHESIVES. J. Meghetha, R.C. Benson, and T.E. Phillips, Johns Hopkins Univ, Laurel, MD; J.A. Emerson, Sandia National Laboratories, Albuquerque, NM.

Silver (Ag)-filled conductive polymer adhesives have been widely used in microelectronic packages due to their lower temperature processing relative to inorganic solders. It is known that the development of electrical conductivity in Ag-loaded adhesives is dependent on the thermal profile of the curing process. The chemical reactions at the interfaces of the silver particles during the cure determine the subsequent performance of the conductive adhesive system. The interaction between the Ag particle and its lubricant layer affects the subsequent particle interaction with the polymer adhesive system, other particles, and the electrical contact on the component or substrate. Therefore, a key to understanding the interfacial properties of the particle, and hence the electrical performance of the conductive polymer lies in the ability to probe the chemical nature of the Ag surface in an in-situ environment. Despite the importance of the lubricant-coated Ag particle, little attention has been focused on the behavior of the Ag interface under conditions that are consistent with polymer curing. In an attempt to characterize the behavior of adhesive electrical conductivity with the chemical nature of the Ag particle interface, we have simultaneously performed four-point electrical resistivity and surface enhanced Raman scattering (SERS) measurements on commercial conductive adhesives. For SERS, studies have shown that it provides chemical specificity and surface sensitivity to interfacial processes such as adsorption and decomposition. In this study, the SERS investigation focused on the interaction between the lubricant layer and the Ag surface under thermal processing conditions that were employed during the cure of adhesives metal in electronic technologies. Variations in the chemical structure of the lubricant layer and decreases in the resistivity of the adhesive were observed at specific points in the curing, suggesting a correlation between macroscopic electrical conductivity and the chemical composition of the particle interface.

SESSION N3: POSTER SESSION
MICROELECTRONICS AND MICROSYSTEMS
PACKAGING
Tuesday Evening, April 17, 2001
8:00 PM
Salon L-7 (Marriott)

N3.4 MECHANICAL PROPERTIES AND FRAGILITY BEHAVIOR OF THE Cu AND CuSbS-Dispersed SnSb, Solder Bumps Processed by Screen Printing. Ho-Seob Cha, Kwang-Eung Lee, Tae-Sung Oh, Hong K Univ, Dept of Metallurgical Engineering and Materials Science, Seoul, KOREA; Jin-Won Choi, Package R&D ChipPAC, Ichon, KOREA.

Cu and CuSbS-dispersed SnSb (SnSb-37pb) solder bump of 760 μm size were fabricated on Au (0.5 μm)/Ni (3 μm)/Cu (27 ± 20 μm) BGA substrates by screen printing process, and their microstructure and shear strength were characterized with variation of dwell time at reflow peak temperature (290°C) and aging time at 150°C. With the dwell time of 30 seconds at reflow peak temperature, the CuSbS-dispersed solder bumps exhibited higher shear strength than the Cu-dispersed ones. With increasing the dwell time longer than 60 seconds, however, shear strength of the CuSbS-dispersed solder bumps became lower than that of the Cu-dispersed ones. Shear strength of both Cu and CuSbS-dispersed solder bumps increased with increasing the aging time at 150°C. The failure surface of the solder bumps could be divided into two regions of crack propagation and critical crack propagation, and the shear strength of solder bumps was inversely proportional to the crack propagation length.

N3.3 MECHANICAL AND MECHANICAL PROPERTIES of the Sn-Ag SOLDER ALLOY WITH ADDITION of Bi and Cu.
Kwang-Eung Lee, Ho-Seob Cha, Kwang-Yong Lee, Tae-Sung Oh,
Microstructural and mechanical properties of the Sn-Ag solder alloys were characterized with addition of Bi and Cu up to 9 wt% to Sn-3.5Ag composition. Compared to the Bi-added Sn-Ag solder alloys, large amount of second phase and fast growth of second phase were observed in the Cu-added alloys. The Bi-added Sn-Ag solder alloys exhibited higher yield strength and higher ultimate tensile strength than the case of Cu-added Sn-Ag solder alloys. The yield strength of the Sn-3.5Ag solder alloy increased from 20 MPa to 50 MPa and to 36 MPa, respectively. The melting temperature of the Sn-3.5Ag solder alloy decreased from 221°C to 218°C and to 217°C with addition of 9 wt% Bi and Cu, respectively. In this study, Bi and Cu-added Sn-Ag solder bumps of 760μm size were also fabricated on the AlCu (0.5 μm)/Ni (μm)/Cu (±20 μm) BGA substrates, and their microstructure and shear strength were characterized. The addition of the dwell time at reflow peak temperature (220°C).

N.3.6 NEW STEPPED PROCESS AND MATERIALS FOR CHIP BONDING TECHNOLOGY OF NONRIGID AND FLEXIBLE SUBSTRATES. Sung Kyu Park, Jeong In Han, Won Keun Kim and Min Gi Kwon, Electronics Devices Research Center, Korea Electronics Tech. Inst., Pyungteck Kyungji, KOREA.

Reliable interconnection of electrodes to the plastic-based display with anisotropic conductive films (ACFs), of which the conductive particles were epoxy resin, is a major challenge for BGA substrates, was accomplished. The contact resistance value was maintained even while the junction was stressed under sudden changes in temperature and pressure. It was found that the conduction failure was caused by the action of a complex mechanism on the changes in temperature and pressure. The major driving factor seems likely to be defects in the transparent electrode due to the thermal strain of substrates and penetration of conductive particles. Conductive particles with elasticity similar to that of the plastic substrate did little damage to the transparent substrate under normal conditions, while a conductive process did not bring about their deformation either. As a result, a highly reliable interconnection with a very low contact resistance (20-50Ω) was realized. In addition to these reliable interconnections, we analyzed the relationship of conductive particle size and bump volume on contact resistance for these substrates. Finally, a prototype plastic film LCD module was fabricated using a driver IC and a polycarbonate based super twisted nematic (STN) LCD panel to confirm whether the module could be realized in accordance with our experimental results.

N.3.7 USING THE SURFACE POTENTIAL DECAY METHOD TO PROBE ELECTRICAL CONDUCTIVITY IN THEPackage. Alain Sylvestre, Patrice Goncal, Lab for Electrostatics and Dielectric Materials, University of Grenoble, FRANCE.

Transverse and longitudinal conductivities quantify the attitude of materials to neutralize an electric charge deposited on their surface. The method which is usually used to determine these conductivities consists in applying electrodes on one side of the sample and measuring the resulting current. This method presents some difficulties related to the contact of electrodes with the insulator. Moreover, the voltage cannot be very weak if one wants to obtain a measurable current and, if the voltage is high, electric discharges can be occur at the edges of the electrodes. Another difficulty is to separate the capacitive current from the conduction current corresponding to the flow of the charges in the electric field. Another way to reach these characteristics is the Surface Potential Decay (SPD) method. An electric charge is deposited on the surface by corona discharge. The surface takes a potential which will change in time, the charge flowing out either through the surface or the volume. The SPD is measured by an induction probe. The interest of this method lies in the absence of electrode on the upper face of the sample, as well as in the absence of high voltage source. In this work, we present the potentials of this method to investigate insulating materials in particular epoxy resin used for packaging. We emphasize the influence of electrical and thermal stresses on the conductivities in these materials and we investigate the importance of relative humidity on these properties.

N.3.8 Abstract Withdrawn.

N.3.9 Packaging for A Sensor Embedded in Concrete


The Johns Hopkins University Applied Physics Laboratory is developing packaging for a sensor platform to be embedded in the highway environment of concrete structures for monitoring corrosion-related degradations over extended periods of 25 years or more. The United States is replacing aging infrastructure and simultaneously developing the tools and techniques to monitor new infrastructure as it ages. The HEPS has requirements for infrastructure monitoring, especially bridge deck monitoring, and developed a concept based on distributed, embedded sensors. The Wireless, Embedded Sensor Platform (WESP) will implement the concept of low-cost, customizable sensor platform suitable for long-term performance in the field. The WESP is designed to be powered and queried remotely as often as required and can be used to map the time evolution of the structural degradation. The objective of this research is to develop and demonstrate packaging techniques for embedded sensor suites commensurate with a 50-year lifetime embedded in concrete that is at a pH >13, and exposed to harsh environments of salt, moisture, mechanical, and thermal stress. The sensor and communications design for such a system is being developed in parallel with the packaging and reliability efforts. To meet this objective, the WESP construction will use a commercial ceramic IC packaging and unique manufacturing and assembly techniques. The prototype is expected to provide sensor identification, temperature, pressure, and conductivity data within a package volume less than 2 cm³ (0.12 in³). Reliability tests will be conducted to evaluate the lifetime and performance for the packaging design. These include such tests as freeze/thaw cycling, thermal shock, thermal cycling, HAST, S8/S8, and accelerated life testing. Future developments will implement additional sensor types to fully characterize the concrete environment.

N.3.10 ELECTROMIGRATION IN LEAD FREE AND EUTECTIC TIN-LEAD SOLDER POWER FLIP CHIPS. Patrick McGhaver, Dhiraj Bussel, University of Maryland, College Park, MD.

The automotive industry has used flip chip for many years as a high density interconnection method in hybrid power modules. With the advent of lead free solder, there is considerable interest in determining the relative electromigration resistance of lead free solder flip chip bumps with respect to tin-lead eutectic bumps, especially at the high current densities needed to power the electronics used for automotive applications. This study focused on the relative susceptibilities and underlying material processes leading to electromigration failure of Sn0.35Pb0.65 eutectic and a lead free solder. To conduct the study, sample boards were constructed consisting of alloyed flip chip die, 0.25 inches on side, attached with one of the two materials. Half of the samples of the solder material were powered so a current density of 6110 A/cm² was maintained through each sample and the other half was kept unpowered. All the samples were subjected to a high temperature lifetime test so that a junction temperature of 150°C was achieved, and any change of resistance of the samples was monitored in situ. The lead free solder investigated was found to have a longer mean time to failure than its eutectic tin-lead counterpart. However, the mode of failure for eutectic tin-lead solder was found to be a slow and steady increase in resistance as opposed to a sudden and complete electrical open for lead-free solder. The presence of large voids in the solder bumps did not have a substantial effect on the rate of failures in both the solders. This presentation will discuss these findings and provide detailed information on the mechanism of failure.

SESSION N4: MICROSYSTEM PACKAGING
Chair: J.C. Bourdeaux and Howard R. Last Wednesday Morning, April 18, 2001
Golden Gate A3 (Marriott)

8:30 AM N4a.1 MEMS PACKAGING: OPPORTUNITIES AND CHALLENGES. Ari L. Elbahnas, Univ. of Arkansas, Electrical Engineering Dept., Fayetteville, AR.

Micro-Electro-Mechanical Systems (MEMS) are rapidly evolving into an important and promising technology. The ability to fabricate switches, micro pumps, sensors, and an array of actuators that can perform unique and complex functions in very compact form factors is an exciting prospect. Potential target electrical applications include: T/R switches in wireless and microwave products, phase shifters, tunable filters, and tunable oscillators. However, a key challenge is the packaging of these devices. Conventional packaging techniques such as plastic encapsulation are generally not suitable for these devices, since
the encapsulant would restrict the movement of the internal mechanical components. In addition, a wide range of new problems that have not yet been faced, arises due to the novel nature of these devices. Some of these problems include: the dicing of MEMS in a manner that does not damage the structures, creating less heat and stress on the wafer, and generating less particles, manipulation of the diced components without damaging the fragile mechanical structures, mechanical and fluidic feed through to the outside world, as well as the fabrication of moving parts, in order to facilitate the production of a more durable and reliable product. This paper will provide a brief overview of MEMS/MOEMS packaging systems as well as the state of the art MEMS packaging techniques. In addition, key problems in MEMS packaging will be highlighted and potential solution will be discussed.

9:00 AM #N4.2
INNOVATIVE MEMS AND MOEMS PACKAGING CONCEPTS
Ken Gilkes, Cochran Electronics, Fitchburg, MA
More than 2 decades old, Micro-Electro-Mechanical Systems (MEMS) paradoxically began to generate tremendous interest just as we entered the new millennium. Traditional MEMS is widely deployed in airbag triggering accelerometers and made-by-the millions ink jet printer cartridges. But it is the emerging advanced MEMS that piques interest. This is because MEMS represents the single point of technology convergence where electronics, mechanics, physics, chemistry and biology can all be merged on a single slice of silicon. Now add optics and we move up to MOEMS: micro-opto-electro-mechanical systems where “magic mirrors” beam the digital cinema into theater screens or route a rainbow of data-rich photons for the new, glass Internet super-highway. But the all-important package has been left behind relegated to an insignificant afterthought. Yet failure to invent a cost-effect MEMS/MOEMS packaging system will likely limit the use of these wonderful 21st century technologies. The cost-hardened classical hermetic package is only a short-term solution for many of the applications. New and innovative packages have been proposed and several have already been built. Some enable fabrication of glass chips, while others use minimal chips on glass chip carrier platforms. Some a new hermetic, but use “getters” to extend life even for critical optical mirror products. This paper will describe the newest design concepts for MEMS/MOEMS and provide a status report on specific packages already built for this technology. Several newer package-enabling materials will also be discussed that include getters and vacuum-deposited anti-stiction agents. Time in and participate in the Grand Convergence of Technologies.

9:15 AM #N4.3
MATERIAL SYSTEM FOR PACKAGING 500°C SiC MICRO-SYSTEM
Liu-Ming Shen, AVT Research Corp. /NASA Glenn Research Center, Cleveland, OH; Robert S. Okole, Philip G. Neudeck, Gary W. Hunter, NASA Glenn Research Center, Cleveland, OH
A systematic packaging technology for high temperature microsystems is essential for both in situ testing and commercialization of high temperature microsystems. Core technologies needed for high temperature electronic packaging are electrical interconnections and die-attach. Aluminum and aluminum oxide were selected as packaging substrates and precious metal thick-film materials were selected for electrical interconnection system (thick film printed wires and thick film metallization based wire-bond) and conductive die-attach layer for high temperature applications. This approach has shown promise. During a 2000-hour test in atmospheric oxygen with and without electrical bias, the electrical resistance of thick-film based interconnection system demonstrated both low and stable electrical resistance at 500°C. A silicon carbide (SiC) Schottky diode was attached to ceramic substrate using gold-thick-film material as the conductive bonding layer and was successfully tested at 500°C in air for more than 1000 hours. These results indicate that the ceramic substrate metallization based interconnection system and die-attach scheme provide a material framework for packaging 500°C operable SiC microsystems. In addition to a general packaging design for SiC electronics and sensors, robust hermetic and non-hermetic packaging for absolute and differential SiC pressure sensors will be discussed with specific packaging requirements. Engine performance parameter monitoring sensors such as pressure sensors must be thermally stable and functionally reliable during their operational life which heightens the demands on the reliability of their packaging. These requirements include reliable contact metallization (on the SiC chip) and the ability to reduce thermomechanically induced stress. High temperature, high power device and gas sensor packaging will also be discussed in parallel. Progress in this area will be presented.

10:15 AM #N4.4
CARRIER-LEVEL PACKAGING AND RELIABILITY OF A MEMS BASED SAFETY AND ARMING DEVICE
Rajesh Swaminathan, Peter Sandborn, CALCE Electronic Products and Systems Center, University of Maryland, College Park, MD; Michael Deeds, Naval Surface Warfare Center, Indian Head, MD
The carrier-level packaging for a MEMS based Safety and Arming (S&A) system has been considered. The package houses the S&A chip, integration demister, and a 3-axis accelerometer demister. The carrier-level package provides traditional electrical, fiber optic, pressure, and explosive interconnects. The S&A chip contains a moving “slider” that either exposes a hole through the chip or blocks the hole, as well as various environmental sensors used to confirm the demister has reached the target position. The demister chip converts electrical energy to mechanical energy upon demand to initiate the explosive train. The demister is placed between the S&A chip and the initiator chip to restrict out of place measurement of the MEMS structures. Various hermetic technologies and carrier approaches/materials have been assessed. The carrier designs include hermetic, non-hermetic, and breathable packages. The impact of moisture ingress and gress from the carrier packaging have been studied as a function of the performance of MEMS parts.

10:45 AM #N4.5
AMBIENT GAS ANALYSIS OF HERMETIC ENCLOSURES
Robert K. Lowry, Intersil Corporation, Analytical Services Laboratory, Melbourne, FL
Hermetically sealed enclosures for microelectronic, MEMS, and optoelectronics devices and associated components may contain gaseous species that can ultimately endanger the functionality of the system. Condensates of moisture and/or ammonia, especially in conjunction with ionic impurities, can result in corrosion, resulting in electrical opens in conductor lines or contacts. Atomic oxygen can oxidize and cause mechanical failure of solder or damage to other oxidation-prone materials within the enclosure. Military specifications impose concentration limits for various species in sealed package cavities of 5000 ppmv and 2000 ppmv, respectively. While there are no specified maximum limits for other volatile species, condensates of organic substances that volatilize from adhesives or other hydrocarbons may form residual deposits that interfere with proper mechanical operation of gears or other moving parts. In optoelectronic systems, condensates of moisture or volatile organics may cloud mirrors and degrade performance. Hydrogen is a rapid disseminator that can degrade MOS device functionality. Argon has been reported to cause arcing in high-power RF hybrid packages. Otherwise, argon and other gases such as carbon dioxide and helium, are not known to adversely affect mechanical or electrical device operation, but their detection can provide clues to packaging materials behavior and overall physical and mechanical integrity of the enclosure. Knowing the ambient gas composition of hermetic device enclosures assists in selecting high quality package materials and enables hermetic sealing process control to assure reliable products. This paper describes the analysis method for hermetic enclosures, known as Residual Gas Analysis (RGA). It discusses methods and scaling practices for new possible sources for the gaseous species which may endanger sealed product reliability. It gives material selection and process improvement guidelines to reduce and control volatile species in hermetic enclosures.

11:15 AM #N4.6
IMPLEMENTATION OF A LOW TEMPERATURE WAFER BONDING PROCESS FOR ACCELERATION SENSORS
Wafer bonding technologies are used for the fabrication and packaging of micro mechanical devices in bulk and surface micro machining. A special low temperature bond process was integrated into the technological process flow to produce an acceleration sensor fabricated by TEMIC TELEFUNKEN microelectronics GmbH. Detailed investigations should show to which extent the low temperature bonding process is able to replace an anodic bonding process between pyrex and silicon. The reason for this wafer substraction was the measured offset sensor values caused by the different expansion coefficient of the glass bottom wafer and the silicon middle wafer. The implementation of the low temperature wafer bonding process which should be used requires special surfaces quality of the process wafer. It is found that the more important parameters are the oxide or silicon oxide roughness as well as the surface contamination caused by the technology process steps before the bonding step. In the paper a low temperature bonding process used with an oxygen plasma pre-treatment followed by 400 °C anneal will be presented with the results of infrared transmission as well as the measured bond
strengths of the prepared test wafers will be plotted. First dicing tests have shown that the new bonding process has the potential to replace the glass wafers. During the development of this bonding process it was shown that it is possible to reach a bond strength between 1.8 J/m^2 and 2.4 m^2 depending on the annealing time. To optimize the necessary size of the bond frame and the bond strength a test pattern was designed with different sizes of bond frames, main structures and chevron notch structures. These structures are used to qualify the bond results concerning the bond strength and bond reproducibility depending on the process technology and sensor design. The results of these investigations are represented in the paper.

11:30 AM N4.3

Amorphous-Diamond (a-D) thin films deposited by pulsed-laser deposition typically have high levels [6-10 GPa] of residual stress. This stress is thought to be intrinsic to the deposition process, but is not intrinsic to hard [>85 GPa] a-D films, since thermal annealing to moderate temperatures (600°C) can completely remove the stress without significantly changing the 4-fold carbon content. We have taken advantage of these low stress a-D films to create true surface micromechanical structures (MEMS). We have fabricated cantilever beams, tensile pull tabs, notched beam pull tabs, and friction test structures to evaluate the micromechanical properties of these films. Tensile test results were obtained by using a nanoincisor to pull laterally on the samples until fracture occurred. The a-D fracture strength was found to be ~8 GPa, much higher than CVD diamond films (~1 GPa), but lower than the yield strength (75 GPa) derived from traditional nanoindentation measurements. The reason for the difference in strength is presumably due to defects that serve as stress concentrators for crack initiation. Obscure candidates for defects in this system are point defects inherent in the deposition process and imperfections introduced due to imperfect device processing. In this amorphous material, defect characterization is difficult but results of SEM, TEM, cross-section EELS, and 13C NMR experiments will be employed to attempt to relate defects and nanoroughness to the observed fracture strength.

This work was sponsored by the U.S. Department of Energy under contract DE-AC04-94AL85000 through the Laboratory Directed Research and Development Program, Sandia National Laboratories.

11:45 AM N4.8

MEMS devices may experience significant alternating loads during service, associated with both applied and vibrational loading. Long-term reliability and lifetime predictions require a careful study of possible fatigue mechanisms in these devices. The material is not generally considered susceptible to fatigue crack growth, recent studies suggest that there may be fatigue processes in silicon MEMS structures. The effect, however, has not still been extensively studied. In this work, we used the micro-mechanical impressive double cantilever beam specimen geometry to examine stable crack growth. Crack growth tests were performed under displacement control under both static and cyclically varying loads. Due to the high compliance of the sample structure, the load was minimally with crack growth. Fatigue crack-growth tests were performed at an applied load frequency of 20 Hz. A titanium thin film was sputtered onto the zide face of the sample to accurately measure crack growth from changes in electrical resistance. The fatigue crack-growth tests were monitored throughout the test in order to distinguish between the role of possible environmentally assisted crack-growth (stress corrosion) processes and mechanically induced fatigue mechanisms. Implications for devices reliability are discussed.

SESSION N5 HIGH TEMPERATURE, HIGH POWER PACKAGING

Chair: F. Patrick McCuskey
Wednesday Afternoon, April 18, 2001
Golden Gate A3 (Marriott)

130 PM N5.1
NOVEL MATERIALS AND JOININGS FOR POWER ELECTRONICS MODULE PACKAGING Eckhard Wolfgang, Gerhard Mue, Gae Lefrant, Herbert Schwarzer, Siemens AG, Corporate Technology, Munich, GERMANY.

Power module packages consist of several layers of different materials according to their function. A base plate is necessary for mounting the module to the cooling unit and to shield key components against high voltages, the power semiconductor chips having metal electrodes on both sides are used for switching currents, and finally power passage layers have to protect chips against high electric fields and environmental impacts. The combination of semiconductors, metals and insulators and their different coefficients of thermal expansion leads to stresses and fatigue during temperature excursions. There are some major trends which require the use of new materials and joinings. Higher voltages (up to 6.5 kV), higher currents (above 2000 A), and higher operating temperatures, e.g. in automotive applications (up to 200°C). To reduce the influence of the thermal mismatch between the base plate and the insulator (Al/HfAlIN) metal layers in the power module the copper base plate and the Si chips to the ceramic substrate a low temperature joining technique using Ag powder under high pressure - can be used which turns out to be reliable at temperatures up to 200°C.

2:00 PM N5.2
A NOVEL PACKAGING CONCEPT FOR HIGH POWER PRESSEPAK IGBT MODULES E. Herr, S. Kraftmann, T. Lang, R. Schlegel, ABB Semiconductors AG, Lenzburg, SWITZERLAND.

Ceramic packaging has been the standard technology for bipolar high power device such as diodes, thyristors and GTOs. High power IGBTs (Insulated Gate Bipolar Transistor) are more and more replacing the thyristors and GTOs for high power applications. They are commercially available as multi-chip modules in plastic packages and as PressPak devices in ceramic packages. A novel packaging concept for high power IGBTs will be presented in this paper, using plastic packaging for PressPak devices, thus combining the advantages of the two available packaging technologies. It will be demonstrated that a considerable number of requirements and constraints severely narrow the choice of materials that can be used. High power devices are mostly used in harsh environments. At the same time, the useful life of the components is required to be 20-30 years. Most critical for proper device performance and good reliability are housing materials, molding compound, and contact materials. It will be explained how these materials were selected and qualified for the use in IGBT high power devices.

2:30 PM N5.3
A DIPBLE ARMY INTERCONNECT TECHNIQUE FOR POWER SEMICONDUCTOR DEVICES Simon S. Wen, Dae Huf, Guo-Qun Lu, Virginia Polytechnic Institute & State Univ, Center for Power Electronics Systems and Dept of MSE, Blacksburg, VA.

This paper describes a wireless-bond interconnect technique, termed Dingle-Army Interconnect (DAI) technique for packaging power devices. Electrical connections onto the devices are established by so-called arrays of parallel wire bonds. Although this approach appears simple, preliminary experimental and analytical results demonstrated potential advantages of this technique such as reduced parasitic noise, improved heat dissipation, as well as lowered processing complexity, compared to the conventional wire bonding technology in power module manufacturing. Thermoe-mechanical analysis using thermal cycling test and FEAT were also performed to evaluate the reliability characteristics of this interconnect technique for power devices.

2:45 PM N5.4
AN INVESTIGATION OF LEAD FREE AND BLOMINE FREE TECHNOLOGIES FOR MEDIUM POWER SEMICONDUCTOR PACKAGING. Pamela Dominguez, Pamela Dominguez, Arthur Wolpertman, Integley R&D, International Rectifier GB, Surrey, UNITED KINGDOM.

Over recent years there has been a growing interest in the removal or substitution of Lead, Bromine and other hazardous chemicals from electronic and electrical equipment. This relates primarily to products whose end of life disposal relies on the use of landfill sites or increasingly on recycling. The driving force for these changes come from both legislation, such as that proposed by the European Union, and also from consumer awareness. The implications of the move towards more environmentally friendly electronics extend right down the level of discrete component packages including those produced in hazardous environments. In this paper the technical challenges associated with the development of a lead and bromine free Medium Power Packaging are discussed and the results of ongoing investigations are presented. The major challenges in the development relate not only to the key electrical performance but also to ensuring compatibility with the higher reflow temperatures.
of which may be associated with Pb-free surface mount processing. This raises particular issues with respect to the die attach material, which is often a high-temperature solder. However, the thermal mismatch with the substrate can lead to degradation of the solder joint reliability and possibly the solder joint itself. The choice of solder material and process is critical to ensure reliable long-term performance. The solder material must possess a balance of thermal, mechanical, and chemical properties to withstand the high temperatures and mechanical stresses encountered during the assembly process. Typically, high-temperature solders are used, which have a eutectic composition of SnAgCu or SnCu.

3:30 PM *P5.5
INVESTIGATION OF MECHANICAL STRESSES IN UNDERLIT SOLDER BUMPS VIA SYNCHROTRON X-RAY TOPOGRAPHY AND FINITE ELEMENT ANALYSIS
J. Kupfer, I. Z. Research Institute for Network and Communications Engineering (RINCE), School of Electrical Engineering, Technion, Haifa, ISRAEL; P. M. Chen, University of California, Berkeley, CA, USA;
M. S. S. University of California, Berkeley, CA, USA

Solder problems can significantly impact the reliability and performance of electronic devices. X-ray topography is a powerful imaging technique that can be used to visualize the internal structure of solder joints and identify defects such as voids and cracks. By combining X-ray topography with finite element analysis, researchers can gain a deeper understanding of the mechanical stresses and strains within solder bumps, which are critical for maintaining long-term reliability. This study used synchrotron X-ray topography to investigate the spatial extent of strain fields induced by solder bumps in a high-performance interposer system. The results show that the strain fields are localized near the bump pads, indicating a need for optimization of the solder bump design to reduce stress concentrations and improve reliability.

4:15 PM *P5.5.8
PREDICTION OF LATERAL FORCE-DISPLACEMENT CURVES FOR FLIP CHIP SOLDER JOINTS
T. E. Nelson, K. H. University of California, Berkeley, CA, USA;
M. S. S. University of California, Berkeley, CA, USA

Flip chip technology is gaining popularity due to its advantages in terms of reduced package size, improved heat dissipation, and enhanced electrical performance. However, the reliability of flip chip solder joints is critical to ensure continuous performance over the lifetime of the device. This study presents a predictive model for the lateral force-displacement curves of flip chip solder joints, which can be used to optimize the solder joint design and improve reliability. The model takes into account the effects of process parameters such as solder thickness, bump diameter, and force magnitude on the lateral force-displacement behavior. By using this model, designers can predict the performance of solder joints under different conditions and make informed decisions to improve reliability.
Silane adhesion promoters are seeing increasing use in microelectronic packaging interfaces. For example, they are currently used to adhere the passivating polymer overlayer to oxide, and these materials are being investigated as surface treatments for silicon particles in underfill epoxies. Until recently, the exact mechanism of adhesion promotion was postulated. In this paper, we present detailed studies of silane adhesion promoters on the silicon oxide surface. Two common promoters (aminopropyltriethoxysilane and vinyltriethoxysilane) as well as non-functional silanes are investigated. It was found that without a functional end group, long carbon chain silanes can severely degrade adhesion, resulting in interfaces weaker than silicon is used. Several spin coat solution formulations are used in depositing these films. Resulting surface coverage is examined and quantified with the help of AFM and XPS. Then, the adhesion behavior of various promoter films are tested in sandwich structures using a fracture mechanics approach. Finally, spin coat solution concentration, surface coverage, and interface fracture energy are compared for the same functional promoter.

METAL/POLYMER INTERFACE AND SOLDER JOINT RELIABILITY OF A WAFER LEVEL CSP. H. Han, Jin Yu, K.O. Lee and I.S. Park, Dept. MSE, Center for Electronic Packaging Materials, Korea Advanced Institute of Science and Technology, Taejon, KOREA

As microelectronic devices get smaller and higher I/O densities are required, various chip scale packages (CSP) are adopted, and wafer level chip scale package (WL CSP) combined with flip chip technology has the highest potential. In doing so, it is necessary to redistribute peripheral bond pads and relax the thermal stress in the WL CSP. Here, we use a low modulus polymers as the stress buffer layer (SBL) to relax the thermal stress generated at the solder joint and studied the reliabilities of the metal/SBL interface and solder joint using peel tests and ball shear tests, and effects of the polymer surface pretreatments by the RF plasma and roller metal structure were investigated. Results showed that the adhesion strength of the met al/SBL interface depended on the RF power density and roller metal structure. The peel strength was low for $\rho < 0.27W/cm^2$ but increased up to $\rho = 0.3W/cm^2$ and tended to saturate around 1000 kgf. Then failure locus analyses were conducted using AFM, AES, and XPS. The peeling locus of peel test and the failure locus of roller ball shear test were dependent on the Ni layer in the under bump metallurgy (UBM) and also on the thickness of the roller metal, particularly the thickness of Cu layer. Depending on the met al deposition condition, metal films over SBL were delaminated or buckled due to the residual stress in the metal film, which was measured using the laser curvature method. Additionally, the stress fields and crack initiation and propagation behaviors around the solder joint were analyzed using micro-Moire pattern and the correlated to the process parameters and package structure. Then, implications to the package processes and designs were discussed.
containing pendant allyl ether groups were synthesized from the parent structures. Upon heating, the polymer would undergo an intramolecular rearrangement reaction (Claisen rearrangement), resulting in a Tg enhancement by increasing the number of fused rings via intramolecular hydrogen bonding between the in situ-formed hydroxyl groups and the nitrogen atom of the adjacent benzonitrile group. At elevated temperature (200-300°C), crosslinking of the allyl groups would occur, thus providing a mechanism for insolubility and dimensional stability of the polymer system. Efforts are underway to control the crosslinking density of the polymer system by partial alkylation of the hydroxyl groups attached to the aromatic benzonitriles. We will address several issues relating to integration of these polymeric materials into current processes and how we have tailored our systems, to address issues such as back-etching, adhesion, dimensional stability, and conformal coating of small feature sizes.

10:45 AM *N6.7/L10.7
MOLECULAR INTERACTIONS AND ADHESION FOR INTERFACES RELEVANT TO FLIP-CHIP ASSEMBLIES
Raymond A. Pearson, Lehigh University, Dept. of Materials Sci. & Eng., Bethlehem, PA.

Debonding is a common wear-out mechanism in flip-chip assemblies that utilize organic substrates. The large mismatch of the thermal expansion coefficients of the silicon chip and the organic substrate generates significant stresses during thermal cycling. These thermally induced stresses promote debonding at several interfaces and debonding at the underfill-passivation interface can occur. This paper focuses on developing an understanding between interfacial molecular interactions and adhesive strength in an effort to engineer reliable interfaces. The experimental approach consists of studying the adsorption of model epoxy systems onto polyimide and boroalluminate surfaces using a flow microcalorimeter and separating these interfaces using double cantilever beam specimens. Acid-base theory is utilized to explain the trends in adhesion strength.

11:15 AM *N6.8/L10.8
THERMOMECHANICAL RATCHETING IN INTERCONNECTS.
P. Soh, M. Huang, Mechanical and Aerospace Engineering, Department of Materials Science, Princeton University, Princeton, NJ; Q. Ma and H. Fujimoto, Intel Corporation, Santa Clara, CA; J. He, Intel Corporation, Components Research, Hillsboro, OR.

Temperature cycling has long been used as an accelerated reliability test to qualify new electronic products. Many commonly observed failure modes, however, are not well understood that the extrapolation of the test results to service lifetime is empirical, loosely based on historical records of similar products. This lack of mechanistic understanding is particularly disconcerting when new interconnect materials are being explored. We have initiated a program to study mechanisms of failure modes under temperature cycling. In this talk, we present our recent study on cracking in the Sn film. The Sn film has been widely used as a passivation layer in microelectronic devices. It has been known for over a decade that the Sn film cracks after packaged devices are thermally cycled. While engineering solutions have been proposed on the basis of trial and error, no basic understanding of the cause of the cracking has been identified before. In this talk, we show that the cyclic temperature, coupled with the shear stress at the die corner, causes the interconnect pads underneath the Sn films to undergo plastic ratcheting. Consequently, in the Sn films the stress builds up as the temperature cycles, leading to cracks. We compare the effects of copper and aluminum interconnects. Implications for design rules and qualification tests are discussed.

11:45 AM N6.9/L10.9
DIELECTRIC PROPERTIES OF FERROELECTRIC CERAMIC-POLYMER COMPOSITE FILMS. C.K. Chung, L.P. Sung and J. Obrutz, National Institute of Standards and Technology, Gaithersburg, MD.

The ferroelectric ceramic-polymer composite thin-film is one of important electronic packaging materials. The dielectric constant of a ceramic-polymer composite thin film follows an empirical logarithmic mixing rule when the powder is dispersed uniformly. The low dielectric polymer matrix usually dominates the dielectric constant of the composite. For example, a composite containing 30 volume percent of barium titanate powder in an acrylic polymer shows the dielectric constant about 21 at 1 kHz. This value is much less than that of ceramic powder in the composite. Further increasing the concentration of the filler has only limited effect on the increase of the dielectric constants. We used laser scanning confocal microscopy and optical microscopy to examine the distribution of particles. The thin-slice images of the thickness of the order of one micron and re-constructed 3D image from them allowed us to visualize the relation of micron-size particles and the polymer interface between