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*Invited paper
SESSION D1: ADVANCED MATERIALS AND STRUCTURES
Chair: Tsunenobu Ikeda
Tuesday Morning, April 22, 2003
Golden Gate C2 (Marriott)

NOTE EARLY START

8:00 AM *D1.1
SCALING CHALLENGES FOR SUB-50-nm CMOS TECHNOLOGY, Tohru Mogami, Silicon Systems Research Laboratories, NEC Corporation, Sapporo, Hokkaido, JAPAN.

Scaling challenges are discussed for sub-50-nm CMOS technology to improve the gate delay of CV/1. The basic scaling challenges must be a small channel-length formation, an equivalent oxide thickness (EOT) thickness, oxide contamination (SOX), and the expression of series resistance. 20-nm MOSFETs are necessarily formed by shallow source/drain extensions (SDE) and a steep slope using a high-temperature source/drain implantation (HR-S/D) formation. The steep slope is useful to suppress parasitic resistances. For gate-dielectric, a radical oxidation/nitridation process achieves a low-leakage SiON film with high reliabilities including negative bias temperature instability (NBTI), because of its lower dielectric constant and well-controlled nitrogen profile. All the aggressive scaling challenges should include a high-k gate dielectric film and a small-depletion gate electrode. The high-k dielectric film with a small EOT of 1.1 nm is achieved with zirconium silicate with a compositional gradient and a post-oxidation contamination-free (PAO) process. For a gate electrode, the gate depletion of poly-SiGe is remarkably suppressed by the control of grain size of poly-SiGe. Furthermore, a thin amorphous-Si layer between poly-SiGe and gate-dielectric films is able to improve the breakdown charge (QBD). The metal gate electrode using W/TiN systems suppresses the gate depletion. Furthermore, dual-metal gate CMOS devices with a threshold voltage difference of 0.1 V are demonstrated with nitride control by forming TiN using a nitride-implantation process. In sub-50-nm CMOS devices formed by challenging technologies, the integration technology must be strongly studied, especially for SOc applications.

8:30 AM *D1.2
PROSPECTS AND CHALLENGES FOR ADVANCED GATE-STACK MATERIALS IN SUB-65-nm CMOS TECHNOLOGY, Hisakazu Honma, Tokyo Institute of Technology, Frontier Collaborative Research Center, Yokohama, JAPAN.

Progress of MOS LSIs has been accomplished by the downsizing of its components such as MOSFETs. Now, the gate insulator thinning becomes the most critical issue for the downsizing of MOSFETs. Already 1.4-nm thick oxynitride films have been used for the gate insulator of high-speed microprocessors. However, the large-direct-tunneling leakage current through the gate oxides is a big problem and will limit further downsizing after a few more generations in near future. The leakage through the gate insulator is a more serious problem for low power standby power devices such as cellular phone and thus, introduction of high dielectric constant (high-k) gate insulator is strongly demanded. Among the high-k dielectrics, HfO2 and ZrO2 have been thought to be the most promising candidates because of their predicted good thermal stability and high dielectric constants. In reality, however, these materials have, at this moment, several serious problems, such as i) interfacial layer growth and micro-crystal formation during the thermal process, ii) lower carrier mobility at the high-k silicon interface, iii) higher densities of fixed charge and interface state, iv) boron penetration from the gate electrode during the thermal process, v) contamination of the film from precursor of CVD. Solutions for the above problems are seriously being developed in the world, and some good results have been reported. In addition, migration on other materials such as rare earth oxides is also being done and some good results of La2O3, Pr2O3, Gd2O3 have been also reported. In this paper, current status of the development of the high-k gate dielectrics for advanced CMOS gate insulator is reviewed.

9:00 AM *D1.3
ISSUES IN SELECTING METAL GATE ELECTRODES FOR CMOS APPLICATIONS, Youn Min Kang, Byoun, Yeo-Suck Sa, Jee-Hoon Lee and Jason Gurgurian, Department of Electrical and Computer Engineering, North Carolina State University, Raleigh, NC.

This paper will focus on the material and electrical properties of candidate metal electrodes on SiO2 and high-K dielectrics. In the gate electrode selection process, work function, thermal stability and gate depletion are all critical parameters that need to be satisfied. Although, metal gates have found to exhibit a wide range of work function values (3 eV to 6 eV), obtaining their thermal stability is problematic. The challenge especially lies in finding low work function metals (for NMOS devices), which also offer thermal stability. One option to achieve this is to introduce N and/or Si in metals with low work functions. Another approach is to use metal alloys of low and high work functions. Both these approaches will discuss the possibility of having of appropriate work functions on high-K dielectrics, thermal stability of EOT and VFB and feasible integration schemes including composition control, dual gate integration and dopant diffusion. Candidate metals for PMOS applications will also be discussed.

9:30 AM *D1.4
STACKED METAL LAYERS AS GATE FOR MOSFET: THRESHOLD VOLTAGE CONTROL, Wei Guo and Yoshi Oto, Sharp Labs of America, Camas, WA.

The transition to metal gates and high-k materials for future MOSFETs requires the right choice of materials for achieving the proper threshold voltages for both p- and n-type FETs. This report describes a study on two layer metal gate stacks that allow the effective work function to be tuned by varying the thickness of the first metal layer. MOS capacitors were fabricated using Al on TaN and Pt on TiN metal stacks on thermal oxide and on HfAIO gate dielectric where the TaN and TiN layer thickness is varied over a range from 0 to 100nm. Electrical and thermal stability measurements were performed and are reported. The effective work function is seen to transition from the value of one metal to the other rapidly as the thickness of the first metal layer is varied from 0 to about 10nm. The VFB transition matches the workfunction difference of the two metals in the stack. Both the first and second metal must be stable in contact with gate dielectric and throughout the remainder of the fabrication process. The advantage of this approach is that it allows the effective workfunction of a metal stack, and the VFB of that device to be finely tuned. It also allows for eventual CMOS fabrication where two different workfunction metal stacks are necessary, without processing directly on the gate dielectric.

10:15 AM *D1.5

In this paper, we first review recent trends of MOSFET development, which are an aggressive scaling of gate length, decrease in on-current with scaling, and an increased variety of transistors for a wide range of target products. To satisfy the requirement for the wide range of target products such as high-end MPU, digital AV, mobile, RF application, and so on, transistors used for them must have variations in their characteristics by optional technologies. The variation is classified to speed performance, power consumption in dynamic, standby, RF performance, and so on. In the 65 nm node, both overcomimg issues on aggressive scaling and satisfying requirements of variety of transistors have to be realized by introduction of a new material, a new structure, and a new process in a short development period. In this paper, we show our approach for the first time such as SOL-DMOSFETs, a dynamic threshold operation, a metal gate-oxide structure, a high-k gate insulator, and a laser annealing process. These new technologies should be properly used from the point of required performance and cost. For example, we developed SOL-DMOSFETs with a metallic overlying gate for one-chip integration of RF/digital ICs for wireless systems and high-speed data communication systems. The transistor has an fmax of 185 GHz, which is forecasted by ITRS as a 200 nm node technology. In addition, a very low noise figure properties have also been obtained. The minimum noise figure is less than 1dB. This value is competitive to GaAs low-noise HEMT one.

10:45 AM *D1.6
EVOLUTION OF THE SOL MOSFET: FROM SINGLE GATE TO MULTIPLE GATES, Jean-Pierre Colinge, Dept. of Electrical and Computer Engineering, University of California, Davis, CA.

During the last 20 years Silicon-on-Insulator (SOI) MOSFETs have evolved from the partially depleted structure inherited from SOS technology into fully depleted devices which are more adapted to high-performance, low-voltage applications. Standard SOI MOSFETs essentially mimic bulk devices and suffer from similar problems when decimeter gate lengths are reached. These problems are usually referred to as 'short-channel' effects and include DHB threshold slope degradation. These effects are caused by the two-dimensional encroachment of drain electric field lines on the channel region. Classically these effects are minimized using engineered doping profiles in the channel region, such as the formation of HALOS. Fully depleted SOI MOSFETs offer another way of reorganizing the current distribution across the channel region by the gate and reduce the influence of drain field lines from the drain: the use of double and triple gate device structures. The scaling benefits of the double-gate device have been extensively studied as early as 1984, and the first report came in 1987. Despite of several proposed embodiments and the fabrication of
11:15 AM D17
A TECHNIQUE FOR SOURCE/DRAIN ELEVATION USING IMPACTATION MEDDIATED SELECTIVE ETCHING, M.Q. Huda and K. S. Sakthivel.
Electronics Research Institute, National Institute of Advanced Industrial Science and Technology, Tsukuba, JAPAN.

A process involving implantation mediated selective etching has been developed for Source/Drain elevation of CMOS devices. Our approach relies on the formation of elevated Source/Drain by non-selective growth of silicon through conventional Low Pressure Chemical Vapor Deposition (LPCVD). Etching in low density SiO$_2$ sidewalls would then be removed by selective etching in a solution of HF/HNO$_3$/CH$_3$COOH. A silicon layer of 100 nm thickness was formed on a sample with Si/SiO$_2$ structure by LPCVD at 700°C. As grown poly-silicon layer formed on the oxide region showed a small rate of etching similar to that of the elevated epilayer silicon. Samples were then implanted with Argon at 140 keV with a dose of 2x10$^14$/cm$^2$. Implantation orientation was aligned in the vertical $<100>$ direction to knock down damage in the elevated silicon region in a minimum level. A short annealing at 420°C was sufficient for damage recovery of the epitaxial silicon. The damage in poly-silicon layer, on the other hand, showed only a small recovery by the same annealing. The implanted silicon layer and silicon showed etching rates of 20 nm/min and 1 nm/min respectively. The selectivity over an order of magnitude was used to etch the polycrystalline layers, leaving the elevated silicon region unaffected. Pattern edges, representing the gate sidewalls in actual devices, showed no sign of residual poly-silicon. The sidewall material SiO$_2$, subjected to the implantation and annealing step, was found to work as an etch-stop with etching rate of 6 mm/min. Much smaller etching rate of 0.5 mm/min was observed for Si$_3$N$_4$ under similar processing conditions. Our approach of silicon elevation does not depend on inclusion/sidewall materials, and is not bound by thickness limits, or etching effects.

11:30 AM D18
STUDY OF USING ELEMENTS FROM GROUP II AS BARRIERS FOR DOPANT PENETRATION INTO GATE DIELECTRICS AND GETTERS FOR METALLIC ION CONTAMINATION, Grace San Vladimir Zuhkov, Sheldon Aronowitz, LSI Logic Corp., Milpitas, CA; Margaret A. Gabriel, Department of Chemistry, University of Washington, Seattle, WA.

Various chemical and mechanical processes may introduce contamination, such as metallic ions, during the creation of an integrated circuit. Dopant degradation and current density leakage. In addition to externally introduced charged species, during annual cycles dopants such as boron can penetrate the silicon substrate from a highly doped poly-silicon gate; this penetration also will cause progressive destructive first principal. Furthermore, calculations using periodic boundary conditions and cluster approximations to search for a novel material that can attract or trap ions and fast diffusing dopant species to reduce or eliminate such problems. Experiments on different metalions interactions with other ions in silicon dioxide was conducted. Strong metal ion interactions to calcium are calculated. Ion attraction to strontium are also found, but the magnitudes are less and, in several cases, even repulsive. Both calcium and strontium attract neutral boron with the stronger attraction found with calcium. Calcium interaction with boron in other dielectric materials was also studied. Attraction was predicted to occur between calcium and boron whether they were distributed in the structure, or were isolated in a field, both metalization, for example. This study leads us to propose incorporation of calcium into critical dielectric layers as a promising material to trap ions and reduce boron penetration through the gate oxide. Compared to existing boron penetration barriers, calcium has several advantages. In this talk, results of our theoretical investigation along with experimental work will be presented.

11:45 AM D19
CREATION OF A NEW CLASS OF SEMICONDUCTOR MEMORY DEVICES GUIDED BY QUANTUM MECHANICAL MODELING, Stefan A. Kossert, Daniel Zuhkov, Greg Sprinkle, Milpitas, CA; Mehmet C. Ozuruk, Yves Jin, Lin, Department of Electrical and Computer Engineering, North Carolina State University, Raleigh, NC.

A new class of semiconductor memory devices is proposed. The class is a product of quantum mechanical calculations that predicted non-zero electron affinities when zincirconium was inserted into a representative structure of silicon dioxide. The zirconium rich region exhibited an electron affinity between 1.7 and 1.9 eV in the simple silicon dioxide models further, the region where excess zirconium is incorporated into silicon dioxide will function as charge storage centers. More elaborate calculations were performed on crystallized using periodic boundary conditions with density functional theory. Transition metal or non-transport metal elements were inserted into the center of a ring and the entire structure then was allowed to relax. It was found that the inserted elements tended to remain in their original positions. Interestingly, the depth of the electron trapping well, if formed, was found to be unique to each element. An existing memory device class, which utilizes states created at the interface between two different dielectric materials such as SiO$_2$ and silicon dioxide, superficially resembles the new one. However, these two classes are fundamentally different. The properties of the new class result from intrinsic electronic interactions between the transition metal with its immediate silicon dioxide environment, for example, and not because of mismatched or dangling bond at the boundary of two materials. The talk will include extensions to other systems, such as amorphous hafnium oxide by itself, and to experimental investigations.

SESSION D2: HIGH-k DIELECTRICS
Chair: Tatjana Mijovic
Tuesday Afternoon, April 22, 2003
Golden Gate C2 (Marriott)

1:30 PM D2.1
IMPACT OF NEW MATERIALS AND TRANSISTOR ARCHITECTURES ON SCALED CMOS FOR MIXED-SIGNAL APPLICATIONS, Yoichi Yamayama, Philips Research Leuven, BELGIUM.

The introduction of both new materials (high-k gate dielectrics, metal gate electrodes, mobility-enhancing materials in the channel, such as strained silicon or SiGe) and alternative transistor architectures (FD-SOI and multigate transistors (FinFET, Double Gate, SON, etc.) into 45nm and smaller CMOS nodes is inevitable. It is quite clear that historical trend of yearly improvement of transistor performance by 17% will be impossible to sustain without it. The driving force of these changes is naturally coming from the necessity to aggressively scale CMOS for digital applications (both logic and memories). However, this will entail significant consequences to the operation of new parts of the IC, which might be either beneficial or detrimental, depending on the application block. In this paper we will review these effects, with special emphasis on analogue/BF parts of the circuitry used for mixed-signal applications. We will show that early feedback loop between new materials and transistor architectures on one side and application domains on the other is of vital importance to ensure future SOC success.

2:00 PM D2.2
IMPACT OF GATE PROCESS TECHNOLOGY ON EOT OF HfO$_2$ GATE DIELECTRIC, Daewon Ha, Qing Li, Hiko Takeuchi, Tzu-Jue King, Department of Electrical Engineering and Computer Science, University of California at Berkeley, Berkeley, CA; Tae Kang Oh, Young Hee Kim, Jack C. Lee, Department of Electrical and Computer Engineering, University of Texas, Austin, TX.

HfO$_2$ is one of the most promising candidates to replace SiO$_2$ as the gate dielectric because of its high permittivity, thermodynamic stability, and large energy-bandgap offset to Si. For simplicity of process integration, polycrystalline silicon (poly-Si) is preferred as a gate electrode material. However, the growth of an interfacial layer at the surface of the silicon upon high-temperature annealing (e.g. used for source/drain formation) increases the equivalent oxide thickness (EOT) and gate leakage current [1]. Polycrystalline silicon-germanium (poly-SiGe) has been received much attention as an alternative gate-electrode material, because it alleviates gate depletion and boron penetration issues [2]. Recently, it was reported that the use of poly-SiGe results in thinner EOT for HfO$_2$ gate dielectric [3]. In this paper, we investigate the mechanism responsible for this effect. Using MOS capacitors, the effect of the gate material and gate deposition rate on interfacial layer formation is studied. A conventional LPCVD furnace was used to deposit the gate materials (poly-Si and poly-Si$_3$N$_4$) at 550°C onto PVD HfO$_2$ gate dielectric. The effect of gate deposition rate was studied by comparing the results for poly-Si deposited using SiH$_4$ against those for poly-Si deposited using SiH$_4$ and Si$_2$H$_6$. The deposition rate for poly-Si using Si$_2$H$_6$ is about 8 times faster than that for poly-Si using SiH$_4$. The deposition rate for Si$_3$N$_4$ is about 7 times faster than that for poly-Si using SiH$_4$. Interfacial layer thicknesses are evaluated by cross-section transmission electron microscopy (TEM) and capacitance measurements. Initial results indicate that poly-Si$_3$N$_4$ gate provides the highest insulation capacitance ($C_{ox}$), while the Si$_2$H$_6$-doped poly-Si gate provides the lowest insulation capacitance. TEM analysis elucidates differences in the thickness of
the interfacial layer between the HfO$_2$ and silicon substrate. The dependence of interfacial layer thickness and gate leakage current on annealing temperature for each gate dielectric will be presented. [1] L. Kung et al., JEDM Technical Digest, pp. 35-38, 2000.

2:15 PM D2.3
ANALYSIS OF INTERFACIAL DIFFUSION BETWEEN HIGH-K DIELECTRICS AND SILICON SUBSTRATE USING MOLECULAR-DYNAMICS TECHNIQUE. Tomio Iwashiki and Hideo Murra, Mechanical Engineering Research Laboratory, Hitsuji, Ltd., Tsukuba, JAPAN.

The problem of interfacial-layer formation between high-k gate dielectrics and a Si substrate is one of the major problems to be solved in order to obtain future devices that have gates with sub-nm equivalent oxide thickness (EOT). Interfacial oxygen diffusion from high-k gate dielectrics into a Si substrate at high temperatures is considered to be a dominant factor in the interfacial-layer formation. To find effective methods for suppressing the interfacial diffusion, we have developed a molecular-dynmics technique for analyzing the atomic diffusion at different-material interfaces. Because this technique uses the extended Tersoff potential that can cope with charge transfer between different elements, we can analyze the atomic diffusion at dielectric/semiconductor interfaces as well as at metal/semiconductor/silicon, dielectric/dielectric interfaces. To suppress the formation of a lower-k interfacial layer, this technique is applied to the modeling of the formation of the interfacial oxygen diffusion from high-k gate dielectrics (ZrO$_2$ and HfO$_2$) into a Si substrate. The analysis results showed that the interfacial oxygen diffusion is suppressed when Ti atoms are positioned in the ZrO$_2$ and HfO$_2$ films. It was also shown that the oxygen diffusion in ZrO$_2$/Si(111) and HfO$_2$/Si(111) interfaces is much more suppressed than that in the ZrO$_2$/Si[001] and HfO$_2$/Si[001] interfaces. Thus, the addition of Ti and the use of Si[111] substrates instead of Si[001] substrates are effective methods for suppressing the interfacial-layer formation. The effectiveness of these methods was confirmed by transmission electron microscopy (TEM). We then conclude that the molecular dynamics technique is useful in finding effective methods for suppressing the interfacial-layer formation between high-k gate dielectrics and a Si substrate.

2:30 PM D2.4
INTERFACE-ATOMIC STRUCTURE AND BAND OFFSETS AT HIGH K OXIDE-Si INTERFACES. J. Robertson, P.W. Peacock, Engineering Dept, Cambridge University, Cambridge, UNITED KINGDOM.

High dielectric constant oxides are needed to replace silicon dioxide as the gate oxide in future CMOS devices. The band offsets should exceed IV to inhibit leakage currents. The atomic structure and band offset between these two materials are critical to forming high-k dielectrics. ZrO$_2$ and SiO$_2$, and Si$_3$N$_4$ and SiO$_2$, have been modeled. The electronic structure and band offsets have been calculated. Atomic models of the epitaxial interfaces Si/ZrO$_2$[100], Si/ZrO$_2$[111], Si/ReO$_2$[100], Si/ReO$_2$[111], and Si/Si$_3$N$_4$[100] and [111] are examined. In the oxides, the bonds across the interface must satisfy more conditions to give charge neutrality and an absence of interface states, than for the simpler case of the Si/Si$_3$N$_4$ interface. The total energy of the interface is found to compare these the differences. It is found that changing the termination oxide can vary the band offset by 0.5 eV, compared to those previously predicted by matching bulk change neutrality levels [1]. [1] J. Robertson, J Vac Sci Technol B 18 1785 (2000).

2:45 PM D2.5
LAYERED TUNNEL BARRIERS USING HIGH DIELECTRIC CONSTANT MATERIALS. Julie D. Casper*, L. Douglas Bell*, Brett W. Bush*, Man Yee He*, Martin L. Green*, Harry A. Atwater*; "California Institute of Technology, Watson Laboratory of Applied Physics, Pasadena, CA; Jet Propulsion Laboratory, Pasadena, CA; Agere Systems, Murray Hill, NJ.

We have modeled and fabricated the layered dielectric barrier structures that address the main performance limitations of floating gate nonvolatile memory devices, such as flash memories and nanocrystal memories, namely the long program time (~1 ms) and erase time (~1 ms) achievable via a Fowler-Nordheim tunneling mechanism for charging the floating gate through a homogeneous tunnel barrier. Silicon compatible layered barrier architectures that enable a large drop in the barrier height with applied voltage are an alternative to homogeneous dielectric films as the tunnel barriers for nonvolatile memories. Such voltage-depended barrier lowering in layered heterostructures is also a basic principle for new class of electrically tunable photodetectors. Using a numerical effect-reverse model, we have been able to optimize and analyze possible layered structures with real materials parameters. Recent device construction work has confirmed simulation that some of the most promising structures for layered tunnel barriers consist of Al$_2$O$_3$ with Si$_3$N$_4$ or HfO$_2$ and we have fabricated such structures. The Si$_3$N$_4$ was made by low-pressure chemical vapor deposition, while the Al$_2$O$_3$ and HfO$_2$ were made by atomic layer deposition. We have fabricated the layered barrier structures Si$_3$N$_4$/Al$_2$O$_3$/Si$_3$N$_4$ and HfO$_2$/Al$_2$O$_3$/HfO$_2$ as well as single- and double-layered structures using these materials. One of the most promising results is the formation of n-Si/Al$_2$O$_3$/Si$_3$N$_4$ and n-Si/HfO$_2$/Si$_3$N$_4$. We find significant asymmetry in the two-layer measurement, an indication of how the nature of the tunneling barrier will influence the conduction. Experiments involving metal-insulator-semiconductor diodes with semi-transparent gates are underway in order to directly measure the band offsets of our dielectric materials, using a chopped tunable laser as light source for illumination. These measurements give us a better understanding of the electrical properties of the heterostructures.

3:15 PM D2.6

Among the metal oxides with high electrical permittivity (high-k) that are currently considered as candidates to replace SiO$_2$ as gate dielectrics, the oxides based on HfO$_2$, TiO$_2$, and Ta$_2$O$_5$ are the most favored ones. Two of the most important deposition techniques to fabricate thin layers of these materials are Atomic Layer Chemical Vapor Deposition (AL-CVD) and Metal-organic CVD (MOCVD). In this presentation, we will compare several aspects of these techniques and the materials deposited as a function of their suitability for gate dielectrics for both low power and high performance applications. First, we will briefly describe the two deposition techniques and the most important differences and similarities. We will discuss some typical growth characteristics, and the importance of these characteristics for the resulting quality of the film. The success of both techniques for this application is heavily depending on the starting surface; this will be illustrated for a number of different surface pre-treatments. The resulting interfacial layer (IL) behaves quite differently for both techniques, as will be shown. Also the stability of this IL during further thermal processing can become an issue. Next, the characteristics of the bulk of both types of films can be very different, such as the density of the films, the surface roughness and the presence of defects. On the other hand, there are also striking similarities such as the k values as they are evaluated from CV measurements on capacitors fabricated on p-type Si(100) with oxide thickness for the AL-CVD oxides is strongly dependent on the type of electrode layer and needs special attention. Whereas the principle of the approach to cope with this interaction is very similar in both cases, the practical way to solve the problem can be quite different. Generally, we will compare some of the pros and cons for low power and for high performance applications.

3:45 PM D2.7

Because of aggressive downscaling to increase device performance, the physical thickness of the SiO$_2$ gate dielectric is rapidly approaching the limit where it will only consist out of a few atomic layers resulting in very high leakage currents due to direct tunneling. To allow further scaling, materials with a k-value higher than SiO$_2$ are explored, the so-called high-k materials, such that the thickness of the dielectric can be increased without degrading performance. For the moment, the only candidates are the Hafnium-based materials HfSiOx and HfAlO$_x$. The present work discusses the potential of MOCVD-deposited HfO$_2$ to scale to 1- and sub-1nm EOTs, where we will focus on the issues that complicate downscaling the HfO$_2$ stack and try to find possible solutions. It is suspected that alterations from the ideal gate stack Si/HfO$_2$/polySi will result in an increased EOT. Hence, a primary concern is the interfacial layer that is formed during the MOCVD deposition process between the Si and the HfO$_2$ for both Hafnium and SiO$_2$ like starting surfaces. This interface will contribute to the EOT reducing...
The continuous scaling down of transistor and memory devices toward 65 nm technology node demands for the replacing of ultra thin SiO2 based gate oxides with high k gate dielectrics. In this study, the incorporation of physical-chemical stability of Al2O3-H2O alloys upon prolonged post-deposition annealings (PDA) is presented. Two different high k-aluminates were analyzed, containing 33% and 75% Al2O3 mol% respectively. Amorphous films were deposited on RCA treated p-type silicon by ALDVTM. Post-deposition annealings were carried out in O2 or N2 atmosphere, at 850°C and 900°C for 30 minutes. Interfacial layer (IL) increase after PDA was detected on all the samples. No impact of annealing temperature was observed on Al2O3/Hflo layer, while sensitive effect was noticed on Hf-rich material. N2 and O2 annealings resulted in limited IL differences, suggesting that these films were not completely permeable to oxygen diffusion. XRD and planar TEM-STEM analyses evidenced first phase separation and then, in the case of Hf-rich samples, crystalization phenomena occurring at HfO2 cluster sites. Differently from HfO2, this alloy crystallized mainly in tetragonal phase with some specific features depending on annealing medium. Such composition was characterized by means of XRD, microRaman, XRF. Growth of interface layer was justified by limited oxygen incorporation from external ambient. Silicon diffusion from the substrate into high-k material and aluminum/hafnium redistribution were observed and associated to annealing temperature. Finally, Hf-aluminates were electrically characterized by means of C-V and I-V measurements on basic capacitors. Variations in material electrical properties were found consistent with change in physical-chemical film structure.

Overall, Hf-aluminates were found to remain amorphous during high temperature prolonged treatments up to 900°C for 75% and 850°C for 35% alloys respectively. The measured high k films, silicon and metals inter-diffusion was observed at these conditions, but with no relevant physical differences and lower impact on electrical properties compared to Al2O3 and HfO2.

As the continued scaling of Si CMOS devices approaches its fundamental limits, alternative semiconductor materials, such as Ge, with high intrinsic carrier mobility are increasingly promising for use in the channel region of field effect transistors. However, in the case of a high k-dielectric, the lack of a semiconducting stable layer (e.g. SiC or TCO) can hinder the formation of a good quality gate dielectric. Recently, deposited high-k dielectric materials prepared on Si by methods such as ALD (Atomic Layer Deposition) have demonstrated excellent film quality and dielectric characteristics.

In this presentation, we compare the microstructural and electrical properties of ZrO2 films grown by the ALD technique on Si and Ge substrates with different surface cleaning/passivation methods. A cold wall ALD system with Zr precursor was used and the deposition was carried out at 300°C. ZrO2 microstructures on different substrates were investigated using HR-TEM imaging and electron diffraction. Several compositional analyses were performed using AlB-EXPS and the electrical properties such as C-V and I-V characteristics were compared using Pt gate capacitor structures fabricated through a shadow mask process. High-k dielectric deposition by ALD often occurs readily on hydroxydized surfaces such as chemical SiO2 or a hydroxylated oxidized glass. Deposition process, high k dielectric preparation on Si surfaces usually result in the uncontrolled and uncontrollable formation of a thin interfacial oxide layer if the Si is not already passivated by a layer prior to deposition. However, in contrast to results on Si substrates, ALD deposition of ZrO2 film on a Ge (100) substrate showed local epitaxial growth without a distinct interfacial layer unlike ZrO2 on SiO2/Si. Due to the large lattice mismatch (~10%) between ZrO2 and Ge, a significant areal density of interfacial dislocations was seen. The influence of the dislocations in the gate dielectric on the MOS characteristics will be discussed at the presentation.

**SESSION D3: POSTER SESSION**

**ADVANCED GATE STACK MATERIALS**

Chair: Hiroshi Fujimura and Robert J.P. Lander

Tuesday, April 22, 2003

8:00 PM

Salon 1-7 (Metropolitan)

D3.1

A NEW PARAMETER OF PREDICATING GM FOR ULTRA THIN NITRIDED GATE OXIDE

Mitsuki Horii1, Naoyoshi Tanahara2, Matsuji Kase3, Hiroko Sakuma4, Hirofumi Obata5, Masumi Shiratori1, Yuzuru Kato1

1Fujitsu, 2Fujitsu Labs., Tokyo, JAPAN.
The application of nitrided oxide gate dielectric continuously has been used, because of its high performance CMOSFET technology. It exhibits a high transconductance of channel carrier, i.e., Gm. Also the understanding of Si/dielectric interface for improving the characteristics of base layer of high-k material is highly demanded. Many methods of nitridation technique were presented and influenced strongly. Previous works indicated that Gm may depend on the nitrogen concentration at the Si/dielectric interface analyzed by SIMS or XPS in the thickness range up to 2.0 nm. Presently the physical thickness is scaled down below 1.1 nm from high performance transistors, then to solve relationship of Gm and nitridation require immediate attention. We proposed new parameter of predicting Gm for ultra thin nitrided gate oxide. We made MOSFET with some variant ultra thin nitrided gate oxide about the physical thickness of 1.1 nm with the base oxide thickness of 0.85 nm, using the Fujitsu state-of-art 90 nm generation CMOS technology of 1.8=0.3μm transistor, and we investigated these Gm. Also, we analyzed the dielectrics by XPS, and estimated the nitrided structure of SiN4 structure accurately. When we observed a good correlation that the ratio of SiN4 structure in SiN3 rather than the amount of nitrogen at Si/dielectric interface.

D3.2 TRISILYLAMINE: A C & Cl-Free SOLUTION FOR LOW TEMPERATURE SILICON NITRIDE CHEMICAL VAPOR DEPOSITION

Christian Duanas, Jean-Mar Girerd, Takanori Kimura, Air Liquide Laboratories, Tsukuba, Ibaraki, JAPAN; Naoki Tanimoto and Yuuuke Satow, Corporate Research & Development Center, Toshiba Corporation, Kawasaki, JAPAN.

With the shrinking of the critical dimension in semiconductor devices towards 100 nm in a near future, the need to maintain sharp dopant concentration profiles throughout the complete chip manufacturing cycle is becoming more critical. In the nitridation of SiN, the nitriding process is a key route for the post-implantation process steps. When performed with a dichlorosilane-ammonia (DCS-NH3) chemistry, the low pressure chemical vapor deposition (LPCVD) of SiN4 is one of the most budget-friendly process since a temperature in the 720-800°C range is required to achieve a sufficient deposition rate. Recently, two new low temperature silicon nitride precursors have been proposed to address this issue, namely hexachlorosilane (HCS) and BITAS. On one hand, HCS yields high quality SiN4 films at low temperature but its results, as for DCS, is the generation of solid byproducts depositing in the exhaust line. Moreover, up to percent level chlorine is incorporated as the deposition temperature is reduced. On the other hand, if BITAS has the advantage of being chlorine-free, it tends to incorporates high carbon and hydrogen levels. Trisilanylamine (TSA, [SiH3]N) has been evaluated to optimize the film properties and deposition kinetics, taking into account several advantages of this precursor: chlorine and carbon-free, direct Si-N bond in the molecule; stable, and therefore convenient to use; very volatile. The LPCVD of silicon nitride was achieved at low temperature (between 550 and 700°C) using TSA. Silicon nitride films deposited with TSA and ammonia showed excellent conformal step coverage. As a result of the chemical composition of TSA, these films were also free of chlorine and carbon contamination. The hydrogen concentration in the films, a critical feature related to boron diffusion from the substrate, is as low as the standard silicon nitride processes.

D3.3 MODELING INHERENT ELECTRON TRAPPING PROPERTIES OF HIGH-K DIELECTRIC MATERIALS: Vladimir Zubkov, Grace Sun, Sheldon Aronowitz, LSI Logic, Milpitas, CA, Margaret A. Gabriel, Department of Chemistry, University of Washington, Seattle, WA.

It has been reported that the well-known high-k dielectric aluminum oxide and hafnium oxide exhibit trapping probabilities that are orders of magnitude higher than that of silicon oxide. This trapping behavior will reduce the acceptable lifetime operation of devices constructed with these dielectric materials or might lead to catastrophic threshold shifts for very sensitive applications. There are at least three possible reasons for electron trapping in these dielectrics: grain boundaries intrinsic to polycrystalline materials, defects in the bulk and at the surface, and inherent bulk electronic properties of these dielectrics. The inherent bulk properties are especially important in other factors can be decreased by surface passivation and appropriate surface treatment. Understanding and evaluating intrinsic trapping properties is important as it may be used for predicting trapping properties of currently considered high-k dielectrics as well as those that are proposed for future generations. In this work, electron affinity (EA) is employed as a measure of electron trapping capability of considered dielectrics. Values of electron affinity have been estimated for two kinds of dielectric bulk models: models with periodic boundary conditions (PBC) and models that have been considered within the framework of density functional theory. In agreement with experiment, calculations reveal no EA for both crystalline and amorphous silicon oxide. In the case of hafnium oxide noticeable EA has been calculated for the amorphous phase; some EA values have been calculated for crystalline phase. Estimated EA values are also reported for various metal silicates and some dielectrics containing oxynitrides in combination with transition metal. The relationship between the electronic structure of dielectrics and their inherent electron affinity has been explored.

D3.4 KINETICS OF CHARGE GENERATION DURING FORMATION OF High Zr SILICATE DIELECTRICS: Theodosios Gougoussis and G.N. Parsons, Dept of Chemical Engineering, NC State University, Raleigh, NC.

Understanding charged defects in high-dielectric constant insulators is a critical challenge for advanced devices. We have formed thin Zr and Hf silicates by sputtering and examined the effect of formation time and temperature on the band voltage from capacitance vs. voltage. Films were formed by depositing thin metal oxynitrides on N-type silicon and oxidizing in N2O at 600 or 900°C, and the resulting equivalent oxide thickness (EOT) ranges from 12 to 30 Å. We find that the thermal budget during oxidation and the type of oxidizing agent significantly affect the amount of fixed charge in the film. Oxidation of Zr metal on Si at 600°C for 15s results in EOT=12Å and a shift in the band voltage by ~0.1V indicating generation of positive fixed charge. For Zr and Hf films longer oxidations in N2O (up to 310k, with an increase in EOT) show an increase in fixed charge. Direct comparison of Si oxidized in the same environment does not show this extent of band voltage shift. A significantly reduced charge generation rate is observed for Hf oxidation under low O2 partial pressure. Extended oxidation (up to 310k) showed minimal increase in EOT (14 Å increased to ~15Å) with a slight decrease in the charged defect state density. X-ray photoelectron spectroscopy indicates formation of HfO2, however the charge generation process results in less silicon incorporation in the film as compared to films oxidized in N2O. Post metal anvil (PMA) results in partial neutralization of the charge. PMA after the Al gate deposition also leads significant decrease in the EOT (from 27 to 21Å) indicating significant reaction of the film with the gate metal. Results suggest that understanding oxidation mechanisms will be important in isolating and controlling fixed charge in high-k dielectrics.

D3.5 ATOMIC SIMULATIONS OF SURFACE CHEMICAL REACTIONS FOR GROWING HIGH K GATE STACKS

Charles Moraillere, Yasunori Watanabe, Joseph Han, Dept of Chemical Engineering, Stanford University, Stanford, CA.

We have used density functional theory to predict the stoichiometric mechanisms and associated kinetics of atomic layer deposition processes to deposit several materials [ZrO2, HfO2, and Hf and Zr silicates] for high-k gate stacks. These processes had not previously been investigated theoretically and our results lead to insights into the details of the process and an explanation of several unanswered questions regarding the deposition rates and their dependence on the environment. An example is the reaction of Zr silicate oxide formation. Native oxide growth on bare silicon is enhanced in the presence of oxygen. The reaction is also enhanced by using ellipsometry. Zirconium dioxide film (~20 Å) is deposited on the etched substrate by electron beam evaporation and subsequently annealed in hydrogen. MOS Capacitor devices are fabricated by depositing metal electrodes on these specimens. Two important parameters that dictate the characteristics of the combination of the cleaning schemes are defined: residual thickness after etching and re-growth rate. From the monitoring of residual oxide after final etching and subsequent re-growth, we found that the maximum difference between conventional RCA cleaning and the new cleaning method after 1 hour is more than 0.16 mm, which is significant for devices demanding equivalent oxide thickness of <2 nm. Degree of hydrogen penetration within monolayer thickness is strongly influenced by the metal removal capability are considered to be the main factors that explain
the differences between the cleaning methods. Data derived from C-V analysis verify the trends resulted by the native oxide thickness measurements of more than 95% in capacitance is observed in the samples treated by the new cleaning method.

D3.7 HIGH QUALITY THIN HfO₂ FILMS DEPOSITED VIA ALTERNATING PULSES OF Hf(NO₃)₄ AND HCl₂, J. F. Conley, Jr. and Y. Ono, Sharp Labs of America, Norcross, GA; R. S. Inoki, Oregon Graduate Institute, Department of Electrical and Computer Engineering, Beaverton, OR.

The most widely used precursor for ALD of HfO₂ is HCl₂ with H₂O as the oxidant. A major drawback of using HCl₂ as a H₂O as the oxidant. A major drawback of using HCl₂ as the oxidant is that it does not allow uniform initiation of deposition directly on H-terminated Si. Because several initial monolayers of SiO₂ are required to achieve deposition of uniform HfO₂ films, it will be difficult to achieve equivalent oxide thicknesses on different substrates using HCl₂ as the oxidant. A novel technique for deposition of HfO₂ that consists of alternating pulses using a combination of two hafnium containing precursors (Hf(NO₃)₄ and HCl₂) with N₂ purges between the pulses. An in-situ 400°C post deposition anneal density and improves the film. H₂O is not used, instead, Hf(NO₃)₄ serves as the oxidant. It was found that this method allows deposition of high quality HfO₂ films directly on H-terminated Si, without any “mating” cycles. The thickness of the resulting films is linearly dependent on the number of cycles (each cycle consists of Hf(NO₃)₄/N₂/HCl₂/N₂). A high deposition rate of approximately ~0.7 nm/cycle was obtained, greater than that for either precursor used individually with H₂O. The deposition rate is independent of temperature over the range of ~15°C-20°C. HfO₂ films were also characterized using spectroscopic ellipsometry (SE), X-ray diffraction (XRD), and X-ray reflectivity. Electrical measurements capacitors on with sputtered TiN gates indicate promising electrical characteristics.

D3.8 ALD OF HfO₂ FROM TETRAKIS(ETHYLHYDRAZOLINO) HAFNIUM (TEHMA) AND TETRAKIS(DIMETHYLMAMINO) HAFNIUM (TDMAH) AND OZONE. Xinyu Liu, Anh Londergan, Anurajan Srivastava, Stefano Russo, Jerry Winkler, Shannon Ramamurthy, Eddie Lee, and Tom Seidel, Genus, Inc., Sunnyvale, CA.

Hafnium oxide (HfO₂) thin films were synthesized from tetraakis(dimethylamino) hafnium (TEHMA) and ozone (O₃) by atomic layer deposition (ALD) on 300 mm silicon wafers. Non-ideal saturation was observed for TEHMA. However, O₃ showed very good saturation behavior within the range that was studied, which indicates that O₃ is a good ALD reactant in combination with TEHMA. Within wafer non-uniformity (WFNU) of less than 1% was achieved. 100% step coverage was achieved for ~100 nm thick HfO₂ films with a step ratio of 3 to 4. Film thickness increased linearly with number of cycles. Temperature dependence of deposition rate was studied as a function of temperature from 100°C to 425°C. Lowest deposition rate and highest refractive index of films was observed at 300°C. Oxygen and hydrogen content decreased as the temperature increased from 100°C to 320°C. Films made with H₂O had lower carbon and hydrogen levels than films made with O₃. The difference of impurity level between O₃ based films and H₂O based films decreased as temperature increased. Mercury probe measured dielectric constant increased from 20 to 420 μm at 320°C. Mechanism of O₃ based ALD process was discussed. Selected comparisons with tetraakis(dimethylamino) hafnium (TDMAH) were also made. Our experiments show that O₃ based ALD HfO₂ deposition with these precursors is promising for advanced capacitor mass production.

D3.9 ATOMIC LAYER DEPOSITION OF HAFNIUM OXIDE USING METAL ORGANIC PRECURSORS AND OZONE. Yoshihide Senezaki, S. G. Park, Randall Higuchi, Eugene S. Lopata, S. Lee, and Aubrey Helms Jr., ASMl, Thermal Division, Scotts Valley, CA.

The need for high-k gate dielectrics with CMOS integration was identified in the International Technology Roadmap for Semiconductors (ITRS). Conventional SiO₂ gate dielectrics are limited below 200 nm due to the increase of gate leakage current. For integration of high-k gate dielectrics, the gate leakage current is in below 10⁻¹⁰ A/cm². high-k dielectrics having stability with Si gate are needed at the 65 nm node. HfO₂ has been extensively studied as a promising high-k candidate and its high performance due to its high permittivity, good thermal stability and large band offset to Si. Charge trapping related to Vt (threshold voltage) instability and electron mobility degradation in MOSFET performance. To improve the performance of high-k dielectrics, a high-k dielectrics, one of the sources for the fixed and trapped charge is OH⁻, a prevailing impurity in H₂O-based high-k dielectric, which can be eliminated by using ozone as an oxidant in lieu of H₂O. We have developed processes to deposit hafnium oxide film using atomic layer deposition (ALD) with metal-organic precursors and using ozone as an oxidant source. The hafnium precursors used in this study are volatile liquids. A comparison was made in film quality and deposited performance among the precursors. The use of ozone allows ALD processes at temperatures below 300°C and provides HfO₂ thin films with good electrical properties.

D3.10 EVALUATION OF TETRAKIS(DIETHYLAMINO)HAFNIUM PRECURSOR IN THE FORMATION OF HAFNIUM OXIDE FILMS USING ATOMIC LAYER DEPOSITION. Ronald Immne, Amil Despande, and Gregory Jursich, American Air Liquide, Countryside, IL.

Due to their thermodynamic compatibility with silicon interface and high dielectric constant, hafnium oxide is considered as a potential candidate for replacing SiO₂ in the future. However, the major challenge remains the deposition of hafnium oxide at low temperatures to avoid high-κ dielectrics and consuming strong candidates in replacing Silicon oxide nitrate as the gate dielectric layer in CMOS devices. To achieve ultimate conformity and thickness control, atomic layer deposition (ALD) using high-κ dielectrics is receiving much more attention in recent years for nanometer size film applications. For hafnium oxide deposition by ALD, metal chlorides have traditionally been used as precursors with moisture being the co-reactant; however, for gate oxide application, metal chlorides are not considered suitable due to the corrosive nature of these compounds and the risks of film contamination. Hence, researchers are exploring alternate organometallic precursors in a CVD process with oxygen being the co-reactant. In this work, tetraakis(diethylamino)hafnium precursor is used in an ALD process with moisture co-reactant to deposit HfO₂ films onto H-terminated Si substrate in a temperature regime of 200 to 350 °C. Film composition is determined by XPS analysis and is found to be stoichiometric without residue from ligand decomposition. Film thickness and uniformity is measured by reflection/transmission electron microscope (XTEM). Film growth rate is measured as a function of substrate temperature and reactant pulsing characteristics. These results will be presented and compared with those obtained with the more conventional hafnium chloride precursor.

D3.11 CHARACTERISTICS OF HfO₂ GATE DIELECTRIC DEPOSITED BY REMOTE PLASMA ENHANCED ATOMIC LAYER DEPOSITION METHOD. Ju Young Kim, Do Youl Kim, Yangdo Kim, and Hyungtae Jeon, Division of Materials Science & Engineering, Hanyang University, Seoul, KOREA.

As the metal oxide semiconductor device continues scale down, the high-k gate dielectrics become one of the solutions in providing increased capacitance and reduced leakage currents without significantly increasing the actual equivalent oxide thickness (EOT) of gate dielectrics. Among the high-k materials, hafnium oxide (HfO₂) is considered to be one of the potential replacements of SiO₂ gate oxide due to its high dielectric constant and good thermal stability in contact with silicon. In this study, we investigated the HfO₂ gate dielectric deposited by remote plasma enhanced atomic layer deposition (PEALD) method using metal organic source. HfO₂ films were deposited at 200-350 °C using tetraakis(diethylamino)hafnium (TDEAH) as Hf precursor and oxygen plasma as reactant gas at the various process pressures. The electrical properties of MOS capacitor were measured after post metal annealing. The physical and chemical characteristics of HfO₂ thin film were analyzed by cross-sectional transmission electron microscope (XTEM). Auger electron spectroscopy (AES), X-ray photoelectron spectroscopy (XPS) and Rutherford backscattering spectroscopy (RBS). The electrical properties and reliability characteristics including EOT, hysteresis, leakage current and capacitance were evaluated by LV and C-V measurements. This paper will present the characteristics of HfO₂ gate dielectric deposited by remote PEALD using metal organic precursors.


W has a midgap workfunction and has been studied in combination with HfO₂ as a possible candidate for metal gate/high-k CMOS devices. In this work, we have investigated the effect of post metal anneals on W gate HfO₂ capacitors with respect to the thermal stability of the gate stack, shifts from the flat band condition, changes in capacitance, charge trapping (C/ET, memory correction) and charge trapping Capacitance-Voltage
(CV) measurements on as-deposited W/HfO films result in a CET ~15.5 A, low CV hysteresis, and low leakage (10⁻⁴ A/cm²). However, high-k gate dielectric candidates are generally characterized on high-density interface states. Post metal anneals are required to eliminate these interface states and result in an increase of the CET. Structural analysis of the as-deposited gate stack by high resolution transmission electron microscopy (HRTEM) shows a well defined W/HfO₂ interface in contrast to as-deposited Al₂O₃/HfO₂ interfaces which clearly show a reacted layer and also a higher CET for the same thickness of stack. Upon post metal annealing, HRTEM images of W/HfO₂ indicate an interfacial layer between as-deposited W and HfO₂ and Si, corroborating the increase in CET. Annealed W/HfO₂ films have a CET ~16.5 A, low CV hysteresis < 15 mV, leakage 5 orders of magnitude better than an equivalent SiO₂ film and minimum fluctuation shift (extracted work function of W ~ 7 eV) indicating little fixed charge in the gate stack. In addition, charge trapping has been monitored in these films as a function of different thermal anneals.

D3.13 YTTRIUM STABILIZED HfO₂ EPITAXIAL THIN FILMS - A NEW APPROACH FOR HIGH-K GATE DIELECTRIC. J.-M. Lee, J.V. Dai, H.L. Chen and C.L. Choy, Department of Applied Physics, Hong Kong Polytechnic University, Hung Hom, Kowloon, Hong Kong, CHINA.

HfO₂ is an attractive candidate for high-k gate dielectric due to its thermodynamic stability on Si under high temperature annealing. Epitaxial growth of HfO₂ thin films on Si is of significant fundamental and technological interest, even though the amorphous structure has been commonly observed in the approach to high-k gate dielectric candidates. We report successful epitaxial growth of yttrium stabilized HfO₂ thin films on p-type (100) Si substrates by pulsed laser deposition. The epitaxial layers display lower residual stress and temperature dependence of the as-deposited HfO₂ films. Transmission electron microscope observation illustrated a refined orientation relationship between the epitaxial films and Si substrates, i.e. [100]Si||[100]HfO₂ and [010]Si||[010]HfO₂. However, the rough film/Si interface suggests that interdiffusion and interfacial reaction at the interface may happen. High-resolution deep probe X-ray photoelectron spectroscopy analysis (XPS) revealed HF silicate formation at the interface area. Very near to Si surface, XPS spectra also show the presence of H₂SiO₆ bonding. Capacitance-voltage measurement revealed the presence of SiO₂ thickness of about 10 Å has been achieved by a 40 Å-thick epitaxial yttrium stabilized HfO₂ film with a leakage current density of 1x10⁻₆ A/cm² at 1 V gate bias voltage. The growth mechanism of the yttrium stabilized HfO₂ thin films on Si has been studied and it was found that substrate temperature is a critical parameter for the epitaxy of yttrium stabilized HfO₂ films. Substrate temperature higher than 600°C causes SiO₂ formation on Si surface before film deposition and therefore prevents the intended epitaxial growth. On the other hand, the films grown at substrate temperature lower than 450°C also resulted in polycrystalline structure even if the interface is free from SiO₂ layer. This is due to the intense lower kinetic energy of HF and O atoms arrived at the Si surface at lower substrate temperature leading to island growth of the films.

D3.14 MICROSTRUCTURAL EVOLUTION OF ZrO₂/HfO₂ NANO-LAMINATE GATE STACKS GROWN BY ATOMIC LAYER DEPOSITION. Kyungsal Kim, Min-Ho Cho*, Paul C. McIntyre, Stanford University, Stanford, CA, and Department of Ceramics Engineering, Yonsei University, Seoul, KOREA; B.H. Kang, C.W. Yang, School of Metallurgy and Materials Engineering, Sungkyunkwan University, Suwon, Kyonggi-do, KOREA; K.Y. Lim, Memory Research and Development Division, Hynix Semiconductor Inc, Ichon, Kyonggi-do, KOREA.

Recently, high K dielectric films have been suggested as alternatives to the currently employed SiO₂ gate dielectric for CMOS/FET technology since high k dielectric films reduce the leakage current and improve the reliability without decreasing oxide capacitance. Among the suggested materials, HfO₂ films have received attention due to the high-k value, wide band gap, and low oxygen permeation. In addition, HfO₂ films are compatible with conventional CMOS processes including polysilicon gate electrode without filling layer. In spite of previous studies, long time and high temperature annealing is required to bring about the silicidation in the poly Si/HfO₂ system, as like poly Si/ZrO₂ system, due to the similar chemical properties. Furthermore, as the gate depletion effect and boron penetration becomes more prominent for the sub-18A oxide regime, it has been considered that other gate material, such as metal gate and poly Si±Ge, may have to replace poly Si. In our experiments, poly Si±Ge films were deposited on HfO₂ films as a gate electrode to combine the electrical benefits of the poly Si/HfO₂ gate stack after annealing. It is well known that the Ge in the poly Si±Ge films retarded the silicidation in the Ti, Co, Zr in Si±Ge system as compared to the Co, Ti, Zr Si system. From these previous results, compared with poly Si/HfO₂ system, the silicidation will be retarded in poly Si±Ge / HfO₂ system after annealing and then, the retardation of silicidation is expected to bring about other reaction, silicate formation, in poly Si±Ge / HfO₂ / HfO₂ films and poly Si±Ge (x=0.6) films were deposited by using a DC magnetron sputtering and a low pressure chemical vapor deposition LPCVD system. After the formation of the MOS structure, the specimens were annealed from 700°C to 900°C in N₂ ambient for 30 minutes and the electrical properties were measured by using CV and I-V measured.

D3.17 HIGH-K METAL OXIDES DIELECTRICS ON Ge (100) SUBSTRATES. David Chi, Roger B. Tripke, and Paul C. McIntyre, Department of Materials Science and Engineering, Stanford University, Stanford, CA; Chi On Chiu and Krishan A. Suresh, Department of Electrical Engineering, Stanford University, Stanford, CA; Eric Garfunkel and Teng-Kai Chang, Department of Chemistry and Physics, Rutgers University, Piscataway, NJ.

Oxidation of thin metal films in the presence of ultraviolet light has been shown to produce high metal oxide dielectric layers. The oxides of hafnium and zirconium are both considered potential high-k replacements for SiO₂ in future MOS devices. Growth kinetics for these two metal oxides under UV- ozone conditions is compared using imaging (HRTEM) and ion scattering (NRA) techniques. The primary advantage of nuclear reaction analysis (NRA) is its high sensitivity to oxygen. Accurate measurements of oxygen areal density were used to calculate effective metal oxide thicknesses. Results from NRA were corroborated using HRTEM. Our results show that the UV-ozone process can be used to fabricate gate oxides of the thickness required for the gate dielectric application. Electrical measurements (CV, IV) on MOSCAP structures demonstrate the promise of UV-ozone grown HfO₂ and ZrO₂ as gate dielectrics on Si substrates passivated by an ultrathin SiO₂ layer. Capacitance-derived EOT values of 1.5-2.0 nm (without quantum mechanical corrections) were obtained for starting metal precursor thicknesses of 2-5 nm, corresponding to 2-5.5 nm thick metal oxide layers. Leakage current densities were on the order 10⁻¹⁰ A/cm² at 1 V bias. Electrical results obtained were highly dependent upon the surface passivation of the silicon substrate. Several passivation methods will be discussed. The procedure yielding the optimum electrical results entailed an HF strip followed by a low P₃O₅ UV-ozone re-oxidation of the Si surface.
amorphous Si films were deposited over the oxides to prepare heavily-doped gate electrodes in the MOS structures. Samples were then thermal annealed at 950, 1000, and 1050°C (nominal zero time at peak temperature). Heating and cooling rates are approximately 50°C/s. Flat band voltages ($V_{FB}$) were determined from CV measurements on dot patterns. The 800°C anneals were used as a baseline, at which the poly-Si electrodes are crystallized and acquire electrical activation while subjecting the high-k dielectrics to a low thermal budget. Positive shifts in $V_{FB}$ were observed, relative to a pure SOI2 control, ranging from 0.2 to 0.6V. Spike annealing changes $V_{FB}$ towards that for SiO2 for ALD films deposited over underlayer films. The $V_{FB}$ shift and the changes with annealing temperature show systematic dependence on the nitridation of the underlayer.

D3.22

LS MOCVD OF BARIUM STRONTIUM TITANATE THIN FILMS USING NOVEL PRECURSOR MATERIALS.

Yung Ho Chi; Young Wo Oh; Jung Woo Park; Young Suk Lee; Chang Yoon Kim; Yung Rae Kim.

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BST have attracted much attention in memory devices due to their high dielectric constants. However, low volatility of the Ba or Sr precursors with only thiol ligands has limited achievements in obtaining high quality thin films by liquid source metal organic chemical vapor deposition (LS-MOCVD) processes. To improve the volatility of these precursors, many attempts have been made such as adding polymer ligands to stabilize the complexes. We report the synthesis of new precursors $\text{Ba(thd)}_3$($\text{tmee}_n$) and $\text{Sr(thd)}_3$($\text{tmee}_n$), where tmee $\equiv$ tris[2-methoxyethoxy]ethylamine, and LS MOCVD of barium strontium titanate (BSTO) thin films using these precursors. Due to increased basicity of amine compared with ethers, it is expected that the nitrogen-donor ligand will make a strong bond to a metal than an analogous oxygen-donor ligand, consequently improving the volatility and thermal behavior of these precursors. Thin films of BSTO were grown by LS MOCVD using a cocktail source consisting of the conventional Ti precursor $\text{Ti(thd)}_2$($\text{OPr}_2$) and these new Ba and Sr precursors. As-grown films were characterized by XPS, SEM, XRD, and CV and LE measurements. BSTO films grown at 870°C were stoichiometric BST with very smooth surface morphology and their dielectric constants were found to be as large as 450. Dependence of the composition and the electrical properties of the BSTO films on the growth temperature, working pressure, and the composition of the cocktail source will be discussed.

D3.23

METAL-ORGANIC CHEMICAL VAPOR DEPOSITION OF Pr2O3 FILMS ON SILICON SUBSTRATES.

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In recent years, Pr2O3 has received much attention because of the possible use as alternative gate dielectrics in CMOS devices. Physical vapor deposition methods have been studied extensively for deposition of Pr2O3 films on silicon substrates, while, to date, there are no studies on chemical vapor deposition methods. We report on the results of a recent study on the deposition of praseodymium oxides thin films on silicon substrates by metal-organic chemical vapor deposition (MOCVD). Sipted Pr(III) is(diketonate) precursor has been used as the metal source and the deposition conditions have been carefully selected because of a large variety of possible Pr2O3 - (x = 0-3) phases. Pr2O3 films have been obtained in a non oxidizing ambient in a hot-wall MOCVD reactor, using 750°C deposition temperature, while Pr2O3 films were formed using 950-1000℃ growth temperature. The structural and morphological characteristics of Pr2O3 films were studied by means of scanning electron microscopy (SEM), X-ray diffraction (XRD), transmission electron microscopy (TEM), energy dispersive X-ray analyses (EDX), and atomic force microscopy (AFM). Chemical compositional analyses have been performed by energy filtered transmission electron microscopy (EFTEM) analysis and a fully understanding of the MOCVD process has recently been achieved. Preliminary electrical measurements pointed to MOCVD as a reliable growth technique to obtain good quality Pr2O3 films.

D3.24

INTERFACE CHARACTERIZATION OF THE HIGH-K GATE DIELECTRIC/Pr2O3/Ho:ZnO Heterostructure.

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Pr2O3 is currently under consideration as a potential alternative gate dielectric candidate for sub-0.1μm complementary Metal-Oxide-Semiconductor (CMOS) technology [1-3]. For all thin gate dielectrics,
the interface with silicon plays a key role, and in most cases is a
dominant factor in determining overall electrical properties. Most of
the high-performance MOSFET systems involve high-k metal
oxide interfaces with Si. In order to maintain a high-quality interface and
channel mobility, it will be important to have no metal oxide or
silicate phases present at or near the channel interface. We studied
the PtO2/Si[100] interface by a non-destructive depth profiling using
synchrontron radiation photo-electron spectroscopy and ab initio
calculations. Our results provide evidence that a chemical reactive
interface exists consisting of a mixed Si-Pr oxide such as
\[ \text{Si}_x\text{Pr}_{1-x} \text{O}_{2-\delta} \] where \( x \) is non-stoichiometrically in the presence of excess 
Pt oxide. In the presence of excess Pt oxide, there is no indication of
high-k dielectric materials because they represent an incremental
modification of SiO2 films by Pt ions so that the interface characteristics can be similar to Si-SiO2 interface properties. The ternary phase diagram, determined experimentally for the first time, indicates that these non-stoichiometric dielectric materials are amorphous and stable on Si up to high temperatures, without phase
separating into crystalline PtO2 and SiO2. Under ultrahigh vacuum
conditions, silicate formation is observed when the Pt is heated above 800°C. The praseodymium silicate system observed at the

D.3.25
SEARCHING NEW HIGH-ß-DIELECTRICS BY COMBINATORIAL
CVD: Bin Xing, Department of Chemistry, Jeffery T. Robberts, Department of Chemistry, Stephen A. Campbell, Department of Electronic Engineering, Wayne State University, Detroit, Department of Chemistry, University of Minnesota, Minneapolis, MN.

To develop a high-ß gate dielectric for replacing SiO2 in MOSFETs, multi-component metal oxides could have advantages over single metal oxides because they may have higher dielectric constants (k) and other favorable properties. However, to find the optimum elemental ratio for obtaining a good dielectric from the given component oxides is a time-consuming and costly work, especially when three or more oxides are involved. Recently, we invented a combinatorial CVD technique to deposit compositional spreads of ternary metal-oxides for
searching new high-ß dielectrics. In the current work, we use this to study compositional spreads of ZrO2, SiO2 and HfO2 deposited using
ammonium metal nitrates. Extending three vertical precursor injectors in a low-pressure CVD reactor so that their exits are close (H = 5-10
mm) to the surface of the horizontal substrate allows each symmetrically distributed precursor flux to spread on the substrate, mix
with the other two components and form a compositional spread. The chemical composition and the film thickness primarily depend on the distances between the spot and each of the three injectors, as well as the mass flow rate of each reactant. The mass flow rates of the reactants are controlled using a precise flow controller. To study the effect of the component oxides in a compositional spread. A crystalline phase, 
\[ \alpha-\text{PtO}_2 \] which does not exist in any of the three pure oxides was observed along with monoclinic \( \text{ZrO}_2 \), \( \text{HfO}_2 \), and rutile \( \text{SiO}_2 \).

D.3.26
SiOxGe3yOz (0.5 < x < 1) OXIDATION IN WET-NITRIC OXIDE
A.M. Habib, G. Tokudome, University of Illinois at Chicago, Dept of Chemical Engineering, Chicago, IL, and
Yunyan Lei, Nigel D. Browning, University of Illinois at Chicago, Dept of Physics, Chicago, IL.

Nitric oxide (NO) added \( \text{SiOxGe3yOz} \) oxidation has been performed at 400°C, 500°C, 600°C, and 700°C, while the wet-NO feed gas was preheated to temperatures before entering the reaction zone. X-ray photoelectron spectroscopy (XPS) and secondary ion mass spectroscopy (SIMS) data suggests that the both nitrogen and oxygen incorporation increases with the dielectric bulk with increasing wet-oxidation temperature, while there is no germanium segregation towards the dielectric substrate interface at all temperatures studied. Moreover, angle-resolved XPS analysis suggests that increase in wet-oxidation temperature above 600°C volatilizes some germanium oxide from the surface region, while silicon monoxide outgases from the dielectric bulk and accumulates near the surface. Nitrogen incorporation is found to stop germanium segregation, since, wet or dry oxidation at the
above-specified temperatures is known to cause germanium segregation. Z-contrast imaging with scanning transmission electron microscopy (STEM) shows that the \( \text{SiOxGe3yOz} \) substrate interface is less than 2 Å. These results are discussed in the context of an overall mechanism of SiOxGe3yOz wet-oxidization.

D.3.27
ORGANO METALLIC RUTHENIUM MOGVD PRECURSORS

Films of ruthenium are currently receiving considerable attention as potential candidates for capacitor electrodes due to their low resistivities, good susceptibilities to dry etching, and the conductivity of the RuO2 oxide phase. Most recently, 1,1’-diethyldithiocarbamate has been described in the literature as a promising candidate for this application. As the ruthenium metal precursor may vary the physical properties of the precursor can change significantly. Novel ruthenium compounds have been synthesized and will be compared to 1,1'-diethyldithiocarbamate. Precursor properties, such as thermal stability, vapor pressures, and viscosities will be presented. Furthermore, results from ruthenium films deposited on an SiO2/Si substrate using the most promising candidate precursor(s) will be discussed and compared to films generated from 1,1'-diethyldithiocarbamate. XPS and Auger results will be used to analyze film composition, crystallinity and the degree of film
orientation as determined by XRD. The results from SEM and AFM measurements will be shown to compare the thickness and morphology of deposited films from different precursors. Resistivities and thermal stabilities of the films will be presented.

D.3.28
ATOMIC LAYER DEPOSITION OF Ti-AlN THIN FILMS AS AN OXYGEN DIFFUSION BARRIER FOR FUTURE HIGH-DENSITY VOLATILE MEMORY CAPACITORS. Yong Ju Lee, Ja Yong Kim, Sang-Won Kang, Korea Advanced Institute of Science and Technology (KAIST), Department of Materials Science and Engineering, Daejeon, REP. OF KOREA.

Perforometric random access memory (PRAM) has been touted as a possible future memory device. Since ferroelectric films are typically prepared at annealing temperatures ranging from 600°C to 700°C in a strong oxygen environment, the polycrystalline film is easily oxidized, and forms an insulating layer of SiO2 which severely degrades the device
performance. Therefore, it is necessary to develop a high-temperature diffusion barrier to prevent oxidation of the polycrystalline film. TiN has been extensively studied as a diffusion barrier in advanced integrated circuit devices, suggesting that TiN can be introduced without any difficulties into existing or future ultra-large-scale processes. However, TiN films oxidize noticeably at temperatures above 500°C forming 
\( \text{TiO}_2 \) (rutile structure). In this study we have investigated the Ti-AlN films deposited by plasma-enhanced atomic layer deposition (PEALD). Ti-AlN films were synthesized from
tetrakis(dimethylamino)tin [TDMAT], NH3, and trimethylaluminum [TMAl] at a low temperature \( 100^\circ\)C using PEALD. A hydrogen plasma was used as a reducing agent for TMAl and to improve film quality. One cycle of Ti-AlN deposition consisted of TiN and Al steps, and the Ti-AlN cycles were then repeated until the desired thickness was obtained. The growth rate was saturated at 0.35 nm/cycle, which makes it easy to control the film thickness. Consequently, Ti-AlN films had excellent surface morphology and good step coverage on a patterned structure, which resulted from the self-limiting surface reactions. Ti-AlN films are polycrystalline with a hexagonal Ti3AlN4 structure and good oxidation resistance when \( \text{O}_2 \) annealed at 700°C for 30 min.

SESSION D4/G1: JOINT SESSION HETEROGENEOUS INTEGRATION AND STAINED Si TECHNOLOGIES
Chairs: Tai-Joe King and Timothy D. Sands
Wednesday, April 30, 2014
Golden Gate C1/C2 (Marriott)
8:30 AM D4/L1.1 HETEROGENEOUS INTEGRATION OF SiGe, GaAs, AND InP WITH Si, E.A. Fitzgerald, Department of Materials Science and Engineering, Cambridge, MA.

A long sought after goal has been to expand the product offerings in semiconductors through the use of new materials. Traditionally, new materials required new and sometimes novel infrastructure to process and manufacture materials and devices. One of the barriers to utilizing incumbent manufacturing infrastructure has been the
disimilarity in semiconductor materials. For example, lattice mismatch between semiconductor materials has prevented most novel materials from being monolithically integrated on common substrate. In this talk, we show that relaxed SiGe is a pathway for introducing novel semiconductor materials in Si CMOS infrastructure. Although strained Si is now attracting much interest, strained SiGe and Ge heterostructures integrated on Si may offer even greater performance enhancements. In addition, we have demonstrated continuous wave, room temperature GaAs and InGaAs lasers on Si using this materials technology. As the use of relaxed SiGe increases, integrated Ge heterostructures allow the introduction of more complex heterostructures for electronics and optoelectronics. We also show that relaxed SiGe on Si creates a new path for wafer bonding, in which relaxed SiGe and GaAs are transferred from an Si substrate to Si wafers. These transferred structures promise to enable monolithic integration of strained Si Ge MOSFETs and Ge heterostructures for high performance CMOS technology. Electrical characterization of strained SiGe MOSFETs has determined the strain-induced mobility enhancement that can be used to evaluate performance and technological viability of strained SiGe MOSFETs. The results help define the challenges for obtaining enhancement for both NFET and PFET devices. The results also indicate the challenges in scaling to nanometer length scales. Si/SiGe heterostructures allow novel device structures and process techniques suitable for ultra-thin body devices. Such devices can combine the advantages of enhanced transport in strained layers and extreme device scaling enabled by ultra-thin body and double gate structures. Some of the progresses in materials and device structures will be presented.

9:30 AM D4.3/G1.1
RELAXATION OF A COMPRESSED FILM ON A COMPLIANT SUBSTRATE: EXPANSION, WRINKLING, AND FRACTURE.
Brian Hwang, University of Texas at Austin, Dept of Aerospace Engineering and Mechanics, Austin, TX; J. F. Forder, and Z. Sze, Princeton University, Dept of Mechanical and Aerospace Engineering, Princeton, NJ; H. Yin and J. C. Sturm, Princeton University, Dept of Electrical Engineering, Princeton, NJ; K.D. Holzrichter Naval Research Laboratory, Washington, DC.

A compressively strained, epitaxial SiGe film was transferred to a Si wafer coated with a glass layer, and then patterned into islands of various sizes. Upon annealing, the glass flows and the SiGe relaxes. The initial relaxation process includes both lateral expansion and wrinkling. The competition sets a critical island size. For small islands, expansion dominates, resulting in flat and relaxed SiGe islands. For larger islands, wrinkling dominates. After a long annealing, the wrinkles either disappear or cause the film to fracture. We model the relaxation process using a nonlinear plate theory for the film and a fabrication theory for the glass and simulate the evolution of the film (in both lateral and vertical directions) and stresses in the film. The results are compared to experiments. By comparing the timescales of expansion and wrinkling, an explicit formula is obtained to estimate the critical island size. For large islands, we show that tensile stress builds up as the wrinkles grow and fracture occurs at a stress level set by the flaws size in the film. We demonstrate that a cap layer suppresses wrinkling, reducing a large island crack-free.

9:45 AM D4.4/G1.4

In the fabrication of SiGe/Si heterostructure devices, the biaxially-strained Si layers are usually deposited on a virtual substrate formed from SiGe on Si. SiGe on Si is usually grown at a temperature higher than 700°C. For SiGe with up to 20% Ge, it was effectively relaxed after annealing with 2.5°C/cm G2 in a temperature range of 700°C to 900°C; relaxation of more than 80% is achieved. PMOS and NMOS devices are successfully fabricated and much enhanced hole and electron mobilities are demonstrated. [1] K. Kim et al, Symp. on VLSI Tech., 98 (2002); [2] H. Trinkaus, et al, Appl. Phys. Lett., 76, 3552 (2000); M. Laybourn, et al, J. Appl. Phys., 92, 4290 (2002).

10:30 AM D4.5/G1.5
SURFACE TOPOLOGY OF IN-SITU STEP-GRATED SiGe,
H. Gu, D. Ge, BUFFER ON Si SUBSTRATE. R. H. Grusk, R. Schen, E. C. Johnsen, P. M. McNeese, and O. Petrov, Stanford University, Microelectronics Research and Development Center (SRDC), Research Division, Yorktown Heights, NY.

Strained Silicon layers grown on less than 1% relaxed SiGe buffer layers on Si are promising materials for CMOS devices because the in-plane tensile strain in the layers enhances the electronic carrier mobility in both hole and electron inversion layers. Generally, FET devices made with low germanium concentration relaxed SiGe material show significant electron mobility enhancement, but low increase in hole mobility. As the germanium concentration increases above 30% in the SiGe layer, hole mobility begins to rise. Therefore, high germanium content silicon materials are expected to be important in future microelectronic device technologies, and their material properties require increasing study. One well known problem in high germanium concentration relaxed SiGe heterostructures is poor surface roughness and high etch pit density. In this work, stepwise graded SiGe buffers with various germanium concentrations are grown in an 8 inch wafer-size CVD system. Low germanium content films, 15%, are found to have significant surface roughness. In RMS value of ~10nm and Z-range of ~90nm, and optical pit density by microscope as high as ~300 pits/mm^2. As the germanium concentration in the buffer layer increases, surface roughness and pit density both increase monotonically. Yet over 10% Ge, the RSM values of this SiGe buffered layer was 1.5 times higher than that of the SiGe buffer layer was 1.5 times higher than that of the SiGe buffered layer. The SiGe buffer layer was subjected to in-situ RT annealing; surface roughness as measured by AFM was reduced by a factor of two and the pit density reduced by a factor of four. The SiGe buffer relaxation, however, as measured by triple axis X-ray diffraction, is unchanged after in-situ annealing.

10:45 AM D4.6/G1.6
FREE STANDING SiGe AS A COMPLIANT SUBSTITUTE FOR Si. G. M. Cohen, P. M. McNeese and J.O. Loff, IBM T.J. Watson Research Center, Yorktown Heights, NY.

We show that SiGe fixed on Si substrate is relaxed, the free-standing SiGe structure consists of a 20nm-thick, 5 μm square silicon slab supported by a SiO2 pedestal at a single contact point at the center of the square (the cross-section resembles a pyramid). A matrix of free-standing structures was made by patterning a bonded silicon-on-insulator (SOI) wafer and undercutting the SiO2 to form the pedestal. Un-patterned areas of the SOI wafer and the exposed bulk Si substrate were included as reference (control) regions. A UHV CVD SiGe layer was grown epitaxially on both sides of the free-standing SiGe and simultaneous monitoring of the blanket SOI and bulk substrate control areas. The SiGe layer thickness was about 200nm, which is 10 times thicker than the free-standing SiGe film. Scanning electron microscopy (SEM) images show faceting at the edge of the free-standing SiGe squares indicating single crystal growth, and thin poly-SiGe is seen on the SiO2 pedestal. The strain, layer thickness, and composition of the SiGe and the strain in the free-standing SiGe slab were determined by high-resolution x-ray diffraction (HRXRD) measurements. The SiGe film grown on both SiO2 and bulk silicon was found to be fully relaxed. In contrast, the SiGe layer grown on free-standing silicon was 0.5% strain-relaxed, and the free-standing SiGe slab was measured to be under tensile strain. Since the same lattice mismatch...
was found between the SiGe layer and the Si on the free-standing silicon and on the SOI and bulk Si control regions, we conclude that the strain relaxation in the SiGe film is not accompanied by the strain accommodated entirely by the free-standing silicon film under tensile strain. This was further confirmed by AFM measurements. The SiGe film on the control regions showed a very smooth surface with only a few misfit dislocations. No surface steps from misfit dislocations were observed on the surface of the SiGe film on free-standing Si. These results show that free-standing silicon serves as an ideal compliant substrate for SiGe.

11:00 AM D4.7/G1.7
HIGH Ge CONTENT (~0.6) RELAXED SiGe LAYERS AND SiGe/GaAs INTERFACES BY COMPLIANT SUBSTRATE APPROACHES. Haihui Yin, Rebecca L. Peterson, Center for Photonics and Optoelectronic Materials, Princeton University, Princeton, NJ; K.D. Hobert, Naval Research Lab, Washington, DC; R. Dufy, Department of Geoscience, Princeton University, Princeton, NJ; J.C. Sturm, Center for Photonics and Optoelectronic Materials, Princeton University, Princeton, NJ.

There has been increasing interest in compliant substrates for integration of heterogeneous epitaxial materials. In our experiments, borophosphosilicate glass (BPSG) on silicon was used as a compliant substrate to allow the relaxation of a strained silicon-germanium (SiGe) layer initially grown pseudomorphically on Si(100) substrate and then transferred to the BPSG by a bond and etch process [1]. The compressed SiGe can then relax outwards by BPSG flow during a 800°C anneal to soften the BPSG. This process in principle allows the formation of a free-standing layer for subsequent device without requiring any misfit or threading dislocations, unlike conventional relaxed buffer technology. We have previously reported how capping layers and patterning the SiGe into islands can prevent a parasitic buckling during the relaxation of the subsequent epitaxial layers [2,3], but the layers were limited in Ge fraction to ~0.3 [3]. In this talk, we first use the relaxed SiGe layer as a substrate for additional SiGe growth with higher Ge content. After annealing, strain partition between the SiGe layers is observed and consequently, the equivalent Ge percentage of fully relaxed SiGe based on lattice constant is increased. Secondly, strain partition for different thickness of the initial relaxed SiGe layer is investigated and we observe that a thinner initial layer allows more relaxation of the subsequent SiGe layer, so that an relaxed layer of x=0.6 is achieved. To further increase the lattice constant, commensurately strained [compressive] 30 nm of Si$_{0.40}$Ge$_{0.60}$ is deposited on pre-relaxed Si$_{0.40}$Ge$_{0.60}$ islands of varying thickness by CVD at 550°C. Upon anneal at 800°C, we observe by micro-Raman spectroscopy that the Si$_{0.40}$Ge$_{0.60}$ film gets stretched by the same amount as that which the Si$_{0.40}$Ge$_{0.60}$ film expands, indicating strain partition between the two layers, consistent with no relaxation by misfit dislocations. By varying the relative thickness of the layers, final relaxed layers with equivalent Ge percentages from 0.45 to as high as 0.57 are obtained. These are the highest Ge fractions known to date by conventional substrate. Finally, the strain qualities of epitaxial Ge layers on top of these structures will be described. This work is supported by DARPA, I. K.D. Hobert, F.J. Buh, M. Fatemi, M.E. Twigg, P.E. Thompson, T.S. Kunn and C.K. Inoki, J. Electron. Mater. 30, 895 (2001); Y. Liu, R. Dufy, K.D. Hobert, Z.S. Kurn, C.K. Inoki, S.R. Shieh, T.S. Dufy, F.J. Buh and J.C. Sturm, J. Appl. Phys. 91, 5716 (2002); S. Yin, R. Huang, K.D. Hobert, Z. Sao, S.R. Shieh, T. Dufy, J.C. Sturm, “Prevention of Buckling during SiGe Relaxation on Compliant Substrates”, MRS Spring Meeting, San Francisco, CA, 2002.

11:15 AM D4.8/G1.8

Strained silicon has superior electronic properties and was used to develop high-performance devices in the mainstream technology in the near future. The key problem of the implementation of strained silicon in MOSFET or MODFET devices is the fabrication of high quality strain relaxed SiGe layers on Si(100) which serve as virtual substrates for the growth of strained Si. Our approach using He or H implantation and annealing to fabricate very thin, high quality buffer layers has gained considerable interest. We will report results on the strain relaxation of strained SiGe layers on Si(100) wafers with Ge contents varying between 1.5 and 30%. The pseudomorphic SiGe layers were grown either by chemical vapor deposition (CVD) or by molecular beam epitaxy (MBE). In addition, results of thin buffer layers on SOI wafers will be presented. The He implantation was performed with energies between 1.0 keV and 200 keV and doses between 1 x 10$^{16}$ cm$^{-2}$ and 3 x 10$^{16}$ cm$^{-2}$ depending on the Ge content and the epilayer thickness. The thickness was varied between 70 and 100 nm for moderate, typically around 850°C, was used to relax the strain. The resulting layers were investigated with numerous analytical techniques, e.g. transmission electron microscopy, AFM, He ion channeling and X-ray diffraction. The relaxed smooth surface only a few misfit dislocations, annealed tensile strain. Residual strain and threading dislocation density will be discussed in relation to the formation of misfit dislocations and the growth conditions and the thermal treatment. We will also show that MODFETs produced on such thin buffer layers show higher drive current and the same RF performance as devices fabricated on unstrained SiGe buffer layers. The strained Ge-3Si buffer layers indicating the high layer quality. A model for the implantation induced strain relaxation mechanism will be discussed, which assumes the formation of misfit dislocations segments from dislocation loops punched out by gas filled platelets.

11:30 AM D4.9/G1.9
REAL-TIME OBSERVATION OF STRAIN RELAXATION IN SiGe FILMS ON ULTRA-THIN SOI VIA LOW-ENERGY ELECTRON MICROSCOPY. B. Yang, A.R. Wolf*, M.M. Roberts, D.E. Savage and M.G. Lagally, University of Wisconsin-Madison; *Current address: CHESS, Cornell University.

We have used low-energy electron microscopy (LEEM) to study the initial stage of strain relaxation in Si$_{x}$Ge$_{1-x}$, thin films grown on silicon-on-insulator (SOI) and bulk Si substrates. Dislocation glide, cross-slip, and reconnection interactions have been observed in real time. In general, strain relaxation is difficult to study by conventional transmission electron microscopy. Because of its sensitivity to the dislocation-induced strain field, LEEM is able to detect single, buried misfit dislocations. In contrast to TEM, LEEM is nondestructive and can observe dynamic events during growth, while TEM is destructive. Dislocation glide in SiGe films that lie below the critical thickness for dislocation motion on bulk Si. These results provide direct experimental evidence for a decrease in line tension of a buried misfit segment as the SiGe layer becomes thinner than the critical thickness. We will discuss our data in the context of recent models of SiGe film relaxation on SOI [1, 2]. Videos of real-time observations, such as dislocation interactions, cooperative motion, and re-connection of glide dislocations with terminal segments of source and sink dislocations will be presented. The discussion of the models. Our observations have direct implications for the fabrication of strained layer devices on SOI substrates. [1] E.M. Rehder, Ph.D Thesis, University of Wisconsin-Madison, 2002; E.M. Rehder, T.P. Kosch, to be published [2] P. Brown, W.D. Nix, Appl. Phys. Lett. 69 123 (1996).

Supported by ONR, DARPA, and NSF.

11:45 AM D4.10/G1.10
HYBRID VALENCE BANDS IN STRAINED LAYER HETEROSTRUCTURES GROWN ON RELAXED SiGe VIRTUAL SUBSTRATES. Minjo Lee, Eugene A. Fitzgerald, Massachusetts Institute of Technology, Dept. of Materials Science and Engineering, Cambridge, MA.

Strained Si, Si$_{1-x}$Ge$_x$, and Ge layers grown on Si$_{1-x}$Ge$_x$ virtual substrates (vs) provide a path for future high performance CMOS device fabrication. Surface strained Si devices exhibit peak hole mobility enhancements of 2 times over bulk Si, while dual channel devices, which combine a strained Si cap with a buried compressive layer, exhibit enhancements of 3 to 8 times. When the strained layer or layers are grown to nanometer-scale dimensions, the wavy function of the hole occupies a hybrid valence band where the relaxed substrate, compressive buried layer, and tensile surface layer each make strong contributions to transport. The hybridization of the valence band results from the low effective mass of holes in the out-of-plane direction, and the relative weighting factor of each layer is determined by the vertical effective field and layer thickness. For example, we demonstrate a p-MOSFET consisting of a single 45Å strained Si layer grown on a Si$_{0.5}$Ge$_{0.5}$ virtual substrate with mobility enhancements comparable to those seen in many dual channel heterostructures. At high $E_{ff}$, the hybridizes the Ge-like effective mass in the relaxed buffer with the valence band splitting in the Si cap, creating a band structure which resembles a compressively strained Si$_{1-x}$Ge$_x$ alloy. We also demonstrate a high mobility digital alloy consisting of ~1 nm alternating layers of strained Si and relaxed Ge. In this device, the hybrid valence band across the device phase does not remain nearly constant with $E_{ff}$. The high mobility of the digital alloy proves that the hole can intermix the properties of many layers, unlike when the layers are only several monolayers thick. The governing mechanism of our devices is shown to be the effective field in the strained layer and the breaking of the symmetrical structure in strained SiGe films.
13:30 PM #D5.1

CHALLENGES AND PROSPECTIVES IN USJ TECHNOLOGY FOR ADVANCED CMOS. Hiroshi Kogawa, NEC Electronics Corporation, Advanced Process Development Division, Kawasaki, JAPAN.

The elimination of the transient enhanced diffusion (TED) of dopants is very important to fabricate sub-10nm CMOS devices. The gentle dopant profile caused by TED degrades the transistor performance. For 90-10nm CMOS devices, the shallow junctions damage, decreasing spike annealing, and the utilization of high-diffusivity dopants can solve to suppress TED. Thermal process optimization also can be an option, since there’s an enough margin of the thermal budget. However, it can realize surface independent annealing with high field (100kV) feedback, and fabrication of shallow and low-resistance layers by using the fast ramp-up/ramp-down recipe. Channeling implantation is also effectively suppress TED. The annealing at the medium temperature range is effective to decrease the damage, especially for heavily ion implantation. For p+ SD-extension profile, Xj of as-implanted is 15-20nm and final Xj is 25-30nm, which meets the ITRS2001. If Xj of 65nm CMOS devices must be shallower than 20nm, as in ITRS2001, we must maintain the implanted dopant profile in SD-extension regions. This implies that thermal process, especially temperature, may be restricted after SD-extension implantation. One candidate is to use short time annealing, such as flash lamp annealing (FLA) and laser annealing (LA). The annealing time is mS range, even for FLA, and this means that feedback control by monitoring wafer temperature is not available. As a result, wide process spread (temperature) margin must be necessary as compared with spike annealing. The other candidate is low temperature annealing, which is more controllable as compared with FLA and LA. But the most critical issue is the junction leakage current. On the assumption of conventional CMOS fabrication process, deep SiN formation will be most critical issue. Elevated SD structure can be an option, for pre-baking and process temperatures decrease down to 600-650°C range.

200 PM #D5.2

OVERVIEW OF THE PROSPECTS AND CHALLENGES FOR LAMP ANNEALING IN 45-65nm TECHNOLOGY NODE CMOS. Kyochi Suguro, Tomoyuki Ito, Tohru Konishi, and Yoshiki Itagaki, Process and Manufacturing Engineering Center, Toshiba Corporation, Yokohama, JAPAN.

Ultra shallow junction with low resistance is required to improve short channel effects in 45-65nm technology node. Since the gate length for high performance MOSFETs shrinks to 28-30nm, the extension depth (p junction) of Si implanted must be shallower than 20nm. However, current RTA tool is confronted with the trade-off problems of thermal diffusion of dopant atoms and electrical activation which is limited by solid solubility. Rapid thermal annealing is also required to reduce dislocation density so that the pn junction leakage specification of high performance MOSFETs can be satisfied. In order to minimize the annealing time at high temperatures, we investigated various lamp annealing methods and newly developed flash lamp annealing (FLA) technology. By optimizing FLA conditions and implantation conditions, /p+n junction depth of 14nm at 120cm3 and 11nm at 180cm3 were realized with the sheet resistivity of 7700Ωcm, and high junction leakage. As well as /p+n junction, ultra-shallow /p+n junction was successfully formed. Since the impurity diffusion is drastically suppressed, the higher acceleration energy for ion implantation can be applied. The use of higher acceleration energy results in the reduction in the process time of as-implanted in especially in ultra-low energy regime. Shorter length ion implantation leads to higher throughput and reduces process cost of shallow junction formation process. In this paper, we overview prospects and challenges for rapid thermal annealing in 45-65nm technology node.

230 PM #D5.3

EFFECT OF SIDEWALL NITRIDE SPACER ON ULTRA SHALLOW JUNCTION ENHANCEMENT IN 45NM TECHNOLOGY NODE. Daniel Krueger, Victor Melnik, Peter Zausig, Peter Berns, Thomas Kope, and Defik Bolze, IBM, Frankfurt (Oder), GERMANY.

Antimony has been suggested as an alternative to As for shallow-source/drain extensions in mOSFETs. Transient enhanced diffusion (TED) effects due to implantation damage and due to As clustering make the tightness of the junction leaks to the ultra-shallow junctions. In recent years, we have discovered that the As TED-SIMS signature is stronger than the Si TED-SIMS signature. Also, the As TED-SIMS signature is more sensitive to the implantation damage in the near-surface region of the device, which can be used to quantify the effect of As TED on the final junction profile. In this paper, we will present evidence that As TED is the dominant source of TED in the ultra-shallow junctions and that As TED is responsible for the enhanced junction leakage. We will show that the As TED-SIMS signature is stronger than the Si TED-SIMS signature, and that the As TED-SIMS signature is more sensitive to the implantation damage in the near-surface region of the device. This indicates that As TED is the dominant source of TED in the ultra-shallow junctions and that As TED is responsible for the enhanced junction leakage.

3:30 PM #D5.5

SH SEGREGATION AND ENHANCED DIFFUSION ANALYSIS DURING ULTRA-SHALLOW JUNCTION FORMATION IN SILICON. Daniel Krueger, Victor Melnik, Peter Zausig, Peter Berns, Thomas Kope, and Defik Bolze, IBM, Frankfurt (Oder), GERMANY.

Antimony has been suggested as an alternative to As for shallow-source/drain extensions in mOSFETs. Transient enhanced diffusion (TED) effects due to implantation damage and due to As clustering make the tightness of the junction leaks to the ultra-shallow junctions. In recent years, we have discovered that the As TED-SIMS signature is stronger than the Si TED-SIMS signature. Also, the As TED-SIMS signature is more sensitive to the implantation damage in the near-surface region of the device, which can be used to quantify the effect of As TED on the final junction profile. In this paper, we will present evidence that As TED is the dominant source of TED in the ultra-shallow junctions and that As TED is responsible for the enhanced junction leakage. We will show that the As TED-SIMS signature is stronger than the Si TED-SIMS signature, and that the As TED-SIMS signature is more sensitive to the implantation damage in the near-surface region of the device. This indicates that As TED is the dominant source of TED in the ultra-shallow junctions and that As TED is responsible for the enhanced junction leakage.
Sb segregation with very high dose loss. The observed reduction of enhanced diffusion makes Sb an outstanding candidate for replacing As in Si/Ge extensions for sub-100 nm CMOS and BiCMOS technologies.

3:45 PM *D5.6

MAXIMUM ACTIVATION AND MINIMUM DIFFUSION BY MILLISECOND ANNEALING. THE KEY TO SHALLOW JUNCTION FORMATION. Peter B. Griffin, Center for Integrated Systems, Stanford University, CA.

The key to ultra shallow junction formation is to maximize dopant activation while minimizing dopant diffusion. In a CMOS process flow, forming shallow diffusion is more difficult than forming shallow NMOS junctions, because the p-type boron diffusion is more rapid than n-type arsenic or antimony diffusion. Fortunately, for the same thermal budget, boron activates more rapidly than arsenic or antimony. It is therefore possible to reduce the diffusion thermal budget for boron by using millisecond anneals while meeting acceptable activation levels. The reason this occurs for boron in particular is related to the atomic details of its activation mechanism. The activation of boron proceeds by boron cluster dissolution, a process that is mediated by silicon self interstitials. Because the supply of self interstitials is limited by the silicon self diffusion rate, going to higher temperatures enhances the dissolution process while minimizing the diffusion process. This occurs because of the higher activation energy for self compared with dopant diffusion. In the case of the n-type dopants, the activation process is not controlled or limited by the native silicon point defects, so going to higher temperatures contributes only a second order enhancement to the activation level based on increased solubility. We will discuss the role of point defects in the activation and diffusion processes and indicate how millisecond annealing at high temperatures provides the optimum path for achieving ultra shallow, highly active junctions.

4:15 PM D5.7

ATOMIC SCALE SIMULATIONS OF EFFECT OF COULOMBIC INTERACTIONS ON CARRIED FLOTTATIONS IN DOPED SILICON. Zudian Qin, Scott T. Dunham, Univ of Washington, Dept of Electrical Engineering, Seattle, WA.

Fluctuations in carrier density associated with discrete dopant atoms have been identified as a critical issue in controlling threshold voltage ($V_{TH}$) in nanoscale MOSFETs. To date, analysis of this phenomenon has largely assumed that the dopants are distributed randomly within the active regions. However, interactions between dopants during device fabrication can lead to correlations in dopant locations, modifying the resulting $V_{TH}$ variations. One source of these correlations is Coulombic interactions between ionized dopants, screened by nearby carriers. In this work, we examine the effect of these interactions on variations in electrical potential within doped regions via kinetic lattice Monte Carlo (KLMC) simulations which simultaneously solve for free carrier distributions and include the effect of ionization potential variations on the diffusion of charged dopants and point defects. Our simulation results clearly show that over a broad range of doping concentrations Coulombic repulsion between like dopants leads to ordering, resulting in a more uniform electrical potential distribution and therefore reduced $V_{TH}$ variations than arises from random doping, with lower temperature annealing giving stronger ordering. In all cases the thermal budget required for ordering is small ($\sqrt{\Delta T} < 2$ nm) compared to projected junction depths (4-6 nm for the 22 nm technology node based on ITRS).

4:30 PM D5.8

DOPANT DIFFUSION SIMULATION IN THIN SOI. Hong-Jyh Li, Robin Tidby, Jonathan Ross, Jeff Gelery, Vertek Industries Ltd, Vancouver, BC, CANADA; Ben Scotts, Heather Gallay, Southwest Texas State University, San Marcos, TX, and Larry Larson, International SEMATECH, Austin, TX.

As the technology of semiconductor devices evolves, the scaling of traditional CMOS devices might approach barriers that make the scaling economically or physically infeasible. New starting materials such as SOI have been attracting attention recently as approaches to overcome these barriers. To further improve the device characteristics using SOI, it is necessary to optimize the top Si layer thickness [1]. As the top Si layer is thinned, the dopant diffusion in the confined Si layer with respect to different thermal treatments needs to be better understood. Recently, dopant diffusion using more advanced annealing technologies like spike and Flash anneals in bulk Si have been studied extensively [2]. The motivation of these annealing techniques is to reduce dopant diffusion and increase thermal treatments needed to be approached the thermal budget. Therefore, it is interesting to study the dopant diffusion and activation in the ultrathin SOI wafers using the spike/Flash anneals. Boron, BF$_2$ and Arsenic were implanted into bulk Si and the same conditions with 35O. Si samples were annealed using both spike (Impulse) anneal and Flash anneal.


4:45 PM D5.9

MODELING AND SIMULATION OF DOPANT DIFFUSION IN SiGe. Chan-Li Liu, Marius Orlovski, Aaron Them, Alex Barr, Ted White, Thich-Yen Nguyen, Hermann Rasen, Advanced Products Research and Development Laboratory, Motorola Inc., Tempe, AZ.

Understanding of dopant behavior in SiGe during implantation and annealing development is critical to further scaling of SiGe technology. We have developed a lattice expansion theory to explain dopant diffusion behavior in SiGe. The theory establishes the relationship between Ge concentration and the changes in dopant activation energies compared to crystalline Si. Quantitative predictions of dopant diffusion for anneal conditions for As, P, and B in SiGe with 20%Ge are in good agreement with experiment. Diffusion equations based on the theory were implemented in the FLIGHT process simulator. Simulated profiles are consistent with experiment under equilibrium conditions without the use of fitting parameters. Implementation of this new tool will help us to speed up the development of novel devices involving strained Si layers.

SESSION D6: POSTER SESSION

STRAINING SI AND SOURCE/DRAIN TECHNOLOGY

Chair: Bin Yu and Tau-Joe King

Wednesday, April 23, 2003

8:00 PM

Salon L-7 (Merriot)

D6.1

A NEW TYPE OF TEXTURE IN THIN FILMS: NiSi, CoSi$_2$ AND o-FeSi$_2$ ON Si(100). Christoph Detznerman and T.M.J. Watson Research, Yorktown Heights, NY; Ahmet Ozer, Boston University, Dept. of Physics, Boston, MA; J.L. Jordan-Sweet, Christian Lavocie, IBM T.J. Watson Research, Yorktown Heights, NY.

We observed a new type of texture for a thin film upon reaction with a single crystal substrate. The type of texture reported so far in thin films are either [1] random, [2] in-plane texture, resulting in distinct spots on a pole figure or [3] fiber texture, with the fiber axis normal to the substrate, creating a ring on a pole figure. For NiSi, CoSi$_2$ and o-FeSi$_2$ on Si(100), we observed an off-normal fiber texture with a fiber axis perpendicular to Si(110) facets in the substrate. NiSi, CoSi$_2$ and o-FeSi$_2$ were formed by depositing Ni, Co or Fe on a Si(100) substrate and annealing at 500, 900 and 950°C, respectively. Synchrontron-radiation was used to measure pole figures for the different silicide films. Standard Bragg-Brentano 8/2θ scans for the silicide planes did not reveal any clear evidence of a strongly textured film. However, full pole figures consisting of complicated line patterns, with very narrow width (ΔD and Δθ < 1°). Unlike with standard fiber texture, these lines are not circles centered in the middle of the pole figure. Especially for the orthorhombic NiSi, very complex patterns were observed, at first sight resembling认真学习 patterns known from electron diffraction. Calculations show that the lines are related to a fiber-type alignment of certain lattice planes parallel to Si(110) planes in the substrate.

D6.2

SHORT-PERIOD (Si$_{14}$/Si$_{75}$Ge$_{25}$)$_{20}$ SUPERLATTICES FOR THE GROWTH OF HIGH-QUALITY Si$_{75}$Ge$_{25}$-0.25 ALLOY.

Lars GRUNBERG, MAN F. BAKMIN, T. TANBO, and C. TOYOGUMA

Department of Electrical and Electronic Engineering, Faculty of Engineering, Tohoku University, JAPAN.

Despite of low cost, abundant in nature, process simplicity and prospect of bandgap engineering, SiGe is still away from its full-fledged usages. To realize the proper utilization of SiGe, strain relaxed and smooth alloy layers is required. In the present experiment, we have grown 2000-A thick Si$_{75}$Ge$_{25}$ alloy layers on Si(001) substrate by MBE process using a short-period (Si$_{14}$/Si$_{75}$Ge$_{25}$)$_{20}$ superlattice (SL) as a buffer. In the SL layers, first a layer of 14 monolayers (MLs) of Si (thickness about 2ML) then a thin layer of Si$_{75}$Ge$_{25}$ (thickness 0.64 ML) was grown. These layers were repeated for 20 times. The alloy layers were grown at 550°C and the buffer layers were grown at different temperatures from 300-800°C. Introduction of the buffer layers dramatically changes the surface morphology of the top alloy layers. The alloy layer showed low residual strain (about -0.16%) and smooth surface (rms roughness ~124Å) with 300°C grown SL buffer. Low temperature growth of Si in SL layer introduces point defects and low temperature growth of
Si$_x$ Ge$_{1-x}$ in Si layer reduces the Ge segregation length, which leads to strained Si layer formation. Strained layers are capable of making barriers for the propagation of threading dislocations and point defect sites that can trap the dislocations. This type of buffer is easier to grow and retains high quality top silicon surface, so this buffer can be considered for the growth of high quality epitaxial structures.

D6.3 MATERIAL CHARACTERIZATION FOR STRAINED-SI CMOS.

Qianghua Nie, Yan Liu, Xiang-Dong Wang, Michael Consonio, Erik Depard, Xingming Zhao, Zhebin Zhu, and Thomas J. Marks. Purdue University, West Lafayette, IN.

Strained Si CMOS devices are moving from the research and development phase to real manufacturing. The greatest hope for this technology is that compatibility with standard CMOS processing could be achieved with minimum process change. Thus, it could become economically competitive in comparison to pushing the lithography limit. The challenges are residing in the use of appropriately engineered strained Si on a relaxed SiGe buffer to achieve sufficient strain in the Si channel, low threading dislocation density, small surface roughness, good uniformity of strain/stress, and good stability with thermal annealing during subsequent CMOS processing. We will present data on our recent effort in establishing a set of analytical techniques to address the needs in these aspects for strained Si material evaluation using SiGe on bulk Si as an example. Transmission electron microscopy (TEM) is used to reveal the defects formation and propagation in the material. Atomic force microscopy (AFM) reveals the cross-hatch patterns, surface roughness, andetch pit density. Raman scattering equipped with mapping capability can measure the strain in Si as well as the spatial distribution of the strain. A stress of ~1.2 GPa was observed in Si with a standard deviation of 0.2 GPa and the stress non-uniformity can generally be correlated to the cross-hatch patterns. TEM and secondary ion mass spectrometry (SIMS) reveals significant intermixing between Si and Ge in the Si channel and SiGe buffer interface upon standard annealing around 900-1000°C used for routine CMOS process.

D6.4 EVALUATION OF STRAIN RELAXATION OF STRAINED-SI LAYERS SELECTIVELY GROWN ON MESA-ISOLATED SiGe-ON-INSULATOR (SGOI) USING RAMAN SPECTROSCOPY AND NANO ELECTRON DIFFRACTION METHODS.


Strained Si MOSFETs are one of the most promising device structures for high-speed CMOS. We have developed strained-Si MOSFETs on the thin relaxed SiGe-On-Insulator (SGOI) structures for combining strained-Si with SOI structures. Since fabrication of the strained-Si MOS with small size is indispensable in the strained-Si MOSFET research, we have investigated strain relaxation during integration processes in an important issue. Here, we have investigated the relaxation of strained-Si layers which were selectively grown on the meso-isolated SGOI layers thinking of the device isolation process. As a result of etching of SGOI structures and successive epitaxial growth of strained-Si, the strain isolation process was carried out using Chemical-Dry-Etching (RTE) procedure performed in N$_2$ atmosphere. As a result, it was confirmed using Raman spectroscopy with resolution of > 1 micrometer square that the strained-Si layers with the size of 5 micrometer square had resistance relaxation to the RPE processes. Meanwhile, to overcome a limit of lateral resolution in the Raman measurements, 2.5-μm square Electron Diffraction (ED) with a resolution of 10μm was employed and the distribution of lattice constant within the strained-Si and SiGe layers was evaluated. It was clearly confirmed that the relaxed-SiGe layer induced tensile strain into the strained-Si layer and the strain was almost maintained to the edge part of the isolated strained-Si layer. In conclusion, it was found that the relaxation of strained-Si layers selectively grown on the meso-isolated SGOI layer was negligible down to 5 micrometer in size, and the nano-ED was effective to evaluate very thin strained-Si layers isolated into sub-micrometer size. This work was partly supported by NEDO. [1] T. Minomo et al., ELDiV-21, 230 (2000).

D6.5 X-RAY SCATTERING AS A PROBE OF INTERDIFFUSION AT Si/SiGe INTERFACES.


We present a thorough analysis of X-ray diffraction as a probe of the interdiffusion at Si/SiGe interfaces. The majority of Si/SiGe interdiffusion studies employ time dependent measurements to test deeper commercial devices. This strategy is limited in the presence of the experimental techniques employed and by the need to assume a functional form for the interdiffusion interdissions and strain dependence when performing the interdiffusion simulations. We have demonstrated that direct extraction of SiGe interdiffusion from X-ray diffraction simulations and numerical solutions to Fick's second law might be performed performing virtual interdiffusion experiments. This approach allows the characterization of the techniques robustness with respect to non-uniformities in the annealing conditions, imperfect knowledge of the rate of strain relaxation, and uncertainties in the structural characterization of samples. We further show that extracted strain relaxation of SiGe interdiffusion from superlattice satellite peak intensity attenuation data is only rigorously valid for superlattices with sinusoidal concentration profiles, in practice it serves equally well for square wave concentration profiles that are common in as-grown samples. Finally, we illustrate the effectiveness of extracting a single, meaningful value for interdiffusion in a system where the interdiffusion varies considerably as a function of Ge concentration and time.

D6.6 DIRECT MEASUREMENT OF THE CONCENTRATION DEPENDENT ACTIVATION ENTHALPY ETHAPLY FOR INTERDIFFUSION AT Si/SiGe INTERFACES.


The activation enthalpy for interdiffusion at Si/SiGe interfaces is believed to be both concentration and strain dependent. An accurate characterization of this quantity is a function of Ge concentration is important both for refining process simulations involving the thermal stability of Si/SiGe interfaces and for understanding the physics of the interdiffusion process. To date, reported measurements of this activation enthalpy are based on unconfirmed assumptions about the functional form of the SiGe interdiffusion with respect to Ge concentration and flux. We demonstrate the use of x-ray diffraction from Si/SiGe superlattices possessing a specially designed concentration profile to directly probe the activation enthalpy as a function of Ge concentration.

Measuring interdiffusion via x-ray diffraction involves monitoring the decay of x-ray (004) or (001) superlattice satellites as a function of annealing time. In a model system, where the interdiffusion concentration independent, the log of the superlattice satellite decay rate is linearly proportional to the interdiffusion. Typically, a straightforward analysis of this type is not possible with SiGe because the interdiffusion is a strong function of Ge concentration. We show that by using Si$_{1-x}$Ge$_x$/Si$_{1-y}$Ge$_y$ superlattices with an as-grown composition amplitude of less than 2% and 2% Ge concentration we can extract the interdiffusion as the film's mean composition. The activation enthalpy is determined by performing these experiments by inert gas annealing at several different temperatures.

D6.7 INVESTIGATING THE CHANNEL LENGTH NON-UNIFORMITY AND VARIOUS IMPURITY STRUCTURES OF SEMICONDUCTOR DEVICES USING AFM/SCM.


Atomic force microscopy and scanning capacitance microscopy (AFM/SCM) have been applied to study various implant structures of semiconductor devices. In this work, two types of semiconductor devices, Si based and GaAs based, were studied. Many researchers have used AFM/SCM to study cross-sectional semiconductor devices to obtain the dopant profiles in the source and drain regions and further determine the channel length. While the width of the gate has been shrinking to below 0.13μm, the length of the gate has not. Therefore, channel length determined from a cross-sectional view may not be representative. AFM/SCM has been used to study a Si device directly from the top, and the channel length of this device was found to be non-uniform in the SCM image. A similar direct top-down AFM/SCM study for GaAs devices has also been applied to a GaAs device. In these cases, the lateral diffusion length of dopants after a thermal annealing process was evaluated. A GaAs substrate is masked and patterned by a layer of SiN$_4$, then Zn dopants are thermally diffused through a line-opening in the nitride layer into the substrate. By observing the AFM/SCM image on top of the SCM image, the lateral diffusion length of the Zn dopants is found to be about 2.2μm from the edges of the exposed GaAs region. Another important application of AFM/SCM is
in device failure analysis by directly comparing a failed device with a properly functioning one in order to identify the cause of failure. AFM/NCM modes helped to study the same N-well structures in two devices, one good and the other failed, and the depth of the N-well for the failed device is found to be about 0.4 µm thinner than in the good device.

D6.8 PHYSICS-BASED SIMULATION OF PROCESSING OPTIONS FOR PRE-AMORPHIZED ULTRA-SHALLOW JUNCTIONS: Nini I., Czochralski Si doped with As up to 10^20 cm^-3 [1]. By studying the annihilation of V - As pairs formed by electron implantation, we found that the V - As concentrations are far higher than that predicted by the Shockley model. The vacancy-impurity complex in Czochralski Si doped with As up to 10^20 cm^-3 [1].

D6.9 SHALLOW JUNCTION FORMATION BY ARSENIC OXIDE DIFFUSION FROM IMPLANTED ARSENIC OXIDE: Omer Dokumaci, Paul Reinhart, Sagi Horev, IBM SRC, Hopewell Junction, NY.

As the devices are scaled down, shallower junctions are needed to prevent short channel effects in sub-0.1 µm devices. We investigated arsenic-oxide diffusion with implanted oxides to form ultra-shallow junctions. A layer of oxide was grown on silicon with an RTA process. The oxide thicknesses were 15A, 35A, and 75A. 15A oxide thickness served as a control. After arsenic implantation with E=1keV, the oxide was implanted with energies between 100keV and 5keV at a dose of 1x10^15 cm^-2. The samples were then annealed in an RTA system between 950°C and 1050°C for various times. Implanted and annealed arsenic profiles were obtained by SIMS. For the 1keV implant, more than half of the implanted arsenic was found to be in the oxide for the 35A oxide sample. When this sample was annealed, nearly all of the arsenic came out of the oxide into silicon. This is the first time such an enhanced diffusion of arsenic through the oxide is observed. We believe that the enhanced diffusion is caused by the implant damage created in the oxide. For the 1keV implant into 75A oxide, only a small amount of arsenic actually diffused out into silicon. In this case, arsenic peaks were further away from the oxide/silicon interface so that the enhanced diffusivity in the oxide was not enough to diffuse out the arsenic into silicon. All the results were in agreement with our simulations which take into account the enhanced diffusivity in the oxide.

D6.10 VACANCY-ARSenic COMPLEXES IN highly n-type SI: Identification, Formation Mechanisms, and Role in the Deactivation of Doping, W. Runki and K. Snarsen, Helsinki University of Technology, Laboratory of Physics, Helsinki, FINLAND; J. Pae-Pedersen, J. Lundgaard Hansen, A. Nylandsted Larsen, University of Aarhus, Institute of Physics and Astronomy, Aarhus, DENMARK.

The detailed atomic structure of vacancy-impurity complexes present in highly doped n-type Si can be experimentally determined using positron lifetime and electron momentum distribution measurements [1]. The monovacancy surrounded by three As atoms in the dominant vacancy-impurity complex in Czochralski Si doped with As up to 10^20 cm^-3. By studying the annihilation of V - As pairs formed by electron implantation, we found that the V - As concentrations are far higher than that predicted by the Shockley model. The vacancy-impurity complex in Czochralski Si doped with As up to 10^20 cm^-3.

D6.11 EVIDENCE FOR A NEW DEFECT IN HIGHLY n-TYPE Si FROM ATOMIC-PRECISION RESOLUTION CHANNELING EXPERIMENTS ON INDIVIDUAL DONOR ATOMS: P. M. Vogley, Materials Science and Engineering Department, University of Wisconsin-Madison, Madison, WI; D. Chadi, NEC Research Institute, Princeton, NJ; P. H. Citrin, D. A. Miller, J. L. Granul, P.A. Northrup, Bell Labs, Lucent Technologies, Murray Hill, NJ; H. J. L. Gosman, Agere Systems, Berkeley Heights, NJ.

Channeling experiments performed in a scanning transmission electron microscope with single dopant atom sensitivity and resolution show that neither a vacancy-centered cluster nor a donor pair can be the shallow defect responsible for the saturation of the carrier density as a function of dopant concentration in n-type Si. We propose a new defect, D1/V[n-1] which consists of a donor pair and a Si vacancy-interstitial pair. This model is consistent with our measurements, has enough free volume to reconcile recent positron annihilation measurements, and explains the observed behavior of the charge carrier density versus dopant concentration.


Studies of dopant and self-diffusion in isotopically controlled silicon heterostructures involving extrinsic boron and arsenic doping have yielded new, quantitative information on the contributions of native point defects to self-diffusion in silicon. As a result of the Fermi level shift under extrinsic conditions, these studies have provided new information on the roles of singly charged self-interstitials (I^+) and negatively charged vacancies (V^-) in diffusion. We present experimental results of dopant and self-diffusion in an isotopically controlled silicon heterostructure with arsenic and phosphorus. As a consequence of extrinsic n-type doping, the concentration of singly negatively charged native point defects is enhanced. However, diffusion of phosphorus is known to cause a superposition of self-interstitials and thereby an underestimation of vacancies. This suppresses the impact of vacancies in the simultaneous diffusion of phosphorus and self-atoms. As a consequence the change states of self-interstitials in the diffusion process can be determined. Multilayers of isotopically controlled 28Si and natural silicon enable simultaneous analysis of 28Si self-diffusion into the 28Si enriched layers and dopant diffusion throughout the multilayer structure. An approximate 28Si thickness of 200 nm was deposited in a multilayer structure. Phosphorus ions were implanted to a depth such that all the radiation damage resided inside the amorphous cap layer. These samples were annealed for different times and temperatures. After diffusion the phosphorus profiles were recorded by means of secondary ion mass spectrometry. Modeling of the diffusion profiles provides information about the point defects mediating phosphorus diffusion and about their diffusion properties for various extrinsic n-type conditions. A complete set of diffusion properties for various extrinsic n-type conditions.

In this work we investigate the diffusion and the electrical activation of In atoms implanted in silicon with different energies, in the range of 4-8keV, with doses between 5 x 10^{11} cm^{-2} and 5 x 10^{13} cm^{-2}, after rapid thermal processing. Our investigation shows a clear dependence of In out-diffusion and electrical activation on the implant depth, being the electrically active fraction higher with increasing the implant depth. We propose that the data can be explained considering the balance between the local In concentration and the C background. The occurrence of coupling between the C present in the implantation and the diffusion, depending on the C/In ratio, may in fact give rise to a significant formation of In-C complexes. Such complexes play a role in the enhanced electrical activation due to the shallower level they introduce into the Si band edge (E_c+0.111eV), with respect to the rather deep level (E_c+0.156eV) of the interaction of In with the SiC lattice inside the silicon substrate has been therefore identified as the most likely origin of this behaviour. In and Co-implantation has also been studied within this work, in order to further investigate the key role of C in the increase of the electrical activation. A large increase of the electrical activation has been detected in the co-implanted samples, up to a factor of about 8 after annealing at moderate temperatures. However, C precipitation occurs at 1100°C, with drastic effects on the carrier concentration that falls down by orders of magnitude. This gives a limitation to the maximum thermal budget to be used for In activation in C co-implanted material.

D6.14

Fluorine co-implantation with boron in silicon has garnered interest due to its demonstrated ability to reduce the transient enhanced diffusion of boron during post-implantation annealing. In addition to significantly reducing the diffusion of boron in silicon during post-implantation rapid thermal annealing (RTA), the presence of fluorine is observed to change the behavior of boron both in the as-implanted state and during low temperature annealing for small phase mismatch growth. The diffusion behavior of boron in each case is characterized by secondary ion mass spectrometry (SIMS). The presence of fluorine is observed to induce room temperature diffusion of boron during ion implantation. Correlation of the effects of fluorine and hydrogen in silicon are investigated by direct comparison of co-implantation of each species into pre-amorphized silicon with low energy boron implants. It is shown that the demonstrated fluorine effects are consistent with the hypothesis that fluorine interacts with silicon lattice vacancies by passivating unbounded silicon orbitals both in crystalline and amorphous silicon. The evolution of the amorphous layer thickness of samples after implantation and subsequent annealing is monitored by variable angle spectroscopic ellipsometry (VASE) and cross-sectional transmission electron microscopy (XTEM). Application of the findings to the challenges encountered in the formation of ultra-shallow junctions, particularly reduction of junction depth without degradation of junction abruptness, will also be discussed.

D6.15
MODELING THE EFFECT OF FLUORINE ON BORON AND PHOSPHORUS. Milan Diebel, Univ of Washington, Dept of Physics, Seattle, WA, Srinivasan Chakravarthi, Charles F. Madland, Shashikant Elkote, Amitabh Jain, Silicon Technology Development, Texas Instruments, Dallas, TX; Scott T. Dunham, Univ of Washington, Dept of Electrical Engineering, Seattle, WA.

Implanted fluorine [F] has been observed to behave unusually in silicon, manifesting an apparent updiffusion. Experimental data show that F can enhance as well as retard boron (B) and phosphorus (P) diffusion depending on the implant conditions. Based on previous presented ab-initio calculations [M. Diebel and S.T. Dunham, Mater. Res. Soc. Symp. Proc. 717], which explain the monomolecular fluorine diffusion behavior, a comprehensive model is developed which explains the different effects of fluorine on B and P under sub-amorphizing and amorphizing conditions. Ab-initio calculations find no significant binding energies between B and F. Instead, the different effects of fluorine on dopants are primarily due to fluorine point-defect interactions. The formation and dissolution of fluorine vacancy clusters alter the local point-defect concentrations and therefore can enhance or retard the P diffusion depending on the implant conditions. A comprehensive continuum model was implemented and compared to experimental data. Fluorine enhances B and P diffusion under sub-amorphizing conditions and retards in amorphized environments. The model is also capable of predicting the fluorine effect on B and P in cases where the dopant concentration is divided by amorphous-crystalline interface in a sub-amorphous and amorphous portion.

D6.16
DIFFUSION OF BORON AND SILICON IN GERMANIUM AND Si$_{1-x}$Ge$_x$ (x>50%) ALLOYS. Suresh Upadhya, Arthur F.W. Willoughby, Materials Research Group, University of Southampton, Janet M. Boros, Dept of Electronics and Computer Science, University of Southampton, Southampton, UNITED KINGDOM.

Diffusion engineering in combination with ultra shallow junctions using ion implantation has shown great potential for improving the performance of existing MOSFET devices. On material front, strained Si, Si$_{1-x}$Ge$_x$ and Ge layers grown on Si$_{1-x}$Ge$_x$ (y>x) virtual substrates are prospective candidates especially for p-type MOSFET [1]. In this paper, diffusion of boron implanted into the strained Si$_{1-x}$Ge$_x$ with elevated source/drain p-MOSFET has also been suggested [2]. In this work, boron diffusion has been studied in germanium and Si$_{1-x}$Ge$_x$ (x>50%) alloys using ion implantation and high resolution secondary ion mass spectroscopy (SIMS). Effect of variation in implantation dose and energy has been investigated. A significantly low diffusivity of boron in Ge contrary to previously reported values has been observed. Si diffusion studies have also been carried out in Ge utilizing ion implantation, furnace annealing and SIMS. The results are discussed from the viewpoint of mechanism responsible for B and Si diffusion in Ge, Si$_{1-x}$Ge$_x$ alloys. Boron diffusion studies are being carried out using epizone growth in order to avoid implantation damage effects. References [1] M.L. Lee, C.W. Leitz, Z. Cheng, A.J. Pitera, T. Lungo, M.T. Currie, G. Travelli, E.A. Fitzgerald, Appl. Phys. Lett., 70, 3344, (2002); [2] P. Romele, H. Takeuchi, V. Subramanian, Tso.Joe King, IEEE Electron Device Letters, 23, 218, (2002).

D6.17
MULTISCALE COMPUTATIONS OF B DIFFUSION IN SiGe. Liguu Wang, Cheruwa S. Murphy*, and Paulette Clancy, School of Chemical and Biomolecular Engineering, Cornell University, Ithaca, NY, IBM Semiconductor Res. & Dev. Center (SRDC), Microelectronics Division, Hopewell Jct, NY.

Device scaling has been driving the integrated circuit (IC) microelectronics revolution for over three decades. One of the critical elements in device scaling is the junction depth (and, now, the extension junction depth), pushed to 25 nm in the 2001 International Technology Roadmap for Semiconductors (ITRS). The scaling is not straightforward since the monomolecular boron diffusion in the post-implantation heating processes poses severe challenges to the formation of ultra-shallow junctions. To reduce the diffusion of boron, other species, e.g., Ge, N, are incorporated into the Si substrate, dramatically reducing the diffusivity of boron (e.g., a factor of 6 in Si$_{1-x}$Ge$_x$ relative to Si). Experimental evidence tends to be indirect, hence the atom-scale migration mechanisms and paths of the boron diffusion in SiGe alloys are not understood yet. The energetics of boron diffusion in Si$_{1-x}$Ge$_x$ can be quantitatively studied with ab-initio calculations. Using the linear, basis-independent Density Functional Theory (DFT) code, DFT++, developed by T. Arias at Cornell University, we are investigating the mechanism that retards boron diffusion in SiGe. Initial results show that stress compensation plays a major role in the boron diffusion in SiGe, contrary to some expectations. Placing a neutral B atom and a Ge atom in close proximity does not lead to an energetically favorable configuration. The energetics of defects involving B and Ge atoms suggest that substitutional boron atoms find it difficult to be “kicked out” by an interstitial Ge atom or to diffuse past a nearby Ge. Larger-scale empirical Stillinger-Weber models show that the preferred interstitial positions and trapping mechanisms of B are different in Si and SiGe. In Si, an initially interstitial boron quickly diffuses to a lattice Si atom and occupies a substitutional site for “long” periods. In contrast, in SiGe an initially interstitial boron in Si$_{1-x}$Ge$_x$ becomes “trapped” for “long” periods in an interstitial position between two substitutional Ge atoms.

D6.18
BORON SEGREGATION AND OUT-DIFFUSION IN SINGLE-CRYSTAL Si$_{1-x}$Ge$_x$. Eric Stewart, James Sturm.

Boron and carbon diffusion in Si$_{1-x}$Ge$_x$C$_y$ and Si$_{1-x}$Ge$_x$ alloys is important to understand for integrating these materials into both MOSFET and HBT devices. Previously, it has been shown that boron segregates into single-crystal Si$_{1-x}$Ge$_x$ [1] and even more strongly into polycrystalline Si$_{1-x}$Ge$_x$C$_y$ [2]. In this work, we report that both boron and carbon segregate into Si$_{1-x}$Ge$_x$C$_y$. We also find that when most of the carbon is removed from the thin Si$_{1-x}$Ge$_x$ layer by
oxidation-enhanced out-diffusion, boron that had previously segregated to the layer can diffuse away as well. Models to explain these effects will be presented, as well as the effect of boron on carbon diffusion. All structures were grown by RTPVD at 625°C and 750°C, using SiC,H and Si:H as carbon sources and SiC,H and B:H as carbon and boron sources, respectively. The test structure used for this study consisted of an undoped, 20 nm SiC film, 100 nm SiC film sandwiched between thicker boron-doped (B) = 2 x 10^19 cm^-3) Si layers, on an n-type substrate. The SiC, 200 nm layer was positioned 50 nm below the surface of the sample. A two-step anneal was performed: the first step was an 850°C, 2 hour N₂ anneal to allow boron to move into the SiC, 200 nm layer. SIMS profiles taken after this anneal show that boron segregates into the SiC, 200 nm layer with a segregation coefficient of 1.8. The second anneal was an 850°C anneal. The test structure used for this study consisted of an undoped, 20 nm SiC film, 100 nm SiC film sandwiched between thicker boron-doped (B) = 2 x 10^19 cm^-3) Si layers, on an n-type substrate. The SiC, 200 nm layer was positioned 50 nm below the surface of the sample. A two-step anneal was performed: the first step was an 850°C, 2 hour N₂ anneal to allow boron to move into the SiC, 200 nm layer. SIMS profiles taken after this anneal show that boron segregates into the SiC, 200 nm layer, with a segregation coefficient of 1.8. The second anneal was an 850°C anneal. A previous study has shown that, for a similar structure and anneal time, oxidation-enhanced diffusion allows all of the carbon to diffuse out of the SiC, 200 nm layer [3]. SIMS profiles of our samples show the same effect, most of the carbon is removed from the SiC, 200 nm layer after the boron that had previously segregated to the layer diffuses away as well. Models to explain the initial boron segregation include: i) B C or B:Si defect complex formation, or ii) point defect gradients caused by the local interstitial undersaturation in the SiC, 200 nm layer. The ability of both carbon and boron to out-diffuse during the oxidation indicates that immobile B:Si defects are not responsible for the boron segregation, favoring the point defect gradient model. This work was supported by DARPA and ARO. 1. S. M. Hu, D. C. Ahlgren, P. R. Rasloukh, and J. O. Chu, Physical Review Letters, vol. 67 (11), p. 1450-1453 (1991). 2. E. J. Stewart, M. S. Carroll, and D. C. Sturm, MRS Symposium Proceedings, vol. 290 (2001), 3. M. S. Carroll, D. C. Sturm, E. Napoleon, D. De Salvador, M. Berti, J. Stainl, G. Bauer, and D. J. Tweet. Physical Review B, vol. 64, 073308 (2001).

**D6.10** PROCESS OPTIMIZATION FOR MULTIPLE-PULSE LASER ANNEALING OF BORON IMPLANTED SILICON WITH GERMANIUM PRE-A-MORPHIZATION. Debora Poon, Duong Pham, Yong Song, Dong Soo Kang, and Sang Hui Lee, Silicon Nano Device Laboratory and Laser Micro-Processing Laboratory, National University of Singapore, SINGAPORE; Mosiwa Bheza, Alex See, Technology Development Department, Chartered Semiconductor Manufacturing, SINGAPORE.

One of the major advantages of multiple-pulse Laser Thermal Annealing (LTA) with moderate energy fluence is that good dopant activation can be achieved without further increases in junction depth by successive pulses. This paper presents the ability to predict the number of laser pulses required to anneal an initially amorphous layer to obtain a defect-free single crystal for different preamorphized layer depths. In addition, a method to separate the reason behind sheet resistance reduction upon multiple laser pulses, into either increased dopant activation, defect annealing or both without the need for further High Resolution Transmission Electron Microscopy (HR-TEM) analysis is also proposed. Wafer are implanted with germanium to form amorphous layers of varying depths, closer to but not on the surface. This is followed by a 0.5 keV boron implantation. The samples are then LTA processed with varying number of pulses and energies ranging from below melt to the energy density required to fully melt the Preamorphization Impairment (PAI) layer. It is demonstrated that when the laser fluence is adjusted to a value that can melt the PAI layer but not the underlying silicon substrate, PAI layer depths control the junction depth. Hence, it is desirable to operate LTA in the PAI regime for a higher process control as opposed to when the junction depth is controlled solely by the laser fluence. HR-TEM micrographs show that with single-pulse LTA at such an energy fluence, although damage in thin amorphous layers can be repaired, the defects in thick amorphous layers are not annealed out effectively, giving rise to microtwins and polycrystalline formation. Our study allows for the prediction, from four-point probe measurements, the maximum allowable PAI depth for a given number of pulses in order to fully remove the damage caused by the PAI.

**D6.20** Abstract Withdrawn.

**D6.21** FORMATION OF NSI SILICIDED P⁺ SHALLOW JUNCTIONS USING IN SITU IMPURITY CONVERSION. M. P. Annamalai, Min-Chuan Wang, Chiao-Ju Lin, and Mac Chih Chen, Department of Electronics Engineering, National Chiao-Tung University, Taiwan.

NSI-silicided p⁺ shallow junctions are fabricated by using BF₂⁺ implant into thin NSI silicide layer (ITS technology) followed by low temperature furnace annealing (from 550 to 800°C). The NSI film agglomerates following a thermal annealing at 600°C, and may result in resistive islands at high temperature. The incorporation of fluorine atoms in the NSI film can retard the formation of film agglomeration and thus improving the film’s thermal stability. The forward ideality factor of about 1.02 and the reverse current density of less than 1.0 A/cm² can be obtained on the NiSiSi₃/10/5/F⁺ junctions fabricated by BF₂⁺ implantation at 35 keV to a dose of 5 x 10¹⁵ cm⁻² followed by a 650°C thermal annealing; the junction formed is about 80nm measured from the NiSiSi₃ interface. Activation of the implanted p⁺ junctions is dominated by the diffusion current, indicating that most of the implanted damage can be recovered after annealing at a temperature as low as 650°C.

**D6.22** Abstract Withdrawn.

**D6.23** THE IMPROVED THERMAL STABILITY OF NICKEL SILICIDE FILMS BY NICKEL AND TANTALUM ALLOY. Dongwon Lee, Kihoon Do, Dong Chul Shin, Dae-Hong Ko, Yongsun Univ., Dept. of Ceramic Engineering, Seoul, KOREA; Je-Hun Ku, Yongshoon Choi, Process Development Team, Samsung Electronics Ltd., KOREA; Cheol-Woong Yang, Sungkyunkwan Univ., School of Metallurgical and Materials Engineering, Suwon, KOREA.

The formation and the thermal stability of Nickel silicide film with pure Ni and Ni-Ti alloy has been investigated for the application to the ULSI device. A comparative study of the silicidation with Ni film and Ni-Ta alloy films deposited on the single crystal Si(100) substrate has been performed by using Rapid Thermal Process (RTP). After silicidation process with different RTP temperature, we measured the sheet resistance of Ni/Si and Ni+-Ta/Si system with different composition of Ta. With addition of Ta system, the sheet resistance become more stable than pure Ni silicide in high RTP temperature range. Moreover, we analyzed the microstructure of the interface by using TEM and phase transition with XRD. Corresponding to the results of sheet resistance, Ni-Ta/Si system shows an improved thermal stability and microstructure than Ni/Si system in higher RTP temperature range. These results show the improvement in the thermal and morphological stability of nickel silicide in case of Ni-Ta/Si system. Therefore, Ni-Ta/Si system, at 500°C, sheet resistance are maintained for 120 hour long time annealing at 600°C. But, the sheet resistance increase with increasing of annealing time due to formation of NiSi₂ in Ni/Si system. After annealing of Ni_xx Ta_yO_x/SiO_x/Si and Ni_xx Ta_yO_x/Si/Ni system at 500°C, we etching at 850°C was done by H₂SO₄/H₂O₂ solution. No formation of silicide and the unreacted metal alloy films on dielectric materials after etching. Through TEM image, there is no residue left on the dielectric materials. Therefore silicide is expected to be selectively grown on poly-Si lines and bulk Si.

**SESSION D7: LASER ANNEALING AND SILICIDE PROCESSES**

**Chair: Bin Yu**

**Thursady Morning, April 24, 2008**

**Golden Grace C2 (Marriott)**

**8:30 AM • D7.1**

**ULTRA-SHALLOW JUNCTION FORMATION BY EXCIMER LASER ANNEALING OF ULTRA-LOW ENERGY B IMPLANTED IN Si, G. Ferretti, and L. Marroccoli, CNR-IFN. Rome, ITALY; V. Privitera, S. Wieland, A. La Magna, G. Mannino, M. Italic and C. Bossi, CNR-IMM. Cernusco, ITALY.

Formation of ultra-shallow junctions by excimer laser annealing (ELA) of ultra-low energy (1keV - 200eV) B implanted in Si has been investigated. High resolution TEM has been used to assess the as-implanted damage and the crystal recovery following ELA. The electrical activation and redistribution of B in Si during ELA has been studied as a function of the laser energy density (melt depth), the implant dose and the number of laser pulses (melt duration).

Under appropriate ELA conditions, ultra-shallow profiles, extending to a depth as low as 25nm with an abrupt profile (2.5nm/dec), have been achieved. The activated and retained dose has been evaluated with spreading resistance profiling and SIMS. A significant amount of the implanted dopant was lost from the sample following ELA. However, the dopant that was retained in the crystal material was fully activated following rapid re-solidification. The electrical activation was increased for high laser energy density annealing, when the dopant was redistributed over a deeper range. We developed a theoretical model, that considers the dopant redistribution during melting and regrowth, showing that the fraction of the implanted dopant not activated during ELA was lost from the sample through out diffusion. The lateral distribution of the implanted B following
Laser annealing has been studied with 3D measurements, using selective etching and cross-section TEM on samples where the implanted dopant was confined with carbon and Pt. The results show that there is substantial lateral diffusion of B under the oxide mask when melting occurs in this region while, if melting under the oxide mask is prevented, the implanted B close to the oxide mask edge was not activated by ELA. The results have been explained by numerical heat-flow calculations and it is concluded that lateral diffusion can be controlled by the oxide mask thickness.

9:00 AM *D7.2
LASER ANNEALING FOR JUNCTION FABRICATION IN CMOS DEVICES. Samit Talukder, Yan Wang, Veridian Technologies, San Jose, CA; Marjorie Thompson, Cornell University, Department of Material Science, Ithaca, NY.

Conventional rapid thermal annealing has evolved to shorter times and higher temperatures to limit transient enhanced diffusion and improve dopants activation. Current spike annealing technologies achieve sub-100 milliseconds exposures near the peak temperature. On the other extreme, laser thermal processing achieves activation in the nanosecond timescale, but requires surface melting and additional layers to address geometry issues. Ion implantation damage annealing and dopant activation for ultra shallow junctions using laser annealing has been explored in the well known melt and solid phase annealing technique by total helium times of microseconds. Low energy boron, phosphorus and arsenic implanted samples were cycled with peak temperatures up to the single crystal melting point using either a single laser cycle or multiple cycles for increased throughput at the same temperature. Activation of all three dopants was achieved with minimal dilution. Defect evolution and annealing time limitations and mechanisms have been investigated by SIMS, TEM, and in-situ probes. Preliminary results suggest that this type of annealing can readily achieve the 20 nm ultra shallow junctions required for the 65 nm NTRS node.

9:30 AM D7.3

According to the International Roadmap for Semiconductors (ITRS), the doping technology requirements for the MOSFET source and drain regions of the future CMOS generations lead to a major challenge. A critical point of this evolution is the formation of ultra shallow junctions (USJ) for which present technologies, based on ion implantation and rapid thermal annealing, will hardly meet the ITRS specifications. Laser Thermal Processing (LTP) has been shown to be a potential candidate to solve this fundamental problem. In the present paper, LTP experiments have been performed using a 10 Hz Laser with 308 nm wavelength, with different pulse characteristics. The first laser (Lambda Physik, Complex 102) delivers 200 mJ laser pulses with a duration of μs μs. The second laser is an industrial tool (SOPRA, VEL 15) that delivers 15 J laser pulses with a duration of μs and allows to anneal a few cm cm in a single laser shot. Here we compare the influence of the pulse duration on LTP of B with and without Ge pre-amorphization and BF 2 with implanted silicon samples on the basis of real-time optical monitoring of the laser induced melting/ recrystallization process, four-probe resistance measurements, secondary ion mass spectrometry (SIMS) depth profiles. Experimental results are compared to model calculations developed in the framework of an industrial software (FIDAP) with pulse characteristics of the laser pulses. The realized dopant dose, junction depth and sheet resistance, as a function of the laser fluence and shot number for both lasers, confirm the efficiency of laser processing to realize ultra shallow and highly doped junctions required for the future CMOS generations. Influence of the pulse duration on the USJ formation process is also discussed.

9:45 AM D7.4
A COMPARISON OF SPIKE, FLASH, SPER AND LASER ANNEALING FOR 45nm CMOS. Richard Lindsey, K. Henson, Wilfried Vanderwerv, Karen Mes, IMEC, Leuven, BELGIUM; Bartek J. Pawel, Radu Sandu, Peter Stolk, Philips Research, Leuven, BELGIUM; Jorge Kitto, Aplis Researcher in IMEC from Texas Instruments; Cristian Torregrossi, Giorgio Baracchi, Master’s Stage at IMEC from University of Pavia, ITALY; Khalid Maimur, Applied Materials, Santa Clara, CA, Jonathan Ross, Steve McCay, Jeff Geley, Keyence Vortex Technologies, Warrington, CANADA; Xavier Pages, ASM Belgium, Leuven, BELGIUM.

Due to integration concerns, the use of metalohxide junction formation processes such as laser annealing (LTA), solid phase epitaxy regrowth (SPER), and flash annealing has largely been avoided for the 65nm CMOS node. Instead fast-ramp spike annealing has been optimized along with co-implantation to satisfy the device requirements, often with help from thin oxide spacer. However for the 45nm CMOS node it is widely accepted that this conventional approach will not provide the required pMOS junctions, even with changes in the transistor architecture. In this work, we will compare junction performance and integrability of fast-ramp spike, flash SPER and laser annealing for 45nm CMOS. The junction depth, abruptness and resistance offered by each approach are balanced against non-uniformity, density of defects. Results show that the main contenders for the 45nm CMOS are SPER and flash annealing but both have to be rigorously optimized for regrowth rates, amorphous positioning and dopant and co-implant profiles. From the two, SPER offers the best junction abruptness (15nm) with leakage at the limit of the reference technology (1.3mA/μm2), while the flash anneal has the better of solid solubility (8%2/m) and less transistor modifications. As expected, Ge and P for implantation into advanced CMOS 45nm. For full-melt LTA, poly deformation on isolation can be reduced but geometry effects result in unacceptable junction non-uniformity. The merits of SPER and flash annealing are discussed.

10:15 AM D7.5
SILICIDES FOR 55 NM CMOS AND BEYOND. Jorge A. Kitti1, Anne Lewans, Omer Chamirian, Mark Van Dal, Armin Abkhezy, Muriel de Potter, Richard Lindsay and Karen Mesi2, IMEC, Leuven, BELGIUM; “Texas Instruments” IMEC Affiliated Researcher, IMEC2; IMEC and EE Department, KU Leuven; Philips Research Leuven; Infineon Technologies (Affiliated researcher at IMEC).

As CMOS scaling ventures into the 65 nm node and beyond, with gate lengths decreasing from 40 to 25 nm and below and junction depths well below 100 nm, the constraints for silicidation processes result in new and harder challenges. As Co-silicide, the industry’s choice for previous nodes, suffers from long heat budgets, the emphasis in development has switched towards alternative materials. This paper presents an overview of silicide development activities at IMEC for the 65 nm node and beyond, with emphasis on Ni silicide as well as in Co-based and Ni based alloy silicides (such as CoNi and NiP). Fundamental aspects of the silicidation reactions are reviewed, such as the reaction kinetics, mechanism of thermal degradation, effect of alloying elements and thickness scaling as well as their implications for implementation into advanced CMOS 65 nm. The effect of non-uniformity, dopants and alloying elements (such as Ge) are also addressed as well as the impact of processing variables and device geometry on parameters such as narrow line sheet resistance, dielectric leakage and contact resistivity.

10:45 AM D7.6
NEW METHOD OF CoSILICIDE FORMATION USING Co/CoTi Ti:SiN NITRIDE-CAP PROCESS: Tecnol, Institute Inoru, Fujitsu VLSI Ltd., Mie, JAPAN; Takahiro Kuroda and Akira Takeshima, Fujitsu Ltd., Mie, JAPAN; Shigeo Koshima, Fujitsu Laboratory Ldt., Konagawa, JAPAN.

In the fabrication of ultra large-scale integrated (ULSI) circuits, cobalt silicide has been used for reducing the parasitic resistance of polysilicon-gate and source/drain area. As the conventional co-silicide process, Co/TiN cap deposition is used at the recent process. However, the conventional process makes bad morphology of CoSi2 due to agglomeration, result in the increasing of junction leakage current. In order to improve these problems, we studied the new cobalt-silicide process using Co/CoTiN-TiN cap deposition with TiN-cap. This Co/CoSi-TiN alloy stack process obtain better uniformity, lower resistance and lower Junction Leakage current at thickness ratios: 1 (50nm Co and 50nm CoTi alloy stack) compare with conventional Co/CoSi-TiN cap process. TiN cap process with Co/CoTiN-TiN cap process is confirmed to exist highly Ti Concentration at the CoSi2 surface. On the other hand, Co/TiN cap and Co/CoSi/TiN cap process are good uniformity of Ti concentration, and Co/CoSi/TiN cap process is fifty times higher concentration compare with Co/TiN cap process. We conclude that the difference in the Ti concentration can affect the morphology, and the high concentration of Ti is effective for suppressing the agglomeration of CoSi2, and the junction leakage current. According to improve the uniformity of Ti concentration in CoSi2, Ti uniformly diffuses into CoSi2 grain boundary. We proposed that the relationship between the Ti behavior in CoSi2 and the junction leakage current due to agglomeration.

11:00 AM D7.7
LOW RESISTIVITY NICKEL AND PLATINUM GERMANO-SILICIDE CONTACTS TO ULTRA-SHALLOW JUNCTIONS.
FORMED BY SELECTIVE CVD SGI TECHNOLOGY FOR NANO SCALE CMOS. Jing Liu, Hongxing Mu, Mehmet C. Ozturk, North Carolina State University, Department of Electrical and Computer Engineering, Raleigh, NC.

One of the key challenges for future CMOS technology nodes is to form source/drain junctions with very low contact resistivity. This requires fundamentally new junction and contact formation techniques to produce ultrathin junctions with super abrupt doping profiles, above solid solubility, dopant activation and contact resistivity values below 10-8 cm-2. Recently, this laboratory reported a new technology based on selective deposition of heavily doped SiGe alloys in source/drain regions isothermally etched to the desired depth. Of particular interest to this paper is the smaller bandgap of SiGe resulting in a smaller metal-semiconductor barrier height, which is a key advantage in reducing the contact resistivity. In this paper, we present recent results on Pt and Ni germanosilicide contacts formed on boron and phosphorus doped SiGe alloys. The contacts were formed by sputter deposition of 10-30 nm thick Ni and Pt layers followed by rapid thermal annealing in nitrogen. Our results show that both Ni and Pt germanosilicide contacts can provide contact resistivity near 10-8 cm-2 on boron doped SiGe. On phosphorus doped SiGe, Ni germanosilicide can yield a low contact resistivity near 10-7 cm-2. However, the contact resistivity obtained with Pt germanosilicide is substantially higher possibly due to the Pt germanosilicide Fermi-level being closer to the valence band. The thermal stability of Ni germanosilicide was found to be limited to approximately 500°C for 30 min. On the other hand, Pt germanosilicide is stable up to 800°C. We have also shown that the thermal stability and film morphology of Ni germanosilicide could be improved using a thin Pt interlayer without sacrificing the sheet or contact resistance values. Using this approach, we have shown that high quality germanosilicide contacts that satisfy the requirements of future CMOS technology nodes can be formed on boron and phosphorus doped SiGe alloys.


NiSi formation in Ni(55%)/SiO2/Si system was investigated. p-type 16.15 g/cm3 (100) Si wafers were used in this study. A thin layer of silicon oxide ~12 Å was grown on some of the wafers using Shinkai cleaning process. Pure Ni and Ni(55%)/Si alloy films of thickness ~300Å were then deposited on all wafers by sputter deposition (co-sputtering of Ni and Ti was used for Ni(55%)/Si alloy film deposition). The concentration of Ti in the Ni(55%)/Si alloy films was measured by Rutherford back scattering (RBS). Rapid thermal annealing (RTA) silicidation was performed in N2 ambient for 60 s at different temperatures. Four probes, X-ray diffraction (XRD), secondary ion mass spectroscopy (SIMS) and cross-sectional transmission electron microscopy (XTEM) were used for monitoring silicidation reaction processes. For the Ni(55%)/SiO2/Si system, it was found that the thin interfacial oxide (Shinkai oxide) is an effective diffusion barrier for Ni as no silicide formed in the Ni/SiO2/Si system up to 700°C. However, a drastic reduction in the ability of the interfacial oxide in blocking Ni diffusio was observed in the Ni(55%)/SiO2/Si system. For example, in Ni(55%)/SiO2/Si system, it was found that the NiSi forms at temperatures as low as 400°C. The observation of NiSi formation at much lower temperatures in the Ni(55%)/SiO2/Si system compared to the Ni/SiO2/Si system, is attributed to the formation of SiO2/TiO2 diffusion membrane by the reaction of Ti and interfacial oxide and resultant diffusion of Ni into underlying Si substrate. It is thought that NiSi may form directly in the Ni/SiO2/Si system, bypassing the Ni-rich Ni-Si phase, due to the much reduced Ni supply for silicidation reaction. It was also found that the NiSi/Si interface in the Ni(55%)/SiO2/Si system is more planar than that silicidation reaction occurred in Si/SiO2/Si/SiO2 system. It was also found that the NiSi/Si interface in the Ni(55%)/SiO2/Si system is more planar than that observed in NiSi/Si and Ni(55%)/SiO2/Si systems.

11:30 AM D7.9 PERFORMANCE OF PLATINUM SILICIDE LOW BARRIER SCHOTTKY CONTACTS. Guilhem Larue, Emmanuel Dubois, IRM / ENS / UM CNRS 6528, Villeneuve d’Asq, France.

One of the grand challenge imposed by CMOS down-scaling is the optimization of the source/drain (S/D) architecture, e.g., dopant activation above solid solubility, steep dopant profiling, low silicide specific contact resistivity. Recently, the concept of very low Schottky barrier S/D MOSFET has emerged as possible alternative to the conventional source/drain structure using highly doped S/D and mixed metal oxide contacts. For p-MOSFETs integration, platinum silicide is an excellent candidate because of its very low barrier to holes. This paper proposes a detailed study of the platinum silicidation reaction obtained by rapid thermal annealing (RTA) based on X-ray photoemission spectroscopy (XPS), transmission electron microscopy (TEM) and low-temperature-dependent current-voltage measurements. Using XPS analysis, it is shown that: i) an initial silicide layer is formed at room temperature, ii) three stable phases Pt, Pt3Si, Pt3Si can coexist providing to iii) the annealing ambience is strictly controlled to avoid the formation of a SiO2 barrier due to oxygen penetration through few nanometers thick platinum layers. Starting from an initial 15 nm thick Pt layer subsequently annealing at 400°C TEM cross-sections reveal that homogeneous 30 nm Pt/Si layers with a uniform grain size distribution are formed. Finally, current-voltage characteristics have been measured on a special test structure that accounts for the lateral disposition of S/D regions in a typical MOSFET architecture. It consists in two back-to-back Schottky contacts separated by a narrow silicon gap both on bulk silicon and silicon-on-insulator substrates. Based on temperature-dependent electrical measurements (Arrhenius plots), it is shown that in addition to thermionic emission, field emission is also involved in the current transport mechanism. An excellent current drive performance of 220 μA per micron width has been obtained for a 45 nm silicon gap on a 10 nm thick SOI substrate.

11:45 AM D7.10 LOW SCHOTTKY BARRIER ON n-TYPE Si FOR n-CHANNEL SCHOTTKY SOURCE/DRAIN MOSFETS. Megha Das, Dooshuk Uleskii, Shwaldha Agrawal, Nazar Eslami, Eduard Malenkov, and Wiley P. Kirk, NanoFab and Dept of Electrical Engineering, Univ of Texas, Arlington, TX.

Schottky source/drain structures in Si MOSFETs provide very shallow junctions, small series resistance, immunity to latchup, and simplified fabrication. They also have the potential to outperform bipolar-junction MOSFETs with their small internal capacitance and resistance. In fact, Schottky diodes have shown performance comparable to tunneling diodes and silicon diodes both with similar bandgap. The benefits of the n-channel Schottky barrier device is the fact that none of the common metals or metal silicides has a low enough barrier height (~0.2 eV) on n-type Si for a large drive current. Exotic materials, therefore, have to be used to obtain the right barrier height, such as erbium silicide that is readily oxidised in air, or tungsten germisilicide that introduces many more process parameters. A method to produce low Schottky barrier on n-type Si with common metals such as Al, Cr, and possibly Ti will be reported in this talk. The interface between metal and Si is engineered at the atomic scale to reduce interface states, and the engineered interface shows nearness to the classical and electronic processes at the interface. One consequence of this electronic nearness is that the Schottky barrier height is now more dependent on metal work function. Al, Cr, and Ti all have work function very close to the conduction band of Si. It has been shown that the Schottky barrier of Al on engineered n-type Si (001) is 0.1 eV, and that of Cr is 0.25 eV. These numbers are significantly different from the decades-old data on Schottky barrier height. Mg contacts on engineered Si (001) demonstrate that the interface is thermally stable up to at least 750°C. These results bring new hope for the future of n-channel S/D MOSFET/S with a metal commonly used in the semiconductor industry.