SYMPOSIUM E

Materials, Technology, and Reliability for Advanced Interconnects and Low-k Dielectrics

April 21 – 25, 2003

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TUTORIAL

ST E: CHALLENGES OF Cu/LOW-k INTERCONNECTS AND EMERGING TECHNOLOGIES BEYOND
Monday, April 21, 2003
9:00 a.m. - 5:00 p.m.
Salon 10/11 (Marriott)

The morning session will cover materials challenges and reliability issues. The tutorial will begin with the challenges and road map for low-k materials below k < 2.2. This will be followed by the thermomechanical reliability of low-k materials in die/package. Then, the electromigration reliability of Cu/low-k will be discussed.

The afternoon session will be dedicated to emerging technologies: 3-D interconnects and wafer-level packaging. It will start with an overview of the limitations in current interconnect paradigm and emerging technologies beyond Cu/low-k interconnects. This will be followed by two technical topics: (1) the potential of 3D system integration and (2) wafer-level packaging technologies.

Instructors:
Raymond Vrtis, Air Products and Chemicals, Inc.
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SESSION E1: ELECTROMIGRATION
Chairs: Jihperng (Jim) Leu and Paul S. Ho
Tuesday Morning, April 22, 2003
Golden Gate B2 (Marriott)

8:30 AM *E1.1
WHAT'S DIFFERENT ABOUT THE RELIABILITY OF Al-BASED AND Cu-BASED INTERCONNECTS? Carl V. Thompson, Massachusetts Institute of Technology, Dept. of Materials Science and Engineering, Cambridge, MA.

Cu has much lower grain boundary and lattice diffusivities than Al, and therefore, can, in principle, have much lower rates of electromigration and electromigration-induced damage. However, the reliability of integrated circuit interconnects depends on all aspects of the materials system used, not just the characteristics of the primary electronic conductor. Presently, Cu-based interconnection technology is based on a materials system in which diffusion at the interfaces of Cu interconnects occurs more rapidly than diffusion along grain boundaries. Coppers reliability advantage over Al is significantly reduced because of this. Also, current Cu-based technology leads to conditions under which the stress required to initiate failure of Cu, through void nucleation, is an order of magnitude lower than for Al. In addition, because a refractory metal layer that can shunt current around a void does not cap Cu, a much smaller void can cause failure in Cu than in Al. Furthermore, because the thin refractory metal liners at the base of Cu-based vias do not reliably block electromigration, a much larger fraction of the kilometers of Cu interconnect in an integrated circuit are susceptible to electromigration-induced failure than in Al-based systems. Finally, as diffusion barrier liners are made thinner, and low-k and low-modulus dielectrics replace high modulus dielectrics, leakage and extrusions become more likely. While Cu has the potential for providing the basis for a high-reliability metallization system, many aspects of the associated Cu metallization technology and materials systems must be changed to realize this needed reliability improvement.

9:00 AM E1.2
QUANTITATIVE CHARACTERIZATION OF DISLOCATION STRUCTURE COUPLING TO ELECTROMIGRATION IN A PASSIVATED Al (0.5wt% Cu) INTERCONNECT. R. Barabash and G. Ice, Oak Ridge National Laboratory, Metal and Ceramics Div., Oak Ridge, TN; N. Tamura, Advanced Light Source, Berkeley, CA; B. Valek and J. Bravman, Stanford University, Dept. Materials Science and Engineering, Stanford, CA; R. Spolenak, Max Planck Institut fuer Metallforschung, Stuttgart, GERMANY; J. Patel, Stanford Synchrotron Radiation Laboratories and Advanced Light Source, Berkeley, CA.

Electromigration during accelerated testing can induce plastic deformation in apparently undamaged Al interconnect lines as recently revealed by the white beam scanning X-ray microdiffraction. In the present paper, we provide a first quantitative analysis of the dislocation structure generated in individual micron-sized Al grains during an in-situ electromigration experiment. Laue reflections from individual interconnect grains show pronounced streaking during the early stages of electromigration. We demonstrate that the evolution of the dislocation structure during electromigration is highly inhomogeneous and results in the formation of unpaired randomly distributed dislocations as well as geometrically necessary dislocation boundaries. Approximately half of all unpaired dislocations are grouped within the walls. The misorientation created by each boundary and density of unpaired individual dislocations is determined. The origin of the observed plastic deformation is considered in view of the constraints for dislocation arrangements under the applied electric field during electromigration.

9:15 AM E1.3
VIA PULL-OUT MECHANISM IN Cu INTERCONNECTS AND POSSIBLE SOLUTIONS. J. Koike, R. Kainuma, A. Sekiguchi, K. Ishida, K. Maruyama, Dept. of Materials Science, Tohoku University, Sendai, JAPAN.

When Cu metallization undergoes thermal processing, Cu flows out from damascene trenches and vias, leaving large voids behind. The mechanism of this so-called "via pull-out" phenomenon has been interpreted in terms of thermal tensile stress. However, the proposed mechanism fails to explain experimental observation. For instance, via pull-out occurs in some vias despite that tensile stress acts on all vias. Furthermore, tensile stress is expected to diminish rapidly by atom migration and cannot act as a sustainable driving force to remove Cu all the way out from the vias. In this work, we first assumed the presence of pre-existing voids due to incomplete filling and considered the possibility of void coalescence under initially large thermal tensile stress. Then, pressure acting on the void surface was considered as a driving force and diffusion equation was solved to estimate the position of Cu at given time and temperature. It was found that the time for Cu to be completely removed from the vias (150 nm in width and 1000 nm in depth) is approximately 10 seconds at 450°C for Cu/Ta/TaN. Via pull-out can be avoided by reducing the energy and diffusivity of the Cu/barrier interface. Proper choice of Cu alloying elements or of barrier species is important in avoiding the via pull-out.

9:30 AM E1.4
PROPERTIES AND BARRIER MATERIAL INTERACTIONS OF ELECTROLESS COPPER USED FOR SEED ENHANCEMENT. C. Witt, K. Pfeifer, International Sematech, Austin, TX.

The conventionally used sequence for copper damascene metallization consists of barrier deposition, physical vapor deposition (PVD) Cu seed and electroplated copper. Due to the limited step coverage of PVD copper, the extendibility of this sequence to feature dimensions below 90 nm is at risk. To reduce the risk of pinch-off of very small features, the PVD layer thickness is to be reduced well below 100 nm, the drawback being poor seed coverage at the bottom of the features. Void free fill by electroplating is hence at risk by both pinch-off and discontinuous seed coverage. In this paper, the use of a conformal metal deposition method, electroless copper, to enhance PVD seed layers as thin as 10 nm is presented. It is demonstrated that sparse, discontinuous copper films provide a catalytic surface for electroless copper deposition. With electroless copper, void-free copper fill of 12.5 aspect ratio (AR) trenches (70 nm width) and 8.3 AR vias is achieved. Furthermore, 6 nm thin electroless copper films were integrated in a dual damascene process and electrically characterized. A yield of approximately 85% was achieved on via chains (360000 links, 0.25 by 1.1 μm vias), with 10 nm PVD seed. This was comparable to the yield when using 100 nm PVD seed. Hydrogen, generated as a byproduct during the electroless copper ion reduction, was found in the copper deposits as well as in the barrier films underneath. In some cases, spontaneous blistering in the plated copper film was observed, and is believed to be due to hydrogen incorporation. The interaction of electroless copper films with various barrier materials (PVD Ta, PVD TaN, CVD TiN(Si) and combinations) is discussed. Electromigration test results presented in this paper indicate that the failure mechanism is qualitatively not different from reference samples with the conventional PVD seed.

9:45 AM E1.5
EXPERIMENTAL CHARACTERIZATION OF THE RELIABILITY OF MULTI-TERMINAL DUAL-DAMASCENE COPPER INTERCONNECT TREES. C.L. Gan[a], C.V. Thompson[a,b], K.L. Pey[a,c], W.K. Choi[a,d], C.W. Chang[a], and Q. Guo[e]; [a]Advanced Materials for Micro- and Nano-Systems Programme, Singapore-MIT Alliance, SINGAPORE; [b]Department of Materials Science and Engineering, Massachusetts Institute of Technology, Cambridge, MA; [c]School of Electrical & Electronic Engineering, Nanyang Technological University, SINGAPORE; [d]Department of Electrical & Computer Engineering, National University of Singapore, SINGAPORE; [e]Institute of Microelectronics, SINGAPORE.

An "interconnect tree" is been defined as a unit of continuously connected high-conductivity metal lying within one layer of

metallization. In integrated circuits, many trees have multiple segments of straight-lines that are connected at junctions. However, most standard reliability-assessment methods are still based on the analysis of individual segments, using the results from straight junction-free lines rather than trees. This method is generally inaccurate as material within an interconnect tree can diffuse freely among connected segments, and the stress evolution in different segments of a tree is coupled. The reliability of Cu dual-damascene interconnect trees with 3-terminal (dotted-I), 4-terminal (T) and 5-terminal (cross) configurations has been investigated. The lifetime of multi-terminal interconnect trees with the same current density through the common middle via was determined to be independent of the number of segments connected at the common junction. The reliability of dotted-I test structures was further studied by varying the distribution of a fixed current density through the middle terminal into the two connected segments. Our experimental results showed an increase in reliability of the interconnect tree when the current distribution was not equal in the two connected segments, especially for the cases where one of the segments was acting as a passive reservoir or active source of Cu atoms for the adjoining segment. Due to the low barrier for void nucleation at the Cu/Si_3N_4 interface, the presence of any small atomic source in neighboring segments will enhance the reliability of a connected segment in which Cu atoms are being drained away. As a consequence, failure can occur in a tree segment which is stressed at significantly lower current densities than more highly stressed adjoining segments. These phenomena are important and their effects must be incorporated into circuit-level reliability analyses for Cu-based interconnects.

10:30 AM *E1.6
EFFECTS OF LOW k DIELECTRICS ON ELECTROMIGRATION RELIABILITY OF Cu INTERCONNECTS. P.S. Ho, K.-D. Lee, E.T. Ogawa, X. Lu, H. Matsuhashi, Laboratory for Interconnect and Packaging, The University of Texas at Austin, Austin, TX.

A statistical approach was used to investigate the effect of low k dielectrics on electromigration (EM) reliability in Cu dual-damascene structures. In this paper, we summarize the results on the EM lifetime and critical current density-length (jLc) product measured using a mutlilink line/via structure with varying line lengths. Using this test structure, the EM lifetime and jLc product were measured for 0.5 um wide Cu interconnects formed with oxide, organic polymers, CVD low k and inorganic porous low k dielectrics. Compared with oxide, low k dielectrics were found to degrade EM lifetime and the jLc product although the EM activation energy remained about the same. This can be attributed to the weak thermomechanical properties of low k dielectrics in reducing the back stress confinement effect and in inducing new failure mode due to interfacial delamination. Results will be presented and discussed.

11:00 AM E1.7
EVALUATION OF COPPER ION DRIFT IN LOW-DIELECTRIC CONSTANT INTERLAYER FILMS BY TRANSIENT CAPACITANCE SPECTROSCOPY. Takenobu Yoshino, Nobuhiro Hata, MIRAI-ASRC, AIST, Tsukuba, JAPAN; Takamaro Kikkawa, RCNS, Hiroshima University, Higashi-Hiroshima, JAPAN.

Cu ion drift is a crucial issue in Cu/low-k interconnect technology. Not only the concentration of Cu drifted into low-k films, but also the electronic states originated from the drifted Cu are important because they govern the current leakage and dielectric breakdown mechanisms. We propose a modified isothermal capacitance transient spectroscopy as a technique to observe Cu-related electronic density of states in the bandgap of low-k films. In the proposed technique, Cu/low-k/p-Si metal-insulator-semiconductor (MIS) structure is used. Cu is drifted into the low-k film by a bias-temperature-stress (BTS). The capacitance of the MIS structure reflects the series connection of low-k film capacitance and depletion layer capacitance in the p-Si. As the net charge concentration in the low-k film changes, the total charge in the depletion layer changes so as to maintain the charge neutrality, and therefore, the depletion layer width and the capacitance of the MIS structure change. Therefore, by measuring the capacitance transient of the MIS sample, we can measure the time-dependent change in the charge concentration in the low-k film. As an initial excitation, we employed the hot-carrier injection by applying 25 V bias and 254 nm UV light irradiation simultaneously, and measured the capacitance transient to observe the thermal emission of injected hot carriers from the electronic states in the low-k bandgap. A decrement of transient capacitance was observed at around 3000 s reproducibly when the BTS applied samples were measured, while not when BTS was not applied. From the result, we attribute the decrement of transient capacitance to copper-related electronic states. By assuming an attempt-to-escape frequency of the charge from the electronic states, the energy position was calculated to be approximately 0.8 eV below the conduction band. In conclusion, Cu related electronic states in low-k film was clearly shown by a transient capacitance measurement.

11:15 AM E1.8
MEASUREMENT OF THE Cu ELECTROMIGRATION DRIFT VELOCITY IN DUAL-DAMASCENE INTERCONNECTS. Frank Wei, MIT, Dept of Material Science and Eng, Cambridge, MA; Intel Corp., Hillsboro, OR; Chee-Lip Gan, Singapore-MIT Alliance, AMM&NS, SINGAPORE; Tom Marieb, Jose Maiz, Intel Corp., Hillsboro, OR; Carl V. Thompson, MIT, Dept of Material Science and Eng, Cambridge, MA; Singapore-MIT Alliance, AMM&NS, SINGAPORE.

Electromigration-induced failure normally occurs through nucleation and growth of voids. In current Cu-based interconnect technology, void nucleation is known to occur easily at low stresses. The lifetime of Cu-based interconnects is therefore often dependent on the rate of void growth, a measure of which is given by the drift velocity. Consequently, measurements of electromigration drift velocities provide an important insight to the diffusional aspects of electromigration. Drift velocities may also serve as quantitative indications to the reliability of a given Cu metallization process. We conducted electromigration stress experiments on dual-damascene Cu interconnect lines that terminated with vias above and vias below the ends of the test lines. In both types of structures we observed that in a significant fraction of the test population, the resistance of the lines increased steadily over time prior to failure. We postulate that this gradual resistance increase results from void growth and that the rate of resistance increase correlates with the electromigration drift velocity. The values of the electromigration drift velocities determined in vias-below lines were similar to those measured in vias-above lines, though there was a broader range of variation in the former case. The larger variation is correlated with the larger range of void shapes and sizes in vias-below structures. Drift velocities in both types of structures were measured as a function of current density and test temperature. Via-below and via-above structures are known to have very different lifetimes under the same stress conditions. Given that the stress for void nucleation should be the same, the observation that the rate of void growth rate is the same supports the proposal that this asymmetry in reliability in the two different configurations is associated with differences in the void sizes required to cause failure.

11:30 AM E1.9
ELECTROMIGRATION STUDY OF DUAL-DAMASCENE Cu INTERCONNECTS WITH CVD LOW k DIELECTRICS. Xia Lu, Ki-Don Lee, Hideki Matsuhashi, Paul S. Ho, Interconnect and Packaging Laboratory, Microelectronics Research Center, The Univerisity of Texas at Austin, Austin, TX; Michael Lu, Kai Zhang, LSI Logic Corporation, Santa Clara, CA.

Electromigration (EM) studies have been performed at temperatures of 305, 325, 345, 365°C and current density of 0.5 MA/cm^2 to investigate the lifetime characteristics and failure mechanism for Cu/low k interconnects. The low k material was a CVD MSQ based dielectric with k of 2.7. Statistical studies were carried out using the critical length (LC) test structures containing multi-link line/via elements with varying line lengths. The activation energies were found to be 0.86 eV for 0.5 μm wide lines and 0.70 eV for 0.25 μm wide lines, suggesting mass transport via interfacial diffusion. Critical current density-length product (jL_c) was determined to be 2000 $\pm$250 A/cm, about half of that of the oxide structure. Failure analysis by FIB revealed the presence of multiple failure modes including voiding at the via bottom, Cu extrusion and delamination at Cu/cap layer interface. These results indicated that the thermo-mechanical properties of the low k materials are important in controlling the EM reliability of Cu interconnects.

11:45 AM E1.10
DEPENDENCE OF VOID EVOLUTION ON SEGMENT LENGTH IN Cu INTERCONNECTS. R. Leon, K.C. Evans, and D.T. Vu, Jet Propulsion Laboratory, Pasadena, CA; J.A. Colon and B. Bavarian, California State University, Northridge, CA; V. Blaschke, International SEMATECH, Austin, TX; E.T. Ogawa, and P.S. Ho, University of Texas, Austin, TX.

Void evolution during electromigration was studied by recording void nucleation, growth and displacements at various intervals during thermal and electrical stress experiments on Cu interconnects. Data was collected for four line lengths in groups of 50 (with 0.25 x 0.35 micron cross sections) segments consisting of 25, 50, 150 and 300 micrometer long interconnects that were serially arranged with a Cu segment and Cu via in each structure. This geometry allows maintaining the same nominal current density in al 50 segments. Void nucleation and evolution were measured at 240°C and 2 x 106 Amps/cm2. Structural data was correlated with the electrical data, which was also monitored for each line. Resistance values (and increases in resistance due to electromigration-induced thinning and voiding) and leakage currents were acquired digitally at regular time intervals. Depleted material and void areas were measured using high

resolution scanning electron microscopy. Averages over all lines measured give rates of void area growth that range from 240 nm2/hr to 1300 nm2/hr. These measurements also show a clear dependence of both void growth and void nucleation behavior on line length.

SESSION E2: INTERCONNECT RELIABILITY ISSUES
Chairs: Oliver Kraft and David P. Field
Tuesday Afternoon, April 22, 2003
Golden Gate B2 (Marriott)

1:30 PM *E2.1
FATIGUE AS A RELIABILITY CONCERN IN MICRO-ELECTRONIC INTERCONNECTS. C.A. Volkert, R. Mönig, Y.B. Park, and G.P. Zhang, Max Planck Institute for Metals Research, Stuttgart, GERMANY.

The development of severe surface damage, crack formation and electrical failure has recently been observed in unpassivated Cu and Al interconnects as a result of thermal-mechanical fatigue. This phenomenon is a potential reliability threat to microelectronic devices since the temperature amplitudes that lead to damage formation are not much larger than those present in typical high performance devices during use. In this talk, the thermal-mechanical testing method and recent results will be presented. The testing method uses alternating currents to produce temperature swings on the order of 100-300°C, and thus strain cycles, in the interconnects. After as few as 10^5 cycles, damage is observed at the surface of the interconnects. Particular emphasis will be placed on the effect of interconnect dimension and grain size and the effect of testing frequency on the nature of the damage that is formed. In large-grained samples (~1.0 μm), damage appears as periodic surface extrusions, reminiscent of the fatigue damage observed in bulk materials. In fact, plan-view TEM studies of the thickest films show that these surface extrusions are associated with characteristic dislocation structures in the film, such as cells and walls. However in smaller grained material, these dislocation structures are absent and the damage forms as grain boundary grooves and sunken grains and appears to be controlled by surface and grain boundary diffusion rather than by a dislocation glide mechanism. In addition, tests performed at different frequencies suggest that there is a creep component to the damage formation process. Finally, an analysis will be presented on the effect of coatings on inhibiting damage formation and it will be shown that soft materials, such as many of the potential low-k interlevel dielectric materials, do little to inhibit the formation of this damage.

2:00 PM E2.2
EFFECT OF BARRIER LAYER ON GRAIN GROWTH AND TEXTURE EVOLUTION IN ELECTROPLATED COPPER FILMS AND DAMASCENE LINES. Tejodher Muppidi and David P. Field, Washington State University, School of Mechanical and Materials Engineering, Pullman, WA; John E. Sanchez, Advanced Micro Devices, Interconnect Research Group, Sunnyvale, CA.

A number of different barrier layers and deposition techniques have been under investigation to get a more conformal coverage in damascene trenches of narrow line width and high aspect ratio. The most commonly used barrier layer and deposition technique in copper interconnects is PVD deposition of Ta or TaN or Ta/TaN. The latest innovation in barrier layer technology includes Atomic Layer Deposition (ALD) of TaN, TCN and WCN; and CVD for deposition of TiNSi. Copper microstructure is known to influence its properties like diffusion, resistivity and electromigration. The effect of the different barrier layers (Ta, TaN, Ta/TaN, TiNSi, TCN and WCN) on the electroplated copper films and Damascene lines will be examined in the present paper. The blanket film samples were characterized by XRD, AFM and OIM to obtain the texture, grain size and roughness values. In addition, EM tests were carried out on the damascene lines to obtain mean time to failure (MTF) and activation energy. The results show that the barrier layer does have an influence on the grain growth and texture evolution in Copper films.

2:15 PM E2.3
EFFECTS OF ADDITIVES ON GRAIN BOUNDARY CHARACTERISTICS AND STRESS VOIDING IN ELECTROPLATED COPPER FILMS. Hyun Park, Soo-Jung Hwang, Young-Chang Joo, Seoul National Univ, School of Materials Science and Engineering, Seoul, KOREA.

Electroplated (EP) copper is used as an interconnect material in advanced ULSIs. It was found out that additives in EP copper films play an important role in grain boundary characteristics and the morphologies of surface defects, i.e. stress voids. After annealing at 435°C, in the EP film the crack-like grain-boundary diffusion wedges along some grain boundaries were observed, while in the EP film with no additive and the sputtered film voids at the triple junctions were mainly observed. The cross-sectional profiles by atomic force microscope showed that the triple junction voids were deeper than the crack-like wedges. The film-thickness dependence on the morphologies of surface defects was inconsiderable. The grain boundary misorientation distribution by electron back-scattering diffraction (EBSD) showed that in the EP film with additives twin boundaries considerably evolved and the fraction of lower energy boundaries, which are low misorientation angle grain boundaries and twin boundaries, of the EP film with additives was higher than those of the EP film with no additive and the sputtered film. The misorientation distribution of the EP film with no additive was similar to that of the sputtered film. EBSD results also showed that crack-like wedges were formed along the higher energy grain boundaries. These results indicate that additives in EP films make an influence on grain boundary characteristics and then atomic diffusion from surface to grain boundary or triple junction for stress relaxation during annealing. The roles of additives in the anisotropy of grain boundary energies and the selective atomic diffusion along the higher energy grain boundaries are discussed.

2:30 PM E2.4
MICROSTRUCTURAL ANALYSIS OF COPPER ALLOY FOR CHARACTERIZATION OF STRESS-INDUCED VOIDING MECHANISMS. Katsuyuki Musaka, Applied Materials, Inc., ECP Division, Santa Clara, CA; Ryan Camacho, Brigham Young University, Dept of Physics, Provo, UT.

Microstructural analysis of an electrolytic plated copper alloy film revealed potential advantage over pure copper films in suppressing stress- induced voiding through a grain boundary pinning effect. The grain boundaries themselves are full of vacancies, which become filled as the grains grow. Any elimination of grain boundaries by grain growth require extra copper supply from somewhere, and hence generate vacancies at boundary gaps, which transport creates sizeable voids usually at the interface between copper and barrier or passivation dielectric where the adhesion is the lowest. It was theorized that the inclusion of a small amount of a second metal in the copper film during electrolytic plating and its segregation at grain boundaries by thermal treatment suppress stress-induced voiding by lowering the copper grain boundary diffusivity. In addition to creating interstitial defects in the lattice structure of the copper, it is thought that the alloyed co-element will fill the vacancies inherent at grain boundaries. This will increase the energy required for grain merging, thereby pinning the grain boundaries. To obtain an indication of the grain boundary pinning effect, the amount of twin formation as a function of thermal treatment of electrolytic plated copper film was evaluated by electron back scattering diffraction measurement. The result indicated that, with existence of copper alloy co-element, i.e. P and Sn, twin formation was significantly reduced compared to pure copper. Furthermore, the stress hysteresis curve of CuSn (0.1at%) indicated a higher film deformation temperature than that of pure copper. These indications are consistent with the theory of less deformation and elimination of grain boundaries, while not inducing voiding, during thermal processing. With the growth of the grain boundaries inhibited, both the boundary filling and vacancies generation issues are suppressed, thus copper alloy is believed to be more resistant to stress-induced voiding.

2:45 PM E2.5
Abstract Withdrawn.

3:30 PM *E2.6
FRACTURE MECHANICS FOR THE LONG-TERM RELIABILITY OF INTEGRATED STRUCTURES. Z. Suo, Mechanical and Aerospace Engineering Department and Princeton Materials Institute, Princeton University, Princeton, NJ.

Interconnect structures have complex architectures, small feature sizes, and diverse materials. The close proximity of dissimilar materials leads to unusual fracture behaviors. A scientific understanding of these behaviors is significant for the development of the future technology. In particular, rate processes, such as creep, subscritical cracking, and ratcheting, limit the long term reliability of the interconnects. Drawing on recent experiments and models, this talk describes a channel crack in a brittle film on an underlayer. When the underlayer is compliant (e.g., a low k dielectric), the driving force on the channel crack is very large. When the underlayer creeps (e.g., a polymer), the crack velocity is set by the viscosity in the underlayer, as well as by subcritical cracking in the brittle film. When the underlayer is plastically deformable (e.g., a metal), on thermal cycling, the crack can grow in the brittle film by ratcheting deformation in the underlayer. I also discuss the use of these phenomena to measure mechanical properties at the small scale. PDF files of papers are available at http://www.princeton.edu/~suo/
Keywords: Interconnects, fracture, creep, plasticity

4:00 PM E2.7
INTERFACIAL ADHESION OF LITHOGRAPHICALLY PATTERNED THIN-FILM INTERCONNECT STRUCTURES.
Christopher S. Litteken, Reinhold H. Dauskardt, Stanford University, Department of Materials Science and Engineering, Stanford, CA; Guanghai Xu, Tracey Scherban, Intel Corporation, Technology Development Quality & Reliability, Hillsboro, OR; Brad Sun, Intel Corporation, Technology Development Quality & Reliability, Santa Clara, CA.

The cohesive and adhesive fracture resistance of interfaces and adjacent materials in lithographically patterned interconnect structures (as opposed to blanket thin-films) containing Cu and low-k materials will be presented. Such structures provide unique opportunities for studying the role of mechanical constraint, complex residual stress fields, and local elastic property variations on the mechanical reliability of interconnect structures. Arrays of Cu lines surrounded by selected barrier and low-k dielectric materials with lateral dimensions of ~150 nm were fabricated with varying aspect ratios, metal densities, and feature orientations. Thin-film fracture mechanics techniques based on the 4-point bend and double cantilever beam specimen configurations were employed to measure the interfacial fracture resistance, G_c, for each patterned structure. Results will be provided that indicate the significant effect of feature orientation and materials on G_c. In order to elucidate the role of varying material properties and residual stress fields, detailed characterization of the resulting fracture surfaces was performed. Trends in adhesion related to the specific patterned structure will be discussed in terms of the relationship observed between multi-dimensional constraint of materials at interconnect length scales, complex residual stress fields and elastic property variations associated with the patterned features, and the relevant energy dissipation mechanisms that control adhesion.

4:15 PM E2.8
QUANTITATIVE MEASUREMENTS OF SUBCRITICAL DEBONDING OF Cu FILMS FROM DIELECTRIC SUBSTRATES.
M.Pang and S.P. Baker, Cornell University, Dept of Materials Science and Engineering, Ithaca, NY.

Subcritical debonding of Cu interconnects from dielectric substrates poses a serious mechanical reliability problem. A driver film method, by which a highly stressed Cr overlayer is imposed to debond a target film from a substrate, was employed to study the subcritical debonding behavior of Cu films from dielectric substrates. Model systems include copper films on flat panel display glasses, silicon oxide, and silicon nitride on silicon wafers. The effect of varying oxygen concentration at copper/silicon nitride interfaces on adhesion was also studied. A range of strain energy densities for driving debonding was provided by depositing Cr with various thicknesses. Driver/target bilayer strips made by microfabrication techniques were used for quantitatively studying subcritical debonding kinetics, i.e., the relationship of the film debonding velocity (v) as a function of the strain energy release rate (G). Subcritical crack velocities were found to be very sensitive to small changes in interface chemistry. A model for these effects based on environmentally assisted processes will be presented.

4:30 PM E2.9
ASSESSMENT OF RELIABILITY OF Cu-BLACK DIAMOND INTECONNECTS USING TIME DEPENDENT DIELECTRIC BREAKDOWN.
Ahila Krishnamoorthy, Ning Yang Huang and Qiang Guo, Deep Submicron Integrated Circuits Department, Institute of Microelectronics, SINGAPORE.

One of the main reliability concerns in dual damascene copper metallization integrated with low dielectric constant materials is the drift of copper ions under electric field to the surrounding dielectric layer [1]. To characterize the failure induced by diffusion, ramp tests and time dependent dielectric breakdown (TDDB) tests were performed. The output from ramp tests was used to identify suitable electric field for TDDB tests. TDDB was performed in the field range of 1 to 2 MV/cm and in the temperature range of 30 to 150°C. Two structures were chosen for study; (1) Metal 1 and Metal 2 intralevel comb structures with metal widths of 0.24 and 0.28 μm respectively, but with different spaces from 0.22 to 0.28 μm and (2) interlevel capacitor structures. The top dielectric barrier layer that covers M1 and M2 was SiC and SiN respectively. The interlevel capacitor structures had a dielectric stack of 500 $\AA$ SiC and 5 k $\AA$ Black Diamond(BD) between M1 and M2. From the leakage between combs at the same level (either metal 1 or metal 2) Cu drift through SiC/BD or SiN/BD interface or through BD can be characterized. The leakage between M1 and M2 in interlevel capacitors gives an estimate of barrier efficiency of SiC. It was found that the copper surface functioned as an easy path for copper drift thereby shorting the lines. In this paper, TDDB of SiC/Cu and SiN/Cu comb structures and Cu/BD/SiC/Cu capacitor structures will be presented. SiN/Cu interface was found to be more reliable than SiC/Cu interface. A mechanism is put forward to explain TDDB failure. Finally, results from different surface treatments that demonstrated improvement in TDDB lifetime will be presented.

4:45 PM E2.10
ADHESION ENHANCEMENT FOR MULTIPLE LEVEL Cu/SILK^{TM} INTEGRATION.
X.T. Chen, D. Lu, Y.T. Tan, Y.W. Chen, and P.D. Foo, Institute of Microelectronics, SINGAPORE.

It is a great challenge to fabricate multilevel Cu/polymer low-k dual damascene structure and one of the key issues is to prevent the metal layer from peeling during fabrication. In this paper, we report the progress on the fabrication of Cu/SiLK^{TM} multilevel structures. Delamination of Cu/Ta from SiLK^{TM} was observed after CMP at wide metal lines in our 0.13 μm copper process integration. It was most pronounced after the devices had undergone high temperature thermal cycle. Poor adhesion can result from many factors such as stress, thermal instability, and poor surface condition. We determined the cause of Cu/Ta delamination to be the formation of an altered SiLK^{TM} surface layer after the reactive (H_2/He) plasma clean (RPC) treatment, employed to remove copper oxide. By means of TOF-SIMS, the as-deposited SiLK^{TM} was found to contain mainly unsaturated C-H clusters that resulted from the ionization of the aromatic hydrocarbon molecules. After RPC, the SiLK^{TM} surface was observed to be hydrogen enriched. There was a systematic shift to the higher masses due to additional hydrogen atoms in the original unsaturated C-H clusters. The intensity of the signal had also increased significantly after RPC process, indicating that the SiLK surface had been modified and ionization of the surface had become easier. It may be concluded that the hydrogen radicals had not only damaged the SiLK surface to result in more molecular fragmentation, but also chemically reacted with SiLK to form a more saturated surface. Further analysis showed that RPC only affected the SiLK surface. To improve adhesion we employed an argon sputtering process to remove this altered SiLK surface layer. With this treatment, adhesion was found to have improved and no delamination was observed even up to 6 metal layers.

SESSION E3: POSTER SESSION
ADVANCED INTERCONNECT MATERIALS
Chairs: Takamaro Kikkawa and Oliver Kraft
Tuesday Evening, April 22, 2003
8:00 PM
Salon 1-7 (Marriott)

E3.1
AlCu PATTERN GENERATION ON 3D STRUCTURED WAFER USING MULTILEVEL EXPOSURE METHOD ON THE ELECTRODEPOSITED POLYMER MATERIAL.
Vineet Sharma, Arief Suriadi, Frank Berauer, Hewlett Packard, SINGAPORE; Laurie Mittelstadt, Hewlett Packard Laboratory, Palo Alto, CA.

Normal photolithography tools have focal depth limitations and unable to meet the expectations of higher resolution photolithography over the highly topographic structures. This paper shows a cost effective and promising technique by combining two different approaches, which are capable of controlling the critical dimensions of the sidewall traces and the pattern continuity throughout the highly topographic structures. Firstly, Electrophoretically deposited photoresist method is being used for photoresist deposition on the 3D structured wafers, which is capable to achieve good conformal as well as uniform photoresist deposition and highly appreciated to coat 3D surfaces. Secondly, Multi step exposure method has been used to expose electrophoretically deposited photoresist on the AlCu seed layer silicon substrate with 350 μm deep trenches. Hence, by combining these two novel methods, metal (AlCu) patterns of up to 75 μm width and 150 μm pitch (from top flat towards down the slope) have been demonstrated on the isotropically etched deep trenches with 5-10% CD loss.

E3.2
COPPER OXIDATION STUDIED BY IN SITU RAMAN SPECTROSCOPY.
Robert Schennach, Graz University of Technology, Institute of Solid State Physics, Graz, AUSTRIA; Andreas Gupper, Graz University of Technology, Research Institute for Electron Microscopy, Graz, AUSTRIA.

The growing importance of copper in the semiconductor industry has led to a renewed interest in the properties and growth modes of copper oxides under a variety of conditions. While thermal oxidation of copper has been studied extensively over the last decades, recent surface studies seem to ignore the possible formation of Cu_3O_2. It has been shown earlier that thermal oxidation of copper leads to multilayer structures, which consist of Cu_xO, Cu_2O, Cu_3O_2 and

CuO, depending on the oxidation conditions. These oxides were analysed ex situ using X-ray Photoelectron Spectroscopy (XPS) combined with depth profiling, Linear Sweep Voltammetry (LSV) and Galvanostatic Reduction (GR). In this work it will be shown that Raman Spectroscopy can be used to follow the formation of the different copper oxides in situ. The experiments were performed using a Raman Microscope with a sample heating extension, which enables in situ copper oxidation in air between room temperature and 300°C. Raman spectra were acquired in the range between 1500 to 150 cm^{-1}. From these spectra one can see that Cu_2O is formed between 70 and 150°C, Cu_3O_2 is formed between 150 and 270°C and CuO starts to form at temperatures higher than 270°C.

E3.3
MATERIAL AND ELECTRICAL CHARACTERIZATION OF HfO_2 FILMS FOR MIM CAPACITORS APPLICATION. Hang Hu, Chunxiang Zhu, Y.F. Lu, J.N. Zeng, Y.H. Wu, T. Liew, M.F. Li, and W.K. Choi.

Thin films of HfO_2 high-dielectric by pulsed-laser deposition (PLD) have been investigated as a function of substrate temperature and pressure. X-ray diffraction (XRD), X-ray photoelectron spectroscopy (XPS), secondary ion mass spectroscopy (SIMS), and ellipsometry were used to characterize the as-deposited films. Experimental results show that substrate temperature has little effect on the stoichiometry, while deposition pressure plays an important role in determining the ratio of Hf and O. It is also shown that the deposition temperature and pressure affect the optical properties of the HfO_2 thin films in different ways. For Metal-Insulator-Metal (MIM) capacitors application in Si analog circuit, the electrical properties of HfO_2 thin films were investigated by means of current-voltage and capacitance-frequency characteristics. It is found that the HfO_2 MIM capacitor fabricated at 200°C shows an overall high performance, such as a high capacitance density of $\sim$3.0 $fF/\mu m^2$, a low leakage current of 2×10^{-9} A/cm^2 at 3 V, low voltage coefficients of capacitance, and good frequency dispersion property. The fabrication process is compatible with the existing VLSI backend of line integration. All these indicate that the HfO_2 MIM capacitors are very suitable for use in Si analog circuits.

E3.4
DETECTION OF VOIDS IN TUNGSTEN INTERCONNECT VIAS USING LASER-INDUCED SURFACE ACOUSTIC WAVES. Joshua Tower and Michael Gostein, Philips Analytical, Natick, MA; Koichi Otsubo, Philips Analytical, Sagamiohno, JAPAN; Atsushi Kawasaki, NEC Corporation, Sagamihara, JAPAN.

Advanced interconnect technology is steadily moving to narrower lines and vias with ever increasing aspect ratios. This trend presents challenges for depositing metals in the damascene structure without leaving voided areas. Such voids can lead to open circuits and ultimately to device failure. In order to optimize and monitor metal-fill processes, novel metrology techniques are needed that can provide timely and non-destructive feedback. Conventional techniques for characterization of voids, such as cross-sectional SEM, take a long time and require the wafers to be sacrificed. Electrical testing does not require destruction of the wafers, but it does require contact probes, and in the case of via chains, several metal levels must be fabricated before the electrical test can be completed. Optoacoustic technology based on laser-induced surface acoustic waves [1], which has previously been implemented for measurement of metal film thickness, provides the capability for detection of incomplete metal-fill (voids) immediately after metal deposition or CMP. This enables real-time feedback for improved process control and also facilitates process development. In this work, test wafers were fabricated with tungsten via arrays of 18 different diameters, ranging from 0.07 microns to 0.50 microns. Four sets of wafers with this test mask were prepared under differing process conditions for tungsten deposition, to determine what process conditions lead to the most complete filling of the vias. Evaluation of the metal-fill effectiveness was done after CMP using ISTS optoacoustic measurements, followed by cross-sectional SEM for confirmation of the results. The data show how incomplete metal-fill depends on via diameter and on processing conditions. In the most effective metal-fill process, complete metal-fill was achieved for all via diameters down to 0.08 microns. For less effective processing, voids were observed in vias for diameters up to 0.12 microns. Optoacoustic measurements were effective in detecting missing tungsten and showed good correlation to voids directly observed in SEM cross-section. References: [1] M. Gostein, et al, "Thin Film Metrology Using Impulsive Stimulated Thermal Scattering (ISTS)," in Handbook of Silicon Semiconductor Metrology, ed. Alain Diebold (Marcel Dekker, New York, 2001), pp. 167-196.

E3.5
THE EFFECTS OF BARRIER TYPE ON THE TEXTURE AND ADHESION STRENGTH OF Cu METALLIZATION. Atsuko Sekiguchi and Junichi Koike, Tohoku Univ, Dept of Materials Science, Sendai, JAPAN; Jiping Ye, Nissan ARC, Ltd., Yokosuka, JAPAN; Kouichi Maruyama, Tohoku Univ, Dept of Materials Science, Sendai, JAPAN.

Cu interconnect reliability is greatly affected by film texture and the adhesion strength of Cu/barrier interface. These microstructural factors are dependent on the barrier materials. This study is aimed at understanding the effects of different barrier materials on film texture and adhesion strength. Three types of barrier layers were employed for a multilayered structure of Cu (150 nm)/ barrier (25 nm)/ SiO2 (100 nm)/ Si (7000 nm). The barrier layers were Ta, TaN, and Ta/TaN. The Cu and barrier layers were deposited by RF magnetron sputtering. Their texture was determined by X-ray diffraction analysis and electron back scattering pattern analysis. The crystalline structure and crystallographic orientation relationship between Cu and the barriers were determined by transmission electron microscopy. Adhesion strength was also investigated by scratch test in combination with finite element method calculation. The results indicated that the crystal structure of each barrier layer was beta-Ta for the Ta barrier, a mixture of beta-Ta and crystalline TaN for the TaN barrier, and a mixture of beta-Ta and bcc-Ta for the Ta layer of the Ta/TaN barrier. The texture of the Cu overlayer was a strong (111) for the Ta barrier and a weak (111) for the TaN and the Ta/TaN barriers. A strong (111) texture of Cu on the beta-Ta barrier was attributed to a heteroepitaxial relationship between Cu (111) and beta-Ta (001) planes. The same reason was found to be applicable to the excellent adhesion strength in the (111) textured Cu and the beta-Ta barrier. The obtained results will be discussed in view of misfit strain and interface energy at the Cu/barrier interface.

E3.6
SUPERCONFORMAL SILVER ELECTRODEPOSITION FOR ADVANCED INTERCONNECTS. Daniel Josell, Thomas Moffat, Daniel Wheeler and Brett Baker, Metallurgy Division, National Institute of Standards and Technology, Gaithersburg, MD.

While aluminum alloy metallizations are being replaced by copper in integrated circuits due to the lower resistivity of copper, surface scattering effects for copper interconnects are becoming quite significant as dimensions move beyond the 130 nm node. Silver metallizations, with their intrinsically lower resistivity (bulk value slightly lower than copper) and potentially lower surface scattering properties are being considered by many as the next metallization of choice. However, the high aspect ratio, dual damascene geometries now used with copper metallizations are possible only because of copper's ability to fill features superconformally during electrodeposition in particular electrolytes, a capacity that, to this point has been unique for copper electrodeposition. This talk presents experiments and modeling of superconformal electrodeposition of silver in fine trenches and vias. The electrolytes yielding superconformal silver deposition, also called "superfill", contain a catalyst but no inhibitor or leveler and are fully disclosed. Experimental results are compared to predictive simulations of feature filling from models based on the CEAC mechanism. Agreement is seen to be excellent, with the experimentally observed fill or failure to fill of a given feature in a given electrolyte as well as the experimentally observed incubation period of conformal growth, the bottom-up filling characteristic of "superfill", and the formation of an overfill bump all predicted; this is particularly impressive because the CEAC mechanism has no fitting parameters. The CEAC mechanism is based on conservation of adsorbed metal-deposition rate enhancing catalyst during surface area change; i.e., the local coverage changes with the surface area on which it is adsorbed by simple mass conservation. The CEAC mechanism leads to increasing catalyst coverage, and thus local deposition rate, on concave surfaces such as the bottoms of fine features (hence the name of the mechanism). The superconformal silver results presented here, both the ability to superconformally fill fine features and the ability to make quantitative predictions using the CEAC mechanism with independent parameters, overcome a substantial hurdle toward industrial use of silver metallizations.

E3.7
MICROSRUCTURE AND MECHANICAL PROPERTIES OF ELECTROPLATED Cu THIN FILMS. Pallavi Shukla and Parshuram Zantye, University of South Florida, Dept of Mechanical Engineering and Center for Microelectronics Research, Tampa, FL; Arun K. Sikder, University of South Florida, Center for Microelectronics Research, Tampa, FL; Ashok Kumar, University of South Florida, Dept of Mechanical Engineering and Center for Microelectronics Research, Tampa, FL; Mahesh Sanganaria, Novellus Systems, Inc., San Jose, CA.

The increasing demand for faster and more reliable integrated circuits (ICs) has promoted the integration of Copper-based metallization. Cu will be adopted in the future deep sub micron ULSI metallization due to its lower resistivity and better reliability as compared to the conventional Al alloys. Electroplated Cu films demonstrate an

intriguing phenomenon known as self annealing. In this paper we intend to investigate the annealing behavior of electroplated Cu films grown on a seed Cu layer on top of the barrier layers (adhesion promoters) over a single crystal silicon substrate. Nanoindentation was performed on all the samples with the continuous stiffness measurement (CSM) technique using the Nanoindenter XP and it was found that the elastic modulus varies from 110 to 130 GPa while the hardness varies from 1 to 1.6 GPa depending on the annealing conditions. The surface morphology and roughness of Cu films were characterized using Atomic Force Microscopy. The tribological properties of all the copper films were also measured using the Bench Top CMP tester. Subsequently, Nanoindentation was performed on the samples after polishing the top surface in order to investigate the work-hardening. Finite Element Modeling is to be performed for the investigation of the stress distribution during nanoindentation.

E3.8
ANISOTROPIC PLASMA CHEMICAL VAPOR DEPOSITION OF COPPER FILMS IN TRENCHES. Kosuke Takenaka, Masao Onishi, Manabu Takeshita, Toshio Kinoshita, Kazunori Koga, Masaharu Shiratani, and Yukio Watanabe, Kyushu Univ, Dept of Electronics, Fukuoka, JAPAN.

While copper (Cu) interconnects in trenches and vias of ULSI in industry are fabricated by the combination of Cu seed layer deposition by PVD and subsequent filling by electroplating, this method faces to a difficulty to achieve void-free full filling of trenches and via holes below 0.1 μm wide and above 1 μm deep. Here, we propose an ion-assisted chemical vapor deposition method by which Cu is deposited preferentially from the bottom of a trench (anisotropic CVD) in order to fill small via holes and trenches. The anisotropy, which is a ratio of deposition rate at the bottom of a trench to that at its sidewall, tends to increase with energy as well as flux of ions impinging on the substrate surface, since ions enhance the deposition rate at the top surface and bottom of trench[1]. Significant sidewall deposition is observed for an H_2 + $C_2H_5OH[Cu(hfac)_2]$ discharge, and such deposition limits the anisotropy to be below 300% and finally leads to pinching-off small trenches and vias. On the other hand, such sidewall deposition is not observed for Ar + H_2 + $C_2H_5OH[Cu(hfac)_2]$ and the films are deposited only on the top surface and bottom of trench. These results indicate that the ion irradiation is a key to realize the anisotropic filling. By using the Ar + H_2 + $C_2H_5OH[Cu(hfac)_2]$ discharge, we have demonstrated a high anisotropy above 1000%. A mechanism bringing about such high anisotropy will be discussed in the presentation.
[1] K. Takenaka, et al., Proc. of Int. Symp. on Dry Process, (2002) pp.221-226.

E3.9
EFFECT OF PLASMA PRE-TREATMENT ON DEWETTING PROPERTIES OF CVD Cu ON CVD W_2N BARRIER LAYER. Degang Cheng, Guillermo Nuesca, and Eric T. Eisenbraun, School of NanoSciences and NanoEngineering, The University at Albany-SUNY, Albany, NY.

The effect of different plasma pre-treatments of chemical vapor deposited (CVD) tungsten nitride (W_2N) surfaces on the dewetting behavior of subsequently grown CVD Cu films was investigated by annealing the resulting film stacks in high purity argon. It was found that a hydrogen plasma pre-treatment significantly improved the resistance to Cu dewetting from the W_2N surfaces while ammonia and nitrogen plasma pretreatment slightly accelerated the dewetting process. The proposed mechanisms and ramifications of these findings will be discussed.

E3.10
REDUCED TIME FOR UNIFORM ETCHING OF COPPER POWER PLANES DURING FIB EDITING. Vladimir Makarov, William Thompson, Theodore Lundquist, NPTest, Inc, San Jose, CA.

Copper etching represents a serious challenge for Focused Ion Beam (FIB) removal of copper metallizations in integrated circuits. Normally copper power planes and traces consist of numerous crystallites each having a specific crystallographic orientation. Each orientation shows significantly different etching rates under FIB bombardment [1]. Ion etching of copper leads to significant roughness on copper and unacceptable damage to underlying and adjacent dielectric [2]. An improved methodology for uniformly etching copper over SiO_2 will be reported. It consists of three steps: 1) Exposure of copper, 2) Initial amorphization of the copper surface and 3) Etching in the presence of an etch-assisting chemistry. The amorphization step uses ion bombardment at an angle of incidence different from normal, so that grains that would show strong channeling and therefore be most resistant to etching under normal bombardment are effectively amorphized (patent pending). How the angle of incidence for amorphization is determined will be explained. The amorphization step significantly reduced differential etching rates among the grains, but did not eliminate it completely. Therefore the critical copper etching operation remained normal ion bombardment in the presence of the NH_3-H_2O mixture [3], which protected underlying and adjacent SiO_2 from etching. Note the amorphization step also improved the etching of copper over low-k dielectric. Examples of copper etching with and without the amorphization step are reported; etching times and effects on underlying and adjacent dielectric are compared. Etching time reduction was found to be almost 2x. References [1] J.R. Phillips, D.P. Griffis, and P.E. Russel, J. Vac. Sci. Technol. A 18(4) (2000) 1061 [2] S. Herschbien et al, Proceedings of ISTFA (1998) 127 [3] V.V. Makarov et al, Proceedings of 3^{rd} AVS International Conference on Miroelectronics and Interfaces (2002) 115.

E3.11
CHARACTERIZATION OF SELF-ANNEALING KINETICS IN ELECTROPLATED COPPER FILMS. Pavel Freundlich, Matthias Militzer, Dan Bizzotto, University of British Columbia, Advanced Materials and Process Engineering Laboratory, Vancouver, BC, CANADA.

The Damascene process has become the method of choice to deposit novel Cu interconnects. This method involves electrochemically plating of Cu layers. Subsequently, these layers self anneal which is associated with a decrease in resistivity by approximately 20% to the nominal bulk resistivity of Cu. As a model system to study microstructure evolution during self-annealing at room temperature, thin copper films are electrochemically deposited onto polycrystalline gold substrates. The electrolyte bath consists of a sulfuric acid copper sulfide solution containing organic additives as levelers and brighteners. Self-annealing of the films is quantified by means of a variety of experimental techniques including electron back-scatter diffraction, transmission electron microscopy, x-ray diffraction and electrical resistivity measurements. Microstructure evolution is characterized by abnormal grain growth where starting from the as-deposited, nanocrystalline structure a bimodal grain size distribution develops. As a result, a coarser grain structure forms with an average grain size of approximately 1.5 microns. The transition from small to coarser grains is consistent with the observed drop in resistivity, as concluded from the grain size-resistivity relationship originally proposed by Mayadas and Shatzkes. Further, grain growth is associated with an increase of the (111) texture component in the present case. The effect of organic additives on self-annealing rates has been quantified and incorporated into a phenomenological model. Utilizing the Johnson-Mehl-Avrami-Kolmogorov approach, the model describes the volume fraction of large grains as a function of time. The challenges in clarifying the mechanisms of the observed abnormal grain growth will be delineated.

E3.12
OBSERVATION AND ELIMINATION OF DEFECT ON COPPER BOND PAD IN DUAL DAMASCENE COPPER INTERCONNECTS PROCESS INTEGRATION. Y.S. Zheng, Y.J. Su and P.D. Foo Department of Deep Submicron Integrated Circuits, Institute of Microelectronics, SINGAPORE.

As transistor scaling extends the 0.18um and below technology node, traditional metal aluminum interconnects and traditional silicon dioxide and silicon nitride dielectric materials will be progressively replaced by the multilevel metal copper interconnects and low-k dielectric materials during the integrated circuits process technology research and development. There are many challenges to be improved and solved because the process technology is a completely new technique. So the defect improvement and yield enhancement is important for IC manufacturability. Make full use powerful metrology tools, effective inspection, accelerating root cause analysis, improving process, reduction defect and enhancement yield is necessary. After pad opening plasma etching, photoresist stripping and post pad polymer removal with wet clean, many trace defects of polymer residue on Cu bond pad surface were observed. And bond pad peeling at copper and Ta (Al) interface was also observed. The different analysis results with different process treatment were obtained. In this study, Scanning Electron Microscope (SEM), Focused Ion Beam (FIB), Atomic Force Microscope (AFM), Auger Electron Spectroscopy (AES) and Energy Dispersive X-ray (EDX) and so on were used to review and to classify such defects generated from pad opening plasma etching process. Some special defects on Cu bond pad were discovered, observed and investigated in details with different processes treatment, and Chemical composition and thickness of this defect were analyzed before Ta+Al deposition. A clear Cu bond pad surface was obtained by using optimized pad opening plasma etch recipe and improved photoresist stripping methods and optimized post pad polymer residue removal methods wet clean recipe. A clear Cu bond pad will contribute to obtainment good adhesion and good ohmic contact between Cu and Al bond pad.

E3.13
ASYMMETRY OF ELECTROMIGRATION LIFETIME OF UPPER

LAYER AND LOWER LAYER Cu LINE IN Cu DUAL DAMASCENE PROCESS. Q. Guo, A. Krishnamoorthy, N.Y. Huang and P.D. Foo.

Electromigration (EM) is a major reliability concern of Cu interconnects in the ultralarge scale integration (ULSI) technology. Extensive studies have been performed to understand the failure mechanism. It has been shown that the failure mechanism of Cu interconnect is more complicated than that of Al(Cu) interconnect (1). In this paper, we investigate EM failure mechanism of Cu dual damascene interconnects. 2 types of via terminated structures A and B were employed in the study. The structure A consists of Main line of M2 (upper layer), via and side lines of M1 (lower layer). The side lines connected to pads were short and wide such that voids would be formed in the main lines between the via. The structure B is the inverse of structure A. EM tests were carried out with DC current densities ranging from 0.8MA/cm2 to 2MA/cm2 and temperatures of 300°C, 325°C and 350°C. In structure A, two failure modes, gradual mode and abrupt mode, were observed. In gradual mode, the structure increases the resistance gradually and microstructure analysis reveals the failure mechanism is fast diffusion of Cu in the interface between Cu and SiN. Activation energy Ea was found to be 0.85eV, in agreement with the previous report (2). The abrupt mode is a new failure mechanism. The failures of structure B can also be classified into gradual mode and abrupt mode according to their resistance degradation profiles. Interestingly, microstructure analysis showed that the failure mechanism of abrupt mode of structure B is the same as that of gradual mode of structure A, but with a much smaller Ea. The degradation behavior and strong degradation of Ea in EM of lower layer Cu line clearly demonstrate the asymmetry of EM lifetime of upper layer and lower layer Cu line in Cu dual damascene process. Reference: 1. J. Proost, T. Hirato, T. Furuhara, K. Maex, J.-p. Cellis, J. Appl. Phys., 87, 2792, (2000). 2. C-K. Hu, R. Rosenbergy, H. Rathore, D. Ngugen, Proceedings of IITC 1999, p.267.

E3.14

Ta THICKNESS EFFECT ON THE SiN PEELING FROM BLACK DIAMOND (BD) IN THE FABRICATION PROCESS OF Cu/BD PASSIVE DEVICE ON SILICON. Yu Mingbin, Li Chaoyong, Yap Kuanpei, Zhang Yibin, My The Doan and Foo Pang Dow, Institute of Microelectronics, Deep Submicron Integrated Circuit, SINGAPORE.

On chip high-Q passive devices are key elements in high performance radio-frequency (RF) analog integrated circuits. In Al and SiO2 technology, the aluminum ohmic loss and silicon substrate loss are the two major reasons that limit the passive device performance at microwave frequency. High Q inductor and high capacitance density capacitor Cu/SiO2 system have been achieved in CMOS compatible Cu interconnection technology on high loss silicon substrate. The reduction of the substrate loss remains the major hurdle for high performance passive devices. To reduce the standard CMOS-grade silicon substrate loss, low k dielectric layers are being used between passive devices and silicon substrate. In this paper, we report a Si-chip passive device fabrication process issue in Cu and BD backend interconnection technology and corresponding solution. On chip inductors and capacitors were built in the top two metal layers (M3 and M4) on silicon substrate. Integrated capacitor bottom Cu plate was built in M3 and upper plate in M4 with a Ta layer under Cu for preventing Cu diffusion into the SiN dielectric layer of capacitor. Peeling was noticed after 1000 $\AA$ Ta film deposition on top of SiN. The SEM inspection revealed that the peeling happened at the interface between BD and SiN indicating that peeling was easier to happen from top of BD area than from M3 Cu area. BD surface was altered by dry etch and Cu CMP process which resulted in poor interface adhesion between BD and SiN. The thick Ta film deposition process was found to cause Ta and SiN peeling together from M3 layer. The Ta/SiN peeling was solved by decreasing Ta film thickness to 500 $\AA$. Full process technology based on Cu and low k process line for integrating inductor and capacitor on silicon substrate was thus successfully developed.

E3.15

LOW TEMPERATURE GROWTH OF Cu SILICIDE AT THE Ag(Cu)/Si INTERFACE UPON ANNEALING AND ITS EFFECTS ON ADHESION, RESISTIVITY, AND OHMIC CONTACTS. Sungjin Hong, Seob Lee, Heejung Yang, Jiyoung Kim, Jaegab Lee, Koomin Univ, School of Advanced Materials Engineering, Seoul, KOREA; Beomseok Cho, Changoh Jeong, Kyuha Chung, Samsung Electronics Co., LTD Yongin.

Ag has received attentions as a potential interconnection in ultra-large scale integration and large area TFT/LCDs because of its lowest resistivity among metals and high electromigration resistance. In addition, it exhibits the stable contact with silicon substrate due to the negligible reaction between Ag and Si, implying no requirement of diffusion barriers against Ag diffusion. However, no chemical reactions occurring at a Ag/Si interface cause poor adhesion of Ag to Si, which must be addressed to implement the Ag/Si contacts into the devices. In contrast, Cu can react with Si to form the Cu silicide at the low temperature, possibly affecting the contact properties. Therefore, Ag(Cu) alloy films were used to enhance the adhesion properties to Si and the electrical properties. 200 nm-thick Ag(40at.% Cu) alloy films have been sputter-deposited on HF-cleaned Si substrate and then annealed at 200 to 800° to form the interface Cu3Si layer in the Ag(Cu)/Si structure. AES analysis reveals that annealing at 200° allowed the fast diffusion of Cu to the Ag(Cu)/Si interface, and forming the Cu3Si layer at the interface. As a result, the content of Cu in Ag(Cu) film decreased to about 20 at.% and the resistivity remarkably dropped to 2.25 $\mu\Omega$·cm from 5.0 $\mu\Omega$·cm of the as-deposited film. According to XTEM of Cu(Ag)/Si annealed at 200°, the uniform thickness (about 200 nm) of Cu3Si layer was grown at the interface; the 70 nm-thick Cu3Si was in the metal side, the 130 nm-thick in the silicon side. In addition, the Ag(Cu)/Si contacts show the ohmic contact characteristics and the enhanced adhesion properties, probably due to the uniformly formed silicide layer at the interface. Raising the temperature to 300° increases the thickness of silicide to 28 nm and reduces the content of Cu to less than 10 at.%. Consequently, Ag(Cu) alloy films on Si can be applied, especially to the source/drain metallization in large area TFT/LCDs because the low temperature growth of Cu silicide at the Ag(Cu)/Si interface can meet the thermal budget (below 300°) limited by the glass temperature, achieving the low resistivity, enhanced adhesion properties, and ohmic contacts.

E3.16

COMPARISON OF THE TIME-DEPENDENT PHYSICAL PROCESSES IN THE ELECTROMIGRATION OF DEEP SUBMICRON COPPER AND ALUMINUM INTERCONNECTS. Guan Zhang, Cher Ming Tan, Zhenghao Gan, Prasad Krishnamachar and Dao Hua Zhang, School of EEE, Nanyang Technological University, SINGAPORE.

Electromigration process is a complex process that involves many different physical processes. For a bamboo metallization, the various physical processes that constitute electromigration are the presence of electron wind force due to external current density, the presence of temperature gradient due to Joule heating and non-uniform heat dissipation especially when voids are present, and the presence of stress gradient due to different thermal expansivities of metal interconnect and the surrounding dielectric and barrier layer. When voids are present, there is also an additional component, namely the surface migration that exists that could cause a change in void volume and shape. All these physical processes are time varying during electromigration process. In this work, we have developed a 3D electromigration model based on the work developed by Dalleau and Weide-Zaage. Some physical processes are added in the model that are not included in the previous model such as the surface diffusion and vacancies generation energy for the substitutional atomic diffusion during electromigration. This will be presented in this work. With this model, we study the different time varying behaviors in aluminum and copper. Although it is known that one of the main different between Al and Cu is that the interface diffusion of Cu/Si3N4 is more significant that Al/ Si3N4, there are other differences that can only be revealed from the simulation, and it is these other differences that will be presented in this work. While the interface diffusion might account for the initiation of voids, these other processes will determine the time to failure and the 3D evolution of the shape of the voids initiated. In particular, we observed that electromigration in Al is mainly driven by the electron wind force. The effects of temperature and stress gradients are found to be insignificant. However, the reverse is true for electromigration in Cu. It is only after certain time that the electron wind force will dominate the electromigration process. This would make the thermo-mechanical properties of the dielectric surrounding the Cu lines important in determining its electromigration performance

E3.17

BARRIER CHARACTERISTICS OF TaN FILMS DEPOSITED BY REMOTE PLASMA ENHANCED ATOMIC LAYER DEPOSITION (ALD) METHOD USING METAL ORGANIC PRECURSOR. Do Youl Kim, Ju Youn Kim, Yangdo Kim, and Hyeongtag Jeon, Division of Materials Science & Engineering, Hanyang Univ., Seoul, KOREA.

As the integrated circuit (IC) feature sizes shrink to deep submicron scale, the need for conformal and reliable barrier metal deposition has become more important. Transition metal nitrides, such as TiN, TaN, and WN have been studied to establish thermally stable and adhesive metallization schemes with low resistivity. Especially, TaN has been investigated as Cu diffusion barrier in ultra large scale integrated (ULSI) devices. For these reasons, we investigated properties of TaN films deposited by remote plasma enhanced atomic layer deposition (PEALD) method using metal organic precursor, pentakis ethylmethly amino tantalum (PEMAT). Hydrogen and/or nitrogen

remote plasma was used to reduce the impurities incorporation and to enhance the barrier properties. TaN films were deposited under various conditions such as the plasma power, exposure time, gas flow rate and temperature. The efficiency of plasma treatment was systematically evaluated to optimize the processing conditions. TaN films were analyzed using Auger electron spectroscopy (AES), x-ray photoelectron spectroscopy (XPS), Rutherford backscattering spectrometer (RBS), cross-sectional transmission electron microscope (XTEM) and four-point probe method. This paper will present about the characteristics of TaN films deposited by remote PEALD method using metal organic precursor.

E3.18
SELECTIVE Cu FILLING OF VIAS BY USING ALD-LIKE Cu AND SELF-ASSEMBLED MONOLAYERS (SAMs). Doosick Park, Jaebum Park, Heejung Yang, Hyunjung Shin, Jiyoung Kim, Jaegab Lee, Kookmin. Univ, School of Advanced Materials Engineering, Seoul, KOREA; MyungMo Sung, Kookmin Univ., Dept of Chemistrys, Seoul, KOREA.

Direct Cu filling over high aspect ratio contacts (or vias) has been highly desirable for the design rules below 0.1 mm. An ALD-like Cu process combined with SAMs for the highly selective deposition of low resistivity copper films onto conductive substates has been investigated. The use of SAMs such as OTS (Octadecyl-Trichloro-Silane) can modify the surface properties of SiO_2, and remarkably increasing the selectivity over conductor substrates such as tungsten. In addition, ALD-like Cu process can be utilized to further improve the selectivity by limiting the growth rate. SAMs were formed on SiO_2 by dipping the substrate in a solution of the organosilane compound dissolved in toluene. OTS coated SiO_2 surface prolongs the incubation periods for the nucleation of Cu at the low temperature, significantly increasing the selectivity of tungsten substrate over SiO_2 for Cu deposition. 2.0 μm-thick SiO_2 coated tungsten/Si subtrates were used to pattern 0.3 um-diameter via holes. Selective deposition of Cu by using (hfac)Cu(1,5-DMB)(3,3 dimethy-1-butene) as a precursor has been carried out over the 7.0 a/r via hole patterns, followed by dipping in the OTS solution. The results show the bottom-up growth of Cu over tungsten substrate, and filling of 7.0 a/r (aspect ratio) vias with no deposition of the surface of SiO_2. However, careful inspection of Cu filling of 7.0 a/r vias reveals that bottom-up growth of Cu on tungsten substrates occurs about 0.5 um high, and then Cu particles produced from the gas phase reactions filling the remaining holes possibly due to the high supersaturation for the Cu nucleation. ALD-like Cu process can control the supersaturation of Cu, providing the complete filling of Cu on 7.0 a/r via holes.

E3.19
THE LEAKAGE CURRENT MECHANISMS OF Cu/POROUS SILICA DAMASCENE STRUCTURE WITH NANO-CLUSTER TASIX BARRIER. Chung-Hsien Chen, Chin-Piao Chang, Department of Electrical Engineering, National Tsing-Hua University, Hsinchu, TAIWAN; Fon-Shan Huang, Institute of Electronics Engineering, National Tsing-Hua University, Hsinchu, TAIWAN.

The leakage current of Cu/porous silica damascene structures with TaSix as barrier layer was investigated. TaSix films were prepared by dc sputtering with a Ta_5Si_3 target at sputtering power/gas pressure of 500 W/90 mtorr. The $TaSi_{0.42}$ films were nano-cluster structures that were verified by x-ray diffraction data. The line-to-line leakage current density (J_L) verse the electric field (E) were measured at various temperatures. The $Ln(J_L)$-$(E)^{1/2}$ plots show the linearly dependent with $(E)^{1/2}$ corresponding to Frenkel-Poole emission due to field-enhanced thermal excitation of trapped electrons of porous silica film. Meanwhile, the leakage current increases with temperature increasing. The same structures with TaN barrier after CMP NH_3-plasma post cleaning were also studied. The NH_3-plasma can clean the residual Ta of TaN barrier but damage the surface. It leads large leakage current in this structure. The leakage current data is deviated from F-P mechanism. From Auger mapping, we observe that the sputtered Ta and Cu atoms are randomly scattered and deposited on the top surface of dielectric film of samples with TaN. But the clear Cu lines and no Ta residue on the porous silica are found on Auger mapping of sample with TaSix. We believe that the CMP processes with traditional NH_4OH post-CMP cleaning can remove the Ta residue easily, the leakage current will be improved. In reliability study, the bias-temperature stress measurement was evaluated. The sample with nano-cluster TaSix as barrier has the best performance among those samples.

E3.20
NANO-CLUSTER Ta-Si DIFFUSION BARRIER. Da-Wei Lin, Institute of Electronics Engineering, National Tsing-Hua University, Hsinchu, TAIWAN; Chung-Hsien Chen, Department of Electrical Engineering, National Tsing-Hua University, Hsinchu, TAIWAN; Li-Sheng Ke, Fon-Shan Huang, Institute of Electronics Engineering, National Tsing-Hua University, Hsinchu, TAIWAN.

The sputtered Ta-Si nanostructure film was investigated as a barrier material for Cu metallization. The Ta-Si film was deposited by co-sputtering of Ta and Si targets in Ar gas. Four point probe, AES, XRD, HRTEM, and I-V measurement were employed to understand the resistivity, chemical composition, crystalline microstructure, and resistivity-temperature. Furthermore, the MOS capacitors of Cu/Ta-Si(13nm)/ SiO_2 /p-Si structure were annealed at the temperature from 450°C to 600°C. From the flat band shift, the diffusion barrier performance can be evaluated. Ta-Si film with large Si/Ta composition ratio has higher resistivity and shows better diffusion barrier performance. The resistivity of Ta-Si film with Si/Ta ratio 1.043 is 444 $\mu\Omega$·cm. The C-V curve of MOS capacitor Cu/Ta-Si($\sim$13.2nm)/SiO_2/Si show that it remains thermally stable after annealing at temperature 600°C. For Si/Ta ratio 0.278, The thermal stable temperature is about 400°C. The resistivity is 267$\mu\Omega$·cm. The XRD pattern shows Ta-Si film is nano-cluster (amorphous) structure. HRTEM pictures shows that average size of Ta-rich and Si-rich nano-clusters is smaller than 5 nm. The resistivity of Ta-Si film decreases as the temperature rises. But I-V characters show the ohmic behavior. We propose a model which can successfully explain the above electrical characteristic relation. CMP technology of $TaSi_x$ film was also developed. From Auger mapping, Ta residues are hardly found on the surface of porous SiO_2. According to above measurements, the properties of Ta-Si nano-cluster thin film can be understood and the optimum deposition condition of diffusion barrier can also be determined.

E3.21
EFFECT OF GRAIN STRUCTURE ON THE ELASTIC PROPERTIES OF ELECTROPLATED COPPER FILMS. A.A. Maznev, M. Gostein, Philips, Natick, MA; S.H. Brongersma, IMEC, Leuven, BELGIUM.

The microelectronics industry is adopting electroplated copper as the new material of choice for electrical interconnects in high-performance integrated circuits. Here we have investigated the elastic properties of electroplated copper films as a function of variations in the grain structure of the films that result from different deposition and annealing conditions. The elastic properties are of intrinsic interest because they govern how the film responds to stress created by processing. Furthermore, calibrated elastic property values are required for non-contact determination of film thickness by laser-induced ultrasonic wave techniques, which are being introduced for metal thickness metrology in advanced manufacturing processes. [1] Variations in the concentrations of plating bath additives and plating current have been previously shown to produce variations in the grain size and the volume fractions of different crystallographic grain orientations; furthermore, annealing of the films causes grain growth and changes the grain texture. [2] As a result, the elastic properties of electroplated films depend on preparation conditions, because average elastic moduli depend on grain structure. We have prepared electroplated copper films under a variety of conditions and characterized the grain structure of the films using x-ray diffraction and scanning electron microscopy. We then characterized the elastic properties of these films by measuring the dispersion of laser-induced surface acoustic waves and analyzing the dispersion relations with a physical model. [1] M. Gostein, et al, in Handbook of Silicon Semiconductor Metrology, ed. Alain Diebold (Marcel Dekker, New York, 2001), pp. 167-196. [2] S.H. Brongersma, et al, J. Mater. Res., Vol. 17, No. 3, 2002.

E3.22
DEPOSITION AND CHARACTERISTICS OF TANTALUM NITRIDE FILMS BY PLASMA ASSISTED ATOMIC LAYER DEPOSITION AS Cu DIFFUSION BARRIERS. Se-Jong Park, Kyung-Il Na, [a]Woo-Cheol Jeong, [a]Se-Hoon Kim, [a]Sung-Eun Boo, [a]Nam-Jin Bae and Jung-Hee Lee The School of Electronic and Electrical Engineering, Kyungpook National University, Daegu, KOREA; [a]Comtecs Incorporated, Daegu, KOREA.

For a diffusion barrier against Cu, tantalum nitride films have been successfully deposited on SiO_2 by plasma assisted atomic layer deposition(PAALD), using pentakis (ethylmethlyamino) tantalum (PEMAT) and ammonia as precursors. TaN film was also grown by conventional ALD to compare the barrier properties for both films. The growth rate of PAALD TaN at substrate temperature 250°C was slightly higher than that of conventional ALD TaN (0.80Å/cycle for PAALD and 0.75Å/cycle for conventional ALD). The properties of TaN films as diffusion barriers were considerably improved by adopting PAALD. Density of TaN films grown by conventional ALD was as high as 8.3 g/cm^{3}and even higher density of 11.0 g/cm^3 film was obtained by PAALD. Negligible aging effect was observed for TaN films by PAALD because of its high density. The N:Ta ratio for conventional ALD TaN was 44:37 in composition and the film contained approximately 8$\sim$10 atomic % carbon and 11 atomic %

oxygen impurities. On the other hand the N:Ta ratio for PAALD TaN layers was 47:44 which is more stoichiometric compared to conventional ALD grown TaN film and the carbon and oxygen levels of TaN layers by PAALD were decreased to 3 atomic % and 4 atomic %, respectively. The resistivity for conventional ALD grown TaN films was 865200 $\mu\Omega$·cm. The resistivity of PAALD grown TaN film was greatly decreased to 1500 $\mu\Omega$·cm. TaN films by PAALD exhibit excellent step coverage for the trench with high aspect ratio of 15:1 (h/w = 1.8:0.12μm) but this is not the case for the conventional ALD. The stability of TaN films as a Cu-diffusion barrier was tested by thermal annealing for 30 minutes in N_2 ambient and characterized through XRD, AES and Cu etch pit analysis, which proves the PAALD grown TaN film maintains the barrier properties against Cu below 700°C.

E3.23
Abstract Withdrawn.

E3.24
BLECH LENGTH VS. TITANIUM-NITRIDE BARRIER THICKNESS. William K. Meyer and Raj Solanki, Oregon Health & Science University, Electrical & Computer Engineering Dept, Beaverton, OR; David Evans, Sharp Laboratories of America, Inc., Camas, WA.

A dual-damascene VLSI interconnect process included sputtered TiN as glue layer (to promote adhesion of electroplated copper) and barrier layer (to provide an electromigration (EM) blocking boundary at the vias). EM reliability measured with highly accelerated wafer-level stress tests showed that time-to-failure by resistance increase improves for shorter structures, as expected from the Blech effect. J*L, the product of stress current and Blech Length (segment length at which diffusion cancels electromigration drift velocity) measured for TiN thickness of 50-100nm is in agreement with simulations of pressure containment by thick-walled vessels. Results indicate that TiN must be >100nm to achieve useful J*L >1 Amp/micron. The tradeoff of high current in short lines vs. low resistance in narrow lines is discussed.

E3.25
GRAIN BOUNDARY AND TEXTURE OPTIMIZATION OF Al FILMS VIA EXCIMER LASER IRRADIATION. J.B. Choi and James S. Im, Program of Materials Science and Engineering, Department of Applied Physics and Applied Mathematics, Columbia University, New York, NY.

There are a number of cases in which incentives exist for manipulating the microstructure of thin films. For Al metallization, it is recognized that a large-grained "bamboo" microstructure with (111) texture is desirable for increasing the resistance of the materials to electromigration-induced failure. In this paper, we demonstrate that such a material can be attained using controlled excimer laser irradiation of Al films on SiO_2. The microstructural manipulation of Al films is accomplished via a lateral solidification technique, referred to as sequential lateral solidification (SLS), that was previously developed in order to provide low-defect-density crystalline silicon films on glass substrates. Depending on the details of the process (i.e., the shape of the patterned beamlets and the microtranslation sequence between the laser pulses), it is possible to obtain a variety of microstructures ranging from grain-boundary-location-engineered polycrystalline films to location-controlled single-crystal regions. For developing electromigration-failure-resistant Al films, the SLS method can be configured to produce a large-grained bamboo microstructure with periodically arranged grain boundaries with controlled locations. The attainment of (111) texture in SLS-processed Al films can be accomplished using either (1) SLS of as-deposited Al films with (111) texture, or (2) SLS of Al films with an equiaxed polycrystalline microstructure that results when the films are flood irradiated with an excimer laser pulse at fluences sufficiently high to fully melt the film. The experimental details include the following: irradiation of 200-nm Al films with and without (111) texture in as-deposited form using an excimer laser (XeCl, 308 nm, 30 ns FWHM), and SEM, AFM, and EBSP analyses of the films.

E3.26
ULTRATHIN POLYMERIC DIFFUSION BARRIERS FOR Cu METALLIZATION. P. Gopal Ganesan, S. McConaughy, G. Cui, S. Kanagalingam, R. Kane, and G. Ramanath, Department of Materials Science & Engineering, Rensselaer Polytechnic Institute, Troy, NY.

Devising <5-nm-thick barriers to inhibit Cu diffusion into adjacent dielectric layers is a major challenge to realize reliable interconnect structures for sub-100-nm devices. This is mainly due to difficulties in depositing conformal films of such thin layers of currently used barrier materials (e.g., transition-metal-based compounds), especially in non-planar geometries. Furthermore, structural and compositional changes, and grain boundary generation, caused by interfacial intermixing in nm-thick films of these materials degrade barrier efficiency. Here, we demonstrate a new approach of harnessing 3 to 5-nm-thick polymeric bilayers of polyacrylic acid(PAA) on polyethyleneimine(PEI), to inhibit Cu diffusion across dielectrics. The underlying rationale is to immobilize Cu through strong local interfacial bonding with molecular moieties, and create a vacuum-like potential barrier between the Cu and the dielectric to prevent Cu ionization and transport. We also investigate the adhesive properties of these layers at Cu/SiO_2 interfaces. Utilizing molecular structures as barriers open up possibilities of seamless integration of barriers with low-k materials to realize barrier-less dielectrics. Bias thermal annealing (BTA) tests of $Cu/PAA/PEI/SiO_2/Si(001)/Al$ structures at 200°C at 2 MV cm^{-1} field show >5-orders of magnitude lower leakage currents and more than a factor-of-4 increase in failure times compared with structures without the PAA/PEI bilayer. Increasing the number of bilayers do not have any observable effect on the failure time, suggesting that Cu immobilization at the Cu/PAA interface is the likely barrier mechanism. Four-point bend adhesion tests on $Cu/PAA/PEI/SiO_2$ reveal debond energy values of $\sim$3 J/m^2, comparable to that of reference Cu/SiO_2 interfaces. X-ray photoelectron spectroscopy measurements show that nitrogen is present on the Cu side of the delaminated interface, and not detectable on SiO_2 fracture surfaces, indicating that delamination is due to weak electrostatic interactions at the PEI/SiO_2 interface.

E3.27
ENHANCED ADHESION PROPERTY OF Cu ON LOW-k BY USING Ti GLUE LAYER, B DOPANT AND N2 PLASMA TREATMENT. Heejung Yang, Seob Lee, Yeonkyu Ko, Jiyoung Kim, Jaegab Lee, Kookmin Univ, School of Advanced Materials Engineering, Seoul, KOREA; Cheonman Shim, Donggeun Jung Department of Physics Sungkyunkwan Univ., Suwon, KOREA.

In order to reduce the R-C time delay of ULSI circuits and achieve highspeed performance, interconnection materials with low resistance and low dielectric constants should be applied to metallization in DRAM or LOGIC. Cu/low-k(PPpX(Plasma Polymerized para-Xylene):HMDS(hexamethyldisilane)) has received attentions as most promising material to overcome the limitation of conventional process using Al and SiO2. Because Cu has excellent electrical conductivity and low-k has lower dielectric constants(2.6), Cu/low-k structure has been satisfied with demand in future integrated circuits. However, poor adhesion characteristics between Cu and low-k must be solved to apply process. In this work, in order to solve these problems, titanium has been employed as an adhesion promoter layer and to improvement in adhesion between Cu and low-k, N2 plasma treatment performed on the surface low-k. Also, boron was added to Cu film to limit interfacial reaction due to Ti boride formation. Using Ti film glue layer on low-k has problem which is discontinuous reaction between Ti and low-k. In order to solve this problems, Ti film after N2 plasma treatment performed on surface was deposited. As effects of N2 plasma treatment have contamination free surface, controlling surface roughness and surface composition modification, Cu/Ti/N2 plasma/low-k multiplayer has good adhesion property. In addition, Continuous reaction between titanium and nitrogen rich surface low-k enhanced adhesion property. Ti boride formed in Cu(B)/Ti/low-k multiplayer after annealing inhibited Cu/Ti and Ti/low-k reaction. Therefore, Ti boride improved adhesion between Cu and low-k. Ti films with 20nm were sputterd on 400nm-thick low-k. 200 nm-thick Cu and Cu(5at.%B) alloy films have been sputterd on low-k deposited Si substrate and then annealed at 100 to 400°. N2 plasma treatment performed with 5mTorr and RF power of 500W for 90sec. Adhesion property has been measured by using scratch tester.

E3.28
VAPOR TREATMENT OF COPPER SURFACE USING ORGANIC ACIDS. Kenji Ishikawa, Teruo Yagishita, Moritaka Nakamura, Association of Super-Advanced Electronics Technologies (ASET), JAPAN.

In ultra-large-scale integrated circuits (ULSI) fabricated with interconnection using copper and low dielectric constant (low-k) materials, high quality via-contact formation is required. Surface damages such as oxidation and roughing of copper by post-plasma etch process, however, have been crucial to degrade device performances. Considering high reactivity of copper, vapor-phase methods for preparation of clean surface of copper are advantageous, because they are able to perform without exposure to atmospheric ambient. Thus, we have examined vapor treatments of copper surface using carboxylic acids. Samples were prepared as follow; initially a copper film was deposited on bare Si substrate by sputtering, then the copper film was oxidized under atmospheric ambient at below 200°C. Then the surface was exposed to acetic acid vapor controlling its vapor density using the permeation method. To monitor the cleaning process, we used real-time infrared reflection absorption spectroscopy (IR-RAS). By increasing vapor exposure time, an infrared absorption was clearly observed at around 1630 cm^{-1}, which indicates that

carboxylate anion (R-COO-) was formed on the surface. When the substrate was heated at about 200°C during the cleaning process, the oxidized copper was reduced and a shiny surface was observed. Volatile products were collected by a liquid nitrogen trap, then, analyzed by using liquid injection chromatography mass spectroscopy (LC-MS). It was shown that dominant product was copper (II) acetate ($(CH_3COO)_2$ Cu) and additionally higher mass components were detected. Through the kinetics of carboxylate formation and detailed analysis of chemical structure of products, properties of various organic acid vapor treatments will be discussed.
This work was supported by NEDO.

E3.29
THE STUDY OF MODIFIED LAYERS ON SiCOH DIELECTRICS USING SPECTROSCOPIC ELLIPSOMETRY. Marcus Worsley and Stacey Bent, Stanford University, Dept of Chemical Engineering, Stanford, CA; Stephen Gates, Kaushik Kumar, Timothy Dalton, IBM Research, Yorktown Heights, NY.

The current challenge in designing new low-k dielectrics is realizing sufficient mechanical and chemical stability such that the material can be integrated into current damascene schemes. The material of interest in this study is a nonporous SiCOH composite (carbon-doped silicon oxide) projected as a 90nm technology interlayer dielectric (ILD). During integration of this ILD, processing steps such as etch, resist strip and chemical-mechanical planarization are known to chemically alter a layer of the dielectric. Here, spectroscopic ellipsometry is used to characterize the modified layer of SiCOH films after exposure to different strip plasmas. The data are analyzed based on a 2-layer model, consisting of a carbon-deficient layer on the surface of the low-k dielectric. This model is supported by XPS data. The effects of two types of plasma etch chemistry on the formation of this modified layer were studied and found to be significant. The 2-layer model accurately describes the modifications produced by the oxidizing plasma, but its description of the modified layer formed by the reducing plasma is not complete. A 3-layer model with an additional nitrogen-doped layer is suggested.

SESSION E4: DEPOSITION AND MICROSTRUCTURE OF METAL FILMS
Chairs: John E. Sanchez and Carl V. Thompson
Wednesday Morning, April 23, 2003
Golden Gate B2 (Marriott)

8:30 AM *E4.1
Cu AND Cu ALLOY THIN FILMS: RESISTIVITY, TEXTURE AND GRAIN STRUCTURE. K. Barmak, A. Gungor, A.D. Rollett, Department of Materials Science and Engineering, Carnegie Mellon University, Pittsburgh, PA; C. Cabral Jr. and J.M.E. Harper, IBM T.J. Watson Research Center, Yorktown Heights, NY.

The need to reduce delays in integrated circuits prompted the replacement of Al(Cu) with Cu in the 1990's. However, as line widths approach 100 nm, the addition of alloying elements to tailor the grain size and texture, and thus the reliability and functionality, of Cu interconnections may become necessary. The impact of eleven alloying elements, namely Mg, Ti, In, Sn, Al, Ag, Co, Ir, Nb, W, and B, at two nominal concentrations of 1 and 3 at.%, on the resistivity, texture and grain structure of copper was investigated. The films were electron beam evaporated onto thermally oxidized Si wafers and had thicknesses in the range of 420-560 nm. Pure evaporated Cu films were used as controls. Isothermal anneals were carried out at 400°C for 5 hours; constant-heating rate treatments were done at 3°C/s to 650 and 950°C. In all cases, annealing resulted in the strengthening of film texture, the growth of grains and the lowering of resistivity when compared with the as-deposited state. In addition, the type and concentration of the alloying element affected the electrical and microstructural characteristics of the films. For example, with the exception of the Co-containing films, the grain sizes for the nominally 3 at.%, 400°C annealed films were smaller than those for the nominally 1.0 at.% films. After the 400°C anneal, Cu(0.4B) and Cu(1.0Ag) had the lowest resistivities at 2.0 and 2.1 micro-Ohm-cm, respectively, Cu(2.8Co) showed the largest average grain size at 1080 nm, and Cu(3.0Ti) had the strongest $< 111 >$ fiber texture at 94.2 vol%. The resistivity, grain size and $< 111 >$ vol% for the pure Cu film after the same anneal were 2.0 micro-Ohm-cm, 790 nm and 59.8, respectively. No alloy film simultaneously satisfied the requirements of a low resistivity, a larger grain size and a stronger texture than pure Cu.

9:00 AM E4.2
IMPACT OF ANNEALING ON THE RESISTIVITY OF ULTRAFINE Cu DAMASCENE INTERCONNECTS.
G. Steinlesberger[a,b], M. Engelhardt[a], G. Schindler[a], W. Steinhögl[a], M. Traving[a], W. Hönlein[a], E. Bertagnolli[b]. [a]Infineon Technologies, Corporate Research, Munich, GERMANY; [b]Vienna University of Technology, Vienna, AUSTRIA.

As the scaling of semiconductor technology continues, sub-100 nm interconnects are becoming the dominant factor determining high-speed reliable performance. A dramatic increase in resistivity was observed as the technology scales to smaller dimensions. This size effect is caused by charge carrier collisions at internal and external interfaces, which effectively reduce the mobility. Based on a comprehensive size effect model, it was found that grain boundary scattering dominates the resistivity increase. Thus, doubling the average grain size in 40 nm lines would lead to a 25% reduction in resistivity. Utilizing standard lithography and an adapted spacer technique, Cu damascene lines with widths down to 40 nm were fabricated. Prior to CMP, a post-plating anneal was carried out to enhance recrystallization. Both standard annealing in a tube furnace and low temperature rapid thermal annealing (RTA) were applied to two different sets of samples. After CMP and line passivation but prior to the pad window opening the samples with standard post-plating anneal were again thermally treated. Some samples were stored at 275°C for more than 3400 hours. Other samples were subjected to RTA at 500°C, 600°C or 700°C for 10 minutes. Finally, the electrical resistance of different line widths, heights and lengths was measured for both sets of samples. The influence of temperature and duration of low temperature RTA on the Cu microstructure was compared to standard annealing. It was found that the resistance decreases with increasing time and temperature. For narrow lines a 40% decrease of the resistance was observed. For higher temperatures larger Cu grains and outgrowth particularly at the grain boundaries were detected by AFM. For the samples, which where thermally treated after passivation deposition, the resistance did not change significantly even after long time storage at 275°C. Moreover hillock formation was observed during RTA at 600°C and 700°C of the finished lines resulting in an undesirable increase of the resistance. The results demonstrate that Cu within damascene trenches does not recrystallize especially once the excess copper is removed by CMP and the lines are passivated.

9:15 AM E4.3
INFLUENCE OF PLATING CONDITIONS ON THE DYNAMICS OF COPPER GRAIN GROWTH DURING THERMAL ANNEALING. Sywert Brongersma, IMEC, Leuven, BELGIUM; Jan D'Haen, Kris Vanstreels, Ward DeCeuninck, IMOMEC, Diepenbeek, BELGIUM; Karen Maex, IMEC, Leuven, BELGIUM, and also E.E.Dept., Katholieke Universiteit Leuven, Leuven, BELGIUM.

The recrystallization behavior of thin electroplated Copper films has been extensively studied by many groups and is understood quite well. Both the as-deposited grain size and the incorporation of impurities from the plating chemistry have a large effect on the final crystallography, grain size, and time-scale of observed changes in stress, sheet resistance and grain growth. In narrow structures, however, conflicting results have been reported and in fact the behavior, once again, depends strongly on the composition of the plating chemistry. Line-resistance shows e.g. that for one chemistry the recrystallization accelerates for narrow lines while it decellerates for another. In order to obtain a better understanding we now compare the behavior for several chemistries using a combination of traditional methods and a dynamic monotoring of grain growth in a FE-SEM at various elevated temperatures. The resulting "movies" show great detail on where secondary grains preferentially start to grow and how their growth proceeds in lines of various widths. This is leading to new insight about the evolution of grain sizes and orientations in reduced dimensions.

9:30 AM E4.4
COMPUTER SIMULATION OF MICROSTRUCTURE EVOLUTION IN DAMASCENE INTERCONNECTS: EFFECTS OF TRENCH WIDTH AND OVERBURDEN THICKNESS.
Jung-Kyu Jung and Young-Chang Joo, Seoul National University, School of Materials Science and Engineering, Seoul, KOREA; Young-Joon Park, Texas Instruments Incorporated, Dallas, TX; Nong-Moon Hwang, Center for Microstructure Science of Materials, Seoul National University, Seoul and Korea Research Institute of Science and Standards, Taejon, KOREA.

We study the characteristics of grain growth in a damascene trench structure, which is used for fabrication of Cu interconnects, by means of three-dimensional grain growth simulation. The characteristics of grain growth in a trench are complicated because of not only simultaneous growth from the bottom and the sidewalls inside the trench but also the competition between grain growth from the trench and that from the overburden, an excessive metal layer over trenches. To investigate the mechanism of the competitive microstructure evolution in such a structure, we use the Monte Carlo method based on the modified Potts model for three-dimensional computer simulation. We take various parameters like line width, overburden

thickness, etc. into account. Simulation results show that the grain sizes of damascene interconnects are restricted by the overburden thickness or the trench width when the grains are in the overburden or the trench, respectively. Thus the grains from the overburden dominate the microstructure in the trench when the trench is sufficiently narrow and the overburden is thick enough. To see this effect quantitatively, we analyze the grain sizes in simulation damascene structures and compare the evolution kinetics. The results indicate that effect of overburden thickness is significant to microstructure evolution characteristics in damascene structures. Effect of line width is less significant, but it affects the growth kinetics. Understanding of the effect would provide a key to optimize the process for fabrication of damascene interconnects with the optimized reliability.

9:45 AM E4.5
OBSERVATION OF GRAIN GROWTH IN Cu FILMS BY IN-SITU EBSD ANALYSIS. David P. Field, School of Mech. and Matls. Eng, Washington State University, Pullman, WA; Matthew M. Nowell, TexSEM Laboratories, Draper, UT; and Oleg V. Kononenko, Russian Academy of Science, Chernogolovka, RUSSIA.

Recrystallization, grain growth and crystallographic texture evolution in Cu films is an area of importance for IC interconnect fabrication as the film characteristics influence the resulting line microstructure. This study examines Cu films deposited by partially ionized beam deposition onto a sublayer of tantalum nitride and additionally onto alpha-C:H. The films were annealed in-situ in the SEM chamber and intermittent orientation imaging was used to characterize the grain growth and crystallographic texture evolution in the films. Both initial and final textures are weak in each of the films analyzed, but grain growth is observed to be a function of grain boundary structure. Results are discussed in terms of how interconnect line reliability might be influenced by Cu microstructure.

10:30 AM E4.6
SEQUENCE AND MECHANISMS OF Mg SEGREGATION AND SELF-ORGANIZED INTERFACIAL MgO FORMATION IN Cu-Mg ALLOY FILMS ON SiO_2. M.J. Frederick, G. Ramanath, Rensselaer Polytechnic Inst., Dept of Materials Science and Engineering, Troy, NY.

Alloying Cu with small amounts ($\sim$1-2 at.%) of Mg is an attractive strategy to improve Cu interconnect reliability with minimal increase in film resistivity. It has been shown that Cu-Mg alloys have higher electromigration and corrosion resistance and interfacial adhesion compared with elemental films, and inhibit Cu diffusion into SiO_2-based dielectrics. Recent studies have, based on compositional depth profiles, attributed these enhancements to Mg segregation, and self-organized formation of interfacial MgO. Here, we describe the sequence and atomistic mechanisms of Mg segregation, phase evolution in the film, and reactions on the Cu surface and at the Cu/SiO_2 interface. Our findings are based on in situ differential resistivity measurements during vacuum annealing, and ex situ high-resolution transmission electron microscopy (HRTEM), electron and X-ray diffraction, and Rutherford Backscattering Spectrometry (RBS). Mg segregates exclusively to the film surface between 200-400°C, and results in the growth of a surface oxide layer. This is accompanied by grain growth and Cu_2Mg formation dispersed throughout the film, and a 40% decrease in film resistivity. Above 400°C, Mg segregates to the interface, where it reduces SiO_2 and forms a laterally uniform 20-nm-thick layer comprised of fcc MgO. In many locations, the MgO grains are epitaxially oriented with respect to Cu grains across the interface. We also observe non-cubic phases that can be indexed as monoclinic $CuMgSi_2O_6$ or a tetragonal Cu silicide. This interfacial reaction releases Si into the film, leading to a 3-fold increase in resistivity. Analysis of resistivity-temperature characteristics obtained at different annealing rates ranging from 0.2-5°C/min reveals an activation energy of 2.5$\pm$0.1 eV for the Mg/SiO_2 interfacial reaction. Based upon these results, we present a phenomenological model describing the atomistic mechanism of Mg segregation and phase formation. The resultant effects on film texture evolution will also be discussed.

10:45 AM E4.7
A NOVEL METHOD TO QUANTIFY THE GRAIN STRUCTURE FOR DAMASCENE CU LINES USING X-RAY POLE PLOTS. Jong-Min Paik, Young-Chang Joo, Seoul National Univ, School of Materials Science and Engineering, Seoul, KOREA.

We investigated line geometry dependence of central peak shape in the (111) pole figures of damascene Cu lines and its relationship with grain structures. In the USG (undoped silica glass) passivated Cu lines with 0.18 μm in width, central pole spreads more broadly across the trenches than along the trenches in the (111) pole figure. Moreover, in the pole figure of 2 μm lines, central pole was observed to be split into two peaks separated by approximately 6 degrees. This anisotropic peak shape is attributed to the tilted sidewall angles because tilted (111) grain is energetically favorable in case that sidewall is inclined toward the direction across the trenches. From the rocking curves along the trenches and across the trenches, we confirmed that the central peak was composed of three peaks; one from exactly (111) oriented grains and two from tilted (111) oriented grains. The BD (black diamond) passivated Cu lines whose side wall angle is larger than USG passivated lines, have also 3 poles and they are separated by as much as 8 degrees. Considering the interface energies as grain structures, we concluded that the exact (111) pole and tilted (111) pole is attributed to the bamboo grains and poly-granular clusters, respectively. Using this concept, fraction of bamboo and polygranular clusters was quantified by analyzing the central peak in the pole plots. The results from XRD agree well with those from microscopy images. Grain structure quantification method using XRD is a simple and non-destructive so it is expected to be very powerful in the interconnects reliability assessment.

11:00 AM E4.8
A NOVEL TECHNIQUE TO RE-CONSTRUCT THREE DIMENSIONAL VOID IN PASSIVATED METAL INTERCONNECTS. Cher Ming Tan, Zhenghao Gan, Krishnamachar Prasad and Dao Hua Zhang Nanyang Technological University, School of EEE, SINGAPORE.

The metal interconnects in ULSI generally contain voids. These voids could be due to processing or electromigration or stress migration. The presence of voids is becoming more serious as the metal line width is decreasing. The voids can be very tiny (as small as 50 nm), but its presence could affect the reliability of the interconnection, especially for narrow metal line width. Presently, the voids are found using manual inspection under SEM. As metal line becomes long and narrow, such a method becomes too tedious and ineffective. Many methods are proposed and patented, but they have their shortcomings. In the present work, a novel method is proposed to locate voids in metal interconnections rapidly and non-destructively. In this method, a constant current is applied to a metal interconnection while an electron beam is scanning and impinging upon the surface of the sample. The voltage at the terminals is monitored simultaneously during electron beam scanning. Resistance change, and hence voltage perturbation are expected when the electron beam approaches the defective area due to uneven electron beam heating and heat transmission. Information on defects or voids is thus obtained by analyzing the voltage alteration. It is found that the recorded voltage perturbation is not dependent of the length of the interconnect, but a linear function of the void volume. Thus, the method is useful as the metal length has increased tremendously as in the copper technology. In addition, it can also provide the void size and depth, with the possibility to re-construct the entire void shape in 3D. The resolution of the method is shown to go as low as 50 nm.

11:15 AM E4.9
HIGH-FREQUENCY HETERODYNE FORCE MICROSCOPY INVESTIGATIONS OF COPPER INTERCONNECTS. Yuegui Zheng, Robert Geer, School of NanoSciences and NanoEngineering, University at Albany, Albany, NY.

A nondestructive methodology for characterizing Cu interconnects has long been sought and has motivated significant efforts regarding metrology tool development. Here, we present investigations of high-frequency heterodyne force microscopy (HFM) to investigate the surface and subsurface mechanical response of damascene Cu interconnect test structures in a silicon oxide dielectric. HFM measures with nanometer resolution the variation of phase delay of an acoustic probe wave transmitted through a material to investigate subsurface defects, interfacial delamination, and mechanical nonuniformity. Simultaneous acoustic signals are supplied to the sample and scanning probe microscope probe tip to generate a heterodyne signal sensitive to the relative phase differences of the two acoustic waves. Phase delay differences on the order of 25 ps have been measured across Cu interconnect lines in a silicon oxide dielectric for an 80 MHz heterodyne carrier frequency. The measured phase delay agrees with estimates based on relative sound velocity differentials between the two materials. This phase difference has been used to characterize surface and subsurface defects within the Cu interconnect resulting from thermal annealing. A simple model is presented to describe the HFM imaging results in terms of relative acoustic phase delay expected for such materials.

11:30 AM E4.10
ATOMIC LAYER DEPOSITION OF HIGHLY CONFORMAL COPPER AND COBALT METAL FILMS. Booyong S. Lim and Roy G. Gordon.

Electrically conductive films of copper and of cobalt were formed by atomic layer deposition from novel precursors. The syntheses and properties of the precursors will be described. Smooth cobalt films

nucleated uniformly and densely on hydroxylated silica surfaces and on tungsten nitride diffusion barriers. Rough copper films nucleated sparsely and were agglomerated when grown on the same substrates. By growing a thin cobalt film followed immediately by a copper film, smooth and adherent copper films were produced. The metal films were found to be highly conformal, with uniform step coverage in holes with aspect ratios over 60:1. These films appear to be suitable as adhesion/seed layers in copper interconnects and as magnetoresistive multilayers in magnetic storage devices.

11:45 AM E4.11
AFM STUDIES OF DEFORMATION AND INTERFACIAL SLIDING IN INTERCONNECT STRUCTURES IN MICROELECTRONIC DEVICES. C. Park, I. Dutta, K.A. Peterson, Center for Materials Science and Engineering, Department of Mechanical Engineering, Naval Postgraduate School, Monterey, CA; J. Vella, Process Materials Characterization Lab, Motorola, Tempe, AZ.

High stresses can develop in back-end interconnect structures (BEIS) of micro-electronic devices during thermal excursions, because of the large differences in thermal expansion coefficients (CTE) between Si, the interlayer dielectric and the interconnect lines. Here we use atomic force microscopy (AFM) to study plastic deformation and interfacial sliding of Cu interconnect lines on Si, embedded in two different types of low K dielectric (LKD). Following thermal cycling, changes were observed in both in-plane Cu line dimensions, as well as the out-of plane step height between Cu and dielectric in single layer structures. The results of AFM measurements following ex-situ thermal cycling between 293 and 723K, and in-situ thermal cycling between 293K and 398K, will be presented, and the differences due to LKD properties will be highlighted. These observations will be rationalized on the basis of some simple modeling studies, utilizing insights from ongoing work on the mechanism and kinetics of interfacial sliding kinetics. The roles of deformation and interfacial sliding on the stability of Cu-low K interconnect structures under package-level stresses will also be presented.

SESSION E5: NOVEL INTERCONNECT CONCEPTS
Chairs: Vincent J. McGahay and Dorel Toma
Wednesday Afternoon, April 23, 2003
Golden Gate B2 (Marriott)

1:30 PM *E5.1
AIR DIELECTRIC FABRICATION VIA CVD SACRIFICIAL MATERIALS. Kelvin Chan, Thomas B. Casserly, Leslie S. Loo, and Karen K. Gleason, Dept. of Chemical Engineering, MIT, Cambridge, MA.

The ultimate reduction in interconnect delay, power consumption, and cross-talk requires air as the dielectric. Air has the lowest dielectric constant of 1.0. It also has the lowest refractive index of 1.0, and the replacement of current low-index material with air would enable high-reflectance optical filters to be made with fewer layers. Fabricating multilevel structures having of air as the dielectric requires improved materials and integration schemes for sacrificial layers. A sacrificial material having excellent mechanical properties and adhesion will make the interconnect structure sufficiently robust to survive all integration steps such as chemical mechanical polishing. The final removal of the sacrificial layer should be facile, occurring at low decomposition temperatures with minimal residue left behind. Long decomposition periods or temperatures in excess of 400°C are to be avoided. Also, liquid-phase etching is undesirable, as surface tension effects can lead to pattern collapse. Chemical vapor deposition (CVD) of a sacrificial layer would be an evolutionary step to extend the toolsets for CVD low-k dielectrics such as Si:O:C:H films. Organic polymers are promising candidates for sacrificial layer formation. However, traditional CVD methods for growing organic films typically involve plasma excitation and lead to highly branched and crosslinked materials. Novel CVD processes will be discussed which maintain the linear chain structure of organic polymers and permit clean decomposition via an unzipping mechanism. In particular, CVD polyoxymethylene (POM) holds great candidate for the sacrificial material, having both a high mechanical modulus and low decomposition temperature. As a bulk synthetic polymer, having trade names including Delrin, POM and is utilized for turbine blades and other engineering plastics applications. Decomposition of POM cleanly produces formaldehyde with no high molecular weight residual products.

2:00 PM E5.2
SELECTION OF AN OVERLYING DIELECTRIC AND SACRIFICIAL MATERIAL FOR AIR GAP FABRICATION. Thomas B. Casserly, Karen K. Gleason, Massachusetts Institute of Technology, Dept of Chemical Engineering, Cambridge, MA.

As feature size in integrated circuits continues to decrease the development of low dielectric constant, k, solutions is increasingly important. The ultimate low-k solution is air as a dielectric. While not having the mechanical and thermal properties of silicon dioxide, air does have the lowest dielectric constant, 1.0. The first step toward air as a dielectric is in the form of air gap structures or air instead of oxide between metal lines. The primary goal of this research is to understand the fundamental processes involved in the decomposition and diffusion of a sacrificial material through an overlying dielectric to form the air gap structures. The longer term goal is to develop a process in which a mechanical robust sacrificial layer remains in place during the mechanically critical steps and is subsequently decomposed to create the air gap. The decomposition mechanisms and rates of several candidate sacrificial materials will be studied by a variety of techniques, including in-situ mass spectrometry, thermogravimetric analysis, and time series Fourier transform infrared spectroscopy. Candidate sacrificial materials include polymethylmethacrylate (PMMA) and polyoxymethylene (POM). Chemical vapor deposition processes for both PMMA and POM films have already been developed in our laboratory. Organosilicon films will be considered as an overlying dielectric material. A continuum model of single and multilevel air gap formation will be created in order to evaluate and eventually select sacrificial and overlying dielectric materials. Air gap structures will be fabricated and their dielectric properties examined.

2:15 PM E5.3
AIR BRIDGE TECHNOLOGY: A COMPARISON OF NOVEL INTERCONNECT MATERIALS AND INTEGRATION SCHEMES FOR BEYOND 45 nm. Kenneth Foster, Mike Mills, Joost Waeterloos, Don Frye, The Dow Chemical Company, Advanced Electronic Materials, Midland, MI.

The continual drive for improved integrated device performance has resulted in a steady shrinkage of the transistor size used in integrated circuits (IC). This increase in device density has a corresponding impact on interconnect technology, where signal lines are becoming longer with ever increasing metal layers (propagation delays) and closer spaced (crosstalk). This has required the IC industry to make some difficult dielectric materials selection choices for the inner layer dielectrics (ILD). But an even more difficult choice awaits the industry in the future. As the industry continually seeks a stepwise reduction of the "effective" (keff) dielectric constant, simple extendibility may lead to achievement of the highest performance possible, air bridge technology. Here, air gaps between interconnect lines can be fabricated resulting in the greatest capacitance reduction possible but not without significant challenges. In comparison to structures prepared with dense dielectrics, air bridge will have the ultimate in reduced mechanical strength and thermal conductivity associated with greater susceptibility to moisture and oxygen permitivity. Not to mention an increased probability of shorts and opens caused by stress induced electromigration. Air bridge technology will need to overcome these and other limitations to be successful. In this paper we will compare and contrast achievable effective dielectric constants, critical integration and reliability concerns and potential choices available for advanced interconnect structures beyond 45 nm, to promote discussion and stimulate new solutions in the industry. The examples presented will include some novel materials from Dow Chemical that have been developed as part of an advanced learning technology probe in air bridge architecture. We will compare and contrast these potential technology offerings with other existing dense and porous ILD integration options and show the choice is not trivial or obvious.

2:30 PM E5.4
USE OF COMPLIANT DIE-SUBSTRATE INTERCONNECTS TO ENABLE LOW k DIELECTRICS. Hollie Reed, Sue Ann Bidstrup Allen, Paul Kohl, Georgia Institute of Technology, School of Chemical Engineering, Atlanta, GA; Muhannad Bakir, Kevin Martin, James Meindl, Georgia Institute of Technology, School of Electrical and Computer Engineering, Atlanta, GA; Lunyu Ma, Qi Zhu, Suresh Sitaraman, Georgia Institute of Technology, The George W. Woodruff School of Mechanical Engineering, Atlanta, GA; Tom Lappin, Richard Emery, Gilroy Vandentop, Intel Corp., Chandler, AZ.

In order to improve the electrical performance of microprocessors, semiconductor manufacturers are seeking to reduce the dielectric constant of the insulator material surrounding the metallic interconnect structures on a silicon chip. The processes employed to produce this low dielectric constant (low k) material also tend to reduce its mechanical strength. In present technologies, the strength of the dielectric is low enough to cause mechanical failure during microprocessor use. The driving force for this failure is the stress imparted on the dielectric due to the thermal expansion mismatch between the silicon die and the composite substrate (often engineered to be expansion-matched to copper) as the system goes through thermal cycles. Therefore, structural improvements that minimize this stress are attractive. Presented here is the assembly process flow and limited mechanical performance data for structures generally referred

to as "compliant interconnects" (CI). These are structures that act to interconnect the die to an electrical substrate while decoupling the deformations of the two. This decoupling is accomplished by making the interconnects out of what is analagous to mechanical springs. Electrical packages using CI are subjected to temperature cycling, showing that they are mechanically reliable through this stress. Further, the ability of CI to reliably connect a die supporting low k material is demonstrated, thus showing that the stress imparted on the die during use can be reduced to an acceptable level by employing CI.

2:45 PM E5.5
DUAL DAMASCENE PROCESS FOR FAT WIRES IN COPPER/FSG TECHNOLOGY. J. Gambino, A. Stamper, H. Trombley, S. Luce, F. Allen, C. Weinstein, B. Reuter, M. Dunbar, V. Samek, IBM Microelectronics, Essex Junction, VT; P. McLaughlin and T. Kane IBM Microelectronics, Hopewell Junction, NY.

Copper interconnects have gained wide acceptance in the microelectronics industry due to improved performance and reliability compared to Al interconnects (1). For CMOS logic, hierarchical wiring can greatly improve performance. Thin wires are used at lower levels to maximize circuit density, while fat wires are used at the upper levels to minimize RC delay (2). Fat wires can be easily patterned using single damascene processing, because of the relatively large dimensions, but the cost is high. To reduce cost, dual damascene patterning is preferred, but the process is more difficult. A via-first process requires a planarizing mid UV anti-reflective coating (ARC) during the trough patterning, to protect the bottom of the vias during trough etch. Many planarizing deep UV ARCs are available for via-first processes (3,4), but mid UV ARCs for via-first processes are less mature. The trench-first process eliminates the need for a planarizing ARC, but the via lithography is much more difficult. Fat wires are typically over 1 um thick, and the associated vias are about 1 um in height. Therefore, the vias must be imaged in a thick resist layer (i.e. thick enough to survive the via etch) that is applied over deep troughs. As a further complication, the thickness of the resist in the troughs depends on the line width (Figure 1); the resist will be thicker over narrow lines than over very wide lines. Hence, characterization of the process window for via lithography is critical for the trench-first process. Trench-first dual damascene processing has been used for fat wires in 0.22 mm and 0.18 mm CMOS technologies in IBM (1, 5). In this report, we describe details of the trench-first dual damascene process for fat wires in 0.18 mm CMOS technology. It is shown that the process window for the patterning of vias in such deep trenches depends on the trench depth and on the line width of the trench. Compared to a single damascene process, the dual damascene process has comparable yield and reliability, with lower via resistance and lower cost. 1. D. Edelstein et al., IEDM Proc., 1997, p. 773. 2. D. Edelstein et al., IBM J. Res. Dev., 39, 383 (1995). 3. C. Tuan et al., SPIE Vol. 4345, 804 (2001). 4. E. Pavelchek et al., SPIE Vol. 4345, 864 (2001). 5. E. Leobandung et al., IEDM Proc., 1999, p. 679.

3:30 PM *E5.6
3D SYSTEM INTEGRATION TECHNOLOGIES. Peter Ramm, Fraunhofer Institute for Reliability and Microintegration, Dept Si Technology and Vertical System Integration, Munich, GERMANY.

Future microelectronic applications require significantly more complex devices: Besides the trend towards higher integration density, there is also a demand for more functionality and increased performance. Due to added device content, chip area will also increase. Performance, multi-functionality and reliability of microelectronic systems will be limited mainly by the wiring between the subsystems (so called "wiring crisis"). This leads to a critical performance bottleneck for future IC generations. 3D System Integration creates a basis to overcome these drawbacks. Furthermore, systems with minimum volume and weight as well as reduced power consumption can be realized for portable applications. The ITRS roadmap predicts an increasing need for systems-on-a-chip (SoC). Conventional fabrication is based on embedded technologies which are cost intensive. 3D integrated systems show reduced chip areas and enable optimized partitioning, both which decrease the fabrication cost of the system. An additional benefit is the enabling of minimal interconnection lengths and the elimination of speed-limiting inter-chip interconnects. Several companies and research institutes all over the world are currently working on the development of 3D system integration. Besides approaches based on fabrication of multiple device layers using recrystallization or epitaxial growth of Si, the large spectrum of technological concepts can be classified in three categories: Stacking of packages, stacking of dies and stacking of wafers. Successful market entry will be determined by the performance improvement achieved and the profitability in relation to the total system cost. Manufacturing technologies that largely rely on wafer fabrication processes show a comparatively favorable cost structure. Wafer yield and chip area issues speak against wafer stacking concepts. In consequence, so called chip-to-wafer technologies mainly based on wafer-level processes utilizing known good dies only, will be of advantage.

4:00 PM E5.7
WAFER THINNING FOR MONOLITHIC 3D INTERCONNECTS. A. Jindal, J.-Q. Lu, Y. Kwon, G. Rajagopalan, J.J. McMahon, A.Y. Zeng, T.S. Cale, R.J. Gutmann, Interconnect Focus Center, Rensselaer Polytechnic Institute, Troy, NY.

Wafer scale three-dimensional (3D) integration has been recognized as an emerging technology to increase the performance and functionality of future integrated circuits (ICs). In our approach, fully processed wafers are aligned and bonded with dielectric glues, followed by top wafer thinning to less than 10 micron. Subsequently, inter-wafer interconnects are formed using a copper damascene patterning process. A baseline wafer bonding with high bonding strength using benzocyclobutene (BCB) and Flare as dielectric glue materials has been established. Subsequent to bonding, precise thinning and leveling of the top wafer is one of the key challenges in this 3D integration process. This work focuses on the thinning of bonded wafer pairs of blanket wafers (bulk silicon, SOI, etch-stop silicon, CTE-matched glass) and processed wafers (e.g.,with interconnect test structures). No visible changes at the bonding interface can be observed after the silicon substrates are thinned to $\sim$30 micron by backgrinding and polishing. Electrical tests on a wafer having multi-level copper interconnect test structures (provided by International SEMATECH) show a very slight change in the via resistance and a change of one order of magnitude in comb-to-comb leakage current after two bonding and thinning processes. Though these results are very promising, thinning failure in some cases occurs at a nominal thickness of $\sim$15 micron, e.g., some areas of the backside silicon are thinned through to the oxide or glue. The grinding/polishing failures have a distinct pattern, attributed to process non-uniformities and/or wafer defects. Failure mechanisms of the mechanical thinning process and its impact on bonding integrity and characteristics of the processed wafers will be discussed.

4:15 PM E5.8
EVALUATION OF DIELECTRIC-GLUE WAFER-BONDING FOR THREE-DIMENSIONAL INTEGRATED CIRCUITS USING FOUR-POINT BENDING TECHNIQUE. Y. Kwon, J.-Q. Lu, R.J. Gutmann, T.S. Cale, Interconnect Focus Center, Rensselaer Polytechnic Institute, Troy, NY.

Wafer scale monolithic three-dimensional (3D) integration is an emerging technology to increase the performance and functionality of future integrated circuits (ICs), with wafer bonding using dielectric polymer glue as a key process step in one promising approach. Several glues, including benzocyclobutene (BCB) and Flare, have been evaluated using optical inspection and a four-point bending technique for measuring the interfacial adhesion energy. The goal is to develop a uniform bonding process that is fully compatible with semiconductor processing protocols, with high bonding strength and low interfacial stress to facilitate 3D integration. A baseline process of 200-mm wafer bonding with good bonding integrity has been established, which is being applied in the fabrication of 3D test structures. High interfacial adhesion energy is obtained, e.g., $\sim$8 J/m^2 using BCB and $\sim$18 J/m^2 using Flare in bonding a silicon wafer to TCE-matched Corning 7740 glass wafers (for optical inspection). Interfacial adhesion energy as high as 34 J/m^2 is measured for a bonding pair of silicon wafers with a 2-micron thermal SiO2 surface using BCB. While large void-free bonding area is achieved using Flare, complete void-free bonding is routinely obtained across 200-mm wafers using BCB. Systematic bonding experiments are conducted by varying (1) glue thickness, (2) glue film preparation (e.g., adhesion promoters and surface treatments), and (3) wafer bonding parameters such as final curing temperature and bonding temperature/pressure as a function of time. Bond uniformity and interfacial adhesion are correlated with wafer surface properties and bonding process parameters.

4:30 PM E5.9
MIM CAPACITORS WITH HfO_2 AND $HfAlO_x$ FOR SILICON RF AND ANALOG APPLICATIONS. Xiongfei Yu, Chunxiang Zhu, Hang Hu, Albert Chin[a], Mingfu Li, B.J. Cho, Dim-Lee Kwong[b], P.D. Foo[c] and M.B. Yu[c], SNDL Dept of ECE, National University of Singapore, SINGAPORE. [a]Visiting Professor, on leave from National Chiao Tung University, Hsinchu, Taiwan, ROC; [b]Dept of ECE, The University of Texas, Austin, TX; [c]Institute of Microelectronics, Singapore Science Park II, SINGAPORE.

The MIM capacitors with HfO_2 and $HfAlO_x$ are investigated for Si RF and analog applications. The results show that both the capacitance density and voltage coefficients of capacitance (VCC_s) increase with decreasing the HfO_2 thickness. A high capacitance density of 13 fF/μm^2 with a low leakage current and a VCC of 607 ppm/V is obtained for 10 nm HfO_2 MIM capacitor, which can meet the

requirement of the ITRS roadmap by 2007 for silicon RF application. On the other hand, it is found that both the capacitance density and voltage coefficients of capacitance (VCC) values of the $HfAlO_x$ MIM capacitors decrease with increasing Al_2O_3 concentration. The results show that $HfAlO_x$ MIM capacitor with an Al_2O_3 mole fraction of 0.14 is optimized. It provides a high capacitance density of 3.5 $fF/\mu m^2$ and a low VCC of ~140 ppm/V^2. Besides, a small frequency dependence, a low leakage current, and a low loss tangent are also obtained. Thus, the $HfAlO_x$ MIM capacitor with an Al_2O_3 mole ratio of 0.14 is very suitable for use in silicon analog applications.

4:45 PM E5.10
Abstract Withdrawn.

SESSION E6: LOW-k MATERIALS AND PROCESS INTERACTIONS
Chairs: Andrew Mckerrow and Nobuhiro Hata
Thursday Morning, April 24, 2003
Golden Gate B2 (Marriott)

8:30 AM *E6.1
SOME ASPECTS OF THE MATERIALS SCIENCE OF LOW-k INTEGRATION. Vincent J. McGahay, IBM Corporation, Semiconductor Research and Development Center, Hopewell Junction, NY.

The microelectronic industry's transition to low dielectric constant insulators in the wiring levels of integrated circuits has proven to be more difficult than expected. Materials properties are an integral part of the problem, as much for yield as for reliability. Unfortunately, many properties which are important for manufacturing robustness tend to degrade as the dielectric constant is lowered. Thus specification of materials properties as a guide to low-K manufacturability could ultimately limit future progress. Application of basic principles of materials science to the integration of low-K dielectrics can give critical insight into the nature of the difficulties. Several examples of problems which benefit from such analysis are given.

9:00 AM E6.2
SEQUENTIAL PROCESS MODELING FOR DETERMINING PROCESS-INDUCED THERMAL STRESS IN ADVANCED Cu/LOW-k INTERCONNECTS. Kwanho Yang, Joost Waeterloos, Jang-Hi Im, Michael Mills, The Dow Chemical Company, Semiconductor Fab Materials, Midland, MI.

The integration of low-k dielectrics in Cu interconnects may pose a significant challenge because their thermal and mechanical properties are quite different from traditional SiO2 dielectric. Failure can occur when significant thermal stresses are introduced especially in high temperature process steps. To understand the development of thermal stress during manufacturing process, sequential process modeling of Cu/low-k interconnects has been developed. Typically, finite element analysis (FEA) has been used to model the thermal stress in Cu/low-k interconnects. Most modeling studies have been performed previously with certain assumptions - 1) no initial residual stress exists in any parts of structure or 2) the entire structure is under zero stress at a so-called stress-free temperature. The first assumption completely neglects the process-induced stress in Cu/low-k interconnects while being manufactured. The second assumption considers only one stress-free temperature, at which all constituent materials are simultaneously stress-free. But there is no such single stress-free temperature, for multiple process steps involved render different level of stress at different parts of the structure. To overcome these limitations of traditional FEA modeling approach, a sequential process modeling technique has been developed to mimic actual process steps. Thus, all the constituent materials are sequentially added in the analysis and numerical simulations are performed in each of these steps. The preliminary results support the previous argument that none of the afore-mentioned modeling assumptions are quite accurate. Designing Cu/low-k interconnects is a difficult process because there are many parameters to consider. Therefore, the results of parametric FEA study will be presented for the purpose. The parameters investigated in this study includes 1) various low-k dielectric materials, 2) aspect ratio of via and trench and 3) via spacing.

9:15 AM E6.3
STRESS STABILITY OF PECVD SILICON NITRIDE FILMS DURING DEVICE FABRICATION. Michael P. Hughey, Robert F. Cook, Department of Chemical Engineering and Materials Science, University of Minnesota, Minneapolis, MN.

The mechanical properties and integration characteristics of films formed by plasma-enhanced chemical vapor deposition (PECVD) are playing an increasingly significant role in advanced microelectronic interconnection structures using low-*k* dielectrics: PECVD materials act as the supporting structural elements and diffusion barriers during device operation and as etch and CMP-stops during fabrication. In this work, we study the composition, structure, and thermomechanical behavior of PECVD silicon nitride (SiN_x:H) films during thermal cycling, which simulates temperature excursions experienced by the films during subsequent deposition steps. It is well known that PECVD SiN_x:H is not stoichiometric and has large amounts of incorporated hydrogen that is known to evolve from the solid film on annealing above the deposition temperature, correlating with a change in film structure and the development of decreasing compressive stress. The film compositional and structural evolution are investigated here before and after thermal cycling by ion beam analysis and infrared spectroscopy, while gas-phase species evolved from the film during thermal cycling are monitored *in situ* with a quadrupole mass spectrometer. The thermomechanical behavior is studied by measuring stress development on thermal cycling. Intriguing results include a change in stress of up to 2 GPa in some films, and observations of several films deposited in compression that were driven into significant values of tension, indicating that the stress alteration is not simply a relaxation process, but a result of structural modifications. The implications of this lack of film stability on device integration and performance are discussed.

9:30 AM E6.4
ACCELERATED OXIDATION OF HYDROGEN SILSESQUIOXANE THIN FILMS FACILITED BY AN ORGANOSILICONE RESIN ADDITIVE. Brian Harkness, Ron Boisvert, Qian Deng, Ben Zhong, Dow Corning Corporation, Midland, MI; Jianing Sun, David Gidley, Randall Physics Lab, University of Michigan, Ann Arbor, MI.

FOx® Flowable Oxide is a spin-coatable hydrogen silsesquioxane based coating commercially available from Dow Corning Corporation. The commercial success of FOx® as a dielectric in semiconductor fabrication can be attributed to its unique material properties and process simplicity. When coated and cured under standard thermal conditions FOx® films provide a low dielectric constant of 2.9 and a modulus in the range of 5-6 GPa. It has recently been discovered that the addition of small amounts of specific organosilicone resins to FOx® films results in a significantly higher level of film oxidation during standard processing. The effect has been traced to an unexpectedly high level of oxidation that occurs during a 350°C/1 minute hot-plate bake unit process. It is hypothesized that during thermal treatment the organic additive increases the diffusivity of oxygen into the modified films compared to standard FOx® films. The higher level of conversion to silicon dioxide results in several positive post cure attributes that include a lower silyl-hydride level, a significantly higher modulus, improved adhesion, reduced outgassing and higher density. Analyses of the films have indicated that a majority of the organic component of the resin additive is removed through oxidation and volatilization during thermal processing. A series of films have been prepared with varying levels of the organosilicone additive, and the effects on the post cure material properties and film composition examined. The results show a limiting modulus value of 12 to 13 MPa, with a diminishing modulus observed for higher additive levels. An explanation for this behaviour is increasing porosity in films derived from higher levels of additive. PALS analysis, density determinations and film shrinkage data support this conclusion.

9:45 AM E6.5
STRUCTURE AND PROPERTIES OF POLYSILSESQUIOXANES AND COPOLYMERS FOR ULTRA-LOW DIELECTRIC FILMS. Do Y. Yoon, Jin-Kyu Lee, Hie-Joon Kim, Kookheon Char, Hyun Wook Ro, Seoul National Univ., KOREA; Hee-Woo Rhee, Sogang Univ., KOREA.

Polysislesquioxanes (PSSQs) with the empirical formula (RSiO3/2) have become very important for information technology as low-dielectric insulators in advanced microelectronic devices, but the detailed structure-property relationships were completely lacking. We have investigated the microstructures and functional properties of PSSQs with varying alkyl substituents and also PSSQ copolymers. As a result, significant advances have been made in the scientific understanding of PSSQ structures and improving the key properties such as the crack resistance, mechanical modulus and hardness, and incorporation of nanometer-sized porosities for ultra-low dielectric constants.

10:30 AM *E6.6
ELECTRICAL AND MECHANICAL RELIABILITY OF HIGH PERFORMANCE INTERCONNECTS INCORPORATING ORGANOSILICATE GLASS (OSG) AND SILICON CARBIDE THIN FILMS. Ting Tsui and Andrew J. McKerrow, Silicon Technology Development, Texas Instruments, Dallas, TX; Youbo Lin and J.J. Vlassak, Division of Engineering and Applied Sciences, Harvard University, Cambridge, MA.

With increasing device performance requirements at the 90 nm node it has become necessary to fabricate Cu damascene interconnects using low dielectric constant materials as the intermetal/interlayer dielectric (IMD/ILD) and as the dielectric barrier. The organosilicate glasses (OSGs) are an example of a class of materials that are used as the ILD/IMD, while Pe-CVD silicon carbide (SiC) is an example of a possible dielectric barrier material. The initial materials evaluation process for selecting suitable low-k dielectrics typically uses blanket film electrical and mechanical tests to distinguish between candidate materials. Specific examples include using metal-insulator-metal capacitors fabricate on blanket films to measure dielectric constant, leakage current, and breakdown as well as four-point bend tests on blanket film stacks for evaluating interfacial adhesion. Although these tests have utility in screening materials, it is our experience that they may provide misleading or insufficient information to predict electrical and mechanical reliability when these materials are integrated in a high performance interconnect. In this presentation we will report time dependent dielectric break down (TDDB) lifetime and temperature-dependent electrical field break down data for dual level copper interconnects fabricated with an Organosilicate (OSG) low-k dielectric and various Pe-CVD silicon carbide (SiC) dielectric barriers. These tests reveal differences among the Pe-CVD SiC films that are not apparent from blanket film tests and suggest that moisture absorption and permeability effects are a critical concern when integrating Pe-CVD SiC as a dielectric barrier with low-k materials. Adhesion measurements for dielectric barriers deposited on OSG and tested under different aqueous and reactive ambients will also be presented. These tests demonstrate that common practice of performing adhesion testing in the ambient atmosphere may not be adequate.

11:00 AM E6.7
PECVD OF ORGANOSILICON PRECURSORS AND WATER: ENHANCING MECHANICAL PROPERTIES. Karen K. Gleason and Daniel D. Burkey, Massachusetts Institute of Technology, Department of Chemical Engineering, Cambridge, MA.

Introduction of porosity into thin films to reduce the dielectric constant makes understanding the relationship between film structure and the mechanical properties important, especially when considering inclusion into production schemes with mechanically rigorous integration steps, such as chemical-mechanical polishing (CMP). While there has been considerable literature on spin-on fabrication of porous thin films using the OSG matrix/porogen (pore-forming species) approach, an all-CVD approach has remained elusive. Using a CVD process versus spin-on to fabricate a porous thin film has numerous advantages, including seamless compatibility with existing toolsets, lower environmental impact, and less solvent/material waste. However, the matrix/porogen model has proved difficult to extend to the CVD approach. Experience in our lab points to the often-incompatible deposition requirements of the matrix and porogen species as a primary stumbling block. This work details the pulsed-plasma chemical vapor deposition of an OSG precursor and water to produce thin films with significant OH content. Subsequent annealing of the films results in condensation of proximal Si-OH groups, generating an Si-O-Si network and strengthening the film. FTIR analysis shows increasing OH content with increasing plasma duty cycle. Nanoindentation results confirm increasing hardness with duty cycle and post treatment, with the film deposited using 10/40 ms-on/ms-off pulse plasma excitation having a hardness value of 0.527 GPa after annealing. These results are explained within the context of the Continuous Random Network theory and percolation of rigidity arguments. Thermal stability was excellent. In the best case, thickness retention was 99.25% after a two hour anneal at 400°C under nitrogen. Dielectric constants for the annealed films ranged between 2.55 and 2.9. The moderate power involved (200 W peak) is amenable to inclusion of a porogen species, opening the possibility of using this methodology to generate an all-CVD porous thin film with adequate mechanical properties.

11:15 AM E6.8
CHEMICAL VAPOR DEPOSITION OF ORGANOSILICON COMPOSITE MATERIALS FOR POROUS LOW-k DIELECTRICS. April Ross, Karen K. Gleason, Massachusetts Institute of Technology, Dept of Chemical Engineering, Cambridge, MA.

The demand for high-speed devices in today's electronics is surging and several changes are being investigated for improvement of current devices. At the forefront of these options is reducing the capacitance, C, of the inter-level dielectric material. Two different pathways are being explored to lower the k-value relative to the silicon dioxide (k 4) commonly used today. Both incorporating atoms and bonds that have a lower polarizability, such as alkyl groups, and lowering the density of the material, sterically or with the integration of air, can be employed to lower the dielectric constant. Creating porous films with a siloxane matrix is an avenue for introducing void space and thereby decreasing density and lowering the dielectric constant. Incorporating polystyrene beads into an OSG film as a sacrificial porogen offers many advantages. First, the deposition of the OSG is decoupled from that of the porogen allowing for any choice of OSG precursor and deposition conditions. Second, the pore size and pore size distribution are controlled. Earlier work examines OSG deposition over several stacked layers of beads dried onto a wafer. Difficulties incurred as the films often collapsed after the beads were removed via annealing. This is caused by both the high degree of porosity inherent in stacking the beads as well as lack of OSG film hardness. Flowing the beads in simultaneously with the OSG precursor as it is depositing would allow for a fewer beads to be incorporated throughout the film. Pulsed plasma-enhanced CVD was used to explore diethylsilane as the OSG matrix of the film. It was shown that properties of the film, such as index of refraction, were tuned by varying the pulsing conditions. In addition, nanoindentation results confirm increasing hardness with both increased oxygen flowrate and increased power, reaching a peak hardness of over 1.6 GPa after annealing.

11:30 AM E6.9
EXPANDING THERMAL PLASMA FOR LOW-k DIELECTRICS DEPOSITION. M. Creatore, W.M.M. Kessels, M.C.M. van de Sanden, Eindhoven University of Technology, Dept of Applied Physics, Eindhoven, THE NETHERLANDS.

As the need for low-k dielectrics in the ULSI technology becomes urgent, the research focuses on the deposition of novel materials with appropriate electrical properties and on the challenges concerning their integration with later processing steps. The spin-on deposition has been the first to be adopted and claimed to be extendible to future generation of low-k materials (k<2). On the other hand, chemical vapour deposition is nowadays acknowledged for the possibility of using existing toolsets and for the simpler process integration due to the SiO_2-like structure, when the choice for a low-k dielectric falls on the siloxane (OSG) class. Here we introduce the expanding thermal plasma (ETP) as a novel remote technique for the deposition of low-k OSG materials from Ar/HMDSO/(O_2) mixtures at very high growth rate (up to 60-70 nm/s). The plasma (a dc cascaded arc, 0.2-0.6 bar) supersonically expands into the deposition chamber (0.1-0.3 mbar) through a nozzle; HMDSO is injected downstream. HMDSO may not appear at first sight a suitable precursor because of the high methyl group concentration, which could lower far beyond the layer density and mechanical stability. However, the ETP allows selecting different fragmentation paths for HMDSO, which eventually can be turned to the progressive cleavage of Si-C bonds: the organic functionalities in the film are responsible for the decrease of the ionic component of the dielectric constant. The plasma characteristics can be tuned independently from the gas chemistry (gas mixture, flow rate, pressure) in the deposition chamber. Film characterization has been obtained by means of IR absorption spectroscopy (which also provides the calculation of the ionic contribution to the dielectric constant) and XPS. UV-VIS spectroscopic ellipsometry has provided the electronic contribution to the dielectric constant from the refractive index values. These results have been correlated with capacitance (1 MHz) and nano-indentation (elastic modulus/hardness) measurements.

11:45 AM E6.10
SUPERCRITICAL CARBON DIOXIDE-BASED FLUIDS USED AS A RECOVERY TOOL FOR LOW-k MATERIALS. R.A. Orozco-Teran and Zhengping Zhang, Univ of North Texas, Dept of Materials Science, Denton, TX; B.P. Gorman and D.W. Mueller, Univ of North Texas, Dept of Physics, Denton, TX; R.F. Reidy, Univ of North Texas, Dept of Materials Science, Denton, TX.

Conventional ash strippers can easily damage most ultra low-k materials, causing increased dielectric constants and decreased film thickness. This effect is more prominent in carbon-containing porous low-k materials such as methyl silsesquioxane (MSQ). Ashed MSQ exhibits increased water adsorption and dielectric constants due to removal of methyl groups and structural damage caused by interaction with plasma species. In recent work, we have developed methods capable of drying and repairing the post ash (oxidizing and reducing) damage using supercritical fluids (SCF) in a single supercritical process-lowering dielectric constant and replacing carbon species. SCF, in particular carbon dioxide (CO_2), has attracted considerable attention due its low cost, easily accessible critical point, and environmentally benign nature. This paper discusses the effect of ash damage on MSQ films after recovery using supercritical carbon dioxide in combination with hexamethyldisilazane (HMDS) as a modifying agent. Fourier transform infrared spectroscopy (FTIR) was used to verify the presence of specific bonding structures in the low-k film, such as Si-O and Si-CH_3. Film hydrophobicity was measured by the sessile-drop goniometric contact angle technique. Ellipsometry was conducted to determine changes in porosity, thickness, and refractive index of the low-k material. Structural changes in the MSQ samples before and after recovery were studied by Scanning electron microscopy (SEM).

SESSION E7: LOW-k THIN FILMS
Chairs: Takamaro Kikkawa and Raymond N. Vrtis
Thursday Afternoon, April 24, 2003
Golden Gate B2 (Marriott)

1:30 PM *E7.1
STRUCTURE AND PROPERTY CONTROL OF a-C:F FILM FOR ULSI LOW-k DIELECTRCS. Yukihiro Shimogaki, Univ of Tokyo, Dept of Materials Engineering, Tokyo, JAPAN.

The ever growing device integration now requires low dielectric constant inter-metal and inter-level dielectrics to reduce RC delay in ULSI multi level metallization. Fluorinated amorphous carbon film (a-C:F) is one of the candidates for this purpose. Plasma enhanced CVD can be used to deposit this material using C_2F_4 and/or C_4F_8 as the source precursors. The CV measurement, FT-IR, and spectroscopic ellipsometry were employed to characterize each dielectric components, i.e. orientational polarization, ionic polarization, and electronic polarization. Kinetic study using AMS (Appearance Mass Spectrometry) was also performed to analyze the major reaction path ways to deposit a-C:F film. The basic strategy to deposit a-C:F film that has lower dielectric constant and good thermal stability will be discussed.

2:00 PM E7.2
SPIN-ON SILICA LOW-k DIELECTRIC FILMS FROM ZEOLITE NANOPARTICLE SUSPENSION. Zijian Li, Shuang Li, Yushan Yan, University of California-Riverside, Department of Chemical and Environmental Engineering, Riverside, CA.

To satisfy the constant demands for more and more powerful micro-processors, the feature size of the logic devices continues to shrink. The traditional Al/SiO_2 interconnect combination can no longer meet the needs of this trend for miniaturization. Although copper has been introduced to substitute Al, the most suitable replacement for SiO_2 has not emerged yet. Here we report a new low-k material and its deposition process – zeolite low-k films by spin coating from zeolite nanoparticle suspension. The suspension was synthesized hydrothermally with a synthesis solution containing $TPAOH/TEOS/H_2O/EtOH$. The as-synthesized solution is a mixture of amorphous silica and crystalline zeolite particles. Surface roughness and mechanical properties are correlated to the ratio of amorphous and crystalline material in the solution. A two-stage synthesis route was employed to synthesize colloidal solution with high yield nanoparticle. By dynamic light scattering, the nano particles were found to be around 50 nm with a narrow size distribution. Uniform zeolitic thin films with very low surface roughness were obtained by spin on coating. The so-obtained films have a very low k value (1.8-2.0), which reaches the range of ultra low k. They also show excellent mechanical strength (modulus of elasticity = 16-18 Gpa)[1-3]. We believe that this approach to prepare zeolite films from nano suspension is a significant step forward toward the commercial application of Cu/low-k technology in semiconductor industry. References: [1] Wang Z.; Mitra A.; Wang H.; Huang L.; Yan Y. 2001. Pure silica zeolite films as low-k dielectrics by spin-on of nanoparticle suspension. Adv. Mater. 13:1463-1466 [2] Wang Z.; Wang H.; Mitra A.; Huang L.; Yan Y. 2001. Pure-silica zeolite low-k dielectric thin films, Adv. Mater. 13:746-749. [3] Wang Z.; Wang H.; Mitra A.; Huang H.; Yan Y. 2001. Pure silica zeolite low-k dielectrics by spin-on process. Studies in Surface Science and Catalysis 135:20-P-11.

2:15 PM E7.3
ORGANOFLUOROSILICATE GLASS (OFSG): A DENSE LOW-k DIELECTRIC WITH SUPERIOR MATERIALS PROPERTIES FOR THE 90nm INTERCONNECT NODE. Aaron S. Lukas, Mark L. O'Neill, Raymond N. Vrtis, Jean L. Vincent, Mark D. Bitner, Eugene J. Karwacki, Electronics Technology, Air Products and Chemicals, Inc., Allentown, PA; Y.L. Cheng[a,b], Y.L.Wang[a,c], M.S. Feng[b]; [a]Taiwan Semiconductor Manufacturing Co., Ltd., Hsinchu, Taiwan, R.O.C.; [b]Department of Materials Science and Engineering, Natl. Chiao-Tung University, Hsin-Chu, Taiwan, R.O.C.; [c]Department of Electrical Engineering, National Chi-Nan University, Nan-Tou, Taiwan, R.O.C.

A primary challenge in fabricating integrated circuits with critical geometries 130 nm and smaller is the development of dielectric insulators with low dielectric constants that have sufficient mechanical strength, resistance to thermal oxidation, and adhesion for integration. Historically, the microelectronics industry has employed undoped-silicate glass (USG) deposited by chemical vapor deposition (CVD) with a dielectric constant (κ) of approximately 4.0 as the material of choice. Currently, fluorosilicate glass (FSG; κ = 3.6) is used in advanced devices because the introduction of Si-F bonds lowers the polarizability and density of the silicate to reduce the dielectric constant by about 10%.[1] Further reduction in the dielectric constant beyond FSG has focused extensively on organosilicate glass (OSG).[2,3] It has been shown that organic functional groups can dramatically decrease the dielectric constant by increasing the free volume of films. Yet their decreased density often diminishes the mechanical strength and makes integration challenging. One of the primary challenges for low-κ OSG materials is improving their mechanical hardness (H) while maintaining a low dielectric constant. We propose as an improvement the incorporation of small amounts of inorganic fluorine as Si-F bonds.[4] Organofluorosilicate glass (OFSG) films with the composition Si:O:C:H:F were deposited via plasma-enhanced CVD from mixtures of trimethylsilane (3MS), silicontetrafluoride, and oxygen (O_2). OFSG films have significantly enhanced mechanical strength, resistance to thermal oxidation, and adhesion compared with OSG films deposited from 3MS and O_2 alone. This is attributed to the presence of inorganic fluorine, which densifies the material while maintaining a low dielectric constant. We propose that the increased density for OFSG is balanced by the decreased polarizability of the fluorine, which retains the low-k dielectric properties while significantly increasing the mechanical strength of the material. The presentation will focus on OFSG materials properties as well as work to integrate the material now underway at TSMC. References: 1. Laxman, R., Low-k Dielectrics: CVD fluorinated silicon oxides. Semiconductor Int'l, May 1995, p.71-74. 2. MacWilliams, K., et al., Low k material optimization. IEEE Proc. 2001, p.203-205. 3. Grill, A. and V. Patel, Ultralow-k dielectrics by plasma-enhanced chemical vapor deposition. Appl. Phys. Lett., 2001, 79(6), p.803-805. 4. Lubguban, J., et al., Thermal stability and breakdown strength of carbon-doped SiO2:F films prepared by plasma-enhanced chemical vapor deposition method. J. Appl. Phys., 2000, 87(8), p.3715-3722.

2:30 PM E7.4
PLASMA ENHANCED CHEMICAL VAPOR DEPOSITION OF POROUS ORGANOSILICATE GLASS ILD FILMS WITH K LESS THAN 2.4. Raymond N. Vrtis, Mark L. O'Neill, Jean L. Vincent, Aaron S. Lukas, Brian K. Peterson, Mark D. Bitner, Eugene J. Karwacki, Air Products and Chemicals Inc., Allentown, PA.

Current leading edge candidates for low-k interlayer dielectrics are PECVD organosilicate glasses (OSG's) with k down to 2.7. Driving the dielectric constants of next generation ILDs below 2.4 will most likely require a shift towards porous materials. We have been studying methods for introducing pores into a OSG film in a PECVD process. Modeling studies showed that the mechanical properties of OSG films decreased more rapidly than dielectric constant as porosity is added. This result indicated that it was necessary to start with an OSG film that not only exhibited low dielectric constant but also high hardness. We surveyed a wide variety of materials to understand the relationship between precursor structure and film properties. From these studies we determined that diethoxymethylsilane (DEMS) provided the optimal balance between k and mechanical properties. Here we report the successful co-deposition of diethoxymethylsilane (DEMS) with several different plasma polymerizable organic polymer precursors (aka. porogen). Thermal post-treatment of the films under inert atmosphere removes the porogen, providing a porous OSG film. By varying the porogen to DEMS ratio in the deposition gases we are able to deposit films with post anneal dielectric constants down to 2.2 and a nanoindentation hardness of ~0.35 GPa. Compositional analysis by XPS indicates that the carbon levels in the as-deposited film drops upon thermal anneal, resulting in a porous film with a composition very similar that of pure DEMS OSG films deposited at identical process conditions. This indicates that essentially all of the porogen is removed from the film upon anneal. Positron Annihilation Lifetime Spectroscopy (PALS) points towards a closed-cell structure, while kinetic analysis of the anneal process indicates that the removal of porogen is not a diffusion limited event.

2:45 PM E7.5
DEVELOPMENT OF POROUS SiLK™ SEMICONDUCTOR DIELECTRIC RESIN FOR THE 65 NM AND 45 NM NODES. R.J. Strittmatter, J.L. Hahnfeld, H.C. Silvis, T.M. Stokich, J.D. Perry, K.B. Ouellette, Q.J. Niu, J.P. Godschalx, T.H. Kalantar, E. Mubarekyan, R.E. Hefner, Jr., J.W. Lyons, J.M. Dominowski, and G.R. Buske, The Dow Chemical Company, Midland, MI.

In order to meet the speed and performance challenges of advanced microelectronic devices, we have developed porous SiLK semiconductor dielectric resin. Porous SiLK dielectric resin is an ultra-low-k ILD designed to meet the needs of the 65 nm technology node and beyond. The porous SiLK film is prepared on-wafer by thermally removing a sacrificial porogen from the porous SiLK dielectric matrix, resulting in a film with spherical, uniformly distributed, closed pores. Technical challenges in the development of porous SiLK dielectric resin include a small average pore size with a tight pore size distribution, while maintaining the desired morphological attributes of closed and spherical pores. In addition, the material must have uniform porosity and the absence of large pores in order to meet the mechanical and electrical property requirements necessary for successful integration. We will discuss the achievement of the desired small pore size and pore size distribution

for the 65 nm node for porous SiLK dielectric film. We have designed this material to maintain the mechanical and electrical properties that will allow for successful integration of porous SiLK dielectric resin using conventional, existing processing technology, and we will show results demonstrating successful process module compatibility. Porous SiLK resin is extendable to the 45 nm node, as well as to lower dielectric constants, and we will discuss the latest developments with regard to pore size reduction and k value reduction. * SiLK is a trademark of The Dow Chemical Company.

3:30 PM *E7.6
FABRICATION OF MESOPOROUS ULTRA-LOW DIELECTRIC CONSTANT FILMS BY THREE DIMENSIONAL REPLICATION OF STRUCTURED ORGANIC TEMPLATES IN SUPERCRITICAL FLUIDS. Rajaram Pai and James J. Watkins, Univ. of Massachusetts, Dept. of Chemical Engineering, Amherst, MA.

The optimization of electrical and mechanical properties of mesoporous silicate and organosilicate thin films will require strict control over porosity, pore structure, matrix composition and ultimately, as device generation recede though 70 nm, the ability to control long range order and patterning at the device level. Current approaches to mesoporous silica using sol-gel chemistry offer good control over local pore structure but limited possibilities for extending this control over multiple length scales in three dimensions. Moreover, casting from alcohol/water solutions limits the degree of network condensation and consequently poses process challenges, including the need for aging periods and concerns over crack formation. Here, we discuss a new approach to mesoporous silicates that involves the infusion and selective condensation of metal oxide precursors within one phase domain of highly ordered, preformed block copolymer templates using supercritical carbon dioxide as the reaction medium. The template is then removed to produce the mesoporous oxide. To date we have replicated ordered spherical and cylindrical morphologies to yield silica, organosilicate and mixed silica/organosilicate mesostructures in films over 1 micron thick while maintaining all the structural details of the sacrificial copolymer template. After post-processing to cap residual silanol functionality, these films exhibit dielectric constants as low as 1.8. One advantage of the process is the elimination of excess alcohol from the reaction media, which provides a pathway for rapid and high degrees of network condensation. Moreover, separation of the template formation and infusion steps is enabling. For example, structure on both the local and device levels can be achieved in three dimensions wholly in the polymer template using established techniques prior to infusion of the inorganic phase. This approach also offers flexibility with regard to framework chemistry and the nature of the copolymer template, which can now be chosen independently without regard to compatibility in solution or concerns about disrupting the coordinated self-assembly process. The implications of this process for the design and fabrication of ultra-low dielectric constant thin films are discussed.

4:00 PM E7.7
NEW NANO-POROUS COMPOSITE FILMS OF SILSESQUIOXANE COPOLYMER AND SILICALITE-1 FOR LOW DIELECTRIC APPLICATIONS. Ruo Qing Su, Gabriela Zadrozna, Thomas E. Mueller, and Johannes A. Lercher, Technische Universiaet Muenchen, Lehrstuhl fuer Technische Chemie II, Garching, GERMANY.

Low - k interlayer dielectric materials have been identified by the microelectronics industry as one of the critical factors in the development of submicron technology for integrated circuits. Present standard in low k materials is SiO_2 with k = 4. In order to reduce the k value relative to that of SiO_2, it is necessary either to incorporate atoms and chemical bonds that have a lower polarizability, or else to lower the atom density in the material, or both. In this study, a new type of organic/inorganic hybrid copolymer with a low dielectric constant (k = 2.1 - 2.7) was prepared based on silsesquioxanes (RSiO1.5)8.[1] Two routes of polymerization were employed to connect the silsesquioxane cubes in a highly defined manner: 1) platinum catalysed hydrosilylation, 2) hydrolytic condensation. The copolymers form a well-defined three dimensional network where each Si atom of one cage is connected through organic linkers (containing alkyl-chains) to another silsesquioxane cage. It is well known, that single C-C bonds have one of the lowest electronic polarizabilities. Concurrently, the material density is reduced by the open structure of the polymers. It is well known that air gaps have the lowest k value at 1, however, they suffer from low breakdown voltage, low mechanical strength and low thermal conductivity. Therefore, further reduction in dielectric constant can only be achieved by introducing porosity into the dense matrix. The k value of the composite is then determined by the mixture rule.[2] Our strategy is to introduce zeolite nanoparticles with a defined pore system into the copolymer silsesquioxane film in order to increase its effective porosity (10 - 30%). The first results show, that the nano-porous composite films have a k value in the range of 2.1 - 1.7 which is much lower than of the corresponding copolymer silsesquioxane film (k = 2.4).

4:15 PM E7.8
A NOVEL POROUS SILICA FILM FOR COPPER/LOW-k MULTILEVEL INTERCONNECTS. Iwao Sugiura, Katsumi Suzuki, Yoshihiro Nakata, Ei Yano, Fujitsu Laboratories Ltd, Inorganic Materials & Polymers Laboratory, Kanagawa, JAPAN; Masanobu Ikeda, Junya Nakahira, Yoshihisa Iba, Shun-ichi Fukuyama, Kazuto Ikeda, Noriyoshi Shimizu, Motoshu Miyajima and Takayuki Ohba, Fujitsu Limited, Advanced LSI Development Division, Tokyo, JAPAN; Akira Nakashima, Miki Egami and Michio Komatsu, Catalysts & Chemicals Ind. Co., Ltd, Fukuoka, JAPAN.

Miniaturization of CMOS interconnection systems causes signal propagation delay due to the capacitance increase between conductors. To solve this problem, the effective dielectric constant of the system must be reduced and porous silica film of dielectric constant below 2.3 is expected to be a promising candidate material for 65 nm node devices. Several types of low-k porous silica films have been proposed. In these materials, the pore was generally formed by the elimination of the components added as a template. However, for the template type materials, it is difficult to control a size and distribution of the pores because of large pore formation by the fusion of smaller pores. A novel coating-type porous silica NCS (Nano-Clustering Silica) without templates was developed. The origin of the pore in the NCS film is due to micropores arranged in NCS precursors, the pore has a extremely small size and a small distribution. We confirmed that the pore size of NCS was less than 2nm, and a low dielectric constant less than 2.3 was achieved. We also obtained high young's modulus at about 10GPa, it was larger than that of template type and CVD-type Low-k materials reported previously. The pores in the NCS film were dispersed uniformly indicating high break down voltage. The Leakage current density was 1E-11 [A/cm2] at an electric field 0.1[MV/cm]. The optimized processing condition such as etching enabled its appliation in Cu Multilevel interconnects.

4:30 PM E7.9
CREATING NANOPOROSITY BY SELECTIVE EXTRACTION OF POROGENS USING SUPERCRITICAL CARBON DIOXIDE. T. Rajagopalan, B. Lahlouh, J.A. Lubguban, , N. Biswas, C.T. Camagong, and S. Gangopadhyay, Department of Physics; J. Sun, D. Huang and S.L. Simon, Department of Chemical Engineering, Texas Tech University, Lubbock, TX; H.C. Kim, W. Volksen and R.D. Miller, IBM Almaden Research Center, San Jose, CA.

This work presents a novel approach using supercritical carbon dioxide (SCCO2) to selectively extract poly(propylene glycol) (PPG) porogen from a poly(methylsilsesquioxane) (PMSSQ) matrix resulting in the formation of nanopores. Thin films of nanoporous PMSSQ were prepared by spin-casting a solution containing appropriate quantities of PPG porogen and PMSSQ dissolved in PM acetate. The as-spun films were thermally cured at temperatures well below the thermal degradation temperature of the organic polymer to form a cross-linked organic/inorganic polymer hybrid. By selectively removing the CO_2 soluble PPG porogen, open and closed pore structures are possible depending upon the porogen load and its distribution in the matrix before extraction. In the present work, two different loadings of PPG namely 25 wt.% and 55 wt.% were used. Transmission electron microscopy (TEM) and small angle X-ray scattering (SAXS) measurements confirm the formation of nanopores in the films after SCCO2 treatment in both compositions. In films with 55% loading of PPG, the structure is that of interconnected pores distributed non-uniformly, whereas films with 25% porogen loading show more uniformly distributed small pores. Quantitative analysis of SAXS profiles further reveals that the average pore size of 3-4 nm with log-normal distribution was observed for the 25 wt.% sample. Bigger pore size with much broader size distribution was observed for 55 wt.% sample. Fourier transform infrared spectroscopy (FTIR) and refractive index measurements further corroborate the successful extraction of the porogens at relatively low temperatures ($\leq 200°C$). For the pure PMSSQ film, the k value is 3.1, whereas it is 1.46 and 2.27 for the open and closed pore compositions respectively after extraction. Thus the reduction in the k-value is attributed to the formation of nanopores.

4:45 PM E7.10
NANOPOROUS SILICA FILMS DERIVED FROM STRUCTURALLY CONTROLLABLE POLY(SILSESQUIOXANES) OLIGOMERS BY TEMPLATING. Wen-Chang Chen and Wei-Chi Liu, Department of Chemical Engineering, National Taiwan University, Taipei, TAIWAN.

In this study, nanoporous silica films were prepared from the poly(hedral oligomeric silsesquioxane)(POSS) and a templating agent. The molecular structures of the POSS could be controlled by the reaction conditions, including the cage/network ratio, molecular weight (MW), and the OH end group content. These molecular parameters played an important role on controlling the pore size distribution and their dielectric constants of the prepared silica films.

The templaing agent was triphenyl silanol (TPS), polystyrene-block-poly(acrylic acid), or poly(tetramethylene oxide). The experimental results of TEM, refractive index, and dielectric constant supported the formation of the nano-size pores in the prepared silica films. The lower MW or higher OH content of the POSS oligomers resulted in a higher porosity and more uniform pore size distribution of the prepared silica films. The dielectric constant of the prepared nanoporous thin films from hydrogen silsesquioxane (HSQ)/TPS was reduced form 2.96 (porosity: 15%) to 1.85 (porosity: 59%) by increasing the added TPS. The type and amount of the templating agent also significantly affected the pore size distribution and dielectric constant. The surface roughness of the prepared nanoporous silica film in comparison with the film thickness was less than 0.5%. The materials could be very important for low dielectric constant applications.

SESSION E8: POSTER SESSION
LOW-k MATERIALS
Chairs: Andrew Mckerrow and Jihperng (Jim) Leu
Thursday Evening, April 24, 2003
8:00 PM
Salon 1-7 (Marriott)

E8.1
A COMBINATORIAL WORKFLOW FOR THE RAPID DISCOVERY AND OPTIMIZATION OF LOW DIELECTRIC CONSTANT MATERIALS. Konstantinos Chondroudis, Keith Cendak, Eric Ramberg, Martin Devenney, Symyx Technologies, Inc., Santa Clara, CA.

Combinatorial synthesis and screening of extraordinarily large numbers of different organic compounds has been widely applied in the pharmaceutical industry for drug discovery. At Symyx, combinatorial high throughput synthesis and screening techniques have been implemented to create integrated workflows that enable scientists to discover and optimize materials across a broad range of applications at an accelerated rate compared to traditional techniques. There is an urgent need in the semiconductor industry for the identification and development of next generation low dielectric constant (low-k) films and several groups are exploring the use of spin-on low-k solutions. Symyx has constructed and utilized a combinatorial workflow for the rapid discovery and optimization of spin-on, porous low-k films. In this talk we will discuss how combinatorial techniques were used to: (a) design the desired parameter space (e.g. composition) of a multi-component solution system, (b) formulate the designed solutions in a microliter scale, (c) rapidly dispense and fabricate low-k film libraries from these solutions, (d) efficiently screen the films for optical properties, dielectric constant and mechanical properties and (e) capture the data and use the information to discover dielectric films with low dielectric constant and high modulus.
This workflow allowed us in approximately 8 months to study more than 12,000 compositions, identifying materials with superior properties. Several compositions were subsequently scaled-up (i.e. prepared in a conventional spin-coated format and scale) confirming the properties as identified by the library data.

E8.2
PATTERNING OF SELF-ASSEMBLY SURFACTANT TEMPLATED NANOPOROUS SILICA THIN FILM AS AN ULTRA LOW-k DIELECTRIC. F.M. Pan, A.T. Cho, B.W. Wu, T.G. Tsai, National Nano Device Laboratories, Hsinchu, TAIWAN; K.J. Chao, Dept of Chemistry, National Tsinghau Univ, Hsinchu, TAIWAN; J.Y. Chen and L. Chang, Dept of Materials Science and Engineering, National Chiaotung Univ, Hsinchu, TAIWAN.

Nanoporous dielectric materials are widely recognized as a potential candidate for interlayer dielectrics (ILD) for sub-100 nm integrated circuit (IC) technologies because of their ultra-low dielectric constants. However, compared with conventional silica dielectrics, porous materials are mechanically weaker and liable to water adsorption, and hence porous dielectrics inevitably face many challenges to process integration, such as dry etching, wet cleaning and chemical mechanical polishing (CMP). In this work, changes in dielectric and chemical properties of self-assembly surfactant templated nanoporous silica dielectric thin films after photolithography and dry etch processes were studied. The photoresist pattern can be well transferred to the nanoporous silica film after the dry etch process. However, the trimethylsilylated nanoporous film, which was originally hydrophobic, became hydrophilic after the dry etch process and photoresist stripping. It was found that photoresist diffused into the nanoporous film if no barrier layer was deposited to protect the nanoporous film. The capacitance and leakage current greatly increased after patterning, and the dielectric degradation was ascribed to ion damage and moisture uptake. From FTIR and AES analyses, the organic methylsilane groups on the pore surfaces in the film were completely removed after photoresist strip, thereby water adsorption became vital. A post-etch thermal anneal at 400°C, followed by an HMDS vapor treatment, could effectively restore the hydrophobicity of the nanoporous silica films, and thus improved the dielectric properties of the nanoporous dielectric as well. Dry etch characteristics of both the blanket and patterned nanoporous silica films will be discussed.

E8.3
ELECTRICAL, MECHANICAL, AND STRUCTURAL PROPERTIES OF FLUORO-CONTAINING POLY(SILSESQUIOXANES) BASED POROUS LOW-k THIN FILMS. Jingyu Hyeon-Lee, Jihoon Rhee, Jungbae Kim, Jin-Heong Yim, Seok Chang, Samsung Advanced Institute of Technology, E-Polymer Laboratory, Suwon, KOREA.

As device dimension decreases, new materials with low dielectric constants are required to reduce signal delays, power consumption, and cross talk between interconnects. Among low dielectric materials, porous SOGs are potentially very attractive candidates. In this work, low dielectric fluoro-containing poly(silsesquioxanes) have been synthesized using trifluoropropyl trimethoxysilane, methyl trimethoxysilane and 2,4,6,8-tetramethyl-2,4,6,8-tetra (trimethoxysilylethyl) cyclotetrasiloxane. The properties of fluoro-containing poly(silsesquioxanes) based thin films were studied by electrical, mechanical, and structural characterization. Film was spun on silicon substrate, baked at 150°C and 250°C each for 1min and cured in the furnace at 420°C for 1 hour under vacuum condition. Thermally decomposable trifluoropropyl functional group of the fluoro-containing poly(silsesquioxanes) was used as pore generator and partially contributed to lower dielectric constant. Cyclodextrin was also used as pore generator. The pore generator concentration in the film was varied from 0% to 30%. The dielectric constants of the porous films were found to be in the range of 2.7-1.9 (at 100 kHz). Hardness and Young's modulus were measured by nano-indentation. The hardness and modulus of the porous films were well correlated with pore generator concentration. Positronium Annihilation Lifetime Spectroscopy (PALS) was employed to characterize pore size of the porous film. The pore size of the film was less than 2.2 nm. The nanoporous films showed quite promising properties for commercial application.

E8.4
CHARACTERIZATION OF PHOTOSENSITIVE LOW-k FILMS USING ELECTRON-BEAM LITHOGRAPHY. Shin-Ichiro Kuroki,[a] Toshiaki Hirota, and Takamaro Kikkawa, Research Center for Nanodevices and Systems, Hiroshima Univ, Higashi-Hiroshima, JAPAN. [a]TAZMO Co., Ltd, Okayama, JAPAN.

Low-dielectric-constant (low-k) interlayer dielectric films are essential for high-performance ULSIs. The combination of cupper interconnects and low-k dielectric films can reduce both interconnect delay and the number of interconnect layers. In spite of Cu/low-k, the process cost will increase due to the increase of fabrication steps according to the scaling rule, such as photo-resist coating, dry-etching, and etch-stop-layer processes. The direct patterning of low-k film by electron-beam lithography simplifies the total fabrication process of the damascene technology [1]. Methylsilsesquioxane (MSQ) has low dielectric constant $k = 2.7$, and is a candidate for interlayer low-k film. Polymethylsilazane (MSZ) is a precursor of MSQ. A photo-acid generator (PAG) is added to MSZ, which acquires photosensitivity. Photosensitive MSZ film needs to be placed in humid environment for its photochemical reaction. The moisture absorption treatment was carried out after an electron-beam exposure. However, the critical dimension of the pattern was dependent on the elapsed time from electron-beam exposure to moisture absorption treatment. This indicates that activated protons from the electron-beam exposed PAG diffused, so that it is necessary to reduce the elapsed time. A new process was developed for MSZ precursor by absorbing moisture before electron-beam exposure. In conclusion, the improved process of the moisture absorption treatment before electron-beam exposure was developed and the minimum feature size of 90 nm with the aspect ratio 3.9 was obtained, which can be practically used. [1] T. Kikkawa, T. Nagahara, and H. Matsuo, Appl. Phys. Lett., **78**, 2557(2001).

E8.5
SPECTRUM OF DEFECT STATES IN POROUS ORGANIC LOW-k DIELECTRIC FILMS, ANNEALED IN ARGON AND NITROGEN. V. Ligatchev, T.K.S. Wong, T.K. Goh, Rusli, Suzhu Yu, School of Electrical and Electronic Engineering, Nanyang Technological University, SINGAPORE.

Defect spectrum N(E) of porous organic dielectric (POD) films is studied with capacitance deep-level-transient-spectroscopy (C-DLTS) in the energy range up to 0.7 eV below conduction band bottom E_c. The POD films are produced by spin coating onto 8-inch p-type (1 - 10 Ohm*cm) single-side polished silicon substrates, undergoing normal baking (325°C) and curing (425°C) in hot plate and furnace.

The film thickness is in the 5000 - 6000 Å range. The "sandwich"-type NiCr/POD/p-Si/NiCr test structures perform both rectifying DC current-voltage characteristics, and linear C^{-2} vs. DC bias dependence at the reverse voltage. These prove the C-DLTS technique applicability for the defect spectrum deconvolution, and point out to n-type of DC conductivity in the studied films. The POD samples, annealed in argon and in nitrogen are investigated. Isochronal (30 min in argon or 60 min in nitrogen) treatment has been done at the different (from 300°C to 650°C) annealing temperatures. Shape of the N(E) distribution is only slightly affected by alteration of annealing temperature in argon, but the distribution is strongly varied on the annealing temperature in nitrogen ambient. In particular, strong N(E) peak at the E_c - E = 0.55 - 0.60 eV is detected in all samples, annealed in argon, but such peak practically totally disappears in the samples, annealed in nitrogen at $T_a > T_g$ (the glass transition temperature T_g value is about 480°C for the studied material). From the other hand, two new strong peaks (at E_c - E = 0.12 and 0.20 eV) appear in the N(E) spectrum of the samples, annealed in nitrogen at T_a = 650°C. The reported alterations of the defect spectrum are attributed to differences in the argon and nitrogen abilities to interact with dangling carbon bonds on the intra-pore surfaces.

E8.6
INVESTIGATION OF CHEMICAL STRUCTURE INSIDE PORE SURFACE TO ENGINEER ESSENTIAL ISSUES IN INTEGRATION OF POROUS LOW-k FOR LSI DEVICE. Hyun-Dam Jeong, Jung-Bae Kim, Kwang-Hee Lee, Jin-Heong Yim, Sang-Kook Mah, Ji-Hoon Lee, Hyeon-Jin Shin, and Jae-Geun Park, E-Polymer Lab., Samsung Advanced Institute of Technology, Suwon-city, Kyungki-do, KOREA.

The industry has been strongly interested in integrating porous low dielectric constant materials to meet new technical demands of future LSI device. Porous silica films are strong candidates among those, which were formed from new silsesquioxane (SSQ) polymer by the addition of a sacrificial material to the SSQ. The electrical property of the porous silica films was significantly affected by chemical structure of pore surface. Local bonding geometry of siloxane network inside nanopore was also investigated by using Auger Electron Spectroscopy (AES) and Time-of-Flight Secondary Mass Spectrometry (TOF-SIMS). Formation of surface hydroxyl groups in the films was related to increase in dielectric constant and dissipation factor. The electrical properties were monitored with varying porogen contents. These results indicated that there is obvious difference between pore surface and wall regions in siloxane network structure. This work will provide chemical structure model of pore surface used to engineer critically chemical diffusion and plasma damage problems, which are generated in integration of porous low-k for LSI device.

E8.7
INTERACTION OF UNIT PROCESS STEPS WITH SiCOH DIELECTRICS. S.M. Gates, K. Kumar, T.J. Dalton, IBM T.J. Watson Research Center, Yorktown Hts., NY, and IBM Microelectronics, Hopewell Junction, NY; M.A. Worsley, S.F. Bent, Dept. of Chemical Engineering, Stanford University, Palo Alto, CA.

During formation of BEOL interconnect structures, unit process steps may modify a thin layer of a SiCOH composition dielectric. These materials are also known as "carbon-doped oxide" or "organosilicate glass". Here, effects of resist strip and CMP are considered. Blanket films of SiCOH dielectrics are exposed to strip and CMP processes, and various methods are used to characterize a thin modified layer formed near the dielectric surface. Non-destructive methods include XPS, water contact angle and spectroscopic ellipsometry (SE). As shown by others 1 etching in dilute HF can also be a useful tool. Here, we compare these methods in an effort to select from the available process chemistries and to minimize the modified layer effects. 1 A Manufacturable Copper/Low-k SiOC/SiCN Process Technology for 90nm-node High Performance eDRAM, K. Higashi and co-workers; Proc. IITC 2002.

E8.8
Transferred to E3.29

E8.9
DETERMINATION OF PORE SIZE DISTRIBUTIONS IN NANO-POROUS THIN FILMS FROM SMALL ANGLE SCATTERING. Barry J. Bauer, Ronald C. Hedden, Hae-Jeong Lee, Christopher L. Soles, Da-Wei Liu, National Institute of Standards and Technology, Polymers Division, Gaithersburg, MD.

Small angle neutron and x-ray scattering (SANS, SAXS) are powerful tools in determination of the pore size and content of nano-porous materials with low dielectric constants (low-k) that are being developed as interlevel dielectrics. Several models have been previously applied to fit the scattering data in order to extract information on the average pore and/or matrix size. A new method has been developed to provide information on the size distributions of the pore and matrix phases based on the "chord length distribution" introduced by Tchoubar and Mering. Examples are given of scattering from samples that have size distributions that are narrower and broader than the random distribution typical of scattering described by Debye, Anderson, and Brumberger. Size distributions of SANS analysis are compared to measurements made by capillary porosimetry on the same films.

E8.10
CHARACTERIZATIONS AND PREPARATIONS OF POROUS LOW DIELECTRIC FILMS USING VARIOUS CYCLODEXTRINS AS TEMPLATE MATERIALS. Jin-Heong Yim, Jung-Bae Kim, Hyun-Dam Jeong, Yi-Yeoul Lyu, Sang Kook Mah, Jingyu Hyeon-Lee, Kwang Hee Lee, Seok Chang, E-Polymer Lab., Samsung Advanced Institute of Technology, Kyungki-do, KOREA; Y.F. Hu, J.N. Sun, D.W. Gidley, Dept of Physics, University of Michigan, Ann Arbor, MI.

Porous low dielectric films containing very small pores (< 20°) with low dielectric constant(< 2.2), have been prepared by using various kinds of cyclodextrin derivatives as porogenic materials. The pore structure such as pore size and interconnectivity could be controlled by varying matrix precursors and functional groups of cyclodextrin derivatives. In this study, we have characterized the pore structure of the thin films by means of FE-SEM, N2 adsorption methods, and Positronium Annihilation Lifetime Spectroscopy (PALS). We have also monitored the electrical properties and mechanical properties of the porous thin films in order to know the potential as low-k materials. We found that the mechanical properties of the porous low-k thin films prepared with CSSQ precursor and cyclodextrin derivatives were correlated to pore interconnection length. Pore size and pore interconnectivity strongly depend on porogen contents in the precursor as well as the functional groups of cyclodextrin derivatives. The longer interconnection length of nano pores in the thin film, the worse the mechanical properties of the thin film such as hardness and modulus.

E8.11
METHYLSILYLATION OF NANOPOROUS SILICA THIN FILMS VIA GAS TRANSPORT FROM AMORPHOUS HYDROGENATED SILICON CARBIDE FILMS. F.M. Pan, B.W. Wu, A.T. Cho, T.G. Tsai, K.C. Tsai, National Nano Device Laboratories, Hsinchu, TAIWAN; K.J. Chao, Dept of Chemistry, National Tsinghau Univ, Hsinchu, TAIWAN; J.Y. Chen, and L. Chang, Dept of Materials Science and Engineering, National Chiaotung Univ, Hsinchu, TAIWAN.

Nanoporous silica dielectric materials are extensively recognized as a potential candidate for interlayer dielectrics (ILD) for sub-100 nm integrated circuit (IC) technologies because of their ultra-low dielectric constants and chemical compatibility with contemporary process technology. Due to the highly porous nature, the as-calcined nanoporous silica films prepared by sol-gel methods are generally hydrophilic resulting in a poor dielectric property. Trimethylsilylation is usually used to modify the hydrophilic nanoporous dielectric to become hydrophobic. In the study, we used thin α-SiC:H films grown by high-density plasma chemical vapor deposition (HDP-CVD) to provide hydrocarbon gas species for hydrophobicity modification for molecularly templated nanoporous silica thin films. The HDP-CVD α-SiC:H films using trimethylsilane (3MS) as the precursor were deposited on the nanoporous silica films, which had a pore size of $\sim$4 nm, at various substrate temperatures. Auger electron spectra (AES) show that carbon uniformly distributes in the nanoporous silica thin layer. The carbon content in the nanoporous film depends on the substrate temperature during the α-SiC:H deposition. Electron spectroscopy for chemical analysis (ESCA) suggests that carbon found in the nanoporous silica dielectric is probably in the chemical form of hydrocarbons. Voids formed in the α-SiC:H films can trap hydrocarbon species and act as the diffusion paths for the trapped gas species to travel through the α-SiC:H film to the nanoporous silica film. A very low effective dielectric constant (1.72) can be obtained for the α-SiC:H/nanoporous silica film stack. The dielectric property of the film stack is stable over 15 days in the cleanroom ambient. This study shows that hydrophobicity modification of the nanoporous silica film and the etch stop layer deposition can be completed at the same time during the α-SiC:H deposition.

E8.12
EFFECT OF MICROSTRUCTURE ON MECHANICAL RELIABILITY OF NANOPOROUS ORGANOSILICATE THIN FILMS. Suhan Kim, Kookheon Char, Seoul National University, School of Chemical Engineering, Seoul, KOREA; Yvete A. Toivola, Robert F. Cook, University of Minnesota, Department of Chemical Engineering and Material Science, Minneapolis, MN; Jin-Kyu Lee, Do Yeung Yoon, Seoul National University, Department of Chemistry, Seoul, KOREA; Hee-Woo Rhee, Sogang University, Department of Chemical Engineering, Seoul, KOREA; Moon Young Jin, Korea Research Institute of Chemical Technology, Advanced Materials

Division, Taejon, KOREA; Sang Youl Kim, Korea Advanced Institute of Science and Technology, Department of Chemistry, Taejon, KOREA.

As the feature size in advanced ULSI microelectronic devices shrinks continuously, it is expected that low-k interlayer dielectric materials with k lower than 2.5 would be needed around 2005. A continuous reduction of the dielectric constant k is also believed to be possible only by incorporating nanometer-sized pores filled with air (k = 1.0) into the electrically insulating matrices such as poly(methyl silsesquioxane) (PMSSQ). Whenever air incorporated into ultra thin films for lowering k, the mechanical strength of the films is sacrificed. Nanoporous films are formed using the micro phase separation between a matrix and a pore generating polymer. The domain size of the phase separated pore generating polymers is controlled by the number of functional groups of a matrix and a core structure of the pore generation polymer, thus allowing the pore size to be controlled. Pore size of nanoporous films could affect the mechanical strength of films. Elucidation of the effect of pore structure on mechanical strength should minimize the sacrifice in mechanical properties of nanoporous films. In present study, in order to investigate the effect of pore size on mechanical properties, nanoporous ultra low-k films were prepared with MSSQ copolymers and star-shaped poly(caprolactone) (PCL) with different core structures. Nanoporous structures including shape, size, and distribution of pores across the film were investigated using field emission scanning electron microscopy. Micromechanical characterizations were also carried out, using a nanoindentor to measure hardness, modulus and cracking properties of the nanoporous thin films, showing a strong correlation between pore structure and micromechanical properties.

E8.13
PROPERTIES OF MESOPOROUS LOW-k DIELECTRIC THIN FILMS PROCESSED UNDER LOW THERMAL BUDGET.
Thomas A. Deis, Thomas R. Gaffney, Steven G. Mayorga, and Lee A. Senecal, Schumacher, Carlsbad, CA; James E. Mac Dougal and Scott J. Weigel, Air Products and Chemicals, Inc., Allentown, PA.

Properties of low-k dielectric thin films were investigated as a function of formulation and processing variables. Formulation variables investigated included inorganic and organic siloxane content, porogen type and porogen content. All films were processed under low temperature (~400°C), short duration (< 5 min.) conditions. Physical, mechanical and electrical properties of films are reported. Using this limited thermal budget, films with a dielectric constant of 2.0 and an elastic modulus of 4.0 GPa were obtained, while maintaining an average pore size of ~3 nm with a narrow distribution. In addition, films exhibited high adhesive strength and were successfully integrated into a dual-damascene copper integration scheme.

E8.14
KINETIC STUDY ON PECVD TO DEPOSIT LOW-k a-C:F FILMS USING APPEARANCE MASS SPECTROMETRY.
Takumi Tokimitsu and Yukihiro Shimogaki, Univ of Tokyo, Dept of Materials Engineering, Tokyo, JAPAN; Tetsuya Okamoto, Tsuyoshi Kano, Nobuo Haneji, and Kunio Tada, Yokohama National Univ, Div of Electrical and Computer Engineering, Yokohama, JAPAN.

Kinetic study on plasma process to produce low dielectric constant a-C:F thin films from C_4F_8 was made by chemical reaction engineering approach. In the present study, we assumed that the reactor as a CSTR (continuously stirred tank reactor) and examined the residence time dependency of gaseous species concentration. This approach is quite effective to elucidate the reaction mechanism that governs the performance of plasma reactor. Ionization voltage controlled AMS (appearance mass spectrometry) was conducted and it was found to be possible to measure the absolute concentration of each molecule. The residence time dependency of C_4F_8, C_2F_4 and C_2F_6 concentrations were measured by this technique. Through this analysis, dissociation of C_4F_8 and intermediate behavior of C_2F_4 and C_2F_6 were observed. It was found that the main species in plasma changed from C_4F_8 to C_2F_4, and finally changed into C_2F_6 as residence time gets longer. Each gas phase reaction rate would get faster as the pressure gets low, and plasma power gets higher. Quantitative understanding is that, electron temperature gets high as the pressure gets low, and electron density gets high as the power gets high. The relation between major gaseous species and the film properties, such as dielectric constant, IV characteristics, film composition and structure, will be discussed.

E8.15
COMPARATIVE STUDIES OF DIFFERENT TYPES OF NANOPOROUS LOW-k DIELECTRIC FILMS USING X-RAY POROSIMETRY. Hae-Jeong Lee, Christopher L. Soles, Da-Wei Liu, Barry J. Bauer, Eric K. Lin, Wen-li Wu, National Institute of Standards and Technology, Polymer Division, Gaithersburg, MD; Alfred Grill, IBM T. J. Watson Research Center, Yorktown Heights, NY.

The characterization of pore structure in the porous thin films is essential to develop robust low dielectric constant materials that are compatible with adjacent semiconductor processes. X-ray porosimetry (XRP) is newly developed technique to extract the detailed pore structures of porous films such as pore size distribution (PSD), wall density, and porosity. Specular x-ray reflectivity (SXR) has been used to determine the mass uptake of probe molecules in porous thin films supported on thick silicon wafers. The adsorption occurs by capillary condensation when the films are exposed to probe vapor at controlled partial vapor pressures. The partial pressure of the solvent has been varied by changing sample temperature at a constant vapor concentration. PSD in the films was calculated from the probe uptake by using the Kelvin equation to convert partial pressure into pore size. XRP is a powerful technique applicable in the semiconductor industry as an in-situ measurement tool without additional assumption concerning physical parameters. In this work, we perform comparative studies using three different types of nanoporous low-k materials on the silicon substrate to investigate the influence of film formation on the detailed structural information. The samples are porous hydrogensilsesquioxane (HSQ), porous methylsilsesquioxane (MSQ) and porous chemical vapor deposited (CVD) type materials. We shall demonstrate that while the dielectric constants of these three samples are similar, approximately 2.2 to 2.4, the pore characteristics are very different. Specifically, we measure the porosity, PSD, wall density, and average film density using XRP. Then these results are compared with those from the combination of small angle neutron scattering (SANS), SXR and ion beam scattering.

E8.16
PLASMA HYDROGENATION - A NEW METHOD OF REDUCING THE k VALUE OF THE LOW k POLYIMIDE FILM. Yue Kuo, Taewoo Chung, and H. Nominanda, Thin Film Microelectronics Research Laboratory, Dept of Chemical Engineering, Texas A&M University, College Station, TX.

A new method of lowering the dielectric constant (k) of a low k polyimide film by plasma hydrogenation has been studied. The influence of the plasma process to the film's material properties, such as the composition, binding energies, and bond types, and dielectric characters, such as k and leakage current, were investigated. The result showed that after hydrogenation, the film's chemical and physical structures were changed. The film's k value could be lowered to 2.3 or less and the leakage current was only slightly increased. This is an effective method in preapring dielectrics with very low k values, which is critical for the success of the multilevel interconnection structure.

E8.17
OPTIMIZED MATERIALS PROPERTIES FOR ORGANOSILICATE GLASSES PRODUCED BY PLASMA ENHANCED CHEMICAL VAPOR DEPOSITION. Mark L. O'Neill, Raymond N. Vrtis, Jean L. Vincent, Aaron S. Lukas, Mark D. Bitner, Eugene J. Karwacki, Y.L. Cheng[a,b], Y.L.Wang[a,c], and M.S. Feng[b] Electronics Technology, Air Products and Chemicals, Inc.; [a]Taiwan Semiconductor Manufacturing Co., Ltd. Hsinchu, Taiwan, R.O.C.; [b]Department of Materials Science and Engineering Natl. Chiao-Tung University, Hsin-Chu, Taiwan, R.O.C.; [c]Department of Electrical Engineering National Chi-Nan University, Nan-Tou, Taiwan, R.O.C.

The leading interlayer dielectric candidates for the 90 nm technology node are organosilicate glasses (OSGs) produced by plasma-enhanced CVD. In this paper we examine relationship between precursors structure and material properties for films produced from several leading organosilicon precursors on a common processing platform, an Applied Materials 200mm DxZ chamber. Providing materials with extendibility beyond a single generation solution requires the optimization of both electrical and mechanical properties. These are competing goals since concomitant with reducing the dielectric constant (κ) is, in general, decreased mechanical strength. The introduction of porosity to a silicate network, for example, leads to serious degradation in mechanical properties. We found that the nature of the precursor has the most significant impact on film structure, composition and properties. OSG films have an O:Si ratio less than 2:1 due to the replacement of Si-O bonds by organic groups. Precursors that have an O:Si ratio of 2:1 in their structure inherently provide the proper amount of oxygen for good silicate network formation. The types of species occupying the remaining bonds to Si also play a significant role. Our work indicated the optimal precursor to be diethoxymethylsilane (DEMS), which contains two Si-O bonds, one methyl group, and a sacrificial hydride that enables good network formation. The result of our study to balance both electrical and mechanical properties for OSG films suggests that the optimal structure has only one methyl group for every two Si atoms. Films produced from DEMS have κ=2.75 and H=1.6 GPa. Identifying the

precursor structure providing the optimal balance between electrical and mechanical properties will provide the maximum opportunity for extension to future generation dielectrics. The presentation will focus on structure-property relationships of OSG precursors and initial integration work for DEMS-based low κ films.

E8.18
SIMS AND RBS (HFS), NRA CHARACTERIZATION FOR LOW-k FILMS. Vivian (Zhongfen) Ding, Luncun Wei, Charles Evans & Associates, Evans Analytical Groups, Sunnyvale, CA.

Low-K films are often composed of Si, O, C, H, F and N as the major or minor components. The films are often porous and unstable. Low primary beam energy Secondary Ion Mass Spectroscopy (SIMS) with good charge compensation is a good tool for the characterization of Low-K films. SIMS depth profiles can provide the details of the concentration fluctuations of the major components and impurities. The real film thickness can be obtained by directly measuring the SIMS craters using surface profilometry. SIMS is a relative method for quantitative information because the secondary ion yield depends on matrix materials and other factors. SIMS quantification is based on standards of the elements of interest with known atomic dose or concentration in matrices. For the Low-K films, ion beam analysis such as Rutherford Backscattering Spectroscopy (RBS), Hydrogen Forward Scattering (HFS) and Nuclear Reaction Analysis (NRA) can give the absolute atomic dose or concentration of the major components of the low-K films with good accuracy. However, the depth resolution of ion beam methods is poor, especially when the film is not homogeneous. SIMS is well known for its high depth resolution and high sensitivity (low detection limits), especially for layered stacks or inhomogeneous films. Relative sensitivity factors (rsf) for SIMS quantification can be calculated based on the RBS, HFS and NRA absolute concentrations or doses. Depth profiles with depth resolution better than 5nm and 4 orders of magnitude dynamic range (0.01 atomic % to 100 atomic %) can be obtained for the major components and impurities. The porosity and density of the Low-K films can also be calculated quite accurately using the RBS areal density measurements and the surface profilometer measurements of the physical film thickness.

E8.19
BUILDING STRONGER ORGANIC LOW DIELECTRIC CONSTANT MATERIALS: A NANOCOMPOSITE APPROACH. Qinghuang Lin, Stephen Cohen, Eva Simonyi, David Klaus, Jeffrey Hedrick, and John Warlaumont, IBM T.J. Watson Research Center, Yorktown Heights, NY.

The scaling of semiconductor devices requires continuous enhancement of low dielectric constant (low-K) materials to improve performance and reliability of dual damascene low-K/Cu interconnects. Organic thermoset resins, such as SiLK, are leading low-K candidates for 130nm node technology and beyond. SiLK offers a wide range of desirable properties and has been successfully integrated into 130nm generation devices. However, its relatively low mechanical properties and high coefficient of thermal expansion (CTE) have prevented its more wide-spread adoption and also posed as formidable reliability challenges. In this paper, we present a new approach to improving the thermo-mechanical properties of SiLK by incorporating inorganic nanoparticles with sizes less than 10nm. The incorporation of the inorganic nanoparticles enhances both elastic modulus and hardness of the resultant SiLK nanocomposites. Moreover the dielectric constant and resistance to crack growth are also preserved with up to 20wt% of the inorganic component. The mechanical properties can be further improved by strengthening the interfacial adhesion between SiLK matrix and the inorganic nanoparticles. Morphologies and reactive ion etch behaviors of the SiLK nanocomposites will be discussed.

E8.20
EFFECTS OF SUPERCRITICAL CO2 DRYING AND PHOTORESIST STRIP ON LOW-k FILMS. Zhengping Zhang, R.A. Orozco-Teran, Dept. of Materials Science; D.W. Mueller, B.P. Gorman, Dept. of Physics; and R.F. Reidy, Dept. of Materials Science, University of North Texas, Denton, TX.

ITRS future interlayer dielectric (ILD) requirements necessitate reductions in dielectric constant initially to 2.2 and, within five years, 1.3, requiring increased porosity in these materials. Due to gaseous-like transport properties and near liquid-like densities, supercritical methods have been developed to dry and strip resist from these highly porous materials. Although carbon dioxide is a non-polar molecule, its solvating capability in the supercritical state can be tailored by varying pressure, temperature, and cosolvents. In addition, supercritical CO2 is non-toxic and has relatively low critical temperatures and pressures. We have conducted experiments on several porous low-k films examining changes in their properties resulting from exposure to supercritical CO2-based fluids (SCF). In both stripping and drying processes, several co-solvent systems, as well as pressure, and temperature have been varied to determine the robustness of these films in supercritical environments. Ellipsometry was conducted to determine changes in porosity, film thickness, and electronic polarization. Nanoindentation was conducted to define mechanical and, possibly, structural changes resulting from supercritical treatment. In-situ supercritical FTIR experiments were used to study changes in film chemistry and ionic polarization during supercritical processing.

E8.21
CHARACTERIZATION OF BORON NITRIDE FILMS DEPOSITED BY LOW TEMPERATURE CHEMICAL VAPOR DEPOSITION. E. R. Engbrecht, C.J. Cilino, Y.-M. Sun, J.M. White, and J.G. Ekerdt, Department of Chemical Engineering, The University of Texas at Austin, Austin, TX; K.H. Junker, Motorola, Austin, TX.

Boron nitride films were deposited by thermal chemical vapor deposition (CVD) for potential application as an insulating diffusion barrier and etch stop for copper interconnects. Films were deposited at 360 to 565°C on thermal SiO_2 using dimethylamine borane complex (DMAB), $(CH_3)_2NH{:}BH_3$, with ammonia. The effects of temperature and ammonia flow on barrier film properties have been studied. Films deposited without ammonia show decreased boron content and increased nitrogen and carbon content as measured by X-ray photoelectron spectroscopy for increasing substrate temperature, with a composition of $BC_{0.26}N_{0.15}$ at 360°C. The N 1s and C 1s chemical states show increased N-B and C-B bonding, respectively, at higher temperature with a reduction in C-N bonding, suggesting more complete decomposition of the complex at higher temperatures. For films deposited at 360°C, the nitrogen content increased with ammonia flow to a N:B ratio of ~0.6 (ammonia to carrier gas flow rate ratio of 1:1). The carbon content decreased from 18 to 3 at. % at higher ammonia flow rates. Fitted B 1s XP spectra indicated three chemical states present at 188.3, 189.2, and 190.4 eV, representing B-B, B-C, and B-N, respectively. Higher ammonia flow decreased B-B and B-C chemical states and increased B-N. Films appeared amorphous when analyzed by X-ray diffraction, and exhibited surface roughness of ~0.30 nm measured by AFM. The dielectric constant, k, was calculated from spectroscopic ellipsometry measurements and Hg probe metal-insulator-semiconductor capacitance-voltage measurements. k decreased with increasing ammonia flow from 4.6 for $BC_{0.26}N_{0.15}$ to 4.3 for $BC_{0.05}N_{0.58}$, and should decrease further at higher N:B atomic ratios.

E8.22
DETERMINATION OF PORE SIZE AND SIZE DISTRIBUTIONS IN ULTRALOW-k INTERLAYER DIELECTRICS. Elbert Huang, Christy Tyberg, Jeffrey Hedrick, Alfred Grill, Vishnubhai Patel, Matthew Colburn, Qinghuang Lin, Eva Simonyi, IBM T.J. Watson Research Center, Yorktown Heights, NY; Michael Toney, Ho-Cheol Kim, Willi Volksen, James Hedrick, Craig Hawker, Victor Lee, Teddie Magbitang, Eric Connor, Robert Miller, IBM Almaden Research Center, San Jose, CA; Lawrence Lurio, Northern Illinois Univ, Dept of Physics, IL.

The successful utilization of porous materials as ultralow-k interlayer dielectrics (k=1.5-2.2) requires that the pores are substantially smaller than minimum device features. Consequently, accurate and quantitative measurements of the pore size and pore size distribution is necessary in order to design dielectric systems and optimize integration processes. Small angle x-ray scattering (SAXS) measurements have been performed on a variety of dielectric systems to quantify the pore structure. Porous dielectrics encompassing a range of pore sizes, i.e., 1-100 nm, and having diverse chemistries including porous SiLK(TM), porous silsesquioxanes, and porous CVD SiCOHs, have been examined. The information generated from these studies has been invaluable to the implementation of porous dielectrics as it provides a means in which the pore structure and its formation can be correlated to the design and processing of the dielectric system.

SESSION E9: PROPERTIES OF LOW-k THIN FILMS
Chairs: Paul H. Townsend and Do Y. Yoon
Friday Morning, April 25, 2003
Golden Gate B2 (Marriott)

8:30 AM *E9.1
INTERFACIAL CHEMISTRY AND ADHESION IN MICROELECTRONIC DEVICES. Michael Lane and Robert Rosenberg, IBM T.J. Watson Research Center, Yorktown Heights, NY.

Incorporation of disparate metallization and dielectrics in microelectronic devices presents a number of challenges related to their overall robustness and reliability. Often a metal/dielectric interface, such as Cu/SiN, or a semi-noble metal/reactive metal interface, such as Cu/Ta, is required in the device build. Because these materials have different reactivities (Cu/Ta) or form nonmetallic

interfaces (Cu/SiN), the properties of the bimaterial interface is determined by the bonding at the interface which in turn is influenced by the deposition environment and the segregation of impurities to the interface. Therefore, there is a need to develop models which allow one to understand these effects and in turn produce more reliable structures. Accordingly, this paper will demonstrate relationships between seemingly unrelated interfacial phenomenon, such as adhesion and electromigration, and show that they may be understood by consideration of simple models of interfacial strength.

9:00 AM E9.2
EFFECT OF CHEMICALLY ACTIVE ENVIRONMENTS ON SUBCRITICAL CRACK-GROWTH IN LOW-k DIELECTRIC MATERIALS. Eric P. Guyer, Reinhold H. Dauskardt, Department of Materials Science & Engineering, Stanford, CA.

Chemical mechanical planarization (CMP) has become a widely used means of fabricating multi-level interconnects in high-density integrated circuits containing copper and low-k dielectrics. The CMP process involves subjecting interconnect structures to an applied polishing force in the presence of an acidic or basic aqueous solution. Previous studies have shown the synergistic effect of moisture and mechanical loads to markedly accelerate debond propagation rates, particularly in dielectric glasses commonly used in interconnect structures. In this presentation, we demonstrate that the additional chemical constituents present in CMP slurries further effect subcritical crack-growth rates in device structures, posing a major challenge for CMP processing. Dilute hydrogen peroxide and buffered solutions with selected pH levels were employed as model test environments to closely simulate the CMP slurries. The mass transport of chemically active species and reaction rate models were utilized to elucidate the mechanisms responsible for subcritical crack-growth behavior in porous methyl silsesquioxane (MSSQ) thin films.

9:15 AM E9.3
INDENTATION FRACTURE TOUGHNESS MEASUREMENTS OF LOW DIELECTRIC CONSTANT MATERIALS. Dylan J. Morris and Robert F. Cook, University of Minnesota, Dept of Chemical Engineering and Materials Science, Minneapolis, MN.

We have been developing an indentation method for estimation of film fracture toughness, with particular focus on low dielectric constant (low-k) thin films. In order to optimize low-k materials selection and microelectronic interconnection integration strategies, a robust metrological method that can be used to evaluate the fracture properties of films is desirable. Conventional indentation toughness analyses, used for ceramics, will be shown to be wholly inapplicable to low-k films. A new crack-driving mechanism has been proposed that potentially explains much of what has been observed in low-k indentation fracture experiments. A fracture mechanics analysis has been developed that is cognizant of the porous nature of low-k films, and is designed to explain changes in fracture behavior when indenter geometry, film thickness, and film elastic properties are changed. Applications relating to low-k material analysis will be discussed, along with comparisons of the toughness properties of various low-k films.

9:30 AM E9.4
SUBCRITICAL DEBONDING BEHAVIOR OF ORGANOSILICATE GLASS (OSG) THIN FILMS. Youbo Lin, J.J. Vlassak, Division of Engineering and Applied Sciences, Harvard University, Cambridge, MA.

Organosilicate glass (OSG) is one of the leading candidates among new low-k dielectric materials that are being assessed for use as the interlayer dielectric (ILD) in integrated circuits at the 90 nm node. Along with electrical performance, its mechanical reliability needs to be evaluated. When an integrated circuit is exposed to a mechanical load in an aggressive chemical environment during the manufacturing process, subcritical crack growth within the OSG film or at the OSG/barrier interface may cause the film stack to delaminate. The load typically arises from residual stresses in the film stack, but could also be caused by mechanical operations such as dicing or chemo-mechanical polishing. In this presentation, we will present data on subcritical crack growth in a number of OSG/barrier layer structures, such as OSG/TEOS, OSG/TaN and OSG/SiNx, obtained using the four-point-bending technique. Data in both controlled ambient and aqueous environments will be reported. We will discuss the effects of sample preparation and environmental factors such as pH and temperature on the subcritical fracture behavior of these systems.

9:45 AM E9.5
USING MULTIDIMENSIONAL CONTACT MECHANICS TO DETERMINE THE POISSON'S RATIO OF POROUS DIELECTRIC FILMS. Barry N. Lucas, Jack C. Hay, Fast Forward Devices, LLC, Knoxville, TN; Warren C. Oliver, MTS Systems Corp., Oak Ridge, TN.

Semiconductor device performance is currently limited by the insulating properties of the dielectric material surrounding the metal conductor. One approach that has been successful in reducing the dielectric constant of these low-k or ultra-low-k materials is to introduce controlled porosity. While this technique has been successful in reducing the dielectric constant, it has come at the cost of dramatically changing the mechanical properties of the insulator and therefore the structural performance of the interconnect structure. This paper will report on the investigation of the mechanical behavior of a series of low-k films with varying degrees of porosity. This work was carried out using a new multi-dimensional contact mechanics tool capable of measuring the elastic response of the film both normal and tangential to the surface. Results of the normal and tangential contact stiffness of the films will be compared as a function of porosity level and discussed within the context of using the Mindlin solution for predicting the Poissons ratio of the film from the ratio of these two experimental variables.

10:30 AM E9.6
ADVANCED CHARACTERIZATION OF ULTRA LOW-k PERIODIC POROUS SILICA FILMS - PORE-SIZE DISTRIBUTION, PORE-DIAMETER ANISOTROPY, AND SIZE AND MACROSCOPIC ISOTROPY OF DOMAIN STRUCTURE. Nobuhiro Hata, MIRAI-ASRC, AIST, Tsukuba, JAPAN; Chie Negoro, Syozo Takada, ASRC, AIST, Tsukuba, JAPAN; Kazuhiro Yamada, Yoshiaki Oku, MIRAI-ASET, Tsukuba, JAPAN; Takamaro Kikkawa, MIRAI-ASRC, AIST, Tsukuba and RCNS, Hiroshima Univ., Hiroshima, JAPAN.

Porous silica films with k-values down to 1.8 were studied, in which cylindrical pores are arranged periodically as is evidenced by X-ray diffraction [1]. Data from measurements of out-of-plane X-ray scattering (XRS) were fitted to calculated scattering curves for the cylindrical pore shape. Nitrogen adsorption experiments were also performed and the results were analyzed by taking into account the cylindrical pore shape. The results from the XRS and nitrogen adsorption showed a good agreement with each other. Anisotropy in pore diameter was investigated by comparing the XRS data measured under in-plane and out-of-plane configurations. The geometrical information about the sizes and arrangements of pores were compared with transmission electron microscope image. The invariance of in-plane XRS data on in-plane rotational angle of the sample evidenced a macroscopic isotropy of domain structure. Reverse-space mapping and rocking-curve measurements of XRS were also made. The FWHM of the rocking curve around the $< 100 >$ diffraction peak of the ordered pore structure was used to calculate the lower limit of the domain size, which was 10 nm, by using the Scherrers formula. Fourier transform infrared spectroscopy (FTIR) was employed to observe vibrational structure of Si-O-Si network in the pore wall. The experimentally obtained correlation between the peak position of asymmetric stretch longitudinal-optical mode at 1200 - 1250 cm^{-1} in the FTIR spectrum and the elastic modulus of the skeletal silica films was used to distinguish the effects of pore and wall structures to the mechanical properties [2]. It is concluded that the obtained information about the structures of both pore and skeleton of periodic porous silica low-k films constitute the bases in aaplying these materials to interlayer dielectrics. 1. K. Yamada, et al, Jpn. J. Appl. Phys., to be published. 2. S. Takada, et al, Ext. Abs. 63rd Autumn Meet. JSAP (2002).

10:45 AM E9.7
CHARACTERIZATION OF NANOPOROUS LOW-k THIN FILMS BY CONTRAST MATCH SANS. Ronald C. Hedden, Barry J. Bauer, Hae-Jeong Lee, National Institute of Standards and Technology, Polymers Division, Gaithersburg, MD.

Much of the recent developmental efforts in low-k dielectrics involve production of nanoporous thin films. It is necessary to characterize the nature of the porosity to guide the synthetic efforts and to correlate a variety of electrical and mechanical properties. Recently, NIST has begun small angle neutron scattering (SANS) contrast match measurements in which a mixture of hydrogen and deuterium containing solvents is used to fill open pores. Films are exposed to solvent vapor, and pores fill with liquid by capillary condensation. Scattering data are recorded for several H/D solvent mixtures of varied composition, and the solvent composition yielding a minimum in scattered intensity (match point) is identified. Film characteristics such as closed pore content, wall heterogeneity, and wall mass density are characterized. Based on the contrast match technique, a new type of vapor adsorption porosimetry experiment is possible. Films are exposed to solvent vapor of the contrast match composition. A solvent vapor delivery apparatus controls the partial pressure of solvent in the sample chamber. The scattering from the unfilled pores is measured as solvent partial pressure is varied stepwise. Measurement of the average size and volume fraction of unfilled pores at each partial pressure then gives information about the pore size distibution. Although the

technique is straightforward only for homogeneous materials, SANS contrast match porosimetry represents a new approach to a fundamental problem in nanoporous materials characterization.

11:00 AM E9.8
X-RAY POROSIMETRY AS A METROLOGY TO CHARACTERIZE LOW-k DIELECTRIC FILMS. Christopher L. Soles, Hae-Jeong Lee, Da-Wei Liu, Ronald C. Hedden, Barry J. Bauer, Wen-li Wu, Eric K. Lin, NIST Polymers Div, Gaithersburg, MD.

We present a form of porosimetry based on X-ray reflectivity that can be readily implemented as a laboratory research tool for evaluating the pore characteristics of low-k dielectric films on a Si wafer. Like most forms of porosimetry, the technique utilizes capillary condensation; upon gradually increasing the partial press of a gas or vapor, condensation occurs in progressively larger pores. By knowing the amount of vapor uptake as a function of the partial pressure (the so-called adsorption/desorption isotherms), pore size distributions and porosity can be extracted using several different analytical expressions common to the field of porosimetry. With low-k dielectric films, the total mass of the condensed vapor in the sub-micron thick film is exceedingly small and conventional techniques that measure pressure or mass changes usually lack the appropriate sensitivity. However, vapor condensation results in a dramatic increase in the electron density of the film, which is manifest as an appreciable increase in the critical angle for total X-ray reflection. We demonstrate how these changes in the critical angle as a function of the vapor partial pressure can be used to generate an adsorption/desorption isotherm. Furthermore, if the atomic composition of the film and the adsorbing vapor are known, the isotherms can be made quantitative in terms of absolute porosity. We demonstrate the technique using toluene vapor and several typical low-k dielectric films. Details on how to construct such an experimental X-ray porosimeter will be provided, and we shall also critically discuss the use of either temperature or pressure to vary the critical pore size for capillary condensation.

11:15 AM E9.9
OPTO-ACOUSTIC METHODS TO DETERMINE CRITICAL PROPERTIES OF MULTI-LAYERED NANOPOROUS LOW-k DIELECTRIC FILMS. Colm M. Flannery, Colorado School of Mines, Golden, CO and National Institute of Standards and Technology, Boulder, CO; Sudook Kim and Donna C. Hurley, National Institute of Standards and Technology, Boulder, CO.

The development of porous low-k dielectric films for microelectronic interconnect has been severely hindered by the lack of useful and accessible characterization techniques to measure their important properties, especially density/porosity and stiffness. In this talk we present two noncontact opto-acoustic techniques which can provide dependable measurements of these important parameters. The first surface acoustic wave spectroscopy (SAWS) involves detection of a laser-generated surface acoustic wavepacket by a focused Michelson interferometer probe. The presence of the thin dielectric film on the silicon substrate causes a loading of the surface and introduces a frequency dependent dispersion into the wavepacket. Measurement of the dispersion allows one to extract the properties of the layer. The second technique, Brillouin light scattering (BLS), involves measurement of the frequency shift of scattered incident photons caused by collisions with ambient thermal phonon modes in the film. From SAWS density/porosity and Youngs Modulus may be extracted and from BLS, Youngs modulus and Poissons ratio. BLS is also useful to characterize pore size variations and vertical anisotropy in the film. We studied several sets of single- and dual-layer nanoporous polymer and silica thin films on silicon and assessed porosity, and mechanical properties dependence on porosity. Stiffness-porosity relationships varied depending on material and processing conditions, but films with smaller pores (less than 3.5 nm diameter) had better stiffness and interlinking and are more suitable for commercial applications. These noncontact optical methods provide very useful data for process control feedback to allow improvement of film properties and may also be incorporated into in-situ and ex situ monitoring.

11:30 AM E9.10
DEVELOPMENT AND APPLICATION OF ON-WAFER SMALL ANGLE X-RAY SCATTERING FOR THE QUANTITATION OF PORE MORPHOLOGY IN LOW-k POROUS SILK™ SEMICONDUCTOR DIELECTRICS. Brian Landes, Brandon Kern, Kacee Ouellette, Dorie Yontz, Sebring Lucero, Ted Stokich, Jim Godschalx, Jason Niu, Danny King, Carol Mohler, and Jerry Hahnfeld, Dow Chemical Co., Advanced Electronic Materials, Midland, MI; John Quintana and Steve Weigand, Northwestern University, DND-CAT.

The continual drive for faster interconnects requires the development of new interlayer dielectric materials with k values less than 2.2. Porous SiLK semiconductor dielectric resin was developed to achieve these low dielectric constants by introducing nanometer-sized pores into the SiLK resin matrix. A quantitative description of the nano-porous morphology in low-k interlayer dielectrics can be difficult to achieve for many reasons. These include complexities in the porous structure (size range, geometry, pore/pore interaction), inadequate mathematical descriptors, limitations of existing metrology technology, and availability of "tailor-made" experimental samples with a wide range of pore morphologies. On-wafer quantitation of pore morphology is even more difficult as data must now be obtained from extremely limited sample volumes (film coating thickness from ~100-500 nm) residing on thick Si wafer substrates. This presentation will focus on the design, development and successful application of on-wafer small angle x-ray scattering (SAXS) technology to characterize porous SiLK resin morphology. It will be demonstrated, by example, that this technology is able to deliver rapid quantitation over the entire pore size range for these systems. Recently developed data acquisition, reduction and analysis tools will be described. Direct evaluation of the strengths and challenges of several models used to generate average pore size and pore size distribution will be reviewed. Finally, additional capabilities offered by this technology (wafer mapping, detection of killer pores) will also be discussed. ™ Trademark of the Dow Chemical Company

11:45 AM E9.11
DIFFUSION IN POROUS LOW-k DIELECTRIC FILMS. Denis Shamiryan and Karen Maex, IMEC, Leuven, BELGIUM.

A study of polar and non-polar solvent diffusion inside porous materials revealed a relationship between diffusion coefficients and porosity, as well as the polar nature of the materials. Porous materials are being investigated as low dielectric constant (low-k) materials. While porosity decreases the k-value of a material by decreasing its density, it simultaneously allows unwanted adsorption and diffusion of chemicals inside the porous matrix. To investigate this different porous low-k materials, specifically silicon oxycarbide (SiOCH), methylsilsesquioxane (MSQ), and a polymer, were exposed to polar (ethanol) and non-polar (toluene) solvents. It is known from chromatography that polar species diffuse through porous media slower than non-polar species due to presence of polar centers. Hence, a difference in diffusion of polar and non-polar solvents would be an indication of the density of polar centers which attract polar molecules (such as water) and increase the dielectric constant of a film. The diffusion coefficients of ethanol and toluene were calculated by measuring the solvent penetration distance inside the low-k materials as a function of exposure time. The porous low-k films were sealed by deposition of 100 nm SiC layer preventing solvent penetration from the top surface such that penetration could only occur through the edges. This penetration was measured as a color variation by optical microscope. During several seconds of exposure, solvents diffuse from microns (polymers) to hundreds of microns (MSQ) into low-k films. The diffusion coefficient for toluene at room temperature was found to be approximately 2E-5 sq.cm/sec for MSQ (40% porosity), 5E-7 sq.cm/sec for SiOCH (7% porosity), 2E-8 sq.cm/sec for the polymer. Diffusion coefficients increased exponentially with film porosity. The toluene/ethanol diffusion coefficient ratios were 4, 1.7, 1 for MSQ, SiOCH, and the polymer, respectively. The difference in toluene/ethanol diffusion can potentially be used to screen a materials affinity for water adsorption.

SESSION E10: SILICIDES AND DIFFUSION BARRIERS
Chairs: Neil H. Hendricks and Mansour Moinpour
Friday Afternoon, April 25, 2003
Golden Gate B2 (Marriott)

1:30 PM *E10.1
SILICIDES FOR THE 65 NM TECHNOLOGY NODE. Paul R. Besser, Simon Chan, Eric Paton, Jack Thomas, Paul King, Todd Ryan, Brian MacDonald, Technology Development Group, Advanced Micro Devices, Sunnyvale, CA; Thorsten Kammler, AMD Saxony LLC & Co KG, Dresden, GERMANY; David Brown, Laura Pressley, Advanced Micro Devices, Austin, TX.

One of the key challenges for future CMOS technologies is the formation of low-resistance, shallow junctions. A key element in this challenge is the silicide and cobalt silicide is the silicide of choice for most IC manufacturers. Cobalt silicide replaced titanium silicide as the silicide at the 250 nm technology node and has been used for the last four few technology nodes. CoSi2 eliminated the linewidth dependence of silicide sheet resistance exhibited by TiSi2 and provided a low resistivity material on the active and poly silicon while also providing a low resistance contact from the silicide to the silicon, enabling higher performance microprocessors. At the 65 nm technology node, CoSi2 is facing some formidable challenges, however, due to the technology changes expected. These challenges include the polysilicon gate CD eventually reaching the sub-25 nm regime,

implementation of high-K gate dielectrics, selective epitaxial Si and alternative dopants, and introduction of Ge into the channel for increased mobility. With its lower silicide to active resistance and its reduced Si consumption, NiSi is being investigated by many IC manufacturers and universities as a viable alternative to CoSi2, but has not been easily inserted into manufacturing. NiSi has the advantages of not exhibiting a linewidth dependence and forming a low-resistance silicide in the presence of Ge. In this paper, the silicide issues for the 65 nm technology node will be reviewed. Process improvements to extend CoSi2 to narrow linewidths and their effect on the silicide thickness, quality and phase will be shown. In addition, the effect of Ge on the formation of low-resistance CoSi2 and NiSi will be shown.

2:00 PM E10.2
CHEMICAL VAPOR DEPOSITION OF NOVEL RUTHENIUM-BASED BARRIERS FOR COPPER METALLIZATION APPLICATIONS. Filippos Papadatos, Spyridon Skordas, Steven Consiglio, Eric Eisenbraun, Alain Kaloyeros, Univ at Albany, Institute for Materials, School of NanoSciences and NanoEngineering, Albany, NY.

Ruthenium-based materials have previously been investigated for front-end electrode applications. The low resistivity (Ru ρ 10$\mu\Omega$·cm, RuO_2 ρ 45$\mu\Omega$·cm), thermal robustness, and excellent intrinsic barrier properties of these materials also make them attractive for interconnect applications. This work describes the development of low-temperature CVD processes for the growth of Ru and RuO_2 thin films using metal organic chemical vapor deposition (MOCVD) in a 200-mm wafer deposition cluster tool. Optimized processes for Ru and RuO_2 are developed and subsequently employed for copper barrier testing. Ultra-thin (<10 nm) Ru and RuO_2 films are utilized in copper/liner/Si and copper/liner/dielectric/Si stacks for thermal and electrical barrier performance testing. Thermal barrier testing is carried out by annealing the stacks at temperatures between 500 and 700°C. The Cu films are then removed from the annealed samples using nitric acid and the samples examined for the presence of residual copper by Rutherford backscattering spectrometry (RBS). Electrical barrier testing was carried out employing triangular voltage sweep on capacitor structures, and the resulting copper diffusion through the liner into the dielectric measured. In both types of testing, PVD TaN is employed as a material standard. In addition, copper wetting and adhesion performance are measured and compared to PVD Ta/TaN standards. The results indicate that MOCVD Ru and RuO_2 are promising materials for nanoscale barrier applications.

2:15 PM E10.3
ENHANCEMENT OF COPPER WETTING VIA SURFACTANT-BASED POST-TREATMENT OF ULTRA-THIN ATOMIC LAYER DEPOSITED TANTALUM NITRIDE LINERS. Oscar van der Straten, Yu Zhu, Kathleen Dunn, Alain Kaloyeros, UAlbany Institute for Materials & School of NanoSciences and NanoEngineering, University at Albany-SUNY, Albany, NY.

The influence of surfactant-based liner post-treatment on the wetting and nucleation characteristics of ultra-thin (8 nm) copper films has been examined, employing ultra-thin atomic layer deposited (ALD) tantalum nitride (TaN_x) as liner material. This surfactant-based post-treatment consists of in-situ exposure of the liner to a metal-organic source containing a low surface free energy metal (Sn) surfactant, which is a potential candidate for inducing subsequent layer-by-layer growth of copper due to both the high atomic volume and low surface free energy of the surfactant relative to copper. A methodology involving thermally-enhanced de-wetting of copper, promoted by annealing the copper/liner stacks in a forming gas (95% Ar, 5% H_2) ambient at 350°C for 30 minutes, was utilized to relate the resulting surface and interfacial roughness profiles, as analyzed by atomic force microscopy (AFM) and high-resolution transmission electron microscopy (HRTEM), of as-deposited and annealed stacks with post-treated liners to those obtained from stacks containing untreated liners. In conjunction, scanning electron microscopy (SEM) and focused ion beam (FIB) analysis were used to evaluate the effectiveness of the liner surface post-treatments in inhibiting copper de-wetting.

2:30 PM E10.4
THE INTEGRATION OF PLASMA ENHANCED ATOMIC LAYER DEPOSITION (PEALD) OF TANTALUM-BASED THIN FILMS FOR COPPER DIFFUSION BARRIER APPLICATIONS. Degang Cheng and Eric T. Eisenbraun, School of NanoSciences and NanoEngineering, The University at Albany-SUNY, Albany, NY.

A plasma-enhanced atomic layer deposition (PEALD) process for the growth of tantalum-based compounds is employed in integration studies for advanced copper metallization on a 200-mm wafer cluster tool platform. This process employs terbutylimido tris(diethylamido)tantalum (TBTDET) as precursor and hydrogen plasma as the reducing agent at a temperature of 250°C. Auger electron spectrometry, X-ray photoelectron spectrometry, and X-ray diffraction analyses indicate that the deposited films are carbide rich, and possess electrical resistivities less than 300 $\mu\Omega$-cm, one to two orders of magnitude lower than those of tantalum nitride deposited by conventional ALD or CVD of TaN using TBTDET and ammonia. PEALD Ta(C)N also possesses a high density, contributing to a strong resistance to oxidation. Copper integration aspects, including nucleation and copper wetting properties of CVD-grown copper deposited in situ on PEALD Ta(C)N with selected surface plasma treatments are discussed. Additionally, the electrical diffusion barrier performance of Ta(C)N as compared to thermal ALD TaN and PVD TaN, measured using triangular voltage sweep (TVS), will be presented and discussed.

2:45 PM E10.5
REACTION MECHANISMS OF DIMETHYLAMINEBORANE REDUCING AGENT IN ELECTROLESS COBALT PLATING BATHS. Michael J. Kelly, Todd M. Alam, Terry R. Guilinger, Theodore T. Borek, and Carly S. Glauner, Sandia National Laboratories, Albuquerque, NM.

Electroless deposition of cobalt alloys is being widely studied for use in integrated circuit (IC) and microelectromechanical system (MEMS) applications. Thin films of Co-W, Co-P, and Co-W-P alloys are effective as high-temperature diffusion barriers and cladding layers for copper interconnections produced by the dual damascene process. These alloy films also protect Cu metallization from corrosion, prevent Cu diffusion into silicon device regions, and promote good adhesion between Cu and dielectric layers. These attributes of Co alloy films are critical to realizing the superior performance of electroplated Cu interconnects, compared to conventional Al metallization, with respect to resistivity and electromigration. We report the results of an investigation into the reaction pathways of dimethylamineborane (DMAB), a reducing agent frequently used in the electroless deposition of cobalt from alkaline plating baths. Nuclear magnetic resonance (NMR) spectroscopy and gas chromatography (GC) were used to identify and quantitatively analyze the reaction products during plating and post-plating waste treatment operations. In the latter case, acid hydrolysis of DMAB at pH ~1 produces hydrogen gas and soluble boric acid, among other products. High-resolution Boron-11 NMR spectra (at 128.3 MHz) of plating solutions were obtained on solutions at various times during processing. Quantitative analysis of DMAB in the plating bath solutions was performed using the NMR resonances at δ = -11 ppm (pH ~9) and +2 ppm (pH ~1). The NMR resonances at δ = +23 and +12 ppm (for all pH values between ~1-9) were used to quantitate the boric acid formed by DMAB hydrolysis. The stoichiometry of these DMAB reactions was confirmed by quantitative measurement of gas evolution during cobalt plating and during post-plating acid hydrolysis procedures. Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin company, for the U.S. Department of Energy under contract number DE-AC04-94AL85000.

3:30 PM E10.6
INVESTIGATION OF CVD TiN FILMS DEPOSITED AS DIFFUSION BARRIERS FOR THE INTEGRATION OF LOW-k DIELECTRIC. W.C. Gau, C.W. Wu, L.J. Chen, Department of Materials Science and Engineering, National Tsing Hua University, Hsinchu, Taiwan, REPUBLIC OF CHINA; T.C. Chang, Department of Physics, National Sun Yat-Sen University, Kaohsiung, Taiwan, REPUBLIC OF CHINA; P.T. Liu, National Nano Devices Laboratories, Hsinchu, Taiwan, REPUBLIC OF CHINA; C.J. Chu, C.H. Chen, Nanmat Technology Co., LTD., Kaohsiung, Taiwan, REPUBLIC OF CHINA.

In a reliable copper interconnect architecture, inserting refractory diffusion barriers between copper wiring and intermetal dielectrics can effectively prevent copper diffusion. In this work a novel diffusion barrier, $Ti_xC_yN_z$ has been investigated for the integration of copper interconnects and low-dielectric-constant (low-k) insulators. $Ti_xC_yN_z$ films have been deposited using tetrakis-dimethylamino-titanium (TDMAT) and NH_3 as a reaction gas at temperatures ranging from 325 to 400 degree C in multi-layers with intermittent Ar/ NH_3 plasma treatment. The effect of the annealing process and the subsequently performed Ar/NH_3 plasma treatment on the $Ti_xC_yN_z$ has also been investigated. Experimental results have shown that $Ti_xC_yN_z$ barrier films are of nano-crystalline structure. In addition, rapidly thermal annealing and furnace annealing above 500 degree C can decrease the reisitivity drastically due to the reduction in the concentration of carbon. With multi-layer Ar/NH_3 plasma treatment, the resistivity of $Ti_xC_yN_z$ film decreases from 960 to 548 $\mu\Omega$·cm and the concentration of oxygen in barrier films is also decreased. The plasma treatment can remove the organic residue and induce crystallization at the surface of the as-deposited nano-crystalline $Ti_xC_yN_z$ films. The integrity of $Ti_xC_yN_z$ barrier has been further verified by measuring electrical characteristics of test structures, including Cu/CVD-$Ti_xC_yN_z$/SiO_2

and Cu/CVD- $Ti_xC_yN_z$ /low-k after being subjected to thermal annealing in a furnace at 500-800 degree C.

3:45 PM E10.7
PLASMA ENHANCED CHEMICAL VAPOR DEPOSITION OF TANTALUM-SILICON-NITRIDE DIFFUSION BARRIERS FOR COPPER/SILK METALLIZATION SCHEMES. Sumant Padiyar, Wanxue Zeng, Eric T. Eisenbraun, Robert E. Geer, School of Nanosciences and Nanoengineering, University at Albany, Albany, NY.

The continuing decrease in integrated circuit (IC) feature size demands concomitant improvements in the performance of diffusion barrier layers used to isolate the Cu interconnect lines from the surrounding dielectric (including low-k dielectrics). Consequently, we have carried out investigations regarding the integration of high-performance TaSiN diffusion barriers in Cu/SiLK metallization schemes via plasma enhanced chemical vapor deposition (PECVD) method. We report first-pass studies that evaluated the process compatibility of PECVD TaSiN barriers with Dow Chemical's SiLK low-k dielectric. In addition, the diffusion barrier performance of 10 nm thick TaSiN films with varying Si concentration was investigated under thermal stressing at 450°C. Auger Electron Spectroscopy (AES), Rutherford Backscattering Spectrometry (RBS), and X-Ray Reflectivity (XRR) were used to characterize the diffusion barrier performance and thin film morphology before and after thermal stressing. TaSiN/Silicon oxide stacks were used for baseline comparisons. Interfacial adhesion studies of PECVD TaSiN films on SiLK and silicon oxide films are also reported. Second-pass studies were also undertaken to evaluate the growth and conformality of ultra-thin TaSiN diffusion barriers on 0.18 micron feature size dual damascene test structures in SiLK using Transmission Electron Spectroscopy (TEM) and to determine the suitability of the PECVD process for further integration studies. Initial result indicate very good conformal TaSiN barrier deposition

4:00 PM E10.8
A STUDY OF ATOMIC LAYER DEPOSITION AND REACTIVE PLASMA COMPATIBILITY WITH MESOPOROUS ORGANOSILICATE GLASS FILMS. E. Todd Ryan, Advanced Micro Devices, AMD/Motorola Alliance, Austin, TX; Melissa Freeman, Lynne Svedberg, J.J. Lee, Todd Guenther, Jim Connor, and Katie Yu Motorola, Dan Noble Center, Austin, TX; David W. Gidley and Jianing Sun Department of Physics, University of Michigan, Ann Arbor, MI.

Low dielectric constant (low-k) films and barrier metal deposition by atomic layer deposition (ALD) and chemical vapor deposition (CVD) are rapidly developing technologies for sub-90nm integrated circuit (IC) generations. However, if the low-k film is mesoporous, it will be difficult to integrate these technologies because the highly conformal CVD and ALD monolayer deposition processes can coat the pore walls or leave metal precursors inside the mesopores. This paper reports a study of the compatibility of ALD and CVD metal deposition with mesoporous and non-mesoporous organosilicate glass (OSG) films. Blanket film studies using TEM, TOF-SIMS, and positron spectroscopy demonstrate that two ALD deposited metals and CVD TiN penetrate deep into the mesoporous film via the films connected pore structure. He and NH3 plasma pretreatments to the mesoporous OSG film surface did not adequately seal the mesopores to ALD/CVD metal penetration, but the plasmas did damage the surface and in some cases the bulk of the mesoporous OSG film. An ALD barrier deposited into a damascene patterned trench also penetrated into the mesoporous dielectric film along the trench sidewall, which indicates that the etch and strip processes did not seal the sidewall. The results are interpreted in terms of mesoporous film properties, and the paper discusses the implications of these findings for process integration and suggests alternative approaches to integrate ALD with mesoporous dielectric films.

4:15 PM E10.9
FILM PROPERTIES OF ATOMIC LAYER CHEMICAL VAPOR DEPOSITION (ALCVD^{TM})-WN_XC_Y THIN FILM AS A DIFFUSION BARRIER FOR Cu METALLIZATION. Soo-Hyun Kim, Su Suk Oh, Dae-Hwan Kang[a], and Ki-Bum Kim, School of Materials Science and Engineering, Seoul National University, Seoul, KOREA. [a]Research Institute of Advanced Materials, Seoul National University, Seoul, KOREA; Wei-Min Li and Suvi Haukka, ASM Microchemisty Ltd., Espoo, FINLAND.

WN_XC_Y films are deposited in a Pulsar$^{?}$2000 reactor by atomic layer chemical vapor deposition (ALCVD^{TM}) using WF_6, NH_3, triethyl boron (TEB) as precursors at 313°C. The as-deposited film shows a resistivity of about 350 $\mu\Omega$-cm and density of 15.37 g/cm^3 for 25-nm-thick film. The film composition determined by resonance Rutherford backscattering spectrometry (RBS) shows a W, C, and N content of approximately 48, 32, and 20 at. %, respectively. Impurities such as F, B, and O in the film are not detected by Auger electron spectroscopy (AES). Selected area electron diffraction pattern and high-resolution transmission electron microscopy (HRTEM) reveal that the as-deposited film is composed of fcc α-WC_{1-X} or fcc β-W_2N. The as-deposited film is found to have an equiaxed grain structure with the size of 3~7 nm as measured from TEM dark-field and high-resolution images. (ALCVD^{TM})-WN_XC_Y film keeps the nanocrystalline state even after annealing at 700°C for 1 hour. When the annealing temperature increases to 800°C, the film is transformed to hcp α-W_2C and bcc W with the release of nitrogen. Finally, diffusion barrier properties of 12-nm-thick film against Cu are investigated by sheet resistance measurement, x-ray diffractometry (XRD), etch-pit test. XRD shows that (ALCVD^{TM})-WN_XC_Y diffusion barrier fails only after annealing at 700°C for 30 minutes due to the formation of copper silicide. It is thought that the superior diffusion barrier performance of (ALCVD^{TM})-WN_XC_Y film is the consequence of both nanocrystalline equiaxed grain structure and high density.

4:30 PM E10.10
ADHESION STUDY OF LOW-k THIN FILMS WITH SILICON CARBIDE HARDMASK LAYERS. Wei Chen, Glenn A. Cerny, W. Douglas Gray, Christopher S. McMillan, Dow Corning Corporation, Midland, MI.

As the scale of IC devices decreases, low-k materials are being applied in semiconductor manufacturing processes to further reduce RC delays in interconnect structures. The adhesion of low-k films with various barriers and hardmasks has become a critical issue and has a large impact on the reliability of the BEOL structure. Recently, a four point bending method has been adopted to quantitatively measure interfacial adhesion of thin films in the IC industry. We evaluated the adhesion of a variety of low-k materials with amorphous hydrogenated silicon carbide (a-SiC:H) and N2O doped a-SiC:H hardmask films using the four point bending method. Additionally, XPS and cross section electron microscopy were used to establish the debonding surfaces of the four point bending samples. For carbon-doped oxide (CDO) low-k films, the interfacial adhesion energies are 4.8±0.5 J/m^2 with the CDO layers deposited on top of either type of hardmask films. The measured adhesion values did not change as the thickness of CDO films in the range from 0.3 to 1 μm. The adhesion energy values are comparable to that of CDO on TaN. The surface analysis results indicate that fractures occur in the interfaces of the CDO and hardmask films during testing. It appears that, while the CDO films are being deposited on the hardmask layers, thin interfacial layers are formed due to oxidation of the barrier surface, therefore, this interfacial layer consists of both CDO and hardmask chemical characteristics. During the debonding process, the CDO film breaks away from the top of the interface layer. In addition to CDO films, the adhesion of various SOG low-k films, such as FOx (HSQ) and methyl-resins, with a-SiC:H based hardmasks were evaluated. We are also looking into the correlation between the adhesion results and process integration steps, such as CMP.

4:45 PM E10.11
WAFER LEVEL DETECTION OF SEALING DEFECTS. Quoc Toan Le, Frank Holsteyns, Francesca Iacopi, and Karen Maex, Interconnection Technologies and Silicides Department, IMEC, Leuven, BELGIUM.

Most of the low-constant-dielectric materials being evaluated for reduction of capacitance between interconnects in ultra large-scale integrated circuits are, to some extent, porous. To avoid degradation from which may result in a change in their dielectric constant, a sealing layer needs to be deposited on the dielectric surface. However, the presence of defects on the sealing layer itself can lead to the exposure of the dielectric to the environment and hence degradation of the dielectric. In this study, we describe a method for evaluation of the sealing efficiency of a dielectric surface, and determination of minimal sealing thickness of a hardmask (HM) layer that can be used on a given dielectric. The combination of optical inspection and solvent adsorption allows sealing defects at the surface to be localized and quantified. Results on different HM/dielectric stacks, such as CVD HM on CVD dielectric, CVD HM on spin-on dielectric, and spin-on HM on spin-on dielectric, will be presented. It has been observed that in the case of CVD HM, the number of light point defects, in particular the number of particles, initially present on the dielectric surface has a strong impact on the sealing defects detected after HM deposition. Various types of defect were identified including flakes, particles, and voids. For both types of dielectric that have been investigated, i.e. CVD and spin-on, particles appear to be a potential source of sealing defect regardless of whether the HM is CVD or spin-on. The effect of the thickness of the sealing layer on the sealing defects detected is discussed.