SYMPOSIUM C

Silicon Front-End Junction Formation—Physics and Technology

April 13 - 15, 2004

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* Invited paper
Annealing parameters. For offers the clear advantages fRTP anneals in terms of profile and devices. In particular, in optimizing dopant profile, we have analyzed dopant diffusion and activation of fRTP junctions as a function of profile and devices. In this work, we have systematically investigated the junction formation of different implants under (fRTP) anneals in terms of profile and devices. In particular, in optimizing dopant profile, we have analyzed dopant diffusion and activation of fRTP junctions as a function of profile and devices. For devices, we have given particular attention to the leakage behavior of the fRTP annealed junctions that shows for spike-annealed junctions, pre-amorphization conditions provide a critical tool to control and reduce the leakage current of co-implanted fRTP junctions to acceptable levels. We will show how the correct implant and anneal are requested for minimizing pattern effect and improving transistor performance. Flash-assist RTP and fRTP are Vortek trademarks.

9:45 AM *C1.4
SPE integration: Effect of the density and the position of defects on electrical characteristic of 65nm CMOS. Rebeka El Farhan1, Cyrille Laviron1, Pierre Morn1, Christine Rossato1, Veronique Caron1, Yves Monard2, Franck Arnaud2, Arnaud Pouydebasque1, Frank van Wouquet2, Damien Lenoble2 and Aomar Halimaoui1, 2, Crolles 2, Philips semiconductors; Crolles, France; 3, Crolles 2, ST microelectronics, Crolles, France; 4, LETI, CEA, Grenoble.

Solid Phase Epitaxy (SPE) is a promising way to perform ultra shallow and highly activated junctions. This method is used to activate the dopants during the crystallization of amorphized silicon. The main advantage of SPE is to control the junction depth and a low thermal budget that is compatible with high-k and metal gate requirements. The drawbacks are the presence of End Of Range (EOR) defects along the former a-Si deposition interface, which may induce junction leakages and as well as Transient Enhanced Diffusion (TED). It is thus very important to control the density and the position of these defects. We integrated SPEIR into a flow chart compatible with CMOS065 platform. Both extension and deep Source/Drain are fabricated using SPE process. The splits include various Preamorphisation conditions (Ge PAI at different energies and dopant self amorphization) and doping species in order to determine the effects of defect density and position on the electrical characteristics of the devices. For device fabrication, we used our standard 65nm CMOS processes flow. However, we did not perform pockets implants in order to study properly the characteristics of junctions. The electrical characterization has shown that devices with high performance can be achieved by using SPE process. Indeed, a very good Ion/Ioff trade off is achieved for PMOS (Ion =2000 microA/micrometer for Ioff = 1-8A/micrometer) at 0.8 volts. For deep preamorphization, we observed an increase of the threshold voltage for the smallest gate length. In addition, these smallest devices exhibit pocket-like behavior, although no pocket implant was performed. We attributed these effects to dopant diffusion from the channel that are trapped at the crystal defects (generated by the deep PAI). Regarding the junction leakage, the best results are achieved when shallow preamorphization is performed at extensions level and when dopant self-amorphization is used for deep Source/Drain. We will show that this result is consistent with device position. In addition to the electrical characterization results, we will present TEM and SIM data that will be largely avoided.

SESSION C1: Device Junction Engineering
Chair: Marius Orlovski
Tuesday Morning, April 27, 2004
Room 2002 (Moscone West)

8:30 AM *C1.1
Materials Challenges for CMOS Junctions, William J. Taylor, Motorola APRDL, Austin, Texas.

For the engineers and scientists involved in the development of CMOS source/drain technologies, the challenges in the next several generations are perhaps the greatest yet faced. While the past 10 or more years have seen primarily variations to the conventional implant-and-anneal-in-Si, the next 10 will likely involve changes to both the material systems and their manner of introduction. Complicating this is the expectation that the channel and the gate stack systems will simultaneously be undergoing significant change, to address the needs for enhanced mobility and reduced gate leakage. Furthermore, the expectation is that industry will move away from conventional planar bulk CMOS, to ultrathin SOI, double-gated structures, or 3-D devices. Against the backdrop of the ITRS predictions, we will compare methods for dopant introduction and activation, methods for making contact to these regions, and methods for measurement of material and device properties. New anneal tools provide the promise of activation without diffusion, placing the burden of Xj and abruptness upon implanters; we will investigate the feasibility of these tools meeting this challenge for a manufacturing throughput. Concurrent changes in the gate stack, with a likely need to avoid interdiffusion or recrystallization, can be expected to push an upper limit on temperature. We will therefore address the feasibility of low temperature solid phase epitaxial regrowth as a method of dopant activation. Regarding contacts to doped regions - although N+Si facilitates current CMOS integration concerns, its temperature limits can be expected to improve as one goes to 3-D integrations later in the decade. Also on the horizon, movement to separate metals for low-resistance contacts to the N+ / P+ regions is expected to put an upper limit on temperature. We will therefore investigate the feasibility of these tools meeting this challenge for a manufacturing throughput.

9:00 AM *C1.2
Ultra-shallow junctions for novel device architectures beyond the 65nm node, Aditya Agarwal, Advanced Technology Group, Axicel Technologies, Beverly, Massachusetts.

Si chip manufacturing is expected to undergo a paradigm change around the 65nm node. This is due to the rapid introduction of new materials and device structures required for further scaling of performance, such as strained Si, ultra-thin-body and multiple (metal-oxide) devices. These novel architectures raise fundamentally new questions for shallow junction formation, ranging from whether an amorphizing source drain implant is acceptable, as in the case of strained silicon, to whether an ultra-shallow junction is even necessary, as in the case of ultra thin body devices. This paper will review new experimental and simulation data on these and related issues.

9:30 AM *C1.3
Device Characteristics of Ultra-shallow Junctions Formed by fRTP Annealing, Alejandro Satta1, Richard Lindsay1, Kirklen Henson1, Steve McCoy2, Jeff Golpey2, Kiefer Elliott2 and Karen Maex2, 3, 4; 1IMEC, Heverlee, Belgium; 2Vortex Industries Ltd., Vancouver, British Columbia, Canada.

The creation of ultra-shallow junction for devices at sub-100 nm node is driving significant efforts in developing thermal processing able to give rise to high dopant activation in combination with limited diffusion. Flash-assist Rapid Thermal Annealing (fRTP) is a promising new annealing approach, which involves the heating of the bulk of the wafer to an intermediate temperature using either conventional RTP, followed by a short and intense pulse of light localized on the implanted wafer surface. The short pulse of intense light (order of 1-10 ms) is responsible for very high dopant activation level and diffusionless profiles. fRTP offers the clear advantages over the conventional spike anneal of forming junctions with shallower depth and lower resistivity, simultaneously avoiding dramatic modifications to conventional process flow of a CMOS device. In this work, we have systematically investigated the junction formation of different implants under (fRTP) anneals in terms of profile and devices. In particular, in optimizing dopant profile, we have analyzed dopant diffusion and activation of fRTP junctions as a function of profile and devices. For devices, we have given particular attention to the leakage behavior of the fRTP annealed junctions that shows for spike-annealed junctions, pre-amorphization conditions provide a critical tool to control and reduce the leakage current of co-implanted fRTP junctions to acceptable levels. We will show how the correct implant and anneal are requested for minimizing pattern effect and improving transistor performance. Flash-assist RTP and fRTP are Vortek trademarks.

10:30 AM *C2.1
Applications of Silicides to 45 nm CMOS and Beyond, Juraj A. Ki6 and their manners1, Osama Chamaran1, 2, Malgorzata A. Pawlak1, 3, Mark Van Da1, 3, Anil Alkejay3, Muriel De Potter1, Anil Kottantharayil2, Richard Lindsay1 and Karen Maex2, 3, 4, 5IMEC, Leuven, Belgium; 6Affiliate researcher at IMEC from Texas Instruments, Leuven, Belgium; 7Katholieke Universiteit Leuven, Belgium.

SESSION C2: Silicides and Germanides
Chair: Richard Lindsay
Tuesday Morning, April 27, 2004
Room 2002 (Moscone West)
Leuven, Belgium; 4Philips Research Leuven, Leuven, Belgium; 5Affiliate researcher at IMEC from NIFN, Leuven, Belgium.

For the 45 nm node and beyond, modifications or departures from conventional scaling schemes may be necessary, which will impact the integration constraints for silicides, their characteristics or even the very way silicides are used in CMOS circuits. The introduction of a higher gate oxide thickness is deposited by rapid thermal processing (RTA) at a temperature range from 300 to 600 °C, stable NiGe film was formed. At higher temperature, NiGe2 was detected. XRD results also identified textured NiGe film with the underlying substrate: NiGe(111)—Ge(100) from 200 to 600 °C. SEM images of the NiGe film up to 500 °C, after which isolated particles of germaine with exposed underlying substrate were evident. Deepening grooves and prominent grain growth were noticeable as early as 400 °C in our case, indicating the inception of agglomeration. Sheet resistance measurement by four-point probe was also carried out. Sheet resistance as low as 10 Ω/sq. was attained after RTA from 300 to 500 °C, after which the resistance was increased tremendously. The change of sheet resistance with temperature correlated well with the surface morphology of the samples. At early annealing temperatures (below 500 °C), the resistance was governed by the resistivities of the phases present in the film. However, at higher temperatures, the electrical property was no longer controlled by the phases present but by the continuity of the film. In other words, agglomeration of the germaine film resulted in the increased sheet resistance at 600 °C and above.

11:00 AM C2.2
Ni-silicided Deep Source / Drain Junctions formed by Solid Phase Epitaxial Regrowth. Anne Lueneur1, Richard Lindsay1, Kirklen Henson1, Simone Severi1, Amal Akshay1, Bartek Pawlak2, Marel de Potter2 and Karen Meeus1,4,5IMEC, Leuven, Belgium; 2Philips Research Leuven, Leuven, Belgium; 3affiliate researcher at IMEC from NIFN, Leuven, Belgium; 4Katholieke Universiteit Leuven, Leuven, Belgium.

The introduction of high-K dielectrics, metal gates and advanced extension junctions in a conventional CMOS process imposes limitations on the thermal budget that can be allowed to activate the dopants beyond the amorphous region, a very abrupt profile can be obtained with the junction depth being determined by the amorphous region thickness. The abruptness depends on the diffusion length and silicide to diffusion contact resistance were studied for SPER source/drain junctions with junction depths ranging between 40 and 190 nm. Ni-silicide was used to contact the source/drain junctions. A comparison was made between SPER source/drain junctions and conventional spike annealed source/drain junctions with similar junction depth. By careful optimization of the implant and anneal conditions, lower junction leakage and lower contact resistance is obtained for the SPER source/drain junctions and in particular for the silicide to diffusion contact resistance were studied for SPER source/drain junctions. The sheet resistance was not to degrade the sheet resistance of the NiSi.

11:15 AM C2.3
Nickel Germanosilicide Contacts to Recessed and Epitaxially Regrown SiGe(B) Source/Drain Junctions. Christian Isheden, Per-Erik Holstom, Henry H. Rudomson, Shi-Li Zhang and Mikael Ostling, Department of Microelectronics and Information Technology, KTH (Royal Institute of Technology), Kista, Sweden.

pMOS transistors with recessed epitaxial SiGe(B) source/drain junctions formed by selective Si etching followed by selective epitaxial growth of insitu heavily doped SiGe layers are presented. The concept has several benefits compared to conventional junctions, such as dopant activation above the solid solubility in Si, arbitrary junction depth and potential high temperature processing. Another merit is that similar source/drain structures can be implemented. The contacts to the source/drain regions are formed using Ni mono-germanosilicide based on low formation temperature and relatively low Si consumption. A Ni film of 200 Å thickness is deposited by electron-beam evaporation and the Ni mono-germanosilicide is formed by rapid thermal processing (RTA) at a formation temperature below 600 °C in N2. The sheet resistance is below 5 Ω/sq. and the specific contact resistances for the NiSi, NiGe, and NiGe2 are respectively 1x10-5, 1x10-4 and 1x10-3 Ωcm2. Electrical device characteristics for the transistors will be presented.

11:30 AM C2.4
Formation and Morphology Evolution of Nickel Germaines on Ge (100) under Rapid Thermal Annealing. Xiao Li Lin1,2,3, Ka Yue Lee1, Dong Zhou1, Soo Jin Chun1, Hai Ping Sun1 and Xiaoqin Pan2, Institute of Materials Research & Engineering, Singapore, Singapore; 2Department of Materials Science, University of Michigan, Ann Arbor, Michigan.

Nickel germaines were formed by rapid thermal annealing (RTA) 15 nm Ni film sputtered on Ge (100) at temperatures ranging from room temperature to 700 °C. Phases were identified by XRD and TEM to understand the formation sequence of nickel germaines. Ni-rich phase was first found after RTA at 500 °C whereas NiGe film grew at temperatures above 550 °C where amorphous SiGe is observed in TEM. NiGe2 remained continuous film up to 300 °C, after which isolated particles of germane with exposed underlying substrate were evident. Deepening grooves and prominent grain growth were noticeable as early as 400 °C in our case, indicating the inception of agglomeration. Sheet resistance measurement by four-point probe was also carried out. Sheet resistance as low as 10 Ω/sq. was attained after RTA from 300 to 500 °C, after which the resistance was increased tremendously. The change of sheet resistance with temperature correlated well with the surface morphology of the samples. At early annealing temperatures (below 500 °C), the resistance was governed by the resistivities of the phases present in the film. However, at higher temperatures, the electrical property was no longer controlled by the phases present but by the continuity of the film. In other words, agglomeration of the germaine film resulted in the increased sheet resistance at 600 °C and above.
changes in the gate dielectric will continue, the gate material may change, and strain is being engineered in with material combinations to increase performance. How can process simulators stay ahead? What can be done to calibrate to new materials? We will discuss some of the approaches we are taking to address these issues. I will discuss approaches to better integrate strain in process simulation and strategies to further calibrate all parameters. We have begun to investigate SiGe samples. Illuminated BF$_2$ samples exhibited less net B diffusion and a slightly lower sheet resistance, $R_s$, with respect to non-illuminated samples for the same anneal conditions. As a result, we have begun to investigate SiGe materials and how dopants behave, and will discuss the literature data and what needs to be done to port models to new materials. We will also discuss the role of the surface and possible strategies to calibrate to new gate and capping materials.

2:00 PM C3.2
Athermal, Photonic Effects on Boron Diffusion and Activation During Microwave Thermal Processing, Christopher John Bonfais$^1$, Keith Thompson$^1$, John Bookey$^1$ and Reid Cooper$^1$.

$^1$Electrical & Computer Engineering, University of Wisconsin, Madison, Wisconsin; $^2$Geological Sciences, Brown University, Providence, Rhode Island.

Recent reports indicate that optically driven phenomena affect the diffusion and electrical activation of B during high temperature rapid thermal processing (RTP). Typical defect reactions require 0.5 - 4 eV of energy to proceed. However, thermal energy follows a Boltzmann distribution whose peak is on the order of 0.1 - 0.12 eV at typical spike anneal temperatures (900 - 1100°C). As a result, most defect reactions rely on multiple near-simultaneous phonon collisions or interaction with the very high-energy tail of the thermal energy distribution. Optical photons, on the other hand, possess a large amount of energy, 1 - 4 eV, which can only be transferred to an atom in a discrete manner. The transfer of a large amount of energy from individual high-energy photons may either enhance the already dominant kinetic reactions (causing them to proceed at faster rate), allow new chemical reactions to dominate the reaction pathways, or both. Microwave RTP is ideal for investigating the effects of optical illumination. Commercial RTP systems are primarily lamp-based, and the wafer is flooded with optical photons during the thermal treatment. While this improves the possibility of optical effects, it makes these phenomena difficult to isolate and study. Microwave RTP, on the other hand, rapidly heats the wafer at $\geq$150°C/sec to temperatures in excess of 1000°C without the presence of optical illumination. This paper details work demonstrating the effect of optical illumination on the flux of dopants in ultra-shallow D$_{1}$ layers. Optical illumination has a significant, yet transient, effect on the formation of ultra-shallow junctions in B-doped Si. Rapid thermal annealing was performed in a "dark" microwave furnace in an ambient with an oxygen concentration controlled at 100 ppm. Optically illuminated samples illustrated a greater amount of B diffusion and a lower sheet resistance, $R_s$, with respect to non-illuminated samples for the B-only implanted Si. The reverse was true for BF$_2$ implanted samples. Illuminated BF$_2$ samples exhibited less net B diffusion and lower $R_s$ when compared to non-illuminated samples. These differences tended to lessen as diffusion continued, and little difference in net B diffusion was observed after 10 seconds. This is in contrast to the spike anneal which, when studied in an oxidizing ambient, showed a significant effect of optical illumination on the diffusion of B in the B-only implanted Si samples. However, while optical enhancement in B diffusion in BF$_2$ implanted samples is observed, the total effect is small relative to the spike anneal result. Finally, the optical enhancement for boron diffusion during low temperature (550°C), 30 minute solid phase epitaxy.

2:15 PM C3.3
Simultaneous Phosphorus and Si Self-Diffusion in Extrinsic, Isotopically Controlled Silicon Heterostructures, Hughes H. Silverstein$^1$, Ian D. Sharpe$^1$, Hartmut A. Bracht$^1$, John L. Hansen$^1$, Arne Nylund-Larsen$^1$ and Eugene E. Haller$^2$.

$^1$Materials Science and Engineering, University of California, Berkeley, Berkeley, California; $^2$MateriSys Sciences Division, Lawrence Berkeley National Laboratory, Berkeley, California; $^3$Institut fuer Materialphysik, Universitaet Muenster, Muenster, Germany; $^4$Institute of Physics and Astronomy, University of Aarhus, Aarhus, Denmark.

We present experimental results of impurity and self-diffusion in an isotopically controlled silicon heterostructure extrinsically doped with phosphorus. A large degree of control over the concentration of singly negatively charged native defects is enhanced and the role of these native defect charge states in the simultaneous phosphorus and Si self-diffusion is determined. The concentrations of isotopically controlled $^{29}$Si and natural silicon enable simultaneous analysis of $^{30}$Si self-diffusion into the $^{28}$Si enriched layers and phosphorus diffusion throughout the multilayer structure. An amorphous 200 nm thick Si cap layer was deposited on top of the silicon heterostructure. The phosphorus ions were implanted to a depth such that all the radiation damage resided inside this amorphous cap layer, preventing the generation of excess native defects and enabling the determination of the Si self-diffusion coefficient and the phosphorus diffusivity under equilibrium conditions. These samples were annealed at temperatures between 850 and 1100 °C to study the diffusion. Detailed analysis of the phosphorus profiles on the basis of a modified Kick-Out mechanism and native defect controlled mode of P diffusion. The consistency of our results with previous experiments on B and As diffusion is discussed as well as the mechanisms mediating P diffusion in Si. This work was funded by the U.S. Department of Energy under Contract No. DE-AC03-76SF00098.

2:30 PM C3.4
Room Temperature Migration of Substitutional Boron in Silicon by Kick-Out Mechanism, Enrico Napolitani$^1$, Davide De Salvador$^1$, Alberto Carnera$^1$, Salvo Mirabella$^2$ and Francesco Priolo$^2$.

$^1$INFN and Dipartimento di Fisica, Pavia, Italy; $^2$MATIS - INFN and Dipartimento di Fisica e Astronomia, Catania, Italy.

Despite the extensive scientific efforts over the last decades, the present knowledge on the point defects and dopant diffusion and interaction in Si between themselves and with substrate impurities stand at many important open points, from both an experimental and theoretical point of view. In particular, very few experiments have been reported so far on the behaviour of the above phenomena at the room temperature (RT) regime. Moreover, whether there are some evidences of the RT migration of Si self interstitials (I) and their interaction with impurities, there is, to our knowledge, only one paper in literature [1] in which boron is shown to migrate at RT for long distances, when put in the substrate already in interstitial position by B ion implantation. In this paper we provide an experimental evidence of the long-range migration of substitutional boron in silicon at RT through its interaction with migrating I's, i.e. via the kick-out mechanism. Several silicon samples grown by Molecular Beam Epitaxy with substitutional B deltas were depth profiled by Secondary Ion Mass Spectrometry (SIMS) using O$_2^+$ ions with different beam energies and currents. Some of the samples were analysed both before and after annealing, and the measurements were done at different temperatures, heating or cooling the sample with a liquid nitrogen-thermo resistance temperature controlled stage. We observed that an anomalous redistribution of boron delta occurs during the analysis of c-Si at RT, consisting in long tails on both the trailing and leading edges of the B deltas at concentrations below 1x10$^{18}$/cm$^3$. This redistribution has not been evidenced and discussed before, but it appears to be present in most of the B delta profiles shown in literature so far. We found that the above redistribution is significantly more pronounced after amorphization or by cooling the sample, up to complete suppression, and it has been interpreted as the result of the interaction of substitutional boron with the I's injected in the samples by the sputtering beam. The phenomenon has been simulated and the temperature dependence has been explained by considering at RT the following mechanisms: the I's are produced by the sputtering beam, migrate for long distances, interact with boron by producing mobile B species via the kick-out mechanism, and eventually the mobile B migrate for long distances resulting in the observed tails. As a result of the simulations, we provided the first experimental estimation of the B diffusivity at RT. Our data have a twofold implication. On one hand, they give significant new insight on B diffusion in silicon from 550°C and onwards. On the other hand, they produce evidence of the B point defects at RT and below. On the other hand this phenomenon, if not properly considered, induces an experimental artifact in the determination of the B concentration profile by SIMS and therefore many of the obtained results in literature might be revised. [1] E. J. H. Collart et al., Nucl. Instrum. Methods Phys. Res. B 139, 98 (1998).
without two 25 nm Si$_x$Ge$_{1-x}$C$_y$ layers at depths of 300 and 750 nm. The samples were subsequently annealed in either nitrogen for 30 s or in argon for 25 s. Boron, geranium and boron concentrations before and after annealing are measured by secondary ion mass spectrometry and boron diffusivities were subsequently extracted by fitting the resulting boron profiles using a standard profile simulator. Boron diffusivities between the SiGeC layer after either nitrogen or oxygen anneals are approximately the same, indicating that silicon self-interstitials in the surface region do not pass through the intervening SiGeC layer. The boron diffusivity in the SiGeC layer is further similar or greater than that observed in the sample without the SiGeC layers. The boron diffusivities between the SiGeC layers, therefore, show no depletion of the self-interstitial concentration in the silicon spacer despite annealing conditions believed to total numbers of self-interstitials from the SiGeC layer being much larger. This result is consistent with the overall characteristics of the defects observed in the sample after nitrogen anneal. Boron diffusivities in the SiGeC layer are thus attributed to a silicon self-interstitial recycling process in which self-interstitials consumed in the SiGeC layer are effectively transported back to the spacer layer as mobile interstitial carbon and are subsequently released in the spacer layer by the reverse “kick-out” reaction.

3:30 PM C3.6 Current Understanding and Modeling of D Diffusion and Activation Anomalies in Preamorphized Ultra-Shallow Junctions. Benjamin Colombeau, Andy Smith, Nicholas E.B. Cowern, Fuccio Cristiano, Alain Claverie, Ray Duffy, Bartek J. Prawlocki, Philippe J. Ortiz, Peter Peicher, Evelynne Lampion, and Christoph Zechner; 1Advanced Technology Institute, University of Surrey, Guildford, United Kingdom; 2Ion implantation group, CEMES/LAAS-CNRS, Toulouse, France; 3Philips Research Leuven, Leuven, Belgium; 4Hoefer IHS, Erben, Germany; 5IEMN/ISEN, UMR CNRS, Villeneuve d’Ascq, France; 6ISE Integrated System Engineering AG, Zurich, Switzerland.

The formation of ultra-shallow junctions (USJs) for future integrated circuit technologies requires preamorphization and high dose boron doping to achieve high activation levels and abrupt profiles. To achieve the challenging targets set out in the semiconductor roadmap, it is crucial to reach a much better understanding of the basic physical processes taking place during USJ processing. In this paper we review current understanding of dopant-defect interactions during thermal processing of device structures - interactions which are at the heart of the dopant diffusion and activation anomalies seen in USJs. First, we recall the formation and thermal evolution of End of Range (EOR) defects upon annealing of preamorphized implants (PAI). It is shown that various types of extended defect can be formed: clusters, (113) defects and dislocation loops. During annealing, these defects exchange Si interstitial atoms and evolve following an Ostwald ripening mechanism. We review progress in developing models based on these concepts, which can accurately predict EOR defect evolution and interactions between different defects. Based on this physically based defect modelling approach, combined with fully coupled multi-scale modelling of dopant diffusion, one can perform highly predictive simulations of boron diffusion and dopant-defect interactions. These results suggest that the overall characteristics of the defects and the way they evolve, i.e. variation of the onset of dissolution and dissolution time with annealing temperature, were found to be roughly the same as those found by Englezos, our results show dose and temperature to not so far in the original experiment. Whatever the temperature, during a first period of time, the (113) defects grow in size while their density decreases. In the meantime, the population losses a small amount of the Si interstitial atoms it contains. This quasi-conservative growth is followed by a period of dissolution. Furthermore, the overall characteristics of the defects contained in the defects, the so-called dissolution regime. Atomic simulations of the Ostwald ripening of Si precipitates in presence of an external sink have been run. In the model, it is assumed that a majority of defects is dissolved in the Si matrix. The dissolution energy (per atom) of the (113) defects decreases when their size increases. These simulations perfectly fit the experimentally observed evolution of the size-distributions, densities and number of trapped interstitials for all temperatures. This work unambiguously shows that the mechanism driving the thermal evolution of (113) defects is an Ostwald ripening one and that the driving force for such an evolution is the decrease of the formation energy of the defects. When the probability for a Si atom emitted by a defect to be trapped by the surface becomes of the same order than that to be trapped by another defect, the population starts to loose atoms with a high rate, its density decreases and dissolution increases further. This catastrophic coupling between the defect population and the surface is at the origin of the so-called defect dissolution. The thermal evolution of (113) defects in the vicinity of a radiating surface shows the dynamic transition to a quasi-conservative to a non-conservative Ostwald ripening. In general, such a behavior cannot be described by a simple exponential law.

4:15 PM C3.8 Doping and Mobility Profiles in Defect-Engineered Ultrashallow Junctions. Andy James Smith, Benjamin Colombeau, Russell Gwilliam, Erik Collart, Nicholas Cowern, and Brian Scaly; 1Advanced Technology Institute, Surrey University, Surbiton, GU2 7XH, United Kingdom; 2Applied Materials, Horsham, United Kingdom.

Silicon on Insulator (SOI) is a promising substrate material for future generations of CMOS devices with inherent advantages over bulk silicon. Performing non-amorphizing MeV implants into SOI material has been shown to produce a vacancy rich region near the surface, separated from the deeper interstitial rich region by the buried oxide (BOX). We have already shown that this placement of excess vacancies in the region of a shallow boron implant in SOI material can significantly retard the transient enhanced diffusion (TED) of the boron atoms. The present paper now considers the impact of vacancy engineering on the corresponding electrical activation and mobility. In order to understand how control of the vacancy concentration distribution influences the electrically active boron concentration and the hole mobility as a function of depth, SOI wafers were implanted with 1 MeV silicon ions with dose of $10^{15}$ cm$^{-2}$ and then implanted at 40 keV with a dose of $6\times10^{13}$ cm$^{-2}$ and annealed under N2 at 650°C, 700°C, 740°C and 815°C. Weak beam dark field imaging under appropriate conditions has been used to follow the evolution of the size-distributions and densities of the population of defects during annealing. To perform such a rigorous statistical analysis more than 300 defects were analyzed at each step and their variants were identified. While the temperature, during a first period of time, the (113) defects grow in size while their density decreases. In the meantime, the population loses a small amount of the Si interstitial atoms it contains. This quasi-conservative growth is followed by a period of dissolution. Furthermore, the overall characteristics of the defects contained in the defects, the so-called dissolution regime. Atomic simulations of the Ostwald ripening of Si precipitates in presence of an external sink have been run. In the model, it is assumed that a majority of defects is dissolved in the Si matrix. The dissolution energy (per atom) of the (113) defects decreases when their size increases. These simulations perfectly fit the experimentally observed evolution of the size-distributions, densities and number of trapped interstitials for all temperatures. This work unambiguously shows that the mechanism driving the thermal evolution of (113) defects is an Ostwald ripening one and that the driving force for such an evolution is the decrease of the formation energy of the defects. When the probability for a Si atom emitted by a defect to be trapped by the surface becomes of the same order than that to be trapped by another defect, the population starts to loose atoms with a high rate, its density decreases and dissolution increases further. This catastrophic coupling between the defect population and the surface is at the origin of the so-called defect dissolution. The thermal evolution of (113) defects in the vicinity of a radiating surface shows the dynamic transition to a quasi-conservative to a non-conservative Ostwald ripening.
of nitrogen. Lattice atoms are given just enough energy to leave their lattice sites, and then prevented from recombining by the formation of an N-V complex. The lattice is pumped by further electron collisions, diffuse away from the e-beam irradiated zone; then the nitrogen related complexes either accumulate vacancies to produce voids, or oxygen atoms to initiate SiO₂ nucleation. The benefit of this nanoscale TED is that normally high-temperature extended defect nucleation processes are observed at room temperature in an area of the TEM operator's choosing. In addition, the interaction of beam electrons with light-element impurities, doping diffusion and nitride-implanted samples by the point defect enhancement and beam stimulation. In the absence of nitrogen, light elements such as boron can be driven to diffuse by electron irradiation [100] oriented N-doped FZ plan-view samples were prepared by conventional TEM thinning methods, including grinding, polishing, dimple grinding and ion milling. A Si sample implanted with $5 \times 10^{15}$ cm$^{-2}$ of 35 keV B$^+$ and 300 keV Sb$^+$ was prepared for TEM analysis by cross-sectional cleaving. The irradiation was performed at 200 keV in JEOL 2010F and Topcon 902B electron microscopes, while high-resolution imaging, Electron Energy Loss Spectroscopy (EELS), and scanning TEM (STEM) were performed on the JEOL instrument. Results will be presented where the experimental EELS spectra for vacancy and self-interstitial rich regions are compared with simulations results. EELS spectra of point defects and their clusters are calculated based on the density of states, obtained using the ZBL approximation applied with density functional theory. The results allow the consistent identification of vacancies, self-interstitials and aggregates thereof. Secondly, the application of the electron irradiation technique to the Sb and B co-implanted samples will be presented with Z contrast, EELS and scanning TEM. A monolayer of an interstitial aggregate is determined and shown to form during the irradiation. The boron-doped delta Si structures used in this work were grown at 800 degC and 20 Torr in an industrial Reduced Pressure Chemical Vapour Deposition system, using SiH₂Cl₂/HCl chemistry. The interstitials resulting in reduced TED. However, this is just a hypothesis without any experimental evidence. The exact role of fluorine on TED is still unclear and controversial. In this article, we have previously reported that F reduced boron diffusion. This hypothesis is supported by the results of this study. The effect of fluorine on boron diffusion is investigated by mean of SIMS depth profiling of the Sb and B-doped layers. However, only a slight diffusion is observed from the top B-doped layer, indicating a possible full mono-germanosilicide formation at 300°C as reported for pure Ge at 400°C and formed alkali metal rich samples did not react with Si at 500°C. Surface composition analysis by XPS showed pure Ni surface on Se-passivated samples annealed at 400°C and 500°C, but silicide surface on bare samples annealed at the same temperatures. Hence, Se passivation suppresses the formation of Ni silicide on the Si(001) surface by over 100°C as compared to the bare Si(001) surface. These results may have important implications in source/drain engineering in sub-100 nm Si CMOS devices.

C4.4 Study of Ni(Pt) germanosilicides formation on Fully-strained Si$_{1-x}$Ge$_x$ and Si$_{0.5}$Ge$_{0.5}$Co$_{1-x}$ by Raman spectroscopy. Jilun Yang, Pengy Pei$^1$, Aomar Halimaoui$^1$, Jean Michel Hartmann$^2$, Cyrille Laviron$^3$, Rebha El Farhane$^2$, Frederic Laugier$^3$

Nitride implantation has been demonstrated. In this work, Raman spectroscopy was used to study the formation of Ni(Si) germanosilicide on Si$_{1-x}$Ge$_x$ and Si$_{0.5}$Ge$_{0.5}$Co$_{1-x}$ substrates and it was shown that both Ge and Sb$_2$Ge$_3$ have previously been demonstrated. In this work, Raman spectroscopy was used to study the reaction of pure Ni and Ni(Pt) at 300°C to fully-strained Si$_{1-x}$Ge$_x$ and Si$_{0.5}$Ge$_{0.5}$Co$_{1-x}$ grown on Si(100) wafer and annealed by rapid thermal annealing (RTA). In addition, four point probe and X-ray diffraction (XRD) techniques were used to determine the sheet resistance and phase of the Ni(alloy) germanosilicides, respectively. With pure Ni, it was found that the incorporation of 0.1% C in the substrate resulted in out-diffusion of Ge from the germanosilicide film at 600°C, compared to 700°C for pure Ni on Si$_{0.5}$Ge$_{0.5}$. This Ge out-diffusion phenomenon is evident by the gradual shift in the NiS$_{1-x}$Ge$_x$ (w < x) Raman peak from 213 cm$^{-1}$ to higher wavenumbers, closer to 217 cm$^{-1}$ reported for pure Ni/Si, an indication that Ge is being depleted from the film with increasing RTA temperatures. Hence, by monitoring this Raman shift, Ge out-diffusion from the film can be studied. In addition, it was found that severe agglomeration of the germanosilicide film occurred at high RTA temperature for the Ni/Si$_{0.5}$Ge$_{0.5}$ system. From the Raman spectra, a sharp increase in the Si substrate peak at 520 cm$^{-1}$ was observed, coupled with the appearance of the Si-flip peak of Si at 301 cm$^{-1}$. When Pt was introduced into the Ni film, significant improvements in the germanosilicide film morphology was observed on both the Si$_{1-x}$Ge$_x$ and Si$_{0.5}$Ge$_{0.5}$Co$_{1-x}$ substrates and it was shown that both Ge out-diffusion and agglomeration were delayed up to 800°C, a 50 to 100°C improvement as compared to that with a pure Ni film. Finally, it was also shown that the addition of Pt enhanced the formation of the low resistivity mono-germanosilicide phase at temperatures as low as 300°C. The Raman peak intensity of Ni(Pt) germanosilicide at 300°C was almost identical to those obtained at 400 and 500°C, indicating a possible full-germanosilicide formation at 300°C as compared to the mixed (Ni$_2$SiGe and NiSiGe) phase obtained with pure Ni. The results show that addition of Pt is useful in improving the morphological stability of the germanosilicide film on fully-strained Si$_{1-x}$Ge$_x$ and Si$_{0.5}$Ge$_{0.5}$Co$_{1-x}$, but also in lowering the formation temperature for the complete transformation of the mono-germanosilicide phase.

C4.5 Study of Nickel (Platinum) (Pt at.% = 0, 5, 10) Germanosilicide Formation Using Micro-Raman Spectroscopy. Lijun Jin$^1$, Kin Leong Pey$^{1,2}$, Wee Kiong Choi$^3$, Eugene A Fitzgerald$^{1,4}$, Dimitri A Antonidis$^{1,4}$ and Dongshi Chi$^5$

$^1$Singapore-MIT alliance, National University of Singapore, Singapore; $^2$Electrical & Electronic Engineering, National Technological University, Singapore, Singapore; $^3$Electrical & Computer Engineering, National University of Singapore, Singapore; $^4$Massachusetts Institute of Technology, Cambridge, Massachusetts; $^5$Institute of Materials Science and Engineering,
The interfacial reaction between 10 nm Ni(Pt) (Pt at % = 5, 10) and (100) Si$_{0.75}$Ge$_{0.25}$ substrate after rapid thermal annealing (RTA) between 400 and 900°C has been studied in detail using Micro-Raman spectroscopy. The results show that Ni or Ni(Pt) mono-germanosilicide exists. For the Ni/PtSi$_2$ system, a peak at around 200 cm$^{-1}$ was clearly observed for the samples annealed 400 and 500°C, and two sharp and distinct peaks at 193 and 212 cm$^{-1}$ were found at annealing temperatures higher than 600°C. These peaks are similar to the reported results for the NiSi peak. The decrease in the Ge concentration (i.e. Ge out-diffusion) in the NiSiGe$_2$ films with increasing annealing temperatures could be the mechanism responsible for the evolution of the broad peak into two distinct Raman peaks. The two distinct peaks correspond to the NiSi$_{1.9-2.4}$Ge$_{3.1}$ phase with $< y < 0.25$. These results are in agreement with our previous Auger mapping and TEM results. In addition, the decrease in the Ge concentration in the NiSiGe$_2$ phase with increasing temperature was supported by a corresponding shift in the NiSi(Ge) peak towards a higher wavenumber in the Raman spectra, and a similar shift of the germanosilicide peaks towards a higher 2# value in x-ray diffraction (XRD) spectra. For the Ni(Si$_{0.75}$Ge$_{0.25}$) peak, it was still observable at 600°C (i.e. 100°C higher than that of the pure NiSiGe$_2$). The broad peaks evolved into one distinct peak at 210 cm$^{-1}$ at an annealing temperature higher than 700°C. The peak at 190 cm$^{-1}$ was not apparent. For the Ni(Pt)/SiGe$_2$ system, the results were similar to that of the Ni/Si$_{0.75}$Ge$_{0.25}$ system but with less Ge-out-diffusion at higher temperature. In the Ni(Pt)/SiGe$_2$ system, the evolution of a broad peak into distinct Raman peaks (i.e., increasing temperatures) shows the formation of the NiSiGe$_2$ cone concentration in the NiSi(4Ge) phase increases at higher annealing temperatures. The latter effect plays a critical role in suppressing Ge-out-diffusion from the germanosilicide grains. And more Ge atoms are consumed in the NiSiGe$_2$ grains with higher amount of Pt added into the Ni(Pt) alloy.

C4.4 Ni Silicide Morphology on Small Features, Oxana Chamirian,1,2 Anne Lauwers2, Jorge A. Kittl3, Mark Van Dal4, Muriel de Potter4, Christa Vrancken3, Caroline Demuynck4, Richard Lindsay2 and Karen Maex1,2 1Electrical Engineering, University of Ghent, Belgium; 2IMEC, Leuven, Belgium; 3Institute of Physical Chemistry, University of Ghent, Belgium; 4Affiliated researcher at IMEC from Texas Instruments, Leuven, Belgium; 5Philips Research Leuven, Leuven, Belgium

With continuous scaling down of device dimensions, issues in the silicide placement process using CoSi$_2$ result in the need for alternative materials. NiSi$_2$ offers the advantages of low resistivity on narrow lines and low silicidation temperatures. However, implementation of NiSi$_2$ faces difficulties such as excessive silicidation on narrow lines, low thermal stability and NiSi$_2$ formation at room temperature. In this work Ni silicide formation on narrow areas is studied in terms of the resulting silicide thickness and morphology, sheet resistance of narrow lines, and diode leakage. The presence of NiSi$_2$ pyramids on the epitaxial NiSi$_2$ film depletes the Ge concentration in the NiSiGe$_2$ grain, with the onset temperature for the formation of NiSi$_2$ pyramids in the range 400-700°C. The peak at 210 cm$^{-1}$ was still observable at 600°C (i.e. 100°C higher than that of the pure NiSiGe$_2$). The broad peaks evolved into one distinct peak at 210 cm$^{-1}$ at an annealing temperature higher than 700°C. The peak at 190 cm$^{-1}$ was not apparent. For the Ni(Pt)/SiGe$_2$ system, the results were similar to that of the Ni/Si$_{0.75}$Ge$_{0.25}$ system but with less Ge-out-diffusion at higher temperature. In the Ni(Pt)/SiGe$_2$ system, the evolution of a broad peak into distinct Raman peaks (i.e., increasing temperatures) shows the formation of the NiSiGe$_2$ cone concentration in the NiSi(4Ge) phase increases at higher annealing temperatures. The latter effect plays a critical role in suppressing Ge-out-diffusion from the germanosilicide grains. And more Ge atoms are consumed in the NiSiGe$_2$ grains with higher amount of Pt added into the Ni(Pt) alloy.


CMOS technology is rapidly closing on the 45 nm node, pushing gate lengths to 25 nm and junction depths to 70 nm. Since scaling alone does not provide the improvements set by the ITRS Roadmap, the production of such small devices demands the integration of new materials with superior properties. For instance, NiSi is replacing CoSi$_2$ (industry choice for previous nodes) due to the instability of CoSi$_2$ on narrow poly gates [1]. One of the key issues for Ni silicidation is its low thermal stability. It is well documented that thermal degradation of NiSi films can be reduced by adding an alloying element to Ni such as Ta [2], Pd [3] or Pt [4]. However, it is important to understand the impact of alloying on other silicide properties such as the improvement of sheet resistance. The two distinct effects of NiSi alloying should be separated: alloying Ni with Ta leads to the formation of NiSi$_2$ pyramids and the impact of device geometry and processing on the formation of NiSi$_2$ pyramids. Additionally, alloying NiSi$_2$ with Ta can affect the diffusivity of Ni inside the Si substrate. The solid state reaction of Ni on strained (001) Si$_{0.8}$Ge$_{0.2}$ was studied using various characterization tools, with a particular emphasis on the influence of Ge-rich Si$_{1-x}$Ge$_x$ segregation on the morphological stability of NiSi$_{1-x}$Ge$_x$ films. XRD results showed that only mono-germanosilicide, i.e. NiSi$_{1-x}$Ge$_x$, was formed within the temperature range 400-800°C. Micro-Raman was used to study the Ge-rich Si$_{1-x}$Ge$_x$ segregation by monitoring the emergence of 493 cm$^{-1}$ Si-Si vibration signal from the segregated Ge-rich Si$_{1-x}$Ge$_x$ regions [1]. Micro-Raman results revealed that the temperature for Ge-rich Si$_{1-x}$Ge$_x$ segregation is critically dependent on the annealing time: 550°C for 1s annealing and 450°C for 180s annealing. XTEM images show that the segregation takes place preferentially at the germanosilicide/Si$_{1-x}$Ge$_x$ interface, more specifically at the triple junctions between two adjacent NiSi$_{1-x}$Ge$_x$ grains and the underlying epi Si$_{1-x}$Ge$_x$. It is accompanied with thermal grooving. With prolonged annealing, the segregation process continued to proceed, and the segregated Ge-rich Si$_{1-x}$Ge$_x$ regions tend to grow up into the surface until complete breaking-up of the NiSi$_{1-x}$Ge$_x$ film. It is believed that the segregation process is thermally driven, controlled by the mobility of NiSi$_{1-x}$Ge$_x$ grain boundaries at the interface. This conclusion is based on the detailed analysis of XTEM images and comparison of SEM images of just agglomerated NiSi$_{1-x}$Ge$_x$ films with those of Ni$_x$Si$_{1-x}$Ge$_x$ films formed on (001)Si and (001)Ge, respectively, and also just agglomerated. The observation of much smaller grains (0.1-0.2 μm) in just agglomerated NiSi$_{1-x}$Ge$_x$ films, as compared to...
growth of epitaxially thin CoSi2 layer using Co-N films as a cobalt source. Sunil Kim, SeungRyul Lee and ByungTae Ahn; Korea Advanced Institute of Science and Technology, Daejeon, South Korea.

Epitaxial layers of CoSi2 grown on (100) Si substrate are of special interest because of their uniform and flat CoSi2/Si interfaces, excellent thermal stability, low junction leakage, and ultra-shallow junction formation. For commercial application of CoSi2 in nanoscale ICs, it is necessary to grow the epitaxial CoSi2 layer as thin as possible, to obtain shallow junction with low leakage current. We developed a new method of forming a uniform epitaxial CoSi2 layer with the thickness of less than 5nm, for the first time, using Co-N film as a cobalt source. The Co-N film for epitaxial CoSi2 layer was deposited either by reactive sputtering or by metallorganic chemical vapor deposition from cobalt carbonyl source (Co2(CO)8) using NH3 gas at 350 - 450°C. The reactive sputtering was done using cobalt target in Ar and N2 ambient at room temperature. Thin amorphous layer and silicide layer were observed between Co-N film and Si (100) substrate by cross-sectional TEM. Ti capping layer was deposited by reactive sputtering to suppress the concentration of cobalt due to amorphous layer as a cobalt source. The Co-N film for epitaxial CoSi2 layer was deposited on Si (100) substrates by reactive sputtering of Co-N target in Ar gas at 350 - 450°C. After annealing and unreacted metal etching, epitaxial thin and uniform CoSi2 layer with 4-5nm thickness was formed. It was demonstrated that this process was done by suppressing the concentration of cobalt due to amorphous layer between Co-N and Si interfaces during annealing.

Introduction

The fabrication of silicon-on-insulator (SOI) has been an important area of research in the field of microelectronics. SOI technology offers several advantages over traditional bulk silicon technology, including reduced parasitic capacitance, improved reliability, and a higher degree of integration. Among the various SOI technologies, the bulk silicon-on-insulator (SOI) process is one of the most promising due to its high potential for high-performance applications. However, the realization of high-quality SOI layers requires precise control of the growth and processing steps to achieve the desired material properties.

In this section, we will discuss the growth and processing of high-quality SOI layers using atomic layer deposition (ALD) as a key technology. First, we will review the basic principles of SOI and the importance of high-quality SOI layers. Then, we will present an overview of the ALD process and its potential advantages for SOI growth. Finally, we will discuss the application of ALD for the fabrication of high-quality SOI layers and highlight some of the recent developments in this field.

SOI Technology

Silicon-on-insulator (SOI) technology is a fundamental building block for modern microelectronics. The basic idea of SOI is to replace the bulk silicon substrate with a thin, high-quality silicon layer on top of an electrically insulating substrate. This provides several benefits, including reduced parasitic capacitance, improved reliability, and a higher degree of integration. In addition, SOI technology can be used to create vertical integration of transistors, which is crucial for the development of high-performance microprocessors.

There are two main types of SOI technology: bulk SOI and thin-film SOI. Bulk SOI involves the growth of a thin silicon layer on a bulk silicon substrate, followed by the removal of the bulk silicon using chemical etching or thermal oxidation. Thin-film SOI, on the other hand, involves the deposition of a thin silicon layer on a high-resistivity silicon substrate, followed by the removal of the high-resistivity substrate using wet etching or dry etching. The quality of SOI layers is critical for the performance of microelectronic devices. Therefore, it is important to develop techniques for the growth and processing of high-quality SOI layers.

Atomic Layer Deposition (ALD)

Atomic layer deposition (ALD) is a versatile and precise thin-film deposition technique that allows for the growth of high-quality, conformal, and uniform layers. ALD is based on the repetitive deposition of a thin film at each step, followed by the removal of excess material using a plasma etch or a chemical etch. This process is repeated until the desired film thickness is achieved. The key advantage of ALD is its high deposition rate, which is achieved through the use of sequential self-limiting reactions. This allows for the precise control of the film thickness, which is essential for the fabrication of high-performance microelectronic devices.

ALD has been used for the fabrication of high-quality SOI layers due to its ability to deposit thin films with high precision and uniformity. ALD has been demonstrated for the growth of high-quality silicon layers on a variety of substrates, including silicon substrates, gallium arsenide substrates, and silicon-on-insulator substrates. In addition, ALD has been used for the deposition of other materials, such as aluminum, silicon dioxide, and silicon nitride, which are important for the fabrication of microelectronic devices.

Recent Developments

In recent years, there has been significant progress in the development of SOI technology using ALD. One of the key developments is the use of ALD for the fabrication of high-quality silicon-on-insulator layers on silicon-on-insulator substrates. This has been achieved through the development of novel ALD processes and the optimization of process parameters. In addition, there has been significant progress in the development of ALD processes for the fabrication of other materials, such as silicon nitride, silicon oxide, and aluminum, which are important for the fabrication of microelectronic devices.

In conclusion, the growth and processing of high-quality SOI layers is a crucial aspect of modern microelectronics. Atomic layer deposition (ALD) is a versatile and precise thin-film deposition technique that allows for the growth of high-quality, conformal, and uniform layers. ALD has been demonstrated for the growth of high-quality silicon layers on a variety of substrates, including silicon substrates, gallium arsenide substrates, and silicon-on-insulator substrates. In addition, ALD has been used for the deposition of other materials, such as aluminum, silicon dioxide, and silicon nitride, which are important for the fabrication of microelectronic devices. In recent years, there has been significant progress in the development of SOI technology using ALD. This has been achieved through the development of novel ALD processes and the optimization of process parameters. In addition, there has been significant progress in the development of ALD processes for the fabrication of other materials, which are important for the fabrication of microelectronic devices.
two pulse duration regimes were studied by Secondary Ion Mass Spectrometry (SIMS) and their electrical activation was deduced both from classical techniques (sheet resistance and Hall effect) and from non-contact infrared spectroscopic ellipsometry (Drude model).

Finally, both n+ and p+:fn ultra shallow junctions (<50 nm in depth) were prepared in optimized laser processing conditions and their electrical properties were discussed in the framework of the future technological requirement.

C4.14
Low Resistive Contacts to Laser Annealed Junctions.

Hun-Ha Kim, Peter B. Griffin and James D. Plummer; Center for Integrated Systems, Stanford University, Stanford, California.

As MOS devices scale down to smaller dimensions, contact resistance will dominate the overall series resistance associated with current flow from source to drain. Contact resistivities below 10⁻¹²Ω·cm² are required for sub-100nm node devices, which represents the lowest contact resistance that can be obtained with a maximum electrically active doping level of 2×10²⁰ cm⁻³ and normal barrier heights associated with metal-silicon contacts. We have employed a laser annealing technique in order to further increase the active concentration beyond the solubility limit and investigated how these super-saturated doping levels can help reduce contact resistance. In this work, junctions were created by either laser annealing or conventional RTP, then the silicon layer was reacted with titanium or nickel to form silicide contacts at varying silicidation temperatures (400-800°C). Contact resistance measurements were performed and the corresponding specific contact resistivity was extracted based on transmission electron microscopy (TEM) images. An increase of the contact resistance was observed at higher silicidation temperatures, due to the deactivation of super-saturated doping created by laser annealing. A particularly low contact resistance can be obtained by minimizing the thermal budget for silicidation. Nickel silicide forms at lower temperature and thus we have found that nickel silicide contacts show better compatibility with the laser annealing process than titanium silicide.

C4.15

Julien Venturini, Miguel Hernandez and Cyril Laviron; 1 Laser Division, SOPRA, BOIS-COLOMBES, France; 2 DTI, CEA-DRT - LETI, Grenoble, France.

Long Pulse Excimer Laser Annealing (LP-ELA), is considered so far to properly activate Ultra Shallow Junction (USJ) for next CMOS technology nodes beyond 65 nm as defined by the International Technology Roadmap for Semiconductors. Particularly, the specific thermodynamic cycle induced in silicon by a long laser pulse leads to interesting behaviour in both the solid phase and molten phase. According to the chosen process, one wants to reach high activation rate (solid phase) or reduced damage of the poly-Si gates (molten phase). In order to optimize the coupling of the laser in the source and drain regions of the activated device, the solid phase activation while avoiding thermal modification of the poly-Si gates, we study here the influence of a layer stack (including both anti-reflective and reflective coatings) deposited on a Ge pre-amorphized BF² implanted Si wafers. The process of activation of the USJ by a long pulse excimer laser (XeCl, 0.308 nm, 200 ns) is studied as a function of the nature and the thickness of the deposited layer. Both molten phase and solid phase regime are evaluated. We rely here on four-point probe resistivity measurements, secondary ion mass spectroscopy (SIMS) depth profiles and Infra-Red Spectroscopic Ellipsometry (IRSE). Melting threshold and efficiency of the activation of the USJ are reported for the different layer stacks, defining new laser process windows. This process window and related integrity of the poly-Si gates is also discussed.

C4.16
Advanced Thermal Processing of Semiconducting Materials Using Flash Lamp Annealing.

Wolfgang Skorupa, Dieter Panknin, Matthias Voelskow, Wolfgang Anwand, Thoralf Gebel and Rossen A Yankov; 1 FWHM, Forschungszentrum Rossendorf e.V., Dresden, Germany; 2 nanospec GmbH, Dresden, Germany.

The successful use of energy pulses from flash lamps for the advanced thermal processing of semiconducting materials will be reported at two examples: (i) For ultra-shallow junction formation in silicon Flash Lamp Processing (FLP) has become methodologies to meet the requirements for the next technology nodes defined by the ITRS roadmap. Low energy boron implants have been heat-treated in this way using peak temperatures in the range of 1100°C to 1300°C and effective peak times of 20 μs and below. Secondary ion mass spectrometry and four point probe measurements have been undertaken to determine the junction depth and the sheet resistance, respectively. Optimum processing conditions using a pulse time of 3 μs have been identified, under which one can obtain combinations of junction depth and sheet resistance values that meet the 90 nm and even the 70 nm technology node requirements. (ii) Another challenging task is related to the production of Si-C layers to make the substrates to overcome for selected applications the need in high cost bulk SiC wafers. Using FLASIC (Flash Lamp Supported Deposition of SiC-SiC) a remarkable improvement in the quality of such cubic phase SiC layers was demonstrated achieving a nano-scale liquid phase epitaxy process at the interface SiC/Si.

C4.17
Flash Lamp Annealing for 65 nm Node : Finding a Common Anneal Condition for All the Implants.

François Wacquant, Rehbo El Farhane, Jeff Gelpey and Steve McCoy; 1 STMicroelectronics, Crolles, France; 2 Philips, Crolles, France; 3 Vortek Industries Ltd., Vancouver, British Columbia, Canada.

Flash lamp annealing has proven over the recent years to be a very promising technique for ultra shallow junction formation. With this anneal, the wafer is exposed to a short pulse (in the milliseconds range) of intense light. This allows to reach very high temperatures which improves dopant solubility and therefore activation, with minimal diffusion. However, some questions remain on the possibilities to integrate this new anneal on real devices. Indeed, the same unique anneal has to give the right activation level for all different kind of implants such as ldd, source/drain, pockets, gate etc... In this paper, we discuss results obtained on the so-called Flash-assist RTP (FATP) anneal. We show that it is depending on the spike anneal temperature and on the implant dose. Source/drain implants were also annealed with this technique and proved to be correctly activated. Finally, gate activation has been simulated on full sheet wafer. We show that it is related to the device integration scheme, to obtain the right dopant profile and activation. Thus the same FATP anneal might be able to fulfill all requirements for all 65nm node implants.

C4.18
P-Type Junction Engineering for 65 nm Node : Use of BF² Implant Defects to Improve Activation With Minimal Damage.

François Wacquant, Rehbo El Farhane and Frederic Salvetat; 1 Metal R&D, STMicroelectronics, Crolles, France; 2 Philips, Crolles, France.

In this paper the formation of P type junction has been extensively studied with the use of a design (D) of experiment (DOE) on process effects of implant parameters. It was found, that a complex interaction of device activation was performed by BF² implant followed by spike anneal, in a wide range of dose (2e14 at.cm⁻² to 2e15 at.cm⁻²), energy (from 0.5 keV to 4 keV) and temperature (100°C to 1100°C). Sheet resistance (Rs) and junction depth (Xj) are modelled by a polynomial of 2nd order depending on these 3 parameters. This simple model appears to be very efficient to predict the main junction characteristics over the entire studied domain. In particular, we show that the junction activation is not only depending on the spike anneal temperature but also on the implant condition. This suggests that the change of defects distribution due to various implant doses and energies plays a significant role on the activation mechanism of B. This gives therefore a new degree of freedom to improve junction activation without enhancing diffusion. Indeed in the last years, main focus to improve sheet resistance for given junction depth was to use sharper and sharper spike anneals that allowed to go to higher temperature. On the contrary, we show here that careful dose and energy choice allow to reach the ITRS 65 nm node specification with low temperature spike anneal.

C4.19
Defect evolution along trench edges in oxide patterned silicon wafers.

Nina Burdick and Kevin S Jones; University of Florida, Gainesville, Florida.

Pattern induced defects during advanced CMOS processing can lead to lower quality devices with high leakage currents. Within this study, the effects of oxide trenches on implant related defect formation and evolution in Si patterned wafers is examined. Oxide filled trenches approximately 4000 A deep were patterned into 300 nm <100> silicon wafers. Patternning was followed by the ion implantation of Si at energies ranging from 10 to 80 keV. Samples were amorphized with doses of 1×10¹⁵ atoms/cm², 5×10¹⁵ atoms/cm², and 1×10¹⁶ atoms/cm². Two independent repeating structures were studied. The first structure is comprised of silicon oxide filled trench lines, 3.2 μm wide spaced 12.5 μm apart, while the second structure contains silicon squares, 0.6 μm on a side, surrounded by a silicon oxide filled trench. Cross-sectional and plan-view TEM samples were used to examine the defect morphology after annealing at temperatures ranging from 600°C to 950°C for various times between 1 second and 4 hours. An array of defects was observed to form near the surface at the silicon/silicon oxide interface. These trench edge defects are not related to recrystallization of the amorphous layer. They appear to coarsen with both increasing annealing time and temperature. The
width of the defect layer as seen in plan-view images with increasing implant energy. It is believed that these defects arise from condensation of dopants at the Si/SiO2 interface and strain appears to play a role. Possible sources of these point defects will be discussed.

SESSION C5: Ultra-Shallow Junction Formation Engineering

Chairs: Alain Clavie`re, Richard Lindsay
Wednesday Morning, April 14, 2004
Room 2002 (Moscone West)

8:30 AM C5.1 Optimized Doping and Annealing for Ultra-Shallow Junctions for 65nm and Beyond. Jeffrey Gelpey1,2, Daniel Downey2, Steve McCoy3 and Edwin Arevalo2; 1Vortek, Boston, Massachusetts; 2Varian Semiconductor Equipment Associates, Gloucester, Massachusetts; 3Vortek Industries, Vancouver, British Columbia, Canada.

To meet the requirements of smaller devices while still maintaining high performance, it is necessary to form very shallow source/drain extensions with very high activation. Although significant progress has been made in meeting these requirements as outlined in the ITRS, continued progress in meeting the needs for the 65nm technology generation and beyond remain a challenge. It will no longer be sufficient to consider the doping (ion implantation) and activation (annealing) steps independently. Both must be optimized together as a process sequence. Improvements have been made on the doping side in both traditional beamline implantation and advanced processes such as plasma doping. Advanced activation methods such as improved spike RTP anneals, solid phase epitaxial growth (SPER) and millisecond annealing during other flashlamps or sub-millisecond processing have been investigated and all have shown promise. This paper will survey the requirements for USJ doping and activation for the 65nm node and beyond and discuss some of the recent results in both doping and activation. Some comparisons of the annealing of shallow PLAD-doped silicon wafers using various advanced activation techniques will be presented and some discussion of the ultimate limits on “conventional” doping and activation schemes will be proposed.

9:00 AM C5.2 Evaluation of flash annealing technique for the formation of Ultra Shallow Junctions. Reubab El Fasihane1, Wouo Sik Yoo2 and Aomar Halimaoui2; 1Crolles 2, Philips semiconductors, Crolles, France; 2Crolles 2. Philips Semiconductors, Crolles, France.

The formation of Ultra Shallow Junction (USJ) is becoming a challenging task in the fabrication high-performance CMOS devices. The standard process that is a spike anneal, using Lamp-based system, is reaching its limit in the formation of USJ for 65 nm-node and beyond. Recent published data have shown that Flash annealing is a promising technique. It has been demonstrated that this technique can be used to anneal Si-doped wafers. The annealing is done both on B+ (500 eV, 1015 cm-2) and BF2+ (2200 eV, 1015 cm-2) implanted wafers. All wafers were analyzed with four point resistance as measured by 4-pt. probe and junction depth as measured by SIMS. It has been demonstrated that flash annealing results in higher spike anneal temperatures (above 850°C) due to the amorphization process occurring during the BF2 + implantation. In this low temperature regime, Boron clustering takes place very rapidly in B+ implanted wafers, as confirmed by both SIMS and TEM analysis. In particular, large clusters, i.e. with diameter above the TEM detection limit (2 nm), undergo a classical Ostwald ripening process (increase in size, decrease in density). SRP measurements indicate that Boron activation in this low temperature regime is not related to clusters dissolution. On the other hand, the initial Solid Phase Epitaxial Growth, BF2+ implanted wafers exhibit an increase in sheet resistance, due to boron clustering induced by the dissolution of EOR defects. Finally, it is found that at higher spike anneal temperatures (above 850 °C), both B+ and BF2+ implanted wafers exhibit a similar behavior, with a peak increase in sheet resistance as measured by Boron activation.


Spice anneals in conjunction with ultra-low energy implants are widely used to form ultra shallow junctions for source/drain extensions in advanced CMOS devices. A deep understanding of the different phenomena involved in forming these junctions (including activation and diffusion anomalies and related defect evolution) is therefore mandatory. In this paper, the evolution of sheet resistance, junction depth and defects during the whole thermal cycle of a typical spine anneal (1050 °C) is investigated in detail. Therefore the anneals were interrupted at peak temperatures ranging from 800 °C to 1050 °C in temperature steps of 50 °C. These experiments were done both on B+ (500 eV, 1015 cm-2) and BF2+ (2.2 keV, 1015 cm-2) implanted wafers. All wafers were analyzed with four point probe and SIMS, while selected samples were selected to carry out AFM and SRP. It is found that BF2+ implanted wafers exhibit a much better electrical activation than B+ implanted ones at temperatures below 850 °C, due to the amorphization process occurring during the BF2+ implant. In this low temperature regime, Boron clustering takes place very rapidly in B+ implanted wafers, as confirmed by both SIMS and TEM analysis. In particular, large clusters, i.e. with diameter above the TEM detection limit (2 nm), undergo a classical Ostwald ripening process (increase in size, decrease in density). SRP measurements indicate that Boron activation in this low temperature regime is not related to clusters dissolution. On the other hand, the initial Solid Phase Epitaxial Growth, BF2+ implanted wafers exhibit an increase in sheet resistance, due to boron clustering induced by the dissolution of EOR defects. Finally, it is found that at higher spike anneal temperatures (above 850 °C), both B+ and BF2+ implanted wafers exhibit a similar behavior, with a peak increase in sheet resistance as measured by Boron activation.

9:30 AM C5.4 Activation, Diffusion and Defect Formation of a Spike Anneal in Laser Annealing Cycles. Silwa Paul1, Wilfred Leung1, Antonino La Magna2, Paola Alippi1, Vittorio Privitera1, Guglielmo Nardella1 and Puccio Cristiano2; 1Process Development, Mattson Thermal Products GmbH, Dornstadt, Germany; 2Ion Implantation Group, LAAS-CENRS/CRNS, Toulouse, France.

9:45 AM C5.5 Technology computer aided design of ultra-shallow junctions in Si devices formed by laser annealing processes. Antonino La Magna1, Paola Alippi1, Vittorio Privitera1, Guglielmo Nardella1 and Puccio Cristiano2; 1CNR-IMMM Sezione Catania, Catania, Catania, Italy; 2CNR-IFN Sezione Roma, Roma, Italy; 3STMicroelectronics, Catania, Italy; 4Department of
The laser annealing process, applied to the formation of ultra-shallow junctions in Si, offers important advantages respect to conventional thermal process such as: the control over the junction depth and a higher dopant activation efficiency. However, the process integration is extremely critical, in the irradiation process, the device itself acts as a complex scattered to the laser light. Moreover, the concurrent evolution of the thermal field, molten regions and dopant density during the process is not predictable without suitable computational support. In this work, we present a numerical simulation of the laser annealing process in transistor structures. Our approach is based: a) on the simulation of electromagnetic field in the structures formed layer of lossy (e.g. Si) or non-lossy (e.g. SiO2) dielectrics; b) on the simulation of the thermal phase and impurity fields under irradiation. Using the former tool, based on a finite difference time domain approach, we calculate the heat source distribution in the specimen. Afterwards, such source distribution is used as input in a phase-field simulation. The phase-field formalism, aimed to simulate the local temperature and phase changes and the consequent dopant redistribution during the laser annealing process. The tools are implemented in view of their integration in technology computer aided design packages. We solved numerically the phase field equations in two dimensional structures, considering as initial status the generic material modification due to an ion implant process: i.e. the implanted impurity two dimensional profile in structured samples containing also SiO2/Si-SiO2/Si stacks. The model is parametrised in the case of different impurity atoms, considering the thermal properties of the materials and the impurity depending diffusivity in the solid, liquid and interfacial region (characterized by a specific phase-field model). In these cases, molecular dynamics simulation is also used to assess such parameters. We present various simulation results by varying not only implanted impurity profiles, and geometry of the CMOS-like structures but also the laser pulse conditions. With the support of the simulation results we discuss the possible problematic and the new perspectives of the excimer laser annealing process: application in the fabrication of scaled CMOS devices. The simulated evolution is compared to experimental characterisation of laser annealed samples performed by secondary ions mass spectroscopy and spreading resistance profiling, transmission electron microscopy and selective etch techniques. The comparisons show the importance of the joined theoretical and experimental investigation in order to understand the effect of laser annealing on our specimens.

Ultra-Shallow Junction Formation Technology from the 130 to the 45 nm Node. Anishtab Jain, Texas Instruments Inc., Dallas, Texas.

One of the main materials challenges of the 130 nm silicon technology node was the need to find a processing solution to the anomalous diffusion behavior of Boron (B) and Fluorine (F) in silicon. Over the last two decades of research. Reduction of implantation energy no longer proved sufficient when trying to reduce source/drain extension junction depth while increasing abruptness and limiting sheet resistance. Spike annealing, a process in which implants are heated rapidly to a temperatures required for dopant activation and then cooled down without dwelling at temperature, adequately addressed the scaling requirements of this node. The resulting junctions achieved high dopant concentration values very close to the surface while having limiting junction depth. However, this increased the propensity for dopant migration to overlying layers associated with the source/drain spacer. Loss of device performance due to this and other integration-related phenomena becomes a strong motivating factor for further materials research in order to sustain progress through the 130 nm and 90 nm node. Complex interactions between various layers have been understood and the resulting developments in spacer diffusion barriers have enabled high performance devices. Whereas the new processes have enabled early 65 nm node development, there are strong indications that they will place constraints on technology before the beginning of the 45 nm node, particularly where high performance is desired. The constraints are likely to show up first in terms of inadequate junction abruptness and then also in terms of junction depth reduction. Recent experiments using ultra-high temperature annealing with arc-lamps or cw lasers have shown that it is possible to reduce the irradiation time while maintaining high sheet resistance and abruptness defined by the initial implant if appropriate processing conditions are chosen. Problems associated with residual damage remain and require further investigation.

Optimization of Fluorine co-implantation for PMOS Source and Drain extension formation to meet the 65nm technology node, Honda Group, Amir Al Bayati, Suzanne Felix and Majed Foad; Front End Product Group, Applied Materials, Sunnyvale, California.

The main challenge for the Ultra shallow junction formation of PMOS remains the transient enhanced diffusion (TED) and the relative low solid solubility of boron in silicon. It has long been demonstrated that low energy boron and the spike annealing are key in meeting the 60 nm technology node ITRS requirements. To meet the 65 nm technology requirements (Xj<17nm, Rs<7600ohms/sq, abruptness<2.8 nm/decade) many studies have used Fluorine co-implantation with boron and Si or Ge preamorphization and spike annealing to meet these requirements. The Fluorine has been shown to reduce TED but its energy needs to be well optimized with respect to the Boron implant energy. In this work we demonstrate that not only the fluorine energy needs to be optimized to the boron's but that a new parameter, the fluorine co-implantation energy needs to be added. In this work, we will include a comparison of the electrical data with atomic profiles measured using SIMS and RBS measurements to determine the residual damage and crystal quality.

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beyond the original amorphous-crystalline (a-c) interface, the so-called end – of – range defects. Finally, we performed thermal anneals under various conditions, in order to induce the release of self-interstitials from these defects and thus provoke the TED of B atoms. The results obtained show several interesting characteristics. First, during the regrowth process, F atoms undergo segregation towards the surface region, although a quantity of F remains in the regrown matrix. Second, after the recrySTALLization, F diffuses both towards the surface and towards the bulk, where it accumulates in the end-of-range region. Third, F diffusion is not affected by the B presence, there being no indication of B-F complexes formation through clustering. Fourth, the B TED decreases with the amount of incorporated F, up to its complete suppression for the highest fluence. Nevertheless, after annealing at 1100 °C for 30 s, we have observed a complete out diffusion of both B and F, which rules out B-F chemical bonding as responsible for the slowing down of B TED. Instead, the B diffusion decreasing is owing to a strong interaction between F and self-interstitials, which results in the reduction of self-interstitials concentration.

11:45 AM C5.10
Post-Anneal Stress Reduction of 200 mm Silicon Wafers in Single Wafer Rapid Annealing. Tsuyoshi Setokubo1, Eichi Nakano1, Kazuo Aizawa1, Hidekazu Miyoshi1, Jiro Yamamoto1, Takashi Fukuda1 and Woo Sik Yoo1, 1Hiroshima Elpida Memory, Inc., Hiroshima, Japan, 2WaferMasters, Inc., San Jose, California.

For advanced ULSI devices below 130nm design rules, the precise control of thermal budget is one of the key issues in thermal processing from the device performance point of view. Minimizing the variation in device performance is very important for device yield management and quality control. With the shrinkage in device dimensions and allowable thermal budgets, lamp-based, single wafer rapid thermal annealing (RTA) systems became very popular for limited thermal processing applications. However, thermally induced stress in wafers during RTA processes causes small distortions on the wafer surface. This increases the difficulty of subsequent lithography steps, as the resolution of lithography is influenced by the local and global flatness of the wafer. Therefore, the temperature of an individual zone is dynamically controlled using feedback signals from in situ pyrometric temperature measurement of the corresponding zone on the wafer. Precise wafer temperature control and measurement are a significant technical challenge, as lamp power is constantly modulated by the feedback signals from the wafer temperature monitoring zones. In the dynamic wafer temperature control of DRAM devices with 110nm design rules, the authors were able to significantly improve electrical characteristics and post-anneal wafer stress by switching annealing steps from a lamp-based RTA system to a furnace-based RTP system. The flatness of wafers after annealing in the SRTF system improved around 15% compared to those annealed using the lamp-based RTP systems. This was due to the nearly isothermal process environment of the SRTF system and the flat surface of the annealed wafers providing better results in subsequent lithography steps. The detailed wafer stress measurement data will be presented at the conference.

SESSION C6: Atomistic Simulation Approaches
Chair: Wolfgang Windl
Wednesday Afternoon, April 14, 2004
Room 2002 (Moscone West)

1:30 PM *C6.1
Modeling atomistic ion-implantation and diffusion for simulation of MOSFET intrinsic fluctuation arising from line-edge roughness. Masami Hane, Takeo Ikezawa and Tatsuya Ezaki; Silicon Systems Research Laboratories, NEC Corporation, Kawasaki, Japan.

We have developed new simulation tools for the more precise designing of sub-100nm MOSFETs in which the intrinsic statistical nature of the fluctuations in device characteristics. First, during the regrowth process, F atoms undergo segregation towards the surface region, although a quantity of F remains in the regrown matrix. Second, after the recrySTALLization, F diffuses both towards the surface and towards the bulk, where it accumulates in the end-of-range region. Third, F diffusion is not affected by the B presence, there being no indication of B-F complexes formation through clustering. Fourth, the B TED decreases with the amount of incorporated F, up to its complete suppression for the highest fluence. Nevertheless, after annealing at 1100 °C for 30 s, we have observed a complete out diffusion of both B and F, which rules out B-F chemical bonding as responsible for the slowing down of B TED. Instead, the B diffusion decreasing is owing to a strong interaction between F and self-interstitials, which results in the reduction of self-interstitials concentration.

We developed new simulation tools for the more precise designing of sub-100nm MOSFETs in which the intrinsic statistical nature of the fluctuations in device characteristics. Towards this purpose, the authors performed a comparative annealing study of each device. The 3D device simulations were based on the classical drift-diffusion approach in which electrostatic potentials are constructed from the long-range Coulombic components of the individual dopant atom potentials. This simulation system was applied to sub-100nm super-halo designed MOSFETs. We found that LER not only modulates Lg but also increases effective dosages from halo-implantation, since it effectively increases the diffusion in sub-100nm technology. For this reason, using atomistic process simulation to examine LER has led to non-trivial insights that will be useful in further optimization of the design of fabrication processes.

2:00 PM C6.2
Fast Diffusion Mechanism of Tri-Interstitial in Si. Yaojun Du, Richard G. Hennig and John W. Wilkins; Department of Physics, The Ohio State University, Columbus, Ohio.

Ab initio nudged-elastic-band and dimer method calculations determine the dynamics of small interstitial clusters in Si. The formation of a three-atom interstitial cluster moves as a five-atom hexahedron along the [111] directions. The correlated motion consists of a 1.31 Å translation and a 60° rotation. The compact tri-interstitial jumps with equal probability into one of the four equivalent, neighboring sites along the [111] bond directions, i.e., it diffuses isotropically on the Si bulk. The computed 0.5 eV activation energy and 0.8.10^-4 cm²/s prefactor are strikingly similar to the measured overall interstitial diffusion rate of 1.0–exp(-0.4 eV/kgT) cm²/s. We speculate that the compact tri-interstitial dominates the diffusion of small interstitial Si clusters and is responsible for the formation of Si planar defects.

2:15 PM C6.3
Theoretical investigations of In-related defects in silicon. Paolo Aliotti, Antonino La Magna, Silvia Scalise and Vittorio Frivitera; CNR-IMM, Catania, Italy.

Indium is considered as an alternative to boron as p-type dopant in silicon, although it shows a lower electrical activity, it allows in fact the realization of steeper as-implanted profiles, due to its heavier mass. Increased activation is found in samples co-implanted with carbon, presumably due to the shallow electronic level associated to In-C complex. The present work is aimed at filling the lack of atomistic theoretical investigations on In defects in silicon, providing a well-founded ab-initio picture of defects energetics and diffusivity over which a continuum diffusion model is built. Equilibrium geometries and formation energies of In complexes with silicon native defects, vacancy (V) and interstitials (I), and with C impurities are investigated within density functional theory, using the Vienna Ab-initio Simulation Package. We determine the migration energies of In and I-mediated diffusion mechanisms through the location of the saddle points along the minimum energy paths. We also identify the In-C complex responsible for the increased electrical activation in In C-doped silicon samples and discuss its formation mechanism from the ab-initio results. Motivated by the results on In-C pair, we present

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A preliminary study of In-Ge defects in silicon, aimed at discussing the efficiency of alternative isovent (i.e., Ge) co-doping in improving In activity, has shown that, in a continuous way, we integrated a diffusion model that allows the direct comparison with experimental data. The diffused profiles obtained by the simulations are compared to those measured by secondary-ion-mass-spectroscopy or implantation and ion beam methods, showing a noteworthy agreement at different process conditions.

2:30 PM C6.4
Sumeet Singh Kapur and Taiid Sinno; Chemical and Biomolecular Engineering, University of Pennsylvania, Philadelphia, Pennsylvania.

Nucleation, growth and dissolution of Silicon self-interstitial clusters play an important part in silicon processing. Self-interstitial clusters produced during ion implantation of boron become unstable and redissolve during subsequent processing, creating a silicon sub-100nm supersaturation. The presence of excess self-interstitials enhances the diffusion of implanted boron, leading to the so-called Transient Enhanced Diffusion (TED) effect. Self-interstitial clusters are also known to lead to large dislocation loop networks during Czochralski crystal growth and prevent the use of interstitial-rich material for device applications. In both cases, it is well known that a carbon atom concentration of over 1019 cm\(^{-3}\) in the region of self-interstitial supersaturation greatly reduces interstitial cluster size evolution, but the exact mechanism remains under debate. In this work, we study the effect of carbon on self-interstitial aggregation using consistent atomistic and continuum representations. In the atomistic approach, two large-scale parallel molecular-dynamics (PMD) simulations were carried out using the multi-component Tersoff potential in a system containing 216,000 silicon atoms, each with an additional 1,000 self-interstitials initially placed in uniformly spaced tetrahedral sites. In the second approach, all self-interstitials were present, corresponding to a carbon concentration of about 0.006 \(4.6\times10^{-20}\) atom/cm\(^3\). We find that presence of carbon leads to slower average cluster size evolution, as is observed in crystal growth experiments. On the other hand, the evolution of single self-interstitials is unaffected by the carbon atoms, and only the evolution of larger cluster sizes show a marked difference between the two simulations. These results are investigated further with long-time diffusion calculations at each cluster size with and without carbon. The aggregation and diffusion simulations are interpreted quantitatively with a mean-field model that confirms the hypothesis that carbon mediates interstitial clustering by interfering with cluster transport and not directly on single self-interstitials. The mean-field model subsequently is used to investigate longer time evolution relevant to crystal growth and wafer processing.

2:45 PM C6.5
Accurate and Fast Monte Carlo simulation of ion implantation into arbitrary 1D/2D/3D structures for Si technology.
Shiying Tian, Victor Moroz1 and Norbert Strecker1; 1Synopsys, Inc., Dallas, Texas; 2Synopsys, Inc., Mountain View, California.

As the semiconductor industry aggressively scales silicon device feature sizes down to sub-100nm regime, Si processing technology moves towards more complex implants with complex device geometries, and topography and diffusionless (<3nm) activation. Ion implantation simulation is one of the most critical steps for accurate prediction of dopant placement in a silicon device. The well-known stand-alone MC ion implantation simulators are not suitable for such tasks. In order to overcome this problem, we have developed an integrated MC simulator, which is capable of simulating implants into any amorphous materials and crystalline silicon with arbitrary geometry and topography and is capable of predicting the 1D/2D/3D as-implanted dopant distributions from sub-kV to above 10 MeV for common dopant species. Our model is based on the classical binary collision approximation (BCA) such as that used by TRIM for amorphous materials. Moreover, we integrated crystalline silicon. We used ZBL universal interatomic potential for nuclear scattering, and a modified version of electronic stopping power model which combines both local and nonlocal contributions. Damage accumulation is based on the modified Kiechle-Pease formula. The dechanneling effect of the damage is realized by switching the model from crystalline to amorphous collision model with the probability proportional to local defect concentration. This scheme is very computationally efficient, and is 10 times faster than TRIM. Our new file-based MCsimulators for large and very large implants. We have implemented trajectory split and lateral trajectory replication algorithms which greatly reduce the simulation time. With the improved efficiency and seamless interface with diffusion simulations, MC implant simulation as a better alternative to analytic implant in a complete process flow becomes realistic. With this simulator, we investigated 2D LDD and halo implants, and 3D cylinder and square trench implants, and illustrated the importance of <110> channeling and lateral scattering for sub-100nm silicon technology. It is demonstrated that, in contrast to analytic implant model, integrated MC simulator is particularly suitable for high tilt halo implants into complex 3D structures (such as FinFET), as the complex geometry and topography, high tilt channeling effect, as well as pre-existing damage are accurately taken into account automatically. Therefore, integrated MC implant simulator is ideally suited for predictive TCAD simulations for silicon technology.

SESSION C7: Boron Activation and Diffusion Modeling
Chair: Mark Law
Wednesday Afternoon, April 14, 2004
Room 2002 (Moscone West)

3:30 PM C7.1
Boron-Interstitial Cluster Kinetics: Extraction of Binding Energies from Dedicated Experiments. Christine J. Ortiz1, Giovanni Mannino2, Peter Pichler3, Vittorio Pruttera, Sandro Solodi1, Silvia Scialow2. 1Technology Simulation Dpt, Fraunhofer IISB, Erlangen, Germany; 2IMM-CNRS Sezione Catania, Catania, Italy; 3IMM-CNRS Sezione Bologna, Bologna, Italy.

In ULSI fabrication, ion implantation at ultra-low energy is nowadays a standard method for introducing dopants such as boron into silicon. Generally, this step must be followed by a high-temperature process in order to anneal the implant damage and to electrically activate dopant atoms. However, damage from boron implantation in boron exhibits large transient enhanced diffusion (TED) due to the high self-interstitial (I) excess concentration produced by ion bombardment. Moreover, boron activation can be incomplete, even at conditions well below solubility limits. Small boron clusters are present, corresponding to a carbon concentration of about 0.9% \(4.6\times10^{-20}\) atom/cm\(^3\). We find that presence of carbon leads to slower average cluster size evolution, as is observed in crystal growth experiments. On the other hand, the evolution of single self-interstitials is unaffected by the carbon atoms, and only the evolution of larger cluster sizes show a marked difference between the two simulations. These results are investigated further with long-time diffusion calculations at each cluster size with and without carbon. The aggregation and diffusion simulations are interpreted quantitatively with a mean-field model that confirms the hypothesis that carbon mediates interstitial clustering by interfering with cluster transport and not directly on single self-interstitials. The mean-field model subsequently is used to investigate longer time evolution relevant to crystal growth and wafer processing.

3:45 PM C7.2
Quantitative investigation of boron-interstitial-cluster formation and dissolution. Davide De Salvador1, Salvatore Mirabella2, Enrico Napolitani3, Gabriele Basso2, Elena Bruno3, Giovanni Impellizzeri2, Leonardo Aldighieri3, Davide Carnera3 and Francesco Pirolo2. 1Dipartimento di Fisica, INFN e Universita' di Padova, Padova, Italy; 2Dipartimento di Fisica e Astronomia, MATIS - INFN e Universita' di Catania, Catania, Italy.

Boron is the primary p-type dopant in Si device fabrication. It was largely demonstrated that in presence of a high self-interstitials (I) supersaturation (typically produced by ion implantation and subsequent annealing) and a high boron concentration, large transient enhanced diffusion (TED) due to the high self-interstitial (I) excess concentration produced by ion bombardment. Moreover, boron activation can be incomplete, even at conditions well below solubility limits. Small boron clusters are present, corresponding to a carbon concentration of about 0.9% \(4.6\times10^{-20}\) atom/cm\(^3\). We find that presence of carbon leads to slower average cluster size evolution, as is observed in crystal growth experiments. On the other hand, the evolution of single self-interstitials is unaffected by the carbon atoms, and only the evolution of larger cluster sizes show a marked difference between the two simulations. These results are investigated further with long-time diffusion calculations at each cluster size with and without carbon. The aggregation and diffusion simulations are interpreted quantitatively with a mean-field model that confirms the hypothesis that carbon mediates interstitial clustering by interfering with cluster transport and not directly on single self-interstitials. The mean-field model subsequently is used to investigate longer time evolution relevant to crystal growth and wafer processing.
induced by the BICs in the different investigated conditions. These analyses provide important information for the structure determination and interpretation of dynamics of BICs when formed and dissolves at high B concentrations.

4:00 PM C7.3
Atomistic Analysis of The Role Of Silicon Interstitials In Boron Cluster Dissolution, Maria Abog, Lourdes Pelaz, Luis A. Marques, Pedro Lopez and Juan Barbolla, University of Valladolid, Valladolid, Spain.

Ion implantation is the preferred method for introducing dopants into silicon. Subsequent thermal annealing is used to remove the implant damage, and electrically activate dopants, such as boron. However, in the initial stages of the annealing B clusters are formed and thus, a significant amount of B atoms are immobilized and are electrically inactive. High temperatures or long annealing times are required to completely activate the B atoms by the slow dissolution of these B clusters. A number of theoretical and experimental data have revealed the role of Si interstitials in the nucleation and growth of B complexes. In this work, we investigate through atomistic kinetic Monte Carlo simulations the role of Si interstitials in the stabilization and dissolution of boron clusters. The simulations process generates a high Si interstitial supersaturation, leading to the rapid formation of Si-B interstitial complexes. Then the system evolves towards lower Si interstitial supersaturations established by the Si-B interstitial complexes and other Si interstitial clusters or extended (311) defects (loops). Also an oxidizing ambient during the anneal establishes a larger Si interstitial supersaturation compared to anneals in inert ambient. Our analysis indicates that the B cluster dissolution is slowed by the presence of higher Si interstitial supersaturations. The simulation shows that the reactivation of B during the post-implant thermal treatment is slower in an oxidizing ambient than in inert ambient, in agreement with experiments [L. Radic et al, Appl. Phys. Lett. 81, 826 (2002)]. This result is consistent with Si interstitial rich B clusters having a lower total energy than those poor in Si interstitials, as proposed by several authors [L. Pelaz et al, Appl. Phys. Lett. 74, 3657 (1999); X-Y. Liu et al, Appl. Phys. Lett. 77, 2911 (2000)]. The presence of Si interstitial supersaturation favors the capture of Si interstitials by B clusters, leading to B clusters rich in Si interstitials, and hence, more stable.

4:15 PM C7.4
BIC Formation and Boron Diffusion in Relaxed Si0.8Ge0.2, Robert T Crosby1, L. Radic1, Kevin Jones1, Mark Law1, Jinning Liu1, P. E. Thompson1, Tony Sanvedra2 and M. Klimes3.

The relationships between Boron Interstitial Cluster (BIC) evolution and boron diffusion in relaxed Si0.8Ge0.2 have been investigated. Structures were used to observe potential strain compensation effects between the boron and germanium constituents. Interstitial supersaturation conditions and the resultant defect structures of ion implanted relaxed Si0.8Ge0.2 and Si0.8Ge0.2 implanted with 2x1015 B/cm2 were examined with Transmission Electron Microscopy (TEM) and energy dispersive x-ray analysis (EDX).

4:30 PM C7.5
The Effect of Photoresist Outgassing on Boron Clustering and Diffusion in Low Energy BF2+ Ion Implantation, Peter Kopalidis and Serguei Kondratenko, Axcelis Technologies, Beverly, Massachusetts.

During high current implantation into photoresist-covered substrates, evolution of gaseous by-products of photoresist breakdown occurs that can affect the dose control of the process as well as diffusion and activation of the implanted dopants in silicon. The dosimetry effects are well understood and accounted for in modern ion implantation. However, there are no reports on the effect due to photoresist outgassing on the distribution of boron concentration in silicon during the subsequent annealing process, boron electrical activation and sheet resistance measurements. Experiments were performed on near-crystalline and pre-amorphized silicon and oxidized wafers that help elucidate the mechanism of boron accumulation and diffusion. The effects of activation temperature and photoresist carbon-containing species driven by ion implantation are investigated and a mechanistic explanation is proposed. Finally, practical ways are proposed that ensure accurate dosimetry and sheet resistance repeatability, independent of the photoresist load.

4:45 PM C7.6
Hydrogenation-enhanced Low Temperature Activation of Boron in Silicon, A. Vengurlekar1, S. Ashok1 and C. E. Kalna2.

The presence of vacancies enhances the boron activation. On a separate but related note, previous theoretical and experimental works have shown that the presence of vacancies leads to enhanced activation of other kinds of dopants in crystalline silicon, by relaxation of strain in the lattice. In this work, we report on the effect of hydrogen plasma treatment on the activation of boron in silicon, and the diffusion of boron in silicon at ultra-shallow depths. It is known that plasma hydrogenation followed by annealing results in creation of vacancies by the out-diffusion of hydrogen during annealing. We aim to make use of the vacancies created by hydrogen diffusion during rapid thermal annealing to influence activation in the boron-implanted region at various annealing temperatures. Boron was implanted into n-type silicon at 5 keV at a dose of 1x1015 cm-2. Prior to implantation, some of the samples were subjected to an ECR plasma treatment. SIMS measurements were performed on the samples after implantation and subsequent annealing at temperatures ranging from 400°C to 750°C for various times. Transmission Electron Microscopy (TEM) was used to monitor the agglomeration of implanted silicon interstitials and the evolution of extended defects in the near-surface region. Secondary Ion Mass Spectroscopy (SIMS) concentration profiles facilitated the characterization of boron diffusion behaviors during annealing, while Hall Effect measurement techniques facilitated the measurement of active boron concentrations. High Resolution X-Ray Diffraction (HRXRD) rocking curves were also employed to observe potential strain compensation effects between the boron and germanium constituents. Interstitial supersaturation conditions and the resultant defect structures of ion implanted relaxed Si0.8Ge0.2 in both the presence and absence of boron have been accurately characterized. The role of strain compensation in the retardation of boron diffusion in relaxed Si0.8Ge0.2 is also discussed further.

SESSION C8: Poster Session II
Chairs: Benjamin Colombenu and Peter Pichler
Wednesday Evening, April 14, 2004
8:00 PM

C8A
Deactivating defects of group V donors in heavily doped Si, Dominik Christoph Mueller and Wolfgang Fichtner, Integrated Systems Laboratory, Swiss Federal Institute of Technology, Zurich, Zurich, Switzerland.

We report new insight into the deactivation mechanisms of P, As and Sb in Si. Based on our sb ion calculations, we suggest a 3 step model which is able to explain experimental data in highly n-doped samples. In the absence of excess native point defects, donor deactivation comes about by lattice distortions that form readily in the proximity of two or more donor atoms. Hence, this deactivation mechanism is strongly dependent upon the donor concentration and becomes predominant at doping levels above 1020 cm-3. Since the preparation takes place without reimplantation of the impurity in the crystal, it is able to explain the measured saturation of conduction electrons above donor concentrations of approximately 5x1018 cm-3 in samples prepared by low temperature molecular beam epitaxy. These
donor deactivating distortions (3 for short) are a precursor to the experimentally observed Frenkel pair generation and donor-vacancy clustering. The latter redistribute the highest energy states that were observed at higher process temperatures, where diffusion of donors and point defects is prevalent. Ultimately, precipitation may set in as a last step in the deactivation chain, most prominently in the case of the large Sb atoms in Si.

C8.2 Arsenic adsorption onto silicon steps surface prepared by Hartree-Fock at semiempirical level. Anna Maria Mazzone, Istituto IMM, CNR, Bologna, Italy.

Arsenic adsorption onto silicon surfaces vicinal to (100) has been studied using the cluster model of the exposed surface and the Hartree-Fock method at a semiempirical level. The results illustrate the properties of the As-doped steps in dependence of the step structure and of the type, substitutional or interstitial, of the impurity. The central finding is that As adsorbed is preferably adsorbed on the step location and the physical explanation is the stronger electrostatic coupling with the step. Preferred pathways of As from surface to bulk are discussed. The study illustrates also the formation of step states and bands and the effects of As on these states.

C8.3 Classical MD Study on the Mobility of Di- and Tri-Interstitials. Matthias Posselt, Institute of Ion Beam Physics and Materials Research, Forschungszentrum Rossendorf, Dresden, Germany.

In a recent work [1], a combined simulation method was applied to investigate ion-beam-induced defect formation in silicon. BCA simulations were used to treat the ballistic processes, whereas the subsequent fast relaxation and the first stage of thermally activated processes were described by classical MD calculations. It was found that the metastable defect structure formed immediately after ion impact consists not only of isolated vacancies and self-interstitials but also of complex defects. A more detailed analysis of the results shows, that at elevated implantation temperatures or during the annealing of the defect structures obtained at room temperature, di- and tri-interstitials are formed. In some cases a high mobility of these defects is observed. In agreement with former studies [2,3], the di-interstitial is found to move relatively fast. The present contribution deals with systematic investigations on the migration of di- and tri-interstitials. The classical MD simulations allow direct investigations of the motion of defects and its atomic mechanisms. Particular attention is paid to the role of transformations between different modifications of di- or tri-interstitials. These transformations may lead to an substantial increase or decrease of the defect mobility. The present results are compared with the few literature data obtained by tight-binding and density-functional methods which employ mainly static potential energy calculations. [1] M. Posselt, Mat. Res. Soc. Symp. Proc. 647 (2001) O1.1.1. [2] G. H. Gilmer, T. Dexe de la Riviere, M. Jaraiz, Nucl. Instr. Meth. Phys. Res. B 102 (1995) 247. [3] M. Hane, T. Ileezawa, G. H. Gilmer, Proc. SISPAD 2000, IEEE Catalog Number 00THS502, p. 119, IEEE, Piscataway, 2000.

C8.4 Interactions of Indium, Arsenic and Carbon in silicon using the pseudopotential technique. Xinyu Yan, Maxim Chuchkine and Maria Stoyanova de La Roche, Institute for Emerging Technologies Research Centre, De Montford University, Leicester, Leicestershire, United Kingdom.

Indium (In) is a promising option for achieving punch-through suppression and threshold voltage control in sub 100 nanometer MOSFET technologies. However, In suffers from poor activation and excessive diffusion due to Transient Enhanced Diffusion. There is an urgent requirement to resolve these issues for the 60 nm node. In this talk, a detailed study of the defect-dopant dynamics at the Si/Si02 interface will be presented. We also find that boron-interstitial pairs become unstable near the interface, which, in turn, lead to boron precipitation and TED reduction. Along with the configuration and energetics, we will also show changes in i) bonding mechanisms (based on electron density and electron localization function topologies) and ii) diffusion pathways and barriers of vacancies, interstitials, and boron-interstitial complexes near the Si/Si02 interface.

C8.5 Behavior of Vacancies, Interstitials and Boron-Interstitial Pairs at the Si/Si02 Interface. Teresa A. Kirschchenko1, Decay Yu Gyeong S. Hwang1,2, Bao Ahn2,3, Paul K. Chu4,1, City University of Hong Kong, Hong Kong, Hong Kong; 2Shanghai Institute of Microsystem and Information Technology, Shanghai, China.

Ion implantation induced damage and the diffusion behavior of indium implanted into silicon-on-insulator (SOI) substrates at different energies and doses and annealing at different temperatures were studied. Using Rutherford backscattering spectroscopy (RBS) in the channeling mode and secondary ion mass spectrometry (SIMS), the redistribution of indium in both the top silicon and buried SO2 layer of SOI after annealing was investigated. At a relatively high implantation energy and dose (200 keV, 1x14cm-2), the diffusion behavior of indium in SOI is different from that in bulk silicon. Indium segregates to the buried Si/Si02 interface and the effects of end of range indium damage are quite prominent. Our data shows that in-diffusion of indium is effectively blocked and so transient enhanced diffusion (TED) is less pronounced in SOI than in bulk Si, thereby making it easier to get a steep retrograde channel profile (SRC) in SOI that is beneficial for subsequent device fabrication. Hence, the use of indium as an n-channel dopant in SOI is a distinct possibility.

C8.6 Ion Implantation Behavior and Implantation-Induced Damage in Indium Implanted Silicon-on-Insulator. Peng Chen1, Ming Zhu2,1, Zheng Hua An2, Ricky King Yu Fu1, Wei Li Liu2 and Paul K. Chu1, 1City University of Hong Kong, Hong Kong, Hong Kong; 2Shanghai Institute of Microsystem and Information Technology, Shanghai, China.

Ion implantation induced damage and the diffusion behavior of indium implanted into silicon-on-insulator (SOI) substrates at different energies and doses and annealing at different temperatures were studied. Using Rutherford backscattering spectroscopy (RBS) in the channeling mode and secondary ion mass spectrometry (SIMS), the redistribution of indium in both the top silicon and buried SiO2 layer of SOI after annealing was investigated. At a relatively high implantation energy and dose (200 keV, 1x14 cm-2), the diffusion behavior of indium in SOI is different from that in bulk silicon. Indium segregates to the buried Si/SiO2 interface and the effects of end of range indium damage are quite prominent. Our data shows that in-diffusion of indium is effectively blocked and so transient enhanced diffusion (TED) is less pronounced in SOI than in bulk Si, thereby making it easier to get a steep retrograde channel profile (SRC) in SOI that is beneficial for subsequent device fabrication. Hence, the use of indium as an n-channel dopant in SOI is a distinct possibility.

C8.7 Experimental characterization and modelling of indium implanted in silicon. Silvia Scelse, Antonino La Magna, Paola Alippi and Vittorio Privitera, CNR-IMM, Catania, Italy.

A systematic experimental study on indium implantation in silicon over a large range of implant energies and doses was performed. The evolution of the implant damage following thermal annealing was observed. A critical issue concerning In is represented by its outdiffusion, taking place during the thermal processes, that is...
limiting factor to get In peak concentration needed for applications in microelectronics. Then the use of different kinds of thermal processes has been evaluated with particular attention to achieve a reduction of the outdiffusion and an increase of the electrical activation of In in silicon. The role of C, present in the silicon substrate as a contaminant or as co-implanted species, on the electrical activation and diffusion of In in silicon was also investigated. In order to explain the peculiar electrical behaviour of In, arising from the presence of C, a model based on the formation of In-C complexes due to the interaction between In and C atoms present in the silicon matrix, was implemented into the simulation software FLOOPS and used to simulate the experimental results. This model, considering the reaction between In, C, interstitials and vacancies, based on the energetics obtained from first-principle calculations, allows to reproduce both the diffusion and the electrical activation of In in Si.

### C8.8
Multiple Implantations - Experiments and Computer Simulations, Matthias Posselt, Michael Maeder, Andrei Lobedev and Rainer Groetzschel, Institute of Ion Beam Physics and Materials Research, Forschungszentrum Rossendorf, Dresden, Germany.

Advanced technologies use successive implantations of p- and/or n-dopants without any intermediate annealing steps. A characteristic example is the engineering of the regions of source, drain, extension and halo. The sequence of the implantations may influence the final distribution of dopants and radiation damage. In particular it affects the as-implanted distribution of dopants if in one or more implantation steps the direction of ion incidence is close to a major crystallographic axis of the silicon substrate. For example, extension implantations are often performed perpendicularly to the wafer surface, i.e. nearly parallel to the [100] axis. The defect production in previous implantations influences the shape of dopant and damage profiles in a subsequent channeling implantation step, since these defects may lead to increased dechanneling. Furthermore, the amorphization dose in a certain implantation step may be affected by the level of radiation damage formed during the previous implantation steps. The present work deals with the simple example of two consecutive implantations in order to demonstrate the effects mentioned above. Two implantation sequences are investigated: (i) 35 keV B followed by 50 keV As, as indicated in the [100] channel direction, (ii) 50 keV As followed by 35 keV B in the [100] channel direction. The depth profiles of B and As are measured by SIMS. The as-implanted damage is determined by RBS/C. The experimental data can be reproduced by atomistic computer simulations using the Crystal-TRIM code with an improved phenomenological model for damage buildup during multiple implantations. The present results contribute to a better understanding of ion-beam-induced defect formation and to progress in TCAD.

### C8.9
Simulation of BF2 ion implantation into crystalline silicon: Influence of boron activation and diffusion, Liyla M. Shahed-De Coq, Jerome Marcou and Kaoutar Ketata, Laboratory of Electronics Microtechnology and Instrumentation (LEMI)-University of Rouen, Mont Saint Aignan, France.

We have investigated and modeled the diffusion of boron implanted into crystalline silicon in the form of boron difluoride BF2+. Secondary ion mass spectrometry (SIMS) has been used to measure dopant profiles in ion implanted samples with an energy of 500 eV (i.e. 1E15 cm-2). 2 keV BF2+ implantation. RTA was carried out at 950°C, 1000°C, 1050°C and 1100°C for 10s, 20s, 30s and 60s. During implantation, fluorine is introduced into silicon either by BF2+ ion implantation or by boron and fluorine co-implantation. BF2+ is traditionally one of the favored ion species used for p-type shallow and ultra-shallow junction formation due to its amphoteric behavior and small projected ranges compared to boron at the same implant energy. It has been shown that the addition of fluorine through introducing more damage in silicon is an effective way to reduce the number of silicon interstitials causing boron transient enhanced diffusion (TED) and enhancing boron activation. Several experimental and theoretical investigations on the diffusion of fluorine and its effects on boron diffusion and activation have been published in the literature. In a recent work, we have investigated the diffusion of ultra-low energy boron implanted in crystalline silicon and tested a complete simulation program which takes into account the effect of the silicon boron layer as a source of self-interstitials. However, our last model was still to be improved for simulating the deeply channelled fluorine tails. We have developed an accurate model based on the last one and carried out simulations which were compared with experiment. The simulations are consistent with most of experimental conditions.

### C8.10
A simple model for boron segregation to Rp defects, Na An and Jianxin Xia, School of Microelectronics and Solid-State Electronics, University of Electronic Science and Technology of China, Chengdu, Sichuan, China.

Boron exhibits anomalous diffusion during the initial phases of ion implant annealing. Boron transient enhanced diffusion (TED) is characterized by enhanced tail diffusion coupled with an immobile peak. Though the peak is lower than that of solubility in silicon, the immobile boron peak is electrically inactive. A simple model of boron segregation to Rp (the projected range) defects has been developed to explain this phenomenon. The immobile part of boron to Rp defects during ion implant annealing. The driving force of boron segregation is the difference of potential energy between boron atoms in the matrix and those at the periphery of Rp defects. After implantation, there is a net excess of interstitials with dose equal to the implanted dose and distribution mimicking the implanted ion distribution, and these interstitials coalesce into Rp defects. The evolution of Rp defects is closely related to the evolution of immobile boron peaks. Rp defects are assumed to decrease exponentially with time. A segregation energy of 0.57 eV was used as a parameter in this model. The enhanced diffusivity and duration in TED are calculated from an interstitial clustering model. A comparison between experimental and simulated boron profiles is shown for samples annealed at 800°C in nitrogen ambient for different times and implanted with dose of 2x10^14 cm^-2 at 15 keV and 30 keV, respectively. The satisfactory agreement between experimental and simulated boron profiles and confirmations indicates the immobile part of implanted boron during annealing originates from boron segregation to Rp defects.

### C8.11

It has been shown recently that significant differences in boron activation exist between silicon-on-insulator (SOI) and bulk Si. This investigation set out to understand the effect of boron concentration on electrical activation in SOI materials. SIMOX and SOITEC wafers, having surface Si thickness of 75 nm and 145 nm were implanted with 11B at 5.5 keV. The dose of the implant was varied from 3x10^14 cm^-2 to 1x10^15 cm^-2 to provide different boron concentrations within the times at temperatures ranging from 750°C to 1000°C to investigate the kinetics of the boron interstitial cluster (BIC) process in SOI. Hall effect was used to measure the fraction of active boron within the surface Si layer. A significant reduction in the active fraction of boron in SOI was observed and depended slightly on the boron concentration. However, increasing the dose loss of boron to the buried oxide (BOX) actually enhanced the active fraction of boron for thin SOI. This is attributed to a loss of boron interstitial clusters for thin SOI. However, the maximum active fraction of boron in thin SOI is limited by dose loss due to the implant, as well as segregation into the BOX. Therefore, there appears to be a tradeoff between a loss of boron to the BOX and maximum activation obtained in SOI. Prospects for modeling of dopant activation in SOI will also be presented.

### C8.12
The Role of Stress in Dopant Activation, Solid Phase Epitaxial Regrowth, and Defect Evolution, Michelle Shirly Ann Phan and Kevin Jones, University of Florida, Gainesville, Florida.

During silicon integrated circuit fabrication, wafers undergo internal stresses. The effect of these stresses on the doping process is of critical interest. This study investigates the role of stress on dopant activation, solid phase epitaxial regrowth, and defect evolution. Ultra-thin 50-100nm Ge+ or 1100°C silicon wafers were amorphized with 1E15 atoms/cm^3 of Ge+ at energy of 30 keV. Amorphization was followed by the implantation of 2 keV B+ at a dose of 1E15 atoms/cm^2 of BF2+ or BF. A known stress was applied to the wafers by bending them at a controlled radius of curvature so that the amorphous layer is in tension or compression. The bent wafers were then annealed at temperatures between 550°C and 750°C to determine solid phase epitaxial regrowth rate. Active dopant concentrations are obtained through the use of Hall effect measurements. Cross-sectional and plan-view TEM samples were utilized to examine defect formation and evolution. Preliminary data shows that regrowth rate was not affected when wafers were strained in tension appeared to have higher regrowth rates compared to those strained in compression. These results are consistent with those that were previously reported, therefore, further investigation is needed to confirm these trends. Hall results indicate that the solid phase regrowth at 620°C of the boron implanted layer activates about 45%
of the 1x10^15 dose independent of the sign of the stress. Additional results on the role of stress on defect evolution will be presented.

C8.13 High Concentration Fluorine: Experiments and Models.
Robert Russell Robinson 1, Mark E. Law 1 and Antonio F. Saavedra 2

Previously, we developed a lower concentration (sub-amorphizing dose) fluorine model, showing the abnormal diffusion of fluorine and its time-dependency. However, other results have indicated that annealing behavior of samples amorphized with fluorine as well as Si pre-amorphized samples implanted with fluorine is distinct from the behavior in crystalline silicon. We have completed new experimental work examining high concentration (amorphizing dose) fluorine and extended our model to explain the behavior. This model continues to fit our current experimental work. Boron dose of 80-2000Ohm-cm were first pre-amorphized with dual implants of 150keV and 40keV 1x10^15/cm2 Si to create a continuous 280um deep amorphous region. Samples were subsequently implanted with the fluorine conditions of 16keV at 2x10^15/cm2 or 8x10^15/cm2 dose. Samples were annealed by either conventional furnace or RTA with an N2 ambient for various times at temperatures of 550-750C. SIMS was used for depth profiling, and TEM analysis of Si and Ge layers were used to check for defects. The high-concentration model was based on our existing model for fluorine diffusion, using the same base equations and binding energies. The model was extended to include Si-Fx complex equations with binding energies based on published chemical data and other experiments. Additionally, a [311] loop model was incorporated into the simulations to account for the damage accumulation, interstitial trapping, and time-dependent release at the end of range. The model obtained good agreement with the experiments. Initial motion, peak concentration, and time dependence are modeled well in the 2x10^15/cm2 simulations at 550 and 750C. The "flat top threshold", an observed phenomena in which the concentration after annealing shows a peak at 10^15 concentration, is in reasonable agreement with the model in both cases. The 2x10^11/cm2 650C sample shows negligible motion after the anneal, a behavior that is distinct from the result in crystalline silicon, is also well modeled. A re-simulation of our previous crystalline results shows that the model well describes the difference in behavior, and is still compatible with previous results. The 8x10^15/cm2 750C results show some clustering effect which is not accounted for by the current model, but is being further investigated.

C8.14 Modeling B cluster dissolution in Si and Si0.74Ge0.26.
Ljubo Radic 1, Aracel Lisak 1, Robert Crosby 1 and Mark Edward Law 1
1 Department of Electrical and Computer Engineering, University of Florida, Gainesville, Florida; 2 Department of Materials Science and Engineering, University of Florida, Gainesville, Florida; 3 TCAD, Department, Intel Corporation, Hillsboro, Oregon.

Diffusion behavior of B in silicon can be affected by transient phenomena, such as the transient enhanced diffusion (TED) or formation of the boron-interstitial clusters (BIC). An experiment is performed to determine whether dissolution of BIC is significant. Initially, B implanted Si samples are annealed at 750 °C for 30 minutes. During this anneal, the BICs form and deactivate the large part of implanted B dose, thus providing the cluster-condition. The samples are then subjected to the reactivation anneal at 850 °C for times up to 60 minutes, in an oxidizing or inert ambient. Hall-van der Pauw measurement of the B active dose shows lower activation in the oxidizing or inert ambient. This implies an interstitial release reaction and dissolves a significant cluster species, since the oxidation of silicon is known to inject interstitials. Such a behavior is not predicted by the interstitial poor BICs (e.g. B4I, B3I) as the dominant clusters, which are used in the current models. Also, the reactivation temperature dependence indicates the reactivation is the result of the dissolution of more than one cluster. The initial increase in activation at short times (less than 10 minutes) is observed irrespective of the annealing ambient, while reactivation at longer times is ambient-dependent. A significant cluster species is dissolved by the reactivation anneal at each ambient. The B dissolution reaction is affected by the ambient sensitive reactivation at longer times. Based on these energetics, with B4I and B3I as the two significant cluster species, we have developed a new physically based model that is the first to incorporate the experimentally observed chemical dissolution time and ambient dependence. The model is also tested on an experimental characterization of B clustering in relaxed Si0.74Ge0.26.

C8.15 The effect of varying fluorine implantation energy on boron diffusion in SiGe.
Huada El Mubarek 1, Janet Bonar 1, Peter Ashburn 2, Luen-Chian Sun 1 and Ying-Lang Wang 1
1 Department of Materials Science and Engineering, National Cheng-Kung University, Tainan, Taiwan; 2 Taiwan Semiconductor Manufacturing Company, Tainan, Taiwan.

Recently, fluorine implantation to suppress boron transient enhanced diffusion in silicon has been of great interest in the literature. However, to date there have been no reports of the effects of fluorine on boron diffusion in SiGe. Boron marker layers in SiGe (14% Ge) were grown by Low Pressure Chemical Vapour Deposition (LPCVD) on (100) silicon wafers. Transient enhanced boron diffusion as well as the thermal boron diffusion were separately studied by characterizing the boron diffusion in samples of the same wafer with and without a 288keV, 6x10^13cm^-2 Pt+ implant. The effect of varying the fluorine implantation energy was studied by using two different Pt+ implants. Samples were either implanted with a 36keV, 9x10^14cm^-2 Pt+ implant, which coincides with the peak of the boron in the marker layer, or with a 185keV, 2x10^15cm^-2 Pt+ implant, which coincides with the peak of the Pt+ implant. The samples were either implanted in nitrogen or in argon at a temperature of 950°C for 30s. The Pt+ concentration profiles in crystalline Si and SiGe were obtained on all samples by Secondary Ion Mass Spectroscopy (SIMS). The fluorine implantation was performed at a similar dose and energy (36keV) F+ implant (43%) at the high anneal temperature 1025°C. A greater reduction in boron diffusion due to the high energy (185keV) F+ implant (79%) was obtained at the lower anneal temperature (950°C) compared with (55%) at the higher anneal temperature (1025°C). The annealed fluorine profiles showed an interesting fluorine peak within the SiGe layer coinciding with the boron marker layer. It is proposed that this peak is responsible for the suppression in boron diffusion.

C8.16 Abstract Withdrawn

Wen-Chu Hsiao 1, Chun-Pu Liu 1, Luen-Chian Sun 1 and Ying-Lang Wang 1
1 Department of Materials Science and Engineering, National Cheng-Kung University, Tainan, Taiwan; 2 Taiwan Semiconductor Manufacturing Company, Tainan, Taiwan.

Secondary electron (SE) imaging in a scanning electron microscope (SEM) is used to map out the dopant profiles of metal-oxide-semiconductor (MOS) structures. SE imaging of dopant profiles is used to construct the maps of dopant profiles. Secondary ions exhibit strong contrast due to the high-energy ions compared with the low-energy ions (36keV) F+ implant (43%) at the high anneal temperature 1025°C. A greater reduction in boron diffusion due to the high energy (185keV) F+ implant (79%) was obtained at the lower anneal temperature (950°C) compared with (55%) at the higher anneal temperature (1025°C). The annealed fluorine profiles showed an interesting fluorine peak within the SiGe layer coinciding with the boron marker layer. It is proposed that this peak is responsible for the suppression in boron diffusion.
We present a complete picture of acceptor diffusion in silicon, based on ab initio density-functional-based calculations on the structure, electronic levels, formation and migration energies of the B, Al, Ga, and In acceptors in crystalline Si, and of their complexes with vacancies and self-interstitials. Complexes are known to be responsible for the transient enhancement of dopant diffusivity in implanted Si, a level that is able to control the formation of junctions in Si-based CMOS integrated circuit technology. We find self-interstitial assisted diffusion to be preferred over vacancy assisted mechanisms in all cases, although the two become competitive as the acceptor increases in size. The transient state of the acceptor is unexpected and "anomalous" in several cases: Al and In coupled to a vacancy go off-site forming a vacancy-interstitial complex; the standard self-interstitial/substitutional acceptor complex predicted for B and In is unstable for Al and Ga, which are ejected in the interstitial region and are electrically deactivated as acceptors.

SESSION C9/B9: Joint Session: SiGe Layers
Chair: Wolfgang Windl
Thursday Morning, April 15, 2004 (Moscone West)

8:30 AM C9.1/B9.1
Current Understanding of Diffusion in Strained Si and SiGe
Nicholas Edward Cowern, Advanced Technology Institute, University of Surrey, Guildford, Surrey, United Kingdom.

The introduction of novel device features such as metal gates and bandgap-engineered channels into upcoming CMOS generations has placed the subject of strained Si and SiGe at the top of the materials agenda for silicon-based technology. A key problem in this field is the diffusion and segregation behaviour of host and impurity atoms in the strained material. Much work has been done in the last decade but the subject remains controversial despite fundamental analyses of the role of strain in diffusion from the points of view of thermodynamics, transition state theory and atomistic calculations, and in spite of very extensive experimental investigations. As yet it seems fair to say that there is still no firmly established understanding of stress/strain effects on diffusion. The talk will review recent progress in understanding, emphasizing the key role played by strain fields that intersect surfaces and interfaces where point defects are generated. A new theoretical framework that takes explicit account of surface strain will be outlined, and its consequences for point defects, diffusion and mass transport in non-uniformly strained structures will be considered and compared with the available experimental evidence. Part of this work was performed within the CEC projects IST/2001-34104 ARTEMIS and IST/2000-30129 FIRENDTECH.

9:00 AM C9.2/B9.2
Impact of Buffered Layer Growth Conditions on Growth-In-Vacancy Concentrations in MBE SiGe
Kareem M. Shoukri1, Yaser M. Haddara1, Andrew P. Knights2, Paul G. Coleman3 and Mohammad M. Rahman4; 1Electrical and Computer Engineering, McMaster University, Hamilton, Ontario, Canada; 2Department of Physics, McMaster University, Hamilton, Ontario, Canada; 3Physics, University of Bath, Bath, BA2 7AY, United Kingdom; 4Electrical and Electronic Engineering, Toyama University, Toyama, Japan.

Silicon-Germanium has become increasingly attractive to semiconductor manufacturers over the last decade for use in high performance devices. In order to produce thin layers of device grade SiGe with low concentrations of point defects and well-controlled doping profiles, advanced growth and deposition techniques such as molecular beam epitaxy (MBE) are used. One of the key issues in modeling dopant diffusion during subsequent processing is the concentration of grown-in point defects. There is evidence that under certain growth conditions (e.g. growth at temperatures below 350°C) a supersaturation of vacancies is grown-in. Using positron annihilation spectroscopy (PAS), we have observed the incorporation of vacancy clusters and vacancy point defects in 200nm SiGe/Si layers grown by MBE over different buffer layers. Variables included the type of buffer layer, the growth temperature and growth rate for the buffer, and the growth temperature and growth rate for the top layer. Different growth conditions resulted in different relaxation amounts in the top layer, but in all samples the dislocation density was below 10⁶ cm⁻². Preliminary results indicate a correlation between the size and concentration of the vacancy clusters and the partial relaxation in the alloy layer. At low relaxation percentages of <50%, the vacancy point defect concentration is below the PAS detectable limit of approximately 1x10¹⁵ cm⁻³. As the relaxation is increased to a maximum value of 95%, small vacancy clusters are observed in the SiGe film.

quantum mechanics density functional theory (DFT) calculations. After relaxation, the local vibration modes (LVMs) were determined with the harmonic oscillator approach. Calculations have been performed for N2, VN2 and VN2 (V: Si vacancy), and N2O, VN2O and VN2O with a single or two oxygen atoms (n=1, 2) bridging the Si-Si dilaed bond next to the N-N core. We found that N2 in silicon has two infrared active LVMs for frequencies 771 and 967 cm⁻¹. Several calculations matching 771 and 967 cm⁻¹ FTIR frequencies used to measure [N] in N-CZ Si [1]. Even though not so stable, VN2 has one line 781 cm⁻¹ falling around observed 771 cm⁻¹ frequency. The calculated LVMs for VN2, 619, 627, 638 cm⁻¹, does not match any of the measured FTIR lines. Nevertheless, VN2O and VN2O2 have one frequency 819 cm⁻¹ and 810 cm⁻¹ respectively, close the measured 815 and 806 cm⁻¹ frequencies. This finding corroborates our previous work in which we suggested that V2N2 is a nucleation center for oxygen precipitates [2]. The second group, Ge is rarely gettered by edge dislocation since it has a very small chance to reach the dislocation core. Besides, Ge is not diffusion enhanced by point defects and the role of strain in diffusion is expected to be small. Ge atoms diffuse through a Frank-Read type source and a dislocation type sink.

C8.19
ATOMIC MODELING OF IMPURITY ATOMS IN SILICON AND DISLOCTION LOCKING EFFECT
Abdulmajeed Kasrou, Materials Science and Engineering, North Carolina State University, Raleigh, North Carolina.

A theoretical study of edge dislocation locking by impurities in silicon is presented. Three atom groups have been considered: (i) light O, N, and C, (ii) large Ga, Ge, and As, and (iii) small dopant atoms B, Al, and P. The binding energy of a dislocation with its impurity atmosphere and the shear stress capable of separating a dislocation from its atmosphere were calculated based on an impurity size effect model, for which we had to calculate the dislocation self-energy. Molecular Dynamics on a large atomic system (H terminated Si(001) axis) provided a self energy of 156 meV/A for a clean edge dislocation. Calculated binding energy and separation shear stress showed that the three impurity groups exhibited dissimilar effects of dislocation locking. The O, N, and C radial distributions are similar with slightly stronger occupancy probability for O and N in the vicinity of the dislocation core. These impurities locate themselves at the core of the edge dislocation to which they strongly bind. At a local fraction of 1/4, 1/2, or 3/4, they are spread over a cylinder whose radius reaches 7 neighbors about the dislocation line. The penta-ring and the upper hexa-ring, both in the compressive part of the dislocation domain, are the most likely zones for O localization; whereas the septa-ring, which is in the tensile part of the dislocation, is the zone which is mostly O atoms. Likewise N and C in tetrahedral interstitial positions locate themselves in the compressive side of the dislocation. It was found that carbon is distributed in a more diffuse way than nitrogen and oxygen. From the second group, Ge is rarely gettered by edge dislocation since it has a very small chance to reach the dislocation core. Besides, Ge atmosphere can withstand only 1/3 of the separation stress that the first group can sustain. From the third group, P atoms are not trapped by edge dislocations. Phosphorus atmospheres have a high shear stress resistance to dislocation separation. The temperature dependency of impurity concentration around an edge dislocation was found to have an Arrhenius behavior. As can be seen in Table 1, at local atomic fraction of 1/4, the impurity binding energy with an edge dislocation varies from 0.008 eV/A for P to 1.7 eV/A for N and 1.8 eV/A for O atoms. Table 1: Edge dislocation-impurity binding energy in silicon, for an atomic fraction of 1E-4.

C8.20
Abstract Withdrawn

C8.21
THEORY OF NATIVE DEFECT-ASSISTED DIFFUSION OF ACCEPTORS IN SILICON
Giorgio M. Lopez1, Claudia Melis1, Paolo Schirra1, Paola Alippi2 and Vincenzo Fiorentini1; 1INFN and Dept. of Physics, University of Cagliari, Monserrato, Italy; 2IMM, CNR, Catania.

We present a complete picture of acceptor diffusion in silicon, based on ab initio density-functional-based calculations on the structure, electronic levels, formation and migration energies of the B, Al, Ga, and In acceptors in crystalline Si, and of their complexes with vacancies and self-interstitials. Complexes are known to be responsible for the transient enhancement of dopant diffusivity in implanted Si, a level that is able to control the formation of junctions in Si-based CMOS integrated circuit technology. We find self-interstitial assisted diffusion to be preferred over vacancy assisted mechanisms in all cases, although the two become competitive as the acceptor increases in size. This finding corroborates our previous work in which we suggested that V2N2 is a nucleation center for oxygen precipitates [2]. The second group, Ge is rarely gettered by edge dislocation since it has a very small chance to reach the dislocation core. Besides, Ge is not diffusion enhanced by point defects and the role of strain in diffusion is expected to be small. Ge atoms diffuse through a Frank-Read type source and a dislocation type sink.
Arsenic diffusion in Si and Si$_3$Ge$_2$ alloy, Suresh Upal$^1$, Janet M. Bonar$^2$, Arthur F. W. Willoughby$^1$ and Jing Zhang$^3$

$^1$Materials Research Group, University of Southampton, Southampton, Hampshire, United Kingdom; $^2$Department of Electronics and Computer Science, University of Southampton, Southampton, Hampshire, United Kingdom; $^3$Department of Electrical Engineering, Imperial College, London, United Kingdom.

Results of As diffusion in Si and Si-Ge (10 - $p_\text{thou}$ - Ge) are presented. Using molecular beam epitaxy (MBE), intrinsic delta doped epitaxial Si and compressively strained and relaxed Si-Ge layers were grown on 3 inch substrates. The grown and annealed diffusion profiles were measured using secondary ion mass spectroscopy after rapid thermal annealing (RTA). Arsenic diffusion is clearly enhanced in Si-Ge as compared to Si and the enhancement factor is recorded to be 2 - 3 for 10 - $p_\text{thou}$ - Ge content. The calibrated diffusion coefficient agree well with literature values for both Si and Si-Ge.

Using RTA in O$_2$ atmosphere, interstitials and vacancies have been injected in the sample structures at 1000°C. Diffusion enhancement with vacancy as well as interstitial juctions as compared to an anneal is recorded in Si and Si-Ge structures. The results suggest that both interstitial and vacancy defects contribute to arsenic diffusion in Si and Si-Ge.

Modeling dopants diffusion in SiGe and SiGeC alloys, L. van der Sar$^1$, A. F. W. Willoughby$^1$, R. J. L. Martin$^1$, T. W. H. van Dijk$^1$, J. A. M. van der Velden$^1$, P. F. J. van der Walt$^1$, M. J. W. van den Berg$^1$, J. M. Bonar$^2$, and A. F. W. Willoughby$^1$.

In this work, a unified physical model of dopants diffusion in SiGe and SiGeC alloys is proposed, based on the hypothesis that the different effects introduced by dopant incorporation and the nature of the alloy matrix modify the equilibrium concentrations of interstitials and vacancies from their standard value in pure Silicon. The primordial role of point defects in dopant diffusion is admitted and the evolution of substitutional atoms diffusivity is described by their concentration variation. The critical analysis of bibliographic studies allows the description of involved physical phenomena: the chemical effect in covalent alloys, the effect of strain and the Fermi-level effect, act on the equilibrium diffusion of Boron in shallow epitaxial SiGe and SiGeC strained and relaxed layers. All reliable and previously published experimental data is analyzed for the calibration of the model physical parameters. Finally, the equilibrium diffusion of Boron in shallow epitaxial SiGe and SiGeC layers is measured and successfully confronted to the unified diffusion model. For the first time, experimental studies of Arsenic equilibrium diffusion are performed, showing an important diffusivity enhancement with Ge and C content of SiGeC strained layers, confirming model predictions for the Vacancy-mediated diffusion.

Athermal Ge-migration during junction formation in s-Si layers grown on SiGe buffers, Juan A. Marques$^1$, Ivan Santos$^1$, Maria Aboy$^1$, Juan Barbolla$^1$, Luis A. Marques$^2$, Iván Santos$^2$, Maria Aboy$^2$, and Juan Barbolla$^2$.

Solid phase epitaxial regrowth (SPER) has been proven to be highly advantageous for ultra shallow junction formation in advanced technologies. Application of SPER to strained Si/SiGe structures raises the concern that the Ge may outdiffuse during the implantation and/or anneal step and thus reduce the strain in the silicon. In the present studies we explore the 8 nm strained silicon wafers to implant conditions that are characteristic for formation of the junctions by solid phase epitaxial regrowth (SPER) and conventional spike activation. We investigated the SIMS of as-implanted wafers to the conditions that are characteristic for formation of the junctions by solid phase epitaxial regrowth (SPER) and conventional spike activation and measure the resulting Ge redistribution using SIMS.

We have studied the dose and energy dependence of this athermal redistribution process by using As implants (2 - 15 keV, 3 x 10$^{14}$ - 3 x 10$^{15}$ at/cm$^2$) such that the location of the implants species relative to the Ge-edge could be determined by SIMS as well. It is shown that the energy of the implant species or more specifically the position of the damage distribution function relative to the Ge-edge (as deduced from RBS-channeling experiments) plays a determining factor with respect to the Ge-migration. For implants whereby the damage distribution overlaps with the Ge-edge a very efficient transport of the Ge is observed, even prior to any anneal cycle. The migration is entirely correlated to the collisional mixing effects as demonstrated by Monte Carlo simulations using SRIM. The scaling with dose for a given energy links the observed Ge-profile with a broadening mechanism related to the number of atom displacements induced in the sample. The Ge redistribution originating from additional anneals after the implant step (or even before the implant) was also studied and is shown to be far more important as compared to the collisional mixing effects. The latter clearly supports the concept an athermal Ge-migration caused by the amorphizing implant. The observed redistribution implies that the use of the SPER process for junction formation in s-Si/SiGe inevitably leads to a strong Ge-redistribution and a corresponding loss off strain in the Si-layer. A careful engineering of the amorphization process (such as using low dose multiple energy implants) may be required to limit the migration process.
agglomerates of IV pairs, whose recrystallization rate depends on the local density of these defects. The local excess or deficit of oxygen according to the environment affects the recrystallization rate. In sub-amorphizing implants amorphous pockets are disconnected and when they recombine, they leave behind the local excess of Si interstitials and vacancies. When a continuous amorphous layer initially extends to the surface, the excess or deficit atoms are swept towards the surface during the regrowth. The atomic model describes the main features of the crystalline to amorphous transition and the defect evolution during the regrowth. The surface concentration and parameters are used for the non-amorphizing and amorphizing implants, and amorphization is the result of the simulation itself.

11:00 AM C10.2


In recent years interest has increased significantly in preamorphization and low-temperature recrystallization techniques to produce highly steep ultrashallow junction profiles with above-equilibrium levels of dopants. However, during solid phase epitaxial regrowth (SPER) complex physical phenomena occur that require careful consideration. Mismatched dopant diffusion at the amorphous-crystalline interface, as well as stress, influence the recrystallization rate, allowing the B atoms to diffuse very slowly when in amorphous Si, during low-temperature thermal annealing. Diffusivity that is several orders of magnitude higher than the value present in crystalline Si was observed at the amorphous-crystalline interface during regrowth. Previous studies have shown that movement at room temperature is isolated to the boron tail region, while no increases in motion are observed during the regrowth process. Maximum boron diffusion is exhibited when the projected range of the boron implant coincides with the tail region of the boron concentration profile. Rearrangement of boron occurs at depths shallower than the tail region, while no increases in motion are demonstrated as the boron projected range moves deeper than the boron profile. Fluorine enhanced diffusion at room temperature does not appear to follow the same process as the enhanced diffusion observed during the regrowth process.

11:30 AM C10.4

The role of stress on the shape of the amorphous-crystalline interface and mask-edge defect formation in ion-implanted silicon. Carrie E Ross and Kevin S. Jones; Materials Science and Engineering, University of Florida, Gainesville, Florida.

Stress is known to affect the regrowth velocities during recrystallization of an amorphous layer. This study investigates how the stress from patterned structures alters the regrowth and in turn affects defect formation. Prior to patterning, 80 A SiO2 and 1540 A of silicon nitride were deposited on a 200 mm (100) silicon wafer. A 40 keV Si+ amorphizing implant at a dose of 1x1015/cm 2 was then performed into the patterned wafer. The regrowth of the amorphous layer along the mask edge was studied by partially recrystallizing the layer for various times at 550 ºC both with the mask present and with etching off the oxide and nitride pads. A significant number of cross-sectional Transmission Electron Microscopy (TEM) samples were prepared and imaged. It was found that the stress from the patterned structures enhances the vertical and lateral regrowth velocities by 15% and 12% respectively, as well as alters the shape of the amorphous-crystalline interface during regrowth. Previous studies have shown that uniaxial tensile stress increases the regrowth velocity. FLOOPS simulations have shown that the region of interest in these samples is under tensile stresses, suggesting that this type of stress should accelerate the regrowth growth velocity. The enhancement in the lateral regrowth velocity was not expected. In addition for certain geometries diocclusion half-loops are observed to form along the mask edge. These defects arise during regrowth and are directly affected by the film stress. The relationship between the stress from the patterned structures, the regrowth of the amorphous layer, and the formation of dislocation half-loops along the mask edge will be discussed.

11:45 AM C10.5

Channel engineering and junction overlap issues for ultra-shallow junctions formed by SPER in 45 nm CMOS technology nodes. Simonsen Severi 1, Kirkland Henson 1, Kristin De Meyer 2, Kristine Lindsay 1, Anne Launere 3,4, Radu Surdeanu 1,3, and Kristin De Meyer 1,2; 1SPDT/DIP, IMEC, Leuven, Belgium; 2ESAT/INteLSYS, K.U. Leuven, Leuven, Belgium; 4Philips Research, IMEC, Leuven, Belgium.

The necessity to control the Short Channel Effects (SCE) for the 45 nm technology node and beyond requires the complete suppression of dopant diffusion in order to control the lateral and vertical depth and the abruptness of the junction profile. It is known that junctions formed by Solid Phase Epitaxial Regrowth (SPER) of a doped amorphous layer allow for meta-stable high activation level and perfectly abrupt profiles. The excellent abruptness of SPER junction formation from a poor activation level results in an improved activation level in the amorphous region. Despite the excellent vertical junction profile, several integration issues arise from the lateral amorphisation and from the End of Range (EOR) defects. In the present work we present an experimental analysis of the lateral dopant and defect profile obtained by this low thermal budget process is presented through electrical pMOS and nMOS transistors characterization. We observe a strong dependence of the lateral amorphous region profile near the gate on the implantation parameters used. Unless optimized this leads to poor doping active concentration under the gate that significantly increases the overlap resistance. Through a SPER extension process only, substitutional combinations of Ge, As, or BF2 and B for P and As for NMOS have been characterized for transistor performance. Under the correct conditions, the transistor performance can be recovered if compared to the spike annealed reference. An optimised SPER junction can preserve the oxide-isolating and avoid the degradation of the poly. The issue of HALO deactivation in the EOR region is
studied in detail through capacitance measurements and threshold voltage roll-off. It is shown that the degradation in the SCE control can be recovered with NMOS and PMOS samples. Superior control on the short channel behaviour is observed with SPER junctions compared to the equivalent resistance spike annealed reference.

SESSION C11: Characterization Techniques
Chair: Alain Claverie and Wilfried Vandervorst
Thursday, April 15, 2004
Room 2002 (Moscone West)

1:30 PM C11.1
Two-dimensional carrier profiling quantitatively measuring invisible dopant concentrations: a non-motor scanning-reflectron microspectroscopy.
Wilfried Vandervorst1, Pierre Eyben1, duhyoun Natasha1, Marc Foucher1 and David Alvarez1,2

Two-dimensional carrier profiling in semiconductors is one of the most demanding metrology tasks (presently still labeled red in the International Technology Roadmap for Semiconductors), as one needs to combine extreme spatial resolution (l 1 nm), with very high concentration sensitivity (5 %), a large dynamic range (5-6 orders of magnitude) and an excellent quantification accuracy (3%). Among the potential candidates (Scanning Capacitance microscopy, Electron holography, Holographic Microscopy, Scanning Resistivity Microscopy (SSRM)) has evolved recently towards a performance level closely meeting the ITRS-targets. Recently a tip-technology has been developed based on moulded solid diamond tips, which provide an optimum pyramidal tip shape and fine tip radius such that a drastically improved spatial resolution can be obtained. Based on dedicated spatial resolution test structures (sandwiched buried oxides, dopant spikes...), it is shown that with these tips SSRM achieves a spatial resolution better than 1 nm. Dopant gradients as steep as 1-2 Angstroms nm/dec have been measured as well. This excellent spatial resolution is combined with straightforward quantification and excellent sensitivity (over the entire dopant range) such that cross correlation with process simulators becomes feasible and details of the Vt-adjustment can be studied. Moreover, in order to infer atomic structure of the defects/discharges, the generation mechanism, and its behavior in a stress field for large area images, patterned multifile simulations using MPI (Message-Passing Interface) have been developed. Using the simulation analysis of discharges, we have performed on B+ implanted Si wafers. In this paper, the simulation method and the results are reported. The code for dislocation identification, well-established two-beam TEM procedures for modeling metal and alloy structures are basically adopted. The Hoeve-Whelan differential equations have been solved. Integration of the electron beam intensity is performed across the entire specimen, taking into account atomic displacements due to defects/discharges. For molecular dynamics simulations of dislocations, speed-up of calculation is the most important issue since large numbers of Si atoms in the range of 108 to 1012 are needed. We have parallelized a molecular dynamics simulator using MPI in the PC cluster system. Additionally, we have modified the simulation algorithm using a well-optimized cell-subdivision method. Using the improved code, more than 107 silicon atoms can be treated in the simulator. Among various examples which we have done, we call upon herein a silicon SOI transistor and FinFET devices were performed. Excellent agreement between effective channel lengths as determined with SSRM versus electrical performance of SOI-devices could be demonstrated, allowing to predict based on the measured underdiffusion, that for that particular technology a 50 nm (physical gate length) transistor would be totally shortened. Effective channel lengths as small as 15 nm could be discerned. Recently we also have applied SSRM to (strained) Si/SiGe-based CMOS structures and were able to deduce the different diffusion characteristics in the Si and the SiGe-layers for each of the three silicon areas examined (5-10 nm). In this paper we will also make a comparison to SCM results (as obtained on the resolution test structures) and electron holography on CMOS-transistors. 

2:00 PM C11.2
Lateral Dopant Profile Metrology using Carrier Illumination. Edward Budzarta, Peter Borden, Susan Fish and Houda Gnour;
Applied Materials, Santa Clara, California.

As CMOS device scaling continues into the sub-100nm regime, the precise control of source/drain extension (SDE) lateral diffusion and dopant profile overlap under the poly-silicon gate has become increasingly critical, directly impacting the transistor saturation drive current. The SDE gate overlap is typically achieved by dopant lateral diffusion during the rapid thermal annealing (RTA) process following the SDE implant. As device dimensions continue to shrink, it becomes necessary to produce <30nm vertical SDE junctions which may require a diffusion-less dopant activation process such as Laser Annealing. Without lateral dopant diffusion, a high tilt-angle implantation may be employed to produce the desired amount of SDE gate overlap. Either approach requires a highly sensitive measurement technique capable of monitoring the SDE gate overlap during processing. This paper describes the application of the Carrier Illumination (CI) technique to conduct such measurement. CI is a non-destructive optical interference technique for measuring the dopant profile depth of ultra-shallow junctions with <2 angstrom resolution. The CI signal from a patterned layer of doped and undoped lines is a linear superposition of individual signals from the fully doped and fully undoped regions, enabling determination of the line dimensions. Furthermore, the extent of implant lateral straggling or the impact of any tilt-angle implant can be measured by comparing the implant mask dimensions to the pre-anneal CI measurement of the width of the implanted regions. Similarly, the extent of dopant lateral diffusion after annealing can be measured by comparing the as-implanted dimensions to the post-anneal CI measurement of the final width of the doped regions. Experimental results on test structures implanted with Boron at implant angles of 0 to 30 degrees and then spike-annealed at temperatures from 950 to 1100 degrees C will be discussed.

2:15 PM C11.3
Highly Parallelized Molecular Dynamics Simulation of Silicon Dislocation Behavior and Dislocation Identification Based on Two-beam Theory. Takako Oda1, Toshihiko Yoko2, Masanobu Kawanaga3, Yasuyuki Kikumagawa4, Kunio Onda4, Shinji Sugiyama3, Ann Marshall3, Kyongjoe Cho4 and Robert W. Dutton5,6; 1Corporate Research & Development Center, Toshiba corporation, Kawasaki, Kanagawa, Japan; 2Toshiba I. S. corporation, Kawasaki, Kanagawa, Japan; 3Information Systems Center, Toshiba corporation, Kawasaki, Kanagawa, Japan; 4Laboratory for Advanced Materials, Stanford University, Stanford, California; 5Department for Mechanical Engineering, Stanford University, Stanford, California; 6Center for Integrated Systems, Stanford University, Stanford, California.

During the fabrication of a silicon integrated circuit, defects and dislocations are often generated in the silicon substrate. Once present in the substrate, dislocations can lead to leakage that degrades performance. Understanding of the dislocation characteristics and generation criteria is an indispensable aid in robust process design for silicon devices. To facilitate of quantitative discussion of TEM images, a computer code for identification of defects and dislocations was developed. Using the code one can identify the Burgers vector and its direction which is otherwise invisible on TEM photos. Among various kinds of silicon defects and dislocations, the morphology can be specified.

Moreover, in order to infer atomic structure of the defects/dislocations, the generation mechanism, and its behavior in a stress field for large area images, patterned molecular dynamics simulations using MPI (Message-Passing Interface) have been developed. Using the simulation analysis of dislocations, we have performed on B+ implanted Si wafers. In this paper, the simulation method and the results are reported. In the source code for dislocation identification, well-established two-beam TEM procedures for modeling metal and alloy structures are basically adopted. The Hoeve-Whelan differential equations have been solved. Integration of the electron beam intensity is performed across the entire specimen, taking into account atomic displacements due to defects/dislocations. For molecular dynamics simulations of dislocations, speed-up of calculation is the most important issue since large numbers of Si atoms in the range of 108 to 1012 are needed. We have parallelized a molecular dynamics simulator using MPI in the PC cluster system. Additionally, we have modified the simulation algorithm using a well-optimized cell-subdivision method. Using the improved code, more than 107 silicon atoms can be treated in the simulator. Among various examples which we have done, we call upon herein a silicon SOI transistor and FinFET devices were performed. Excellent agreement between effective channel lengths as determined with SSRM versus electrical performance of SOI-devices could be demonstrated, allowing to predict based on the measured underdiffusion, that for that particular technology a 50 nm (physical gate length) transistor would be totally shortened. Effective channel lengths as small as 15 nm could be discerned. Recently we also have applied SSRM to (strained) Si/SiGe-based CMOS structures and were able to deduce the different diffusion characteristics in the Si and the SiGe-layers for each of the three silicon areas examined (5-10 nm). In this paper we will also make a comparison to SCM results (as obtained on the resolution test structures) and electron holography on CMOS-transistors. 

2:30 PM C11.4
Direct observation of thermal vacancies in highly n-type Si.
Ville Runki and Kimmo Saarinen; Laboratory of Physics, Helsinki University of Technology, Espoo, Finland.

The thermal vacancies in Si have escaped the direct experimental observation, despite their fundamental and technological importance. Hence their basic thermodynamic properties as the formation energies have been unknown. In this paper we report experimental observation of thermal vacancies in Si. The vacancies are created by thermal annealing and observed as quenched to vacancy-impurity complexes in highly As and P-doped Cz Si. The density of atomic structure of vacancy-impurity complexes as measured by electron irradiation was found to be typically in highly n-type Si can be experimentally determined by combining positron lifetime and electron momentum distribution measurements [1]. The monovacancy surrounded by three As atoms (V-As3) is the dominant vacancy-impurity complex in Czochralski grown highly n-type Si with a density of about 1020 cm-3. By studying the annealing of V-As complexes formed by electron irradiation, we can show that the V-As3 complexes are formed as a result of the subsequent migrations of V-As and V-As3 [2]. In the experiments we create thermal vacancies by annealing highly As and P doped Si at 900 - 1100 K. After the
annealing we observed increased concentrations of vacancy defects and identify that the vacancies are surrounded by three As or P dopants. We also oxidize thermal vacancies to be trapped by impurities, and form the V-As$_3$ and V-P$_3$ complexes by migration similarly as in electron irradiated Si [2]. These results provide useful feedback on thermal vacancies and explain the formation of transition complexes during the growth. A preliminary estimate of about 2 eV can be deduced for the vacancy formation enthalpy in highly n-type conditions where the Fermi level is close to the conduction band. This estimate is in good agreement with those of other workers [1, 2]. Defects generated by ion implantation can modify these parameters. Solid Phase Epitaxial Regrowth (SPER) is considered as a promising doping technology to provide solutions for highly-activated, shallow, and abrupt dopant profiles for sub 65nm CMOS technologies. However the principal drawback of this method is the high density of defects. Under certain conditions, these defects can generate a local space charge region, reorganize the carrier distribution and deactivates dopant. This raises a question about the perturbations of electrical characterizations due to the presence of a large defect band after SPER. The aim of this work is to evaluate the effect of these defects on the electrical properties of the material. The measurement of these properties will allow to determine the quality of the material. We will show results from Nano-SRP measurements on p+ / n junctions made with different preamorphization conditions. The results strongly depend on the position of the damage area: the electrical junction disappears when the defects are located in the space charge region. To investigate these interactions further we realized a well targeted CVD regrowth. A preliminary estimate of about 2 eV can be deduced for the activation level of the CVD with or without thermal annealing. We are using the latter as a metric of the quality of the CVD process. The implanted region also shows optical properties similar to amorphous silicon as determined by variable-angle scanning ellipsometry (VASE). Other electrical measurements, such as capacitance-voltage and sheet resistivity, show changes characteristic of implantation damage. We have assumed a model for which the implanted region has optical and electronic properties similar to amorphous silicon. In this work, we correlate the surface lifetime of implantation damage with the optical properties acquired with VASE measurements. The lifetime increases with various annealing processes, and the optical constants approach those of amorphous silicon. We will correlate the lifetime changes with the measured optical spectra for a variety of annealing conditions. We will also show data for the sheet resistance and the correlations with the surface lifetime. For the fully activated implantation layer, the device structure acts to produce charge separation, and the lifetime may become larger than the original bulk lifetime. In this case, the photoconductive decay time of the annealed structure is shown to be related to the leakage current in the finished device. In summary, we will present a protocol for quickly evaluating the effectiveness of various implantation annealing processes.

3:00 PM C11.8


Rapid thermal annealing (RTA) is required to heal the lattice damage created by heavy ion implants such as boron or arsenic. The RTA process maintains the structural integrity of the semiconductor used for submicron-integrated circuits. Quick, efficient, and contactless diagnostics of the implantation damage are highly desirable in both research and production environments. A new measurement technique has been applied to this problem and correlated with other diagnostics. The resonant-coupled photoconductivity decay (RCPCD) technique uses a deeply penetrating, low-microwave-frequency probe in conjunction with a variable-wavelength pulse from a tunable laser source. The recombination lifetime of the implanted region decreases many orders of magnitude after implantation. The crystallinity is restored by RTA, and the degree of restoration varies with the details of the RTA process. We are looking at efficient ways of assessing the efficiency of various processes for removing damage. The damage is then assessed in a sharp decrease in the lifetime when using strongly absorbed light. This damage strongly affects the surface lifetime, which is the lifetime measured using strongly absorbed light. The as-implanted layer acts as a sink for minority carriers, and the surface lifetime becomes very small after the lattice damage of the implantation damage ameliorates. The implanted region also shows optical properties similar to amorphous silicon as determined by variable-angle scanning ellipsometry (VASE). Other electrical measurements, such as capacitance-voltage and sheet resistivity, show changes characteristic of implantation damage. We have assumed a model for which the implanted region has optical and electronic properties similar to amorphous silicon. In this work, we correlate the surface lifetime of implantation damage with the optical properties acquired with VASE measurements. The lifetime increases with various annealing processes, and the optical constants approach those of amorphous silicon. We will correlate the lifetime changes with the measured optical spectra for a variety of annealing conditions. We will also show data for the sheet resistance and the correlations with the surface lifetime. For the fully activated implantation layer, the device structure acts to produce charge separation, and the lifetime may become larger than the original bulk lifetime. In this case, the photoconductive decay time of the annealed structure is shown to be related to the leakage current in the finished device. In summary, we will present a protocol for quickly evaluating the effectiveness of various implantation annealing processes.

4:15 PM C11.9

Novel, non-contact mapping metrology for ultra-shallow junction sheet resistance and leakage current. Michael Ira Current, Vladimir Faier, Phuc Van, Wojtek Walecki, S. H Lau and Ann Koo; Frontier Semiconductor, San Jose, California.

Production controls for ultra-shallow junctions requires in-line methods for measurements of sheet resistance in the range from 100 to 900 Ohm/square for junction depths in the range of 30 to less than 10 nm (according to the ITRS03 requirements). Physical probing methods are limited by effects such as junction penetration, probe current heating and leakage current induced errors in sheet resistance measurements. Optical interference and reflection methods give structural information on junction depth and doping density, but do not have limited or no sensitivity to electrical activation of shallow junction dopants. This paper describes a novel, non-contact method for determination of ultra-shallow junction sheet resistance and leakage current density which combines pulsed photo-generation of surface carriers with analysis of amplitude and phase signals from capacitance probes. At light pulsing frequencies of about 10 kHz, the surface voltage signal gives a direct measure of the junction sheet resistance, independent of the injection depth. At high pulsing frequencies, the junction leakage current density is determined. This method provides for direct monitoring of sheet resistance in the range from 50 to 10,000 Ohms/square and junction leakage current densities in the range from 10-6 to 10-3 A/cm2. Coupling this capacity to the monitoring of pulsed photo-generated free carriers with a precision wafer motion stage allows for rapid acquisition of sheet resistance and leakage data for efficient wafer-scale mapping applications. Examples of the use of this novel non-contact mapping metrology for electrical characterization of ultra-shallow junctions, including a variety of
implant and pulsed heating anneal techniques, will be described.

4:30 PM C11.10
XAFS as a Direct Local Structural Probe in Revealing the Effects of C Presence in B Diffusion in SiGe Layers.
Mehmet Alper Sahiner1, Parviz Ansari2, Malcolm S. Carroll2, Charles W. Magee3 and Joseph C. Woclawik2, 1Seton Hall University, South Orange, New Jersey; 2Sandia National Laboratories, Albuquerque, New Mexico; 3Evans East, East Windsor, New Jersey; 4NIST, Gaithersburg, Maryland.

The local structural information around the germanium atom in boron doped SiGe alloys is important in understanding the dopant diffusion mechanisms. Epitaxial SiGe test structures with B markers were grown on Si substrates by using rapid thermal chemical vapor deposition (RTCVD). In these structures, C was also incorporated with various concentrations. The local structure around the Ge atom was probed using Ge K-edge x-ray absorption fine structure spectroscopy (XAFS) to determine the effects of the C and B on the Ge site. The concentration profiles obtained from secondary ion mass spectroscopy are correlated with the Ge XAFS results. The modifications on the local structure around the Ge atoms are revealed from the multiple scattering analysis on the Ge near neighbors. The trapping mechanism for the B diffusion due to the presence of the C atoms will be discussed using the SIMS concentration profiles and these local structural changes.

4:45 PM C11.11
On the diffusion of interstitial Fe in Si1-xGe x alloys.
Gerd Weyer1,2, H.P. Gunnnlaugsson3, K. Bharuth Ram4, M. Dietrich2, R. Mantovan5, D. Naidoo3 and R. Sielemann4; 1Department of Physics and Astronomy, Aarhus University, Geneve 23, Denmark; 2EP Division, CERN, CH-1211 Geneva 23, Switzerland; 3School of Pure and Applied Physics, University of Natal, 4041 Durban, South Africa; 4Hahn-Meitner Institute, D-14109 Berlin, Germany; 5Laboratorio MDM-INFM, 20042 Agrate Brianza, Italy.

Among the transition metal impurities in silicon Fe and interstitial Fei in particular can be said to be the best studied. The detrimental role of Fe in devices is due to a large extent to a deep donor state in the band gap and a fast diffusivity, which in silicon is different by more than an order of magnitude at low temperatures for neutral and positively charged Fei0+/+. Recently, the diffusivity of Fei0+ in Si1-xGe x for x<0.1, measured for an ensemble of jumps, was found not to be affected by alloying with Ge, whereas the donor state shifts towards the valence band [1]. Here we report on the observation of diffusional jumps of Fei0+ on an atomic scale by means of the resulting line broadening in their Mössbauer spectra, which is directly proportional to the jump frequency. Radioactive 57Mn ions (T1/2=1.5 min.) were implanted at the ISOLDE facility into bulk and epitaxially grown Si1-xGe x alloys (x<0.08) with 60 keV energy to fluences <1017/cm2. The crystals were held at 500-800 K. The radiation damage from the implantation of single ions is known to anneal at these temperatures during the 57Mn lifetime and the 57Mn probe atoms are incorporated on substitutional lattice sites. An average recoil energy of 40 eV, imparted on the 57Fe daughter atoms in the nuclear decay to the 14 keV Mössbauer state, expels the majority into tetrahedral interstitial sites. A few diffusional jumps of the interstitial 57Fe0+ atoms during the lifetime of the Mössbauer state (140 ns) lead to a line broadening and eventually to the formation of Fei0+/V pairs with the vacancy created in the recoil process. Thus determined jump frequencies were found to increase in Si1-xGe x with increasing x. The implications of this effect for the purely interstitial Fe diffusion mechanism as well as conclusions from a comparison to the unaffected “macroscopic” diffusion, as determined in ref. 1, will be discussed. It is noteworthy that the Fei0+/+ diffusivities in pure silicon determined by, respectively, similar techniques in ref. 1 [2] and by analogous Mössbauer experiments as the present [3] are in very good agreement for both charge states.