SYMPOSIUM D

High-k Insulators and Ferroelectrics
for Advanced Microelectronic Devices

April 12 - 16, 2004

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* Invited paper
The scaling of the gate dielectric in the future generations of MOS (Metal-Oxide-Semiconductor) devices is recognized as a major issue in the field of microelectronics. Consequently, tremendous research efforts have been focused in recent years to the investigation of high-k gate dielectrics for the potential replacement of silicon dioxide in MOS devices. One of the key issues concerns the characterization and understanding of the electrical properties of these structures. After a general introduction to the field, the electrical characteristics of these devices will be described in details. Issues such as threshold voltage control and instabilities, mobility degradation, charge trapping, defect generation and ion transport in high-k gate stacks, device lifetime and dielectric breakdown, and negative and positive bias temperature instabilities will be covered. Our current understanding of these properties will be emphasized. Based on these results, possible future directions in the field (including high mobility substrates, metal gates, etc.) will be discussed.

Instructor:
Michel Houssa, IMEC

SESSION D1: Atomic Layer Deposition of High-k Dielectrics

Chairs: Jamie Schaeffer and Bob Wallace
Tuesday Morning, April 13, 2004
Room 2006 (Moscone West)

8:30 AM D1.1 Recent Developments in Understanding Local Effects and Device Properties of HF-based High-k Dielectrics. Glen Wilke1, Dave Muller2 and Jan Willem Moes1; 1 ASM America, Phoenix, Arizona; 2 Department of Applied and Engineering Physics, Cornell University, Ithaca, New York.

Atomic scale electron spectroscopy is used to determine the local electronic structure of atomic layer deposited HfO2 gate dielectrics as a function of annealing conditions. Oxygen core-loss spectra from monocrystalline samples exhibit a more strongly pronounced crystal-field splitting with increasing anneal temperature up to 1000°C, consistent with a decrease in point defects. Concomitantly, electrical measurements of the same structures show a correlated reduction of fixed charge. An unintentional 5 A SiO2 layer is observed at the top interface, between the HfO2 and poly-Si electrode. No Hf-silicate intermixing is detected at either interface on a scale down to 2 A. In addition, improved understanding of the nucleation and growth behavior of ALD HfO2 and HfSiO(N) has led to well-engineered interfaces, thus allowing smaller incubation times for HfO2 growth. With these tailored dielectric stacks, much improved transistor characteristics have been achieved, including higher carrier mobilities and higher drive currents for both high-performance and low standby-power devices.

9:00 AM D1.2 The growth kinetics of HfO2 films on Si (100) grown by atomic-layer deposition using in-situ medium energy ion scattering. Hyo Sik Chang1, Hyunsang Hwang1, Mann-Ho Ch0 2 and Dae Won Moon3; 1Department of Materials Science and Engineering, Kwangju Institute of Science and Technology (KJIST), Gwangju, South Korea; 2Nano Surface Group, Korean Research Institute of Standards and Science (KRISS), Daejeon, South Korea.

The growth kinetics and initial growth stage of HfO2 films on p-type Si(100) grown by atomic-layer deposition (ALD) using HfO2 films on Si substrates was examined in relation to the film thickness, substrate temperatures, and surface states of the Si substrates. Interfacial reaction between Si and Hf at the initial growth stage was occurred and significantly depended on the surface state of the Si. The HfO2 film with an amorphous structure was grown on the oxidized Si substrate at an initial growth stage. In particular, the interfacial layer thickness and the stoichiometry of the layer were dependent on the surface state of Si substrate. The physical analysis of the films with XPS and TEM also supported the interfacial reactions. Based on the interfacial reaction at the initial growth stage, we suggested the model for the interaction between Si and Hf at the initial growth stage in relation to the atomic size, bonding characteristics, and formation energy. This study will be helpful to understand the interfacial reactions at the initial growth stage and to control the reactions for the application of high-k dielectrics.


Thin films deposited via atomic-layer deposition show to be less dense than the bulk material. Densification typically requires high temperature post deposition annealing that may violate the thermal budget of a sensitive process. We have found that modulated temperature annealing of pulse deposited films at 200–450°C results in a very high density without elevated temperature anneals are performed after every n deposition cycles, results in film densification. HfO2 films were deposited via a dual metal precursor technique in which alternating pulses of HfCl4 and Hf3O4 are separated by N2 purges. Rapid thermal anneals (30 sec at approx 420°C in N2) were performed after every n deposition cycles where n ranged from one to the total number of cycles. Films were characterized via ellipsometry, x-ray diffraction, x-ray reflectivity, capacitance vs. voltage, current vs. voltage, and limited TEM. Film thickness and deposition rate / cycle were found to decrease and film density was found to increase with decreasing anneal interval (more frequent annealing). Using interval annealing, we were able to "tune" the density of HfO2 thin films from 7.7 (for samples annealed only at the end of the deposition) to 10 g/cc. It was found that the highest density films (10 g/cc) can be achieved only by every-cycle annealing. Densification was likely due to the removal of unreacted ligands that remain after a deposition cycle is complete. Consistent with the film density results, it was found that the refractive index of the films ranged from 1.9 for the samples annealed only once to about 2.2 for every-cycle annealed samples. For films annealed every cycle, XRD results indicate the appearance of additional crystallization phase. Films annealed every cycle and every other cycle demonstrated improved behavior in dielectric properties. Films annealed every cycle were shown to have a reduction in interfacial layer thickness from 1.1 nm to 0.5 – 0.6 nm. The level of densification and improvement of electrical properties observed in the every cycle annealed films could not be achieved by post deposition annealing.

9:30 AM D1.4 ALD Grown Lutetium-Based Oxides for Gate Dielectric Applications. Giovanna Scarl1, Sabina Spiga1, Gabriele Seguini1, Claudia Wiemer1, Igor Fedchuk2, Herbert Schumann3, Andrei Zenkevitch2 and Yuri Lebedinski4; 1Laboratorio MDM, INFN, Agrate Brianza, Italy; 2Institut fuer Chemie, TU Berlin, Berlin, Germany; 3Physics of Solids, Moscow Engineering Physics Institute, Moscow, Russian Federation.

Rare earth oxides could represent a valuable alternative to SiO2 in CMOS devices. In particular, LuO3 is proposed because the calculated x only in the range between 12-13, it is predicted to be thermodynamically stable on silicon with a high (> 2 eV) conduction band offset (CBO), expected as a consequence of three factors. (i) The large band gap, related to the completely filled 4f shell of Lu, (ii) the possibility of only one oxidation number (3), which avoids mixed Lu oxide stoichiometries with different electronic structures, and (iii) the 2.3 metal oxygen stoichiometry ratio which promotes a low value of the charge neutrality level and hence a high CBO at the oxide/silicon interface. In addition, low density of interfacial traps are predicted for Lu2O3 due to the intrinsic high energy of the 5d shells and their low occupancy (only one electron) in Lu. Lu silicates are also promising candidates due to their predicted thermo-dynamical stability on Si, acceptable CBO, and, moreover, silicates have a higher crystallization temperature than the corresponding oxides. To assess the quality of Lu-based oxides, Cpx(Me3Si) and Cpx3N2 ligands were synthesized and bound to Lu atoms to form volatile and nonmonomeric complexes. These complexes were used as Lu precursors during atomic layer deposition (ALD) in a temperature range between 250 and 280 °C of Lu-based oxides, Cpx and Cpx3N2 as source gases. The chemical reactions and structural, and morphological analysis revealed that the ALD Lu(Cp(Me3Si)3)2/H2O process gave rise to a stoichiometric, polycrystalline, and quite rough (rms smoothness of about 2.7 nm for a 1.9 nm thick film) Lu2O3 layer. In particular, x-ray diffraction and Fourier transform infrared spectroscopy analyses identified respectively the cubic Ia3 structure with a lattice parameter of 1.034 nm and absorption bands at 304 cm-1, 340 cm-1, and 385 cm-1, similar to those of cubic Y2O3. On the other hand, the ALD Lu(Me3Si)2N3/H2O and Lu(Me3Si)2N3/H2O processes produced amorphous layers of a form of Lu-silicate, as revealed from Rutherford back-scattering analysis and x-ray photoelectron spectroscopy (XPS) measurements. The evolution of the Lu and O chemical states in both the Lu2O3 and in the Lu-silicate layers is
monitored with XPS upon annealing in O2 and vacuum at 750 °C and 950 °C, respectively, and the band energy positions of La2O3 and La2O3 films layer by layer, indicating a remarkable thermal stability. MOS capacitors were fabricated by Al thermal evaporation through a shadow mask. The k value measured in the 10-300 kHz frequency range for as-grown La2O3 and Lu2O3 was remarkably larger than 12-17 and 7-8. CV curves revealed positive and flat band and hysteresis in both La-based oxides. Interface state density is found to be of the order of 1.10eV-1 cm-2, with a remarkable increase for the Lu-silicate films grown using O3 as oxygen precursor.

9:45 AM DL15
Optimization of ALD grown HfO2 properties based on a novel precursor combination including Hf(OtBu)2 (mpmp)2 and HfC14, Giovanna Scarel, Sabina Spiga, Claudia Wiemer, Grazia Tallarida, Emiliano Bonera, Sandra Ferrari and Marco Fasciulli; Laboratorio MDM, INFN, Atrage Brinza, Italy.

HfO2 as well as Hf silicates and amalldates are among the most promising candidates to substitute SiO2 as active dielectrics in CMOS-based devices. In this work we study the combination of the monomeric and metal-oxide-sensitive Hf(OtBu)2 (mpmp)2 precursor with HfC14 for the growth of HfO2 films using atomic layer deposition (ALD) on Si(100) with chemical oxide or upon HF-last treatment. The mentioned precursor combination leads to excellent structural and morphological properties combined with good electrical ones. Upon injection in the reaction chamber of Hf(OtBu)2 (mpmp)2, the reaction proceeds, at 375 °C, through partial decomposition of the precursor leaving (OH)® species on the growing surface. The reaction of HfC14 not only reacts with the (OH)® surface functionalities, but supplies an additional amount of Hf atoms so that the growth rate (0.17 nm/cycle) is almost doubled compared to the Hf(OtBu)2 (mpmp)2 + H2O or O2 (both about 0.09 nm/cycle) ALD processes. Films obtained from Hf(OtBu)2 (mpmp)2 + HfC14, x-ray reflectivity measured an electronic density of 2.37 e-/Å3, as expected for thin HfO2 layers in the monoclinic phase. Indeed, both by x-ray diffraction and Fourier transform infrared spectroscopy analysis as on grow films detect the monoclinic phase with a small fraction of a metastable component. The latter is a remarkable result in the full oxidation of TiAl can be achieved at 500 °C, with a remarkable increase for the Lu-silicate films grown using O3 as oxygen precursor.

11:00 AM DL17
HfO2 Thin Films from Cyclopentadienyl Precursor by Atomic Layer Deposition. Jaakko Niinisto, Matti Putkonen and Lauri Niinisto; Laboratory of Inorganic and Analytical Chemistry, Helsinki University of Technology, Espoo, Finland.

For the atomic layer deposition (ALD) of HfO2, the HfC4/H2O process has mostly been applied. However, for gate oxide applications, structural problems, such as chlorinated oxide contamination and corrosion, have caused problem concern. Therefore, it is important to explore alternative precursors. In this work, HfO2 thin films have been deposited on native oxide or H-terminated Si(100) substrates by ALD using C6P/Hf(CH3)2 (C6P = cyclopentadienyl), C6H6 and water as precursors at deposition temperatures ranging from 300 to 500°C. Process parameters were optimised and ALD-type growth verified at 350°C. Stoichiometric HfO2 films deposited at 350°C had impurity levels below 0.2 and 0.4 atomic % for carbon and hydrogen, respectively as analyzed by TOF-ERDA. The crystallinity, morphology and dielectric properties were characterized. The effective permittivity of HfO2 in Al/HfO2/native oxide or HF-etched Si/Al capacitor structures was dependent on the HfO2 layer thickness and substrate pretreatment used. Strong inhibition of HfO2 film growth was observed with the water process on HF-etched Si. The effect of the oxygen source on the properties and growth of TiAlOx films is discussed, while comparative depositions with O2 as an oxygen source have been made.

11:15 AM DL18

High dielectric constant materials are recently attracted for alternative gate dielectric application in sub-0.1 μm in metal-oxide-semiconductor (MOS) devices due to its thermodynamical stability, high dielectric constant, a high breakdown electric field, and a large band gap. Among the several high dielectric constant materials, HfO2 gate oxide has been focused to study increased during recent years due to its high dielectric constant and good thermal stability in contact with silicon. We investigated the HfO2 gate dielectric material deposited by remote plasma enhanced atomic layer deposition (PEALD) method. HfO2 films were deposited at 200–650°C using tetraakis-dimethyl-amino-hafnium (TDEAH) as Hf precursor and oxygen plasma as O2 source. The analysis system is constructed and is connected with remote PEALD system. We deposited HfO2 with this system and thickness of HfO2 was controlled by the number of deposition cycle. One cycle of HfO2 deposition consists of Hf precursor injection and O2 plasma injection. The cycle is repeated until 100% of the Hf precursor was consumed. The Auger electron spectroscopy (AES), XPS. The electrical properties and reliability characteristics including EOT, hysteresis, leakage current and capacitance were evaluated by I-V and C-V measurements. This paper presents the characteristics and in-situ analysis of HfO2 gate dielectric deposited by remote PEALD using metal organic
Atomic Layer Deposition (ALD) of High-k Dielectrics:
Lanthanum Aluminum Oxide and Praseodymium Aluminum Oxide, Antti Raito, Philippe de Rouffignac and Roy G Gordon; Chemistry and Chemical Biology, Harvard University, Cambridge, Massachusetts.

Lanthanum aluminum oxide thin films were grown by ALD from a new lanthanum precursor, tris(N,N-diisopropylacetamidinato)lanthanum, trimethylaluminum and water. La$_2$Al$_2$O$_5$ films were deposited on HF-last silicon and measured without post-deposition annealing. Their composition was measured by RBS, XPS and SIMS. The films contained less than 1 at. % of carbon. C-V cycles was needed to deposit ALD film on Si wafers and also with sputtered gold electrodes. A thin (8.9 nm) film showed low leakage current (5x10^{-10} A/cm$^2$ at 1 V at an equivalent oxide thickness of 2.9 nm), flat-band voltage of -0.1 V and low hysteresis (20 mV). Thicker films had even lower leakage currents (<10^{-12} A/cm$^2$ at 2 MV/cm) but larger flat-band shifts and more hysteresis. The permittivity of the films was 13 and the dielectric strength 4 MV/cm. Cross sectional HRTEM showed a smooth interface between the La$_2$Al$_2$O$_5$ and the silicon substrate. Thin films of praseodymium aluminium oxide, Pr$_2$Al$_2$O$_5$, were also grown using a similar new praseodymium oxide precursor, tris(N,N-diisopropylacetamidinato)praseodymium. Their electrical properties will be reported and compared with those of the La$_2$Al$_2$O$_5$ films.

SESSION D2 Electrical Characterization and Reliability of High-k Oxynitrides

1:30 PM *D2.1
Threshold Voltage Instability and Inversion Layer Mobility Degradation of HfAlO$_x$(N) Gate Dielectric CMOS. Akira Toriumi 1,2, Naoki Yasuda 3, Hiroyuki Ota 2, Hirokazu Hamasakita 3, Wataru Mizubayashi 3, Tsuh hide Nabatame 3 and Tatsuyoshi Horikawa 3, 1The University of Tokyo, Tokyo, Japan; 2MIRA-I, Tsukuba, Japan; 3MIRA-ASET, Tsukuba, Japan.

The threshold voltage instability and the mobility degradation are main concerns of high-k gate stack technology. In order to clarify each degradation mechanism, high-k CMOS (n- and p-MOSFETs) with the same dielectric film (HfAlO$_x$(N)) and the same gate electrode (TaN or n-poly-Si) were fabricated through the same thermal processes. The interface layer at HfAlO$_x$(N)/Si was varied in terms of the thickness and the material (SiO$_2$ and SiON). First, the difference of Vfb (Vth) between n- and p-MOSFETs is discussed. In particular, Vfb of n-MOSFET - Vfb of p-MOSFET has been compared with the Fermi potential difference, $\delta\phi_F$, in Si substrates for TaN and n-polySi gate electrodes. In the case of TaN, $\delta\phi_F$ is roughly a half of $\delta\phi_F$, while in the case of poly-Si $\delta\phi_F$ is in good agreement with $\delta\phi_F$, even though the gate stack is nearly the same. This fact clearly indicates that Vfb (Vth) is very sensitive to the interface characteristics between gate electrode and high-k dielectric film, and that electronic states are induced at the top interface with metal gate. The mobility degradation has been also investigated from the viewpoint of the scattering mechanism differences between electron and hole in the inversion layer. As the absolute value of the mobility is different between electron and hole due to the effective mass difference, we have paid attention to the ratio, $\rho$, of the actual mobility with the universal one, so as to discuss the scattering probability rather than the absolute value of the mobility. The relationship between the ratio, $\rho$, and the inversion carrier density, Ns, indicates a remote characteristic as well as a clear difference of scattering mechanism between electron and hole in the high-k MOSFETs inversion layers. Since we employed absolutely the same gate stack for both n- and p-MOSFETs, it is strongly suggested that the experimental results come from a scattering difference between electron and hole. Furthermore, it is noted that $\rho$ of n-MOSFET and $\rho$ of p-MOSFET is of the ratio of a scattering rate newly introduced into high-k MOSFET, which is defined as the ratio of a scattering rate newly introduced into high-k MOSFET, to that of the universal one, runiversal$^{-1}$. It is worthy of particular attention that $\rho$ values for both electron and hole seem to be approximately proportional to $N_s^{-0.5}$, and moreover that detailed observation shows the significant scattering enhancement and the non-monotonic Ns dependence of $\rho$ for electron in spite of the same gate stack structure.

2:00 PM D2.2
Improved Electrical Characteristics of Hafnium Oxynitride High-k Dielectric Films Prepared by Ultraviolet-Assisted Assisted Oxynitride and Nitride Films in pMOSFETs. Dongping Wu 1,2, Vainonen-Ahlgren 3, Eva Tois 3, Marko Tauno 3, Mikael Oesling 3 and Shi-Li Zhang 3, 1Dept. of Microelectronics and Information Technology, Royal Institute of Technology, Kista, Sweden; 2The Angstrom Laboratory, Uppsala University, Uppsala, Sweden; 3ASM Microchemistry Oy, Espoo, Finland.

In order to combine the merits of both HfO$_2$ and Al$_2$O$_3$ as high-k gate dielectric materials for CMOS technology, high-k nano-laminate structures in the form of either HfO$_2$/Al$_2$O$_3$ or Al$_2$O$_3$/HfAlO$_x$/Al$_2$O$_3$ were implemented in pMOSFETs. After full transistor-processing including a rapid thermal processing step at as high temperature as 950 °C, the two interfaces of the high-k nano-laminate remained flat and distinct, indicating no observable occurrence of surface or interface degradation between the high-k films and Si-channel or TiN gate. The two thin capping Al$_2$O$_3$ layers were found to remain in the amorphous state for both types of the high-k nanolaminate by using high resolution transmission electron microscopy. The HfO$_2$ layer in the former nano-laminate, however, was found to be crystallized. In contrast, the HfAlO$_x$ layer in the latter high-k nano-laminate, remains in the amorphous state. Good capacitance-voltage (C-V) characteristics were observed for transistors with both high-k nano-laminates. The transistor with the HfAlO$_x$ layer showed a hysteresis of 20 mV at a gate bias range of +/-2 V, while the transistor with HfO$_2$ film exhibited a degraded value of 45 mV. The sub-threshold slopes for pMOSFETs with HfAlO$_x$ and HfO$_2$ films were determined to be 100 and 75 mV/dec., respectively, indicating that the nano-laminate with the amorphous HfAlO$_x$ yields a substantially improved interface quality compared with the nano-laminate with the polycrystalline HfO$_2$. In particular, HfAlO$_x$ based high-k MOSFETs with ultraviolet-assisted oxidation and nitridation of hafnium films.
As transistor sizes continue to shrink, gate oxide thicknesses are scaling below 1.0 nm to increase the gate stack capacitance, which will allow for overall improvement in power consumption according to Moire’s Law. With decreasing gate oxide thickness, however, direct tunneling becomes a major device issue as it contributes to leakage current and, subsequently, to increased standby power consumption. By increasing the permittivity of the high-k gate dielectric, the dielectric constant can be reduced and the capacitance can be scaled. Researchers have recently been studying hafnium-based high-k dielectrics as an alternative to SiO2. Further, the method of deposition often investigated has been Atomic Layer Deposition (ALD) in which thin films are used to deposit the high-k dielectric. This work has emphasized ALD utilizing inorganic precursors. We shall describe a process in which hafnium oxide and hafnium silicate films were deposited from alternating pulses of volatile metal-organic Hf/Si precursors and ozone on 200nm diameter Si substrates using an Aviza Technology PANTHEON™ ALD system. Electrical characterization of the films is presented, including equivalent oxide thickness (EOT), gate leakage, and electron mobility data, showing an achievement of 1.44 nm EOT with low mA/cm2 Jg and high field mobility equal to 74% of that of SiO2 (2.2 nm film).

3:15 PM D2.5 Limitations of poly-Si gated CMOS devices with high-k gate dielectrics. Edward Albert Cartier, Research Division, IBM, YORKTOWN HEIGHTS, New York. Finding a suitable replacement for SiO2 as the gate dielectric in CMOS devices appears to be a precondition to continue conventional device scaling. Without replacing SiO2, the power consumption due to gate leakage cannot be acceptably reduced in scaled devices. In this case, a new dielectric would be in the industry’s interest to only replace the SiO2 gate oxide, such that the established self-aligned CMOS manufacturing process, which uses n- and p-doped poly-Si gate electrodes for the nFET and pFET, respectively, can be used with minimal changes. However, concerns are increasing that the selected high-k materials are incompatible with the established manufacturing process and that the successful introduction of high-k dielectrics may require more substantial changes, such as the replacement of all poly-Si gate electrodes by metals. In this presentation, the electrical performance of CMOS devices with high-k gate dielectrics and poly-Si gates will be reviewed. Three major challenges can be identified: 1) Accurate control of the transistor threshold voltage is difficult. Threshold voltage control is particularly poor for the p-FET with Hafnium based dielectrics. 2) Channel mobility is reduced with a high-k dielectric in the gate stack. The mobility degradation is generally more severe for the nFET, especially for aggressively scaled devices with minimized SiO2 buffer layers between the Si substrate and the high-k dielectric. 3) The threshold voltage stability during device operation is reduced. Charge trapping in the high-k dielectric and charge trapping in the voltage instability primarily in the nFET. Extensive process optimization and materials modifications have provided partial solutions for some of these issues. However, it remains challenging to realize an aggressively high-k scaled gate stack with low SiO2 buffer layers. Some of the discussed difficulties may be fundamentally tied to the properties of the selected gate materials.

3:45 PM D2.6 Effect of Structural Defects on Hf-Based Gate Stack Transistor Performance. Gennadi Bersuker, Chadwig Young, Joel Barnett, Nam Moon, James Peterson, Patrick Lynghirt, George A. Brown, Peter M Zeitzoff, Mark Gardner, Robert W. Murray and Howard R. Huff, International SEMATECH, Austin, Texas. Aggressive transistor scaling required to achieve higher drive current calls for an equivalent electrical thickness (EOT) of the gate dielectric less than 1 nm as well as a low gate leakage current. These conditions cannot be supported by the conventional SiO2 dielectric. On the other hand, transistors built with the high-k gate dielectric, which can provide both high capacitance and low leakage currents, usually exhibit low drive currents. In this presentation, we analyze several structural features of the high-k films, which may contribute to the degradation of transistor performance. The presence of electron traps may lead to the loss of the inversion charge in the channel. Reduction of the charge would be interpreted as a degradation of the channel mobility. By applying a fast transient measurement technique to the transistors manufactured using HfO2 dielectrics, it was demonstrated that trapping occurs on a very small time scale as compared to DC measurements, manifesting itself as a mobility reduction. The data suggest that the bulk high-k traps, rather than the traps located in the high-k/SiO2 interface, are responsible for the inversion charge loss. Coulomb scattering by the fixed charges in the high-k gate dielectric located in close proximity to the interface with the substrate can reduce the carrier mobility. From the Tlb dependence on EOT for a wide range of the dielectric thickness, we find a significant difference in the interface charge of the ALD and MOCVD Hf-based dielectrics, higher interface charges correlating to lower mobility in the corresponding samples. At the same time, both charge pumping and DC-IV data do not show any significant differences in the interface densities of these gate stacks, indicating that the interface states are not responsible for the observed degradation of the carrier mobility. In the set of Hf-silicide samples with 20% SiO2 deposited on the thermally grown SiO2 layers in the range of 0.5 nm to the final (post break-in) interfacial SiO2 thickness was electrically estimated to increase by 0.1 nm to 0.3 nm. This small increase of the process-grown SiO2 thickness correlates to mobility degradation, which may be caused by the low quality of this thin post-process oxide (1AOx, 0.5 nm) deposition at temperatures as low as 800°C. Structural non-uniformity in the high-k gate dielectric, which may be associated with the random grain orientation of the crystallized high-k film, can contribute to the non-uniformity of the vertical electric field in the transistor channel that may suppress carrier mobility. This non-uniformity effect increases for the thinner interfacial SiO2 layers and higher k values of the gate dielectrics.

4:00 PM D2.7 Dielectric Breakdown Characteristics of HfAlOx/SiON gate stack. Kazuyoshi Torigi, Hiroshi Ohji, Tatsuki Kawahara, Ichiro Matsuhashi, Atsushi Horichi and Seichi Miyazaki.
1Semiconductor Lending Edge Technologies, Tsukuba, Ibaraki, Japan; 2Hiroshima university, Nishiga-Hiroshima, Hiroshima, Japan. Hf based oxide thin films with high dielectric constant (high-k) have been intensively studied because of their potential use as alternative gate dielectrics. The integration of high-k dielectrics has several challenges, 1) The high-k dielectric must be able to withstand the sub-100 nm gate leakage current that has already been demonstrated; however, there are few reports on the reliability of HfAlOx. In this study, we investigate the dielectric breakdown behavior of MOSFETs with HfAlOx gate dielectrics fabricated using mass production worthy 300 mm process. The Poly-Si gate FETs were made using standard CMOS process adapted to high-k gate stack. The HfAlOx thin film was deposited by ALD on a wafer with an intentionally formed interfacial layer (IL). Because of higher crystallization temperatures (1400°C), the IL content of less than 30% was selected. The uniformity of the Hf concentration is ±1.8% and that of the optical thickness is ±2.5% over a 300 mm wafer. The gate leakage depends little on the temperature and it shows a good linearity in a F-N plot under higher gate voltage. The time dependent dielectric breakdown (TDBB) behavior was examined using constant voltage stress. If SiO2 is used as an IL, the IL reduction and the interleaving between the HfAlOx layer and the IL occurred, which makes the IL thickness variation larger. In the TDBB measurements, it causes extrinsic breakdown resulting in lower Weibull slope. By using the SION as an IL, the interfacial reaction can be suppressed and the extrinsic breakdown component can be eliminated even if the post process temperature is as high as 1000°C. In the case of gate injection, abrupt increase of gate leakage was observed, and gradual increase is followed after that. Using either E-model or 1/E model, the MTTF (for 0.1 cm2 at 125°C) is 107 years. On the other hand, gate leakage starts to increase gradually at a certain stress period without abrupt jump in the case of substrate injection. Therefore, it is difficult to determine the time to breakdown, Tbd. If we define the Tbd at the onset of leakage current increase, the MTTF would be only 3.7 years if it obeys the E-model (MTTF predicted by 1/E model was 1.6x107 years). In order to discuss the mechanism of the TDBB, the band diagram was examined using XPS. The band gap and the valence band offset of HfAlOx are determined to be 6.5eV and 3.6eV, respectively. This band alignment suggests that the leakage current is restricted by the IL in the case of the substrate injection while it flows through both HfAlOx and IL in the case of the gate injection. The mechanism of TDDB is not clear at the moment; however, we would interpret the TDDB as high-k IL in the case of substrate injection and low-k IL in the case of gate injection, which suggests that the gradual increase in leakage is due to the HfAlOx wear out whereas the leakage of the HfAlOx/SiON gate stack is mainly determined by the IL.

4:15 PM D2.8 Electrical breakdown in a two-layer dielectric in the MOS Structure. Sheng Park 1,2, Seung Park and Yoshi Senzaki 2; 1Sematech, Austin, Texas; 2Aviza Technology, Scotts Valley, California; 3North Carolina State University, Raleigh, North Carolina.

The formation of interfacial oxide between high-k and Si creates a two-layer dielectric in the MOS structure. In this talk, we present a model to describe electrical breakdown in the two-layer dielectric. The leakage current through the two-layer dielectric shows three regimes with applied voltage: both layers intact, one layer breakdown, and...
both layers breakdown. Accordingly, three conduction mechanisms are presented for the three regimes: tunneling through two layers, tunneling through one layer, and hard breakdown for high-K materials. Our model has been compared with experimental data obtained from the HfO$_2$/SiO$_2$ MOS structure, and good agreement is achieved. This model can be used to estimate the thickness, breakdown field, or dielectric quality. Each of the three regimes of the model also predict the overall breakdown field for different combinations of dielectric layers. When combined with C-V measurements, more information about the two-layer dielectric is obtained.

4:30 PM D2.9

Physical impact of a high-temperature post-nitridation anneal on advanced plasma nitrided gate dielectrics (45nm to 65nm technologies). Maxime Beaucens$^1$, David Barge$^1$, Nicolas Emonet$^2$, Francois Guyader$^2$, Lucky Vashishth$^3$ and Kathy Barla$^2$; $^1$Philips Semiconductors R&D, Crolles, France; $^2$STMicroelectronics, Crolles, France; $^3$Motorola, Crolles, France.

It is common knowledge that the continued scaling of CMOS devices will require the integration of high-K gate dielectrics in the very near future. However, extensive screening of high-K material properties still shows a number of unresolved issues, and their integration into the 45nm platform remains uncertain. Consequently, the downward extension of plasma nitrided gate oxides is being actively pursued. Typically, plasma processes are performed in three serial steps including a thermal pre-oxidation, the nitrogen incorporation and a high temperature post-nitridation anneal. In this paper, we propose simple physical models for understanding the nitrogen incorporation and distribution after each individual step. Several in-line techniques such as SIMS, ALD, constant capacitance profiling (CCP) and delay-to-oxidation are used to estimate the concentration and location of nitrogen species. We show that nitrogen atoms are chemically implanted into the bottom oxide prior to diffusing down to the silicon-oxide interface. Oxidizing (O$_2$) and neutral (N$_2$) anneals are processed at various temperatures from 500°C to 1000°C, and the specifics of each is detailed. Using this knowledge, the need for a post-nitridation anneal is discussed in terms of dielectric film stability. We show that annealing plasma nitrided oxides at a high temperature allows an efficient reorganization of nitrogen bonds in the silica lattice, with interfacial Si-N-O(2) unstable bonds turning into N-Si(Si) stable bonds. The nitrogen dose incorporated in annealed and unannealed oxides is also monitored with time, showing that a significant amount of nitrogen is released in the ambience when the films are not annealed. This parasitic outgasing is directly correlated to the local concentration of nitrogen at the dielectric surface, and can lead to nitrogen dose non-repeatability in the case of non-clustered nitridation-anneal sequences. Finally, previous results are compared with end-of-line characteristics from 1-2.1nm CET Capacitance Equivalent Thickness plasma nitrided oxides. The effect of the high temperature anneal on the gate leakage vs. CET trend is reviewed for various process conditions. Its impact on the device effective mobility and on the dielectric reliability is discussed as well.

4:45 PM D2.10

Study of pulsed RF DPN process parameters for 65 nm node MOSFET gate dielectrics. Anke Rothbach$^1$, P A Kraus$^1$, T C Chua$^2$, F Nouri$^2$, Florence N Cubaynes$^3$, Anabela Veloso$^1$, Sofie Mertens$^2$, Lenie Schilt$^2$, Jungsic Hong$^3$, Paul C. McTynon$^2$ and Kathy Barla$^2$; $^1$IMEC, Leuven, Belgium; $^2$Philips Semiconductors R&D, Crolles, France; $^3$Department of Material Science and Surface Modification for Area-Selective Atomic Layer Deposition. Rong Chen$^1$, Hyoungsub Kim$^2$, Junsic Hong$^3$, Paul C. McTynon$^2$ and Stacey F. Bent$^3$; $^1$Department of Chemistry, Stanford University, Stanford, California; $^2$Department of Material Science and Engineering, Stanford University, Stanford, California; $^3$Department of Chemical Engineering, Stanford University, Stanford, California.

High-k oxides have recently become the focus on intense research as replacements in advanced MOS devices of the extremely thin SiO$_2$ gate oxides. Pulsed laser deposition (PLD), although not a microelectronics production tool, is one of the best techniques for the growth of high quality complex oxide thin films for conducting rapid investigations of deposited oxides properties and their chemical interactions with the substrate or the gate material. One of the main problems encountered during PLD of high-k dielectrics directly onto Si samples, as well as other investigations using different growth techniques, is the formation of an unwanted interfacial layer at the interface. Even though the oxide grown was found to exhibit excellent electrical properties such as high dielectric constants, the presence of this interfacial layer diminishes this advantage for the resultant devices. We investigated the oxygen source and the kinetics of the interfacial layer growth during deposition and thermal treatments of HfO$_2$, Y$_2$O$_3$ and ZrO$_2$ layers on Si. Several techniques having nanometer scale resolution were employed to elucidate the interfacial layer chemistry and growth kinetics. The positions and shape of the metal, oxygen and Si XPS peaks suggest that at the temperatures used for deposition (< 650 deg C) the SiO$_2$ layer is physically mixed with the deposited oxide layer without forming silicate compounds. X-ray reflectivity and cross-section transmission electron microscopy investigations confirmed the presence of the interfacial layer, whose density was found to be higher than that of pure SiO$_2$ but lower than that of the corresponding silicate, corroborating the XPS results. Two possible routes using ultraviolet-assisted low temperature conditioning of the Si substrate prior to deposition to reduce interfacial layer thickness and optimize the electrical characteristics of the grown structures will be also presented.

D3.8

Surface Modification for Area-Selective Atomic Layer Deposition. Hong Chen$^1$, Hyungsoo Kim$^2$, Junsic Hong$^3$, Paul C. McTynon$^2$ and Stacey F. Bent$^3$; $^1$Department of Chemistry, Stanford University, Stanford, California; $^2$Department of Material Science and Engineering, Stanford University, Stanford, California; $^3$Department of Chemical Engineering, Stanford University, Stanford, California.

Gate dielectrics with permittivities greater than that of SiO$_2$ are required to continue the downward dimensional scaling of MOSFET devices. Among many possible deposition techniques, atomic layer
deposition (ALD) is very promising for preparing high-k dielectric materials because it can produce high quality films with excellent conformality and precise film thickness control. While ALD inherently provides nano-scale control of materials in the vertical direction, we are investigating an area-selective ALD technique that will enable nano-scale definition of the lateral structure. Our research emphasizes controlling the interface of inorganic thin film dielectrics in order to improve spatial selectivity to ALD. Availability of area-selective ALD processes for the application of gate dielectric and gate electrode deposition could substantially reduce the number of lithography, etch, and cleaning operations required to integrate circuitry. We are using a two-pronged approach to generate a patterned substrate in which certain well-defined regions have been “primed” for deposition and others have been “deactivated.” We have focused mainly on HfO2 and ZrO2 as the high-k dielectric materials in the ALD process because of their compatibility with conventional metal-oxide-semiconductor device processing. We will show that well-controlled self-assembled monolayers (SAMs) are efficient deactivating agents to block HfO2 and ZrO2 growth by ALD. A series of SAMs of organosilanes have been investigated as deactivating agents for the HfO2 ALD process. Three important factors for the quality of SAMs formation—molecular chain length, reactivity and steric effect—were studied by water contact angle (WCA) measurement, ellipsometry, X-ray photoelectron spectroscopy (XPS), transmission electron microscopy (TEM) and atomic force microscopy (AFM). The effect of these factors on ALD deactivation was investigated by a combined XPS, TEM and AFM analysis. We find that it is crucial to choose deactivating agents with high reactivity, low steric effects and certain chain length in order to form condensed, highly hydrophobic film for the deactivation. The analysis provides insight into the mechanism of the deactivation and ALD growth. The area-selective ALD approach, in principle, could be applied to many other materials or varieties of shapes and surfaces in the future. Moreover, an area-selective ALD process, which requires cleaning and etching steps by depositing materials only where they are needed, would be particularly useful for fabrication of expensive materials, fabrics that are difficult to be etched away, processes that required non-residual contaminations, non-planar MOSFETs and other complex nano-devices.

D3.4 Atomic Layer Deposition of Zirconium Oxide and Hafnium Oxide from novel metal-organic precursors. Junjue Kim and Sangman Koo; Chemical Engineering, Hanyang University, Seoul, South Korea.

High-k metal oxides are sought-after for a variety of applications in the electronic industry. To meet the demand of preparation of these materials in a manner compatible with conventional Si-based processes, Atomic layer deposition (ALD) is desired for film growth. In this study, thin films of ZrO2 and HfO2 have been deposited by ALD using novel metal-organic precursors: [M(macact)]2(ONeop)3] in the temperature range of 300-500°C on silicon substrate: [macact = methylimidazolato (1H)pyrazolyl (1)] and ZrHf([macact])2. The films were characterized by a combination of transmission electron microscopy, Auger spectrometry, atomic force microscopy and X-ray diffractometry.


Hafnium oxide thin films have successfully been deposited on silicon substrates by Atomic Layer Deposition (ALD). The films were grown at the substrate temperature of 300 °C and 27 oC in pure oxygen and water vapor, respectively. The Laser Ablation Pulsed Plasma (LAPP) laser to create hot plasma to ablate material from a rotating hafnium target rod. Oxygen was used as the carrier gas to entrain the ablated material in a cooling expansion process. The choice of carrier gas exerts considerable control over the plasma properties, it can control both the chemical composition and the temperature of the ablation plasma. Depositions yielded controlled thickness of 5 nm to 100 nm of stoichiometric HfO2 films. In this work the film microstructure will be compared to the microstructure of films deposited by LAMBDA at room temperature. Optical characterization of high dielectric constant (k) hafnium (HfO2) was performed by means of spectroscopic ellipsometry (SE) and grazing X-ray reflectivity (GXR) measurements. The thickness is obtained with absolute GXR technique for very thin films and the optical constants are calculated from ellipsometry measurement. The relationship between microstructure and their optical properties will be discussed in this paper.

D3.6 Thermal stability of amorphous praseodymium silicate films on silicon. Gaetano Peccianti, Niall Meade, Wang Jun, Xuefeng Dong, Taro Toru, Vito Raineri1 and Ignazio Luciano Frasigla; 1sezione di Catania, IMM-CNR, Catania, Italy; 2Dipartimento di Scienze Chimiche, Università di Catania, Catania, Italy.

New dielectric materials with sufficiently high permittivity are needed as future insulators to replace SiO2 in complementary metal oxide semiconductor (CMOS) devices. Praseodymium silicate amorphous films can be an interesting alternative. We have investigated the effect of thermal annealing on praseodymium silicate thin films grown by Metal Organic Chemical Vapor Deposition (MOCVD). Praseodymium silicate films have been obtained at 750 °C using the Pr(tmhd)3 ([H3tmhd=2,6,6-tetramethylheptane-2,5-dione]) precursor. Their structural characterisation has been performed by X-ray diffraction (XRD) as well as by transmission electron microscopy (TEM) analysis. Both investigation have demonstrated that as-deposited praseodymium silicate films are amorphous. Evidence of the thermal stability of the praseodymium silicate films have been obtained by post annealing processes. In fact it is well known that one of the most critical issue, for the implementation of new dielectrics in substitution of silicon oxide, is their structural and chemical stability against the thermal processes during the fabrication of MOSFET devices. In this context, the thermal stability of the deposited films have been tested by two different annealing processes: Rapid Thermal Annealing (RTA) and long ramped annealing in a furnace, in order to evaluate time dependence of praseodymium silicate thermal stability. The influence of the process atmosphere has been fully investigated and the praseodymium silicate has been found to be stable up to 900 °C in nitrogen atmosphere. In fact, their XRD spectra have shown no peaks as in the as-deposited film patterns, thus indicating that no other phases are formed upon heating and, consequently, that the praseodymium silicate phase is thermally stable. Moreover, no changes occurred on film morphologies as assessed by TEM analyses. However evidence of crystallisation processes have been detected at 800 °C in oxygen environment. In fact, the XRD patterns have shown some of the most intense reflections that are characteristics of the stoichiometric Pr8Si6024 phase. TEM cross section images have clearly shown that praseodymium grains morphology have changes and rounded grains 100 nm large have formed. These results imply significant oxygen diffusion through the praseodymium silicate dielectric layer during the thermal treatment at 800 °C, however it has demonstrated not to suffer of any structural and compositional variation up to 900 °C in controlled atmosphere.

D3.7 Determination of nitrogen concentration of oxynitride gate dielectric films by using spectroscopic ellipsometry. Yong Jai Cho, Hyun Mo Cho, Hyun Jong Kim, Won Chegal and Yun Woo Lee; Department of Optical Metrology, Korea Research Institute of Standards and Science, Daejeon, South Korea.

We have applied spectroscopic ellipsometry (SE) to investigate a set of various nitride silicon dioxynitride films and to determine film thicknesses, optical properties with the nitrogen concentrations of the films. Silicon oxynitride is an intermediate solution for high-k gate dielectrics in present and future ultra-large-scale-integrated (ULSI) devices. Advantages of oxynitrides as gate dielectric in the ULSI devices improve high carrier reliability with a little nitrogen at Si-SiO2 interface and prove a diffusion barrier for boron in poly-silicon gate, and reduce tunneling currents. Therefore, in the future ULSI technology, it will be needed to evaluate the reliability in measurements of the thickness and nitrogen concentration of ultrathin oxynitride film. Ultrathin oxynitride films were grown on Si substrate by NO thermal deposition and then annealed at a high temperature. SE measurements were performed on a spectroscopic ellipsometer. The dielectric functions of these films were determined by using widely used dispersion models and Bruggeman effective medium approximation, respectively. It will be shown which model can be used to effectively describe the optical properties of the ultrathin oxynitride films. We will also show that SE can easily and quickly quantify the nitrogen concentration of oxinitride films without employing a more elaborate method such as a medium energy ion scattering spectroscopy (MEIS).


Variations in annealing temperature alter the physical, materials, and electrical properties of tantalum pentoxide (Ta205) thin films. In this

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Experimental Ta2O5 films were deposited onto p-type silicon substrates using reactive DC magnetron sputtering. This study examines the effect of varying the deposition temperature. Samples were annealed for one hour in a dry ambient air at temperatures of 730°C, 780°C, and 830°C. Mechanical properties examined include stress, hardness, elastic modulus, and surface roughness. Annealing at 830°C resulted in a near zero compressive stress for samples annealed at 730°C. Samples annealed at 780°C and 830°C were tensile, but were on the order of 100 MPa lower in stress than the as-deposited samples. Elastic modulus did not vary significantly with values maintained at approximately 70 GPa, with the exception of the sample annealed at 780°C which demonstrated a hardness of 12 GPa. Surface roughness was lowest for the as-deposited samples. For the annealed samples, a minimum was observed at 780°C, with surface roughness increasing for samples annealed at 830°C. Electrical properties studied were leakage current, breakdown field, resistivity, and dielectric constant. Leakage current generally improved with annealing, especially at the lower temperatures, electrical breakdown field was observed for annealed and for 780°C annealed films. Resistivities of the films were 6.5 x 10^10 to 6.1 x 10^12 ohm-cm, with the film annealed at 830°C being the most conductive. Annealing also led to an increase in dielectric constant up to 80°C, before decreasing at 830°C. Dielectric constants varied from 7.7 for the as-deposited to 19.1 for the 780°C annealed sample.

**D3.10**

**TiO2-based Tunneling Transistors on Silicon Substrates.**

Asghar Behnam, Bahman Hekmahzadeh, Behnaz Arvan, Farshid Karsabian and Ebrahim Asl-Soleimani, Electrical and Computer Engineering Department, Univ. of Tehran, Tehran, Iran.

We have successfully fabricated tunneling transistors on Si substrates based on TiO2 insulator films. The structure used for such transistors is a sandwich of Ni-Si/TiO2/Ni-Si/TiO2 layers with a thickness of 100Å/150Å/20Å/150Å on an n-type (100) Si substrate. All deposition steps were carried out consecutively in a single run using a multi-target RF-sputtering system at a base pressure of 10^-4 torr. A mesa structure is realized by chemical etching of the top-emitter, intermediate base and bottom collector regions. Also the intermediate Ni-Si layer acts as the contact to the intrinsic base. The voltage applied between the top-emitter and the base-silicide layers sets the level of electrons in the base-emitter interface for annealed and for 780°C annealed films. The presence of the electrons that pass through the base-silicide layer can pass over the bottom oxide and make the collector current. In this configuration, \( \beta \) is defined as the ratio of the collector current to the base one and it has been found to be around 11 with an emitter current of 2mA. From the electrical characteristics of the device, one can observe a "kink" in the current-voltage behavior of the transistor. This "kink" occurs when the base current becomes minimal and \( \beta \) rises. We believe that the titanium dioxide layer deposited using RF-sputtering does not possess good quality in terms of leakage current and stoichiometry, leading to higher base currents. To improve the leakage characteristics of the TiO2 insulator, we have developed a low temperature atmospheric pressure chemical vapor deposition (APCVD) of TiO2 films using a mixture of TiCl4 and O2. The presence of H2O2 during the deposition of the oxide significantly improved the electrical and crystalline quality of the TiO2 layers as confirmed using XRD, SEM and FTIR spectroscopy tools. H2O2 is believed to be an additional source of oxygen radicals, enhancing the growth conditions and yielding high quality films. Also the electrical quality of the insulating layer was examined by means of fabricating MOS capacitors on p-type (100) Si substrates. The films are grown at temperatures ranging from 150 to 300°C. The films grown at 170°C in the presence of H2O2 show a leakage current density of 10^-7 A/mm, a breakdown field of 10^7 V/cm, and a relative permittivity of 15 to 21. Also from the capacitance-voltage (C-V) characteristics a threshold voltage of 1 V is measured for the MOS structure. Since the growth temperature of the oxide film is as low as 150°C, compared to the use of polycrystalline silicon as the insulating layer base. The fabrication of the TiO2-based tunneling transistors on polyethylene terephthalate (PET) plastic substrates is being carried out and the electrical characterization of the devices is currently underway. We speculate that such transistors may be used as high performance switches for flexible electronic applications.

**D3.11**

**Engineering the nm-thick interface layer formed between TaOx high k film and silicon substrate.** Yue Kuo and Jing Lu, Thin Film Nano & Microelectronics Research Laboratory, Texas A&M University, College Station, Texas.

Tantalum oxide (TaOx) is a promising high-k gate dielectric material to replace thermally grown SiO2 in the sub-0.1 micron CMOS technology node. However, TaOx forms a low quality interfacial layer when it is in contact with silicon [1]. Previously the authors reported that when TaOx was doped with Hf, several advantages were obtained: increasing the amorphous-to-polycrystalline transition temperature, improving interface layer quality, and enhancing the k value [2]. When a 5 angstrom tantalum nitride (TiNx) was inserted between the Hf-doped TaOx and silicon, many of the film dielectric properties were further improved [3]. Effects of HF doping process and the insertion of the ultra-thin TaNx layer on the interfacial layer material and electrical property changes after a high temperature annealing step had not been systematically studied, previously. In this paper, we investigate these effects with the help of various characterizing instruments, such as SIMS, ESCA, TEM, and IV/CV measurements on the fabricated MOS capacitors. The following results have been obtained: 1) the Hf dopant in the TaOx film was involved in the interface formation process, forming a new thin TiOx/HfO2/SiO2 interface layer than the SiO2 layer. 2) when the TaNx interface layer was inserted, the interface further changed, e.g., by forming new TiOxNy and HfSio2Oy compounds. 3) when the thin TaNx interface layer was inserted, the above electric properties were further improved. However, the high temperature annealing step lowered these values. Above results were due to the insertion of nitrogen into the interface layer and the repairing of damaged bonds. In summary, the interfacial structure layer and the properties of TaOx high-k film were improved with the doping process and the insertion of an ultra-thin TaNx interface film. This research is partially supported by NSF DMI-0243469 and DMI-0300032 projects. [1] K. J. Hubbard and D.C. Schom, J. Mater. Res. 1996; 11: 2737-2737. [2] L. Lu, J.-Y. Tewg, Y. Kuo, and P. C. Liu, ECS Proc. Six Int Symp. High-K and Low-K Dielectric Materials: Constant Materials: Materials Science, Processing, Manufacturing, and Reliability Issues, PV 2002-28, pp 105-112, 2003. [3] Y. Kuo, J. Lu, and J.-Y. Tewg, Jpn. J. Appl. Phys., 42(2), 7A, L769-771, 2003.

**D3.12**

**Effects of A12O3 layer thickness in A12O3/HfO2 gate oxide deposited by Atomic Layer Deposition Method.** Myungjin Park, Jaehyoung Koo and Hyonguk Jeon, Division of Materials Science and Engineering, Hanyang University, Seoul, South Korea.

As the metal-oxide-semiconductor (MOS) device is scaled down to the sub-micrometer, the high-k dielectrics are needed as new gate oxide materials. Among the various high-k dielectric candidates, HfO2 and Al2O3 have been mainly investigated due to their large band gap, good thermal stability, and relatively higher dielectric constant compared to SiO2. For these reasons, they are widely used in place of SiO2 as an alternative high-k (k=2530) gate oxide in MOSFET. But, even though HfO2 has a lot of advantages over other high-k dielectrics, it has also problems to solve such as, high leakage current and to cleaved interfacial layer. According to research, thin interfacial layer causes lowering dielectric constant and flat band voltage shift. Al2O3 is one of materials, which exhibits the amorphous phase in contact with Si substrate. And this material is considered to be effective to stop the diffusion of hydrogen and oxygen atoms. In this study, we used Al2O3 material to prevent interfacial layer formation. To investigate the effects of Al2O3 thickness, we deposited various thicknesses of Al2O3 and followed by HfO2 deposition by atomic layer deposition (ALD) method. This method has already known as one of the method to deposit very thin film precisely and high quality films. With this experiment, we investigated the HfO2 formation depending on the thickness of Al2O3 interfacial layer. The physical and chemical properties of Al2O3/HfO2 films were analyzed by high-resolution transmission electron microscopy (HRTEM), X-ray
photoelectron spectroscopy (XPS) and Auger electron spectroscopy (AES). The electrical properties were calculated and analyzed by using capacitance-voltage (C-V) and current density-voltage (J-V) measurements. Characteristics of Al2O3/HfO2 films will be discussed based on the results mentioned above.


HfAlOx is one of the candidate for high-k dielectric for high performance MISFETs, though large CV hysteresis has been observed in poly-Si/HfAlOx stacked MISFET with high temperature annealing. With C-V measurements, the thermal budget of the PDA should be low because thermally unstable NiS on S/D for high performance LSI was formed before high-k deposition. Flash lamp is a strong candidate for very short time heating process compared with conventional RTA process. In this work, we investigated electrical properties of flash lamp annealed HfAlOx using n/p-MISFET with W/TiN/HfAlOx/SiO2 gate stack, where these films were formed after source/drain formation and the activation. A 2.5 nm-thick HfAlOx was deposited on a 1-mm-thick SiO2 by atomic layer deposition (ALD) at 300°C. The Hf concentration, Hf/(Hf+Al), was 0.3. For the flash lamp PDA, the flash was set on the stage held at RT - 500°C, and it was irradiated with energy density of 24-27 J/cm² in 0.6-0.8 msec. High temperature PDA at 1050°C was carried out for reference samples with poly-Si and W/TiN gate electrode. W/TiN/PolySi gate samples were deposited on 100nm and 150nm SiO2, respectively. The samples with poly-Si gate electrode were annealed at 1000°C for 3sec after the gate patterning for the gate dopant activation. The EOT of the reference sample with W/TiN was 1.5nm. CV hysteresis of the poly-Si and W/TiN gate reference samples was approximately 50mV at the inversion and 20mV at the accumulation potential for growing high quality thin films at room temperature by electron-beam evaporation through a shadow mask. NRA data show that the electrode. W and TiN was deposited by CVD at 100nm and 10nm respectively. The hysteresis loop suggest that origin of the hysteresis is electron injection from substrate or electrode. In the case of the substrate injection, the amount of injected electron is limited by the interfacial SiO2, resulting in large hysteresis at the inversion in nMISFET or at the accumulation in pMISFET. Even though the flash lamp PDA was applied, the high temperature activation for the SiO2 gate caused a hysteresis about 100mV. The lower thermal budget achieved by the flash lamp annealing and metal gate deposition is effective to suppress the interfacial reaction which causes the traps responsible for the hysteresis.

D3.14 High-k (ZrO2, HfO2) Dielectrics on Si Substrates Synthesized by Elevated Temperature UV-Ozone Oxidation Technique, Kang-il Seo, Paul C. McIntyre, and Krishna Saraswat; 1Materials Science & Engineering, Stanford University, Stanford, California; 2Electrical Engineering, Stanford University, Stanford, California.

Recently, there has been a significant effort in developing high-k metal oxide materials such as ZrO2 and HfO2 to replace SiO2 as the gate dielectric in future CMOS devices. Among many methods to grow high-k dielectrics, the UV-ozone oxidation (UVO) technique has shown potential for growing high quality thin films at room temperature. UVO processing also avoids incorporation of impurities related to the reaction of precursor molecules used in alternative deposition methods such as chemical vapor deposition and atomic layer deposition. In this presentation, we report the oxidation kinetics of Hf and Zr via the UVO technique in the temperature range from 25°C to 300°C, and correlate our results with the microstructural and electrical properties of UVO ZrO2 and HfO2 films grown on Si (001). In the oxidation kinetics study, nuclear reaction analysis (NRA) was performed at various oxidation times and temperatures to determine the oxygen incorporation on the Si substrate with high sensitivity. To synthesize MOSCAP structures, 20 50A Zr or Hf metal films were deposited by electron-beam deposition on Si after different surface cleaning/ultrathin oxide passivation treatments. In - situ UV-ozone oxidation was performed in the temperature range from 25°C to 300°C. Platinum electrodes were deposited ex - situ by electron-beam evaporation through a shadow mask. NRA data show that the oxidation kinetics of Hf 25°C is enhanced significantly as the UVO temperature is increased. It is thought that the incorporation of Zr25°C into the Si substrate is thicken this interface layer. The leakage current density is significantly reduced as the UVO temperature increases due to interfacial oxide growth and, perhaps, improved oxygen stoichiometry of HfO2 films.

D3.15 Abstract Withdrawn

D3.16 The effect of ZrO2 incorporation into rare earth Gd2O3 film grown on Si(111): a so sh park1, Yonguk Kim1, J.H. Baeck1, M.H. Cho2, M.K. Noh1 and K.H. Jeong1, 1Yonsei university, seoul, South Korea; 2Korea Rearch Institute of Standard Science, seoul, South Korea.

Gd2O3 films incorporated with ZrO2 were deposited on Si(111) using electron-beam evaporation by reactive thermal evaporation. High resolution x-ray diffraction and RBS data showed that Gd2O3 films incorporated with ZrO2 are superior epitaxial quality to pure Gd2O3 films. The improved crystallinity is caused by interfacial reaction between rare earth metal Gd and Si substrate. The chemical state of the films investigated using X-ray photoelectron spectroscopy (XPS) showed that the incorporated Zr played an important role to restrain silicate layer. The high quality films grown on Si(111) were deposited at temperatures below 600°C for 10 min were homogeneous and dense, and the electrical properties confirmed the good quality of these films.

D3.17 Influence of Pre-Oxidation of an Ir Film on Chemical Composition and Crystal Property of a PZT Film Deposited on the Ir Film by Sputtering, Sasanu Horita and Makoto Shongu, School of Materials Science, Japan Advanced Institute of Science and Technology, Tatsunokuchi, Ishikawa, Japan.

We investigated the influence of pre-oxidation of an Ir film on the chemical composition and crystal property of the PZT film deposited on the pre-oxidized Ir film. The Ir film was deposited on a thermally oxidized Si substrate at 600°C by Ar gas sputtering with an Ir metallic target. The Ir film had (111) preferable orientation. The pre-oxidation of the Ir film was performed at 600°C in 10Pa of O2 gas for 20 min in the deposition chamber prior to depositing a PZT film. The PZT film was deposited on the Ir film at 600°C by reactive sputtering of Ar+O2/(9:1) gas with a 106-mm-diameter ceramic PZT target and 10-mm-diameter PZT pellet. Instead of Ar+O2 gas, we changed the target composition to Pb(1/2)(Zr0.52Ti0.48)O3 and Pb(1/2)(Zr0.48Ti0.52)O3. Also, on each target, 8 or 15 pieces of PbO pellet were placed circularly to control Pb stoichiometry in the PZT film. At first, we found from the XRD measurement that a strong PbO(101) peak appeared from the PZT film deposited on the pre-oxidized Ir film with the target of Zr0.52Ti0.48 and 15 PbO pellets. This means that the products is much less than for Zr oxidation. Capacitance-voltage measurements indicate that frequency dispersion of the capacitance decreases with increasing temperature. The capacitance-derivative equivalent oxide thickness evolves with UVO process times and temperatures in a manner consistent with a competition between reduction of the initial SiO2 surface passivation by the reactive Ir or Hf metal precursor layer, and oxidation of the underlying Si substrate to thicken this interface layer. The leakage current density is significantly increased. For given oxidation times and UVO treatments. Characteristics of the PZT film deposited on the non-oxidized Ir film were almost the same as those of the PZT film on the pre-oxidized Ir film. The RBS measurement showed that the chemical composition ratio of Pb/Zr+Ti on the pre-oxidized Ir film was about 3.5 larger than that on the non-oxidation Ir film, 1.3. This means that oxidation of Ir film has a role to suppress the PbO and PbO2 re-evaporation from the PZT film deposition. The same phenomenon was observed.
in the PZT film deposited from the Zr/Ti = 20/80 target. However, in the case of the Zr/Ti = 80/20 target, the chemical composition of the PZT film doped in Ir film was almost equal to that without pre-oxidation regardless of the number of PbO pellet. Also, the ratios of Pb/(Zr+Ti) for the pre-oxidation cases were decreased with the number of PbO pellet in the same manner. We speculate the reasons for these results as follows. Since some reports have mentioned that XRD peak of (110) IrO$_2$ is observed from the oxidized Ir film, the surface of the pre-oxidized Ir film may contain IrO$_2$(110) phase. Because the lattice constants of (101) PbO plane are 0.605 and 0.383 nm, which are less than the most used, the (110) PbO plane can easily grow on the IrO$_2$(110) phase film. The crystallization of PbO phase prevents itself from decomposition and re-evaporation during the PZT film deposition, which increases the amount of Pb content in the PZT film. On the other hand, IrO$_2$ is thermally stable, oxides containing much of Zr may be hardly decoupled during the deposition. So, for Zr/Ti = 80/20, the chemical composition of the PZT film is independent on the surface state of the Ir film, i.e., oxidized or metallic surface.

D3.19 Effect of excess Cu on dielectric properties of CaCu$_3$(Ti$_{1-x}$Ta$_x$)$_4$O$_{12}$ thin films by pulsed laser deposition. Ram S Katyar, Vinay Gupta, Anju Dixit, Piyush Bhattacharya and Rasmi R Das, Department of Physics, University of Puerto Rico, San Juan, Puerto Rico.

High dielectric constant oxides have become increasingly important in microelectronic applications due to continuous size reduction of microelectronic devices. Cubic perovskites CaCu$_3$(Ti$_{1-x}$Ta$_x$)$_4$O$_{12}$ (CCT) has been paid much attention due to very high dielectric constant (108 [@28]). In this study, the thin films of CCT were fabricated on platinum and Cu coated Pt/TiO$_2$ substrates by using stoichiometric and excess Cu ceramic targets. The thickness of the film is controlled by adjusting the oxygen pressure of 300 to 500 mTorr and the substrate temperature of 400 to 700°C. The X-ray diffraction and atomic force microscopy measurements revealed that the films were polycrystalline in nature having uniformly distributed grains. The Raman vibrational modes of CCT thin films are in agreement with the reported results on bulk CCT. The dielectric constant and the loss tangent for CCT films were investigated in a wide frequency range (100 Hz to 1 MHz) CCT films at different substrate temperatures (100-800 K). The results from the measurement indicate that the dielectric constant increased from 1575 to 2200 in the film deposited with the excess copper at 190 K. The Authors acknowledge the financial support of NSFINT0667018, NASA/NCC3-1034. One of the authors (VG) is also thankful to DST, India, for BOYCAST fellowship and financial assistance.

D3.20 Dielectric Properties of KTa$_2$.53Nb$_{0.46}$Ti$_{0.07}$O$_{2}$. Thin Film using PLD. Hyung-jin Bae1, Jennifer Sigman2, Byoung-seong Jeong1, I A Bonneter2 and David P Norton1, 1Materials Science and Engineering, University of Florida, Gainesville, Florida, 2Solid State Division, Oak Ridge National Laboratory, Oak Ridge, Tennessee.

KTa$_2$.53Nb$_{0.46}$Ti$_{0.07}$O$_{2}$ (KTN) has been intensively studied for its ferroelectric properties in microwave applications and optical waveguide. A key issue for these materials is losses at frequency. One approach to minimizing losses of paraelectrics is through cation distribution. In this study, 3 at% of Ti was doped in KTa$_2$.53Nb$_{0.46}$Ti$_{0.07}$O$_{2}$ (KTN:Ti) target. The Ti doped KTN films were grown on MgO (100) single crystal in different oxygen pressure at 750°C of deposition temperature, and 34 cm$^2$ of laser energy density with 4 cm$^3$ of distance between target and substrate by PLD. The dielectric properties of Ti-doped KTN were observed as a function of oxygen growth pressure and film thickness using C-V measurement. The physical properties of KTN:Ti films were characterized with XRD, and AFM. The loss properties of the Ti doped KTN films will be compared to these for undoped materials.

D3.21 MOCVD Processes for Electronic Materials Adopting Bi(C$_3$H$_7$)$_3$. Precursor: Kinetics and Mechanisms. Cedric Bedoya1, Giuligilo Guido Condorelli1, Giuseppe Anastasi1, Judit Lison2, Dirk Wouters2 and Ignazio Luciano Fregnoli1, 1Dipartimento di Scienze Chimiche, Universita di Catania, Catania, Italy, 2IMEC, Leuven, Belgium.

Bi$_2$O$_3$-based layered-perovskites are promising materials for superconducting electronics and for the non-volatile ferroelectric memories (NVF-FeRAM). Among ferroelectric oxides, SrBi$_2$Ta$_2$O$_9$ (SBT) and Bi(La$_{1-x_1}$Ti$_{1-x_2}$)$_2$O$_{12}$ (BLT) are very attractive materials due to their superior endurance resistance and good retention characteristics under high polarization. High level integration required by commercially competitive 1TIC stacked ferroelectric cells is entirely suited with MOCVD due to the better conformality of deposition and the higher throughput with respect to the other deposition techniques, such as b-diketonates or alkoxides have been proposed as Bi sources to obtain smooth and homogeneous morphologies. These sources, however, require MOCVD reactors equipped with liquid delivery systems (LDS) due to their low thermal stability and efficient sublimation/evaporation processes. Moreover, they are highly moisture-sensitive, thus requiring particular care for storage and manipulations. By contrast, Bi(C$_3$H$_7$)$_3$ is more versatile and conventionally stable precursors, which can be efficiently used in both classical and LDS equipped MOCVD reactors without problems for storage and manipulations. In this paper, we report on an extensive study of MOCVD processes on technological substrates involving Bi(C$_3$H$_7$)$_3$ precursors. A key issue for these materials is losses at frequency. One of the authors (VG) is also thankful to DST, India; 2Instrumentation, Indian Institute of Science, Bengaluru, Karnataka, India.

Photo refractive barium titanate crystals are used for self-pumped phase conjugation in advanced laser systems for laser - beam cleanup via two - wave mixing and for optical interconnects. Dop ing of the Ca in the BaTiO$_3$ ceramics had showed a remarkable improvement in the electromechanical behavior, increase in the temperature range of the stability of the tetragonal phase and inhibited the formation of the unwanted hexagonal phase of BaTiO$_3$. Ba$_{1-x}$Ca$_x$TiO$_3$ [at. % Ca $>$ 0.15, 0.13 and 0.18] targets were prepared by solid state reaction technique and the BCT thin films were deposited on Pt coated Si substrates by pulsed excimer laser ablation technique. The dielectric constant and ferroelectric phase transition temperature in both the bulk and the thin films were found to increase with the increase of Calcium content in Barium titanate matrix. At higher Ca contents, (x > 0.1), a sharper phase transition temperature was observed for the Ca substituting Ba site, while it exhibited a diffuse phase transition with the highest amount of Calcium entering the Ti site with a significant decrease in the transition temperature. This anomaly in the decrease of phase transition temperature has been investigated which could have arisen due to the size effect in ferroelectric domains, intergranular stresses, strain existing at the film - substrate interface. Attempts on the structural correlation of these thin films are also done. There was a diffused phase transition observed for the higher calcium content (> 10 at % Ca) on Pt coated Si substrates and also exhibited frequency independence on temperature beyond the curie temperature. This vividly exhibits a cross over from the ferroelectric to non lead relaxor type behavior observed, for the higher calcium concentration. This might be due to the presence of A site entering the Ti site and creating disorder. There is an evidence from neutron diffraction, of the possibility of the Ca ions going into the B site. As a result of the Ca going into the Ti sites, the energetic and dynamics of the reorientation of the Ca oxygen vacancy (Ca:Vo) pair is affected considerably and the relaxor behavior beyond certain at.% substitution.

D3.22 Preparation of Ferroelectric Ph(Zr$_{0.25}$Ti$_{0.75}$)$_2$O$_5$ Films on Conducting Oxide Ga-Doped ZnO Films for Ferroelectric Transparent Thin-Film Transistors. Kwan Bae Lee1, Kyung Hae Lee1 and Byung Kwon Ju2, 1Computer & Electronic Physics, Sangji University, Wonju, Gangwondo, South Korea; 2Microelectronics Research Center, Korea Institute of Science and Technology, Seoul, South Korea.

We have investigated the feasibility of ferroelectric transparent thin-film transistors using Ph(Zr$_{0.25}$Ti$_{0.75}$)$_2$O$_5$ (PZT) and Ga-doped
ZnO (GZO), which act as a ferroelectric layer and a transparent conducting oxide, respectively. Sputter-deposited GZO films having the resistivity of 3×10^4 Ω-cm were obtained at the substrate temperature of 250 °C, and the sol-gel derived ferroelectric PZT films deposited on GZO could be obtained at the annealing temperature of 580 °C in O2 ambient. However, for such conventional annealing, the resistivity of GZO increased rapidly with increasing the annealing temperature, which implied the failure of gate layers. Hence we attempted the rapid thermal annealing (RTA) process in N2 ambient. The ferroelectric PZT films with relative low coercive field 15 kV/cm and 56 kV/cm, respectively. In this study, we also investigated the characteristics of ferroelectric transparent thin-films transistors, basically consisted of the GZO/PZT/GZO structure.

D.3.24 Effect of La-doping on the structure and electrical properties of Sr0.5Bi0.5Te0.2Ox, Ram S Katryan, Nora Ortega, Sudipta Bhattacharyya and Pijush Bhattacharya; Department of Physics, University of Puerto Rico, San Juan, Puerto Rico.

Bismuth-layered ferroelectrics have been the major focus of interest in the field of ferroelectric memories. SBT was one of the foremost candidates belonging to this family, which meet all the requirements of a nonvolatile memory device. Moreover, it is already established that the lanthanum doping in bismuth-layered ferroelectrics significantly alters the processing parameters without compromising in their ferroelectric properties. This led us to dope lanthanum in pure SBT to study its effect on processing and electrical properties. In this report, we have demonstrated that phase pure SBT bulk samples can be synthesized with up to 15 % lanthanum doping without any phase segregation. Sputter-deposited SBT layers were used for depositing thin films by pulsed laser ablation. The XRD patterns indicated the formation of lanthanum ions inside the lattice without any significant peak shift. The absence of any lattice distortion indicated an isovalent replacement of bismuth with lanthanum, which had the same ionic radius. We have compared the normal Raman modes in doped as well as undoped samples. The ferroelectric soft mode (at 27 cm^{-1}) has shifted towards lower frequencies and doping concentration was increased at room temperature. The dielectric constant was nearly constant ( 150) irrespective of the lanthanum content. The thin film data will be compared with those of bulk SBT. The temperature dependence of the dielectric and Raman spectra will be presented in this paper.

D.3.25 The Influence of Composition on Properties and Structure of PZN-PLZT Ceramics; Li Ai Ding1, yang zhang1 and suming li2;
1Key State Lab. of Materials, Shanghai Institute of Ceramics, Chinese Academy of Sciences, Shanghai, China; 2Shanghai Hengtong Optic & Electric Technology Co., Ltd., Shanghai, China.

PZN-PLZT ferroelectric ceramics with different composition has been successfully prepared by hot-pressed sintering in oxygen atmosphere. The results showed that structure and properties sensitively affected by the content of Pb, Zn, Ti and Ti and PLZT. X-ray analysis and SEM in acoustic mode showed that the non-perovskite structure formed easily in PZN-PLZT ceramics as the ratio of PZN/PLZT is larger than 1.[0.3[Pi]N0.7[Sn3O4]0.7[PLZT]0.5] (Li et al. 2003) exhibits excellent optical transparency for wavelength from near ultraviolet to infrared and electro-optical properties. Good piezoelectric properties are shown in [0.3[Pi]N0.7[Sn3O4]0.7[PLZT]0.5] (Li et al. 2003). PZN-PLZT ceramics with both outstanding piezoelectric properties and electro-optical properties can be realized by adjusting the composition and such PZN-PLZT ceramics is useful for MEMS and integrated optic system.

D.3.26 Grain distribution of ferroelectric BT-based films for high-density semiconductor memories; Ween-I Kweon1, Mi-Jin Kim1, Bieyoung Yang1, No-Jin Park2, Sung-Jin Kim2, Suk-Kyoung Hong2, Seung-Suk Lee2 and Young-Jin Park2; 1Materials Science & Engineering, Kumoh National Institute of Technology, Gumi-Si, Gyeongbuk, 730-701, South Korea; 2Memory R & D Division, Hynix Semiconductor Inc., Icheon-Si, Kyongki-do, 467-701, South Korea.

Issues of ferroelectric high-density memories (>64Mb) indispensable for upcoming ubiquitous era have been on the cell integration less than 0.1um2 and reliabilities. Thus nanoscale control of microstructure of ferroelectric films as target of switching polarization has been one of the issues to obtain the uniform electrical properties for realization of high-density memories. In this study the grain orientation and distribution of BT-based films by spin-on coatings were examined by FEG-SEM/EBSD and XRD. Ferroelectric domain characteristics by PFM were also performed to study the dependency of polarizations on grain orientation and distribution. Film process effects such as RTA and furnace annealing on grain orientation and uniformity will be discussed aiming at understandings of the nucleation and growth of the films during the processes.

D.3.27 Influence of the tungsten and nickel dopants on the crystallization and electrical properties of PZT; 1Mania Appanah, Scenio Grove, 2Fujita, 3Denilson Moreira dos Santos1, 2Carlos Oliveira Paiva - Santos2 and Jose Aruna Varela2; 1IBTQ, CMDMC, LIEC, Instituto de Quimica, Universidade Estadual Paulista, Araquara, Sao Paulo, Brazil; 2DFQ, CMDMC, LIEC, Instituto de Quimica, Universidade Estadual Paulista, Araquara, So Paulo, Brazil; 1DQ, CEFET - Maranhao, Sao Luis, Maranhao, Brazil.

Ferroelectrics ceramics based on lead titanate zirconate (PZT) have a remarkable impact on a large number of practical applications in the electronic industry. It has been reported many different methods and dopants to obtain PZT ceramics with better properties. Nevertheless, chemical based processes have been revealed as a promising preparation route due to their low cost processing and the facility for controlling the stoichiometric of complex systems. The objective of this research was to investigate the influence of the tungsten and nickel dopants on crystallization and physical properties of the Pb(Zr0.53Ti0.47)O3. Pure, tungsten and nickel doped PZT with concentration range from 2 to 8 mol% were prepared by the polymeric precursor method. The samples were decomposed at 300°C during 4 hours and calcined at 760 °C for 3 hours. The samples were sintered at 1100 °C for 3 hours in a closed system. The influence of dopants concentration on the structural, microstructural and electrical properties were investigated by X-ray diffraction, scanning microscopy and transmission electron microscopy. The main diffraction patterns of powders showed that there are only PZT crystalline phase. The addition of nickel shift the shrinkage temperature to low values while tungsten shifts the shrinkage temperature to higher values compared to pure PZT. The highest values for remanent polarization, Pr ( 40 mC/cm2) and coercive field Ec (1200 V /cm) were observed for the sample doped with 8 % molar of tungsten.

D.3.28 Analysis of Ferroelectric Microcapacitors by Scanning Probe Microscope; Nobuhiro Kin1, Kiichiro Honda, Fujitsu Laboratories Ltd., Atsugi, Japan.

In order to promote the development of higher density FRAM, the cell size should be reduced. Therefore, the size effects resulting from processing and the physical properties must be measured. So it has become important to study the electrical characteristics of a single bit cell capacitor. On the other hand, as the characteristic of ferroelectric material, it is known that the Ec increases at low temperatures and then falls at high temperatures. In order to evaluate the impact of temperature on the ferroelectric, we constructed a new evaluation system based on scanning probe microscope, which was able to measure the electric characteristics of a single bit cell capacitor. This system is used in the temperature range from -120°C to 300°C. It is realized by circulating liquid nitrogen around a SPM stage and an electrical heater. We measured the electrical properties of ferroelectric microcapacitors by using a sample with a IrOx/PZT/Pt structure. As a result, 2Pr is 41.9 [μC/cm2], Vc+ is 0.8 [V] and Vc- is 71.1 [V] at 25°C. However, at -45°C, 2Pr is 41.9 [μC/cm2], Vc+ is 0.8 [V] and Vc- is 71.1 [V]. That is, it can be shown that Ec increases 15% at low temperatures also in an actual FRAM single bit cell capacitor.

D.3.29 Structural and electrical investigations on laser ablation grown Ba-xCaxTiO3 thin films on Si substrate in MFS structure; Victor Pushparaj1, J. Nagaraju2 and S.B. Krupanidhi1; 1Materials Research Center, Indian Institute of Science, Bangalore, Karnataka, India; 2Instrumentation, Indian Institute of Science, Bangalore, Karnataka, India.

Ferroelectric thin films are playing a vital role in the areas of MEMS, microwave applications, capacitors and electro-optic devices. The Ba0.65Ca0.35TiO3 crystals play an important role in the application of electro-optic modulators and related devices. There are very few reports in the open literature on Ba1-xCaxTiO3 thin films and hence in this study we have grown Ba1-xCaxTiO3 (0 < x < 0.15) thin films (thickness ~ 0.3μm) by pulsed excimer laser ablation technique on p-type Si substrate in Metal-Ferroelectric-Semiconductor (MFS) configuration. A thorough electrical and structural analysis has been made on the integration of Ba1-xCaxTiO3 thin films on Si substrate. The structural studies involves the Micro - Raman spectroscopy.
SIMS, SEM, TEM and the electrical characterization involves the C-V measurement, dc leakage current conduction behavior and interface states measurement. The leakage current of dielectric constant calculated in the accumulation region was found to decrease with increase of Ca in Ba site of the $Ba_{1-x}Ca_{x}TiO_3$. The interface states calculated were order of $10^{-17}$ eV$/cm^2$ for $Ba_{1-x}Ca_{x}TiO_3$ thin films deposited on the Si substrate. As $x$ increases, the interface states was found to increase which could have arised due to the decrease in grain size (i.e. when larger amount of Ca replaces Ba site) which leads to large number of dangling bonds at the interface. These investigations are very essential in order to have a good electric-optic modulator on the Si substrate.

The Space Charge limited conduction mechanism was found to obey the dc leakage current behavior observed in our case.

D3.30 Effect of different annealing procedures on microstructural and electrical properties of CSD derived BST thin films. Sandip Halder1, Theodor Schneider2 and Rainer Waser1, 1IWE-II, RWTH Aachen, Aachen, NRW, Germany; 2Institut für Festkörperorschung, Forschungszentrum Juelich, Juelich, NRW, Germany.

Processing of BST thin films is becoming more and more important for microwave electronics and for its probable incorporation in future high density DRAM's. A correlation between processing and final device characteristics is of utmost importance. Differences in microstructure and electrical properties were observed when chemical solution deposited thin films of BST were annealed using a conventional diffusion furnace and a rapid thermal annealing furnace. Films were prepared by depositing a solution made by the all propionate precursors (APP) route, of different concentrations (0.1M-0.3M), on Pt coated silicon wafers and crystallized between 550°C and 700°C. Cross sectional SEM on the films reveal differences in microstructure for the films annealed by different methods. Differences of the microstructure are also visible when films are annealed at different concentration are used. The electrical properties of the films were found to vary considerably. Frequency dependence of dielectric constant and IV measurements were performed on the different types of films.

D3.31 Suppression of Read-Out Data-Disturb Effect by Novel Ferroelectric Gate-Arrays. Eiichi Takahashi and Hiroyasu Saiki; Precision and Intelligence Lab, Tokyo Institute of Technology, Yokohama, Japan.

One-transistor (1T) type ferroelectric random access memory (FeRAM) using ferroelectric-gate transistors is promising for future nonvolatile memory applications. To read-out the stored data from transistor-arrays of 1T-type FeRAM, the drain current of the non-accessed devices should be zero, regardless of the ferroelectric polarization. In other words, the device should be normally-off. To realize this, the threshold voltage should be controlled by channel ion-implantation or changing the work function of the gate electrode material. However, when the read voltage is applied to read-out operation after the device is retained at VG = 0, the drain current for read-out operation becomes small, because the operation point of the device goes into one of the minor P-E hysteresis loops. In this work, to overcome the read-out data disturbance, we propose a new method to suppress the disturbance. The details of our method will be at first been discussed. First approach is the use of a splitgate structure, where an additional MOSFET is equivalently connected to the ferroelectric-gate FET. The MOSFET is used to cut off the drain current when VG = 0. On the other hand, the ferroelectric-gate FET can be remained on state when VG=0, hence, the device still can use the major P-E loop and produce large on drain current. SPICE simulation demonstrates that the drain current for read-out becomes much smaller than that in the write process for conventional ferroelectric-gate FETs, whereas the degradation in the read drain current is negligible for the proposed new structure. Second approach is a new device structure which consists of a MOSFET with a ferroelectric-gate transistor and an additional normal dummy capacitor, where both two capacitors are connected to the gate of MOSFET. When the device is retained at VG = 0V, this capacitor is negatively biased because of the remnant polarization of ferroelectric capacitor, which compensates the total charge applied to the gate of MOSFET. Hence, the device can realize off state when the gate voltage is zero and still can use a major P-E loop for read-out operation. P-E characteristics required for the ferroelectric-gate transistors are also discussed in the presentation.

D3.32 Microwave Dielectric Properties of Modified CaTiO3-Based Ceramics Systems. Jing Tao and Chen Wen; Department of Material Science and Engineering, Wuhan University of Technology, Wuhan, Hubei, China.

The microwave dielectric properties of CaTiO3-based system were investigated, especially for temperature coefficient of resonant frequency (TCF). Perovskite-type dielectric ceramic, CaTiO3, with high dielectric constant and high dielectric quality factor Qf and unacceptable negative TCF, was modified by CaMg1/3Nb2/3O3(CMN), Li1/2La1/2TiO3(LLT) and Al2O3(AlO), which all have negative TCF, to form compounds system: (1-x)CaTiO3-xCMN/LLT/AlO. The compounds present excellent microwave dielectric properties: near-zero TCF at certain x value and remain high dielectric constant and low dielectric loss. The temperature compensated series show adjustable properties as a function of the composition of the materials. The microstructure of the films and properties for the dielectric compounds, such as top-shared Ti-O octahedron, cation order and structure stability, were also discussed.

D3.33 Structural, Dielectric and Pyroelectric Properties of Lanthanum modified Lead Titanate Thin Films.

Tae Kim1 and Jung Ho Park2

Lanthanum modified lead titanate (Pb-x La1-x TiO3) thin films were deposited by sol-gel spin coating process on ITO coated 7059 glass substrates. Investigations have been made on the crystal structure, surface morphology, dielectric and ferroelectric properties of the films. For a better understanding of the crystallization mechanism, the structural investigations were carried out at various annealing temperatures (900°C, 950°C and 650°C). Characterization of these films by X-ray diffraction show that the films annealed at 650°C exhibit tetragonal structure with perovskite phase. Replacement of lead in titanate lead titanate results in reduction of tetragonal ratio (c/a), resulting in better mechanical stability. The dielectric properties of the films were also carried out by X-ray diffraction. AFM images are characterized by slight surface roughness with a uniform crack free, densely packed structure. Dielectric, pyroelectric, and ferroelectric studies carried out on these films have been discussed.

D3.34 Single transistor type ferroelectric memory with Pt/Sr0.8Ti0.2O3/Pt/CeO2/Si MFMIS gate structure.

Sim H Shim1, 2, Ik Soo Kim1, Yong Suk Kwon1, Seong-II Kim1, Yong Tae Kim3 and Jung Ho Park2

1systems technology division, Korea Institute of Science and Technology, Seoul, South Korea; 2Electronical Engineering, Korea University, Seoul, South Korea.

The single transistor type ferroelectric random access memory (1T Type FRAM) has advantages over the capacitor type FRAM in nondestructive readout and small cell size. In spite of its advantages, there are still many problems. The metal ferroelectric metal insulator semiconductor (MFMIS) gate structure have been proposed for overcoming the major problems. The metal ferroelectric metal insulator semiconductor (MFMIS) gate structure have been proposed for overcoming the major problems. In order to lower the operating voltages and prevent the insulating layer from breaking down, the insulating layer with high dielectric constant and the high area ratio of MIS capacitor to MFM capacitor were required because the voltage induced the insulating layer decreases and the voltage induced the ferroelectric layer increases. We have developed the MFMISFET with CeO2 film as a high-k insulating layer. The CeO2 film with the thickness of 20 nm was deposited by rf sputtering of Ce target in the reactive oxygen ambient and annealed at 800°C for 30 min in the oxygen ambient. The MFMIS capacitor gate MFMISFET were fabricated with various area ratios and the electrical characteristics were investigated. The SrBi2Ti2O9 (SBT) film was used as a ferroelectric gate material. The inductively coupled plasma reactive ion etching (ICP-RIE) system was adopted to remove the useless ferroelectric film and electrode. The drain current - gate voltage (I_D-V_G) characteristics with the area ratio of 2 showed the threshold voltage difference of 1.3 V at the 5 V operating voltage. The drain current - gate voltage (I_D-V_G) characteristics showed that the drain current difference between programmed on state and erased off state was more than 2 orders at the operating voltage of 3 and 5 V, respectively. The electrical performance of MFMISFET shows that it has good ferroelectric memory characteristics and programmable operation.

D3.35 Dielectric properties of epitaxial Ba0.5Sr0.5TiO3 films on silicon substrates using bi-axially oriented ion-beam-assisted deposition technique.

Saiki; Precision and Intelligence Lab, Tokyo Institute of Technology, Yokohama, Japan.

The microwave dielectric properties of Ba0.5Sr0.5TiO3-based system were investigated, especially for temperature coefficient of resonant frequency (TCF). Perovskite-type dielectric ceramic, Ba0.5Sr0.5TiO3, with high dielectric constant and high dielectric quality factor Qf and unacceptable negative TCF, was modified by CaMg1/3Nb2/3O3(CMN), Li1/2La1/2TiO3(LLT) and Al2O3(AlO), which all have negative TCF, to form compounds system: (1-x)Ba0.5Sr0.5TiO3-xCMN/LLT/AlO. The compounds present excellent microwave dielectric properties: near-zero TCF at certain x value and remain high dielectric constant and low dielectric loss. The temperature compensated series show adjustable properties as a function of the composition of the materials. The microstructure of the films and properties for the dielectric compounds, such as top-shared Ti-O octahedron, cation order and structure stability, were also discussed.

The nonlinear dielectric property of Ba$_1-x$Sr$_x$TiO$_3$ makes it very attractive for electrically tunable microwave devices. Recently, there have been many studies to obtain a large capacitance change ratio [$\text{tunability} = (C_{\text{max}} - C_{\text{min}})/C_{\text{max}}$] of Ba$_1-x$Sr$_x$TiO$_3$ films grown on single crystal oxide substrates, such as LaAlO$_3$ and MgO. In order to achieve silicon compatibility, we have deposited epitaxial Ba$_0.9$sro$_0.1$TiO$_3$ (BST) films on silicon substrates using pulsed laser deposition, by introducing a bi-axially oriented MgO as the template layer. The epitaxial BST films were successfully grown at 750°C under a 10 Torr oxygen. The dielectric properties of the BST films were measured in coplanar capacitor structures by depositing gold electrodes on top of the BST surface. The structural properties of the BST films were found to be closely related to the in-plane mosaic spread of the template layers. The effects of the crystallinity of the BST films on their dielectric properties were investigated. This work demonstrates the importance of the crystalline quality of the template layers in pursuit of silicon-compatibility of the tunable microwave devices using BST films.

D3.36
Investigations of Pb$_{1-x}$Sr$_x$-TiO$_3$ Thin Films and Ceramics for Microelectronic Applications, Masanori Jair, Yu J. Yunoyuk, R. S. Katsyna, Y. Sonu, A. S. Bhule, F. A. Miranda and F. W. VanKeuls, 1Physics, University of Puerto Rico, San Juan, PR; Puerto Rico; 2Physics, Rostov State University, Rostov-on-Don, Russian Federation; 3Materials Research Institute, The Pennsylvania State University, University Park, Pennsylvania; 4NASA Glenn Research Center, Cleveland, Ohio; 5The Ohio Aerospace Institute, Cleveland, Ohio.

We have investigated electrical and optical properties of thin films and ceramics of (Pb$_{1-x}$Sr$_x$)-TiO$_3$ (PST) in the complete range. The Curie temperature and the lattice parameters of Pb$_{1-x}$Sr$_x$-TiO$_3$ (PST-x) solid solutions were found to be dependent upon Pb/Sr ratio. Only one phase transition in the PST system (compared to three in Ba$_1-x$Sr$_x$-TiO$_3$) was recorded. The studies indicate that PST has potential for tunable microwave devices in the paraelectric phase whereas in the ferroelectric phase it is suitable for ultra-large-scale integration (ULSI) devices. The thin films of PST deposited on platinum-substrate were polycrystalline and those on lanthanum aluminum (LAO) were highly (100) oriented. These films were characterized in terms of their electrical properties and dielectric behavior at low frequencies (1kHz-1MHz). Eight element coupled micro-strip phase shifters on SiON and CVD-WSix film are used for gate insulator and gate electrode, respectively. Workfunction of CVD-WSix gate estimated from C-V measurements was 4.3eV. Therefore, CVD-WSix gate is an attractive material as metal gate electrode for nMOSFETs. We measured the relationship between the Si/W ratio of CVD-WSix and the capacitance change ratio of MOSFETs. In this study, we fabricated CVD-WSix gate transistors by using Damascene gate process. After dummy gate removal, ion implantations were carried out through the gate groove in order to form local channel profiles for high performance transistors. Activation annealing by spike RTA at 1000°C Plasma SiON and CVD-WSix film are used for gate insulator and gate electrode, respectively. Workfunction of CVD-WSix gate estimated from C-V measurements was 4.3eV. Therefore, CVD-WSix gate is an attractive material as metal gate electrode for nMOSFETs. We measured the relationship between Tinv and gate leakage current (Jg) and gate dielectric breakdown voltage (Vbd) of MOSFETs. Vth variation of L=1μm/10μm CVD-WSix nMOSFETs can be suppressed to be lower than 8mV in 22chip. In CVD-WSix gate MOSFETs, where gate length is 50nm, a drive current of 380μA/μm was achieved for effective field of 1100V/μm. In addition, the electric resistances of these materials were measured by C-V and DC, and 10$^{15}$Ω are similar to that of CaTiO3. The structures changes gradually from CaTiO3 to HfO2 below the Curie temperature in both compounds. The thin films of PST-x solid solutions were found to be dependent upon Pb/Sr ratio.

8:30 AM D4.1

As traditional poly-silicon gated MOSFET devices scale, the additional series capacitance due to poly-silicon depletion becomes an increasing fraction of the total gate capacitance, excessive boron penetration causes threshold voltage shifts, and the gate resistance is elevated. To solve these problems and continue aggressive device scaling we are studying metal gates with suitable work-functions and sufficient physical and electrical stability [1,2,3]. Our studies of metal gates on HfO2 indicate that excessive inter-diffusion, inadequate phase stability, and interfacial reactions are mechanisms of failure at source drain activation temperatures that must be considered during the electrode selection process.

SESSION D4: Metal Gates
Chair: Marc-Aurel Nicolet
Wednesday Morning, April 14, 2004
Room 2006 (Moscone West)

9:00 AM D4.2
Highly Reliable Metal Gate nMOSFETs by Improved CVD-WSi6 films with 4.3eV of Workfunction, Kazuaki Nakajima, Hiroshi Nakawaz, Katsuyuki Sekine, Koji Matsu, Tomohiro Sato, Tomio Katata, Kyochi Suguro and Yoshikata Tsunashima; Toshiba corporation Semiconductor company, Yokohama, Japan.

In this paper, we first propose an improved CVD-WSi6 metal gate with 4.3eV of workfunction as gate electrode for nMOSFETs and the relationship between the Si/W ratio of CVD-WSix and the capacitance change ratio of MOSFETs. In this study, we fabricated CVD-WSi6 gate transistors by using Damascene gate process. After dummy gate removal, ion implantations were carried out through the gate groove in order to form local channel profiles for high performance transistors. Activation annealing by spike RTA at 1000°C Plasma SiON and CVD-WSix film are used for gate insulator and gate electrode, respectively. Workfunction of CVD-WSix gate estimated from C-V measurements was 4.3eV. Therefore, CVD-WSix gate is an attractive material as metal gate electrode for nMOSFETs. We measured the relationship between Tinv and gate leakage current (Jg) for same Tinv. The CVD-WSix gate MOSFETs, where gate length is 50nm, a drive current of 380μA/μm was achieved for effective field of 1100V/μm. In CVD-WSix gate MOSFETs, where gate length is 50nm, a drive current of 380μA/μm was achieved for effective field of 1100V/μm. In addition, the electric resistances of these materials were measured by C-V and DC, and 10$^{15}$Ω are similar to that of CaTiO3. The structures changes gradually from CaTiO3 to HfO2 below the Curie temperature in both compounds. The thin films of PST-x solid solutions were found to be dependent upon Pb/Sr ratio.

9:15 AM D4.3
High-permittivity dielectric materials and metal gate materials are currently being investigated by many research groups world-wide in an effort to continue the aggressive dimensional scaling of metal oxide semiconductor devices. The development of relatively high-quality deposited gate dielectrics to replace SiO2-based dielectrics for silicon field effect transistors presents an opportunity to consider alternative materials for the semiconductor channel in such devices. There are many fundamental advantages to using Ge in the channel in place of Si. The relative instability of GeO2 with respect to most high-k metal oxides under oxidizing conditions may avoid growth of an undesirable low-k interfacial layer under the deposition conditions used to form the high-k gate dielectric, in contrast to the typical need for high-k deposition on Si. Furthermore, use of Ge may result in lower temperatures for dopant activation compared to Si. The larger (and better-matched) low-field carrier mobilities in Ge relative to Si result in devices that operate beyond the universal mobility model for Si MOSFETs. In this presentation, results obtained from atomic layer deposition- and UV-ozone oxidation-synthesized metal oxide dielectric layers on Ge (100) substrates will be compared. Physical characterization of the interfacial, structural, and electrical properties of ALD ZrO2 and HfO2 dielectrics on Si substrates after removal of the interfacial oxide. To prepare high-k dielectric films, ZrO2 and HfO2 films were deposited using atomic layer deposition (ALD) on Si substrates passivated by a thin chemical oxide layer. Pt, Al, and Ti were deposited as gate electrodes via room temperature e-beam evaporation. Microstructural and chemical analyses were performed using HR-TEM, EELS, and annular dark field STEM imaging. Electrical properties such as C-V and I-V characteristics were compared using capacitor structures fabricated in devices that operate beyond the universal mobility model for Si MOSFETs. In addition, this novel dielectric technology has led to the demonstration of high-performance Ge MOSFETs with enhanced carrier mobility. To study the scalability of the gate-stack and inspect the existence of an interfacial layer, high-resolution cross-sectional transmission electron microscopy (HR-TEM) was used to examine the ZrO2-Ge interface microstructure; though the poor quality Ge native dielectrics for gate insulator and field isolation have hindered the realization of Ge MOS devices in the last four decades. Inspired by the recent successes of the high-k dielectric deposition technique on Si and the thermodynamically unstable nature of the common germanium native oxides, we have investigated the possibility of applying high-k dielectrics to Ge without a native oxide interlayer. We have fabricated MOS capacitors on Ge with zirconia gate dielectric using ultraviolet-assisted oxidation (UVO) of thin Zr metal at room temperature on Ge surface with various treatments. In addition, this novel dielectric technology has led to the demonstration of high-performance Ge MOSFETs with enhanced carrier mobility. To study the scalability of the gate-stack and inspect the existence of an interfacial layer, high-resolution cross-sectional transmission electron microscopy (HR-TEM) was used to examine the ZrO2-Ge interface microstructure; though the poor phase contrast between ZrO2 and GeOx (if any) mandates a better physical characterization. In this presentation, we analyze the elemental composition variation across the dielectric layer by applying synchrotron radiation photoemission spectroscopy (SR-PES) to ZrO2 on Ge samples wet etched in an atomic layer scale. Core-level spectra for Ge have been taken at specific kinetic energies to minimize the Zr shell photoemission cross-section and thus avoiding interference. These spectra were then peak fitted and modeled to extract elemental depth profile. Lastly, their impact on future Ge MOSFET scaling will be addressed.
Strained Si devices can provide significant mobility enhancements for both electrons and holes and is being aggressively studied by many research groups. The incorporation of high-K dielectrics on strained Si devices allows the additional benefit of low gate leakage current. In addition, the ultimate gate depletion problems and Fermi level pinning associated with polysilicon electrodes, metal gates are also necessary. This warrants the investigation of high-K gate dielectrics and metal gate electrodes with strained Si devices. Issues that need to be understood include the i) interfacial layer formation of strained Si/high-K dielectrics, ii) effects of metal gate electrodes on high-k dielectrics, and iii) corresponding effects on the channel strain. In this paper, strained Si films were deposited on (100) relaxed SiGe virtual substrates by chemical vapor deposition (CVD). Different Ge compositions in the SiGe substrate and different strained Si thickness were formed to introduce varying strain levels which were confirmed by Raman spectroscopy. HfO2, one of the most promising high-K gate dielectrics, was deposited by physical vapor deposition (PVD) of thin Hf layers followed by oxidation at 600 C in N2 for 30s. Different metal gate electrodes, both element metal and binary metal alloys, were deposited by PVD and MOS capacitors were fabricated. The paper will discuss the electrical characteristics of metal-gate high-K dielectrics and present a comparison of EOT, flatband voltage, interface traps, leakage current and work function between strained Si samples and bulk Si controls. Also the interfacial layer formation of strained Si/high-K system will be investigated and compared with bulk Si/high-K. Finally, thermal stability of EOT, flatband voltage will also be presented.

11:30 AM D5.5/B5.5
Retarded Growth of Sputtered HfO2 Films on Germanium.
Koji Kita, Masashi Sasagawa, Masahiro Toyama, Kentaro Kyuno and Koji Kita, Masashi Sasagawa, Masahiro Toyama, Kentaro Kyuno and Yukihiro Saito; Dept. of Materials Science, Tokyo Institute of Technology, Tokyo, Japan.

Ge CMOS has recently attracted much attention, because of the trend of using deposited high-k films than thermally grown SiO2 for further scaling of CMOS devices, and of the intrinsically higher carrier mobility of Ge than that of Si. In this paper, we report a new advantage of high-k dielectrics over both the interface layer and the HfO2 film on Ge are thinner than those on Si despite of simultaneous fabrication processes. HfO2 films were deposited simultaneously on Ge (100) and Si (100) wafers, after removing the native oxides. In order to restrict the interface layer thickness, an ultra-thin Hf metal layer was deposited, followed by the HfO2 film deposition by a reactive sputtering of Hf in O2/Ar. By using TEM and a combination of the glancing incident X-ray reflectivity (GIXR) with the spectroscopic ellipsometry measurements, the interface layer thickness was accurately determined to be 0.5 nm on Ge and 1.1 nm on Si, for the samples annealed at MOCVD-HfO2 (0.1%)-N2+4N ambient. This result shows that the interface layer thickness on Ge is only a half of that on Si even though the films on both substrates were processed simultaneously. The ultra-thin Hf metal layer has an important role for thinner interface layer formation on Ge, since no difference of interface layer thickness was observed when HfO2 films were deposited directly on both substrates without high-k metal layers. This phenomenon can be explained if it is assumed that Ge oxides may form a Hf-Ge-O ternary volatile compound with Hf metal. If this is the case, the total HfO2 film thickness (without the interface layer) on Ge must be thinner than that on Si. The fact is that the HfO2 film on Ge was 0.6 nm thinner than that on Si with TEM and GIXR measurements. Furthermore, the film thickness difference (ΔT Ge = T HfO2 (Si) - T HfO2 (Ge)) was observed after annealing, and then it can be assumed Hf-Ge-O volatilization would occur during the film deposition process. It is worthy of particular attention that ΔT Ge was seen as a retardation of the film growth on Ge in the very early stage of the growth. Thus it is inferred that the Hf-Ge-O volatilization would occur with the assistance of oxygen plasma until the ultra-thin Hf metal is fully oxidized, and that it is the key mechanism for forming a thinner interface layer and a thinner HfO2 film on Ge than those on Si. Finally, C-V characteristics of Au/HfO2/Ge and Au/HfO2/Si MOS capacitors were characterized. As was expected from the thickness difference of both interface layer and HfO2 film discussed above, HfO2/Ge MOS capacitor showed a larger accumulation capacitance than HfO2/Si, even though they were fabricated simultaneously by the same process conditions. These results show new advantages of high-k/Ge over high-k/Si system from the viewpoint of fabricating a CMOS with ultra-thin high-k gate dielectric.
some fundamental limitations of high-k materials on the electrical response of MOS capacitors and nanoscale transistors. Two important current sources of leakage have been considered: the quantum fluctuations in the high-k layer and the physical dielectric thickness versus its equivalent-oxide-thickness (EOT) for very high-k materials. The first one is now well-identified to induce a stretch-out of the capacitance-voltage characteristics and threshold voltage dispersion, the second problem is known to be at the origin of the loss of the electrostatic control of the channel by the gate electrode. In both cases, we will illustrate with simulation results the importance of these two problems for decananometer devices and we will push our investigations to ultimate double-gate devices working in the ballistic regime.

2:00 PM D6.2
Electronic structure of Nitrided High K gate oxides.
John Robertson, P W Peacock and G Shang; Engineering, Cambridge University; Cambridge, United Kingdom.

Nitrogen is often added to gate oxides to improve their reliability, performance, either by co-oxidation or deposition, or by annealing in a nitrogen containing atmosphere. This is also true for high dielectric constant oxides such as HfO2 or the silicates and aluminates. We have calculated the effect of nitrogen on the electronic structure of the oxides. Nitrogen atoms were added to supercells of HfO2, La2O3 and HfSiO4, withdrawing oxygen so as to maintain an insulating configuration. The total energy of the structure was relaxed to find the equilibrium configuration. We find that in general nitrogen prefers a 4-fold coordinated configuration. We find that N introduces N 2p states above the valence band maximum. This narrows the band gap by about 1.2 eV. This reduces the valence band offset. Nevertheless, we find that even in La2O3 which has a smaller VB offset, the offset is still large enough to act as an adequate hole barrier. The conduction band offset remains large enough.

2:15 PM D6.3
Ab Initio Dielectric and Dynamical Properties of High-k Oxides.
Alexio Filippetti, Pietro Delugas and Vinizio Fiorentini; Dept. of Physics, University of Cagliari, Monseirato, Italy.


2:30 PM D6.4
Defect Levels in SrTiO3, HfO2, ZrO2 and La2O3.
K Xiong, P W Peacock and John Robertson; Engineering, Cambridge University; Cambridge, United Kingdom.

The leakage currents, stability and reliability of high dielectric constant (K) gate oxides will depend on their intrinsic defect energy levels. There have been few calculations of these defect levels. In many cases, for those levels high in the band gap, the results are affected by the correction of the band gap for the error in the local density formalism used. Here we find the energy levels and behaviour of oxygen vacancies in key oxides, by referencing the levels to those of possible shallow donors next to the conduction band edge. This is the so-called ‘marker method’ which has been used for wide gap systems like diamond. The method is tested on oxygen vacancies in SrTiO3 using substitutonal La as a reference. The vacancy is found to be shallow, as it is in SrTiO3. It is then used for vacancies in ZrO2, where the results correspond well to those of Louie et al using the GW approximation. These results allow us to build up a more accurate picture of the vacancy and interstitial levels in these wide gap systems.

3:15 PM *D6.5
Physical structure and electrical characterization of MBE deposited high-k dielectrics.
Athanasio Dimoulas1, George Apostolopoulos1, Ab03 Hf02 to be 3.5 eV and 3.1 eV, respectively. Measurements and Hf0 2 fluctuations in the high-k layer and the physical dielectric thickness above the oxide valence band maximum. This narrows the band spectra, dielectric constants, and band structure of selected high-k oxides such as HfO2 or the silicates and aluminates. We have calculated the effect of nitrogen on the electronic structure of the oxides. Nitrogen atoms were added to supercells of HfO2, La2O3 and HfSiO4, withdrawing oxygen so as to maintain an insulating configuration. The total energy of the structure was relaxed to find the equilibrium configuration. We find that in general nitrogen prefers a 4-fold coordinated configuration. We find that N introduces N 2p states above the valence band maximum. This narrows the band gap by about 1.2 eV. This reduces the valence band offset. Nevertheless, we find that even in La2O3 which has a smaller VB offset, the offset is still large enough to act as an adequate hole barrier. The conduction band offset remains large enough.

Using molecular beam epitaxy (MBE) we investigated a number of other factors which may influence the electrical quality of the high-k layers, such as the stability of the oxides on silicon, the microstructure, the Si in-diffusion and the mass density of the oxides were studied using a large variety of in-situ and ex-situ methods such as RHEED, HRXRD, XRR, HRTEM, ToF SIMS and XPS. [1] P. Masson et al., Appl. Phys. Lett. 81, 3392 (2002).

2:45 PM D6.6
Measurement of high-k dielectric stacks for nonvolatile memory applications by internal photoemission.
Julie D. Casperson1, L. Douglass Bell2, Robert J. Walters3, Damon B. Farmer1, Roy G. Gordon3 and Harry A. Atwater1; 1Watson Laboratory of Applied Physics, California Institute of Technology, Pasadena, California; 2Jet Propulsion Laboratory, Pasadena, California; 3Department of Chemistry, Harvard University, Cambridge, Massachusetts.

Solid state memory device speeds are limited by electron tunneling through the gate dielectric barrier. By fabricating dielectric gates from multiple layers of dielectric materials, with appropriate band offsets and dielectric constants, voltage application can make the electron tunneling barrier to be lowered, resulting in significantly faster read/write times, without sacrificing retention time. Such silicon-compatible layered barrier heterostructures that enable a large drop in the barrier height with applied voltage are promising candidates to replace single dielectric films as the tunnel barriers for nonvolatile memories. Floating gate MOS capacitor structures have been fabricated using these heterostructures as the tunnel barrier and results will be presented. Additionally, the voltage-dependent barrier lowering may also form the operating principle for a new class of photodetectors with electrically-tunable cutoff wavelengths. We have modeled and fabricated silicon-compatible, layered high-dielectric constant structures that enable voltage injection from the source electrode to a floating gate or contact electrode that can be modulated by an applied bias. We utilize an effective mass-based tunneling model to predict the current-voltage characteristics and carrier distributions in layered tunnel barrier structures under applied bias. We find from our simulations that some of the most promising structures for layered tunnel barriers consist of Al2O3 with HfO2 and we have fabricated such structures. We have fabricated and characterized the layered barrier structure HfO2/Al2O3/HfO2 as well as single- and double-layered structures using these materials. The Al2O3 and HfO2 were deposited by atomic layer deposition. Experimental characterization of tunneling and band offsets has been performed using current-voltage, capacitance-voltage, and internal photoemission spectroscopy measurements. Internal photoemission spectroscopy measurements have been performed on metal-insulator-semiconductor structures with semi-transparent gates in order to directly measure the band offsets of layered tunnel barriers using a tunable x-ray lamp source for illumination. Our measurements indicate band-offsets for SiO2 and Al2O3 to be 3.5 eV and 3.1 eV, respectively. Measurements for other single dielectrics and heterostructures will be presented.

4:00 PM D6.7
Pr4f occupancy and VB/CB band offsets of Pr2O3 at the interfaces to Si(001) and SiC(0001) surfaces.
Dietrich Schneider1, Applied Physics, BTU Cottbus, Cottbus, Germany; 2IHP, Frankfurt, Germany.

Resonant photoelectron spectroscopy (PES) at the Pr4f and Pr3d absorption edges is used to study the electronic properties at the interface of epitaxial grown Pr2O3 on Si(001). We compare these results to Pr2O3 films grown on SiC(0001) surfaces. In the electronic structure of bulk Pr2O3 the valence band (VB) states are predominantly of Pr3d and O2p atomic parentage. Weak contributions...
from Pr4f states are identified from the strong increase of the VB formed. At the Si(OOl) interface in-situ prepared epitaxial layers show an offset of 2eV as well as a 1eV increase in the electron affinity caused by an interface dipole moment. In addition, there is a negative space charge within first 1nm of the Pr2O3 layer, most probably caused by Pr vacancies. The offset of the conduction band is deduced from the onset of the Si2p and Pr4d XAS data, it is of the order of 2eV again. Our data allow to derive a full description of the interface properties of that high K material, a prerequisite for its possible application in storage, logic, and power electronics.

4:15 PM D6.8

The physical metrology of high-k layers: how can we obtain an accurate measurement of composition and thickness?

Thierry Conard1, Hugo Bender2, John Wolstenholme1, Roumen Vitchev3, Laurent Houssiau3, Andreas Bergmaier4 and Wilfried Vandervorst1

1MCA, IMEC, Leuven, Belgium; 2ThermoVGScientific, East Grinstead, United Kingdom; 3LISE, FUNDP, Namur, Belgium; 4University of Munich, Munich, Germany.

With the downscaling of the gate insulator (SiO2) in advanced metal-oxide-semiconductor (MOS) devices, one expects its thickness to reach the fundamental limits both from the point of view of gate leakage current as well as from intrinsic reliability. A solution to this problem is the use of dielectric layers with higher electrical permittivity than SiO2. Consequently, alternative gate insulators with high electrical permittivity are currently widely investigated for the future generations of MOS transistors. The mainstream research concentrates on Hf based oxide systems but the understanding of the Pr4f electronic contributions to the electronic properties of these films remains a challenge. Many different analysis techniques are usually considered for the determination of thickness and/or composition of thin layers. Among those, one usually finds Ellipsometry, TEM, XPS, TOFSIMS, XRR, ETD, RBS ... In the first part of this study we concentrate on the metrology aspect of the analysis of those layers through the intercomparison of results obtained on a limited set of sample composed of HfO2, Al2O3 and their mixture. From these analyses we were able to determine the necessary physical parameters (electron mean free path, dielectric function, ...) in agreement with the different analysis techniques. Recent development in the field of high-k dielectrics include the presence of nitrogen in or around the stack (interfacial layers and/or nitride capping layer). In this study, both MOCVD and ALD/ALCVD layer deposition technologies are considered. For the high-k dielectrics, it is very important to be able to acquire knowledge of the density distribution of the nitrogen in the layers with enough accuracy. This remains a real challenge for SIMS due to varying matrices in which the nitrogen is distributed. Next to the usual operational mode (Xe, Ar and Cs profiling in positive and negative detection modes), we investigated the possibility of nitrogen detection through the use of MCs+ clusters while reducing surface Cs concentration at low energy by a Xe-Cs co-sputtering set-up. We also recently introduced the possibility to detect nitrogen through the detection of CN -clusters by a carbon flooding scheme. This work has been extended now and its results will be validated against some known layer structure.

4:30 PM D6.9

Structural Properties of (ZrO2)x(AI2O3)1-x on Si (100).

Ming Zhu1,2, Peng Chen1, Ricky K. Y. Fu1, Weili Liu1, Chenglu Liu1 and Paul K. Chu1

1City University of HongKong, Hong Kong, Hong Kong; 2Shanghai Institute of Microsystem and Information Technology, Shanghai, China.

(ZrO2)x(AI2O3)1-x composite films were deposited on p-type Si (100) substrate by ultra-high vacuum electron-beam co-evaporation at room temperature, followed by rapid thermal annealing (RTA) conducted in N2 ambient for 30s at 1000℃. The X-ray diffraction (XRD) conducted to determine the crystallization temperature and high-resolution transmission electron microscopy (HRTEM) was used to study the interfacial quality and the morphology of the (ZrO2)x(AI2O3)1-x film annealed at 900℃. The chemical compositions and thermal stability of the annealed samples were determined by x-ray photoelectron spectroscopy (XPS) and the current-voltage characteristics were measured by producing a multi/individual structures.

SESSION D7: Silicenites and Nitrogen Incorporation into High-K Layers

Chairs: Jean Pompeyrin and Michel Housa

Thursday Morning, April 15, 2004

Room 2006 (Moscone West)

8:30 AM D7.1

A Review of HFSION Gate Dielectrics

Luigi Colombo, Texas Instruments, Inc., Silicon Technology Development, Dallas, Texas.

Hafnium based dielectrics are the most common high-k gate dielectrics being investigated today to replace the incumbent reliable silicon oxynitride. While many have reported on both HfO2 and HfSiON, HfSiON has better thermal stability against crystallization, better electrical stability as EOT degradation and leakage current degradation with annealing, can be scaled to <1nm with poly Si, has less trapped charge, and has higher channel mobility. Overall, based on the data available HfSiON is a robust dielectric. However many high-k dielectrics including HFSION have a large flat band offset with respect to the expected flat band voltage. The objective of this presentation is to review basic material characteristics, deposition processes, dielectric scaling, thermal and electrical stability characteristics, reliability properties and limitations poly Si gates.

9:00 AM D7.2

Nitrogen distribution in HFO2, N2gate dielectrics deposited by MOCVD using [CF3-H2, Hf with NO and O2]. Minseo Lee1, Dolf Landheer2, Xiaohua Wu3, Martin Couillard3, Zhenghong Lu4, Wui Tung Ng5 and Gianluigi Bottin5

1Materials Science and Engineering, University of Toronto, Toronto, Ontario, Canada; 2Institute for Microstructural Science, National Research Council Canada, Ottawa, Ontario, Canada; 3Brockhouse Institute for Materials Research, McMaster University, Hamilton, Ontario, Canada; 4Electrical and Computer Engineering, University of Toronto, Toronto, Ontario, Canada.

Crysalization temperatures of less than 500℃ and high impurity
diffusion rates are serious concerns if HfO₂ is to replace silicon oxide nitride as a gate dielectric in deep submicron CMOS applications. Nitrogen incorporation was reported to improve these properties in sputter-deposited HfO₂ films [1]. This paper describes the deposition and characterization of HfO₂:N₂ gate dielectrics deposited by metal organic chemical vapor deposition (MOCVD) using tetraethyl(hydrido)hafnium (TDEAH, [C₂H₅SiH₂]₄Hf) and NO.

The films were analyzed by x-ray photoelectron spectroscopy (XPS), high resolution transmission electron microscopy (HRTEM), and electron-energy loss spectroscopy (EELS). Si <100> substrates were given an HF-last RCA clean and introduced into an ultra high vacuum cluster tool with a low pressure MOCVD chamber, in-situ XPS spectrometer, and an evaporation chamber with a high-temperature-quartz-halon in-situ heating stage. By introducing TDEAH and oxidizing gas, either O₂ or NO, into the MOCVD system in separate pulses, we deposited high-purity HfO₂:Nₓ films. The N is XPS peak had (N-O), (N-H), and (N-C) components due to N bonded to O, Hf, and C, respectively. The (N-O) component, due to unreacted NO, was detected on the surface of the films deposited by XPS. Post-deposition thermal annealing. The distribution of the N in the films was determined by EELS and by XPS coupled with etch-back in 1% HF solution. Using standard sensitivity factors for the O is (O-Hf), N is (N-H), and Hf and its atomic concentrations were determined by XPS analysis of the films deposited with NO as the oxidant was determined to be 11 ± 1% while those deposited with O₂ was 4 ± 1%. The interface layer depositing on O₂ was silicon dioxide, while with NO it was silicon oxynitride, but a contribution from sub-oxides cannot be ruled out. HRTEM images revealed that the HfO₂:Nₓ films containing 11% nitrogen stayed amorphous following post-deposition annealing at 1000°C in vacuum.

Oxidation of the HfO₂:Nₓ using a rapid thermal processor resulted in a shift of the Hf 4f 7/2 XPS peak away from that of pure HfO₂ at 17.9 eV and a reduction in the N Is (N-H) peak, indicating that bulk nitrogen was replaced by oxygen. This reduction in N concentration was investigated by EELS analysis. We are grateful to S. Moas and T. Quance for technical assistance. M. S. Shaheen, J. J. Chambers, A. L. P. Rotondaro, A. Shanware, and L. Colombo, Appl. Phys. Lett., 80, 3183 (2002).

9:15 AM D7.3
Nitridation of Hafnium Silicate Thin Films, Howard Chatman¹, Yoshi Senzaki², and Wesley Nieveen²; ¹Aviza Technology, Inc., Scotts Valley, California; ²Charles Evans and Associates/Evans Analytical Group, Sunnyvale, California.

High-quality gate dielectrics with higher dielectric constant to replace SiO₂ are required to meet future device requirements as the integrated circuit device scaling continues. Conventional gate oxides suffer from leakage and reliability deficiencies as the silicon oxide thickness decreases below 1.8 nm. Acceptable high-k gate dielectric materials must be thermally stable with Si and provide good electrical properties. MoₓOᵧ, zirconia, and silicate form of these materials have been studied as promising alternatives to SiO₂ [1], with the Hf-silicate materials being the leading candidates. HfSiON is of particular interest as it remains amorphous and shows no leakage current degradation or increase in EOT (equivalent oxide thickness) even after annealing at 1100°C in an inert gas [2]. We have developed an atomic layer deposition (ALD)-based HfSiON process using volatile liquid precursors at temperatures below 250°C. The use of ALD allows us to process at low temperatures and provides good electrical properties [3]. In this paper, we discuss the nitridation of ALD-deposited hafnium silicate films by post-deposition NH₃ rapid thermal annealing or by remote nitrogen plasma annealing. Nitrogen concentration [N] as measured by X-ray photoelectron spectroscopy (XPS) is determined as a function of the annealing temperature and other process conditions for both nitridation methods. The effect of [N] on the electrical properties determined from the current-voltage and capacitance-voltage characteristics of HfSiON films were with and without additional high temperature annealing. Information on the structure and properties of HfSiON and the resulting interface with Hf(hafnium)-based dielectrics through many research efforts over the past years, the optimal dielectric composition is still not evident. Biological issues such as degradable carrier mobility, large Vfb shift, and charge trapping still need to be resolved, i.e. dielectric charge properties need to be well understood. In this work, we first investigated the compositional dependence of the scaling limit of HfSiON films, using a figure of merit introduced in The direct tunneling leakage current model for bulk-Si CMOS transistors. Pure HfO₂ is predicted to have an advantage over Hf-silicates. However, A HfO₂ film typically is accompanied by an interfacial layer which significantly increases the equivalent oxide thickness (EOT). By employing an interfacial Si₃N₄ diffusion barrier, the formation of this interfacial layer can be suppressed, to allow for more effective EOT scaling. Alternatively, if a relative permittivity of 11 can be achieved, 20%silicate (without an interfacial layer) can be used to improve than HfO₂ (with an interfacial layer). We have recently developed new...
methodologies for characterizing the bulk and interface charge properties of dielectric films. Surface charge analysis (SCA) is used to extract interfacial charge densities, fixed charge densities, and near-interface trap densities of ultra-thin dielectrics, and is useful for tracking the influence of post-deposition processing on the HfO2/Si interface charge properties. Spectroscopic ellipsometry is used to determine the structural properties of the films. An additional absorption peak is observed within the bandgap of HfO2, and its intensity is clearly correlated with leakage current and near-interface trap densities. Based on our observations, the defects within the HfO2 films are likely to be oxygen vacancies.

11:00 AM D7.7
High Quality HfSiOxY Gate Dielectrics Fabricated by Solid Phase Reaction between Metal Hf and SiO2 Underlayer. Heiji Watanabe, Motofumi Saitoh, Nobuyuki Ikaraishi and Toru Tatsumi; NEC Corporation, Sagamihara, Kanagawa, Japan.

High permittivity metal oxides, such as HfO2 and its silicate, have been extensively studied as alternative gate dielectrics. The main concern with high-k gate devices is to improve the film and interface properties. Imperfections in high-k films that were introduced from source gases must be eliminated, and the insertion of SiO2 underlayers is indispensable to improve interface properties. Current research in high-k thin film fabrication has been focused on depositing the metal oxides using CVD techniques. However, we think that high-quality film should be prepared by interface reactions just like oxidation at the SiO2/Si interface. Previously, we proposed a novel high-k fabrication method based on interface solid phase reaction between metal and SiO2 underlayer for preparing La-silicate gate dielectrics using CVD techniques. In this study, we report on an investigation of physical and electrical properties of HfSiOy gate dielectrics by the solid phase reaction method and results from its physical and electrical characterization. Thin Hf-metal layers ranging from 0.2 to 1 nm thick were deposited on SiO2 underlayers using low-damage PVD equipment. The PVD system has sufficient controllability and film uniformity. High-quality HfSiOy gate dielectrics were formed by diffusing Hf into the oxide underlayer. In this method, the metal composition and profile were controlled by the Hf layer thickness and annealing conditions. The permittivity of the oxide underlayer increases due to metal diffusion; however, the thickness of the insulator becomes thicker than that of the initial SiO2 underlayer. An EOT of less than 1 nm was achieved and we confirmed that the silicate films endure activation annealing. When using a conventional poly-Si gate electrode, the gate leakage reduction compared with SiO2 ranged from two to four orders of magnitude depending on the amount of Hf metal. The interface trap density was in the order of $10^{10} \text{eV}^{-1} \text{cm}^{-2}$ and hysteresis of C-V curves was as low as 10 mV ($2 \text{V} - 2.5 \text{V}$). These results clearly indicate advantages of this solid phase reaction based method for the fabrication of high-quality high-k gate dielectrics. [1] H. Watanabe et al. Appl. Phys. Lett. 83 (2003) 3546.

11:15 AM D7.8
Effect of plasma and different oxygen precursors on stability of hafnium oxide and hafnium silicate thin films grown on Si(100). Hanah Bahu Chandrasi, Ping Chen and Tonya M Klein; Department of Chemical Engineering, University of Alabama, Tuscaloosa, Alabama.

The downscaling of MOSFET devices has brought considerable attention to the possible high-k dielectric replacement for SiO2, owing to its high leakage current. Hafnium oxide and hafnium silicate are among the alternative high-k dielectric materials being considered for its thermal and chemical stability. Hafnium oxide thin films were grown using plasma enhanced chemical vapor deposition (PECVD) reactors using different oxygen precursors such as N2O, water vapor and high purity O2. Silane was used to grow hafnium silicate thin films using different oxygen precursors. Hafnium-silicide was used as the precursors for the thin films grown. These films were then compared with those grown without the plasma source. Profilometer and X-ray diffraction (XRD) were used to determine the deposition rate and crystallinity. The films were characterized for atomic composition using X-ray photoelectron spectroscopy (XPS) and the depth profile was performed using Auger electron spectroscopy (AES) for different thermal treatments.

11:30 AM D7.9
Systematic Examination of Boron Diffusion Phenomenon in HfSiOx High-k Gate Insulator. Masato Koyama, Tsunehiro Ito, Yuuchi Kaminata, Masamichi Suzuki, Chie Hongo and Akira Nishiyama; 1 ASL, Toshiba Corp., Yokohama, Japan; 2 ADL, Toshiba Corp., Kawasaki, Japan.

Boron penetration is a major issue when integrating high-k gate dielectrics into conventional CMOS devices, because this phenomenon is reported to be enhanced in high-k materials such as Al2O3 and HfO2 compared to the case of SiON. HfSiOx is thought to be a promising high-k material since it has high resistance to boron diffusion even at high-temperature (1000 oC) [1]. It is suggested that the suppression of the film crystallization by N-incorporation is responsible for the improved boron penetration [2]. However, a more comprehensive understanding, such as its dependence on the film composition, is necessary. Boron diffusion in HfSiOx films was systematically examined, widely changing the film composition (Hf/(Hf+Si) = 22-80%, [N] = 5 at.8%). Thick HfSiOx films (100 nm) were deposited onto Si substrates by co-sputtering of Hf and Si targets in an Ar/O2/N2 ambient, followed by deposition of poly-Si layers with 300 nm thickness. Boron ions were implanted into poly-Si layers at an acceleration energy of 30 keV with a dose of 5E15 atoms/cm2. Specimens were annealed at 1000 oC for 30 min, in order to drive boron atoms into the HfSiOx films. Poly-Si layers were then completely removed by dry etching and boron profiles inside the HfSiOx films were measured by means of SIMS (secondary ion mass spectroscopy) from the surface of the specimens. Good fit of the experimental results to the complementary error function is due to the boron diffusivities in the material. As a result, we confirmed that boron diffusion in HfSiOx decreased monotonically with increasing [N] of the film when Hf/(Hf+Si) was almost the same. It was also shown that higher [N] leads to the suppression of the film crystallization through the annealing by XRD (x-ray diffractometry). Based on these results, we think the film microcrystallization plays an important role in the microscopic diffusion process of boron. On the other hand, we also found that the diffusivity increased for one order of magnitude by increasing Hf/(Hf+Si) from 20% to 60%, even at the same [N] content that is high enough to keep the film in an amorphous state ([N] > 30 at.%). This experimental finding indicates that additional factors determine the diffusivity should be taken into account. The dominant factors of boron diffusion in HfSiOx with various chemical compositions will be clarified and presented in this paper. [1] M. Koyama et al., Tech. Dig. Int. Electron Devices Meet., 2002, p849. [2] M.A. Quevedo-Lopez et al., Appl. Phys. Lett., vol.82, 2003, p4699.

11:45 AM D7.10

A major problem in fabrication of high-k dielectric films to substitute SiO2 in future CMOS technologies is the interface engineering. The density of interfacial traps Dit is low when a SiO2 buffer layer separates the substrate from the film, but this very buffer increases the equivalent oxide thickness EOT of the gate dielectric stack. Self-contradicting demands (low Dit and low EOT) may possibly be efficiently compromised in high-k silicates grown by solid phase reaction. For this purpose, an ultrathin thermal SiO2 is grown and then enriched with metal in-diffused from a deposited metal layer, so that a high-k silicate is obtained. We report results of structural and electrical measurements for ultrathin silicates obtained by Pr in-diffusion. Depending on the growth and annealing conditions, films with various morphologies, composition, and electrical parameters are obtained. We interpret these observations in terms of formation energies obtained from ab initio calculations and from experimental thermodynamic data, focussing on the physical mechanisms responsible for the resulting EOT. We discuss feasibility of the in-diffusion method for preparation of high-quality gate dielectrics with EOT below 1 nm and conclude that a careful tailoring of growth and annealing procedure is needed to avoid hazardous inhomogeneities in composition of the film which are detrimental to its electrical performance.

SESSION D8: Ferroelectrics I
Chair: Athanasios Dimoukas and Tzu Joe King Thursday Afternoon, April 15, 2004 Room 2006 (Moscone West)

2:00 PM D8.1

Ferroelectric thin films have attracted considerable attention for use in a wide range of wireless communications products. For advanced digital-baand circuits, high-density, embedded ferroelectric memory (FeRAM) based upon Pb(Zr,Ti)O3 (PZT) has the potential to be a low-power, high-performance substitute for embedded DRAM, SRAM, and Flash technologies. In the RF front end of wireless devices, the large and voltage-variable permittivity of (Ba,Sr)TiO3 (BST) is being exploited for thin film varactor and high-density capacitor applications, and shows considerable promise for use within compact, frequency agile front end modules. Moreover, the
piezoelectric properties of PZT may be exploited for a variety of filter and sensor components. In this presentation, we will review recent advances in the field of ferroelectric thin films, noting how high resolution TEM (HRTEM), and chemical solution deposition (CSD), and the relative merits of each will be reviewed. Next, requirements for diffusion barriers, adhesion layers, and capacitor electrodes are presented, and high frequency stabilization schemes described. The primary sources of integration-induced damage will also be addressed, and strategies to mitigate their effects reviewed. Finally, the requisite electrical properties of these capacitors at high frequency will be described in detail.

2:30 PM D8.2
Sharp Ferroelectric Phase Transition in Strained Single-Crystal SrRuO3/Ba0.7Sr0.3TiO3/SrRuO3 Capacitors. Regina Dittmann1, R. Plonka2, E. Vasco1, N. A. Persson1, J. Q. He3, C. L. Jia1, S. Hoffmann-Eifert1 and R. Waser2; 1Institut fuer Festkoerperschung, Forschungszentrum Juelich, Juelich, Germany; 2WTH Aachen, Aachen, Germany.

Single-crystalline all-perovskite SrRuO3/Ba0.7Sr0.3TiO3/SrRuO3 (BST/SRO/BST) thin-film capacitors epitaxially grown on SrTiO3 by pulsed laser deposition exhibit a sharp paraelectric-to-ferroelectric phase transition at 350 K with a maximum permittivity of about 6600. This value is comparable to that of bulk ceramics and exceeds by several times the highest values reported for BST thin film capacitors. A detailed structural analysis, which has been completed at the BST microstructure, of our thin film heterostructures is performed. X-ray and HRTEM measurements indicate the presence of a critical thickness of 10 nm for the formation of misfit dislocations and thickness-dependent lattice strains in our epitaxial BST films. The influence of the strains on the observed temperature and thickness dependence of the dielectric response is analyzed with the aid of a thermodynamic theory. Hence, the increase of the transition temperature by about 40 K relative to the bulk value can be attributed to the in-plane compressive misfit strains. It is shown that the weak decrease of the permittivity with the BST thickness decreasing from 200 to 10 nm can be explained solely by the thickness-dependent strain relaxation in epitaxial films without assuming the presence of low-lying states in the film/electrode interfaces. We compare these results to SRO/BST/Pt thin-film capacitors which have the same crystalline quality but show a paraelectric-to-ferroelectric phase transition which is strongly influenced by the top Pt- BST interface. [1] R. Dittmann, R. Plonka, E. Vasco, N. A. Persson, J. Q. He, C. L. Jia, S. Hoffmann-Eifert and R. Waser, to appear in Appl. Phys. Lett.; 6 Dec. 2003.

2:45 PM D8.3
The Influence of Crystallization Route on the Properties of Lanthanum Doped B4Ti3O12 Thin Films Prepared From Polymeric Precursors. Anaemii Junior1, Cristiane Quinelato1, Carla dos Santos Ricciardi2, Mario Cilenio1, Andreia Nascimento3, Marin Aparecida Zaghete1, Jose Arana Varela1 and Elson Longo,1; 1Physics-Chemistry, Chemistry-Institute-Unesp, Araraquara, Sao Paulo, Brazil; 2Physics-Chemistry, Chemistry-Institute-Ufscar, Sao Carlos, Sao Paulo, Brazil.

Polycrystalline lanthanum doped B4Ti3O12 thin films were synthesized on Pt/ITO/SiO2/Si substrate using the polymeric precursors solution. The spin-coated films were specular and crack-free and crystallized after annealing at 700 degree Celsius for 2 hours. Crystallinity and morphological evaluation were followed by X-ray diffraction (XRD) and scanning electron microscopy (SEM), and atomic force microscopy (AFM). Multilayered films obtained using the intermediate-crystallized layer route present a dense microstructure with spherical grains. Films obtained using the intermediate-crystallized layer precursor have larger grains around 200 nm in size. The dielectric and ferroelectric properties of the lanthanum doped B4Ti3O12 films are strongly affected by the crystallization route. 3:30 PM D8.4
Identification of hydrogen induced atomic deformation in SrBi2Ta2O9 and Ba0.5Sr0.5TiO3. W. J. Kim1, Yong Dae Kwon2, Jeong Yong Lee3, Sungkyun Kwan University & Institute for Nanotechnology, Suwon, South Korea; 2Department of Materials Science, Korea Advanced Institute of Science & Technology, Daejeon, South Korea; 3Department of Materials Science, Korea Advanced Institute of Science & Technology, Daejeon, South Korea.

Even if it has been well known that hydrogen annealing degrades ferroelectric properties, there is no conclusive report to confirm that hydrogen influences on atomic arrangement in SrBi2Ta2O9 (SBT) thin films. In this work, for the first time, we have investigated how hydrogen annealing at Curie temperature causes atomic deformation with higher resolution TEM (HRTEM), and chemical solution deposition (CSD), and the relative merits of each will be reviewed. Next, requirements for diffusion barriers, adhesion layers, and capacitor electrodes are presented, and high frequency stabilization schemes described. The primary sources of integration-induced damage will also be addressed, and strategies to mitigate their effects reviewed. Finally, the requisite electrical properties of these capacitors at high frequency will be described in detail.

3:45 PM D8.5

The investigation of high-K materials such as ferroelectrics in the parasitic phase in integrated circuits presents several challenges. If high-K materials are deposited on-chip or between metalization steps, then those leakage currents include line processing gas composition, deposition temperature and electrode material. Specifically, the atmosphere present during deposition and annealing must be oxygen-free, the deposition and annealing temperature must not exceed 450 C and the electrode material must be etchable with chemical techniques. We studied rf magnetron sputtered BCTZ with Ni electrodes because this system meets all the above requirements. The BCTZ deposition process uses pure Ar as the sputter gas and a substrate temperature of 450 C. Subsequent anneals may be performed in a reducing (forming gas) atmosphere with a little effect on either dielectric constant or leakage current. The Ni electrodes provide a good substrate for BCTZ films and much easier to integrate than Pt films. Observed values for the relative dielectric constant K exceeding 100 were not as high as for BCTZ films on Pt electrodes however these values are sufficient to provide clear advantage over other non-ferroelectric materials. Overall, the device characteristics observed prove that the Ni/BCTZ/Ni capacitor is a valuable technology for on-chip capacitor applications.

4:00 PM D8.6
Epitaxial growth of Ba1-xSrTiO3 thin films by polymer-assisted deposition. Yuan Lin1, Haiyan Wang1, Jang-Sik Lee2, Yuan Li1, S. R. Foltyn1, Quanxi Jia1, G. Collis2, A. K. Burrell1 and T. M. McCleskey2, 1Material Science & Technology Division, Los Alamos National Lab, Los Alamos, New Mexico; 2Structural and Inorganic Chemistry, Division of Chemistry, Los Alamos National Laboratory, Los Alamos, New Mexico.

Ba1-xSrTiO3 (BST) thin films with different Ba/Sr ratio (x=0.3, 0.5, 0.7, 1) were epitaxially grown on (001) LaAlO3 (LAO) substrates using polymer-assisted deposition (PAD) we developed recently. Microstructural studies by x-ray diffraction and transmission electron microscopy show that the films are epitaxial with an orientation relationship of (001)BST/(001)LAO. In order to investigate exactly the same atomic arrangements along [100]BST / [100]LAO and [001]BST / [001]LAO, we performed a comparison study of (001)BST / (001)LAO and [100]BST / [100]LAO. In this presentation, we will review recent developments in this area. 

4:15 PM D8.7
Heteroepitaxial Pb(Zr,Ti)O3 thin film growth by hydrothermal treatment. Kyoon Choi1, June Choi1, Ho-Yong Lee2, and Eui-Seok Choi1; 1Thin Film & Single Crystal Lab, Korea Inst of Ceramic Eng & Tech, Seoul, South Korea; 2Cerameccomp Co., Ltd., Asan, South Korea.

The dense and thick lead mircronate titanate (PZT) films were synthesized via hydrothermal treatment on BstTiO3 (BT) and Bst0.7Ti0.3O3 (BZT) perovskite crystals that are grown by the
solid-state single crystal growth (SSCG). The PZT films were grown in a strong alkaline solution (pH>13.9) with variation of the solute concentration where Zr to Ti weight ratio was 56/44 and no excess lead was added. The film obtained showed an epitaxial relationship with the substrate crystal while the film characteristics depended on the hydrothermal condition. The BTO crystal is determined to be more effective substitute for the PZT film because of their low lattice mismatch.


Microstructure studies of ultra-thin BaTiO3 films (2-10nm thick) show nano-domains having a width as small as one unit cell. High resolution TEM investigation revealed only 180° nano-domains and 90° domain boundaries in a sample with 300nm thickness. These nano-domains are mostly oriented in parallel to the film plane, but few domains were observed out of the plane orientation. The ferroelectric behavior was characterized as a function of thickness to the films plane. A polarization hysteresis loop was recorded even in the 2nm thick-films having a remnant polarization of about 3nC/cm2 and a coercive field of 0.7MV/cm. Fatigue tests show an initial degradation of the remnant polarization at about 107 cycles under a continuous 5Vdc load at a frequency of 1kHz. The values of remnant polarization and fatigue edge are improved with increasing the film thickness. The switching response of the nano-domains is relatively fast in the range of few ms to seconds increasing with increasing applied electric field according to power law dependence with a coefficient of minus 2.5. The dependence of the leakage current on the applied electric field is characteristic to a hopping conductivity mechanism. The measured values of the leakage current density and activation energy are comparable to bulk size ferroelectric films. Two temperature-dependent peaks of dielectric constant were observed; a broad peak that spans between 60-80°C and a narrow peak between 105-110°C. These peaks are attributed to two Curie temperatures associated with the orientation of the nano-domains relative to the in-plane stress direction. The two peaks are slightly shifted towards the bulk Curie temperature as the film thickness increases. A correlation between microstructure, film thickness, film stress and ferroelectric properties is demonstrated and discussed.

4:45 PM D9.9 Thickness dependence of leakage conduction in MOCVD deposited Pb(Zr,Ti)O3 and PbTiO3 thin films. David V. Taylor, Maxim B. Kelman, Lawrence F. Schloss and Paul C. McIntyre; Materials Science and Engineering, Stanford University, Stanford, California.

The next generation of low-power, high density nonvolatile embedded memory technology required for wireless devices will necessitate cost-effective integration with CMOS logic and other components. Among the contenders, Ferroelectric Random Access Memory (FeRAM) appears to be the most advanced. Although FeRAM is considered nonvolatile since the two polarization states are stable even after removal of the device, several long-term reliability issues such as fatigue, imprint and retention loss are of concern. Since these FeRAM device limiting phenomena are believed to be closely related to trapping of electronic charges, detailed leakage conduction studies should shed light on conduction mechanisms which can ultimately lead to memory failure. In addition, major film thickness scaling (<100nm) will be required to meet the operating voltages specified by the International Technology Roadmap for Semiconductors (ITRS). We will present a comprehensive investigation of leakage current characteristics of state-of-the-art MOCVD deposited polycrystalline Pb(Zr,Ti)O3 (PZT) thin film capacitors as a function of film thickness (<100nm) and compare them with those of epitaxial PbTiO3 thin films deposited on (001)-oriented Si substrates. Temperature-dependent measurements are used to assess the conduction mechanisms responsible for the observed leakage behavior.

SESSION D9: MBE, PLD, and MOCVD of High-k Materials. Chairs: Luigi Colombo and Dolf Landheer

8:30 AM D9.1 Deposition of Amorphous La2O3 on Silicon by MBD for Alternative Gate Dielectric Applications. Lisa F. Edge1, Darrell G. Schloen1, Scott A. Chambers2, Matt Copel3, Bernhard Hollander4, and Jurgen Schubert5; 1Materials Science and Engineering, Pennsylvania State University, University Park, Pennsylvania; 2Fundamental Science Division, Pacific Northwest National Laboratory, Richland, Washington; 3IBM T. J. Watson Research Center, Yorktown Heights, New York; 4Institut für Schichten und Grenzflächen ISG-IT, Forschungszentrum Julich GmbH, Julich, Germany.

La2O3 is being studied as an alternative gate dielectric material for the replacement of SiO2 in silicon MOSFETs. A major challenge in the growth of alternative gate dielectrics on Si is the formation of excessive SiO2 at the interface between Si and the high-K gate dielectric. Although this potentially improves device performance and reliability, it impacts adversely on the smallest attainable values of the equivalent oxide thickness, EOT. One technique to prevent the formation of SiO2 is to grow in a low temperature / kinetically-limited oxidation regime. We have investigated the oxidation kinetics of La2O3 from their elemental state to the high-K oxide using reflectance and absorption spectroscopy and XPS. For example, in addition to atomic force microscopy (AFM), x-ray photoelectron spectroscopy (XPS) techniques were used to determine the optical band gap energy and the band offset of the hafnate film on Si, respectively. Contrary to SrTiO3 on Si with a negligible conduction band offset, the alkaline earth hafnate films posses sufficient band gap as well as fairly balanced conduction band offset and valence band offset against Si. These characteristics result in that the hafnate films are very promising as high-k gate dielectric materials for future generation CMOS technology.

9:15 AM D9.3 Alkaline Earth Hafnate Oxide Films on Si(001) Substrates. Zhiyi Yu1, Xiaoming Hu1, Jay A. Curless2, Yong Liang1, Brad Craig1, Karen Moore1 and Rich Gregory2; 1Microelectronics and Physical Sciences Laboratory, Motorola Labs, Tempe, Arizona; 2Process and Materials Characterization Laboratory, Motorola SPS, Tempe, Arizona.

Hf-based metal oxides are attractive for high-k gate dielectric applications in the sub-90nm CMOS technology node. In this work we present a comprehensive investigation of the deposition and properties of alkaline earth hafnate films on Si(001) substrates. Epitaxial strontium hafnate and barium hafnate oxide films were grown by molecular beam epitaxy (MBE) using an ultrathin SrTiO3 buffer layer. The x-ray diffraction (XRD) and Rutherford backscattering spectroscopy (RBS), ultra-violet spectroscopic ellipsometry (UV-SE) and x-ray photoelectron spectroscopy (XPS) techniques were used to determine the optical band gap energy and the band offset of the hafnate film on Si, respectively. Meanwhile, amorphous alkaline earth hafnate films were deposited on Si(100) surface in an MBE chamber. Various in-situ and ex-situ techniques were utilized to characterize these hafnate films. For example, in addition to atomic force microscopy (AFM), x-ray diffraction (XRD) and Rutherford backscattering spectroscopy (RBS), ultra-violet spectroscopic ellipsometry (UV-SE) and x-ray photoelectron spectroscopy (XPS) techniques were used to determine the optical band gap energy and the band offset of the hafnate film on Si, respectively.
from the growth kinetics, show no detectable SiO2 or Si-O bonding at the interface with Si. The films also do not show evidence for interfacial oxidation even after prolonged exposure to air making LaScO2 a promising material for the replacement of SiO2.

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9:30 AM D9.4
Laanthum Hafnate High-κ Gate Dielectrics by MBE. George Vellianidis1, Athanassios Dimoulas1, Georgios Mavrou1, Anastasios Travlos1, Jacob C. Hooker2, Zacharias M. Rittersma2, Marco Panchiulli1, Claudia Wiemer3 and Sandro Ferrani1; 1Institute of Materials Science, NCSR "DEMOKRITOS", Athens, Greece; 2Philips Research Leuven, Leuven, Belgium; 3Laboratorio MDM, INFM, Agrate (Milano), Italy.

Ultimate scaling of devices with EOT as low as 0.5 nm requires high-κ gate dielectrics with atomically sharp interfaces with silicon, which could be obtained by molecular beam epitaxy (MBE) methodologies. The stoichiometric La2Hf2O7 (LHO) compound being lattice matched to silicon is a model material for epitaxial growth. This is a new material which has been investigated before in the context of high-κ dielectrics. We show that the delicate balance between the growth temperature $T_g$ and the O2 partial pressure control the structural and electrical quality of these LHO films. At temperatures lower than 650 °C, the material is amorphous. In as-grown films, the measured EOT decreases from 1.2 nm to 0.7 nm as $T_g$ varies between 600 and 650 °C, compatible with $κ$ values around 20. However, the gate current $J_g$ increases from $6\times10^{-13}$ to $2\times10^{-10}$ A/cm² @ 1V above a critical temperature of $600-650$ °C. This behavior can be attributed to the fact that a low-κ, O-rich interfacial layer is formed at low $T_g$, which becomes unstable at higher temperature given that the growth takes place at a reducing atmosphere with a low partial pressure of O2. At higher temperatures in the range of 720-770 °C the oxide is crystalline with a preferential orientation along the (001) direction of growth. The oxide exhibits a complex microstructure, where the random fluoride and the ordered pyrochlore phases are visible by TEM, the latter continuous from the substrate into the oxide epilayer indicating commensurate growth and perfectly clean interfaces with no interfacial layer as required for aggressive device scaling. However, the exposure of the oxide to O2 prior to growth towards $T_g$ above 600 °C affects the oxide epilayer inducing excess roughness. This prevents the electrical characterization of the crystalline LHO oxides, given that the fabrication and testing of reliable MIS capacitors is not possible unless smooth morphology films are obtained.

9:45 AM D9.5
Epitaxial Growth and Structure of Thin Single Crystal ~Al2O3 Films on Si (111) Using e-Beam Evaporation of Sapphire in Ultra-High Vacuum. Mingwei Hong1, A. Reif Kortan1, J. Raynien Kwo3, Joseph Mannapalam3, S. Y. Wu3 and C. P. Chen1; 1Materials Science and Engineering, National Tsing Hua University, Hsin Chu, Taiwan; 2Physics, National Tsing Hua University, Hsin Chu, Taiwan; 3Industrial Technology Research Institute, Hsin Chu, Taiwan.

Heteroepitaxial growth of insulators on semiconductors and vice versa is of great interest in many branches of science and technology. Typical examples are the growth of GaN on sapphire, which provides a basis for blue, green lasers and LEDs, and the epitaxial growth of insulators on silicon. Hafnium oxide, an amorphous dielectric with very high $κ$ ($κ ∼ 100$), has been extensively employed as an interlayer dielectric in advanced ICs. However, the main challenge for using hafnium oxide as a high-κ material is to grow single crystal layers. The use of hafnium oxide as a high-κ gate dielectric in advanced CMOS technology is limited due to lattice mismatch and high interface roughness. In this work, we report the growth of single crystal Al2O3 films on Si(111). The Al2O3 films were grown by electron beam evaporation of sapphire on Si(111). The growth process was performed in a vacuum chamber with a base pressure of $10^{-9}$ Torr. The substrate temperature was fixed at 600 °C, and the Al2O3 films were grown in situ by electron beam evaporation. The films were characterized using X-ray diffraction (XRD) and atomic force microscopy (AFM). The XRD measurements revealed the presence of a single-crystal Al2O3 film with a preferred [001] orientation, which is in agreement with the orientation of the Si substrate. The AFM images showed a smooth surface with a root mean square roughness of less than 1 nm. These results demonstrate the feasibility of growing high-κ Al2O3 films on Si(111) substrates using electron beam evaporation, which could be a promising approach for the development of high-performance CMOS devices.
Praseodymium oxide (Pr$_2$O$_3$) is a potential high-K dielectric for use in DRAM or CMOS devices. Here we present results on metal organic chemical vapor deposition (MOCVD) and characterization of amorphous and crystalline Pr$_2$O$_3$. The layers were grown on Si(100) by pulsed liquid injection MOCVD in the temperature range 400-750°C. Pr$_3$(tmhd)$_3$ (tmhd = 2,2,6,6-tetramethyl-3,5-heptanedione) dissolved in monoglyme (1,2-dimethoxyethane) or toluene was used as precursor solution. The influence of deposition conditions on film composition, growth rate, crystallization and surface roughness has been investigated. The main parameters influencing film composition and properties were substrate temperature and partial oxygen pressure during deposition. The presence of molecular oxygen in the reactor leads to the growth of Pr$_2$O$_3$ at the most stable phase or its mixture with Pr$_2$O. Only deposition in inert atmosphere (Ar) allows to obtain Pr$_2$O$_3$ films which were amorphous or crystalline depending on the deposition temperature. Crystalline Pr$_2$O$_3$ films can be obtained at the growth temperatures 650°C and higher, while crystalline Pr$_2$O$_3$ films grow in the whole range of studied temperatures (400-750°C). No interaction between praseodymium oxide and silicon at deposition temperature has been observed by XRD. Ex-situ annealing (750°C, vacuum) of the amorphous Pr$_2$O$_3$ films leads to film crystallization. Annealing of crystalline as-deposited films improves the crystallinity of the films. Step coverage studies have been performed for amorphous and crystallized Pr$_2$O$_3$ films. The presence of oxygen in the precursor using as carrier gas a 100 sccm Ar flow under 10-3 torr oxygen partial pressure. Films have been characterized by X-ray diffraction (XRD), transmission electron microscopy (TEM), photoelectron spectroscopy (XPS) and capacitance versus voltage as well as current densities versus voltage measurements. The interfacial composition and its effect on the dielectric properties have been fully examined. Two precursors have been investigated by High-Resolution TEM image and it consists of a SiO$_2$ layer and a bottom praseodymium oxide based layer, about 8 nm thick, having no long range order. The 8 nm bottom layer have shown a selected area diffraction pattern typical of an amorphous layer and its chemical composition has been investigated by Energy Filtered transmission electron microscopy (EF-TEM) analysis using the three windows method. This represents an innovative technique to study chemical composition and film/substrate interface in a non-destructive way. The EF-TEM analysis point to the formation of three layers whose chemical composition has been assessed to be: a SiO$_2$ layer at the Si interface, an oxygen-rich 8 nm layer, and the praseodymium oxide amorphous layer. Moreover, in order to establish the chemical composition of the amorphous layer, films grown for 10 minutes consist of a 8 nm layer have been analyzed by angle resolved X-ray photoelectron spectroscopy. The recorded spectra at various incidence angles (20, 45 and 80 degrees) point to the formation of a silicate interfacial layer. The formation of multiple layer stacks consisting of REO/RE$_2$O$_3$/SiO$_2$, where RE is an element of rare earths, has been already observed for other RE elements such as Y and La, in both physical vapor deposition (PVD) and chemical vapor deposition (CVD) processes. Polycrystalline Pr$_2$O$_3$ and amorphous Pr-silicate films have shown interesting dielectric characteristics. In particular, the potentiality of the praseodymium silicate amorphous layer as alternative gate dielectrics for complementary metal semiconductor technology has been investigated. Considering all of the desired properties these materials possess, praseodymium silicate could be an excellent materials candidate for advanced gate dielectrics.

The preparation of BST heterostructures by sequential deposition of thin films of low dielectric materials (e.g., MgO or MgTiO₃) and barium strontium titanate by sol-gel technique is demonstrated to be a highly effective approach to synthesize ferroelectric films with low dielectric losses. Although the dielectric constant and tunability are reduced somewhat by the insertion of low dielectric material, the dramatic reduction in the dielectric loss tangent effectively increased the figure of merit of the hetero-structured thin films compared to pure BST films. We prepared BST/MgO and BST/MgTiO₃ (BST-MT) heterostructured films with different thicknesses of BST/MgO/MgTiO₃, and found that there is a considerable effect of the insertion layer on the properties of the heterostructured films. The dielectric properties, including tunability, loss tangents, and phase transition behavior, were measured in the frequency range of 1kHz-1MHz on the films. The synthesized films were used to make eight element coupled microstrip phase shifters and characterized in terms of their degree of phase shift and insertion loss characteristics in a frequency range of 13-15 GHz. BST-MT films showed the figure of merit of 58 JdB measured at 533 kV/cm. In the optimized BST/MgO heterostructured films, the high frequency figure of merit (kHz phase shift/insertion loss), dramatically improved to 87 JdB measured at 533 kV/cm, which is the highest known value measured in the Kα band region for BST based materials. These results represent the current state of the art technology.

Reproducibility Issues for ultra-thin ferroelectric thin film characterization for high density FRAM applications. Choong-Rae Cho, YoungSoo Park, Sang Min Shin and June Mo Koo; MD lab., Samsung Advanced Institute of Technology, Suwon, South Korea.

To realize high-density, low operating voltage ferroelectric random access memory devices, reliability issues such as fatigue, imprint, and retention properties for ultra-thin ferroelectric thin films should be resolved, while these properties have been deteriorated seriously as the film thickness is decreased below 100 nm. We have prepared sets of MOCVD PZT thin films with different thickness from 25 nm to 150 nm on different kinds of pure metal and metal oxide substrates. Several tendencies on thickness dependent dielectric and ferroelectric properties have been observed according to electrode material, which could be explained by intrinsic and extrinsic reasons. From the results on systematic studies of the reliability issues, the feasibility for Gigabit density FRAM would be discussed.

Data Retention Characteristics and Hydrogen-Induced Domain Switching in Barium Strontium Titanate Films. Ji-O, Cho, Yoon-Soo Park, Sang Min Shin and June Mo Koo; MD lab., Samsung Advanced Institute of Technology, Suwon, South Korea.

The electrical properties of ferroelectric thin films strongly depend on the electrode materials and crystalline orientation. In this work, BiₓSr₁₋ₓLa₂₋ₓTiO₃ (BLT) thin films were prepared on SrRuO₃ and Pt electrodes by pulsed laser deposition. The electrical properties of the BLT films on different electrode materials were characterized. Both crystalline orientation and the electrical properties were controlled by the substrate and the type of the bottom electrode being used. Also, it was found that the conductive oxide electrode showed better endurance over Pt electrode especially in data retention and hydrogen-induced degradation in BLT films. The effects of electrode materials and crystalline orientation on the data retention characteristic and hydrogen-induced degradation in BLT thin films will be discussed in detail.
The ITRS roadmap calls for the implementation of high-k material as gate dielectric starting with the 65nm technology generation. This requires high quality interfaces between the high-k dielectrics and Si substrate in the channel region. We investigated the effect of surface preparation prior to high-k film deposition on transistor performance. The surface preparation affects the growth of the high-k film and the final EOT. This work discusses the effect of NH3 anneals and process conditions on high-k transistor performance such as gate leakage, Vt and electron mobility. Transistors were fabricated on 200nm p-type <100> Si substrate using a conventional silicon gate transistor process flow with thin high-k dielectrics deposited by atomic layer deposition ALD. The ALD-HfO2 does not grow very consistently on an HF-last surface. The resulting films exhibit high gate leakage current or non-working devices. However, addition of NH3 pretreatment is shown to affect the properties of the interfacial layer at the silicon/high-k interface, which is critical for controlling the final EOT. An NH3 anneal pretreatment i.e., an NH3 predeposition (PreDA), after HF-last clean led to the reduction of the interfacial layer at the silicon/high-k interface to 5Å which is about 50% thinner than that seen with ALD films grown on chemical oxides without the NH3 PreDA. Lower EOT and lower leakage current are obtained when an NH3 PreDA for ALD HfO2 films follows the HF-last. These surface preparation processes result in an EOT reduction of 4Å to 5Å versus chemical oxides, providing a potential solution to achieving a sub-1nm EOT.

4:30 PM D10.10
IR Absorption Study of HfO2 and HfO2/Si Interface Ranging from 2000cm⁻¹ to 2000cm⁻¹
Kazuyuki Tomida, Haruka Shimizu, Koji Kita, Kentaro Kyuno and Akira Toriumi; Materials Science, The University of Tokyo, Tokyo, Japan.

This paper reports the IR absorption study of HfO2 (HfSiOx) and HfO2/Si interface. Although a number of reports on HfO2 system for CMOS gate dielectric application have been published, no systematic study with the IR absorption has been reported. The IR absorption data provide the local bonding information of the microcrystalline structure, the crystallization, inter-diffusion and reaction. First, the thermal treatment effects on bulk HfO2 and HfO2/Si interface were investigated with FT-IR as functions of annealing temperature, ambient and initial film thickness. 30 nm HfO2 was deposited on FZ-Si wafers by RF sputtering, followed by annealing at 400-1000°C for 5 minutes in O2. In the FT-IR measurement, TGS (2000cm⁻¹ - 600cm⁻¹) & PE-TGS (600cm⁻¹ - 200cm⁻¹) were employed for the wide range of sensitive detection. Before annealing, it was hard to detect any signal mid-IR region, while there was a broad structure in far-IR region. However, after annealing at 600-1000°C all the annealed samples showed absorption peaks around 1070cm⁻¹ and 735cm⁻¹, while in far-IR region absorption peaks at 250, 325, 410, 512cm⁻¹ were clearly observed. The peak intensity of HfO2, particularly the 325cm⁻¹ one, increased with annealing temperature. This fact indicates the local bonding relaxation of annealed samples with the monoclinic phase structure (confirmed by XRD). On the other hand, the 1075cm⁻¹ peak is assigned to the Si-O-Si anti-stretching mode, which indicates that SiO2 was formed at the HfO2/Si interface. To investigate a quantitative difference between the interface grown and thermally grown SiO2 films, the dependence of the peak wave number on SiO2 thickness was compared. As a result, different wave numbers were observed between the interface and thermally grown SiO2. This fact means that the interface grown layer is basically the thermal SiO2 in terms of the network structure. Next, since it is not easy to distinguish a small amount of SiO2 in annealed HfO2/Si system, 20nm HSiO2 was intentionally deposited by the co-sputtering (Ar+10%O plasma) of Si (3%) and Hf, followed by annealing at 400 1000°C for 5 minutes. The sample annealed at 1000°C showed the crystalline structure with monoclinic or orthorhombic, depending on Si %. Only a few at % Si incorporation into HfO2 drastically reduced the IR intensities of typical HfO2 peaks such as 250, 325, 410 and 512cm⁻¹ ones, even though the monoclinic phase was maintained. Further Si incorporation (about 10 at %) into HfO2 showed the crystalline structure change from monoclinic to mixed phase of monoclinic with orthorhombic in XRD analysis, and made a new broad IR peak at 490cm⁻¹ evidently which was quite different from the monoclinic HfO2 spectrum. Those far-IR spectra indicate that the bond structure of HfSiO2 (a few percent of Si) is very sensitive to the amount of Si. Conversely, a small amount of Si substantially changes the local bonding characters in HfO2 film.

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Controlling the metal-oxide-silicon interface role of initial surfactant preparation and post deposition annealing.
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Alternative gate dielectric materials such as HfO2 are required in the future generations of microelectronic devices to enable the rapid scaling of MOSFET devices. As the thickness of gate dielectrics decrease, the electrical performance of the dielectric/Si interface will dominate the transport properties of the MOSFET device. Hence the initial surface preparation of the Si(100) surface prior to the gate dielectric deposition and post deposition annealing can significantly affect the resulting device characteristics. In this work, we investigate the material and electrical properties of ultra thin HfO2 films on Si(100) substrate. The Si(100) surface was pretreated with a thin layer of rapid-thermally-grown SiOx or SiNx, or a thin layer of SiO2 grown by UV/O2 oxidation. HfO2 films were deposited by an atomic layer controlled deposition process involving alternate pulses of HF-t-butoxide precursor and oxygen at deposition temperatures from 390°C to 470°C. Post deposition annealing was performed in-situ in various chemistries including O2, N2, N2O, NH3 and H2/O2 at temperatures from 500°C to 1000°C. MOS capacitors were fabricated by depositing aluminum electrodes on top of the deposited films and followed by photolithographic patterning. Material characteristics of the deposited films were analyzed by x-ray photoelectron spectroscopy (XPS), extended x-ray absorption fine structure (EXAFS), and spectroscopic ellipsometry. XPS measurements indicated the formation of interfacial layer between the HfO2 and silicon and its structural changes upon annealing will be addressed in this talk. EXAFS measurements indicated that the short-range order in these films resembled to that of the monoclinic phase. Capacitance-voltage measurements were performed on MOS devices to extract the dielectric constants, flat band voltage shifts, and interface state densities. Temperature dependent current-voltage measurements were performed to elucidate the conduction mechanisms in these ultra thin films. The as-deposited HfO2 samples yielded dielectric constants from 18-23 depending on the processing conditions and their leakage currents were significantly less than that of SiO2 films at the same equivalent oxide thickness. Post-deposition annealing in O2, NH3 and N2/O2 ambient is found to significantly reduce the leakage currents by orders of magnitude though the overall dielectric constant is reduced by O2 annealing due to the formation of an interfacial layer. Spectroscopic ellipsometry measurements showed notable changes in the dielectric function of the materials upon post-deposition annealing indicating that the bulk properties of the films were affected. Post-deposition annealing in H2 or D2 resulted in reduced interface state densities and improved leakage current characteristics while D2 annealing is shown to increase the reliability of HfO2 dielectrics upon constant voltage stress.