SYMPOSIUM F

Materials, Technology, and Reliability for Advanced Interconnects and Low-k Dielectrics

April 13 - 15, 2004

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* Invited paper
SESSION F1: Scaling and Integration Challenges
Chairs: Richard Carter and John Ekerdt
Tuesday Morning, April 13, 2004
Room 2003 (Moscone West)

8:30 AM F1.1 Challenges for the Aggressive Scaling of Advanced Interconnects. Karen Maxey, IMEC, Leuven, Belgium.

The introduction of low-k materials in IC processes has been very cumbersome. Some key materials aspects in all of the implementation of new materials in such a complex process. Meanwhile, the insight in low-k dielectrics, their properties and their impact on the processing has become much clearer based on a lot of scientific studies. The low-k dielectrics, in an aggressive scaling of narrow Cu wires reveals new phenomena and requires novel solutions to maintain or improve the electrical performance of the wires. In this paper an overview will be given on the status and future of the aggressive scaling of Cu/Low-k technology. The results will be brought in a wider perspective of the specifications for electrical performance in integrated circuits.

10:00 AM F1.2 Molecular Caulking: A Pore Sealing Technology for Ultra-Low K Dielectrics. Jay J. Senkevich1, Vincent Jezewski2, Deli Lu1, William A. Lanford1, Gwo-Ching Wang1 and Toh-Ming Lu2; 1Physics, Rensselaer Polytechnic Institute, Troy, New York; 2Physics, University at Albany, Albany, New York.

Much effort has been undertaken to develop high performance ultra-low k (< 2.2) (ULK) dielectrics to improve the interconnect speed and performance of ultra-large scale integrated devices. metallization issues and their poor mechanical properties have plagued the successful integration of these porous ULK dielectrics. Both of these issues are exacerbated by their open pore structure. We have developed a pore sealing technology, which may allow the successful integration of these materials. We have coined the term Molecular Caulking to describe the materials used with the playlene platform for the chemical vapor deposition of these polymers. They are very unique since they can be conformally coated on demanding geometries pin-hole free at a 10 A thickness. We have shown that the first generation material is selective against copper and can seal porous MSQ after 20 A of deposition. This is roughly the pore diameter of the baseline materials have a very fast lateral growth rate. In the past pores supported TEM grids were made with a 16 um hexagonal grid array. An overview will be give with respect to the Molecular Caulking technology.

10:30 AM F1.3 Understanding Plasma-Induced Damage in Integration of Porous Organosilicate Ultra-Low K Materials. Guanghuang Lin1, S.-T. Chen2, Stefanie Chirila1, Steve Cohen3, Tan Daltom1, Nick Fuller1, Andrew Keelock1, David Klaas1, Kaushik Kunwar2, Nancy Klymko2, Vincent McGahay2, Henry Nye2, Eva Simonyi1, Terry Spooner1, Christy Tyberg2, H. Widman3 and David Gidley1; 1IBM TJ Watson Research Center, Yorktown Heights, New York; 2IBM Microelectronics Division, Hopewell Junction, New York; 3IBM Almaden Research Center, San Jose, California; 4University of Michigan, Ann Arbor, Michigan.

Integration of porous ultra low-k materials into dual damascene Cu interconnects poses significant challenges due to new material chemistry, incorporation of porosity, and degraded mechanical properties. The present work aimed to understand critical materials issues in integration of porous organosilicate ultra-low-k materials, particularly plasma-induced dielectric material damage. Extensive analytical techniques were employed to investigate the chemistry, nanostructure, and electrical properties of the porous organosilicate low-k material exposed to both patterning etch and photoresist strip etch chemistries. These analytical techniques include FT-IR, 29Si Nuclear Magnetic Resonance Spectroscopy (NMR), Rutherford Backscattering Spectroscopy (RBS), X-ray Photoelectron Spectroscopy (XPS), Positronium Annihilation Lifetime Spectroscopy (PALS), Surface Contact Angle, and Scanning Electron Microscopy (SEM), dielectric constant, and breakdown measurements on a metal-insulator-silicon structure.

While patterning etch does not change the electrical properties of the porous organosilicate low-k material appreciably, various photoresist strip etch chemistries cause significant increases in the dielectric constant and leakage current as well as formation of dielectric voids in the resultants of the dry etched porous organosilicate low-k material. The degradation of the electrical properties of the plasma-treated porous organosilicate low-k material is attributed to the de-methylation and partial cleavage of Si-O-Si bonds to form more hydrophilic Si-OH groups in the surface layer. A bilayer model has been found to account for the plasma-treated porous organosilicate low-k material. This bilayer model consists of an unaltered bottom layer and a hydrophilic, denser, higher-K surface layer. The chemistry, nanostructures, properties, and pore-sealing capability of the plasma-damaged surface layer will be presented. Implications of the bilayer model for the integration of porous organosilicate low-K materials will also be discussed.

10:45 AM F1.4 Repair of Porous Carbon Doped Ultra low-k Films Using Supercritical CO2. Bo Xie and Anthony J. Muscat; Chemical & Environmental Engineering, University of Arizona, Tucson, Arizona.

The next generation of low-k dielectric films will contain manufactured pores to achieve dielectric constants below 2.6 for the 65 nm technology node and beyond. Low-k films are needed in device integration to lower power consumption and minimize cross talk between metal lines. Porosity in low-k films and must be cleaned, free of etching damage, and capped before deposition of the barrier and seed layers. Water is introduced into organosilicate low-k layers in the form of silanol (Si-OH) groups during patterning of photoresist. Silanol (Si-OH) groups have no surface tension, which makes it a promising technology for cleaning and repair of porous low-k films. Fourier transform infrared (FTIR) spectroscopy, electrical measurements, and contact angle were used to investigate the effect of adding Si-bearing precursors to scCO2 to repair etched and ashed blanket porous ultra low-k (ULK) methyl silsesquioxane (MSQ) films (JSR LKDS109) (k = 2.5). ULK MSQ films were processed in scCO2 containing 1.2% precursor by volume at 200-300 atm and 45-55°C for 2 min soak times. The results with the Si-bearing precursors hexamethyldisilazane (HMDS) and trimethylchlorosilane (TMCS) showed that both lone (Si-OH) and H-bonded (Si-OH) silanol groups reacted. A k value of 2.5 ± 0.2 was measured on MS devices made using the blanket films. While the silanol etch uptake of water from ambient air. Cross-sectional transmission electron microscopy (TEM) images showed that after 1% HMDS addition to scCO2 at 212 atm and 57°C for 2 min, the pores had nearly spherical geometries with diameters of approximately 100 nm. HMDS and TMCS treatments are an effective approach to repair the degradation of ULK MSQ films due to plasma ashing but work is needed to learn how to completely close off the pores at the surface. Electrical leakage measurements after different steps in the processing sequence are currently being done to complement the CV curves and spectroscopic information obtained on ULK MSQ films. In addition, work is in progress to systematically investigate precursor chemistries.

11:00 AM F1.5 Sidewall Damage and Electrical Performance of Porous Dielectrics in Narrow Spaced Interconnects. Eric Jacob1,2, Youssef Tawfick1,2, Dharmesh Kothari3, Victor Sutcliffe4, Herbert Stratuf1, Stefan Peeters2, Rik Janssens1, Peter Leunissen1, Marleen Van Hove1 and Karen Mex1,2; 1SPDT IMEC, Leuven, Belgium; 2E.E. Dept., Katholieke Universiteit Leuven, Leuven, Belgium; 3affilie at IMEC from, Texas Instruments, Dallas, Texas; 4affilie at IMEC from, LAM Research, Fremont, California.

Recent studies have shown that porous low-k dielectrics are extremely sensitive to exposure to plasma processes, due to the diffusion of reactive species into the film through the pore network. The damage induced in the low-k material upon exposure to dry etch and ash plasmas through recesses sidewalls is a point of major concern in terms of preservation of the dielectric properties. The weight of the damaged dielectric portion will have an increasing effect onto the overall electrical performance as interconnects line spacing shrinks. Meander-fork structures with spacings between 250nm and 70nm are used in this study as vehicle to investigate trends in electrical performance for different dielectric materials and patterning chemistries. SiO2 and SiO2:CH low-k materials with increasing porous volume are compared as Inter-Metal-Dielectrics. For SiO2 the no significant dependence of dielectric performance on interline spacing is found. A clear worsening in leakage and breakdown is observed for the porous materials as the spacing is increased. These external processing damage is found to be larger for increasing dielectric porosity. As indicated by the electrical equivalent sidewall damage [2] extracted from interline capacitance measurements. Line-to-line electrical analysis is also supported by physical characterization of the


In order to meet the RC-delay requirements of future technologies, low-dielectric constant (low-k) back-end integration is required. The 2005 ITRS roadmap indicates dielectric k values of less than 2.7 will be required for the 130nm technology node with a reduction to ultra-low-k (ULK) dielectric k values of less than 2.4 for the 90nm node, and further reduction to less than 2.1 for the 65nm node. While the integration of SiCOH (pSiCOH) prepared by plasma-enhanced chemical vapor deposition (PECVD) has been explored to hybrid polymers on grounded or negatively biased substrates, in the 2003 microelectron devices- beyond their traditional role as photoresists. New areas include their application as low-k dielectrics. Interfaces between organic and inorganic materials are of interest, including in fields such as molecular electronics and organic light-emitting diodes. To date, the great majority of the work concerning the formation of organometallic interfaces on pre-existing organic layers has involved metal thin films deposited by (elemental) evaporation. In the work described here we examine an alternative approach to the formation of inorganic-organic interfaces, namely, the use of organometallic (e.g., Ti and Ta) complexes. Concerning the organic layer itself, we make use of self-assembled monolayers (SAMs) with a variety of organic functional endgroups (OFG), e.g., -OH, -NH2 and -CH3. Using a variety of techniques, including molecular beam scattering and x-ray photoelectron spectroscopy, we have investigated a number of issues that are key to the formation of abrupt and robust interfaces between organic materials and inorganic thin films. These issues include the kinetics and mechanism of adsorption of the organometallic precursors on surfaces possessing different organic functional groups, the ability of the precursor to penetrate the organic layer, and the ability to form uniform inorganic multilayers on the SAMs using atomic layer deposition. In addition to examining the temperature dependence of these processes, using supercritical molecular beam techniques we are also able to examine explicitly the role of incident molecular kinetic energy and beam angle of incidence in promoting reaction between the organometallic precursors and the OFG penetration of the SAM, etc. Finally, in selected cases we are able to compare directly predictions made by ab initio quantum chemical calculations of the reaction kinetics, which provides additional insight into inorganic-organic interface formation.


Organic materials are playing an increasing role in modern microelectronic devices—beyond their traditional role as photoresists. New areas include their application as low-k dielectrics. Interfaces between organometallic and inorganic materials are of interest, including in fields such as molecular electronics and organic light-emitting diodes. To date, the great majority of the work concerning the formation of organometallic interfaces on pre-existing organic layers has involved metal thin films deposited by (elemental) evaporation. In the work described here we examine an alternative approach to the formation of inorganic-organic interfaces, namely, the use of organometallic (e.g., Ti and Ta) complexes. Concerning the organic layer itself, we make use of self-assembled monolayers (SAMs) with a variety of organic functional endgroups (OFG), e.g., -OH, -NH2 and -CH3. Using a variety of techniques, including molecular beam scattering and x-ray photoelectron spectroscopy, we have investigated a number of issues that are key to the formation of abrupt and robust interfaces between organic materials and inorganic thin films. These issues include the kinetics and mechanism of adsorption of the organometallic precursors on surfaces possessing different organic functional groups, the ability of the precursor to penetrate the organic layer, and the ability to form uniform inorganic multilayers on the SAMs using atomic layer deposition. In addition to examining the temperature dependence of these processes, using supercritical molecular beam techniques we are also able to examine explicitly the role of incident molecular kinetic energy and beam angle of incidence in promoting reaction between the organometallic precursors and the OFG penetration of the SAM, etc. Finally, in selected cases we are able to compare directly predictions made by ab initio quantum chemical calculations of the reaction kinetics, which provides additional insight into inorganic-organic interface formation.

2:00 PM F2.2 Using Self-Assembled Monolayers as Model Substrates for ALD. Caroline Mary Wehman1, Anne-Cecile Demas2, Jorg Schulmacher2 and Karen Maes1,1. 1SPDT, IMEC, Leuven, Belgium; 2Electrical Engineering, KUL, Leuven, Belgium.

The trend towards increasing functional density in integrated circuits cannot be supported by traditional materials. Device performance dictates the requirement of an alternative material for the interconnect metal. Low-k dielectric constant (k) and Cu instead of Al for lower resistance wiring. Such interconnect metallization requires the introduction of a barrier layer to prevent Cu diffusion under electrical bias. It is, however, difficult to
obtain conformal barriers of the thicknesses \(< 5 \text{ nm}\) foreseen in future device architectures without resorting to unconventional methods. To this end, the unique self-assembled monolayer (SAM) approach as a novel, conformal method of atomic layer deposition (ALD) of films from W, Ti, and Ta compounds is being investigated. Based on sequential saturated gas phase-surface reactions, the growth rate in ALD is theory layer-by-layer, controlled by the growth rate of deposition cycles. In practice, the early stages of film formation may be non-linear, involving three-dimensional growth depending on substrate reactivity. Due to the heterogeneous nature of low-\(k\) materials, our understanding of the nature of the interface on such mechanisms is limited. In this study, we explore the use of self-assembled monolayers (SAMs), organic films formed spontaneously upon adsorption from the gas or liquid phases, as model substrates for ALD WCN diffusion barriers. The role of the initial surface on ALD-mediated growth mechanisms is limited. In this study, we explore the use of self-assembled monolayers (SAMs), organic films formed spontaneously upon adsorption from the gas or liquid phases, as model substrates for ALD WCN diffusion barriers.

Characterization including X-ray, fluorescence, mass, and electron spectroscopies and high-resolution microscopies are used to evaluate various organic films. Our results showed that the deposition of the alkyl chain length and terminal functionality (competing for methyl, cyano, thiol, halide groups) of silane-derived SAMs can be used to manipulate metal deposition and hence barrier properties. We show that, in a tunable structure and surface chemistry, SAMs provide a novel approach to interface engineering, essential in extending the boundaries of current microelectronics technology.

**2:15 PM F2.3**

Carboxyl terminated molecular assemblies as interfacial diffusion inhibitors for future nano-devices, P.G. Gunnane, Amit Pratap Singh and Ganapathiraman Ramanath; Material Science and Engineering, Rensselaer Polytechnic Institute, Troy, New York.

As the device dimension shrinks systematically, in sub-50 nm scale devices, inhibiting interfacial diffusion is very challenging. Particularly, \(\text{Cu}/\text{SiO}_2\) stack in the Cu interconnect technology for ALD WCN diffusion barriers. The role of the initial surface on ALD-mediated growth mechanisms is limited. In this study, we explore the use of self-assembled monolayers (SAMs), organic films formed spontaneously upon adsorption from the gas or liquid phases, as model substrates for ALD WCN diffusion barriers. The role of the initial surface on ALD-mediated growth mechanisms is limited. In this study, we explore the use of self-assembled monolayers (SAMs), organic films formed spontaneously upon adsorption from the gas or liquid phases, as model substrates for ALD WCN diffusion barriers.

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**3:00 PM *F2.4**

**Growth and Properties of Ultra-thin Composite Ru/Ta Barriers**, John G. Ekardt1, Qi Wang2, Andrew Lemonds1, Tibor Bolom3, Patrick Fitzpatrick1, Wesley Abern1, Yang Ming Sun4 and John M White1; 1Chemical Engineering, University of Texas at Austin, Austin, Texas; 2Department of Chemistry and Biochemistry, University of Texas at Austin, Austin, Texas.

This paper addresses near-zero thickness copper diffusion barriers needed to realize interconnect performance improvements by reducing the RC delay in the sub-50 nm technology nodes. Growth of ultra-thin films of Ru on Ta by chemical vapor deposition (CVD) and growth of ultra-thin Ta films on various dielectric surfaces by atomic layer deposition (ALD), and the supporting surface chemistry to explain the growth processes are presented. The materials properties of the constituent films and the composite films are reported. Composite barrier effectiveness against copper diffusion will be tested in - situ using interconnect dielectric test structures and - in situ XPS analysis will be reported at the meeting. Ruthenium films are selected because of their excellent wetting properties with Ta and Cu, their potential for seedless Cu plating, and the reducibility of its oxide. A low temperature Cu-Si reaction line for ultra-thin Ta and SiO\(\text{2}\) surfaces was developed using ruthenium carbonyl \([\text{Ru}(\text CO)_12]\) as the precursor. Films deposited at substrate temperatures between 423 and 930 K were characterized using - situ X-ray photoelectron spectroscopy (XPS), atomic force microscopy (AFM), and four-point probe resistance measurements. A pure, 3.5 nm thick Ru film with low resistivity (30 \(\mu\) cm) was deposited on SiO\(\text{2}\) at 423 K. Ion scattering spectroscopy (ISS) and Ta 4f XPS peak attenuation indicated that the minimum thickness to form a film thick than Ru film 3.5 nm. Ta-Si bond on SiO\(\text{2}\) is 2.5 nm. The barrier properties will be reported as both the Ru thickness is varied from 2.5 to 5 nm and the Ta thickness is varied from 3 to 6 nm. The ALD deposition of Ta-Si thin films was achieved on SiO\(\text{2}\) at 473 K through the repetition of separate exposures to TaF\(\text{5}\) and Si\(\text{4H}_\text{4}\). Films were deposited and in - situ analyzed by XPS to evaluate growth kinetics, interfacial chemistry with the substrate, and film composition. The first 25 exposures of the early stages of film formation result in a stack comprised of \(\text{Ta/SiO}_2\). Multi-stack and - in - situ XPS show that interfacial diffusion is limited at a rate of 0.1 nm/cycle and films deposited using 50 ALD cycles are about 2.5 nm thick. The Si content, which is uniform throughout the film, can be as high as 40 percent and is dependent on temperature and exposure cycle times. Fluorine concentration is highest at the surface and fluorine persists into the film. On-going experiments to eliminate the fluorine and minimize the silicon will be presented at the meeting.

**3:30 PM F2.5**

**Interfacial differences between sputter-deposited Ru and Ta on low-dielectric substrates: The role of carbide formation**, Jeong K和谐, Xiaopeng Zhao and Jinghong Tong; Chemistry, University of North Texas, Denton, Texas.

We report XPS studies of the interfacial chemistries between sputter-deposited Ru, sputter-deposited Ta on parylene and SiO\(\text{2}\)/Cu low-dielectric substrates. Ruthenium is the subject of increasing interest for ULSI copper-low-k applications, due to its semi-noble nature. The conductive nature of Ru oxide phases may mitigate contact resistance problems. Parylene is contemplated as a pore-sealing material for porous low dielectric substrates. Sputter deposition of Ta on parylene yields a tantalum carbide (TaC) phase approximately 60% thick, prior to the evolution of metallic Ta. Similar results are obtained for Ru sputter-deposited onto an SiO\(\text{2}\)/substrate. Subsequently deposited Cu will not wet TaC, and therefore the formation of a TaC interface phase before metal Cu diffusion limits the formation of Ru and Ta barriers on carbon-containing substrates. In contrast, sputter deposition of Ru on parylene results in conformal growth of the first layer, followed by 3-D nucleation of metallic Ru in the second layer, without carbide formation. Similar results are observed for Ru deposition on an SiO\(\text{2}\)/substrate. These results indicate the formation of a laminar Ru/substrate interface, without thickness limitations imposed by a carbide interphase. These results suggest a substantially higher kinetic barrier to Ru carbide than to Ta carbide formation, since the corresponding enthalpy of formation is greater for Ru carbide. The data also indicate that substantially thinner barrier layers are possible for sputter deposited Ru than for Ta on these materials.

**3:45 PM F2.6**

Formation of ALD Ta(N) Barriers on Porous Trikon Low k Surfaces, Junjun Liu1, Michael Scharnberg2, Junjing Bao2, Paul S. Ho1 and Michael Lu1; 1Microelectronic Research Center, University of Texas, Austin, Texas; 2LSI Logic, Portland, Oregon.

Proper surface chemistry and sealed top surface are important for formation of ultra-thin barrier layer by atomic layer deposition (ALD) on porous ultra-low-k dielectric surfaces. An ALD system with in-situ XPS analysis capabilities was developed to study the formation of ALD barriers on low \(k\) dielectrics. The versatile surface pre-treatments with an atom/ion hybrid source and in-situ XPS analysis capabilities make this system well-suited for studying the effects of surface modification and pore sealing pre-treatments of porous low \(k\) surfaces prior to the deposition of ALD barriers. The formation of ALD Ta(N) barriers on a dense Organosilicate Glass (OSG) film and porous Trikon low \(k\) films under various process conditions has been investigated in detail with in-situ XPS analysis. A long incubation period and slow initial growth rate were observed even on the dense OSG film. More energetic or reactive nitrogen species were found to deplete the methyl groups from the surface and result in a surface with more nitrogen termination. The correlation between the ALD growth rate and surface concentration of Si-O and Si-N bond densities was observed. Addition of sufficient atomic hydrogen species at an optimal substrate temperature was found to be able to enhance the reaction, reduce the metal compound to a more conductive phase and decrease the chlorine impurity concentration. Nitrogen terminated surface with atomic species extracted from NH\(\text{3}\) ECR plasma is also critical to inhibit Cu diffusion. In particular, coordination complex formation between Cu\(^+\) and COOH group and Cu is critical factor to inhibit Cu diffusion. In conclusion, ALD Ta(N) barriers on porous low \(k\) surfaces are possible for sputter deposition of Ru and Ta through on these materials.
Atomic layer deposition (ALD) is an attractive method to deposit ultrathin Cu diffusion barrier films for semiconductor interconnect applications due to the high conformity of deposition. The ALD process relies upon chemisorption of precursor molecules onto the surface of the substrate for nucleation. Thus, ALD processes are inherently sensitive to the starting surface chemistry of the substrate. Integration of ALD with porous low k dielectric materials can be problematic due to the heterogeneous nature of the surface chemistry at a molecular level. These factors complicate the ability of the ALD process to penetrate into the porous structure of dielectrics allowing unwanted internal deposition. This work focused on the ALD WNC process and attempted to assess the sensitivity of the precursor chemistry to the starting surface chemistry. For several material systems from copper oxide to ultra low k dielectric films. An investigation into different surface treatment conditions to modulate the nucleation and growth was also conducted. ALD WNC nucleation and growth was observed to be strongly affected by different substrate materials and surface chemistries. Nucleation was found to be inhibited on hydrophobic closure and surface roughness of the WNC layer was found to strongly close to 2:1, compared to 1:1 of SiC films with higher k. These results will be compared to fundamental reaction chemistry for the WNC process and nucleation and growth models.

4:15 PM *F2.8* Ultra low-dielectric-constant materials for 65nm technology node and beyond, Hao Cui, APMD, LSU Logic Corp., Gresham, Oregon

The impact of different dielectric layers in Cu dual-damascene (DD) interconnects on the overall effective dielectric constant (k) have been studied. Positron Annihilation Lifetime Spectroscopy and Ellipsometric Porosimetry analyses were used to characterize the dielectric constants of amorphous BN. Capacitance-voltage measurements on the Cu/BN/metal stack were employed for analyzing the changes in chemical structure of the BN film after BN growth. Growth parameters were optimized to minimize the diffusion and chemical reaction within the nanoporous substrate, which were found to have deleterious effects on the dielectric properties. FTIR, Raman and XPS were employed for analyzing the changes in chemical structure of the low-k films after BN growth. Capacitance-voltage measurements on the Cu/BN/metal stack were employed for analyzing the changes in chemical structure of the BN film after BN growth. Growth parameters were optimized to minimize the diffusion and chemical reaction within the nanoporous substrate, which were found to have deleterious effects on the dielectric properties. FTIR, Raman and XPS were employed for analyzing the changes in chemical structure of the low-k films after BN growth. Capacitance-voltage measurements were used to characterize the effective dielectric constants of amorphous BN (k<2.4) on Si and BN-integrated porous low k materials (k<2.5). LV measurement and SIMS characterization were carried out to estimate the performance of the BN film against copper diffusion. We found that an ultra-thin (20 nm, by XSEM) densified layer that was formed on the surface of LkD after BN deposition may enhance the diffusion barrier performance.
For silicon CMOS microelectronics applications targeted with 65 nm gate lengths, it is expected that low-k dielectric materials with k<2.8 will be required in order to produce interconnection structures with the required minimum gate delay. Research to develop low dielectric constant materials with k<2.8 has tended to concentrate on producing porous films by both CVD and spin on technologies [1]. Integration efforts using designed porous low-k materials have not produced results consistent with expectations based on experiences from established low-k processes at the 130 and 90 nm technology nodes. Continuous Integration with Low-k Technology Development Platform focuses on developing molecular engineering concepts to extend the performance of incumbent organosilicon low-k PECVD processes [2] and produce robust films with k<2.8. In one approach, as an alternative to oxide at the SSQ ratio in the films can be manipulated in a way to reduce the film permittivity. As an example, the experimental performance results of one new carbon enriching PECVD process chemistry have demonstrated it is possible to reduce the relative permittivity to the range of 2.5 to 2.2 with a specifically designed precursor. The properties of engineered one-SiCO:H films are shown in the attached tables. The typical atomic composition of the a-SiCO:H film with the dielectric constant of 2.5 shows a ratio of carbon to silicon of 2.6 by X-ray photoelectron spectroscopy (XPS) and 3 by Rutherford backscattering (RBS). The bulk film density measured by RBS-HFS was 1.2 g/cm3. These films have good electrical isolation characteristics and show thermal stability to 400 C. Unexpectedly, it is observed that while the surface morphology was investigated by transmission electron microscope (TEM). The results from the TEM micrographs exhibit the existence of highly porous structures and the pores size ranged below 15 nm. These hybrid materials would be slightly the mechanical properties of the thin films such as hardness and modulus.

F3.3 Nanoporous Organosilicates Templated from Unimolecular Self Organizing Polymers, Jing-Won Kang, Byung-Ro Kim, Gwi-Gwon Kang, Myung-Sun Moon, Bum-Gyu Choi and Min-Jin Ko, Corporate R&D, LG Chem Ltd., Daejeon, South Korea. We have demonstrated that star-shaped polymers with a compatibilizing outer corona can be dispersed into a thermosetting organosilicate and used to create a dispersed porous material. These stimuli-responsive, copolymerize create nano-sized domains through a matrix-mediated collapse of the interior core of the star corona, polymer structure. Clearly, this approach relies on the outer corona of the star to control the insoluble core with the thermosetting resin and prevent aggregation such that these individual molecules template the crosslinking of the matrix and ultimately generate a single hole. The organic polymer was selectively thermolized to leave behind its latent image in the matrix with a pore size that reflected the size of the polymer molecule, and provided the expected reduction in dielectric constant as the smallest pores achieved by the star and dendrimer-like star macromolecular architectures is in excess of 10nm, which is too large for future device generations. To address this, we will describe the templating of organosilicates from new macromolecular architectures that result in the interface of small-molecule and polymeric amphiphiles. By developing new and well-defined synthetic pathways to produce environmentally responsive macromolecules, macroscopic, nano-structured thin films of technological interest were produced.

F3.4 Preparation and structure of Organic/Inorganic Hybrid Materials Based on Polyphenylsilsesiquoxane (PPSQOH). Seung Sang Hwang, Sungwon Ma, Hangsoek Lee and Cheol Chung; Polymer Hybrid Center, Korea Institute of Science & Technology (KIST), Seoul, South Korea. New hybrid materials which have low dielectric constants were prepared. Polyphenylsilsesiquoxane (PPSQOH) with hydroxyl end groups was synthesized by following the existing method. Hydroxyl-functionalized polyethylene (PSEOH) and hydroxyl-functionalized polyactic acid (PLOH) were also prepared by anionic and bulk polymerization. PSSQOH series at various composition ratios and molecular weights were obtained using reaction between PPSQOH at PSOH, PLOPSQH series at various composition ratios and molecular weights were obtained from reaction between PPSQOH and PLOH. These hybrid materials were characterized by 1H-NMR and FT-IR. The thermal decomposition behavior of hybrid materials was also investigated by thermogravimetry analysis (TGA). Their surface morphology was investigated by transmission electron microscope (TEM). The results from the TEM micrographs exhibit the existence of highly porous structures and the pores size ranged below 5 nm are regularly dispersed. These hybrid materials would be useful for various applications to better electric and optical device.

F3.5 Characterization and preparation of porous low dielectric films that use various molecular weight (M.W) and polydispersity (PD) of silsesquioxane (SSQ). Hee J.-hoon1, Kim Taewan2, Lee Kwang-Hoe2, Koo Ja ho1 and Jeong Hyun-Dam2; 1H.I.D Center, Samsung Corning Corp Ltd, suwon, South Korea; 2Electronic Materials Lab, Samsung Advanced Institute of Technology (SAIT), suwon, South Korea.

The industry has been strongly interested in integrating porous low dielectric constant materials to meet new technical demands of future LSI device. Porous low dielectric films are strong candidates among those, which were formed from new silsesquioxane (SSQ) polymer by the addition of a sacrificial material to the SSQ. The electrical property of these porous low dielectric films was significantly affected by molecular weight (M.W) and polydispersity (PD) of SSQ. In this study, we have characterized the network structure of the thin films and molecular weight (M.W) and polydispersity (PD) of SSQ by means of Gel permeation chromatography (GPC) and Particle counter and dynamic layer spectrometry (DLS) and Transmission Electron Microscopy (TEM), and residual hydroxyl group of thin films using FT-IR. In addition, we monitored the electrical properties and mechanical properties of the porous thin films in order to know the potential as a low-k material. We found that the mechanical properties of porous low-k thin film prepared with polydispersity (PD) of SSQ and molecular weight (M.W) was correlated to density of the thin film. Network structure and density in the thin film strongly depend on molecular weight (M.W) as well as polydispersity (PD) of SSQ. These results indicated that the lower molecular weight (M.W) and polydispersity (PD) of silsesquioxane (SSQ) on the thin film was increased slightly the mechanical properties of the thin film such as hardness and modulus.

F3.6 New hybrid low-k dielectric materials prepared by vinylsilane polymerization. Jung-Won Kang, Byung-Ro Kim, Gwi-Gwon Kang, Myung-Sun Moon, Bum-Gyu Choi and Min-Jin Ko, Corporate R&D, LG Chem Ltd., Daejeon, South Korea. Spin-on Low-k materials are potentially very attractive as interconnection materials in a wide range of semiconductor structures. A large variety of polymers have been proposed for use as low-k materials with low dielectric constants for applications in microelectronics. Inorganic polymers such as silsesquioxane are more like SiO2 than other polymeric dielectrics. They have perceived advantages for higher Tg, hardness and adhesion to polar surfaces. However, the main disadvantage for these inorganic polymers is that they are also brittle. This makes them susceptible to damage during CMP. Organic polymers, especially aromatic carbon with thermal stability, have higher toughness yielding crack free film. But they show somewhat high CTE and low mechanical strengths (hardness, adhesion). In this work, we have prepared new organic-inorganic hybrid low-k Dielectrics by vinylsilane polymerization. The dielectric constants of these materials were evaluated to be 2.3-3.1, which depend on these composition and additional fabrication. The hardness was 2.0 GPa after 430°C curing. These materials also show very high toughness and good adhesion properties. The fracture toughness of these thin film was 0.22 Mpa*m1/2 without adhesion promoters. This result indicates that these organic-inorganic hybrid materials are very promising polymers for low-k dielectrics that have low dielectric constants with high thermal and mechanical properties.

F3.7 Inter-pore interactions in highly porous ultra low-k films. Nobutaka Hata1,2, Peter Klurenk1, Nobutatsu Fujii1, Hirofumi Takada1, Che Negoro1, Kazuhiro Yamada3 and Takamasa Kikkawa4,5; 1MIRAI-ASRC, AIST, Tsukuba, Ibaraki, Japan; 2ASRC, Tsukuba, Ibaraki, Japan; 3MIRAI-ASRC, Tsukuba, Ibaraki, Japan; 4ICNS, Hiroshima University, Higashi-Hiroshima, Hiroshima, Japan.

Catastrophic deterioration of electrical, chemical and mechanical stabilities of porous low-k films, which occurs when the porosity exceeds a critical porosity Xc of about 35 %, is known as one of the biggest issues in development of ultra low-k materials. We hypothesized that the deterioration is caused by strong inter-pore interactions such as random coagulation of pores, perforation path formation, and formation of large voids. We took advantages of the three different pore characterization techniques of in-situ spectroscopic ellipsometry in a home-made quartz optical cell for heptane or toluene vapor sorption at room temperature, volumetric argon or nitrogen physisorption analyses at cryogenic temperature, and film X-ray analyses based on small angle X-ray scattering technique, to investigate pore structures in silica-based highly porous (above Xc) low-k films. The ultra low-k films were prepared by spin coating of precursor solutions of sacrificial surfactant templated sol-gel synthesis.
The results from X-ray scattering and total adsorbed amount evidenced successful control of pore size and porosity, respectively, by the selection of the molecular-template. The pore-size controllability was confirmed also by sorption isotherm analyses based on Brunauer-Emmett-Teller theory and Kelvin equation. Cooherence of X-ray was utilized to examine the existence of ordered structures. The in-situ ellipsometry spectra were analyzed with the optical model of low-k films on c-Si substrate to obtain vapor pressure dependencies of the film thicknesses and reflective indices, which were then used to calculate the adsorbed vapor amounts, or adsorption isosteres. The isosteres were analyzed to clarify the meta-stable adsorption states due to the existence of necks in adsorptive perforation paths. Also the slopes of sorption isosteres at high partial pressure region and of X-ray scattering curves in low scattering angle region was analyzed to reveal large voids. From these results it has been demonstrated that not only high porosity periodic porous silica films but also disordered porous silica films can be made free from random pore coagulations, long random perforation paths, and large voids. It has been shown that careful control through preparation conditions of pore structures in highly porous low-k films is a key for realizing highly stable ultra low-k films for future low-k/Cu interconnects.

### F3.8 The preparation of mechanically strong order mesoporous silica ultra-low-k film using low temperature and fast ozone ashing dry technology.

A. T. Cho and F. M. Pan; National Nano Device Laboratories, Hsinchu, Taiwan.

Ozone ashing dry technology has been applied in the formation of a mesoporous silica ultra-low-k film with an ordered pore structure, uniform pore size distribution, well electrical reliability of k 2.0 and better mechanical properties than other nano-porous films. The growing N2 flux results in an N enriched film, with a maximum N atomic concentration of 57%. Film density is obtained by combining atomic concentration of 57%. Film density is obtained by combining RBS results with the measured films thickness. Preliminary results reveal that 22 nm thick W-C-N successfully prevents the Cu diffusion after the annealing at 700°C for 30 min. Finally, NH3 gas was also introduced for 0.2 s and purged with N2 gas. During a cycle of ALD process, pulse plasma was applied for the exposure of the starts. The pulse plasma powers were 100 W, 8 kV of peak-to-peak voltage. The substrate temperature was 300 to 400°C. The W-C-N film was deposited with the rate of 2.0 Å/cycle at 350°C. Stoichiometric ratio of W-C-N film was determined by Rutherford backscattering (RBS) and Auger electron spectroscopy (AES). During the PPALD processes, the N and C concentration is uniformly distributed in the W-C-N film. The growth rate and the stoichiometry were not changed with each cycle time. The interface between W-C-N film and Si was observed by high resolution transmission electron microscopy (HR-TEM). In order to investigate the performance of PPALD grown W-C-N thin films (thickness is 22 nm) as a diffusion barrier against Cu diffusion, 200 nm thick Cu film was deposited on the W-C-N/TEOS/Si structure. Cu/W-C-N/TEOS/Si structures were annealed at 500 700°C for 30 min in N2 ambient. After the annealing processes, the samples were characterized with RBS, HRTEM and chemical vapor deposition (CVD). The results showed that the ozone treatment leads to a reduced process time and process temperature.

### F3.10 Structural and functional characterization of W-Si-N sputtered thin films for copper metallizations.

Alberto Vomiero,1,2 Stefano Frabboni,3 Enrico Boscolo Marchi4, Gino Marrotta, Giampiero Ottaviani, Stefano Poizzi1 and Alvise Benedetti1; 1Dept. of Physics, University of Padova, Padova, Italy; 2TNFX Laboratory, Nazionali di Legnaro, Legnaro (PD), Italy; 3Dept. of Physics, University of Modena, Modena, Italy; 4Dept. of Chemical Physics, University of Venice, Venice, Italy; 5Dept. of Materials Engineering and Industrial Technologies, University of Trento, Trento, Italy.

In the framework of the development of new materials to be applied as ultrathin diffusion barriers for Cu interconnected structures in microelectronics, ternary W-Si-N thin layers (~200 nm thick) are produced by RF magnetron sputtering, starting from a W5Si3 target. The aim of this work is to add information about a ternary system, which has been studied with respect to other ternary systems as Ta-Si-N. Nitrogen incorporation is obtained by inserting N2 gas in the inert Ar plasma atmosphere, giving rise to a reactive sputtering process. The structural and chemical properties of the layers are characterized before and after annealing, in order to investigate the effects of heating on the stability of the deposited films. Heat treatments are performed in vacuum in the range 600 - 1000°C. The stoichiometric composition is measured by the means of Rutherford Backscattering (RBS) and Elastic Recoil Detection Analysis (ERDA). The growing N2 flux results in an N enriched film, with a maximum N atomic concentration of 57%. Film density is obtained by combining RBS results with the measured film thickness. Preliminary results reveal that 22 nm thick W-C-N successfully prevents the Cu diffusion after the annealing at 700°C for 30 min. Finally, NH3 gas was also introduced for 0.2 s and purged with N2 gas. During a cycle of ALD process, pulse plasma was applied for the exposure of the starts. The pulse plasma powers were 100 W, 8 kV of peak-to-peak voltage. The substrate temperature was 300 to 400°C. The W-C-N film was deposited with the rate of 2.0 Å/cycle at 350°C. Stoichiometric ratio of W-C-N film was determined by Rutherford backscattering (RBS) and Auger electron spectroscopy (AES). During the PPALD processes, the N and C concentration is uniformly distributed in the W-C-N film. The growth rate and the stoichiometry were not changed with each cycle time. The interface between W-C-N film and Si was observed by high resolution transmission electron microscopy (HR-TEM). In order to investigate the performance of PPALD grown W-C-N thin films (thickness is 22 nm) as a diffusion barrier against Cu diffusion, 200 nm thick Cu film was deposited on the W-C-N/TEOS/Si structure. Cu/W-C-N/TEOS/Si structures were annealed at 500 700°C for 30 min in N2 ambient. After the annealing processes, the samples were characterized with RBS, HRTEM and chemical vapor deposition (CVD). The results showed that the ozone treatment leads to a reduced process time and process temperature.

### F3.11 Diffusion Barrier Properties of Nano-crystalline ZrCN films in Cu/Si Systems.

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ZrN has a lower negative formation energy and a lower resistivity than TaN. Therefore, ZrN system could be a good candidate for the diffusion barrier in IC technology. In this paper, the proposed novel
zirconium carbon nitrides (ZrCN) layers were deposited by reactive sputtering ZrC target (50-50 wt% at 99.5% purity) in a mixture of Ar and N2 ambient. The physical and electrical properties of ZrC-N films were examined with respect to the N2 content. The barrier properties of ZrC-N films were evaluated and compared to the cases of Zr-C and Zr-N films. For thermal stability analysis, the prepared samples were subsequently subjected to thermal treatment at temperatures in the range of 300-900 °C in a vacuum tube with the base pressure of 3x10^-5torr. Possible chemical reactions and Cu diffusion inside the annealed Cu/barrier/ Si contact systems due to thermal annealing were examined by employing four-point probe sheet resistance measurement, scanning electron microscopy (SEM) for surface morphology investigation, X-ray diffraction (XRD) technique for phases of possible reaction products identification, and the interdiffusion of each species upon annealing is studied by Auger electron spectroscopy (AES). Finally, the possible mechanism governing for the failure of the present barrier after high temperature annealing was discussed.


Two particularly important reliability issues facing the integration of low-k dielectric films are the fracture energy of the barrier-dielectric interface and the barrier layer integrity during processing. The effect of dielectric porosity and pore size distribution on the physical properties of the barrier and copper barrier layers has not been studied.

We have noticed that the compressive stresses in the barrier layers lead to spontaneous delamination and formation of telephone-cord like morphologies. These morphologies allow the measurement of fracture energy and understanding of the fracture energy for self-terminating features to yield realistic debonding parameters. The fracture energy of two barrier films, TaN and Ta, was determined using this method for varying porosity nanoporous silica. Detailed surface area characterization was done for the substrates using two complementary techniques of AFM (Atomic Force Microscope) and EP (Ellipsometric Porosimetry). The dielectric properties i.e. pore size and chemistry, were varied and their effect on fracture energy was determined. Strong correlation was found in the dielectric chemistry, available surface area, porosity and the fracture energy. The mechanisms of such a correlation will also be discussed.


A previously developed metal-organic atomic layer deposition (ALD) tantalum nitride (TaN x) process was employed to investigate the growth of TaN x liners on low dielectric constant (low-k) materials for liner applications in advanced Cu/low-k interconnect metallization schemes. ALD of TaN x was performed at a substrate temperature of 250°C using TBTDET as precursor and a hydrogen plasma as the reducing agent at a base pressure of 3x10^-5 torr. The dependence of TaN x film thickness on the number of ALD cycles performed on both organosilicidate and organic polymer-based low-k materials was determined and compared to baseline growth characteristics of ALD TaN x on SiO2.

In order to address the effect of the deposition of TaN x on surface roughness, atomic force microscopy (AFM) measurements were carried out prior to and after the deposition of TaN x on the low-k materials. The stability of the interface between TaN x and the low-k materials after an applied thermal budget was studied by examining interfacial roughness profiles using cross-sectional imaging in a high-resolution transmission electron microscope (HREM). The wetting and adhesion properties of Cu/low-k were quantified using a solid-state wetting experimental methodology after integration of ALD TaN x liners with Cu and low-k dielectrics.


Atomic layer deposition (ALD) has been regarded as a highly promising thin film deposition technique for growing copper diffusion barrier/seed layers [1] particularly in 45 nm technology node and below [2]. Due to its excellent step coverage and precise control of ultrathin barrier layer thickness. In this work, a low temperature ALD process has been developed for the growth of ultra thin TaN x films with the use of TaCl5 as Ta-containing precursor and NH3 as co-reactant gas in a 200-mm wafer platform. An optimized process was identified by performing a systematic study of the film growth rate as a function of TaCl5 pulse time, NH3 pulse time, and Ar purge time. The properties of the TaN x films deposited via the optimized process conditions were studied using Rutherford backscattering spectrometry (RBS), scanning electron microscopy (SEM) and cross-sectional electron microscopy (SEM), X-ray diffraction (XRD), atomic force microscopy (AFM), Auger electron spectroscopy (AES), and nuclear reaction analysis (NRA). It was found that the as-deposited TaN x films had a Ta/N ratio of 0.78, excellent step coverage, an orthorhombic microstructure, and low oxygen, hydrogen and chlorine contamination levels.

The preliminary copper diffusion barrier performance as investigated by RBS shows that a 2 nm-thick TaN x films could prevent copper from diffusing into low-k dielectrics.


Tantalum carbon nitride, Ta(CN) x, films are of potential interest in copper barrier and front-end electrode applications owing to their low resistivity, robust diffusion barrier properties, and excellent thermal stability. Key aspects of such materials are the initial growth and nucleation characteristics, as these will play a significant role in their ultimate performance. To study this, Ta(CN) x films were deposited by a plasma-enhanced atomic layer deposition (PEALD) process employing tertbutylidinitrilo-tris(dihydromido) tantalum (TBTDET) as precursor and a nitrogen plasma as the reducing agent at a substrate temperature of 250°C. The deposited films demonstrate promising diffusion barrier properties for copper metallization at thicknesses as small as 1nm. Initial growth was investigated by varying the number of deposition cycles, yielding films ranging from 0.4nm to 10nm thick.

The resultant films were analyzed by atomic force microscopy, Rutherford backscattering spectrometry, and transmission electron microscopy. Nanostructural characteristics are discussed, and a mechanism is proposed for the observed diffusion barrier behavior.

F3.16 Effect of Annealing on The Structural, Mechanical and Tribological Properties of Electroplated Cu Thin Films. Pallavi Shukla,1,2 Parshuram Balkrishna Zantye,1,2 Arun Sridhar,1 Ashok Kumar,1,2 and Mahesh Sangarela; 1Department of Mechanical Engineering, University of South Florida, Tampa, Florida; 2Nanomaterials and Nanomanufacturing Research Center, University of South Florida, Tampa, Florida.

The increasing demand for faster and more reliable integrated circuits (ICs) has promoted the integration of Copper-based metallization. Electroplated Cu films demonstrate a microstructural transition at room temperature, known as self annealing. In this paper we intend to investigate the annealing behavior of electroplated Cu films grown on a Cu seed layer on top of the barrier layers over a single crystal silicon substrate. All the samples were undergone through a multistep annealing process. Grazing incident X-ray diffraction pattern shows stronger reflection on Cu (111) and (220) planes and weaker reflections from (200), (311) and (222) planes in all the electroplated Cu samples. Transmission electron microscopy was performed on the cross section of the samples and the diffraction pattern showed the crystalline behavior of both seed layer and electroplated Cu.

Nanindentation was performed on all the samples using the continuous stiffness measurement (CSM) technique and it was found that the elastic modulus varies from 110 to 130 GPa while the hardness varies from 1 to 1.6 GPa depending on the annealing conditions. The tribological properties of all the copper films were also measured using the Bench Top CMP tester. Subsequently, Nanindentation was performed on the samples after polishing the top surface in order to investigate the work hardening and an increase in hardness and modulus was observed. The surface morphology and roughness of Cu films before and after polishing were characterized using Atomic Force Microscopy. Finite Element Modeling is to be performed in order to investigate the stress behavior during nanindentation.

F3.17 Copper Metallization in High Aspect Ratio Trenches Using Filtered Vacuum Arc Deposition. Yong Ju Lee and Othon Monteiro; Lawrence Berkeley National Laboratory, Berkeley, California.

With decreasing feature size and increasing complexity of the metal
wiring in microelectronics, the signal delay introduced due to the increasing resistance of the longer metal lines became critical. It exceeded the threshold for inductance for interconnects. Copper (Cu) is posed to take over as the main on-chip conductor for all types of integrated circuits to decrease the resistance compared with aluminum and tungsten. We introduce the filtered cathodic vacuum arc (FCVA) technique for the deposition of Cu capable of filling trenches with lateral dimensions of 150 nm and high aspect ratios. The method uses a filtered cathodic arc plasma source with tight ion energy control. With the FCVA technique, the plasma stream is steered by a magnetic filter to eliminate neutral particles generated at the cathode. By applying a variable bias to the substrate, the energy of ions impinging the substrate can be controlled in the range from tens to hundreds of electron volts. 100-nm-wide trenches with aspect ratio of 200:1 were effectively filled by Cu ions. The thickness of the copper film on the horizontal surface of the wafer is significantly smaller than the depth of the trenches, suggesting that filling is accomplished at least in part with material sputtered from or reflected by the film on the trench walls.

**F3.18**

**Thermal Conductivity of Carbon Nanotube Composite Films.**
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Carbon nanotubes (CNT) possess exceptional thermal properties such as high heat-carrying capacity. Developing new materials that can disperse heat has long been a challenge in space exploration. Exploiting CNT films for their superior thermal conductance properties has the potential for such applications that require efficient heat transfer. Another potential application includes using CNT films as heat sinks in single-chip large-scale integrated (LSI) or microelectronic circuits, where power density is a critical reliability metric. State-of-the-art integrated circuits (IC) for microprocessors routinely dissipate power densities on the order of 50 W/cm². This large power is due to the localized heating of ICs operating at high frequencies, and must be properly controlled for future high-frequency microelectronic applications. In this work, we present fundamental thermal conductivity measurements of CNT composite films. CNTs grown using the plasma-enhanced chemical vapor deposition (PECVD) process [1] have been optimized for dense vertical arrays of nanotubes. These asgrown nanotubes can be estimated as having 10–20 percent packing density, providing relatively small surface area for thermal conduction through the nanotubes. Clearly, the remaining 80–90 percent of the sample is essentially filled with air, a poor thermal conductor (k=2.5×10⁻⁴ W/cm·K). By filling these gaps with a material exhibiting more efficient heat-carrying properties, we can maximize thermal conductivity of the CNT composite film. To characterize the conduction capability of these materials, we used the methodology applied to diamond-like carbon films by Goodson, et al. [2]. In this approach, a thin platinum microwire is deposited on the sample and used as a localized Joule heating device, with temperature and heat conduction determined from voltage pulses. A Wheatstone bridge circuit is employed to measure resistance changes in the microwire, through which transient temperature response is calculated and thermal conductivity is inferred. Additional calculations are performed to account for lateral heat conduction through the film. A variety of CNT composite films with different gap-fill materials have been investigated for efficient heat transfer. The characterization results will be presented comparing the merits and drawbacks of all test structures. [1] B.A. Cruden, A.M. Cassell, Q. Ye, and M. Meyyappan, J. Appl. Phys., 94, 4070 (2003). [2] K.E. Goodson, O.W. Kading, M. Rosler, and R. Zachal, J. Appl. Phys., 77, 1385 (1995).

**F3.19**

**Silver Patterning by Ecr-Ribe for Advanced Interconnects.**

As devices continuously shrink in ultra-large-scale integration (ULSI), the RC delay of the interconnection system becomes one of the most critical limitations on IC performance. Silver, with a lower bulk resistivity than that of copper and also a potentially lower surface scattering property, is being considered by many as the next metalization candidate. Silver has also received attentions in features sizes below 100 nm. To evaluate the potential application of silver metalization in industry, one of the important aspects is the pattern transfer by etch processing. Dry etching of silver for the metalization in microelectronics is investigated. Etching is performed using an electron-cyclotron-resonance reactive-ion-beam-etching system (ECR-RIE) in an Ar/C4F2 or Ar/C4F4/O2 mixture. The etch characteristics are strongly dependent on the beam frequency (MHz) and microwave energy. By changing the beam voltage from 250 V to 600 V, there is an increase in etch rate from 3.3 nm/min to 112 nm/min. The O2 concentration in the reactive mixture has only a small effect on the etching speed. However, the root-mean-square (RMS) roughness at 500 V beam voltage with only C4F4 reactive gas is less than that of 500 V beam voltage with reactive gas C4F4 and O2 (9:1), and also the surface after etching is clearer after etching without oxygen gas. An anisotropic, reactive-ion-beam-etched surface is obtained. Focused ion beam (FIB) and atomic force microscopy (AFM) have been used to study the etched profile and the roughness, respectively.

**F3.20**

**Free-standing line patterns of nanocrystalline electrodeposition.**
Karen Pandion1, Marcel A.J. Sonneveld1, Henrik M. Hansen2, Andy Hendriksen1, iHPL - Dept. of Manufacturing Engineering and Management, Technical University of Denmark, Lyngby, Denmark; 2MEK - Dept. of Mechanical Engineering, Technical University of Denmark, Lyngby, Denmark.

Electrochemical deposition has become the key technology in manufacturing functional thin films with finite structures, e.g. for microsystems and microcomponents. The two most popular materials in that field are copper, which has become the dominant material for interconnects in integrated circuits in microelectronics, and nickel, a promising material to realize movable structures for micro-electro-mechanical systems (MEMS). Finite metal structures with very small dimensions or extremely high aspect ratio range are either inlaid in trenches of an insulator (like Cu-damascene lines) or they form free-standing patterns on a substrate (like so-called LIGA-structures). The functionality and reliability of such fine structures depend on their microstructure - however, the thermodynamically non-equilibrium state of as-deposited films may cause substantial changes of the microstructure and related properties with time at room temperature and/or elevated (operating) temperatures. Free-standing discontinuous Cu- and Ni-line patterns were manufactured by combining photo-lithography and electrochemical deposition. Several pattern geometries varying in line width and interline distance in the range of a few micrometers were deposited onto two different substrates (sub-micron trenches etched in silicon) with a typical ratio range from 5 to 9 nm and the four point probe measuring the resistivity of the deposits by means of light optical and electron microscopy. For Cu-line patterns, finite element modeling (FEM) of strain distributions within individual free-standing lines was carried out. FEM-results were used to simulate X-ray diffraction peak profiles, which were compared to experimental results.

**F3.21**

**Pulsed CVD of Cu seed layer using a (hfac)Cu(3-dimethyl-1-butene) source plus H2 reactant.**
Jae-Bum Park and JaeGab Lee; A School Of Advanced Materials Engineering, Kookmin University, Seoul, South Korea.

For electroplating Cu, thin seed layer of Cu has been successfully deposited over 0.1 μm wide trenches with a high aspect of 22 by pulsed CVD of Cu using a organometallic Cu(I) source, DMB and H2 reactant gas. Prior to pulsed CVD of Cu, about 20 μm of TiN was deposited using TDMAT at 300°C over the deep submicron trenches, which acted as a glue adhesion layer for Cu metallization. After deposition of MOCVD TiN, the resultant trench profiles showed 50 nm wide trench with aspect ratio over 40:1. The growth proceeds by exposing the MOCVD TiN coated trenches alternately to the Cu precursors and the following Ar pulse, and H2 pulse. The typical deposition cycle consisted of 3 sec DMB pulse, 6 sec Ar pulse, and 3 sec H2 pulse at the substrate temperature of 500 °C and pressure of 0.4 torr. Compared with ADL Cu using a organometallic Cu(II) source, pulsed CVD using a Cu(I) precursor can provide a significantly lower deposition temperature for nucleation and growth, and leads to a much higher surface morphology. AFM analysis reveals the root mean square of the surface roughness ranging from 5 to 9 nm and the four point probe measuring the resistivity of 4.2 to 1.8 Ω·cm, depending on the thickness of Cu. In addition, the growth rate of pulsed Cu shows a weak function of substrate temperature. The addition of H2 pulse step remarkably reduces the
growth rate of Cu and carbon contamination as well. Further, the added H2 pulse decreases a sticking probability, and thus leading to excellent conformality of Cu in trenches with aspect ratio over 40:1. These films can be suitable as a seed layer for the electroplating of Cu in an advanced device.

F3.22
Effects of ion irradiation on anisotropic plasma chemical vapor deposition of Cu. Kouyo Takegaki, Manabu Takahita, Kazunori Koga, Masaharu Shiratori and Yukio Watanabe; Dept. of Electronics, Kyushu University, Fukuoka, Japan.

We have proposed an anisotropic plasma chemical vapor deposition method by which Cu is filled preferentially from bottom of a trench with sidewall deposition. 1-2 We have studied the deposition and sputtering rates on the top and bottom surfaces decrease to tend with increasing R and eventually they become zero for R > 85%, whereas no deposition on the sidewall takes place for R > 11%. On the other hand, the sputtering rates on the top and bottom surfaces decrease slightly with increasing R, whereas no sputtering on the sidewall takes place. These results indicate that the ion irradiation is the key to the anisotropic deposition and is not appreciable on the sidewall. We have identified ion species irradiating on the substrate surface with a quadrupole mass-spectrometer. The dominant light and heavy ionic species in the discharge are H3+ and ArH+. Signal intensities of H+ and Ar+ in one order of magnitude with increasing R from 11 to 83%, whereas those of Ar+ and ArH+ are nearly constant in the same range. Roles of these ions on the anisotropic deposition will be discussed in the presentation. 1 H. Takegaki, et al., Mater. Sci. Semicond. Processing, 5, 301 (2003). 2 H. Takegaki, et al., Mater. Res. Soc. Symp. Proc. 766, E3.8.1 (2003).

F3.23
Preparation and Characterization of Copper Film on Plastic Substrate by ECR-MOCVD Coupled With a DC Bias. Joong Ke Lee, Bupju Jeon and Byung Won Cho; Eco-Nano Research Center, Korea Institute of Science and Technology, Seoul, South Korea.

Metalized polymers are very interesting materials for microelectronic packaging of flexible PCB and COF (chip on film), flexible solar cell, gas barrier and EMI (electromagnetic interference) shielding purpose. However, a lot of plastic can be easily corroded with a thin metal layer without pretreatment due to lack of nucleation sites. Conventional methods for metalization of polymer are electrochemical plating and physical vapor deposition (PVD) such as thermal evaporation and magnetron sputtering. Wet chemistry processes, however, have some inherent problems such as complex procedures and environmental pollution. For the PVD, it is technically difficult to maintain metal film on the polymer substrate due to poor adhesion, substrate deformation and an aging effect. CVD processes for the preparation of copper film are of considerable interest since continuous deposition of large areas can be easily achieved without metal mask. However, most conventional metal organic chemical vapor deposition techniques for the preparation of copper film are based on thermal CVD procedures. Operating temperatures in the range of 150 to 200°C have been used to prepare copper films with CVD. Therefore, the deposition of thin copper film on polymer substrates by the MOCVD method at room temperature has not been tried. Recently, there has been great interest in using MOCVD at ambient temperature in order to produce metalized polymer. Chemical vapor deposition at ambient temperature using organometallic precursors should be possible with the aid of a DC bias. The aim of this work was to test the ECR-MOCVD method for deposition at room temperature and characterize the copper film prepared thereby. We also report the results of experiments designed to investigate the deposition of copper and carbon containing hybrid thin films from Cu(hfac)2 as a copper precursor in an Ar-H2 atmosphere by using ECR microwave plasma coupled with a DC bias. The structural and chemical analyses of the Cu/C films were carried out and their electrical resistances were determined as a function of H2/Ar mole ratio, microwave power, periodic negative voltage and the magnet current.

F3.24
Thermal stability and electrical properties of Ag(AI) metallization. H. C. Kim1, N. D. Theodore2, J. W. Mayer1 and T. L. Alford1; 1Chemical and Materials Engineering, Arizona State University, Tempe, Arizona; 2Digital DNA Labs, Motorola Inc., Tempe, Arizona.

The thermal stability and electrical resistivity of Ag(AI) alloy thin films on SiO2 are investigated and compared to pure Ag thin films by performing various analyses: Rutherford backscattering spectrometry, X-ray diffractionmetry, optical microscopy, and four-point probe measurements. The sputtering rate on the top and bottom surfaces decreases to tend with increasing R and eventually they become zero for R > 85%, whereas no deposition on the sidewall takes place for R > 11%. On the other hand, the sputtering rates on the top and bottom surfaces decrease slightly with increasing R, whereas no sputtering on the sidewall takes place. These results indicate that the ion irradiation is the key to the anisotropic deposition and is not appreciable on the sidewall. We have identified ion species irradiating on the substrate surface with a quadrupole mass-spectrometer. The dominant light and heavy ionic species in the discharge are H3+ and ArH+. Signal intensities of H+ and Ar+ in one order of magnitude with increasing R from 11 to 83%, whereas those of Ar+ and ArH+ are nearly constant in the same range. Roles of these ions on the anisotropic deposition will be discussed in the presentation. 1 H. Takegaki, et al., Mater. Sci. Semicond. Processing, 5, 301 (2003). 2 H. Takegaki, et al., Mater. Res. Soc. Symp. Proc. 766, E3.8.1 (2003).

F3.25

TiAl based thin-films possess high oxidation-resistance and high melting points, making them possible candidates for application in high-temperature electronics. The behavior of the films upon exposure to various temperatures is of interest for such application. In the present study, Ti37Al63 thin films were deposited onto SiO2 substrates using RF magnetron sputtering from a compound target. Anneals were performed in vacuum at temperatures ranging from 400°C to 700°C. The phases and microstructural behavior of the films were evaluated as a function of annealing. Morphostructural behavior was correlated with resistivity changes in the films. The results are relevant for potential application of the films to electronics.
thin films (MTFs) to be cast that are commensurate with the requirements of the processing technology. Strict control of the MTFs and their precursors is required. i.e. the films must be stabilized and have the required properties in terms of dimension, adhesion, and mechanical performance. The films also have to be sufficiently chemically robust to survive secondary processing environments. The films produced here were derived from silane sols hydrolyzing from TEOS in a low-power plasma. Mm from silica sol. These films are shown to be promising candidates of films almost single crystal in nature. In all cases studied here, the properties of the MTFs such as adhesion, mechanical performance and chemical robustness could be greatly improved by the addition of aluminium into the two-dimensional framework of the pores. The beneficial effects of aluminium addition can be seen in figure 2 where the hardness of films is plotted against aluminium content. Data is presented showing how aluminium incorporation improves chemical robustness. The value of K decreases with addition. Strict control of process conditions are required to prevent contamination of the film and resultant high K values. At low aluminium loadings the K value is largely unaffected compared to native silica films. The possibility of use of MTFs in IBD applications is discussed in light of these results. References 1. C T Kresge, M E Leonowicz, J C Roth, J C Vartulli, J S Beck, Nature; 359(1992)710.

9:00 AM F4.2 Theoretical Investigation of the Dielectric Constant and the Elastic Modulus of Porous Materials for Designing Pore Structures of Ultra Low-k Films with High Mechanical Strength. Hidenori Miyoshi 1, Hisanori Matsuo 1, Hirofumi Tanaka 1, Kazuo Kohmura 1, Nobutoshi Fujii 1, Yoshiaki Oku 1, Syozo Takada 1, Nobuhiro Hata 1 and Takamori Kawakita 1; 1RIKEN-AIST, Tsukuba, Ibaraki, Japan. 2ASRC-AIST, Tsukuba, Ibaraki, Japan; 3RIKEN-ASRC-AIST, Tsukuba, Ibaraki, Japan; 4RCNS, Hiroshima Univ., Higashi-Hiroshima, Hiroshima, Japan. The desirable structures and arrangements of pores in the dielectrics for the development of ultra low-k porous films with high mechanical strength are described. We have calculated the dielectric constant of k and the elastic modulus of E of porous films in the film thickness direction by finite element method (FEM) that assuming that properties of the wall materials are constant. We have previously shown that the elastic modulus decreases with increasing K values. We calculated the shrinkage of pores in the film thickness direction will hinder the simultaneous achievement of ultra low dielectric constant and high elastic modulus. Two-dimensional periodic porous films have anisotropic properties. The simulation between E/k and the two-dimensional periodic porous films. The simulation three-dimensional cubic porous films have isotropy in k. If the porous films have the form of the single crystal of the cubic lattice, values of E depend on the crystal orientations. When the porous films consist of polycrystalline domains where each domain has the periodic cubic pore structure, the films have isotropy in E. Periodic porous silica films and disordered porous silica films can be synthesized by use of a self-assembling technology of surfactant and an acidic silica derived from silane precursors. These films are shown to be promising candidates of ultra low-k films with high mechanical strength.
There are increasing needs for low-k solutions in integrated circuits that can be extended to future generations. Two different pathways are explored to lower the dielectric constant of these materials relative to silicon dioxide (k 4). By incorporating atoms and bonds that have a lower polarizability, such as alkyl groups, or by lowering the density of the material, either sterically or through the introduction of air, the dielectric constant is reduced. Creating porous films using an organosilicate glass (OSG) matrix is an avenue for introducing void space and thereby lowering the dielectric constant. Since the introduction of porosity severely diminishes the mechanical integrity of the material, understanding the relationship between film structure and mechanical properties becomes extremely important. The main dichotomy of methods for producing low-k materials is between chemical vapor deposition (CVD) and spin-on dielectrics (SOD). At this time, the focus is on using an OSG matrix/porogen approach. Due to increasing awareness and concern for environmental, safety and health (ESH) issues, CVD has the advantage of being a solventless process and therefore is favorable when compared to SOD. In addition, a CVD process for the creation of porous materials would lead to easier integration with existing toolsets. Depositing matrix and porogen precursors simultaneously using CVD creates many obstacles as the deposition requirements of the two species are significantly different. A novel approach to alleviate this problem is to use pre-formed porogens, such as polystyrene micro-spheres, to form a cycloalumin. This allows the use of the deposition conditions that give the optimal material structure, with disregard to the effect on the porogen deposition. An ultrasonic atomizer can be used to introduce these pre-formed porogens into the reactor for deposition. Another advantage gained from this technique is that the pore size is controlled and determined by size of the porogen. Cycloalumin is a prime porogen candidate due to its low decomposition temperature and high molecular size. The porogen matrix was deposited using pulsed plasma-enhanced CVD from octamethylcyclotetrasiloxane (D4). In addition, hydrogen peroxide (H2O2) was used as an oxidant to promote Si-OH end groups throughout the film. Upon annealing the films at 40°C, condensation reactions occur between proximal Si-OH groups, liberating water and generating Si-O-Si network bonds to strengthen the film. A study of the film structure before and after annealing through FTIR analysis confirms increased crosslinking upon annealing and provides a key step to understanding the link between film structure and mechanical properties. For a deposition with a precursor flowrate ratio of H2O2 to D4 of 25:1 and an equivalent power of 30 W, a two-fold increase in hardness was observed upon annealing (0.201 to 0.417 GPa).

11:15 AM F4.6
Sacrificial Porogens for the Production of Low-k Organosilicates: Nucleation and Growth vs. Templating, Robert D. Miller1, Victor Lee 1, Eric Connor 1, James L Hedrick 1, Craig J Hessler 2, Teddie Magbitang 1, Hea-Chool Kim 1 and Willi Volksen 1; 1K1F7, IBM Almaden Research Center, San Jose, California; 2Symyx Technologies, Santa Clara, California.

The drive toward smaller device features and increasing functional densities is fueling the push for new low-k materials. Dielectric targets with $k < 2.2$ will require porous materials. We have studied for some time the generation of porosity in organosilicates using sacrificial macromolecular porogens. These porogens can function by either a nucleation and growth mechanism or by templating. The latter process ultimately produces pores which reflect the size and shape of the porogen molecule in the thermosetting matrix. Recently, we have found that existing particle crosslinking is not necessary to achieve templating behavior in organosilicate matrices. Unimolecular, polymeric amphiphiles containing a nonpolar core and a compatibilizing corona show nanoparticle-like behavior in many organosilicate matrices. Star-shaped amphiphile block copolymers show micelle-like behavior without the need for dynamic self assembly. Materials of this type can be prepared by various tandem polymerization techniques such as controlled radical-radical and anionic-radical processes. These use of these techniques for the dielectric preparation of nanoporous thin film organosilicates will be discussed.

11:30 AM F4.9
Atomizer Delivery of Porogen for Creating Porous Low-k Dielectrics by Chemical Vapor Deposition, April Denise Ross and Karen K Gleason; Chemical Engineering, Massachusetts Institute of Technology, Cambridge, Massachusetts.

There are increasing needs for low-k solutions in integrated circuits that can be extended to future generations. Two different pathways are explored to lower the dielectric constant of these materials relative to silicon dioxide (k 4). By incorporating atoms and bonds that have a lower polarizability, such as alkyl groups, or by lowering the density of the material, either sterically or through the introduction of air, the dielectric constant is reduced. Creating porous films using an organosilicate glass (OSG) matrix is an avenue for introducing void space and thereby lowering the dielectric constant. Since the introduction of porosity severely diminishes the mechanical integrity of the material, understanding the relationship between film structure and mechanical properties becomes extremely important. The main dichotomy of methods for producing low-k materials is between chemical vapor deposition (CVD) and spin-on dielectrics (SOD). At this time, the focus is on using an OSG matrix/porogen approach. Due to increasing awareness and concern for environmental, safety and health (ESH) issues, CVD has the advantage of being a solventless process and therefore is favorable when compared to SOD. In addition, a CVD process for the creation of porous materials would lead to easier integration with existing toolsets. Depositing matrix and porogen precursors simultaneously using CVD creates many obstacles as the deposition requirements of the two species are significantly different. A novel approach to alleviate this problem is to use pre-formed porogens, such as polystyrene micro-spheres, to form a cycloalumin. This allows the use of the deposition conditions that give the optimal material structure, with disregard to the effect on the porogen deposition. An ultrasonic atomizer can be used to introduce these pre-formed porogens into the reactor for deposition. Another advantage gained from this technique is that the pore size is controlled and determined by size of the porogen. Cycloalumin is a prime porogen candidate due to its low decomposition temperature and high molecular size. The porogen matrix was deposited using pulsed plasma-enhanced CVD from octamethylcyclotetrasiloxane (D4). In addition, hydrogen peroxide (H2O2) was used as an oxidant to promote Si-OH end groups throughout the film. Upon annealing the films at 40°C, condensation reactions occur between proximal Si-OH groups, liberating water and generating Si-O-Si network bonds to strengthen the film. A study of the film structure before and after annealing through FTIR analysis confirms increased crosslinking upon annealing and provides a key step to understanding the link between film structure and mechanical properties. For a deposition with a precursor flowrate ratio of H2O2 to D4 of 25:1 and an equivalent power of 30 W, a two-fold increase in hardness was observed upon annealing (0.201 to 0.417 GPa).
3:10 PM  **F5.1**

**Pore Characterization of Mesoporous Dielectric Thin Films Using Positron Annihilation Spectroscopy (PAS).**

Kelvin G. Lynn1,2, Marc Weber1,2 and Cai-Lin Wang1,2,3, Center for Materials Research, Washington State Univ., Pullman, Washington; 2Physics Department, Washington State University, Pullman, Washington.

Beam-based Positron Annihilation Spectroscopy (PAS) is a recent addition to the family of characterizing low-dielectric constant (low-k) films. Using the annihilation signatures of positronium (Ps: H-like positron-electron atom), PAS provides information on total porosity, pore size, pore size distribution and void interconnectivity (percolation) as a function of film depth. In this presentation examples of the utility of various PAS techniques to characterize porous MSSQ films as a function of porogen load will be presented. The PAS results are subsequently compared to more traditional characterization techniques including CV, AC-conductivity, FE-SEM, FTIR, TGA, ellipsometry, and hardness measurements. Various beam PAS techniques (PALS, 3-Ps annihilation, Doppler Broadening) were used in this work to obtain global pictures of the materials. We report results from measurements of various types of mesoporous films, in which the porosity has been varied. The following aspects of this work will be highlighted in this paper: (1) Positron Lifetime Spectroscopy (PALS) lifetime distributions, pore size distributions and pore interconnectivity are deduced. (2) 3Ps self-annihilation measurements, from which void interconnectivity and the fraction of open cell and closed cell porosity. (3) Ps momentum sensitive Doppler Broadening techniques from which pore distributions are deduced. (4) Various porogen depth-profiles from which non-uniform pore distributions, open and closed cell porosity can be determined. Examples, on how information of open versus closed porosity, the total porosity, the pore sizes and a mean average size of interconnected pores will be briefly discussed. This work shows that PAS offers a number of unique techniques for the characterization of thin film porosity and compared to other measurements. The authors wish to thank collaborations with Ken Rodbell, M. Petkov, C. Fisher on various stages of this work.

2:00 PM  **F5.2**

**3-dimensional evaluation of nm-pores in porous low-k films using TEM stereoscopic / electron tomography observation method.**

Junichi Shimanski1, Shinsachi Ogawa2, Myoko Shimasu2 and Yasuhide Inoue2, 1Nano Analysis Section Research Department, NISSAN ARC LTD., Yokosuka, Japan; 2Semiconductor Leading Edge Technologies, Inc., Tsukuba, Japan.

Porous low-k films are expected to be one of ultra low dielectric materials for multilevel Cu interconnects below 65nm node. It is notable that some of pore properties such as size, shape, spatial distribution in the films may affect mechanical and electrical properties of the interconnects during BEOL processes such as metallization, CMP, and cleaning, and packaging processes. Several methods for characterizing the pore distribution and pore interconnectivity have been eagerly studied, e.g. high-resolution X-ray reflectivity, small-angle neutron scattering (SANS) curves collected under a satuarted solvent environment composed of different mixtures of hydrogenated and deuterated solvent. Because the SANS intensity is modified at the match point, mass density can be estimated from the SLD of solvent mixture displaying minimum scattering intensities. The correlation lengths of pores are determined at various partial pressures of CM solvent and the porosities at same partial pressures determined from the XRP are used to calculate the correlation lengths into pores sizes. In this work, we investigate pore structures in the methylsilsesquioxane-based materials with porogen loadings from 0% to 45%. We discuss the influence of porogen loading on the detailed structural information of pores in the thin films such as pore size distribution, wall density, average density, depth profile, wall homogeneity and porosity by using XRP and NP as complementary methodologies.

2:15 PM  **F5.3**

**Structural Characterization of Methylsilsesquioxane based Low-k Films Using X-ray and Neutron Porosimetry.**

Hoe-Jeong Lee1, Christopher L Soles1, Bryant D Vogt1, Da-Wei Liu1, Barry J Bauer1, Wen-li Wu1, Eric K Lin2, Gwi-Gwon Kang2 and Min-Jin Ko2, 1Polymers Division, National Institute of Standards and Technology, Gaithersburg, Maryland; 2LG Chemical Ltd, Taejon, South Korea.

The characterization of pore structure in porous thin films is essential to develop robust low dielectric constant materials that are compatible with adjacent semiconductor processes. X-ray porosimetry (XRP) and neutron porosimetry (NP) are recently developed methodologies to extract the detailed pore structures. These methodologies utilize unique principles to determine the volume fraction of solvent molecules (probe molecules) inside the accessible pores as a function of relative partial pressures. The partial pressure of the solvent is isothermally varied by mixing stream of dry air and solvent saturated air in a gas flow ratio. As the partial pressure increases, smaller pores are filled gradually. In XRP, the partial pressure is converted into pore sizes using the Kelvin equation and the amount of probe molecule uptake is used to determine the population of pores corresponding to that size. The mass uptake determined from the critical angle for total x-ray reflection without additional assumption concerning physical parameters using specular x-ray reflectivity. In NP, contrast matched (CM) solvent with a scattering length density (SLD) that is the same as that of wall material is first determined from a series of small angle neutron scattering (SANS) curves collected under a saturated solvent environment composed of different mixtures of hydrogenated and deuterated solvent. Because the SANS intensity is modified at the match point, mass density can be estimated from the SLD of solvent mixture displaying minimum scattering intensities. The correlation lengths of pores are determined at various partial pressures of CM solvent and the porosities at same partial pressures determined from the XRP are used to calculate the correlation lengths into pores sizes. In this work, we investigate pore structures in the methylsilsesquioxane-based materials with porogen loadings from 0% to 45%. We discuss the influence of porogen loading on the detailed structural information of pores in the thin films such as pore size distribution, wall density, average density, depth profile, wall homogeneity and porosity by using XRP and NP as complementary methodologies.
As the complexity of back-end-of-line processing continues to increase with the use of many new materials and deposition techniques, the need for reliable rapid adhesion evaluation becomes increasingly important. 4-point bending has established itself as the reference technique based on its ability to yield reproducible quantitative data. Additionally, it is independent of stresses in the stack as both sides of the tested interface remain fixed on a substrate after testing. Consequently it yields real interface adhesion, although this may not always be a good indicator for performance in an actual structure. Sample preparation and obtaining good statistics is, however, quite time consuming resulting in a slow feedback for process optimization. A faster method for adhesion evaluation is cross-section nano-indentation where a diamond tip is pressed into the side surface of a cleaved sample. By doing this just behind (several microns) the deposited stack, cracks can form from two of the corners of the triangular shaped tip outwards. When these cracks deflect into the weakest interface of the stack, delamination occurs and the length of delamination is proportional to the maximum indentor set-up. A series of 4-5 of such indents at several distances behind the interface normally yields a clear correlation between the force exerted and the delamination observed, and from this adhesion can be obtained. For quantification of the results we depend on both finite element simulations and a comparative study with 4-point bending. So far results have been obtained for adhesion of the copper-barrier interface using several different deposition techniques for both layers (ILD, electroplating, direct plating) as well as for the copper-barrier to the dielectric layer. 

Low-k dielectric materials have attracted a great deal of attention for application to multilevel Cu interconnects and packaging structures. The integration of microelectronic components requires various intermetal and interface layers between the low-k material and inorganic dielectric layers, such as SiO2 and SiC. Usually, the low mechanical properties exhibited by low-k dielectric materials are apt to cause debonding of the low-k layers and poor interfacial adhesion will lower the reliability of the interconnect structures. In this work, the adhesion of low-k interconnects with a SiO2 cap layer was evaluated using a nanoscratch method combined with AFM and TEM observations. The nanoscratch test demonstrated that the low-k layer with a rare-gas plasma pretreatment exhibited low delaminated densities in Cu CMP processes. Specimens having a microstructure of Cu/Ta/TiN/SiO2/low-k/SiC/pSiO2/Si-sub were examined, where the low-k layer of some samples was pretreated with rare-gas plasma before growing the SiO2 cap layer. Using the nanoscratch method, the fracture strength was characterized on the basis of the critical normal load at the first abrupt decrease in the friction coefficient. It was observed that specimens with the rare-gas plasma pretreatment displayed a higher friction coefficient and a higher critical normal load than specimens without the pretreatment. AFM observations showed that larger pile-ups were not present ahead of the nanoscratch on the nanoscratch side for specimens with the rare-gas plasma gas pretreatment. As for specimens without the rare-gas plasma pretreatment, it was observed that a scratch residual was situated ahead of the nanoscratch and was easily peeled while much smaller pile-ups were found at the nanoscratch side. These nanoscratch measurements demonstrated that the rare-gas plasma pretreatment reinforced the adhesion strength of the low-k interconnect with the SiO2 cap layer, as well as with the results obtained. The results indicated that the nanoscratch method make it possible to predict the CMP process endurance of the low-k interconnect structures and processes.

With device scaling continuing beyond the 130 nm node, low-k interlevel dielectrics (ILD) are being implemented to replace oxide in Cu interconnects. Their weak thermo-mechanical properties cause significant reliability problems for Cu/Low-k interconnects. Indeed, their low modulus and high thermal expansion coefficient can cause interfacial delaminating during thermal cycling or CMP. The dual-damascene structure of the Cu interconnect can give rise to complex stress states at the Cu/ILD interface. Therefore, it is important to study interfacial adhesion as a function of mode-mixity, from pure tension to pure shear. In this study, we developed a system allowing interfacial adhesion measurements as a function of mode-mixity. This system was evaluated by measuring the adhesion of a porous MSQ-based spin-on dielectric to a polished Cu surface comparing the results with previous results obtained with the four-point bending method. Critical adhesion energies were measured for various stress states ranging from mode I (pure tension) to mixed-mode loading (mode II combined) to mode II loading (pure shear). It was found that in every case, the debonding energy increased, by a factor of 3 to 10, as the amount of shear stress increased, approaching mode II conditions. The crack propagation path as a function of mode-mixity was also investigated using analytical tools including SEM, FIB and AFM. Additionally, the debonding energy increased on surrounding thin film layers on the adhesion energy was also observed.


While low-k dielectrics are being pursued by the semiconductor industry because of their electrical characteristics, mechanical properties such as hardness and elastic modulus are equally important in terms of providing structural integrity of interconnect structures. Techniques currently accepted in the industry for measuring mechanical properties (e.g. nano-indentation) are based on the assumption that film properties are isotropic. In thin film deposition, however, the presence of a substrate presents an asymmetric condition that may lead to structural anisotropy resulting from one-dimensional shrinkage, preferential alignment of polymer chains, or orientation of the pores. Consequently, elastic properties of thin film materials may be different for the directions parallel and perpendicular to the plane of the film. Nano-indentation is not adequate for characterization of such anisotropic materials. Methods based on surface acoustic waves, on the other hand, have proved capable of determining anisotropic elastic properties of thin films [1]. In this work, we characterized elastic properties of Novellus low-k materials by a non-contact technique utilizing laser-generated surface acoustic waves. Two materials were analyzed: a PECVD-deposited CORAL film (k = 3.0), and a novel porous ultra-low k film (k = 2.3). The most interesting finding is that of a strong anisotropy in the advanced porous low-k material. Namely, the "in-plane" compressional modulus is found to be 2-3 times larger than the "out-of-plane" modulus. We will discuss the relationship between the elastic anisotropy and the potential impact of a higher in-plane stiffness on the film performance.
Repeatability of Dielectric Barrier Films in Copper Damascene Applications. Albert Sanghyup Lee, Annamalai Lakshmanan, Nagaraj Balaraman, Young Le, Deonesh Padhi, Girish Dixit, Li Qin Xin, Bok Heon Kim and Hichem M’Saad; Dielectric Systems & Modules Product Business Group, Applied Materials, Inc, Santa Clara, California.

With the advent of copper dual damascene, dielectric copper barriers are becoming the cornerstone for back end of line device reliability. This paper will address two concepts for dielectric thin film reliability: hermeticity of the bulk barrier film and adhesion between the barrier and copper layers. It is known that improved adhesion corresponds to improved electromigration. In this paper, we show that adhesion is improved by interfacial engineering of the barrier film. We introduce the concept of a non-hermetic film, which is the film’s ability to prevent moisture from penetrating into the underlying layer. The barrier film hermeticity is important because a non-hermetic film can allow copper oxide formation at the barrier-copper interface, leading to adhesion loss and poor electromigration performance. In this work we have optimized the hermeticity of BLOs low-k copper barrier film. In addition, we have examined methods to modify the interface between copper and barrier films in such a way as to dramatically improve the adhesion of the BLOs and Damascene Nitride in SIN films to copper. We deposit BLOs in a PECVD Producer® Twin Chamber. We used a method to quantitate the film’s hermeticity, where 300Å copper barrier film is deposited on top of a 200Å TEOS oxide film with tensile stress, and the stack is subjected to 85°C and 85% humidity for 17 hours. A stress change in the stack indicates moisture uptake by the underlying oxide film, and a stress change of >25% indicates a non-hermetic barrier film. We adjusted the BLOs bulk film properties by varying the process deposition conditions to optimize the hermeticity. We compare the hermeticity of four films: 1) the optimized BLOs I, 2) Damascene Nitride, 3) an unoptimized BLOs film and 4) a reference with a copper barrier cap. The results demonstrate that the optimized BLOs I allows a stress change of 10MPa in the underlying oxide layer, and the hermeticity of BLOs I is comparable to that of silicon nitride. We used the 4-point bend technique to characterize the adhesion of BLOs I and Damascene Nitride to copper. We engineered the interface between the dielectric barrier and copper to promote adhesion of the two materials. During deposition of Damascene Nitride and BLOs, an in-situ pre-treatment step is used to remove copper oxide prior to depositing the barrier film. We optimized the transition between the pre-treatment and deposition to improve the barrier film adhesion to copper. By modifying the interface between the dielectric barrier and copper, we were able to significantly improve the adhesion strengths to >10 J/m² for both films. By optimizing both the bulk film properties (hermeticity) and the interface with copper (adhesion), we have demonstrated barrier film performance that minimizes reliability issues related to copper electromigration and stress migration.

SESSION F6: Poster Session: Integration and Reliability
Chairs: Grant Kloster and Toh-Ming Lu
Wednesday Evening, April 14, 2004
Salons 8-9 (Marriott)

F6.1 Deposition and Integration of a Novel Ultra-Low k (2.2) Material. Michelle T. Schulberg, Rashmi Himnayen, Arvinder Sangupta and Jia-Ning Sun; Novellus Systems, Inc., San Jose, California.

Increasing demands for faster chip speed and reduced power consumption are driving the semiconductor industry to develop insulating layers with lower dielectric constants. As the dielectric constant of a material is reduced, however, it becomes increasingly difficult to achieve the mechanical strength required to manufacture a multilevel interconnect. A new route to the synthesis of mesoporous silica has been demonstrated on 200 mm wafers. Silicate precursors dissolved in supercritical CO₂ are infused into a block copolymer film. The polymer is then removed, but the resulting porous SiOₓ replicates its ordered structure, which enhances the strength of the network. Incorporation of alkyl silicates further lowers the dielectric constant. Post-treatment to cap residual silanol groups renders the surface of the film hydrophobic and stabilizes it under air exposures. By appropriate choice of the block copolymer and other process parameters, the pore size and density can be varied and k values as low as 1.8 can be achieved. For a film with a dielectric constant of 2.2, the pore size is 4 nm. The hardness and modulus are 0.6 GPa and 4.0 GPa, respectively, as measured by nanoindentation. Four-point bend measurements yield fracture energies of 9.8 J/m². More importantly, the film can withstand chemical mechanical planarization (CMP) using standard oxide polishing conditions.


As ultra large scale integrated circuits (ULSIs) are scaled down, the signal delay through metal interconnects increases due to the parasitic capacitance. For 45 nm technology node, ultra-low dielectric constant (k ≤ 2.0) materials are needed. In order to reduce the dielectric constant, porous materials have been developed, while the introduction of pores to the film has caused severe degradation of the mechanical strength such as the elastic modulus and hardness. The motivation of this work is to achieve both ultra-low-k and high elastic modulus of the dielectric films. It is demonstrated that the mechanical strength of the porous silica films can be significantly improved by a novel organosiloxane vapor annealing process. The 1,3,5,7-tetramethylcyclotetrasiloxane (TMCTS) vapor treatment to the porous silica film was performed at the temperature range from 250°C to 350°C in nitrogen ambient. It was found that the elastic modulus of the porous silica film increased significantly with TMCTS treatment at 350°C or higher. When the porous silica film was treated by TMCTS at 400°C, the elastic modulus and the hardness of the film were enhanced by a factor of 2.5 and 3.0, respectively, as compared with the case without TMCTS. The FT-IR analysis indicates that the increase of the elastic modulus corresponds to the increase of the ratio of C-H stretching peak intensity arising from Si-C groups to the Si-H stretching peak. The thermal desorption spectroscopy analysis also suggested that the part of Si-H groups of TMCTS reacted with Si-OH groups on the porous silica wall surface via dehydrogenation, and the residual Si-H groups were converted to Si-OH groups through hydration by desorption of water. Subsequently, Si-OH groups of TMCTS reacted with other TMCTS. Finally polymerized TMCTS network was formed on porous silicon wall surface, resulting in the significant improvement of the mechanical strength of the porous silica film.

F6.3 Abstract Withdrawn

F6.4 Effect of Aqueous Solution Chemistry on Accelerated Cracking of Nanoporous Thin-Films. Eric P. Guyer and Reinhold H. Dauskardt; Materials Science & Engineering, Stanford University, Stanford, California.

Considerable effort has been directed toward integrating nanoporous films.
inorganic ultra-low dielectric constant materials into the interconnect structures of high-density integrated circuits. The reliable fabrication of low-k materials is an extremely challenging task. The issue is worsened when high moisture levels are generated in the low-k dielectric materials, which can lead to interlayer dielectric (ILD) failures. The reliability of low-k materials is highly sensitive to moisture absorption, resulting in the degradation of electrical properties. The moisture absorption in low-k dielectric materials occurs through the surface diffusion and different concentration of water-related traps. The moisture absorption can be quantified from the hysteresis effect in the C-V curves. This work is aimed at understanding the nature of the interactions between metal interconnects and dielectrics (dense and nanoporous) in integrated circuits. The mechanism for metal diffusion and charge injection and its dependence on porosity, size, surface area and surface chemistry of the dielectric in a closely coupled oxide-dielectric structure is of interest. A physically-based mathematical model of diffusion through dense and nanoporous structures was done through voltage ramp test at dense and isolated structures and results showed that film was sensitive to certain plasmas.


Future integrate circuit requires low dielectric constant (k) material as interlayer dielectric (ILD). The incorporation of porosity is the most plausible way of reducing the dielectric constant of a material below 2.2. Porous silica or silica xerogels are one promising alternative dielectric material as they can be made hydrophobic and the porosity and thickness can be tailored to desired values. Nevertheless, the porous material has several shortcomings such as metal precursor penetration into pore during CD and ALD and/or PVD processes, poor mechanical strength, and low thermal conductivity, etc. To avoid metal penetration during its deposition process, the pore sealing of the top surface of the porous material has been proposed without affecting the dielectric properties of the nanoporous material and it might even be improved. The fluorocarbon plasma is widely used to etch the low-k material and its intrinsic polymerization always exists during the process. We used CHF3 as a resistant gas to expedite the rate of polymerization due to the presence of hydrogen atom. Pressure is varied widely from 30mTorr to 90mTorr to change the number of neutrals which act as the polymerizing species. Film morphology is investigated by the scanning electron microscopy and perfect pore scaling is observed at 90mTorr on 56% porosity film.
discussed. The upper limit of Cu diffusivity in nanoporous silicas is estimated, and the model simulates the current observed during BTS testing reasonably well.

**F6.9**

**Pure Structure Determination and the CMP Performance of a Spin-On Porous Low-k Film Created with a Meso-Templating Technique, Wen-Li Wu, Youhan Liu, 2 sol, Brendan Foran, 2, Hae Jeong Lee, 2 and Bryan Vogt, 1** Polymers Division, NIST, Gaithersburg, Maryland; 2 International Sematech, Austin, Texas; 3 Intel, Hillsboro, Oregon.

A methylsilsesquioxane (MSQ)-based porous spin-on dielectric film produced using a mesocellular-templating scheme containing tubular structural units has been evaluated for advanced interconnect applications. The film structure was determined quantitatively with a combination of small-angle neutron scattering (SANS), specular X-ray reflectivity (SRX) and transmission electron microscopy (TEM). The tubular pores were found to align along both the free surface as well as the film/substrate interface. The number of surface aligned layers could be determined non-destructively from SRX results, which agreed with observations from cross sectional TEM. Other structural information, including porosity, average pore diameter and the density of the matrix material were also determined. The possible connection between the layered structure of the film and the cohesive failure of this film type during chemical-mechanical polish (CMP) process will be discussed.

**F6.10**

**Fundamental Limits for 3D Wafer-to-Wafer Alignment Accuracy, Markus Wimpinger, 1, Jian-Qiang (James) Lu, 2, Jia Yu, 1, Yongchao Kwon, 3, Thorsten Matthias, 3, Timothy S. Cale, 1 and Ronald J. Gutmann, 1** EV Group Inc., Phoenix, Arizona, 2 Focus Center - New York, Rensselaer: Interconnections for Hyperintegration, Rensselaer Polytechnic Institute, Troy, New York, 3EV Group Inc., Scharding, Austria.

Fundamental Limits for 3D Wafer-to-Wafer Alignment Accuracy. M. Wimpinger, J-Q. Lu, Y. Yu, Y. Kwon, T. Matthias, T. Cale, and R.J. Gutmann** EV Group Inc., 3701 E. University Dr., Phoenix, AZ 85034 1Rensselaer Polytechnic Institute, 110 8th Street, Troy, NY 12180 2EV Group, E. Thallner Str. 1, 4780 Scharding, Austria 3luj@rpi.edu Wafer-level three-dimensional (3D) integration as an emerging architecture for future chips offers high interconnect density, especially in the amount of hydrogen incorporated into the film. Detailed modeling is used for design optimization and also addresses how manufacturing variations from ideal design may affect device performance.

**F6.11**

**Optical Interconnect Components for Wafer Level Heterogeneous Hyper-Integration, Peter D. Persans, M. Ojha, R. Gutmann, J-Q. Lu, A. Filin and J. Flaws; Rensselaer Polytechnic Institute, Troy, New York.**

Future computer chips will include novel components that may include quantum spin state, quantum dot, magnetic, and/or magneto-optic components. Some of which may be based on molecular-scale structures. It is likely that these components will be integrated with CMOS-like devices and with significant portions of the chip based on CMOS manufacturing technologies. Connection to, or reading of, some of these components will be facilitated by direct optical interaction. High-speed communication off the chip will also be facilitated by integrating optics onto the chip. Here we describe optical waveguides for three-dimensionally stacked chip fabrication technologies, in which optical connection between layers plays a central role. We also address CMOS-compatible, low-k, dielectric films for optical waveguide fabrication. Detailed modeling is used for design optimization and also addresses how manufacturing variations from ideal design may affect device performance.

**F6.12**

**The Study of Modified Layers in Porous Dielectrics Formed by Plasma Interactions, Marcus Andre Worsley, 1, Perry A. Bent, 1, Stephen Gates, 2, Nicholas Fuller, 2 and Timothy Dalton, 2** Chemical Engineering, Stanford University, Stanford, California; 2 The Study of Modified Layers in Porous Dielectrics Formed by Plasma Interactions, Marcus Andre Worsley, 1, Perry A. Bent, 1, Stephen Gates, 2, Nicholas Fuller, 2 and Timothy Dalton, 2

Integration of new low-k interlayer dielectrics (ILD) with current damascene schemes is a continuing issue in the chip manufacturing industry. During integration of the ILD, processing steps such as etch, resist strip and chemical-mechanical planarization are known to chemically alter a layer of the dielectric. Here, porous and non-porous organosilicate glass films (OSG) are investigated. Both spectroscopic ellipsometry and XPS are used to characterize the modified layer of the O2 and H2 plasma. The effects of the two types of plasma etch chemistry on the formation of the modified layer were studied and found to differ significantly. These effects include both the degree of modification (i.e. chemical composition) and depth of modified layer. A key modified layer constant between the Q2 and H2 plasma is the fact that SiH4 is present in the modified layer after exposure to H2 plasma but not after exposure to the Q2 plasma. In addition, the influence of OSG porosity on the etch rate and modified layer thickness is demonstrated. The etch rate was found to increase rapidly with porosity. Finally, conditions including relative gas flows and substrate temperature for the H2 plasma were varied. These parameters produced considerable changes in the chemistry of the modified layer, especially in the amount of hydrogen incorporated into the film. Details of these results will be discussed in the context of the mechanism by which modification and etching occurs. The effects of process variables on the modified layer will also be discussed.

**F6.13**

**Effect of Porosity on the Properties and Processability of Low-k Dielectrics, Ananth Namag, 1, Teressa A. Ramos, 2 And Bhanap, 3 Ann Caramena, 1, Yohannes Negga, 1 and Rob Roth, 3** Honeywell Electronic Materials, Sunnyvale, California; 3 Nanopore Incorporated, Albuquerque, New Mexico.

The need for lower dielectric constant materials for use as intermetal and interlevel dielectrics is well-known in the semiconductor industry. The adoption has been well delayed compared to the ITRS forecast due to difficulties in integrating them into established BEO process flows. In this work, we present a systematic evaluation of the effect of porosity on the NANOGLASS family of materials. NANOGLASS offers the unique opportunity to tailor the porosity between 2.0 and 2.6 but maintaining the same polymer backbone. Predictably, increases in porosity lead to linear decrease in both dielectric constant as well as elastic modulus. The impact on porosity is not fully understood until these materials are used in single and multi level damascene interconnect structures. Integration issues such as the adhesion to adjoining layers is shown to also degrade. Additionally, the porous material shows much higher permeability resulting in higher moisture uptake along with higher susceptibility to damage during plasma processing such as RIE and ashing. This however is not all bad. Development of adhesion promotion materials along with toughening agents have proved that integration of materials with dielectric constants as low as 2.0 can be possible. Blanket films will be discussed with responses of interest being optical, electrical, thermal, mechanical, and elemental. In addition, single level damascene structures will be demonstrated actual use in a typical integration process flow.

**F6.14**


Properties of SOD low-k dielectric thin films were investigated as a function of formulation and processing variables. Characterization variables investigated included siloxane content, porogen type and porogen content. Formulations were shown to have excellent shelf life stability under standard conditions. All films met a dielectric constant of 2.2 and an elastic modulus of 5.6 GPa were obtained, while maintaining an average pore size of 3 nm with a narrow distribution. In addition, films exhibited excellent film thickness uniformity, high adhesion strength and were successfully integrated into a dual-damascene copper integration scheme.

**F6.15**

**Investigation of the Interfacial Adhesion and its Correlation with Chemical Mechanical Polishing for Various Low-k and Cu-low k Multi-layered Thin Films.** Parasharan Balkrishna Nare, 1, Arun Sikder 2 and Ashok Kumar 1, 2.

1 Department of Mechanical Engineering, University of South Florida, 2 Center for Nano-Science and Applications, USA.
Tampa, Florida; *Nanomaterials and Nanomanufacturing Research Center, University of South Florida, Tampa, Florida.

There is increasing implementation of low k materials as inter layer dielectrics (ILD) and multilevel metallization schemes using Cu-low k single and dual damascene structures to reduce the RC (Resistance X Capacitance) delay in advanced ICs. In our approach, we have performed extensive studies on the mechanical properties of Chemical Polishing (CMP). Estimation of interfacial adhesion energy is done using the four-point bend test. In this research, after having done the four point bend test, we have performed a number of important experiments. We have achieved an interfacial adhesion energy of 1.2 J/m², which is significantly higher than the reported values of 0.5-0.8 J/m². The adhesion energy is directly proportional to the bonding strength between the interfacial layers and the adhesion energy is done using the four-point bend test. In this test, the samples are bent to a specific angle, and the force required to cause failure is measured. The adhesion energy is then calculated using the following formula:

\[ \text{Adhesion Energy} = \frac{1}{2} \times F \times b \times L \]

where F is the force at failure, b is the thickness of the sample, and L is the distance between the load and the support points.

The interface failure gives rise to the increase of local bonding energy and modulus at low temperatures. For the hardener alone we have measured film hardness and modulus of 2.5 GPa and 14.5 GPa for a deposition temperature of 300 °C. For tetramethyldicyclosiloxane (TMCTS) with 25% hardener we have observed film hardness and modulus as 1.4GPa and 8.8GPa. To achieve this, significant efforts are being made in developing new materials that can withstand the high temperatures and pressures involved in the CMP process.

Yongchao Kwon, Jian Yu, Jay J. McMahon, Jian-Qiang Lu, John Y. Q. Huang, Abigail A. Ebbing, and Excellence in the Science and Engineering, University of Massachusetts, Amherst, Massachusetts; 2Department of Chemical Engineering, University of Massachusetts, Amherst, Massachusetts; 3Department of Materials Engineering, University of Massachusetts, Amherst, Massachusetts; 4Polymer Science and Engineering, University of Massachusetts, Amherst, Massachusetts; 5Department of Materials Engineering, University of Massachusetts, Amherst, Massachusetts.

We have recently applied small-angle neutron scattering (SANS) contrast variation to characterize four spin-on low k materials including a methylsilsesquioxane (MSQ), an organic polymer, a xerogel, and a variety of low K precursors their mixtures specifically chosen to characterize four spin-on low k materials including a methylsilsesquioxane (MSQ), an organic polymer, a xerogel, and a low-K precursors. We have observed film hardness and modulus at low temperatures. For the hardener alone we have measured film hardness and modulus of 2.5 GPa and 14.5 GPa for a deposition temperature of 300 °C. For tetramethyldicyclosiloxane (TMCTS) with 25% hardener we have observed film hardness and modulus as 1.4 GPa and 8.8 GPa. To achieve this, significant efforts are being made in developing new materials that can withstand the high temperatures and pressures involved in the CMP process.

Dong Niu, Qingguo Wu, Ananda Bandyopadhyay, Haiying Fu, and David Mordo; Novelus Systems, Tualatin, Oregon.

As the interconnect design continues to shrink, the back end of the line (BEOL) technology encounters severe challenges due to increasing signal propagation delay and crosstalk among metal lines situated in close proximity. To minimize these effects, significant efforts are being made to develop low dielectric constant (low k) materials, such as carbon doped oxide (CDO), that can be used as interlayer dielectrics for 90nm and 65nm technology nodes. The current method for the development of low-k CDO films primarily relies on the incorporation of methyl group (-CH3) in the Si-O matrix. However, this approach adversely affects the mechanical properties of the CDO film, thus elevating adhesive and cohesive failures in the Cu-low k integrated structures. Consequently, there is a need to develop a method that can be used to modify the k value and the mechanical strength of the bulk CDO film.

In this study, we report the results of our studies toward obtaining improved mechanical properties of CDO film deposited by using plasma enhanced CVD method. Various properties of the deposited films, including k, stress, hardness, modulus, and cracking behavior, have been extensively studied to achieve deeper understanding of their interdependence. In addition, their correlation with film composition and structure has been established. With appropriate optimization of film deposition conditions, the mechanical strength and the cracking resistance of CDO film are dramatically improved without sacrificing its dielectric constant.

F6.18 Chemical Routes to Improved Mechanical Properties of PECVD Low k Thin Films.
Steven Biddle, Alexander S. Borowik, Abigail A. Ebbing, Daniel J. Vest, and Chongying Xu; Jeffrey F. Roeder and Thomas H. Baum; ATMI, Danbury, Connecticut.

Increasing the elastic modulus and hardness of low k films addresses one of the key challenges towards integration of these materials into future integrated circuits. Several approaches are under consideration for increasing the hardness of CDO dielectrics. We have evaluated a variety of low k precursors to achieve hardness that is significantly higher than the currently observed values. This has been achieved by reducing the content of Si-CH3-Si bonded in the deposited films. This has been confirmed by the observed decrease of the fraction of bonded area and weak adhesion at the BCB interface. The failure of the interface gives rise to the increase of local bonding energy and modulus at low temperatures. For the hardener alone we have measured film hardness and modulus of 2.5 GPa and 14.5 GPa for a deposition temperature of 300 °C. For tetramethyldicyclosiloxane (TMCTS) with 25% hardener we have observed film hardness and modulus as 1.4 GPa and 8.8 GPa. To achieve this, significant efforts are being made in developing new materials that can withstand the high temperatures and pressures involved in the CMP process.

F6.19 Abstract Withdrawn.

Ronald C. Hedden, Barry J. Bauer, Hao-Jeong Lee, Christopher L. Sikes, Wei-Li Wu, and Eric K. Lin; 1Materials Science and Engineering, Penn State University, University Park, Pennsylvania; 2Polymers Division, NIST, Gaithersburg, Maryland.

We have recently applied small-angle neutron scattering (SANS) contrast variation to probe the structure of mesoporous low-k thin films. Using a flow-through sample cell for SANS, samples are exposed to saturated solvent vapor in air, whereby the pores fill with liquid by capillary condensation. The pores are filled with mixtures of hydrogen and deuterium containing solvents to vary the contrast between the wall and the pore. The composition of the solvent mixture is systematically varied to identify a composition that minimizes the scattering intensity (contrast match point). From the contrast match point composition, film microstructure characteristics including film density and homogeneity are assessed. Previously, we applied SANS contrast variation to characterize two spin-on low k materials indicating a methylsilsequioxane (MSQ), an organic polymer, a xerogel, and a hydrosilsequioxane (HSQ). Calculated matrix mass densities were comparable to independent density measurements obtained by an established X-ray reflectivity (SXR) technique. We found no evidence of "closed pores," defined as pores inaccessible to the probe solvent, in any of the materials studied. Our recent work has combined SANS contrast variation with capillary porosimetry, creating a new approach to the determination of pore size distributions. Capillary porosimetry experiments are conducted using solvent uptake from SXR characterizes the pore size distribution directly without the need for a thermodynamic model for adsorption.

F6.21 SANS characterization of mesoporous materials using contrast match method. Barbara D. Vogel, Hao-Jeong Lee, Ronald C. Hedden, Christopher L. Sikes, Wei-Li Wu, Eric K. Lin, Barry J. Bauer, Rajaram Pai, and James J. Watkins; 1Polymers Division, NIST, Gaithersburg, Maryland; 2Department of Chemical Engineering, University of Massachusetts, Amherst, Massachusetts; 3Department of Materials Engineering, University of Massachusetts, Amherst, Massachusetts.

The pore structure of thin mesoporous silica films have been characterized using a small-angle neutron scattering (SANS) porosimetry technique. The films were synthesized via a CO<sub>2</sub>-based infusion process using block copolymers containing hydrophilic and hydrophobic domains as the mesopore templates. The nature of the pore structure, and its adjustment with the composition of the framework of the mesoporous structure. Structures containing various levels of carbon in the framework as well as pure SiO<sub>2</sub> were prepared by the selection of an appropriate precursor or mixtures of precursors. SANS porosimetry exploits the
partial pressure dependence of capillary condensation of a probe molecule within a pore on the pore size. Therefore, changes in the scattering profile of deuterated toluene can be directly related to the pore structure. For case of data analysis, a contrast match solvent is used as the probe molecule. To create a contrast match solvent for the porous films, the scattering profiles of the films were collected under a series of saturated solvent environments composed of deuterated and protonated toluene. At a concentration of approximately 40% (v/v) deuterated toluene, all the coherent scattering from the sample was eliminated, indicating a contrast match point. At this point, the scattering length density of the wall material equals that of the solvent, which can be used to determine the wall mass density with knowledge of the wall material chemical composition. The presence of a match point indicates that (1) all the pores are accessible to the toluene vapor and (2) the wall material is homogeneous. The pore structure is then determined by varying the relative partial pressure of the contrast match solvent from 0 to 1. In the case of all empty pores \( p/p_o < 0.1 \), the scattering profile contains two distinct structures: a strong Bragg peak corresponding to the mesopores templated by the block copolymer and a Debye-type scattering corresponding to disordered micropores with an average dimension of approximately 11 nm. These micropores are likely a result of the interpenetration of the silica network and the hydrophillic domain of the block copolymer. Analysis of films synthesized in the same manner as the mesoporous sample, but using a homopolymer template of the same chemical composition as the hydrophillic domain in the block copolymer template supports this view. In the case of the homopolymer template, disordered micropores with the same dimension were observed.

**F6.22 Characterization of PECVD Low-k Films by Positronium-Annihilation Lifetime Spectroscopy (PALS).**
Toshiyuki Ohdaira, Toshihiko Suuki, Yoshimi Shioya, and Komo Masuda,光学生物研究所,国立中央大学,日本; 2 Semiconductor Process Laboratory, Co., Ichikawa Chiba, Japan.

Positronium annihilation lifetime spectroscopy (PALS) was used to measure pore (free volume) size distributions in SiOCH films for low-k ILD and Cu diffusion barriers, which were grown by PECVD with source gas of HMDSO (hexamethyldisiloxane). In the PECVD, the dielectric constant \( k \) of the film changes with the deposition conditions such as gas flow rate, pressure, temperature, RF power, etc. The PALS results showed that the PECVD-grown SiOCH films with \( k \) in the range from 2.6 to 4 contain pores with average sizes from 0.4 to 1.2 nm, and that the \( k \) value by PALS is 2.6. These micropores are likely a result of the interpenetration of the silica network and the hydrophillic domain in the block copolymer template. Little metal ions were detected in the nanoporous dielectric films.

**F6.23 Morphology and Physical Properties of Hybrid Materials based on Novel Poly(methyl phenylsilsesquioxanes).**
Soon Man Hong, Seung Sang Hwang, Kwang Ung Kim, Hang Seok Lee, Cheol Chung and Sungwon Mo, Polymer Hybrid Center, Korea Institute of Science & Technology(KIST), Seoul, South Korea.

Inorganic/organic hybridization based on polyorganosilicones and PSSQs has lately attracted scientific and industrial interests because of excellent optical transparency and low refractive index of inorganic polymer. The organic dispersed inorganic matrix would be applicable to innumerable industrial fields such as microelectronic packaging insulators, optical devices, liquid crystal materials, etc. Inorganic/organic hybrid nanostructures are studied by morphological behaviors, and different conditions.

**F6.24 Electrical and Thermal Stability of Moleculely Templated Nanoporous Silica Dielectrics for Cu Metallization.**
Ji-Yu Chen, Fu-Ming Pan, Li Jiang, An-Thong Cham and Kuei-Jung Chen, Materials Science and Engineering, National Chiao Tung University, Hsinchu, Taiwan; 2 National Nano Device Laboratories, Hsinchu, Taiwan; 3 Chemistry, National Tsing Hau University, Hsinchu, Taiwan.

Nanoporous silica thin films are believed to be a potential candidate for intermetal dielectrics for sub-70 nm technology nodes due to their ultra-low dielectric constant \( 2.0 \) and chemical compatibility with modern ULSI process technologies. The as-prepared nanoporous silica films are usually hydrophilic, and, therefore, needed to be chemically modified to improve the hydrophobicity so that stable dielectric properties can be obtained. Trimethylsilylation is a common method to enhance hydrophobicity of porous silica films. However, trimethylsilyl groups thereby created in the porous film may be destroyed during the subsequent IC processes, causing reliability problems. In this work, the effects of and dielectric properties of trimethylsilylated nanoporous silica films exposed to hexamethyldisilazane (HMDS) vapor, have been studied. Hydrophobicity of the as-calcined nanoporous silica films spin-coated on Si wafers was significantly improved by the trimethylsilyl treatment. The nanoporous silica films before any hydrophobicity treatment were used as porogen materials. Prepared inorganic/organic hybrids are spin-coated on Si wafers was significantly improved by the trimethylsilyl treatment. The nanoporous silica films before any hydrophobicity treatment were used as porogen materials. Prepared inorganic/organic hybrids were spin-coated on Si wafers to form microporous silica films.

**F6.25 Three Dimensional Interconnect Stress Modeling for Back End Process.**

In modern integrated circuits, interconnects consist of multilevel metal lines that are embedded within dielectric insulators and separated by diffusion barriers above the silicon transistors. To prevent electromigration, the interconnects are surrounded by viscous materials, and the geometry changes due to deposition and etching steps. The evolution of stress changes is three dimensional in nature. The residual stresses in interconnects are known to cause yield and reliability issues and it has been a major effort to develop stress models for back end processes. Historically, interconnect stresses are modeled with various assumptions. For example, 2D plane strain or 2D axisymmetric simplifications are made for a 3D structure; viscous relaxations in low-k dielectric materials are ignored. A recent numerical treatment has been introduced to activate and deactivate elements in the mesh for deposition and etching of materials. Stress simulations with such assumptions become increasingly inadequate to predict stress distributions inside interconnects that are fabricated with complex back end process flows. In this study we use our three-dimensional process simulator Taurus-Process to simulate the stress evolution for the entire interconnect fabrication process flow. No ad hoc assumptions regarding stress states are required during region adoptions and removals. Interconnect stresses are introduced during material formation, thermal mismatch stresses from temperature ramps, stress relaxations from viscous deformation, and stress profile redistribution of deposition and etching are all considered at every process step by solving stress equilibrium equations with evolving boundary conditions. Parametric studies are carried out to examine the effects of intrinsic stress, process thermal budgets, layer formation, viscous flow and material selection. Full stress evolution histories are obtained for all components in the interconnect trees. A TCAD-based design approach is suggested for lowering stress levels of high reliability stress components. The implications of the stress modeling results on yield and reliability issues are discussed.
This study is devoted to thermomechanical stresses and their modeling in copper interconnects. Constitutive behavior of encapsulated metal wires is first determined by experimentally measuring the stress-temperature response during thermal cycling. The material model is subsequently used for predicting stresses in copper interconnects. Various combinations of postulated low-k dielectric schemes are considered. The evolution of stresses and deformation pattern in the dual-damascene copper, barrier layers, the dielectrics and their interfaces is seen to have direct connections to the structural integrity of contemporary and future-generation devices. In particular, stresses experienced by the thin barrier layers and the mechanically weak low-k dielectrics are critically assessed. Salient features are compared with those in traditional aluminum interconnects. Practical implications in reliability issues such as voiding, interface delamination, electromigration and dielectric failure are also discussed.

**F6.27**


We have developed a near-field ultrasonic holography (NFUH) system which combines the nanometer-scale spatial resolution of conventional scanning probe microscopies (SPMs) with the surface and sub-surface imaging capabilities. In NFUH, a high frequency (500 KHz) acoustic wave is generated on the bottom of a structure, and the wave is launched on AFM-type cantilever tip under a different frequency. The spectrum acoustic wave interacts with defects in the specimen and subsequently interferes with the cantilever “reference” wave. The sub-surface defects are then measured and analyzed by the scanning probe tip as an “antenna”. The resulting signal can be readily split between phase and amplitude part of the local interference, lending remarkable useful information about the internal structure of specimen. This technique will fill a critical void in characterization and investigation of the static and dynamic mechanics of nanoscale systems, ranging from engineering system to biologically active structures, in-vitro. In the presentation, we will report our results on high resolution sub-surface imaging copper vias (without doing any cross-sectioning) and in-vitro biological structures (e.g. looking through the cell-membrane, implant-bio interfaces etc) at acoustic carrier frequency of 2 MHz. It will be argued that ramping the cantilever frequency to 100 MHz would enable the extraction of sub-surface defects (voids, delamination, cracks etc) with Z height resolution (depth height) of << 5 nm, while maintaining the high spatial resolution of SPM.

**SESSION F7: Copper Reliability**

Chair: Christine Hau-Riege and Stefan Hau-Riege

Thursday Morning, April 15, 2004

Room 203 (Moscone West)

**8:30 AM *F7.1**


The metallization of integrated circuits consists of complexly connected segments between nodes. Nodes include vias and junctions at which segments join other segments, either in the same level of metallization or in other levels of metallization. Most strategies for circuit-level reliability assessments are based on analyses of segments that are treated as independent fundamental reliability units. However, as has now been shown for both Al-based and Cu-based metallization, the reliability of a segment depends on the numbers, types, and stress conditions of neighboring segments, so that segment-based circuit-level reliability assessments give projections that are neither consistently conservative nor optimistic, and in fact have no usefulness. When via fully block electromigration, interconnect trees can be defined as independent fundamental reliability units and can be used as the basis for accurate circuit-level reliability assessments. Interconnect trees are a collection of connected segments that are segments that have current density along the interconnection path. This alternative strategy will be described, along with its implementation in circuit-level reliability analyses using a new tool SynRel, which has been developed for this purpose. This tool permits assessment of the impact of critical assumptions on reliability assessments, and can guide the development of technology improvements that will have the greatest impact on circuit-level reliability.

**9:00 AM *F7.2**


Different values of critical current-density line-length product (jL) C for Cu interconnects, below which the interconnects are immortal, have been reported. We report studies of the mortality of interconnect segments connected to active and inactive adjacent segments. Experiments were carried out on straight via-terminated lines with an additional via in the middle that creates two segments with 25 μm lengths (‘dotted-I’ structures). The test structures were in metal 2 and connected to metal 1 in ‘via-below’ configurations. The current density in the right segment was kept constant at 0.5 MA/cm² with the electrons flowing from the right via towards the middle via, while the current density in the left segment was varied from 0 to 2.5 MA/cm², with electrons flowing in both directions. All the samples were stressed for 780 hours and the failure criterion was set as 30% resistance increment. Due to the low failure rate of the samples, comparison between the different testing conditions was done using the failure percentage instead of t50. Mortalities were found in the dotted-I right segment with a jL value as low as 1250 A/cm compared to the lowest reported (jL) C of 1500 A/cm. Moreover, we found that the mortality of a dotted-I right segment is dependent on the direction and magnitude of the current in the segment. The failure percentage of the right segment reduces with the current density when the electrons flow in the same direction in the left segment. It increases with current density when the electrons flow in the opposite direction, with the lowest failure percentage corresponding to about 0.35 MA/cm² in opposite direction. For the cases in which the left segments have a current density of 1.5 MA/cm², flowing in the same direction as the right segment, over 40% of these samples’ right segments failed earlier than the left segments, even though the current densities in the left segments were higher. These results suggest that there is not a definite value of the jL product that defines true immortality in individual segments that are part of an interconnect tree. Moreover the critical jL value for a single segment of Cu interconnects may be reduced or increased by an adjoining segment. Therefore independently determined (jL) C values cannot be applied to interconnects with branched segments, but rather the magnitude as well as the direction of the current flow in the adjoining segments must be taken into consideration in evaluating the immortality of particular interconnects.

**9:15 AM *F7.3**

Unexpected Mode of Plastic Deformation in Thin Films Undergoing Electromigration. Arif S. Budiman, 1 N. Tamura, 2 C. B. Valek, 1 K. Gadre, 3 J. Maiz, 3 R. Spolenak, 4 W. A. Caldwell, 2 A. A. MacDowell, 2 R. S. Celestre, 3 H. A. Padmore, 4 J. C. Bravman, 5 W. B. Batterman, 1 W. D. Nin, 5 and J. R. Patel, 2, 4 Materials Science & Engineering, Stanford University, Stanford, California; 5 Advanced Light Source (ALS), Lawrence Berkeley Laboratory (LBL), Berkeley, California; 6 Max-Planck-Institut fur Metallforschung, Stuttgart, Germany; 7SSL/SLAC, Stanford University, Stanford, California.

An early (pre-failure) mode of plastic deformation was previously reported during in-situ x-ray micro-diffraction experiments on electromigration (EM) in the copper (Cu) system. Indeed, observations on passivated lines of damascene Cu interconnects during electromigration are described in this paper. During in-situ electromigration studies on Cu lines, streaking or broadening of Laue spots transverse to the direction of electron flow has been observed. Some broadening of Laue spots was detected at the anode end of the line and preliminary findings indicate that the bending of individual grains is convex. From the broadening we calculate the dislocation density at an individual grain boundary from the observed streaking. In the broadened spot we can determine the tilt of small angle boundaries. The deformation geometry leads us to conclude that dislocations introduced by plastic flow lie in the broadened spot transverse to the direction of electron flow in the opposite direction, with the lowest failure percentage corresponding to about 0.35 MA/cm² in opposite direction. For the cases in which the left segments have a current density of 1.5 MA/cm², flowing in the same direction as the right segment, over 40% of these samples’ right segments failed earlier than the left segments, even though the current densities in the left segments were higher. These results suggest that there is not a definite value of the jL product that defines true immortality in individual segments that are part of an interconnect tree. Moreover, the critical jL value for a single segment of Cu interconnects may be reduced or increased by an adjoining segment. Therefore independently determined (jL) C values cannot be applied to interconnects with branched segments, but rather the magnitude as well as the direction of the current flow in the adjoining segments must be taken into consideration in evaluating the immortality of particular interconnects.
9:30 AM F7.4
Coupling Between Precipitation and Plastic Deformation During Electromigration in a Passivated Al (0.5 wt % Cu) Interconnect. Rozalia I Barabash1, Gene E. Ice1, Nobumichi Tanura2, Bryan Valek2, John Bravman3, Ralph Spolenak2 and Jim Patton1, 1Metals and Ceramics Div., Oak Ridge National Laboratory, Oak Ridge, Tennessee; 2Advanced Light Source, Berkeley, California; 3Dept. Materials Science and Engineering, Stanford University, Stanford, California; 4Stanford Synchrotron Radiation Laboratories, Stanford, California; 5Max Planck Institut für Metallforschung, Stuttgart, Germany.

The scaling of device dimensions with a simultaneous increase in functional density poses a challenge to materials technology and reliability of interconnects. White beam X-ray microdiffraction is particularly well suited for the in-situ study of electromigration. The technique was used to probe microstructure in interconnects and has recently been able to monitor the onset of plastic deformation induced by mass transport during electromigration in Al (Cu) lines even before any macroscopic damage became visible. In the present paper, we demonstrate that the evolution of the dislocation structure during electromigration is highly inhomogeneous and results in the formation of unpaired randomly distributed dislocations as well as geometrically necessary dislocation boundaries. When almost all unpaired dislocations and dislocation walls with the density n are parallel (as in the case of Al-based interconnects), the anisotropy in the scattering properties of the material becomes important, and the electrical properties of the interconnect depend strongly on the direction of the electric current relative to the orientation of the dislocation network. A coupling between stress-assisted, growth and diffusion of Al2Cu precipitates and the electromigration-induced plastic deformation of grains in interconnect is observed.

10:15 AM F7.5
Effect of mass transport along interfaces and grain boundaries on copper interconnect degradation. Birnfredt Zeschch, Moritz Andrea Meyer and Eckhard Langer, Materials Analysis, AMD Saxony LLC & Co. KG, Dresden, Germany.

For leading edge microprocessors, both advanced process technologies and new combinations of materials bring new reliability challenges to on-chip copper interconnect microstructures. Other types of interfaces and new degradation phenomena. Electromigration, stress-induced migration and mechanical weakness in case of low-k materials are reliability concerns for inlaid copper interconnects. In addition to standard reliability tests which allow statistically relevant conclusions, the study of degradation mechanisms for a limited number of representative samples is needed to understand process weaknesses and to exclude reliability-related failures in copper interconnects. We designed experimental setups to study reliability-limiting degradation mechanisms in interconnects in such a way that mass transport and interconnect degradation are visualized in-situ at fully embedded copper via/line test structures [1,2]. Depending on the location of the bonding copper/barrier stop and the copper/barrier layer, voids are formed at one of the interfaces. Initial shallow voids remain at their position until a certain critical size is reached. The mass transport dominates along the weakest interface, i.e. the pathway with the highest transport rate, towards the end of the line. The discontinuous, step-like void movement process depends on the localization of grain boundaries. At the line end, the voids merge into a larger void which subsequently grows within the via. Once a large void, and consequently an inner surface, has been formed, the void growth process seems to be dominated by diffusion along inner surfaces. Since the diffusion rate is expected to be different for different crystallographic orientations of the grain next to the void, grains with different orientation are disintegrated at different speeds. It is an important observation from these in-situ SEM experiments that both the void movement along the copper line and the void growth in the via are discontinuous step-like processes. To make this time-dependent void evolution more visible, we have analyzed the projected void area from the SEM image for the via/line interconnect structure [3]. Combining the results of the in-situ SEM study with copper microstructure data obtained on EBSD, it can be clearly shown that void formation, growth and movement, and consequently interconnect degradation, depend on both the interface bonding and the copper microstructure of the inlaid copper interconnects. [1] S. Haschke et al., Acta Mater. 50, 5615-5625, 2002 [2] G. Schneider et al., Dynamical X-ray Microscopy Investigation of Electromigration Phenomena in Fully Embedded Copper Interconnect Structures, Microelectronics Engineering 64, p. 375, 2002 [3] E. Zeschch et al., Failures in Copper Interconnects: Localisation, Analysis and Degradation Mechanisms, Proc. IFFA, in press, 2003

10:45 AM F7.6
Fatal Void Size Comparisons in Via-Below and Via-Above Cu-Doped-Damascene Interconnects. Zung-Sun Chol1, Choe Lop Gan2,3, Carl V. Thompson1,2 and Jung Hoon Lee3, 1Materials Science and Engineering, MIT, Cambridge, Massachusetts; 2Singapore-MIT Alliance, NUS, MIT, Singapore, Singapore; 3School of Materials Engineering, Nanyang Technological University, Singapore, Singapore; 4Advanced Light Source, Advanced Energy Engineering and Computer Science, MIT, Cambridge, Massachusetts.

The median-times-to-failure (50%) for straight dual-damascene via-terminated copper interconnect structures, tested under the same conditions, depend on whether the vias connect down to underlying layers (metal 2, M2, or via-below structures) or connect up to overlaying leads (metal 1, M1, or via-above structures). Experimental results for a variety of line lengths, widths, and numbers of vias show higher 50%'s for M2 structures than for analogous M1 structures. It has been shown that despite this asymmetry in lifetimes, the electromigration drift velocity is the same for these two types of structures, suggesting that fatal void volumes are different in these two cases. A numerical simulation tool based on the Korhonen model has been developed and used to simulate the conditions for void growth and correlate fatal void sizes with lifetimes. These simulations suggest that the average fatal void size for M2 structures is about two to three times the size of that of M1 structures. This result supports an earlier suggestion that preferential nucleation at the Cu/Si3N4 interface in both M1 and M2 structures leads to different fatal void sizes, because larger voids are required to span the line thickness in M2 structures while smaller voids at the base of vias can cause failures in M1 structures. However, it is also found that the fatal void sizes corresponding to 15 times the median-times-to-failure (95%) are similar for M1 and M2, suggesting that the voids that lead to the shortest lifetimes occur at or in the vias in both cases, where a void need only span the vias to cause failure. Correlation of lifetimes and critical void volumes provides a useful tool for distinguishing failure mechanisms.

11:00 AM F7.7
Void Growth and Failure Statistics for Electromigration in 0.13 μm Cu Interconnects. M. Haschke1, S. Thrasher2, M. Michaelson2, R. Hernandez2, P. Justison2, M. Gall2, H. Kawasaki2 and P S Ho1, 1Interconnect and Packaging Group, The University of Texas at Austin, Austin, Texas; 2DigitalDNA Laboratories, Motorola, Austin, Texas.

The introduction of Cu and low-k dielectrics and continuing scaling of on-chip interconnects raise serious reliability concerns on electromigration (EM) and stress-induced voiding (SIV). EM lifetime statistics usually follow a lognormal distribution with the median lifetime depending on the quality of the interface, which controls the mass transport. The standard deviation $\sigma$ is a key parameter for extrapolating EM lifetime under operating conditions, yet its origin is not well understood. In this study, we investigate EM failure statistics and the origin of $\sigma$ for Cu interconnects by analyzing the statistics of EM lifetime and void size distributions at various stages during EM testing and their correlation to the grain size distribution. EM experiments were performed on 0.18 μm Cu test structures at 300°C and 1.5 MA/cm2 where tests were terminated after specific amounts of resistance increases for void growth analysis. To examine the statistical correlation of EM lifetime, void size distributions were analyzed in 0.18 μm Cu lines using focused ion beam and transmission electron microscopy. The lifetime and void size distributions were found to follow lognormal distribution functions with $\sigma$ values of both data sets decreasing with higher percentages of resistance increase. Results on grain size analysis showed that $\sigma$ decreases with the number of combined grains, but their values are larger than the corresponding values of EM lifetime and void size. This result suggests that geometrical factors related to the grain size distribution cannot account for the observed EM and void growth characteristics. Statistical factors governing the kinetics of mass transport for different grain interfaces have to be considered, together with the statistics of initial void formation and its effect on void morphology. The statistical correlation among these parameters is being evaluated using Monte Carlo simulations. Initial results indicate that void size distributions can indeed be simulated by considering geometrical variations of the void shape. Results will be reported.

11:15 AM F7.8
Stress-induced voiding in Cu/oxide interconnect structure. Won-Chong Back and Paul S. Hc, University of Texas at Austin, Austin, Texas.

Stress-induced voiding in Cu/oxide interconnect structure with 0.36 μm via was investigated. Via chain structures composed of two metal levels with different linewidth connected by vias were used. Results show two kinds of void formation mechanisms depending on linewidth. In narrow line structures (linewidth = 0.44 μm and via = 0.36 μm), temperature dependence of resistance increase indicates a typical
behavior of stress-induced voiding with an activation energy of 0.75 eV, and peak rate at 240 °C. The activation energy is consistent with that of interfacial mass transport in Cu. Most of resistance increases arose from void formation at the periphery of via bottom as FIB observations revealed. This phenomenon occurred at relatively low temperatures. However the resistance increase was small, so further study is needed to elucidate the influence of this type of stress-induced voiding on resistance. In wide line structure ( linewidth = 2.0 μm, via ≈ 0.36 μm), resistance increases did not follow the typical type of stress-induced voiding. The rate of void formation did not show a peak at an intermediate temperature, the rate of resistance increase increasing exponentially up to 350 °C. The activation energy was found to be 1.0 eV. Similar to narrow lines, most of resistance increases arose from void formation in the lower metal lines. This phenomenon is significant at relatively higher temperatures, and at 350 °C, the resistance increase was four times as large as that of peak rate of narrow line stress migration. Further study is underway to investigate this phenomenon.

Effect of Dielectric Materials on Stress and Stress Induced Voiding

In the case of dual damascene Cu interconnects were studied using x-ray diffraction and three-dimensional finite element analysis. For this purpose, periodic line structures and via-line structures incorporating two different dielectric materials, tetraethyl orthosilicate (TEOS) and low-k materials, were investigated. Damascene Cu lines varied in width and spacing simultaneously were fabricated by controlling a lithography dose in order to manage stress on narrow lines using x-ray diffraction. For the case of the lines with TEOS, high Young's modulus, and very low Young's modulus. Using a three-dimensional finite element analysis, the stress and stress distributions of the via-line structures were calculated with two types of dielectrics. In the case of TEOS, large hydrostatic stress was concentrated on the via and the top of the lines, where voids were expected to nucleate and grow. On the other hand, the line spacing dependence on stress was not prominent in the case of lines with CORAL which have higher CTE and very low Young's modulus. A good correlation between the FEM prediction and experimentally observed failure was obtained in the different dielectric materials. Based on experimental and simulated results, it was found that stress-induced damages are caused by level and distribution of von-Mises and hydrostatic stress and strain structures of the lines which are related to vacancy diffusion path. From a successful optimized process condition and geometries of via-line structures to prevent stress induced damage are obtained.

Characterization of the Copper Migration through Dielectric Materials during Bias Temperature Stressing by Capacitance-Voltage Measurement and the Numerical Analysis

Copper migration through inter-metal dielectric (IMD) materials is one of the serious problems in the reliability concerns for copper metallization. In order to develop the comprehensive model to describe the copper migration in IMD during bias temperature stressing (BTS) was investigated by capacitance-voltage (C−V), current-voltage (I−V) time-dependent dielectric breakdown (TDBB) measurements. The numerical model is validated by the measurements. It is thought that the present numerical method can be used to evaluate the copper diffusivity in various low-k dielectric materials with the C−V measurement of Cu/low-k dielectric material/Si capacitors during BTS. Finally, the extracted copper diffusivities in dielectric materials by numerical analysis, conduction modes by IV measurement, and time-to-failure (TTF) characteristics by TDDB measurement, two-stage model to describe the copper migration in dielectric materials was suggested.

MEMS Metallization

Today crystalline silicon is the dominant material for MEMS fabrication. Its usage is not limited to act as the base plate but as the functional film or component too. The electrical resistivity of crystalline silicon can be varied in a wide range (0.01 up to 1000 Ohmcm) offering a large flexibility as MEMS material. However, from an application and technology point of view in certain cases metal films are to be used. For example for RF MEMS a resistivity as low as possible is desired in order to minimize electrical losses. It is known that a resistivity of a few 10−7 Ohmcm meet this requirement. Furthermore light reflection from MEMS components can also be increased by metal coating of surfaces. Several signals for signal transmitting offer other application fields; e.g. thermoelectrical, thermal-mechanical (bimorph) and magnetoelectrical transducers. Further fields for metal application are given by technology. The galvaniforming process within the LIGA technology represents a powerful method for shaping material into any form, even if it is difficult to etch. For mass fabrication by using bulk technology nowadays metal is often used as an electrode and contact pad material. In this case the requirements are for instance: good adhesion, low thermal mismatch to adjacent films (substrate) and high long-term stability (reliability, migration). This is quite comparable to IC fabrication. Surface micromachining by sacrificial layer etching underneath metal films as known from RF devices and laminated post CMOS MEMS illustrates much more challenges with respect to the mechanical properties. Thin film stress, yield strength, hardness and Young's modulus are critical issues. Although structure bending can be minimized by stress compensation, stress hysteresis due to relaxation can influence reliability and long-term behaviour deeply. Thus even metal surrounded crystalline silicon core structures like SCREAM devices indicate strong temperature dependence. On the other hand it is shown that metal based devices can offer excellent reliability even through continuous research (TI’s Digital Mirror Device). Data as published recently indicate that problems like hinge fatigue, hinge memory, temperature and light influence can be solved by material and technology adaptation. Metal based fixtures for the fabrication of highly capacitive isolated anchor structures are proven to be stable enough for its application within certain MEMS. Further challenges for MEMS metallization within special applications are given when the operation temperature is increased up to 400 degree C. Thus the interconnect system as well as the whole packaging concept has to be adapted. The huge number of possible interactions within and between several materials of the functional parts at elevated temperatures are critical. Nevertheless, metallization concepts exists and have been verified even at the harsh atmosphere of a car exhaust and a surrounding temperature up to 400 degree C.

Chlorine-based Reactive Ion Etching Process to Pattern Platinum for MEMS Applications

In MEMS applications, chlorine-based Reactive Ion Etch (RIE) processes are needed to deposit, pattern and remove low loss RF transmission lines within a MEMS process flow. Various combinations of chlorine-based gases were tested to find the optimum gas mixture for RIE. A mixture ratio of 0.25 of pure chlorine to argon and 100-150 Watts of RF microwave power were
found to be optimum conditions for the RIE of platinum metal. The addition of argon gas to chlorine was found to contribute to the anisotropic etch of platinum, obtaining vertical side-wall patterns. A simple model of the platinum etching mechanism is proposed. Following the plasma enhanced formation of platinum and chlorine ions, volatile products of platinum chlorides were formed and washed away. The results of our RIE process, using our gas mixture of pure chlorine and argon, micrometer-sized platinum patterns with vertical side-walls were fabricated. Currently we are investigating the chemistry behind this etching process for platinum using Micro-Auger analysis. Results of this work will be presented.

2:15 PM F8.3 Silver Metalization with Reactively Sputtered Tin Diffusion Barrier Films. Liming Guo1, Ch. Linsmeier2, Juergen Gostecner3, A. Witner2, Rainer Emling1, Walter Hansch2 and Doris Schmitt-Landsiedel2.
1 Technical University, Munich, Germany; 2EURATOM Association, Max-Planck-Institut f. Plasmaaphysik, Garching b. Munich, Germany.

As devices continuously shrink in ultra-large-scale integration (ULSI), the RC delay of the interconnection system becomes one of the most critical limitations on IC performance. Silver is being considered by many as the next metallization choice for advanced interconnects and has also received attention as a potential interconnection in the large area TFT/LCDs because of its lowest resistivity and high electromigration resistance. No chemical reactions occurring at a Ag/Si interface, however, adhesion of silver to Si or SiO2 is poor. Ag also diffuses rapidly in silicon to degrades the devices. This report describes production and characterization of titanium nitride (TiN) as a diffusion barrier for silver (Ag) metallizations. RF reactively sputtered TiN films with Ar/N2 ratio of 10/5% ccm and the barrier thickness of 12 nm and covered by 200 nm Ag were deposited. The thermal stability of Ag/TiN metallizations on Si, as-deposited and after annealing at 350-550 °C, was investigated with sheet resistance measurement, X-ray diffraction (XRD), focused ion beam-scanning electron microscopy (FIB-SEM), atomic force microscopy (AFM) and X-ray photoelectron spectroscopy (XPS). The change of sheet resistance was observed after annealing at 600 °C, but an abrupt rise appeared at 650 °C. After an annealing of an Ag/TiN/Si sample at 650 °C, an oxygen concentration with the result of XPS was found because of the slight oxidation during the high temperature annealing. However, there is no evidence of Ag diffusion through the TiN diffusion barrier. The work will be presented.

3:00 PM F8.4 Electrical Behavior of Nano-Scaled Interconnects. Manfred Engelhardt, Gunther Schindler, Werner Steinhoegl, Gernot Steinlebener and Martin Traving; Corporate Research, Infineon Technologies, Munich, Germany.

Sub-lithographic damascene copper lines were fabricated to investigate already today the physical phenomena of metallic conductors in the metallization scheme of chip generations which are believed to be in production 10 years from now and later. Using standard manufacturing processes and state-of-the-art process tools, including standard lithography tools, narrow copper lines were fabricated at the expense of a relaxed pitch by use of a removable spacer technique. These copper nano interconnects were passivated and subjected to electrical measurements. Our results show that continuous down scaling to increase device performance will result in an unfavourable increase of the electrical resistivity of copper in state-of-the-art interconnects. As a consequence, RC delays associated with interconnects will gain increasing importance on the overall performance of future highly integrated circuits. Electrical measurements over a wide range of temperatures down to cryogenic temperatures reveal the limited potential of cooling to reduce resistivity of conductors as lateral dimensions will be shrunk down to the sub-100nm regime. Electromigration life times of sub-100nm copper lines embedded in oxide were found to be comparable with those obtained for similar structures fabricated with today's feature sizes. By down scaling of copper diffusion barriers in damascene trenches, barrier functionality was demonstrated after high temperature anneals and excessive bias-temperature stress tests for films meeting the end-of-roadmap thickness requirements. An analysis of the results of leakage current measurements at very high electric fields applied between neighboring damascene lines suggests that the conduction mechanism in the intermetal dielectric is Frankel-Poole type rather than Schottky emission.


The resistivity of Cu interconnects increases as the wire cross section approaches the electronic mean free path for scattering. 40 nm in copper. This rise is attributed to the gradually higher contributions from surface scattering as function of decreasing cross section due to the wave nature of electrons. Other contributors to the rise in resistivity include grain boundary and surface roughness scattering. This study seeks to correlate the electronic scattering in a wire with key micro-and nanostructural features in order to isolate the individual contributions of each of these phenomena. Accordingly, relatively wide copper lines were patterned by damascene processing into 900, 320 and 240 nm-wide electrical test structures embedded in silicon dioxide. In these trenches, 10 or 20 nm-thick TaN diffusion barriers were first deposited by either physical vapor deposition (PVD) or atomic layer deposition (ALD). The trenches were then filled with 400 nm PVD Cu and the excess Cu removed by mechanical polishing using different Ag3O2 particle size to modify surface roughness. Alternatively, narrower copper test structures (100, 80, and 40 nm) were fabricated by a 2-step lift-off process. In the first step, electron beam lithography was used to pattern 120 nm-thick PMMA photoresist to define the ultra-fine Cu lines and the 3-micron wide trenches, PVD Cu, 40nm thick, deposited on the patterned resist and, standard lift-off procedures were used to remove the PMMA and leave the copper lines on the oxide substrate. A second lift-off process employed standard optical lithography to define the 150, 50 microns square contact pads for electrical testing of the lines. The geometry and surface morphology of the resulting Cu lines were measured by focused ion beam scanning electron microscopy (FIB-SEM) equipped with an electron back-scattered diffraction (EBSD) detector for determining local orientation of grains as small as 10 nm. Surface roughness was measured by atomic force microscopy (AFM) and resistance was measured by probe contact and multi-meter. While it is not surprising that the measured resistivity of Cu wires increases as the wire width decreases, additional results demonstrate that surface roughness and local grain orientation can also play a significant role in the increase in resistivity as well.

3:45 PM F8.6 Kinetics and Adhesion Enhancement for Cu Metallization in Supercritical Carbon Dioxide. Yinfeng Zong and James J. Watkins; Chemical Engineering, University of Massachusetts Amherst, Amherst, Massachusetts.

Copper is the material of choice for advanced interconnects due to its low electrical resistance and superior electromigration resistance. However, as the device size shrinks, the difficulty of filling of high aspect ratio features increases. Supercritical Fluid Deposition (SFD) is a promising hybrid technique for single step conformal metal deposition that is extendable to sub 45 nm device structures. Here we report a kinetic study of Cu SFD using Bis(2,2,4,4-tetramethylcyclopentene-2,4,5-dioate) Cu(II) [Cu(TMOD)]2 as the precursor. Film deposition rates in the temperature range of 150 °C to 300 °C as a function of the relevant experimental parameters including precursor and H2 concentration will be reported. The implication of these results for mechanistic pathways for Cu deposition in CO2 will be discussed. We also report a novel adhesion enhancement of Cu films deposited from CO2 onto current and potential barrier systems. In particular, the efficacy of a sacrificial adhesion promoting layer is demonstrated. The surface modification produces strongly adherent Cu films as evidenced by scribe tape testing. The films and interfaces are characterized by x-ray photoelectron spectroscopy depth profiling, field emission scanning electron microscopy, spectroscopic ellipsometry, atomic force microscopy and four point probe measurements.

4:00 PM F8.7 Microscopic Process and Driving Force for Room-temperature Recrystallization in Cu Thin Films. Makoto Wada and Junichi Koike; Dept. of Materials Science, Tohoku University, Sendai 980-0877, Japan.

Cu thin films undergo microstructure change at room temperature, known as room temperature recrystallization. Its microscopic mechanism and effects on the final microstructure after heat treatment are not well understood. A driving force is also in controversy. In this work, we investigated the microscopic mechanism and effects on the heat-treated textured in electroplated Cu thin films. A driving force was investigated in sputtered Cu thin films. The recrystallization process was monitored by x-ray diffraction, nanindentation,
scanning electron microscopy with electron backscattering diffraction. As-plated films had a random texture and was highly strained. After three hours at RT, strain-free grains appeared. Each neighboring grain had a twin orientation relationship. Recrystallization was completed after 10 hours and more than 60% of recrystallized grain boundaries were coherent (111) twin interfaces. When the as-plated film and RT-recrystallized film were heated to 725°C, no difference was found in the heat-treated microstructure. This was because the as-deposited film underwent the same microstructure change as in the RT-recrystallized film during initial portion of heating at about 100°C. Thus the both films had the same microstructure before grain growth occurred at higher temperatures. A driving force was investigated by using sputtered films. Two types of films were prepared, one having a random texture and another having a <111> texture. Grain size of the both films were nearly the same, eliminating the proposed possibility of grain boundary energy as a major driving force. The use of sputtered film also eliminated proposed influence of chemical impurities that would otherwise be present from an electroplating solution. RT recrystallization was observed in the random film but not in the <111> film. XRD peak position indicated that both films were initially highly strained to a similar magnitude. Strain relaxation was observed only in the random film associated with the RT recrystallization. On the other hand, peak width was much larger in the random film than in the <111> film. This indicated that the strain variation among grains is larger in the random film than in the <111> film. The obtained results suggested a major driving force to be a gradient of strain energy density.

4:15 PM F8-8
A Study of Dilute Cu Alloys for Dual-Damascene Interconnect Applications, C. Hutchison1, A. Bhanap1, M. Pinter2, K. Scholer3, N. Truong4, R. Prater1 and E. Lee1;

In an effort to identify potential candidate alloys with reduced electro- and stress-migration for Cu dual damascene applications, 6N Cu and Cu alloys with 0.3 at. % of Ag, Al, Sn, Ti, and 1.3 at. % Mg were evaluated. Targets were made in the Applied Materials ENDURA® MPF configuration and films were prepared by depositing on a TaN/Ta barrier layer in the ENDURA. Alloying addition refined target grain size and increased hardness. One notable finding was that the grain refinement resulted in improved deposition yield. Alloying elements increased electrical resistivity and decreased thermal conductivity. Ti increased electrical resistivity most and Ag least. However, there was no significant difference in sputtering performance. All Cu seeds showed predominantly <111> orientation regardless of composition, but the electrochemically deposited Cu film deviated from complete <111> orientation by 10% to 44%. AFM examination revealed that deposited film grain size was refined with alloying addition, 6N Cu (110 nm), CuAl (115 nm), CuTi (86 nm), CuSn (57 nm), CuAg (25 nm). Ti and Al were found to retard corrosion most upon exposure to moisture by forming a passivating layer. SIMS analysis showed that solute atoms diffused readily through electroplated Cu at 400°C. Sn and Ag have the fastest diffusing species. Alloying addition imparted little affect on the electrical resistivity of plated Cu except with Ti and Sn in blanket films. All alloyed seed layers showed good adherence to Ta barrier. For test structures, 6N Cu seed rendered the lowest line resistance and CuTi the highest. There was no discernable difference in the line to line leakage current for all alloys. This paper also discusses the strengths and weaknesses of each alloy and suggests potential candidate alloys for future interconnect conducting materials.

4:45 PM F8-10
The initial nucleation behavior during Al, Cu, W-CVD on Barrier metal layers, Yukihiro Shimogaki1, Tomohisa Ino2, Masakazu Sugiyama3, Takeshi Momose2, Young Sok Kim1, Takeshi Tsujiura2, Yuya Kajikawa2, Suguru Noda2 and Hiroshi Komiyama2;
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The ever growing shrinkage of ULSI devices requires nano-meter level ultra thin metal films with smooth surface morphologies and good adhesion onto the under layer in multi level interconnects. The high aspect ratio trenches or holes also require CVD process to deposit metal thin films, like Cu and W onto barrier layer. We have investigated the initial nucleation behavior of Al, Cu and W-CVD using laser light reflection method. TiN thin films prepared by PVD or CVD were used for underlayer of Al, Cu, and W-CVD. Ta thin films were also used as under layer for Cu-CVD. The incubation period, in which no nuclei were observed on the surface, was easily identified with this technique. The surface chemical compositions during the incubation period was analysed by XPS and micro-AES methods. We found that several monolayers of adsorbates exists on the barrier layer during the incubation period. When this adsorbates exceeds certain amount, small nuclei in the order of 10nm were formed. The effects of preparation method and pretreatment method of barrier layer onto the nucleation behavior will be discussed.