SYMPOSIUM J

Silicon Carbide—Materials, Processing, and Devices

April 14 - 15, 2004

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* Invited paper
An overview of SiC Power Devices will be provided. Progress in SiC Schottky diodes (600 V, 1200 V), SiC PIN diodes, SiC MOSFETs, SiC BJTs and Thyristors will be described. SiC MOSFETs, SiC BJTs and Thyristors have already been commercialized. The next step of inserting these devices in Si IGBT modules is happening now. Emphasis will be placed on the problems and issues at the SiC device/process interface which need to be urgently addressed such as the roughness created during the implant anneals, reliability of the gate oxide under positive and negative bias, low current gain of the BJTs, forward voltage instability in the pn junctions etc. Overcoming these issues in the near future will be critical to the successful commercialization of SiC devices.

8:00 AM J1.2 Doping-Induced Strain and Relaxation of Al-doped 4H-SiC Homo-Epitaxial Layers, Sung Wook Han¹, HunJung Chung², Marek Skowronski¹ and Joseph Sunakker²; Carnegie Mellon University, Pittsburgh, Pennsylvania. ¹Cree, Inc, Durham, Pennsylvania.

Aluminum-doped 4H-SiC epilayers with Al concentrations in the 7×10¹⁸ - 2×10²⁰ cm⁻³ range were deposited on off-axis (0001) wafers by chemical vapor deposition method and analyzed using high resolution x-ray diffraction, transmission electron microscopy, and Raman scattering. X-ray rocking curves of (0008) reflection revealed two distinct peaks separated along the 2θ axis. The higher 2θ peak was identified as due to Al-doped strained epilayer due to increase of c-lattice parameter with Al-doping. For Al-concentration up to 2×10²⁰ cm⁻³, 10 nm thick layers were fully strained with the a-lattice parameter of the layer matching that of the substrate. The basal planes of the epilayers were tilted in respect to the substrate in the direction of the off-cut. The amount of tilt is consistent with the elastic strain in the epilayer. The layer with highest Al-concentration ([Al]=2×10²⁰ cm⁻³) was partially relaxed. The Full Width at Half Maximum (FWHM) of reflection increased by a factor of approximately two, the c-lattice parameter decreased, while at the same time the a-lattice parameter increased compared to the lattice parameter of the strained epilayer. The threading dislocation density in relaxed layer determined from KOH etching exceeded 10⁶ cm⁻². Since no inclusions has been found in the relaxed region by TEM, we interpret the above changes as due to film relaxation. This assertion agrees with the estimates of the critical layer thickness. This is the first observation of strain relaxation in an epilayer of hexagonal semiconductor.

9:15 AM J1.3 Pressure Dependence of Aluminum Doping in SiC Vapour Phase Epitaxy, Adolf Schoner and Malin Gustafsson; Acreo AB, Kista, Sweden.

The control of the doping incorporation in vapour phase epitaxy (VPE) of SiC is an important issue for the growth of device structures. The doping incorporation in vapour phase epitaxy (VPE) can be controlled through the parameters dopant precursor flow, silicon precursor flow, carbon to silicon (C/Si) ratio in the gas phase, growth temperature, and reactor pressure. In this study we will report on the aluminum incorporation in 4H-SiC and 6H-SiC in dependence on the total pressure in the reactor. The experiments on the pressure dependent aluminum incorporation were done in a VPE reactor of hot wall type equipped with substrate rotation. Hydrogen was the carrier gas, silane and propane were the growth precursors. Trimethylaluminum (TMAI) was the precursor for aluminum doping. To compare the growth at different reactor pressure, parameters like growth temperature, silicon flow, C/Si ratio, and the TMAI flow were kept constant. The reactor pressure was varied in the range 150 mbar to 230 mbar. In addition, epitaxial growth was done with periodic opening and closing of the pressure control valve in the pumping system. The open-close cycle period was about 20 seconds. For comparison, epitaxial growth runs with pressure change were performed for n-type doping with nitrogen. The biggest influence of the reactor pressure on the aluminum incorporation was seen for the medium concentration range (1×10¹⁶ to 1×10¹⁷ cm⁻³). A change in the reactor pressure from 210 mbar to 150 mbar reduced the doping concentration determined from capacitance-voltage (C-V) measurements from about 3×10¹⁶/cm² to 1×10¹⁷/cm². The doping variation divided by the average doping increase with decreasing aluminum concentration and variations of the factors could be around 7 to 9 at concentration below 1×10¹⁶/cm² to 1×10¹⁷/cm². Periodic pressure change resulted in sinus-like depth profiles of the net doping concentration with a variation of the net doping by the factor 3 to 7, depending on the average net doping level. The variation of the net doping can only be explained by a change in the aluminum concentration. The concentration of compensating donors is typically below 1×10¹⁷/cm³ in hot wall VPE reactor cells. Therefore compensating donors are not responsible for the observed variation of the net doping with changing pressure. In addition, a change of the n-type doping concentration for nitrogen doped epilayers grown with periodic pressure change was not measured by C-V characterisation.

9:30 AM J1.4 Ion Implantation and 1 MeV Electron Irradiation of 4H-SiC—Comparative Studies, Predrag Ewarsya¹,², Steven R. Smith¹,², William C Mitchel¹,² and Gary C Parlow¹,²; ¹Air Force Research Laboratory, Wright-Patterson Air Force Base; ²Physics, University of Dayton, Dayton, Ohio.

In silicon carbide based electronic device technology, ion implantation of donor/acceptor ions (N, P, Al, B) is widely used to selectively dope silicon carbide. This is necessary because the thermal diffusion rates of these dopant species in SiC is low at reasonable temperatures (≤1200°C). Ion implantation causes lattice damage and local stoichiometric imbalance. A post ion implantation anneal at high temperature (1000 -17000C) is therefore necessary to repair the damaged lattice and to activate the implanted species. Some implantation induced defects survive the high temperature anneal and these may, especially the deep defects, affect the performance of electronic devices. High energy electron irradiation of silicon carbide produces point defects—vacancies, interstitials, and anti-vacancies. These may form thermally stable complexes such as divacancies (Vsi-Vc). In this work, we compare the defects produced by Ar⁺ implantation in 4H-SiC with those produced by 1 MeV electron irradiation of 4H-SiC. A 4 micron thick nitrogen-doped 4H-SiC epitaxial layers with a doping concentration of 1.5 × 10¹⁵ cm⁻³ was Ar⁺-implanted at 0000C. The energy of the ions was 150 keV and at a dose of 2 × 10¹⁶ cm⁻². Post implantation anneal was carried out at 1000OC for 10 minutes. An n-type 4H-SiC bulk with a doping concentration of 1.5 × 10¹⁵ cm⁻³ was irradiated with 1 MeV electrons at a dose of 0.1 to 6.1 × 10¹⁷ cm⁻². The electron irradiation was carried out at room temperature; the temperature of the sample did not rise above 500 C during irradiation. Both the Ar⁺-implanted and electron irradiated samples were studied with deep level transient spectroscopy (DLTS) and the results compared. After electron irradiation dose of 4.1 × 10¹⁷ cm⁻², three strong peaks at Ec -0.63 eV, Ec -0.81 eV and Ec -0.78 eV were observed. The defect at Ec -0.63 eV is the Z1/Z2 and the defect at Ec -0.78 eV is the so called RD1/2. The concentration of Ec -0.63 eV increases with the electron fluence. This suggests that the ion-implanted defects in this complex. The isochronal annealing of the electron induced defects show that the annealing behavior of these defects may depend on the source of formation. The DLTS measurements of the Ar⁺ 4H-SiC reveal six capacitance peaks. The two most prominent peaks are at Ec -0.74 eV and at Ec -0.81 eV. A photo-DLTS measurements showed that the peak at Ec -0.81 eV shifted to lower temperatures when the sample was illuminated with white light. However, illumination of the electron irradiated sample produced no observable effect.

9:45 AM J1.5 A Robust Process for Ion Implant Annealing of SiC in Low-Pressure Silicate Ambient, Shalaya P. Rooth¹, Stephen E. Saddow¹, Roberta Nipoti², Fabio Bergamin², Yusuf Emirov³, and Anant Agrawal¹; ¹Electrical Engineering, University of South Florida, Tampa, Florida; ²CNR, CNR - Istituto per la Ricerca sulle Energy, Bologna, Italy; ³Cree, Inc, Durham, North Carolina.

High-dose AI implants in n-type epitaxial layers have been successfully annealed at high temperatures without any evidence of step bunching. Anneals were conducted in a silane ambient and at a pressure of 150 Torr. Silane, premixed in UHP Ar, was further diluted in a 6.5% Ar carrier gas and introduced into a CVD reactor where the sample was heated via RF induction. A 30 minute anneal was performed followed by a purge in Ar at which time the RF power was switched off. The samples were then studied via plan view secondary electron microscopy (SEM) and atomic force microscopy (AFM). The resulting surface morphology was step-free and flat. Results of the annealing process and characterization results will be presented along with electrical data relating to the dopant activation and implanted region conductivity.
layers with a reduced micropore density. Hideaki Tachibana, Isaharu Katama, Syunsuke Iizumi, Tatsuya Takemura, Tatsuya Nakamura, Toshiyuki Miyagi, and Kazumasa Iizumi, Yokosuka Research Laboratory, Central Research Institute of Electric Power Industry, 2-6-1 Nagasaka, Yokosuka, Kanagawa 240-0196, Japan.

The growth techniques of thick SiC epitaxial layers with a reduced micropore density have been developed using a vertical hot-wall CVD reactor with a lower susceptor configuration. Micropore closing by growing an epitaxial layer on low C/Si ratio samples is possible with a nearly 100% probability for 4H-SiC (0001) and (000-1) substrates.片刻cut-off-cuts-favor either <11-20> or <11-00> directions. Growth of low-doped and thick SiC epitaxial layers is also possible in the reactor with high growth rates of 15-20 μm/h achieving a small roughness. A 210-μm-thick 4H-SiC epilayer with a doping concentration of 9x10^15 cm^-2 demonstrated 14.4 kV blocking performance for a 1 mm thick Ni-Schottky barrier diode with a low leakage current density. Growth of epitaxial layers on (000-1) substrates with low doping at mid 10^15 cm^-2 and a low-epi-induced defect density was also demonstrated. Dislocations and stacking faults in epitaxials grown on substrates off-oriented toward different directions and substrates oriented different faces were investigated by reflection-synchrotron x-ray topography using a monochromator, KOH etching, and photoluminescence mapping. The character and densities of basal plane dislocations and in-grown stacking faults were compared for the different off-cut directions. The carrier lifetime of 4H-SiC epilayers was evaluated by time-resolved photoluminescence and microwave-detectected photoductive decay. A long carrier lifetime of 1.4 μs at room temperature and 6.5 μs at 500 K was measured from a sample, while a large sample-to-sample variation was observed. The deep centers, impurities and dislocations were investigated to determine the lifetime killer of the epitaxial layers, and we found a correlation between carrier lifetime, and T_{1/2} and EL\textsubscript{HT} centers.

11:00 AM J2.2
Epitaxial Growth of 3C-SiC on T-shape columnar Si Substrate. Shigehiro Nishino, Akiro Shoji, Taro Nishiguchi and Satoru Ohashi, Electronics and Information Science, Kyoto Institute of Technology, Kyoto, Kyoto, Japan.

Cubic SiC is a suitable semiconductor material for high temperature, high power and high frequency electronic devices, because of its wide bandgap, high electron mobility and high saturation electron drift velocity. The usage of Si substrates has the advantage of wide area substrates for the growth of 3C-SiC layers. However, a large mismatch between 3C-SiC and Si has caused the generation of various defects at the SiC/Si interface. Lateral epitaxial overgrowth (LEO) of 3C-SiC on Si substrates has been reported to reduce the defect density. In this report, epitaxial growth of 3C-SiC on (100) Si and (111) Si substrates has been investigated to reduce interfacial defects. Epitaxial growth of 3C-SiC on the patterned seed 3C-SiC was performed by CVD using hexamethylldisilane (HMDS) as a source gas. Various patterned Si substrates were prepared. We employed a new approach for the epitaxial growth supported by conventional RIE and T-shape pattern was created on the Si substrate. Seed 3C-SiC layers were deposited on 3C-SiC on (100) Si and (111)Si. Top surface of T-shape pattern consists of 1 micron thick, 30 micron wide 3C-SiC and 50 micron wide 3C-SiC by seed supported by Si substrate. Epitaxial growth of 3C-SiC was carried out as following three steps. First step is in situ etching of the substrate. Second process is deep centers, impurities and dislocations were investigated to determine the lifetime killer of the epitaxial layers, and we found a correlation between carrier lifetime, and T_{1/2} and EL\textsubscript{HT} centers.

11:15 AM J2.3
Dry Thermal Oxidation of SiC: Modelization and Elemental Composition of the Interface. Fernando Chiarello Stedile, I. Radkic, B. C Ferrero, J. Bavaresco, E. M Commi, L C Goedtel, I. R Baumov and R M C de Almeida, Instituto de Quimica, UFRGS, Porto Alegre, RS, Brazil; Instituto de Fisica, UFRGS, Porto Alegre, RS, Brazil.

We propose a model based on reaction diffusion equations to describe the oxidation of silicon carbide in dry O\textsubscript{2} and we present experimental evidences of the SiO\textsubscript{2}/SiC interface elemental composition using oxygen isotopic tracing. In the model we take into account several experimental evidences and some hypotheses completely considered, since it has been experimentally verified that oxidation kinetics curves depend on the face exposed to the oxidant atmosphere: C-face, Si-face, or (1120)-face. After oxidation is completed, we find an amorphous SiO\textsubscript{2} film on c-SiC, with C located mainly near the SiO\textsubscript{2}/SiC interface; and iii) C atoms concentrations in SiC bulk and SiO\textsubscript{2} are different. Reaction diffusion equations are proposed in one dimension, taken as normal to the sample surface, where the variables are the local concentrations of C, O, and Si. The model geometry is introduced as initial condition. Reactions between the diffusing and fixed species are considered. The results of the model show that different kinetics curves may be collapsed by adequate scaling to fit experimental data. We will discuss the effect of the temperature of the second oxidation step and the role of thscaleneous species (mainly CO) formed during oxidation were also investigated. Besides, the presence of C and/or Si are also needed to complete stoichiometry of the dielectric film close to the interface.

1:30 PM J3.1
Charge Controlled Silicon Carbide Switching Devices. Peter Friedrichs, SICED GmbH & Co. KG, Erlangen, Bavaria, Germany.

Silicon carbide power devices are believed to revolutionize the power semiconductor business in the near decade. A first step was realized by the commercial availability of SiC Schottky barrier diodes from Infineon and Cree in 2002. Looking into the near future, the following logical step in the device chain should be a SiC switching device. The perspectives range from high voltage applications in energy systems down to the huge market for low voltage power switches, where even in the blocking voltage range below 100V SiC is believed to be one
potential candidate for fulfilling the increasing demands on power density. Clearly this development should be empowered by a high volume production which at the moment rather visible in the blocking voltage range around 1000 V or even down to 600 V for applications where charge controlled silicon devices are not suited (hard switching, high frequency bridge topologies with free-wheeling functions e.g.). But if one succeeds in developing new dielectric materials, blocking voltages above 3 kV will be available as a next generation of SiC switches. The decision which type of device can play a vanguard role is not straightforward to decide. Facing the today’s volume numbers, change of voltage controlled device structures are clearly favored due to their powerless control and the unique compatibility with most of the driving circuits available at the market. Thus, the silicon carbide power MOSFET was for a long period developed and tested, however, without neglecting the necessity of stability and channel conductivity issue the availability at the market will take place most probably sooner in 2008. As an alternative the silicon carbide JFET silicon MOSFET combination was developed at SiCED. Several experiments which make the device more attractive for the customer. It will be shown which factors drive this optimization and how they can be implemented.

The result is a device which behaves for the user more and more like a classical MOSFET with respect to the input as well as the output characteristic. Although the primary target for this devices is the >1000 V blocking voltage range, it will be discussed how the important 600 V power switch market can be accessible for SiC power devices too. With respect to high blocking voltages two concepts were developed by SiCED. Firstly a stacked switch based on the JFET technology was introduced which behaves like a cascode but with blocking voltages of up to 2.5 kV. As a second concept switch called BIFET was developed showing a promising performance especially for blocking voltages above 3 kV. The presentation will give an overview about the developments of SiC power switches at SiCED, in addition some application examples as drivers for SiC power switch development will be sketched. Finally, an outlook to near and long term perspectives for SiC power switches will be given.

2:00 PM J3.2

In this work, the influence of SiO2 and Si3N4 passivation treatments suppress the trapping effects at the surface improving both DC and RF performances. Recent progress in SiC growth technology has resulted in high purity semi-insulating substrates, with a significant reduction in interface traps density 10^{10} cm^{-2} eV^{-1} has been obtained at 160 MV/cm. [1] A. Perez et al. Proc. of ICSCRM 2003 (Lyon).

1:25 PM J3.2

The Effects of Surface Passivation Treatments on Large Signal Characteristics of SiC MESFETs in Class A and Class B Operations. Ho-Young Cha1, Y C Choi1, Lester F Eastman3, A O Konstantinov2, C H Harris5, P Ericsson4 and Michael G Spencer1

High breakdown field and high saturation velocity coupled with high thermal conductivity make SiC very attractive for high power microwave applications. To date, SiC MESFETs have suffered from a current instability problem due to trapping in the substrate and at the surface. In wide bandgap semiconductors, the trapping/detraping is a slow process which causes degradation of both DC and RF performances. Recent progress in SiC growth technology has resulted in high purity semi-insulating substrates, with dramatically reduced Vanadium content. Using better semi-insulating substrates should result in improved device performance.

Nevertheless, the surface issue cannot be managed completely by growth techniques alone. Instead, it is dominated by the fabrication process, and can be mitigated considerably by using surface passivation. In this work, the influence of SiO2 and Si3N4 passivation treatments was investigated by comparing electrical characteristics before and after passivation. Both SiO2 (two different types of SiO2) and Si3N4 films were deposited using a PECVD system. Regardless of passivation type, DC current instability was suppressed dramatically, and the breakdown voltage was increased significantly. The improvement of RF performance did depend on passivation type and operation conditions. CW RF performances in both class A and B operations were measured before and after passivation. Among different passivation treatments, Si3N4 results in the best RF performance, especially in class B operation where the power added efficiency increased from 30% up to 50%. After passivation treatments, the output power improved to equal the theoretical value deduced from the DC characteristics. The enhancement of output power has a correlation with the suppression of DC current instability, which can be explained by a reduction in trapping effects at the surface after passivation. The fact that the improvement of RF performance was more pronounced in class B operation suggests that the trapping effects would be more apparent in class B than in class A operation before passivation. In class B operation, the gate bias is close to the pinch-off, which is a high reverse bias condition in the Schottky contact between the gate metal and the semiconductor. A high reverse bias applied to the barrier increases the field in the junction and thus increases the probability for an electron to tunnel from the metal into the semiconductor. A higher number of injected electrons from the gate increases the probability of trapping. It is clear that the passivation treatments suppress the trapping effects at the surface improving both DC and RF performances. Passivation results using an MBE grown AlN layer are expected by the time of this conference.

2:30 PM J3.3

Laser Direct Write and Gas Immersion Laser Doping for Formation of SiC Diodes. Islam Salama2, Nathaniel R Quick1 and Arsvinda Kar2

Among compound semiconductors, only SiC can be thermally oxidized to grow insulating SiO2 layers. The use of amorphous, thermally grown SiO2 as a gate dielectric offers several key advantages in CMOS processing, including a thermodynamic and electrical stable interface as well as superior electrical isolation properties. Nevertheless, the high density of defects encountered at the SiC/SiO2 interface represents a major obstacle in the successful fabrication of MOS electronic devices. In fact, the inversion channel mobility of SiC 4H-SiC nMOSFETs is far below the predicted value from their bulk electron mobility in the presence of nonuniform, amorphous dielectrics as gate material, with a higher dielectric constant, can be considered as a valuable alternative in order to enhance the channel conduction and reduce the oxide degradation due to current injection. We propose the use of deposited amorphous SiO2 and Si3N4 substrates in an alternative dielectric in metal-insulator-semiconductor structures. In a previous work [1], the feasibility of this insulator was demonstrated on 4H-SiC substrates. Ta2Si target films of 150 Å and 400 Å thickness have been deposited by direct sputtering after a SNC cleaning process. X-ray diffraction analysis showed no specific peaks of Ta, Si or Ta2O5, indicating that the as-deposited films were amorphous. Following the deposition the samples were oxidized in dry environment at 930°C and 850°C during 60 min. Using X-ray diffraction analysis, Ta2O5 peaks are clearly evidenced implying an orthorhombic Ta2O5 [1 1 0] preferential orientation. Thereby, no peaks corresponding to Ta, Si or Ta2O5 have been observed. MIS capacitors were fabricated with the insulator previously deposited using Al as permanent metallization using a mercury probe. An effective dielectric constant of 16 has been achieved for the Ta2Si deposited and oxidized insulating films derived from C-V measurements along with SIMS depth profiling analysis. This result has been fitted using a simple physical model. From C-V measurements, the interface state density spectra of the different samples has been derived by means of the Derman-McIntyre equation. The samples oxidized at 930°C, an interface traps density of 10^{12} cm^{-2} eV^{-1} has been obtained at Ec-EF = 0.2 eV. Thus, a similar Dit to thermal non-oxidized SiC/SiO2 insulators has been inferred. Nevertheless, for the samples oxidized at 850°C a significant reduction in interface traps density 10^{11} cm^{-2} eV^{-1} has been obtained at Ec-EF = 0.2 eV. The average breakdown field has been extracted from I-V measurements. For the 150 Å Ta2Si 950°C oxidized sample, a critical breakdown field of 200 kV/cm has been required. In spite of that, considering the equivalent thickness of SiO2 that would be required to achieve the same capacitance density, the critical breakdown field would be of 160 MV/cm. [1] A. Perez et al. Proc. of ICSCRM 2003 (Lyon).
high frequency switching and sensing applications.

2:45 PM 13.5
Improvement of GaN epitaxial growth by using SiC buffer layers with skin layer on. Marina Mynbaeva and Alla Sitnikova; Ioffe Physico-Technical Institute, St.-Petersburg, Russian Federation.

It has been shown that porous silicon carbide (PSC) is an effective buffer for heteroepitaxy of GaN, as it allows one to reduce the density of point defects and dislocations penetrating from the substrate into the epitaxial layer [1]. Another application for PSC is using it as a buffer layer for heteroepitaxy of GaN on SiC. It is known that main cause of defect formation in heteroepitaxial layers is stress due to lattice mismatch and thermal stress due to thermal expansion coefficient mismatch. But this type of stress causes one type of defects to penetrate from the heterosubstrate into the epitaxial layer. On the other hand, relaxation of these stresses is accompanied by formation of dislocations in the epitaxial layer. In this work, we present the data showing that using PSC layers it is possible to reduce the effect of mismatch in GaN/SiC heterostructures. By employing PSC buffer layers, substantial reduction in structural defect concentration in GaN layers was achieved. Growth experiments were performed using PSC buffer layers with various thickness and morphology of porous structure. The important role of the skin layer covering porous structure will be demonstrated. 1. S. Mynbaeva, V. Chistyakova, et al., J. Cryst. Growth 281, 118 (2005).

SESSION 14: Sensors
Chair: P. Gouma
Wednesday Afternoon, April 14, 2004
Room 2009 (Moscone West)

3:30 PM 13.1
SiC a Sensor Material for Extreme Environment. Anita Lloyd Spetz, IFM, Linkoping University, Linkoping, Sweden.

The excellent properties of silicon carbide have paved the way for commercially available Schottky devices for high power from Infineon Technologies in Munich, Germany and UV flame detectors from General Electric in the US [1,2]. The high band gap preserves the semiconducting feature of the material even at 1000°C and makes it suitable for high temperature sensors and electronics. The high melting point and chemical inertness makes it especially suitable for harsh and corrosive environments, and also as an insulator material. A metal insulator silicon carbide field effect transistor, MISiCFET, with buried source, drain and channel region has been developed [3]. It functions as a gas sensor by the application of catalytic gate metals, such as Pt and Ir. The voltage at a constant current is the sensor signal, and the size of the gas response can be controlled by an applied negative bias voltage on the substrate. The MISiCFET sensors have successfully been tested in several applications. For instance, a Catalyst Reduction, SCR, of NOx by NH3 in the catalytic converter in diesel exhausts can be regulated by an NH3 sensitive MISiCFET sensor operated at 300°C. A cold start sensor, which can be operated at 550°C already a few seconds after start of the engine, will reduce emissions substantially. The combustion process in a boiler can be controlled by a MISiCFET sensor array measuring online in the flue gases. These applications require very long term stable and, especially in the case with the NH3 sensor, very selective and sensitive sensors. Nanoparticles of e.g. Au1203 impregnated with Pt or Ir is developed as the gate material for the MISiCFET devices. This will provide a very large amount of active sites for the gas response and hopefully a very stable metal / insulator interface. The transport mechanism on the spectral region and on the applied bias voltage is explained taking into account the experimental data. Recent Major Advances in SiC, Jim Choyke, Hirohiyuki MatsuTani, Gerhard Pensl, Springer, Berlin, chapter 36, pp. 879-906.

4:00 PM 13.2
Colour image sensor based on amorphous silicon carbide p-i-n structures. Paula Louro, M. Fernandes, A. Fontal, A. Macaroco, M. Vieira, N. Carvalho and G. Lavareda; DEETC, ISEL, Lisboa, Portugal. [4] The devices developed by ACREO, Stockholm, Sweden, is a short channel MISiCFET device, and the baseline and performance devices on a micro-hot plate will be discussed. [1] 2. M. Fernandes, A. Fontal, A. Macaroco, M. Vieira, N. Carvalho and G. Lavareda. Photodiodes based on p-i-n amorphous silicon carbide structures have several applications in the field of photoactive devices. In this work we report its use as a colour image sensor. These structures exhibit a strong dependence of the spectral response on the applied voltage, which means that the spectral sensitivity can be electronically tuned. We used several p-i-n structures based on amorphous silicon and amorphous silicon carbide produced by PE-CVD with the configuration glass/ITO/p-SiC:H/i(a-Si:H)/n(a-SiC:H)/Al/ITO. All have the same intrinsic layer and in the doped layers we changed the resistivity through the addition of methane to the doping gas. For the optical characterisation of the devices we measured the (V) characteristics under daylight-like illumination (AM1.5) and with interference filters we also varied the photon flux. Combining the signal information at different voltages a colour image can be acquired. The dependence of the transport mechanism on the applied bias voltage is explained taking into account the experimental data and the results obtained through a detailed numerical simulation based on the ASCA simulator.
the sensing layer and the semiconductor, and the SiC semiconductor. This paper discusses the gas sensing needs of several aerospace applications and the use of SiC-based gas sensors, often in conjunction with other gas sensors, to meet these needs. In particular, this paper will discuss methods being used to tailor the sensor structure for the application. For example, a carbide or oxide intermediate layer can improve the sensor stability at higher temperatures while changing the sensing material decrease the sensitivity to certain hydrocarbons. Most importantly, the approach of using atomically flat SiC to provide an improved and uniform SiC semiconductor with the sensor deposition will be discussed. Examples of the demonstration of SiC gas sensors in aerospace applications will also be given. It is concluded that, while significant progress has been made, the development of SiC gas sensor systems is still at a relatively early level of maturity for some applications.

SESSION 15: Poster Session
Wednesday, April 14, 2004
8:00 PM
Salons 8-9 (Marriott)

15.1 Abstract Withdrawn

15.2 Aluminum-ion implantation into 4H-SiC (11-20) and (0001).
Yuki Negoro, Tsunenobu Kimoto and Hiroyuki Matsuoi, Electronic Science and Engineering, Kyoto University, Kyoto, Japan.

Aluminum-ion (Al⁺) implantation into 4H-SiC (11-20) and (0001) has been investigated (RT). Implantations were carried out at 500°C or room temperature. Post-implantation annealing was performed in an Ar ambient at 1800°C with a graphite cap made from photo-resist. The graphite cap roughening of high-dose Al⁺-implanted (0001), resulting in an excellent flatness with an rms roughness of 1.0 nm. Regarding electrical properties, a sheet resistance of 1.7 kΩ/sq. could be achieved by co-implantation with carbon ions, in the case of RT implantation into (11-20). For 500°C implantation, the lowest sheet resistance of 1.7 kΩ/sq was obtained by increasing the Al⁺ dose up to 6.0 × 10¹⁷ cm⁻². The Hall mobility (hole) differs in (11-20) and (0001). The mobility in (11-20) is 10 cm²/Vs at RT, whereas it is about 3 times higher than that in (0001). The temperature dependence of free hole concentration for each face is extremely weak. Annealing time dependence of sheet resistance, SIMS profile, and surface morphology of Al⁺-implanted 4H-SiC (11-20) and (0001) will be discussed.

15.3 Morphology-controlled synthesis of nanostructured silicon carbide, Xing-Yan Guo and Guo-Qiang Jin, State Key Laboratory of Coal Conversion, Institute of Coal Chemistry, Taiyuan, Shanxi Province, China.

The sol-gel route was employed to synthesize nanostructured silicon carbide materials. In the route, tetraethoxysilane (TEOS) and phenolic resin were used for preparing a binary carbonaceous silicon xerogel, the xerogel precursor was then temperature-programmed heated to about 1250°C and kept at the temperature for 20 hours in an argon flow. Purified β-SIC was obtained by removing excess silica, carbon and other impurities. By controlling different additives in the sol-gel process, we can obtain differently nanostructured SiC materials: (a) SiC whiskers if no additive employed, (b) SiC nanowires under the presence of alumina sol, (c) mesoporous SiC under the presence of a small quantity of nickel nitrate and (d) spherical SiC nanoparticles under the presence of excess nickel nitrate. The different products are indicated by the additives in the sol-gel process results in a self-organization of primary colloidal particles, which usually forms large secondary grains consisting of phenolic resin and embedded silica particles. The self-organization has changed the reaction environment of carothermal reduction, as a result differently morphologic SiC samples can be produced.

15.4 600V 4H-SiC RESURF-type JFET, Satoshi Nakaizumi, Michitomo Iyama, Kazuhiro Fujikawa and Atsushi Ito; Energy and Environmental Technology Research Laboratories, Sumitomo Electric Industries, LTD., Osaka, Japan.

An integrated circuit module with SiC switching devices is promising, because of low loss and high temperature operation, especially in an electric or hybrid automobile. A lateral switching device is suitable for the module from the point of view of system integration. In spite of recent progress, SiC-MOSFETs have still suffered from the low channel mobility and oxide reliability. A RESURF-type JFET is suitable structure as a lateral switching device with the breakdown voltage of above 600 V for an inverter module which drives motors of an electric or hybrid automobile. In this study, 600 V RESURF-type JFETs fabricated by co-implantation with other gas sensors, to meet these needs. In particular, this paper will discuss methods being used to tailor the sensor structure for the application. For example, a carbide or oxide intermediate layer can improve the sensor stability at higher temperatures while changing the sensing material decrease the sensitivity to certain hydrocarbons. Most importantly, the approach of using atomically flat SiC to provide an improved and uniform SiC semiconductor with the sensor deposition will be discussed. Examples of the demonstration of SiC gas sensors in aerospace applications will also be given. It is concluded that, while significant progress has been made, the development of SiC gas sensor systems is still at a relatively early level of maturity for some applications.

15.5 Deep Level Defects in He-implanted 6H-SiC Studied by Deep Level Transient Spectroscopy, Xudong Chen, Department of Physics, The University of Hong Kong, Hong Kong, Hong Kong, China.

Deep level transient spectroscopy (DLTS) was used to study deep level defects in He-implanted n-type epi-6H-SiC samples. Low dose He-implantation (1X10¹¹ cm⁻²) has been employed to keep the as-implanted sample conductive so that studying the annealing behavior of the He-implantation induced defects becomes feasible. Strong DLTS peaks at Ec-0.6/0.5eV and Ec-0.5/0.4eV were observed in the as-implanted sample. The intensities of the Ec-0.6/0.5eV levels increase even with filling pulse widths longer than 10 ms. The electrons captured at these traps were found to depend logarithmically on the duration time of the filling pulse. This indicates that these traps may be related to the charged dislocation defect. The peak can be significantly reduced by annealing the sample at 500°C. For the Ec-0.5eV peak, it anneals at about 300°C. Moreover, Ec-0.35eV and Ec-0.3/0.4eV (E1/E2) deep levels were found to be generated after the He-implanted sample was annealed at 500°C. ACKNOWLEDGEMENT This work is supported by the RGC, HKSAR (No.7089/01P) and CRGC, HKU.

15.6 The interaction of C60 with Si(111) and Co/Si(111), Md. AK Zilani, Hui Xue, Xue-xen Wang and Andrew Thye-shen Wee; Physics, National University of Singapore, Singapore, Singapore.

We report STM (scanning tunneling microscopy) and XPS (X-ray photoelectron spectroscopy) studies of the interaction of C60 on Si(111)-7x7 and Co/Si(111) at different annealing temperatures (room temperature to ~720°C). On Si(111), Si(100) [1], Pt(111) and Ni(110) [2], C60 molecules decompose completely at 500°C, 850°C, 780°C and 490°C, respectively. They form SiC at the interfaces with Si and graphite sheets with Pt and Ni surfaces, the latter surfaces catalyzing the decomposition process. Usually SiC films are grown by chemical vapor deposition at 1300-1500°C. Due to the 22% difference in the thermal expansion coefficients and 20% lattice mismatch between Si and SiC, SiC grows with a high density of defects during high temperature carbonization process. One way to improve the crystallinity of the film and the quality of interface is to reduce the synthesis temperature. Several papers have reported growing SiC at lower temperatures (800-1000°C) using C60 as a precursor on Si(100) and Si(111). One recent study using supersonic C60 beams on Si(111) surface reported SiC formation at 780°C [3]. We have done a comparative study of the thermal decomposition of C60 on Si(111) and Co/Si(111). The C-1s core level XPS peaks show the shift of the carbon peak and formation of SiC. The C60 cage begins to break at ~500°C on Co/Si(111) which is ~250°C lower than in previous reports [4]. The C-C component disappears completely with only the C-Si component remaining at 910°C on Si(111) and 720°C on Co/Si(111). The growth of a small peak at the higher binding energy end of the Si-2p peak confirms SiC formation on both surfaces. Our STM images are in agreement with the XPS results where we see "ball-like" C60 molecules as well as small SiC clusters at 450°C on Co/Si(111) indicating partial decomposition of C60. STM line profiles show that some C60 molecules have opened their cage at 450°C, SiC clusters with thickness of ~25 Å. STM images also show localized SiC reconstructions at 625°C and regular SiC clusters at 720°C on Co/Si(111). We conclude that the carbothermal reduction of C60 cage at significantly lower temperatures, facilitating SiC growth.


of Pt were deposited onto the (≈5 nm) substrates. Electrical measurements characterizing the multilayers were successfully formed on epitaxial SiC substrates. A typical device consisted of 500 nm AIN depositions were carried out by magnetron sputtering. Details of the fabrication, as well as preliminary data on the response to Hydrogen, have been presented. The electrical behavior of these structures is that of a rectifying diode, the forward bias corresponding to positive Pd contact. The sensor response was obtained by monitoring the change in forward bias required to keep a preset constant current as the concentration of Hydrogen in the surrounding flow was being changed. Detailed results will be presented describing the dependence of this bias shift on hydrogen concentration and on flow rate and temperature effects. At fixed flow rate, the response initially increases roughly linearly with concentration, but eventually becomes completely saturated. The magnitude of the response as well as the saturating concentration increase with temperature. The response saturates at 60 ppm at 120 °C, and at 125 ppm at 250 °C. The magnitude of the response also increases with flow rate, up to a flow rate of 500 sccm beyond which it remains constant. In linear region, the magnitude of the response increases by a factor of 6 between 120 and 250 °C, at a flow rate of 250 sccm. At a typical sensitivity of 0.02 V/ppm was obtained, with a detection limit of 1ppm determined by instrumental noise. Reference: J. F. Serina, K.Y.S. Ng, C. Huang, G.W. Auner, L. Rimai, and R. Naik, Appl. Phys. Lett. 79, 3350-3352 (2001).

J5.8 The electrical behavior of Pd/AIN/Semiconductor thin film hydrogen sensing structures, L. Rimai1, E F McCullen2, M. H. Rahman3, Z. Linfeng4, J. S. Thakur5, R. Naik6, G. Newaz7, K. Y. S. Ng8, and G. W. Auner8, 1Department of Electrical and Computer Engineering, Wayne State University, Detroit, Michigan; 2Department of Physics and Astronomy, Wayne State University, Detroit, Michigan; 3Department of Chemical Engineering and Materials Science, Wayne State University, Detroit, Michigan; 4Department of Mechanical Engineering, Wayne State University, Detroit, Michigan.

Earlier work has shown that such structures, either on Si or on SiC substrates respond selectively to small (ppm) concentrations of H2 in the surrounding gas flow, but in different manner. The device on Si substrates behaves as an MIS capacitor with the AIN playing the role of a catalytic electrical contact and 1800 V. The magnitude of this response is in the same order as the shift in the C(V) curve of the Si based device with approximately the same thickness and at the same temperature. It was shown that the response of either type of device can be explained as resulting from the accumulation of positive charges within the AIN but in the vicinity of the heterojunction, with an apparent barrier height in the absence of hydrogen of about 1.5 eV (AIN thickness of 500 Å). In the presence of 100 ppm of hydrogen, at 250 °C this barrier is reduced by about 0.25 V. The magnitude of this response is in the same order as the shift in the C(V) curve of the Si based device with approximately the same thickness and at the same temperature. It will be shown that the response of either type of device can be explained as resulting from the accumulation of positive charges within the AIN but in the vicinity of the heterojunction. The source for these charges are the catalytically dissociated atoms of Hydrogen which diffuse through the Pd and at the interface with the AIN leave the electron behind in the conduction band of the Pd. These charges (protons) set up an additional voltage across the structure thus resulting in the observed shifts. Whether the AIN behaves as a near ideal insulator, or as a semiconductor will depend on the distribution of conduction electrons (and holes) across the layers. These experimental results can be analyzed to obtain information about the valance band offsets, the doping are discussed. Low temperature photoluminescence (LTPL) data will be presented showing the Ti lines in the visible spectrum and the V lines in the near infrared. Luminescence lines associated with other deep centers will also be reported.

J5.10 A kinetic model for doping in silicon and silicon-carbide epitaxy by CVD. Bhuvosh Mehta and Meng Tuo; University of Texas at Arlington, Arlington, Texas.

A kinetic model based on 1) the collision theory of heterogeneous unimolecular elementary reactions, 2) the kinetics of thermal CVD, photo-CVD, and MOCVD. The concept of competitive adsorption is proposed for doping in silicon and silicon-carbide epitaxy by chemical vapor deposition (CVD). The model provides analytical equations to describe carrier concentration as a function of deposition conditions including the growth temperature and the partial pressures of various precursors. The model agrees well with the experimental data for both p-type and n-type doping in silicon epitaxy. It also predicts the carrier concentration as a function of the carbon to silicon ratio in silicon-carbide epitaxy. By assuming the reaction mechanism for a precursor, the model also presents a method to estimate the activation energy for the particular heterogeneous reaction. This model has been successfully applied to describe the kinetics of thermal CVD, photo-CVD, and MOCVD.

J5.11 Formation of Si/SiC Heterostructures for Silicon-based Quantum Devices Using Single CH3SiH3-gas Source Free Jet. Ryota Ohtani, Yoshihumi Ikoma and Teruaki Motooka; Department of Materials Science and Engineering, Kyushu University, Fukuoka, Japan.

Silicon carbide (SiC) can be epitaxially grown on Si(100) substrates and the SiC/Si(100) heterostructure has a large band offset. Therefore, SiC is potentially useful for applications to silicon-based quantum devices. Recently, we successfully formed Si/SiC heterostructures by supersonic free jet CVD, using SiH4 and CH3SiH3 gases. In this study, we have investigated formation of SiC/Si/SiC(100) heterostructures utilizing single gas source, CH3SiH3. CH3SiH3 10% diluted by H2. At first, the substrate temperature was set at 850 °C and a Si layer was grown on Si(100) by irradiation of 18000 free-jet pulses. Then the substrate temperature was reduced at 650 °C and a Si layer was formed on SiC layer by irradiation of 18000 pulses. For growth of the Si layer, CH3SiH3 jets were excited using a tungsten hot filament. Finally, the substrate was heated again at 850 °C and the top SiC layer was grown by irradiation of 18000 pulses. These samples were characterized by using cross-sectional transmission electron microscopy and x-ray photoelectron spectroscopy measurements. It was found that SiC (~5 nm)/Si (~20 nm) multilayers were successfully formed on epitaxial Si layers (~18 nm). Electrical measurements characterizing the SiC/SiC quantum confinement effects are currently under way.

J5.12 SiC power devices improved by fine surface polishing. Yoshitoshi Ohashi1, Akihito Fujita1, Raul Perez2, Dominique Tournaire3, Narcis Mestres3, Hugo Oudin2 and Daniel Turcotte2, 1Power Dept., Centro Nacional de Microeletronica, Cerdanyola, Barcelona, Spain; 2R&D, NOVASIC, Le Bourget du Lac, France.

Surface polishing can be considered as a potential technological process to improve electrical and reliability characteristics of SiC devices. It is already used as surface treatment prior to epitaxy growth on SiC substrates. In this work we take profit of a novel fine polishing process to improve the quality of SiC or Si on SiC implanted Schottky and p/n planar diodes. The mentioned fine polishing process allows to remove a layer thickness of 100nm to 3000nm on the surface of a processed SiC wafer. The impact of this process on the surface properties of the sample is analyzed in this
Boron and nitrogen depth profiles were measured by secondary ion mass spectroscopy. Transmission electron microscopy has been used to determine the structural and electronic properties of implanted layers. Nitrogen concentration profiles remained unchanged after the annealing. Boron atoms showed strong out- and in-diffusion in both studied SiC polytypes. Deep penetrating diffusion tails extending up to 4 μm were observed in samples both implanted with B⁺ and with N⁺. However, the amount of mobile boron atoms, which formed in the tail region, was approximately 4 times less in the co-implanted samples as opposed to samples implanted with B⁺. Boron diffusion parameters in 4H and 6H polytypes have been determined and boron diffusion mechanism has been discussed.

15.15
Porous GaN/SiC templates for epitaxial growth. Marina Mynbaeva¹, Andrei Sarus² and Martin Kubal³; ¹Toffe Physico-Technical Institute, St.-Petersburg, Russian Federation, ²H.H. Wills Physics Laboratory, University of Bristol, Bristol, United Kingdom.

Despite much progress in III-nitride technology, the task of reducing the density of defects caused by mismatch in parameters of III-nitride epitaxial layers and foreign substrates is still on the agenda. One of the ways to reduce the defect density in epitaxially grown material is to use porous buffer layer formed on the substrate surface. Our preliminary results on the growth of GaN-epitaxial layers on porous GaN/SiC structures, obtained on 1x1 cm² samples, showed that porous substrate allows one to improve epitaxial growth of GaN [1]. In this work, we report on the development of porous GaN/SiC templates with 2° in diameter. We show that by selecting optimal formation conditions it is possible to fabricate porous substrate with reduced level of residual strain, as compared to initial GaN/SiC heterostructures. Most remarkable is the fact that to reduce the strain to the minimum possible value, porous structure in GaN/SiC template must be developed not only in the GaN layer, but in the SiC substrate as well. We discuss technology matters related to fabrication of porous templates with such type of structure.

15.16
Laser Direct Write of a Tunable SiC Filter for Sensor Applications. Islam Salama¹, Nathanael Quick² and Aravinda Kar²; ¹AppliCote Associates, LLC, Lake Mary, Florida; ²University of Central Florida, Orlando, Florida.

Laser direct write fabrication of a silicon carbide optical filter with a tunable response in the infrared (IR) regime of the electromagnetic spectrum is presented. Applications rely on the fact that the optical properties of n-type 4H-SiC are controlled by its free carrier concentration. A laser direct write technique is used to fabricate metal-like contacts in situ in n-type 4H-SiC (approximately 5 x 10^19/cm³) substrates generating a conductor-semiconductor-conductor structure without the addition of metal. Application of a biasing voltage, either forward or reverse, between two contacts in this structure affects the optical transmission of the SiC semiconductor. The transmission increases as the magnitude of the applied voltage increases for wavelengths higher than 1500 nm at an applied bias of 5-7 volts. For an applied bias of 9 volts, the transmission increased over the range 2000-3000 nm which is followed by a rapid decay in the transmissivity leading to a maximum value of 2670 nm. The difference between the maximum and minimum values increases with the applied bias. These results indicate that the laser-fabricated SiC conductor-semiconductor-conductor device can act as a tunable optical filter in the infrared regime. The origin of the tunability is related to the free carrier absorption phenomenon, i.e., the free carrier response to the incident electromagnetic field, at the IR wavelength, in the presence of the biasing voltage or the electric field. When the sample is under no external bias the optical transmission at a given photon energy smaller than the bandgap is controlled by both the sub-bandgap transition and free carrier absorption. This tunable filter will select radiation for detection by a Si Schottky diode sensing element fabricated by laser doping and laser metallization.

15.17
Fabrication of SiC microtubes with a villus-like microstructure. Jae-Won Kim¹, Seoung-Soo Lee², Yeon-Gil Jung², Je-Hyun Lee³ and Chang-Yong Jo4; ¹Material Science and Engineering, Changwon National University, Changwon, Kyungnam, South Korea, ²High Temperature Materials Group, Korea Institute of Machinery and Materials, Changwon, Kyungnam, South Korea.

Silicon carbide microtubes were successfully fabricated by reacting between SiO vapors and carbon microfibers. Silicon carbide precursor
was prepared by mixture of Si/ $\text{SiO}_2$. The precursor led to complete conversion of ($\text{SiO}_{2+x}$ + $\text{C}_{\text{solid}}$) into ($\text{SiC}_{\text{solid}}$ + $\text{CO}_{2}$) through overall reaction with high treatment under inert gas flow rate at temperature higher than 1620K. The amount of unreacted carbon was determined by thermogravimetric analysis (TG/DTA), fourier transfer infrared spectroscopy (FTIR) and scanning electron microscopy (SEM). Let 1.3 mm fiber (1 $\text{m}^2$ $\text{g}^{-1}$) was initially converted to high specific surface area SiC microtubes ($50 \times 10^3$ $\text{m}^2$ $\text{g}^{-1}$) after removing of the residual carbon by oxidation. Inner surface of SiC microtubes showed a villus-like microstructure, which consists of sub-micron (20.5mm) sized SiC particles, while outer surface of SiC microtubes was smooth. The smooth inner surface of SiC microtubes transformed into villus-like morphology with increasing sintering temperature. The thickness of villus-like layer in the SiC microtube also increased with increasing sintering temperature.

15.18

Epitaxial Growth of 2 inch 3C-SiC on Si Substrates by Atmospheric Hot Wall CVD, Jilian Zhu, Yi Chen, Yusuke Mukai, Akira Shoji, Satoshi Ohshima and Shigehiro Nishino, Electronics and Information Science, Kyoto Institute of Technology, Kyoto, Japan.

A high mobility, wide bandgap semiconductor, 3C-SiC has great promise. In this paper, we examined to obtain 3C-SiC epilayer on Si substrates using hot-wall CVD furnace and report the use of hexamethyldisilane (HMDS) and propane as reaction gases to grow uniform thickness on (100). Temperature of the susceptor was measured at inside wall of the susceptor by optical pyrometer. The susceptor was surrounded by graphite foam. Temperature of the susceptor was 1700 $^\circ$C at inside wall of the susceptor by optical pyrometer. HCl flow rate for etching was 1.0 - 2.0 sccm. An initial carbonization procedure was performed using 1 sccm propane at 1250 oC for 2-3 minutes. During the growth of SiC at 1300 oC for 1 hour, the flow rate of HMDS was 0.76-1.2 sccm and the flow rate of propane was 0.1-0.5 sccm. The hydrogen carrier gas flow rate was 3-3.5 sccm. Typical growth rate was 3 micron /h. Uniform thick 3C-SiC was obtained. The samples were examined using optical microscopy, SEM and RHEED. Electrical properties are also discussed

15.19

Characterization and Mapping of Crystal Defects in Silicon Carbide, Eijiro T Emhofer 1, Thomas Kerr 1, William T. Ellington 2, Ilya Zwieback 1, Michael Dudley 1, Thomas Anderson 1, John Chen 1, and Carl Johnson 1; 1Wide Bandgap Materials Group, II-VI Inc., Pine Brook, New Jersey; 2Wide Bandgap Materials Group, II-VI Inc., Saxonburg, Pennsylvania; 3Department of Materials Science and Engineering, State University of New York at Stony Brook, Stony Brook, New York.

A method is presented for detecting, counting and mapping dislocations and micropipes in n+, undoped, and semi-insulating Silicon Carbide wafers. The technique is based on etching in molten Potassium Hydroxide (KOH). The polish-etch regime of the etching process has been developed to produce etch pits which allow quick and accurate analysis of the optical contrast. Etch pits from dislocations and micropipes are detected and differentiated by an image processing system that is sensitive to the optical reflection profile of the etch pit. The instrument probes an area of 700 x 700 mm2 and is capable of producing topographic maps showing distribution of dislocation and micropipe densities (MPD). The MPD scan time for 2-inch wafers is less than two hours per wafer. The created MPD maps are in good agreement with the contrast images produced by the Synchrotron White Beam X-Ray Topography.

15.20

The Effect of Doping Concentration and Conductivity Type on Preferential Etching of 4H-SiC by Molten KOH, Ying Gao 1, Zehong Zhang 2, Robert Bondokov 2, Stanislav Soloviev 2 and Tangali Sudarshan 1; 1Bandgap Technologies, Inc., Columbia, South Carolina; 2University of South Carolina, Columbia, South Carolina.

Molten KOH etching of SiC is a simple and effective method for revealing structural defects. However, it has been reported that molten KOH etching is better able to identify specific defects in medium and high-resistivity SiC wafers than in highly doped SiC wafers. This is a more effective defect delineation tool when preferential etching is enhanced compared with isotropic etching. In this work, molten KOH etching was implemented to delineate defects on the n+ 4H-SiC samples with different doping concentrations. The dimensions of the etch pits were compared using Normal Interference Contrast (NDIC) microscope. The etch preference is significantly influenced by both the doping concentration and conductivity type. The preferential etching of Si-face 4H-SiC substrates is n+ < n- < p- < p+. It is concluded that the molten KOH etching process is a combination of a chemical and an electrochemical process, during which the electrostatic etch rate and preferential etching are competitive. Based on the above observations, the n+ 4H-SiC wafer was etched by p-type diffusion of boron followed by molten KOH etching at 600 $^\circ$C for 10 minutes. The results clearly showed three types of distinguishable etch pits corresponding to threading screw, threading edge and basal plane dislocations even in highly doped n+ substrates. In addition, this approach has been used to investigate defect correlation between the 4H-SiC epilayer and substrate.

15.21

Photoluminescence Characterization of Defects Introduced in 4H-SiC During High Energy Proton Irradiation and Their Annealing Behavior, Mi Ahoujja 1, H C Crockert 2, M B Scott 2, Y K Yeo 2 and R B Hengelhofer 2; 1Physics, University of Dayton, Dayton, Ohio; 2Engineering Physics/ ENP, Air Force Institute of Technology, WPAFB, Ohio.

The robust nature of SiC makes it an ideal material in both space-based and high temperature environments where conventional Si and GaAs based devices would fail. However, a clear understanding of how SiC behaves under a radiation environment is required before it is incorporated in devices for space applications. In this paper, we report on the optical properties of defects introduced in epitaxial 4H-SiC by 2 MeV protons using photoluminescence spectroscopy. The concentration, type and energy depth characteristics of the defects present in the optical spectrum of the as-grown samples. Following a proton irradiation, the material is altered and the luminescence of the shallow centers is attenuated almost entirely with the emergence of deeper shallow traps at energies greater than 350 meV below the conduction band. Subsequent high-temperature thermal annealing of the material results in an increase in the emission spectrum at both the near band edge region ($E_g = 3.25$ eV) and between 2.65 and 2.95 eV. Recovery of the characteristic nitrogen-related peaks at the near band edge following high-temperature annealing (TA) is identified, but is not complete at TA $= 1500$ oC. In the deep trap region below 2.06 eV, activation of trap centers with annealing results in a sharp increase in the signal intensity an irradiation damage trap ($2.90$ eV) as well as the associated phonon replicas. Based on previous ion-implantation studies in 4H-SiC, the emergence of the 2.90 eV defect complex and associated phonon replicas may not be related to hydrogen implantation as a result of the proton irradiation, but instead as a result of the ensuing lattice damage.

15.22

High Resolution Optical Defect Mapping in High-Resistivity Boron-Doped Silicon Carbide Wafers, Milind G Mier and John J. Boeckel, USAF Air Force, Wright Patterson AFB, Ohio.

Silicon carbide (SiC) is a promising materials system for extreme-environment high power substrates. While the carrier mobility in SiC itself limits performance to X-band frequency, higher-mobility device layers can use the high thermal conductivity of SiC to dissipate heat. This environmental tolerance comes at high price: SiC has no useful melt phase and new growth technology had to be developed. The leading technique involves growth by physical vapor deposition (PVD). A number of defects unique to the PVD growth have appeared, the most troublesome being the micropipe (um), a hollow hexagonal screw dislocation running along the growth axis. These uPs can have any size from sub-micron dimensions to hundreds of microns. It is a tribute to the ability of SiC crystal growers that uP density is typically no greater than a few tens per cm2. The up defect, unfortunately, propagates into epitaxial device layers grown on SiC substrates. Even small uPs degrade device performance severely and must be avoided. We show here a novel non-destructive wafer-level visible-light optical technique for high-resolution mapping of defects, including uPs, in bare SiC wafers and measure a number of experimental 2-inch boron-doped high-resistivity SiC wafers. Substrate wafer information is stored in a conventional compressed bitmap file and can be restored and analyzed at full resolution for comparison to device and device failure results. Defects located by this analysis of optical data are confirmed by conventional optical and scanning electron microscopy techniques. We have obtained both transmission and reflection visible-light scans of the whole wafers at various resolutions down to one micron resolution. Our analysis of this data reveals and allows us to map the locations of optical defects in each wafer. We conclude that the intrinsic nondestructive technique of visible-light optical scanning with the data stored in a compressed bitmap is a practical way to collect and store substrate information for troubleshooting subsequent processing difficulties.
15.24 6H-SiC Bulk Growth by Advanced PVT, Avinash Gupta1, Yoganathan Murugesu2, Edward Semenov3, Ilan Zwiebel2, Efjoe Emorhokpor1, Christopher Martin1, Thomas Kerr1, Andrew Souzis1, Jer en Henry3, Liutauras Storasta3, Erik Janzen3 and Robert F. Thomas3

II-VI, Inc. is interested in being a major commercial supplier of high-quality SiC substrates. Semis insulating 6H-SiC single crystals, doped with vanadium and vanadium-free have been grown by using Advanced PVT growth technique (APVT). The APVT process incorporates synthesis of ultra-pure SiC from semiconductor purity Si and C sources. The synthesized polycrystalline SiC demonstrates a large background contamination structure at the 3C-SiC/poly-crystalline SiC interface where an amorphous region is observed, likely the Si0_2 originally present between the bonded Si film and poly SiC substrate. The TEM cross sections indicate that the film is wholly amorphous which is advantageous for more optimized growth temperatures exceeding the melting point of Si. A detailed study of this material system is presented with the aim of providing feedback for possible improvements in the 3C-SiC growth process.

15.25 Characterization and comparison of a-plane and 8-degrees off-axis c-plane homoepitaxial films and the doped substrates, Sean Bishop1, Edward A Preble2, Christer Hallin3, Marek Skowronski; Carnegie Mellon University, Pittsburgh, Pennsylvania.

Structural, microstructural, electrical and optical characterization of a- and c-plane 4H-SiC homoepitaxial films and their substrates have been conducted. A range of x-ray rocking curve full-width half-maximum values for a-plane wafers and films were markedly smaller than analogous values acquired from the c-plane materials. Atomic force microscopy of the surface of the as-received a-plane, synthesized boules exhibited axial and radially uniform resistivity around 1E11 Ohm cm at room temperature. V-free undoped wafers contained residual boron and nitrogen at levels below 1E16 atoms/cm3, and demonstrated semi-insulating properties (resistivity between 1E6 and 1E11 cm^{-2}) with a carrier concentration ranging from 3x10^{14} cm^{-3} at 100 K to 7x10^{14} cm^{-3} at 300 K. These data indicate higher electron mobilities than reported previously for c-plane 4H-SiC from single crystal boules.

The sharp free exciton line present in a-plane photoluminescence data indicates the quality of the material. The results of additional investigations will also be presented, including structural characterization of the density and distribution of defects in these materials as well as preliminary electrical characterization of a- and c-plane PIN diodes.

15.26 Characterization of defects generated by boron diffusion in SiC, Xue-feng Lin1, Stephen P Smith1, Xianyun Ma2, Liang Wang3, Tangali S. Dadashzadeh2, Qingchun Zhang3 and Hsueh-Rong Chang3, Charles Evans Associates, Sunnyvale, California; 2Electrical Engineering Dept., Univ. of South Carolina, Columbia, South Carolina; 3Electronics Division, Rockwell Scientific, Thousand Oaks, California.

The diffusion of implanted boron (B) in silicon carbide (SiC) has been studied by using secondary ion mass spectrometry (SIMS) and photoluminescence (PL) spectroscopy and imaging. The focus of this paper is using a new approach to investigate the nature of defects generated by B implantation and thermal annealing. A commercial 4H-SiC(1000) substrate with an n-type epitaxial layer was implanted with 2x10^{14} atoms/cm^2 B. The sample was annealed at approximately 1700°C for about 1 second. High-resolution scanning PL images were acquired to determine the doping distribution of the as-implanted and annealed samples. Following annealing, various thicknesses of the sample were removed by mechanical polishing, and low temperature PL spectrum measurements were obtained to investigate the changes in the PL spectra with depth. The thermal annealing generated a B diffusion profile measured by SIMS to extend to about 3 microns depth. PL measurements were specifically taken on the as-implanted sample, the unpolished activated sample, and the sample with the diffused B layer removed by polishing for 2 to 3 microns of the sample. PL measurements were also made after removing another 3 microns of material. These measurements allow us to trace the variation of the PL spectrum and further explore the nature of the defects induced by the B implantation and thermal annealing. It is found that after removing the diffused B layer, the spectral feature at 415 nm disappears, which is consistent with its previous identification as arising from donor-acceptor pairs (DAP) [1]. The PL spectral features surviving after removing the B layer were investigated, supporting previous suggestions that these features are due to the di-interstitial (C-C or Si-Si) or di-vacancy (C-C or Si-Si) defects. [1]: V. Thanha, et al. Materials Science Forum 338-342 (2000) 909.
images with the optical micrographs of the sample taken in each step of preparation. Using this technique, we could uniquely correlate each particular morphological feature observed in transmission electron microscopy with it recorded in optical emission microscopy. Burgers vector analyses performed by applying different techniques indicated that the mobile segments are silicon-core 30 degrees partial dislocations while the immobile segments are carbon-core 30 degrees ones.

15.20 Photoluminescence at 1540 nm from erbium implanted amorphous silicon carbide films. Syros Gallas 1, Harry Efstrathiadis 1, Meng Bing Huang 2, Ei Ei Nyn 2, Uwe Hommerich 3, and Alain E Kalyeros 1; 1School of NanoSciences and NanoEngineering, The University at ALBANY-SUNY, ALBANY, New York; 2Department of Physics, Hampton University, Hampton, Virginia.

Erbium (Er) implanted material systems have received significant attention, since the Er 3+ exhibits an optical transition around 1540 nm, a wavelength falling in the infrared region, which is of interest for silica optical fibers used in optical communications. In particular, implanting silicon carbide (SiC) with Er can further extend the application of SiC to devices requiring light sources. Technologically important wavelength of 1540 nm on this work, we report on strong room temperature photoluminescence (PL) from Er-implanted and post-annealed amorphous silicon carbide (a-SiC:Er) films. The stoichiometric SiC films were grown by thermal chemical vapor deposition (TCVD), then implanted to Er fluences in the range of 5x1013 to 1x1016 ions/cm2 using 380 keV implantation energy. Post-implantation annealing was carried out at the temperature range of 550°C to 1350°C in argon (Ar) ambient. The resulting SiC films were characterized by Auger electron spectroscopy (AES), Fourier transform infrared spectroscopy (FTIR), nuclear reaction analysis (NRA), x-ray diffraction (XRD), and high-resolution transmission electron microscopy (HRTEM). Characterization was achieved on the annealed a-SiC:Er samples, even at room temperature, with PL intensity reaching a maximum for samples annealed at 900°C. Further studies of thermal quenching of Er luminescence from a-SiC:Er samples annealed at 800°C indicated that as the sample temperature increased from 14K to room temperature, the luminescence intensity at 1540 nm dropped by a factor of 3.6. In addition, post-deposition annealing at room temperature performed on the formation of SiC nanocrystals within the amorphous SiC matrix. The effect of these SiC nanocrystals on Er luminescence was also investigated.

15.30 Structural Analysis of the Carrot Defects in 4H-SiC Epilayers. Mourad Benannara 1, Marsh Snowdon 1, Joseph Summers 2, and Michael Melville 3; 1Department of Materials Science and Engineering, Stony Brook University, Stony Brook, New York; 2Mechanical Engineering, Stony Brook University, Stony Brook, New York; 3Mechanical Engineering, Florida International University, Miami, Florida.

The Silicon Carbide (SiC) is a potential semiconductor material to replace and out-perform the conventionally used silicon crystal in several electronic devices for high power and high frequency and high temperature applications because of its unique combination of properties such as high electric field break down strength, high electron velocity and high thermal conductivity. Due to the phase equilibrium in the Si/C system, SiC cannot be grown from melt transport (PVT) growth, also known as seeded sublimation, has been the most successful method to date for growing large SiC single crystals. In this method, SiC powder in a semi-sealed crucible is sublimed and recrystallized on a seed crystal maintained at temperatures above 1000°C was performed, leading to high-temperature solution growth of bulk SiC using Si melt. The growth process of SiC is complex and difficult to optimize due to the fact that the operating temperatures are extreme (2100-2500 deg C) and monitoring and controls are difficult. Since growth process occurs in almost air-tight graphite crucible and it is not feasible to observe the growing boule or determine experimentally the exact thermal conditions in the growth zone due to high operating temperatures and the opacity of the graphite crucible. The temperature field in the hot-zone has been predicted using numerical modeling. We have grown 6H SiC crystals using PVT system designed and fabricated in our laboratory. A new seed mounting technique has been developed for holding the seed on the crucible lid. Crystals up to 50 mm diameter have been grown at temperature range 2100-2200 deg C. The seed crystals and the grown bulk crystals have been characterized using Nomarski, SWBXT and Echting techniques to understand the formation of micropipes during the growth. The details on crystal growth of 4H SiC and defects characterization will be presented. References: 1. Carter, Jr, C.H., Tsvetkov, V.F., Glass, R.C., Henshall, D., Brudy, M., Muller, St.G., Kordina, O., Irvine, K., Edmond, J.A., Kong, H.S., Singh, R., Allen, S.T. and Pailour, J.A., Progress in SiC: from Material Growth to Commercial Device Development, Mater Sci. Engg, B61-62, 1-8, 1999. 2. G. Dhananjay, X.R. Huang M. Dudley, V. Prasad and R.H. M. Silicon Carbide Crystals: Part I : Crystal Growth and Characterization, chapter 6, p.181-232, in Crystal Growth Technology, Ed. K. Byrappa, T. Ohachi, Springer with William Andrew, New York, 2003 3. Chen, Q.S., Prasad, V., Zhang, H. and Dudley, M., Silicon Carbide Crystals: Part II:Process Physics and Modeling, Chapter 7, p 233-269, in ibid.
Atomic Force Microscope Observations of Growth and Defects on As-Grown (111) 3C-SiC Mesa Surfaces.

Philip G. Neudeck1, Andrew J. Truneck2 and J. Anthony Powell3.

1 NASA Glenn Research Center, Cleveland, Ohio; 2 OAI, Cleveland, Ohio; 3 Sest, Inc., Cleveland, Ohio.

We have previously reported the step-free surface heteroepitaxy growth technique for obtaining high yields of 3C-SiC mesa heterofilms completely free of stacking fault defects [1,2]. However, only abbreviated atomic force microscopy (AFM) data of as-grown 3C mesa film surfaces have been published to date [3]. This paper presents more extensive observations of as-grown (111) 3C-SiC mesa heterofilms by AFM. In nearly all cases, the as-grown (111) 3C-SiC surface consisted of single bilayer height (0.25 nm) steps.

Macrotips (i.e., step edges) were however observed. AFM also revealed some as-grown mesa surfaces in which sub-bilayer height line features with <111> orientation were superimposed across many single-bilayer height step patterns. Thermal oxidation of a selected 3C-SiC mesa confirmed the presence of step edges in the mesa film surfaces corresponding to where line features were previously imaged by AFM in the as-grown film surface. Other small perturbations in the step structure of the film surface are attributed to the intersection of isolated threading edge or basal plane dislocations. AFM revealed that the morphology on the (111) surface of 3C heterofilms varied as a function of growth conditions, film thickness, and film defect content. AFM of 3C-SiC film surfaces grown at temperatures below 1500 °C exhibit clear evidence of two-dimensional (2D) terrace nucleation. In some regions, the terrace nucleation appears quite random. In other regions, terrace nucleation is enhanced by the presence of threading edge dislocation defects producing triangular growth hillocks on the 3C-SiC growth surface [2,3]. At higher growth temperatures, 2D nucleation on the (111) surface becomes suppressed contributing to previously reported large differences in growth rate between mesas with and without stacking fault defects [3]. Experimental data (including AFM) suggests that 3C-SiC film growth becomes governed by growth on evolving facets at the edges of mesa crystals. Because the edge facet surfaces have higher chemical bond density than the top (111) surface, the facet surfaces are hypothesized to support more rapid crystal growth. [1] P. Neudeck, et al., Mat. Sci. Forum 389-393 (2002) p. 311. [2] P. Neudeck et al., to appear in Silicon Carbide and Related Materials 2003. [3] A. Truneck et al., to appear in Silicon Carbide and Related Materials 2003.

Abstract Withdrawn

Fabrication of Desk-Top type ion implanter for SIC device application.


The driving force of stacking fault formation in 4H silicon carbide p-i-n Diodes has been investigated using optical emission microscopy and transmission electron microscopy. The forward voltage drop has been observed to increase with time due to expansion of single-layer stacking fault stacking faults. TEM observations revealed 4H-SiC substrates which had an n-type epilayer doping as low as 5 x 1017 cm-3. This epilayer doping level is approximately two orders of magnitude below the reported threshold value (3 x 1019 cm-3) previously suggested for the onset of the generation of SIs in annealed epilayers.

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It is found that the basal planes of silicon carbide wafers are not parallel to the growth direction, but are inclined by an angle of about 3.8°. This inclination is typically known as the 4H-SiC orientation, which is one of the most common orientations in silicon carbide substrates.

The thermodynamic free energy difference between the perfect and a faulted structure is the driving force for the formation of stacking faults. The activation energy and stress exponent play a crucial role in determining the rate of SF growth. The SF growth is also influenced by the presence of pre-existing defects, such as dislocations, which act as nucleation sites for SFs.

The SFs are observed to move as long straight lines parallel to the basal plane with asymmetric location as compared to the position of the nucleation centres (edges or scratches of the samples). These lines correspond to faulted half loops consisting of the sample and ii) two 30 Shockley partial dislocations with a carbon core, one of them emerging at the sample surface and the other linked to the 30 Shockley partial dislocation with a silicon core, one of them emerging at the sample surface and the other linked to the 30 Shockley partial dislocation with a carbon core.

The SFs can be nucleated from pre-existing defects, such as dislocations, which act as nucleation sites. The SFs can also be nucleated from plastic deformation of boules during growth. They frequently form characteristic arrays with morphology consistent with that of basal plane slip bands. SiC homoepitaxy has a major effect of dislocation distribution. The threading dislocations are nucleated in the blocking layer even in the case of single crystal substrates, called pair array, will be presented. Finally, the defect characteristic of silicon carbide, the basal plane stacking fault, frequently found in as-grown epilayers, will be discussed.

Despite the essential role of dislocations and the increasing importance of silicon carbide in the high-power electronic industry, no direct experimental values on either perfect or partial dislocations velocity in SiC have been published so far, whatever their core. Nevertheless, transmission electron microscopy (TEM) observations show that partial dislocations with silicon core have a higher mobility than those with carbon core. This is actually in contradiction with ab initio calculations which demonstrate that partials containing core C are more strongly reconstructed whereas partials containing core C are more weakly reconstructed indicating that the latter partials are more mobile. The purpose of this work is to derive the stress exponent m and the activation energy Q of dislocation velocity [1] from introducing and developing fresh dislocations by cantilever bending in as-received high quality (11-20) 4H-SiC. V=A sinh (Q/RT) [1] A is a constant and sinh is the sinhoidal stress in the gliding basal plane. The wafer orientation is selected because of its most suitable geometry for deformation (high Schmidt factor).

The stress along the sample length is measured by determining the local radius of curvature. The plastic deformations are carried out at temperatures ranging from 823K to 1323K under neutral atmosphere. The dislocation propagation distance is measured by X-Ray transmission Topography (XRTT) or chemical etching. In addition, TEM studies are carried out to characterize the Burger's vector and the dislocation cores. XRTT observations and chemical etching reveal straight lines parallel to the basal plane with asymmetric location as compared to the position of the nucleation centres (edges or scratches of the samples). These lines correspond to faulted half loops consisting of i) one 30 Shockley partial dislocation with a silicon core, parallel to the surface and located close to the neutral plane at half the thickness of the sample and ii) two 30 Shockley partial dislocations with a silicon core, one of them emerging at the sample surface and the other linked to the 30 Shockley partial dislocation with a carbon core.

The SFs are formed by the gliding basal plane. The wafer orientation is selected because of its most suitable geometry for deformation (high Schmidt factor). The stress along the sample length is measured by determining the local radius of curvature. The plastic deformations are carried out at temperatures ranging from 823K to 1323K under neutral atmosphere. The dislocation propagation distance is measured by X-Ray transmission Topography (XRTT) or chemical etching. In addition, TEM studies are carried out to characterize the Burger's vector and the dislocation cores. XRTT observations and chemical etching reveal straight lines parallel to the basal plane with asymmetric location as compared to the position of the nucleation centres (edges or scratches of the samples). These lines correspond to faulted half loops consisting of i) one 30 Shockley partial dislocation with a silicon core, parallel to the surface and located close to the neutral plane at half the thickness of the sample and ii) two 30 Shockley partial dislocations with a silicon core, one of them emerging at the sample surface and the other linked to the 30 Shockley partial dislocation with a carbon core.
structures, Karim Myrbaev, Sergey Ostapenko, Igor Tarnovskii, Gregory Onukhtin and Marina Myrbaeva, 4枭iffe Institute, St.-Petersburg, Russian Federation; 5Nanostructures and Nanomanufacturing Research Center, University of South Florida, Tampa, Florida.

Results of optical studies of porous GaN/SiC structures and single- and multi-layer GaN epilayers grown on porous SiC (PSC) substrates are presented. In porous GaN/SiC structures, the most remarkable feature is strong photoresponse (PS) in visible part of the spectrum. The PS demonstrates peculiarities typical of persistent photoreconductivity effect in GaN, including non-exponential decay with characteristic times of thousands of seconds. Detailed PS, photoluminescence and electron microscopy studies allowed us to relate the PS to charged states localized at GaN/SiC interface in porous GaN/SiC structures. On single crystal epitaxial layers grown on PSC and SiC substrates, a PL study was performed. It appeared that layers grown on PSC substrates demonstrated increased PL intensity as related to those grown on non-porous SiC substrates. All PL bands were increased by approximately the same amount, which indicates that a mechanism of the increase is a reduction in density of non-radiative recombination centers in the layers grown on PSC. As transmission electron microscopy revealed reduction in dislocation density in GaN layers grown on PSC substrates, such a non-radiative recombination can be related to dislocations. Finally, results of electroluminescence (EL) measurements on a DH GaN/AIGaN LED structure grown on PSC will be presented. Luminance properties of GaN layers and GaN-based device structures will be used to discuss the advantages of epitaxial growth on porous substrates.

SESSION J8: MOS Structures
Thursday Afternoon, April 15, 2004
Room 209 (Moscone West)

1:30 PM J8.1
Comparison of electrical properties for MOS structures fabricated on the 4H-SiC (0001), (11-20), (000-1) faces. Kenji Fukuda, Power Electronics Research Center, National Institute of Advanced Industrial Science and Technology, Tsukuba, Ibaraki, Japan.

SiC MOSFET is expected to be available for next-generation switching devices. However, at present, the on-resistance (Ron) of the SiC power MOSFET is much higher than the theoretical value of SiC, which is well below 1E12 cm-2eV-1. The effective channel mobility of the MOSFET is much higher than the theoretical value of SiC the oxide integrity under electron injection from the semiconductor device at room temperature. To the best of our knowledge, this is the first observation of SDR in a SiC MOSFET.

We utilized a particularly sensitive form of electron spin resonance (ESR) called spin dependent recombination (SDR) to observe deep level defect traps at or near the interface of 6H silicon carbide and the SO2 gate dielectric in SiC MOSFETs. We find that the SDR response is strongly correlated to SiC/SiO2 interface recombination currents and also that the magnitude of the SDR response is correlated with processing induced changes in interface trap density, an extremely strong indication that we are observing the dominating interface/near interface trapping defects. The SDR response is extremely large, as large as one part in 350. To the best of our knowledge, this is the largest SDR response ever reported in a semiconductor device at room temperature. To the best of our knowledge, this is the first observation of SDR in a SiC MOSFET and arguably the first direct observation via magnetic resonance of a SDR signal. A fuller description of the electronic properties of these defects.

2:15 PM J8.3

We utilize a particularly sensitive form of electron spin resonance (ESR) called spin dependent recombination (SDR) to observe deep level defect traps at or near the interface of 6H silicon carbide and the SO2 gate dielectric in SiC MOSFETs. We find that the SDR response is strongly correlated to SiC/SiO2 interface recombination currents and also that the magnitude of the SDR response is correlated with processing induced changes in interface trap density, an extremely strong indication that we are observing the dominating interface/near interface trapping defects. The SDR response is extremely large, as large as one part in 350. To the best of our knowledge, this is the largest SDR response ever reported in a semiconductor device at room temperature. To the best of our knowledge, this is the first observation of SDR in a SiC MOSFET and arguably the first direct observation via magnetic resonance of a SDR signal. A fuller description of the electronic properties of these defects.

2:30 PM J8.4

One of the attractive features of MOS-based silicon carbide devices is their potential use for high temperature and high power applications. Earlier problems with high interface trap density (Drift) and low mobility on (0001) 4H-SiC MOS structures have been steadily improved via nitridation annealing with Drift reported as low as 1E11 cm-2 eV-1 near Ec and mobility approaching 100 cm2/V s. However, the use of such devices will ultimately be limited by oxide integrity and reliability. This paper presents high temperature dielectric breakdown (TDDB) results from both n-type and p-type MOS capacitors with thermal oxides grown under different nitridation conditions. Reliability measurements on n-type MOS capacitors biased into strong negative bias accumulation enable us to observe the oxide integrity under electron injection from the semiconductor where the barrier is relatively low due to the wide 4H-SiC bandgap. This emulate the on-state mode of operation thereby predicting the maximum allowable gate voltage (i.e., the minimum on-state resistance). Reliability measurements on p-type MOS capacitors, on the other
hand, predicts the maximum allowable field in the semiconductor (i.e., the maximum blocking voltage) by simulating the oxide stress during the MOSFET packaging mode of operation which is governed by hole injection. TDDDB measurements of MOSCAP MOSFETs (1200 °C dry oxide with 1300 °C N2O anneal) were performed at 175 °C and 300 °C under high positive bias stress. The devices are biased into strong avalanche conditions such that the electric field is high enough to collect breakdown data in a reasonable period of time. We observe that at 175 °C, a 100-year MTTF is obtained if the field in the oxide is kept below 6.5 MV/cm. The TDDDB measurement has also been performed at two lower bias lifetimes has been reduced by a few orders of magnitude. Recent reliability results on similarly oxidized MOSFETs have shown failures along the same trend as the n-type capacitors, indicating that MOSFETs and MOS capacitors can have similar reliability despite inherent processing and structural differences. PMOS capacitors fabricated with the aforementioned dry + N2O process as well as capacitors fabricated using the low D2HT nitridation techniques are currently being evaluated. [1] M. K. Das, "Recent Advances in 4H-SiC MOSFET Devices," International Conference on Silicon Carbide and Related Materials, Lyon, France, October, 2003. [2] G. Gudjonnsson, H. O. Olafsson, E. O. Sveinbjörnsson, "Enhancement of inversion channel mobility in 4H-SiC MOSFETs using a gate oxide grown in nitrous oxide (N2O)," International Conference on Silicon Carbide and Related Materials, Lyon, France, October, 2003.

2:45 PM 18:5

Electronic devices based on single crystal silicon carbide represent a good choice for high frequency and high power devices for use as sensors, switches, pressure devices and control electronics in high temperature applications such as inside fuel cells. The challenge is to develop a package that is resistant to thermal degradation in harsh environments. The packaging must protect the die and allow it to maintain functionality for durations of at least 1000 h. Elevated temperatures place severe loads on both the device and package. The thermal cycle is extreme and this all rules out only a handful of materials and materials systems. Polycrystalline silicon carbide is the material that we have chosen to study as a suitable package and materials suitability/compatibility has been considered on several levels. The package must be able to withstand prolonged exposure to harsh environments. We have demonstrated that quenching polycrystalline SiC can reduce fracture toughness and we have used indentation methods to determine the effect of thermal cycling on the mechanical properties of SiC. Sealing the package would be accomplished using a glass. The seal must be mechanically strong and hermetic. The maximum processing temperature for package joining using SiC electronics is 1888 deg.C and the package should operate up to 1000 deg.C. A glass with both that of thermodynamic stability place severe restrictions on the glass. We will describe our results in selecting suitable glasses for this application. Electrical connections between the device and package are required to be ohmic and long lasting. The interconnect lead wire system must be stable at high temperatures and resistant to thermal cycling. The bonding system that we will describe uses diffusion and transient liquid phase bonding. A copper interlayer is used to form a bond between the top chip level tungsten pads and the nickel wire lead. This method has produced some very promising results in recent long-term aging studies.

SESSION J9: Growth and Characterization
Thursday Afternoon, April 15, 2004
Room 909 (Moscone West)

3:30 PM 19:1
Device Critical Defects in SiC, Peder Bergman, Christer Hallin, Liutauras Storasta, Bjorn Magnusson and Erik Janzen; Department of Physics and Measurement Technology, Linkoping University, 58183 Linkoping, Sweden.

SiC devices, such as schottky barrier diodes and MOSFETs, are today available for different applications. Further development also in other applications requires improved material quality. Both in order to make the devices reliable, but also for improved performance. Critical defects are a great type of surface defects such as micropipes, stacking faults and dislocations. But also the role and influence of point defects, both impurities and intrinsic defects, remains to be understood. In this presentation we will review known properties and influence of these defects. In particularity the properties of dislocations, the properties and influence on point defects on for example carrier lifetime, and the role of intrinsic defects both as recombination centers and as responsible for semi insulating properties of high purity material.

4:00 PM 19:2
A correlation between implantation induced defects and dopant profiles in P implanted (0001) and (11-20) oriented 4H-SiC; Jennifer Wong-Leung1, Margaretta K. Linnarsson2, Bengt Gunnar Svensson3, 1Dept. of Electronic Materials Engineering, Australian National University, Canberra, Australian Capital Territory, Australia; 2Solid State Electronics, Department of Microelectronics and Information Technology, Royal Institute of Technology, Kista-Stockholm, Sweden; 3Department of Physics/Physical Electronics, University of Oslo, Oslo, Norway.

In this study, both (11-20) and (0001) n-type 4H-SiC substrates were implanted with 400 keV P and then annealed at different temperatures namely 1300°C and 1700°C. The various samples, both as-implanted and annealed, were studied by secondary ion mass spectrometry (SIMS), Rutherford backscattering and spectrometry (RBS) and transmission electron microscopy (TEM) to understand the damage evolution and defect structures resulting from different crystal orientations and different implantation damage. TEM analysis of the (0001) wafer shows the formation of basal plane dislocation loops, voids and some precipitates close to the loops. The (11-20) wafer showed some larger voids faceted on the [1-100] planes, some loops with basal plane as habit plane and other loops with the (11-20) habit plane. Some elongated loops on the basal plane were also observed to be pitted by precipitates. SIMS profiles show in some cases distinct differences between the two crystal directions. A comparison between the TEM and the SIMS results suggests a role of the difference in the behaviour of P at certain and precipitation close to dislocation loops.

4:15 PM 19:3
A Comprehensive Study of Impact Ionization Coefficients of 4H-SiC, Tetsuo Hatakeyama1, Takatoshi Watanabe1, Kazunori Kojima2, Nobuyuki Sano3, Takashi Shinohe1 and Kazuo Arai2, 1Corporate R&D Center, Toshiba corporation, Kawasaki, Japan; 2Power Electronics Research Center, National Institute of Advanced Industrial Science and Technology, Tsukuba, Japan; 3Institute of Applied Physics, University of Tsukuba, Tsukuba, Japan.

Impact ionization coefficients are important physical properties for power devices, because avalanche breakdown caused by impact ionization limits the voltage blocking capabilities of a power device. However, our knowledge of the impact ionization coefficient of 4H-SiC is limited, and the reported coefficients differ one another. Further, anisotropy of breakdown field of 4H-SiC was reported and it was shown that there is a significant reduction of the breakdown field when the electric field is applied perpendicular to the c-direction. In order to understand avalanche breakdown behavior of a 4H-SiC power device, reliable parameter sets for the impact ionization coefficients are needed. In this talk, we present the parameter sets of impact ionization coefficients of 4H-SiC for <0001> and <11-20> directions that reproduce avalanche breakdown behavior of p+n diodes on (0001) and (11-20) epitaxial 4H-SiC wafers. Impact ionization coefficients show large anisotropy; the breakdown voltage of a p+n diode on (11-20) wafer is 60% of that on (0001) wafer. We also discuss the origin of anisotropy of impact ionization coefficient of 4H-SiC based on the microscopic description of the ionization and the transport physics under high electric field; impact ionization coefficients can be obtained by integrating the product of impact ionization scattering rate, the distribution function and density of state. Impact ionization rate and density of state are independent of electric field. Distribution function varies according to a carrier temperature, and carrier temperature is proportional to saturation velocity and electric field. Saturation velocity varies according to the direction of the electric field, in general. Thus, the anisotropy of the impact ionization coefficients is attributable to the anisotropy of saturation velocity originated from the electronic structure of 4H-SiC. The experimental results of the anisotropic saturation velocity and temperature coefficients of impact ionization coefficients will be presented at the meeting.

4:30 PM 19:4
Growth and Metrology of Silicon Oxides on Silicon Carbide, Andrew M Hoff, Nanomaterials and Nanomanufacturing Research Center, University of South Florida, Tampa, Florida.

Thermal oxidation of SiC by the afterglow method has opened new pathways of opportunity to address both thin film growth and defects that hinder electronic device development with this important semiconductor material. Oxide growth, with rates up to 700 Å per hour, on SiC has been demonstrated using this technique over a temperature range from 600 °C to 1100 °C at 1 Torr total pressure. Electrical and physical properties of oxide films grown by conventional means or by the afterglow method were obtained with a novel,
non-contact charge-voltage (Q-V) metrology approach. This instrument employs a combination of incremental contact potential difference values obtained in response to applied corona charge generated from air. The slope of the Q-V characteristic within a bias range corresponding to accumulation of the semiconductor provides an effective dielectric permittivity value for the grown film. Effective permittivity values for afterglow oxides grown on SiC approach that of SiO₂ grown on silicon substrates whereas the values for oxides grown on SiC in an atmospheric steam oxidation process are always depressed relative to SiO₂ on silicon, indicating that the latter process always produces low-k oxides. A mechanistic discussion regarding these observed differences between the two oxidation methods is presented along with suggestions for an integrated process and metrology approach to reduce defects in oxide films on SiC.