SYMPOSIUM J

Silicon Carbide–Materials, Processing, and Devices

April 14 - 15, 2004

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* Invited paper
A Robust Process for Ion Implant Annealing of SiC in a Low-Pressure SiSiC Ambient, Shalaja P Rao, Stephen E Saddow, Roberta Nipoti, Fabio Bergamini, Yusuf Emirov and Anant Agarwal; 1Electrical Engineering, University of South Florida, Tampa, Florida; 2CNR, CNR - IMM Sezione di Bologna, Bologna, Italy; Cree, Inc, Durham, North Carolina.

High-dose Al implants in n-type epitaxial layers have been successfully annealed at high temperatures without any evidence of step bunching. Anneals were conducted in a silane ambient and at a pressure of 150 Torr. Silane, ranging in concentration from 21% to 100%, was diluted in a 6 slm Ar carrier gas and introduced into a CVD reactor where the sample was heated via RF induction. A 30 minute anneal was performed followed by a purge in Ar at which time the RF power was switched off. The samples were then studied via plan-view secondary electron microscopy (SEM) and atomic force microscopy (AFM). The resulting surface morphology was step-free and flat. Results of the annealing process and characterization results will be presented along with electrical data relating to the dopant activation and implanted region conductivity.

12000C). Ion implantation causes lattice damage and local stoichiometric imbalance. A post ion implantation anneal at high temperatures (1600 -17000C) is therefore necessary to repair the damaged lattice and to activate the implanted species. Some implantation induced defects survive the high temperature anneal and these, especially the deep defects, affect the performance of electronic devices. High energy electron irradiation of silicon carbide produces point defects—vacancies, interstitials, and anti-sites. These may form thermally stable complexes such as divacancies (Vsi -Vc). In this work, we compare the defects produced by Ar+ implantation in 4H-SiC with those produced by 1 MeV electron irradiation of 4H-SiC. A 4 micron thick silicon-doped 4H-SiC epitaxial layers with a doping concentration of 1 x 1015 cm-3 was Ar+ implanted at 6000C. The energy of the ions was 150 keV and a dose of 4.1 x 1016 cm-2. Post implantation annealing was carried out at 16000C for five minutes. An n-type 4H-SiC bulk with a doping concentration of 1 x 1017 cm-3 was irradiated with 1 MeV electrons at a dose of 0.1 to 6 x 1017 cm-2. The electron irradiation was carried out at room temperature; the temperature of the sample did not rise above 50 0C during irradiation. Both the Ar+ implanted and electron irradiated samples were studied with deep level transient spectroscopy (DLTS) and the results compared. After electron irradiation dose of 4.1 x 1017 cm-2, three strong peaks at Ec - 0.81 eV, Ec - 0.63 eV and at Ec -0.78 eV were observed. The defect at Ec -0.63 eV is the Z1/Z2 and the defect at Ec - 0.78 is the so called RD1/2. The concentration of Ec -0.63 eV increases with the electron fluence. This suggests that this isochronal annealing of the electron induced defects show that the annealing behavior of these defects may depend on the source of formation. The DLTS measurements of the Ar+ 4H-SiC reveal six capacitance peaks. The two most prominent peaks are at Ec - 0.74 eV and at Ec - 0.81 eV. A photo-DLTS measurements showed that the peak at Ec - 0.81 eV shifted to lower temperatures when the sample was illuminated with white light. However, illumination of the electron irradiated sample produced no observable effect.

SESSION J2: Crystal Growth & Processing
Chair: P. G. Neudeck
Wednesday Morning, April 14, 2004
Room 2009 (Moscone West)

10:30 AM J2.1

Homoepitaxial growth and characterization of thick SiC
layers with a reduced micropipe density, Hideaki Tachida, Isahs Kumat, Syun-juke Iizumi, Toshio Saka, Toshikiyo Misaki, Tomonori Nakamura and Kunikazu Iizumi; Yokosuka Research Laboratory, Central Research Institute of Electric Power Industry, 2-5-1 Nagasaki, Yokosuka, Kanagawa 240-0196, Japan.

The growth techniques of thick SiC epitaxial layers with a reduced micropipe density have been developed using a vertical hot-wall CVD reactor with an inner susceptor configuration. Micropipe closing by growing an epitaxial layer with a low C/Si ratio is possible with a nearly 100% probability for 4H-SiC(0001) and (001-0) substrates off-cut towards either (11-20) or (1-100) directions. Growth of low-doped and thick SiC epitaxial layers is also possible in the reactor with high growth rates of 15-20 mm/h, achieving a small roughness. A 210 \( \mu \)m-thick 4H-SiC epitaxial layer with a doping concentration of \( 9\times10^{19} \) cm\(^{-3} \) demonstrated 14.4 kV breakdown performance with a Ni Schottky contact. A long carrier lifetime of 1.4 \( \mu \)s at room temperature and 6.8 \( \mu \)s at 500 K was measured from a sample, while a large sample-to-sample variation was observed. The deep centers, impurities and dislocations were investigated to determine the lifetime killer of the epitaxial layers, and we found a correlation between carrier lifetime, and \( E_{1/2} \) and \( E_{III} \) centers.

11:00 AM *J2.2
Epitaxial Growth of 3C-SiC on T-shape columnar Si Substrate, Shigehiro Nishino, Akira Shoji, Taro Nishiguchi and Satoshi Ohashi; Department of Electronics and Information Science, Kyoto Institute of Technology, Kyoto, Kyoto, Japan.

Cubic SiC is a suitable semiconductor material for high temperature, high power and high frequency electronic devices, because of its wide bandgap, high electron mobility and high saturation electron drift velocity. The usage of Si substrates has the advantage of large area substrates for the growth of 3C-SiC layers. However, a large mismatch between 3C-SiC and Si has caused the generation of various defects at the SiC/Si interface. Lateral epitaxial overgrowth (LEO) of 3C-SiC on Si substrates has been reported to reduce the defect density. In this report, epitaxial growth of 3C-SiC on (100) Si and (111) Si substrates has been investigated to reduce interfacial defects. Epitaxial growth of 3C-SiC on the patterned seed 3C-SiC was performed by CVD using hexamethyldisilane (HMDS) as a source gas. Various patterned Si substrates were prepared. We employed a new approach for the substrate modification supported by computer simulation. For SiC etching and T-shape pattern was created on the Si substrate. Seed 3C-SiC layers were deposited on 3C-SiC on (100) Si and (111) Si substrates. Top surface of T-shape pattern consists of 1 micron thick, 50 micron wide 3C-SiC and 50 micron wide 3C-SiC and 50 micron wide 3C-SiC at the left side was supported by a source with a width. Epitaxial growth of 3C-SiC was carried out as following three steps. First step is in situ etching of the substrate. Second process is carbonization of the substrate. Third step is 3C-SiC deposition by atmospheric-pressure chemical vapor deposition. For (100) Si substrate, growth temperature was 1370 °C. Flow rate of H2 carrier gas and HMs were 2.5 slm and 0.23 SCCM, respectively. For (111) Si substrate, the seed 3C-SiC layer was grown at the growth temperature of 1350 °C. Grower layer showed trapezoidal shape and extended laterally. Crystal quality of the 3C-SiC film on the Si substrate and extended region without Si support is discussed.

11:15 AM *J2.3

We propose a model based on reaction diffusion equations to describe the oxidation of silicon carbide in dry O2 and we present experimental evidences of the SiO2/SiC interface elemental composition using oxygen isotope tracing. In the model we take into account several experimental evidences, the sample geometry and the sample preparation completely considered, since it has been experimentally verified that oxidation kinetics curves depend on the face exposed to the oxidant atmosphere: C-face, Si-face, or (1120)-face; ii) after oxidation is complete, we find an amorphous SiO2 film on c-SiC, with C located mainly near the SiO2/SiC interface; and iii) Si concentrations in SiC bulk and SiO2 are different. Reaction diffusion equations are proposed in one dimension, taken to be the direction normal to the sample surface, where the variables are the local concentrations of Si, C and O, either in their diffusive or fixed states. The sample geometry is introduced as initial condition. Reactions between the diffusing and fixed species are considered. Adequate sets of reaction rates and diffusion coefficients yield different kinetics curves depending uniquely on the initial sample geometry, as found in experiments. Different oxidation pressures yield different kinetics curves which may be collapsed by adequate scaling transformation. In our previous work [1] we observed that dry thermal oxidation of SiC and of Si produced similar silicon oxide films in the near surface and bulk regions for both semiconductors. However, the amount of O from a second oxidation performed in \( 18^0\)O enriched O2 gas (following a previous one in \( 16^0\)O) incorporated in the near interface region, was always smaller in the case of SiO2/SiC samples as compared to those of SiO2/Si, in which the concentration of \( 18^0\)O was equal to the isotope enrichment of the gas. In the present work with a stoichiometric sample of SiO2/SiC and SiO2/SiC oxidized either in \( 18^0\)O or in \( 16^0\)/180 gas sequences in order to determine the presence of O from the first oxidation in the interfacial region by \( 18^0\)O nuclear reaction profiling. Results indicate that in the case of SiO2/SiC samples both O isotopes are present in this region. The effect of the temperature of the second oxidation step and the role of carbonaceous species (mainly CO) formed during oxidation were also investigated. Besides, the presence of C and/or Si are also needed to complete stoichiometry of the dielectric film close to the interface.

11:30 AM *J2.4

Based on the predicted performance enhancements offered by the new generation of high power devices there is enormous potential for growth in SiC power devices in the next few years. In the development of substrate and epitaxial materials for this emerging commercial market it is imperative to develop a product to meet the targeted application. We will discuss the status and requirements for SiC substrates and epitaxial material for power devices such as Schottky and PIN diodes. For the SiC Schottky device where current production is approaching 50 amp devices, there are several material aspects that are key. These include: wafer diameter (3-inch and 100 mm), micropipe density (<0.3 cm\(^{-2} \) for 3-inch substrates and 20 cm\(^{-2} \) for 100 mm substrates), epitaxial defect densities, epitaxial doping and epitaxial thickness uniformity. For the PIN diodes the major challenge is the doping and the V\(_T\) characteristics due to the introduction of stacking faults during the device operation. We have demonstrated that the stacking faults are often generated from basal plane dislocations in the active region of the device. Additionally we have demonstrated that by reducing the basal plane dislocation density, stable PIN diodes can be produced. At present typical basal plane dislocation levels in our epitaxial layers are 100 to 500 cm\(^{-2} \). However, with proprietary epitaxial procedures we have achieved densities as low as 4 cm\(^{-2} \) in epitaxial layers grown on 8-inch off-axis 4H-SiC substrates. Work supported in part by DARPA contracts N00014-02-C-0309, N00014-02-C-0302, and Title III contract F33615-99-C-5316.
potential candidate for fulfilling the increasing demands on power density. Clearly this development should be empowered by a high volume production which is at the moment rather visible in the blocking voltage range around 1000V or even down to 600V for applications where charge controlled silicon devices are not suited (hard switching, high frequency bridge topologies with freewheeling diodes works too). Even reflecting the newest efforts regarding device stability and channel conductivity issue availability at the market will take place most probably soonest in 2005. As an alternative the silicon carbide MOSFET silicon carbide VJFET silicon MOSFET combination was developed and tested, however, even reflecting the newest results regarding the current instability problem due to a trapping phenomenon in the substrate and at the surface. In wide bandgap semiconductors, the trapping/detrapping is a slow process which causes degradation of both DC and RF performance. This excellent substrate quality and its high purity semi-insulating substrates, with dramatically reduced Vanadium content. Using better semi-insulating substrates should result in improved device performance.

In this work, the surface issue cannot be managed completely by growth techniques alone. Instead, it is dominated by the fabrication process, and can be mitigated considerably by using surface passivation. In this work, the influence of SiO2 and Si3N4 passivation treatments was investigated by comparing electrical characteristics of MOSFETs for a long period of 3 - 6 months. After SiO2 and Si3N4 passivation treatments, the output power improved to equal the theoretical value derived from the DC characteristics. The enhancement of output power has a correlation with the suppression of DC current instability, which can be explained by a reduction in trapping effects at the surface after passivation. The fact that the improvement of RF performance was more pronounced in class B operation than in class A operation suggests that the trapping effects would be more apparent in class B than in class A operation before passivation. In class B operation, the gate bias is close to the pinch-off, which is a high reverse bias applied to the field, on the field, on the metal and the semiconductor. A high reverse bias applied to the barrier increases the field in the junction and thus increases the probability for an electron to tunnel from the metal into the semiconductor. A higher number of injected electrons from the gate increases the probability of trapping. It is clear that the passivation treatments suppress the trapping effects at the surface improving both DC and RF performances. Passivation results using an MBE grown AlN layer are expected by the time of this conference.

Recent progress in SiC growth technology, a 150 nm p-type doped junction is fabricated in a commercial SiC wafer. Trimethylaluminum (TMAI) and Aravinda Kar2; 1AppliCote Associates, LLC, Lake Mary, Florida; 2University of Central Florida, Orlando, Florida.

Silicon carbide diodes are fabricated using a combination of gas immersion laser doping (GILD) and laser direct write (LIDW) in situ metallization in a commercial SiC wafer. Trimethylaluminum (TMAI) and nitrogen are the precursors to produce p-type and n-type silicon carbide semiconductors, respectively. Nd:YAG and excimer laser dopants, in SiC devices and under ambient conditions, increase the dopant concentrations by two orders of magnitude. Nd:YAG produces deep (500-600 nm) junctions while excimer produces shallow (50 nm) junctions. Laser doping results are shown in Table 1. Doping diffusion is introduced and utilized to dope Al in SiC wafers. Using this GILD technique, a 150 nm p-type doped junction is fabricated in semi-insulating 4H-SiC and n-type doped 4H-SiC wafers. Ohmic contacts are created by laser direct metallization producing patterned conductive phases in these doped materials. No metal is added to the SiC during LDW. These conductors are carbon rich when processed by nanosecond/pulse frequency doubled Nd:YAG laser (532 nm wavelength) and exhibit a stable contact resistance annealing up to 3 hours at 950 degrees Centigrade. Alternatively, an excimer (185 nm, 248 nm and 351 nm wavelength) laser can be used to create silicon rich Schottky contacts. The geometry of the diodes can be vertical or planar to the wafer surface and the high frequency performance is thought to reduce defect densities in the irradiated areas. Interconnection can be achieved by LDW in situ metallization on the surface or through the volume of the wafer. These laser processed diodes are intended for use in high-temperature, high-voltage and
high frequency switching and sensing applications.

2:45 PM **J3.5**
Improvement of GaN epitaxial growth by using SiC buffer layers with skin layer on. Marina Mynbaeva and Alia Sitnikova, Ioffe Physico-Technical Institute, St.-Petersburg, Russian Federation.

It has been shown that porous silicon carbide (PSC) is an effective buffer for homoepitaxy of SiC, as it allows one to reduce the density of point defects and dislocations penetrating from the substrate into the epitaxial layers. Further, in the case of stress mismatch, this type of stress reduction on one hand, hinder defects to penetrate from the heterosubstrate into the epitaxial layer. On the other hand, relaxation of these stresses is accompanied by formation of dislocations in the epitaxial layer. In this work, we present the data showing that using PSC buffer layers it is possible to reduce the effect of mismatch in GaN/SiC heterostructures. By employing PSC buffer layers, substantial reduction in structural defect concentration in GaN layers was achieved. Growth experiments were performed using PSC buffer layers with various thickness and morphology of porous structure. The important role of the skin layer covering porous structure will be demonstrated. 1. Sadow S E, Mynbaeva M., Choyke W J., et al., Mater. Sci. Forum 335-336, 115 (2000). 2. M Mynbaeva, S E Sadow, G Melnychuk, et al., Appl. Phys. Letters 78, 117 (2001).

SESSION J4: Sensors
Chair: P. Gouma
Wednesday Afternoon, April 14, 2004
Room 2009 (Moscone West)

3:30 PM **J3.1**
**SIC a Sensor Material for Extreme Environment.**
Anita Lloyd Spetz, IFM, Linkoping University, Linkoping, Sweden.

The excellent properties of silicon carbide have paved the way for commercially available Schottky devices for high power from Infimyn Technologies in Munich, Germany and UV fame detectors from General Electric in the US [1,2]. The porous bulk present the semiconducting feature of the material even at 1000C and makes it suitable for high temperature sensors and electronics. The high melting point and chemical inertness makes it especially suitable for rough and corrosive environments, and also a biocompatible material. A metal insulator silicon carbide field effect transistor, MISICFET, with buried source, drain and channel region has been developed [3]. It functions as a gas sensor by the application of catalytic gate metals like Pt and Ir. The voltage at a constant current is the sensor signal, which changes to a lower voltage e.g. in the presence of hydrogen, hydrocarbons or ammonia. The sensitivity to ammonia requires a porous gate metal. The device developed by ACREO, Stockholm, Sweden, is a short channel MISICFET device, and the baseline and the size of the gas response can be controlled by an applied negative voltage on the substrate. The MISICFET sensors have successfully been tested in several applications. Selective Catalytic Reduction, SCR, of NOx by NH3 in the catalytic converter in diesel exhausts can be regulated by an NH3 sensitive MISICFET sensor operated at 300C. A cold start sensor, which can be operated at 500C already a few seconds after start of the engine, will reduce emissions substantially. The combustion process in a boiler can be controlled by a MISICFET sensor array measuring online in the flue gases. These applications require very long term stable and, especially in the case with the NH3 sensor, very selective and sensitive sensors. Nanoparticles of e.g. Al2O3 impregnated with Pt or Ir is developed as the gate material for the MISICFET devices. This will provide a very large amount of active sites for the gas response and hopefully a very stable metal /insulator interface. Interactions between the carriers and the Al2O3 causes a free standing chip with integrated heater and temperature control as well as processing devices on a micro-hot plate will be discussed. [1] http://www.infimyn.com/cgi/erf.dll/erfscripts/pro/etc.js?sid=18680 [2] D M Brown, J Krichmer, J Fedison, T Dean, Electrochem. Soc. Proc. 3, 83 (2002). [3] Recent Major Advances in SiC, eds. Jim Choyke, Hiroyuki Matsunami, Gerhard Pensl, Springer, Singapore.

4:00 PM **13.2**
**Colour image sensor based on amorphous silicon carbide p-i-n structures.**
paula louro 1, M Fernandes 1, A Fasoi 1, A Maccarri 1, M Vieira 2, N Carvalho 2 and G Lavesarde 2 , 1DEETC, ISEL, Lisboa, Portugal; 2CFM, IST, Lisboa, Portugal.

Photodiodes based on p-i-n amorphous silicon carbide structures have several applications in the field of photosensitive devices. In this work we report its use as a colour image sensor. These structures exhibit a strong dependence of the spectral response on the applied voltage, which means that the spectral sensitivity can be electrically controlled. We used several p-i-n structures based on amorphous silicon and amorphous silicon carbide produced by PECVD with the configuration glass/ITO/p(a SiC:H)/n(a Si:H)/a Si:H/Al/ITO. All have the same intrinsic layer and in the doped layers we changed the resistivity through the addition of methane to the doping gas. For the optical characterisation of the devices we measured the I(V) characteristics under daylight-like illumination (AM1.5) and with appropriate neutral density filters we also varied the photon flux. Interference filters with maximum transmission at wavelengths 450 nm, 550 nm and 650 nm and half width (FWHM) of 40 nm were also used in order to evaluate the I(V) characteristics under monochromatic illumination at different photon fluxes. Results show that for 650 nm illumination a higher voltage is needed for complete collection of photo-generated carriers, while for 450 nm illumination a lower voltage is sufficient to reach the collection of carriers in the saturation current. Thus, at a constant photon flux it is possible to separate different wavelengths at distinct bias voltages. The spectral response dependence on the applied voltage and on optical bias was also studied. Results show that the spectral sensitivity is strongly dependent on the applied voltage, namely the maximum spectral sensitivity shifts with the voltage, and the spectral response goes down to zero at certain wavelengths, which allows a different sensitivity and enables colour imaging. By simply varying the applied voltage, at each wavelength the red signal is suppressed allowing green recognition. The red information is obtained by tuning the voltage to higher values where the green signal goes down to zero. Combining the signal information at different voltages a colour image can be obtained. The use of this transport mechanism on the spectral region and on the applied bias voltage is explained taking into account the experimental data and the results obtained through a detailed numerical simulation based on the ASCA simulator.

4:15 PM **13.3**
**Robust Gas Sensors using 3C-SiC/Si Epitaxial Layers.**
John W. Weilbacher 1, Tammy Forbes 2, Rachel L. Myers 2, Jeremy Walker 2 and Stephen E Sadow 2, 1Chemical Engineering, University of South Florida, Tampa, Florida; 2Electrical Engineering, University of South Florida, Tampa, Florida.

A hydrogen gas sensor consisting of planar electrical ohmic contacts formed on the surface of a 3C-SiC epitaxial layer grown on Si(001) has been fabricated and tested. The n-type, 4 μm thick 3C-SiC epi layer was grown under low-pressure conditions with an approximate doping density of 1018 cm-3. This sensor demonstrates a two-fold repeatable improvement in stability and sensitivity in comparison to an n-type Si sensor of the same type also fabricated and tested under the same conditions. Both the 3C-SiC/Si and Si sensors operated up to 290C; however, the 3C-SiC/Si sensor also allowed detection of hydrogen at concentrations far exceeding that of the Si sensor. The 3C-SiC/Si device detected hydrogen at concentrations ranging from 0.33% to 100% in Ar while the Si sensor could only detect hydrogen at concentrations ranging from 2% to 100% in Ar. In the preliminary data, it has been shown that 3C-SiC/Si hydrogen sensors of this type have a larger dynamic range and higher sensitivity to hydrogen than Si sensors, thus allowing for harsh environmental applications. The 3C-SiC/Si sensor response to hydrocarbons, moisture, and air will also be presented. In addition, the second generation contact design for high temperature operation will be demonstrated.

4:30 PM **J3.4**
**Development of SiC-Based Gas Sensors For Aerospace Applications.**
Gary W. Hunter 1, Philip G. Neudke 1, Jennifer Xu 2, Dorothy Lukes 2, Michael A. Artale 3, Peter S. Lampard 3, Drago Androjoa 3, Chung-Chun Liu 5, Darby B. Makoi 5 and Benjamin J. Ward 5, 1NASA Glenn Research Center, Cleveland, Ohio; 2QSS Group, Inc., Cleveland, Ohio; 4Akima/NASA Glenn Research Center, Cleveland, Ohio; 5Case-Western Reserve University, Cleveland, Ohio; 6Makel Engineering, Inc., Chico, California.

Silicon carbide (SiC) based gas sensors have the ability to meet the needs of a range of aerospace applications including leak and fire detection, emission monitoring, and environmental control. The ability of SiC-based gas sensors to potentially operate at a range of temperatures, in oxygen free environments, or in extreme conditions contributes to this considerable advantage. A common challenge for each of these applications is the design and operation of the sensor in such a way so as to detect the species of interest at the appropriate concentration ranges while maintaining stable operation. Each application has its own requirements. Interference is surrounding the various components of the SiC gas sensor structure play a crucial role in determining the feasibility of the sensor for use in a given application. This structure varies depending on the application but typically includes a reactive sensing layer, an interfacer layer between

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the sensing layer and the semiconductor, and the SiC semiconductor. This paper discusses the gas sensing needs of several aerospace applications requiring SiC-based gas sensors, often in conjunction with other gas sensors, to meet these needs. In particular, this paper will discuss methods being used to tailor the sensor structure for the application. For example, a carbide or oxide intermediate layer can improve the sensor stability at higher temperatures while changing the sensing material decrease the sensitivity to certain hydrocarbons. Most importantly, the approach of using atomically flat SiC to provide an improved and uniform SiC semiconductor surface for sensor deposition will be discussed.

Examples of the demonstration of SiC gas sensors in aerospace applications will also be given. It is concluded that, while significant progress has been made, the development of SiC gas sensor systems is still at a relatively early level of maturity for some applications.

SESSION J5: Poster Session
Wednesday Evening, April 14, 2004
Salons 8-9 (Marrriott)

J5.1 Abstract Withdrawn

J5.2 Aluminum-ion implantation into 4H-SiC (11-20) and (0001). Yuki Negoro, Tsunenobu Kimoto and Hirohiko Mutsunai, Electronic Science and Engineering, Kyoto University, Kyoto, Japan.
Aluminum-ion (Al⁺⁺) implantation into 4H-SiC (11-20) and (0001) has been investigated (RT). Implantations were carried out at 500 °C or room temperature. Post-implantation annealing was performed in an Ar ambient at 1800 °C with a graphite cap made from photo-resist. The graphite cap, after the growth of high-dose Al⁺⁺-implanted (0001), resulted in an excellent flatness with an rms roughness of 1.0 nm. Regarding electrical properties, a sheet resistance of 1.9 MΩ/sq. could be achieved by co-implantation with carbon ions, in the case of RT implantation into (11-20). For 500 °C implantation, the lowest sheet resistance of 1.7 MΩ/sq. was obtained by increasing the Al⁺⁺ dose up to 6.0×10¹⁶ cm⁻². The Hall-mobility (hole) differs in (11-20) and (0001). The mobility in (11-20) is 10 cm²/Vs at RT, which is about 3 times higher than that in (0001). The temperature dependence of free hole concentration for each face is extremely weak. An annealing time dependence of sheet resistance, SIMS profile, and surface morphologies of Al⁺⁺-implanted 4H-SiC (11-20) and (0001) will be discussed.

J5.3 Morphology-controlled synthesis of nanostructured silicon carbide. Xiong-Yun Guo and Guo-Qiang Jin, State Key Laboratory of Coal Conversion, Institute of Coal Chemistry, Taiyuan, Shanxi Province, China.
The sol-gel route was employed to synthesize nanostructured silicon carbide materials. In the route, tetraethoxysilane (TEOS) and phenolic resin were used for preparing a binary carbonaceous silicon xerogel, the xerogel precursor was then temperature-programmed heated to about 1250°C and kept at the temperature for 20 hours in an argon flow. Purified β-SiC was obtained by removing excess silica, carbon and other impurities. By controlling different additives in the sol-gel process, we can obtain differently nanostructured SiC materials. (a) SiC whiskers if no additive employed, (b) SiC nanowires under the presence of aluminol sol, (c) mesoporous SiC under the presence of a small quantity of nickel nitrate and (d) spherical SiC nanoparticles under the presence of excessive nickel nitrate. The different products in the sol-gel process results in a self-organization of primary colloidal particles, which usually forms large secondary grains consisting of phenolic resin and embedded silica particles. The self-organization has changed the reaction environment of carbothermal reduction, as a result differently morphological SiC samples can be produced.

J5.4 600V 4H-SiC RESURF-type JFET. Satoshi Hatakeyama, Michitomo Iyama, Kazuhiro Fujikawa and Atsushi Ito, Energy and Environmental Technology Research Laboratories, Sumitomo Electric Industries, LTD., Osaka, Japan.
An integrated circuit module with SiC switching devices is promising, because of low loss and high temperature operation, especially in an electric or hybrid automobile. A lateral switching device is suitable for the module from the point of view of system integration. In spite of recent progress, SiC-MOSFETs have still suffered from the low channel mobility and oxide reliability. A RESURF-type JFET is suitable structure for a lateral switching device with the breakdown voltage of above 600 V for an inverter module which drives motors of an electric or hybrid automobile. In this study, 600 V RESURF-type JFETs were fabricated on SiC with the operation characteristics. The drift region between the drain and the source areas has a double RESURF structure to reduce the on-resistance. The width and the length of the channel are 200 μm and 10 μm, respectively. The distance between the drain and the gate area, which is the drift length, is 15 μm. The fabricated devices showed normally-off operation. The threshold voltage is about 0.3 V. The saturation current is about 0.6 mA at a gate voltage of 3 V. The specific on-resistance is about 160 mΩ·cm². The maximum breakdown voltage is 720 V.

J5.5 Deep Level Defects in He-implanted 6H-SiC Studied by Deep Level Transient Spectroscopy. Xudong Chen, Department of Physics, The University of Hong Kong, Hong Kong, Hong Kong, China.
Deep level transient spectroscopy (DLTS) was used to study deep level defects in He-implanted n-type 6H-SiC samples. Low dose He-implantation (1X10¹¹ cm⁻²) has been employed to keep the as-implanted sample conductive so that studying the annealing behavior of the He-implantation induced defects becomes feasible. Strong DLTS peaks at Ec-0.57/0.7 eV were observed in the as-implanted sample. The intensities of the Ec-0.57 eV levels increase even with filling pulse widths longer than 10 ms. The electrons captured at these traps were found to depend logarithmically on the duration time of the filling pulse. This indicates that these traps may be related to the charged dislocation defect. This peak can be significantly reduced by annealing residual defects at 500°C. For the Ec-0.57 eV peak, it anneals at about 300°C. Moreover, Ec-0.57 eV and Ec-0.3/0.4 eV (E1/E2) deep levels were found to be generated after the He-implanted sample was annealed at 500°C. ACKNOWLEDGEMENT This work is supported by the RGC, HKSA (No.7085/01P) and CRCEG, HKU.

J5.6 The interaction of C60 with Si(111) and Co/Si(111). Md. Akhil Zulian, Hai Xu, Xue-song Wang and Andrew Thye-Shen Wee, Physics, National University of Singapore, Singapore, Singapore.
We report STM (scanning tunneling microscopy) and XPS (X-ray photoelectron spectroscopy) studies of the interaction of C60 on Si(111)-7x7 and Co/Si(111) at different annealing temperatures (room temperature to ~720 °C). On Si(111), Si(100) [1], Pt(111) and Ni(111) [2], C60 molecules decompose completely at 500 °C, 850 °C and 50 °C, respectively. They form SiC at the interfaces with Si and graphite sheets with Pt and Ni surfaces, the latter surfaces catalyzing the decomposition process. Usually SiC films are grown by chemical vapor deposition at 1300-1500 °C. Due to the 8% difference in the thermal expansion coefficients and 20% lattice mismatch between Si and SiC, SiC grows with a high density of defects during high temperature carbonization process. One way to improve the crystallinity of the film and the quality of interface is to reduce the synthesis temperature. Several papers have reported growing SiC at lower temperatures (800-1000 °C) using C60 as a precursor on Si(110) and Si(111). One recent study using superionic C60 beams on Si(111) surface reported SiC formation at 750 °C [3]. We have done a comparative study of the thermal decomposition of C60 on Si(111) and Co/Si(111). The C1s core level XPS peaks show the shift of the peak and formation of SiC. The C60 cage begins to break at ~500 °C on Co/Si(111) which is ~250 °C lower than in previous reports [4]. The C-C component disappears completely with only the C-Si component remaining at 910 °C on Si(111) and 720 °C on Co/Si(111). The growth of a small peak at the higher binding energy end of the Si2p peak confirms SiC formation on both surfaces. Our STM images are in agreement with the XPS results where we see “ball-like” C60 molecules as well as small SiC clusters at 450 °C on Co/Si(111) indicating partial decomposition of C60. The C60 profiles show that some C60 molecules have opened their cages and formed SiC clusters with thickness of 25 Å. STM images also show localized SiC reconstructions at 625 °C and regular SiC clusters at 720 °C on Co/Si(111). We conclude that cobalt acts as a catalyst to open the C60 cage at significantly lower temperatures, facilitating SiC growth. References: [1] C. Cepek, P. Schiavuta, M. Sancrotti and M. Pedio, Phys. Rev. B 53, 7466-7472 (1996). [2] L. Aversa, R. Modesti, Phys. Rev. B 53, 7466-7472 (1996). [3] L. Rimai 3, G. Newaz 4, S. Ng', R. Naik 2 and G. Auner 3; Physics, The University of Hong Kong, Hong Kong, Hong Kong, China.

A multilayer was successfully formed on epitaxial SiC in the presence of a thick Pd film deposited onto the AlN as a catalytic electrical contact and 1800 Å thick Pt film was deposited onto the AlN, forming an ohmic contact. Details of the deposition processes were carried out by magnetron sputtering. Depositions of insulators, as well as preliminary data on the response to Hydrogen have been presented. The electrical behavior of these structures is that of the forward region of the transmission line corresponding to the p-type Pd. The sensor response was obtained by monitoring the change in forward bias required to keep a preset constant current as the concentration of Hydrogen in the surrounding gas was changing. Detailed results will be presented describing the dependence of this bias shift on Hydrogen concentration and on flow rate and temperature effects. At fixed flow rate, the response initially increases roughly linearly with concentration, but eventually becomes completely saturated. The magnitude of the response as well as the saturating concentration increases with temperature. The response saturates at 60 ppm at 120 °C, and at 125 ppm at 250 °C. The magnitude of the response also increases with flow rate, up to a flow rate of about 100 sccm, above which it remains constant. In the linear region, the magnitude of the response increases by a factor of 6 between 120 and 250 °C, at a flow rate of 200 sccm. This flow rate change is due to the increase in concentration, but in different manner. The Si-based device on SiC has approximately the same behavior which is consistent with that expected from an AlN/SiC heterojunction, with an apparent barrier height in the absence of Hydrogen of about 1.5 eV (AlN thickness of 500 Å). In the presence of 100 ppm of Hydrogen, at 250 °C this barrier is reduced by about 0.25 eV. The magnitude of this response is in the same order as the shift in the C(V) curve of the Si based device with approximately the same thickness and at the same temperature. It will be shown that the response of another type of device can be explained as resulting from the accumulation of positive charges within the AlN in the vicinity of the interface. The source for these charges is the catalytically dissociated atoms of Hydrogen which diffuse through the Pd and at the interface with the AlN leave the electron behind in the AlN. The response behavior is consistent with that expected from an AlN/SiC heterojunction, with an apparent barrier height in the absence of Hydrogen of about 1.5 eV (AlN thickness of 500 Å). In the presence of 100 ppm of Hydrogen, at 250 °C this barrier is reduced by about 0.25 eV. The magnitude of this response is in the same order as the shift in the C(V) curve of the Si based device with approximately the same thickness and at the same temperature. It will be shown that the response of another type of device can be explained as resulting from the accumulation of positive charges within the AlN in the vicinity of the interface. The source for these charges is the catalytically dissociated atoms of Hydrogen which diffuse through the Pd and at the interface with the AlN leave the electron behind in the AlN. The response behavior is consistent with that expected from an AlN/SiC heterojunction, with an apparent barrier height in the absence of Hydrogen of about 1.5 eV (AlN thickness of 500 Å). In the presence of 100 ppm of Hydrogen, at 250 °C this barrier is reduced by about 0.25 eV. The magnitude of this response is in the same order as the shift in the C(V) curve of the Si based device.
paper through both physical characterisation and electrical characterisation using a highly surface quality sensitive devices such as high voltage Schottky diodes. Schottky diodes have been fabricated using room temperature Boron implantation to form the JTE termination as well as the P+ anode of the pn diodes. The targeted breakdown voltage is 2.5kV. One of the critical step is the high temperature annealing, performed at 1700°C, which degrades the samples surface but is necessary to correctly activate the Boron impurities. After this process, the RMS measured by AFM is 10.7nm on 5mmx5mm area and can reach 20.9nm on 15mmx15mm area in some parts of the sample. The measured breakdown voltage of the diodes is in the range of 900-1100V. The ohmic contacts made on the pn diodes are rectifying. This is due to the fact that the boron implanted near the surface has exodiffused and the true concentration of boron impurities is far less than expected in this near surface region. This has a direct impact on the JTE termination efficiency and the ohmic contact formation. After removing the top layers of metal and passivation, fine polishing process has been made. The RMS values measured by AFM after the polishing are 1.4nm on 5mmx5mm area and maximum 5.35nm on 15mmx15mm area in some parts of the sample. The diodes have been fabricated again with the same process and mask steps. After the polishing step, we do not observe a degradation of the forward characteristics of the diodes. Schottky barrier, ideality factor and On-resistance are almost unchanged. At low current, we see the improvement of the I-V characteristics, indicating a possible removal of surface defects in localised part of the sample. In the reverse mode we observed a clear improvement of breakdown voltage. This results is due to several factors. First of all, it is due to the elimination of surface un-doped region caused by strong oxide diffusion. Second, there is also an improvement of surface roughness and a removal of residuals thanks to the polishing step. We are also expecting a possible improvement of yield on large area devices. This point is under study and will be presented at the conference.

**15.13 First Observation of Deep Level Defects in 4H SiC Diodes with Magnetic Resonance**, Shin-ichi Miyahara1, Patrick Lassak1 and Robert S. Okolie2, 1The Pennsylvania State University, University Park, Pennsylvania, 2NASA Glenn Research Center, Cleveland, Ohio.

We report the first observation of deep-level defects in 4H SiC PIN diodes with a very sensitive electron spin resonance technique called spin-dependent recombination (SDR). The diodes were subjected to high current stressing prior to SDR measurements. We observe a relatively strong SDR signal consisting of at least two peaks. The stronger peak has a g value of approximately 2.005 when the magnetic field is oriented parallel to the crystalline c-axis. The stronger signal exhibits weak g anisotropy. Although we have yet to develop a detailed model of the defect structure, we very tentatively link the paramagnetism to unpaired electrons in silicon wave functions. The SDR amplitude is a strong function of forward bias voltage; the signal is strongly peaked at a forward bias of 2.2 volts. This result is consistent with, and strongly supports the idea that the observed signal is caused by deep-level defects (presumably involving stacking faults) which play dominating roles in recombination processes in the diode. According to Lindefelt and colleagues, a stacking fault in 4H-SiC PIN diode acts as a one-dimensional quantum well, thus altering the optical and electronic properties of the crystal [1]. This idea is based on total energy calculations of a 4H-SiC crystal containing an intrinsic, where it has been found that a narrow band is split off from the bottom of the conduction band and extends about 0.2 eV into the bandgap of 4H-SiC [2]. [1] U. Lindefelt and H. Iwata, in "Recent Major Advances in SiC", Springer-Verlag, Berlin (2003). To press [2] M. S. Miao, S. Linanujumong, and W. R. L. Lambrecht, Appl. Phys. Lett. 79(26), p. 4360 (2001).
was prepared by mixture of Si/ SiO2. The precursor led to complete conversion of (SiO2+ C Si3O2) to (SiC) through overall reaction with heat treatment under inert gas flow at temperature higher than 1623K. The amount of unreacted carbon was determined by thermogravimetric analysis (TG/DTA), Fourier transfer infrared spectroscopy (FTIR) and scanning electron microscopy (SEM). Laser ablation of solid substrates was used to convert SiC into nanotubes with outer diameter smaller than 150 nm, inner diameter larger than 100 nm and length of the order of a few microns. The growth was controlled using different substrate temperatures. The GaAs wafer was converted to p-type by thermal annealing. The effect of dopant concentration and conductivity type on preferential etching of 4H-SiC by molten KOH. Ying Gao1, John Chen2 and Carl Johnson 2; 1Wide Bandgap Materials Group, Elkington2, Ilya Zwieback’, Michael Dudley3, Thomas Anderson’, Sudarshan2; 2Engineering Physics/ ENP, Air Force Institute of Technology, WPAB, Ohio.

As a high mobility, wide-bandgap semiconductor, 3C-SiC has great promise. In this paper, we examined to obtain 3C-SiC epilayer on Si substrates using hot-wall CVD furnace and report the use of hexamethyldisilane (HMDS) and propane as reaction gases to grow thick (5-50 micron) 3C-SiC epilayers. The susceptor was surrounded by graphite foam. Temperature of the susceptor was measured at inside wall of the susceptor by optical pyrometer. HCl flow rate for etching was 1.0 - 2.0 sccm. An initial characterization procedure was performed using 1 sccm propane at 1250 °C for 2-3 minutes. During the growth of SiC at 1300 °C for 1 hour, the flow rate of HMDS was 0.75-1.2 sccm and the flow rate of propane was 0.1-0.5 sccm. The hydrogen carrier gas flow rate was 3-10 slm. Typical growth rate was 3 micron /h. Uniform thick 3C-SiC was obtained. The samples were examined using optical microscopy, SEM and RIEED. Electrical properties are also discussed.

15.18 Epitaxial Growth of 2 inch 3C-SiC on Si Substrates by Atmospheric Hot Wall CVD. Jiliang Zhu, Yi Chen, Yusuke Mukai, Akira Shoji, Satoru Oshima and Shigehiro Nishino; Electronics and Information Science, Kyoto Institute of Technology, Kyoto, Japan.

High mobility, wide-bandgap semiconductor, 3C-SiC has great promise. In this paper, we examined to obtain 3C-SiC epilayer on Si substrates using hot-wall CVD furnace and report the use of hexamethyldisilane (HMDS) and propane as reaction gases to grow thick (5-50 micron) 3C-SiC epilayers. The susceptor was surrounded by graphite foam. Temperature of the susceptor was measured at inside wall of the susceptor by optical pyrometer. HCl flow rate for etching was 1.0 - 2.0 sccm. An initial characterization procedure was performed using 1 sccm propane at 1250 °C for 2-3 minutes. During the growth of SiC at 1300 °C for 1 hour, the flow rate of HMDS was 0.75-1.2 sccm and the flow rate of propane was 0.1-0.5 sccm. The hydrogen carrier gas flow rate was 3-10 slm. Typical growth rate was 3 micron /h. Uniform thick 3C-SiC was obtained. The samples were examined using optical microscopy, SEM and RIEED. Electrical properties are also discussed.


Silicon carbide (SiC) is a promising materials system for extreme-environment high power substrates. While the carrier mobility in SiC itself limits performance to X-band frequency, higher-mobility device layers can use the high thermal conductivity of SiC to dissipate heat. This environmental tolerance comes at a price: SiC has no useful melt phase and new growth technology had to be developed. The leading technique involves growth by physical vapor deposition (PVD). A number of defects unique to the PVD growth have appeared, the most troublesome being the micropipe (up), a hollow hexagonal screw dislocation running along the growth axis. These up’s can have any size from sub-micron dimensions to hundreds of microns. It is a tribute to the ability of SiC crystal growers that up density is typically no greater than a few tens per cm2. The up defect, unfortunately, propagates into epitaxial device layers grown on SiC substrates. Even small up’s degrade device performance severely and must be avoided. We show here a nondestructive whole-wafer visible-light optical technique for high-resolution mapping of defects, including up’s, in bare SiC wafers and measure a number of experimental 2-inch boron-doped high-resistivity SiC wafers. Substrate wafer imaging is performed in a conventional convexed bitmap file and can be restored and analyzed at full resolution for comparison to device and device failure results. Defects located by this analysis of optical data are confirmed by conventional optical and scanning electron microscopy techniques. We have obtained both transmission and reflection visible-light scans of the wafer samples at various resolutions down to one micron resolution. Our analysis of this data reveals and allows us to map the locations of optically detected defects in each wafer. We conclude that the noninvasively nondestructive technique of visible-light optical scanning with the data stored in a compressed bitmap is a practical way to collect and store substrate information for troubleshooting subsequent processing difficulties.
Single crystal 3C-SiC epitaxial layers have been grown on SOI substrates using low-pressure chemical vapour deposition (LPCVD). The SOI substrates consist of nominally 1.9 μm Si layers bonded to 100 nm poly 3C-SiC substrates using direct wafer bonding and SOI film transfer techniques. Misfit Si(100) films were incorporated into the wafer alignment process in an effort to further minimize the strain and facilitate epitaxial growth of the films. The Si films were transferred from Si(100) wafers miscut 4° toward the (110) direction. For growth of 3C-SiC layers, a two-step process is needed. First the Si is etched in a hydrogen carrier gas to convert the surface to SiC at atmospheric pressure. Next SiC growth is conducted by the addition of silane into the gas mix and a reduction of the pressure process to 150 Torr. Characterization of these films via SEM and XRD indicate that the films are single crystal and oriented with respect to the starting Si bonded film. The films are of high quality and XRD FWHM of less than 600 arc-sec have been achieved. In this work we present results of TEM analysis of these films which show a high degree of the 3C-SiC/poly-crystalline SiC interface where an amorphous region is observed, likely the SiO₂ originally present between the bonded Si film and poly SiC substrate. The TEM cross sections indicate that the Si film is wholly carbonized which is advantageous for growth at optimized growth temperatures exceeding the melting point of Si. A detailed study of this material system is presented with the aim of providing feedback for possible improvements in the 3-C SiC growth process.


The electroluminescence, mobility and core structure of partial dislocations in silicon carbide p-i-n diodes were investigated using optical emission microscopy and transmission electron microscopy. It is well-known that the formation of partial dislocations in diodes under forward bias is responsible for formation of the light-emitting faults and the dislocations. In this paper we will use PL to understand this phenomenon, the mechanism of the dislocation glide should be identified. It is generally accepted that the properties of partial dislocations in semiconductors are determined by their core structure. The results presented below indicate that such relationship also exists for the partial dislocations in silicon carbide. The p-n diodes examined in this study were fabricated on a 35 mm diameter, 4H-SiC, n-type substrate (n=3x10^{18} cm^{-3}). The substrate was off-cut by 5° degrees from the [0001] toward the [11-20] direction and the diodes were processed on the silicon-face. The low-doped (n 10^{15} cm^{-3}) blocking layer (35 microns) and the p-type anode were deposited by horizontal hot-wall chemical vapor deposition method. Standard metal contacts were formed on the diode surface and substrate backside. Diode mesa were defined by reactive ion etching. Optical emission microscopy was applied to record the evolution of dislocations during the forward operation of the diodes. A liquid-nitrogen cooled, UV sensitive camera and an optical microscope mounted on a probe station were used. Pre-existing dislocations in the blocking layer could be imaged as bright spots and lines due to preferential recombination of electrons and holes along the dislocation line. The dislocations moved and stuck faults developed at high current bias with current densities between 0.1 and 10 A/cm². Their bounding partial dislocations showed two distinct characteristics. Bright luminescent segments were mobile while dark invisible ones were stationary. The core nature of the dislocation segments was determined by transmission electron microscopy. The locations of dislocation segments could be traced throughout the sample preparation by comparing the diode emission microscopy...
images with the optical micrographs of the sample taken in each step of preparation. Using this technique, we could uniquely correlate each partial dislocation observed in transmission electron microscopy with it recorded in optical emission microscopy. Burger's vector analyses performed with different techniques indicated that the mobile segments are silicon-core 30 degrees partial dislocations while the immobile segments are carbon-core 30 degrees ones.

15.28 Novel approach of 6H-SiC single crystal growth for diameter enlargement. Soo-Hyung Seo, Crystal Growth Division, Neosemsotech Corp., Inchon, South Korea.

Silicon carbide (SiC) grown by sublimation method is considered to be on wide bandgap semiconductor layers, typically 6H-SiC, and high-voltage power electronic devices and optical sensors in the ultraviolet range. Low defect and large diameter SiC crystals are necessary for development of SiC-based devices. From an industrial viewpoint, also the yield of the cut wafer is inefficient for device applications from now on and the enlargement of diameter from small seed to either 3 inches or 4 inches demands a long time. In this study, we demonstrate a novel approach for rapid enlargement of SiC crystal diameter. This method includes the assembling together several SiC seeds which are the precisely cut and crystallographically oriented single crystals plates along the well aligned pattern as a mosaic arrangement. In previous works, the successful growth of SiC crystal using an alternative mosaic arrangement has not been exhibited until now and this result has not still been reported in monograph. Consequently, we present the possibility and realization to outgrow the diameter of 6H-SiC crystals using mosaic arrangement. 6H-SiC (0001)-oriented seeds were precisely cut and they were attached on graphite lid as a mosaic arrangement. The various mosaic conditions were artificially considered for the evaluation of possible effects such as the widths of junctions, the misaligned angle and the rotated arrangement during the processes of seed attachment. The abrasive-grade SiC powder was etched in hydrogen chloride solution for removing metal impurities and was used for the source material. As-grown SiC surfaces and junction morphologies were investigated for step structures and the connected shape at junctions between seeds by using an optical microscopy with Nomarski interference contrast and AFM (atomic force microscopy). The connected properties of as-grown surface at junctions were improved under the high rotation pressure, narrow junction widths, and so on. Micro-Raman spectra for analysis of polytype formation at junctions are obtained at room temperature by Renishaw micro-Raman spectrometer (model 1000) attached to a optical microscopy. The excitation was carried out with the Ar laser (514nm, 25mW) focused on the 6H-SiC surface and the focusing beam size is about 2μm in diameter. From Raman spectra, the polytypes except 6H-SiC were not confirmed at junctions. Furthermore, the analysis data of the crystallographic and spectroscopic properties on the overgrowth at junctions are presented through employing high-resolution XRD, photoluminescence, FE-SEM (field emission scanning electron microscopy) to elucidate the growth behavior at junctions.

15.29 Photoluminescence at 1540 nm from erbium implanted amorphous silicon carbide films. Spyros Gallis1, Harry Efthathios1, Meng Bing Huang1, Ei Ei Nyein2, Uwe Hommerich and Alain E Kaloyeros2; 1School of NanoSciences and NanoEngineering, The University at ALBANY-SUNY, ALBANY, New York; 2Department of Physics, Hampton University, Hampton, Virginia.

Erbium (Er) implanted material systems have received significant attention, since the Er ion exhibits an optical transition around 1540 nm, a wavelength falling in the window of minimal absorption for silica optical fibers used in optical communications. In particular, implanting silicon carbide (SiC) with Er can further extend the applications of SiC as a high temperature optical source and enable technological use of the Er ion as a sensor. For example, Er-doped SiC has been studied as a candidate for infrared laser materials. Using an alternative mosaic arrangement has not been exhibited until now and this result has not still been reported in monograph.

The Silicon Carbide (SiC) is a potential semiconductor material to replace and out-perform the conventionally used silicon crystal in several electronic devices for high power and high frequency and high temperature applications because of its unique combination of properties such as high electric field break-down strength, high electron mobility and high thermal conductivity. Due to the phase equilibrium in the Si/C system, SiC cannot be grown from melt methods. Theoretically predicted temperature and pressure for atmospheric pressure growth of SiC is complex and difficult to optimize due to the fact that the operating temperatures are extreme (2100-2500 deg C) and monitoring and control are difficult (2,3). Since growth process occurs in almost air-tight graphite crucible and it is not feasible to observe the growing boule or determine experimentally the exact thermal conditions in the growth zone due to high operating temperatures and the opacity of the graphite crucible, the temperature field in the hot-zone has been predicted using numerical modeling. We have grown 6H SiC single crystals using PVT system designed and fabricated in our laboratory. A new seed mounting technique has been developed for holding the seed on the crucible lid. Crystals up to 50 mm diameter have been grown at atmospheric pressure using a crucible temperature of 2100-2200 deg C. The seed crystals and the grown bulk single crystals have been characterized using Nomarski, SWBXT and Etching techniques to understand the formation of micropipes during the growth. The details on crystal growth of 6H SiC and defects characterization will be presented. References: 1. Carter, Jr. C.H., Tvetkov, V.F., Glass, R.C., Henshall, D., Brady, M., Muller, St.G., Kordina, O., Irvine, K., Edmond, J.A., Kong, H.S., Singh, R., Allen, S.T. and Palmour, J.A., Progress in SiC: from Material Growth to Commercial Device Development, Mater. Sci. Eng., B61-62, 1-8, 1999. 2. G. Dhananjay, X.R. Huang M. Dudley, V. Prasad and R.H. M., Silicon Carbide Crystals: Part I: Crystal Growth and Characterization, chapter 6, p218-232, in Crystal Growth Technology, Ed. B.K. Byrappa, T. Ohachi, Springer with William Andrew, NY 2003. 3. Chen, Q.S., Prasad, V., Zhang, H. and Dudley, M., Silicon Carbide Crystals: Part II:Process Physics and Modeling,Chapter 7, p 233-269, in ibid.
Atomic Force Microscope Observations of Growth and Defects on As-Grown (111) 3C-SiC Mesa Surfaces. Philip G. Neudeck1, Andrew J. Trunek2 and J. Anthony Powell3; 1NASA Glenn Research Center, Cleveland, Ohio; 2OAI, Cleveland, Ohio; 3Seat, Inc., Cleveland, Ohio.

We have previously reported the step-free surface heteroepitaxy growth technology for obtaining high yields of 3C-SiC mesa heterofilms completely free of stacking fault defects [1,2]. However, only abbreviated atomic force microscope (AFM) data of as-grown 3C mesa film surfaces have been published to date [3]. This paper presents more extensive observations of as-grown (111) 3C-SiC mesa heterofilm surfaces by AFM. In nearly all cases, the as-grown (111) 3C-SiC mesa surfaces consist of a single bilayer height step. Macrosteps (i.e., step-bunching) were almost never observed. AFM also revealed some as-grown mesa surfaces in which sub-bilayer height line features with <111> orientation were superimposed across many single-bilayer height step patterns. Thermal oxidation of a selected 3C-SiC mesa confirmed the presence of stacking fault defects exactly corresponding to where line features were previously imaged by AFM in the as-grown film surface. Other small perturbations in the step structure of the film surface are attributed to the intersection of isolated threading edge or basal plane dislocations. AFM revealed that the morphology on the top (111) surface of 3C heterofilms varied as a function of growth conditions, film thickness, and film defect content. AFM of 3C-SiC film surfaces grown at temperatures below 1400 C exhibit clear evidence of two-dimensional (2D) terrace nucleation. In some regions, the terrace nucleation appears quite random. In other regions, terrace nucleation is enhanced by the presence of threading edge dislocation defects producing triangular growth hillocks on the 3C-SiC growth surface [2,3]. At higher growth temperatures, 2D nucleation on the top (111) surface becomes suppressed contributing to previously reported large differences in growth rate between mesas with and without stacking fault defects [3]. Experimental data (including AFM) suggests that 3C-SiC film growth becomes governed by growth on evolving facets at the edges of mesa crystals. Because the edge facet surfaces have higher chemical bond density than the top (111) surface, the facet surfaces are hypothesized to support more rapid crystal growth. [1] P. Neudeck et al., Mat. Sci. Forum 389-393 (2002) p. 311; [2] P. Neudeck et al., to appear in Silicon Carbide and Related Materials 2003; [3] A. Trunek et al., to appear in Silicon Carbide and Related Materials 2003.

Fabrication of Desk-Top Type Ion Implanter for SiC Device Application. Satoshi Furukawa1, Yasuhiro Nakata2, Yuji Horino3, Yoshinori Hosokawa4 and Shigehiro Nakano5; 1Department of Electronics and Information Science, Kyoto Institute of Technology, Kyoto, Kyoto, Japan; 23C Semicon Corp., Osaka, Japan; 3AIST, Osaka, Japan; 4X-ray Precision Ltd., Kyoto, Japan.

Ion implantation is a key technology for SiC devices. Generally, implantation is carried out using large scale ion implanter, however, small scale implanter has a lot of merit in the field of SiC devices. We made desk-top type ion implanter which consists of PIG ion source, small acceleration tube, mass separation by Wine filter and chamber for sample stage. We already applied this machine to 4H-SiC devices. Carrier concentration of the epilayer of 4H-SiC substrates was 2E15 cm-3. Edge termination of PIGB was made using Ar ion with acceleration voltage (Va) of 10 KeV and high resistive amorphous layer was made around Schottky barrier metal. Dose of Ar was 1E16 cm-2. Amorphous state of the implanted region was confirmed by RHEED pattern. Implanted layer was also examined by IR reflection measurement. Without edge termination, break down voltage was 600 V, but after edge termination by Ar implantation, break down voltage increased to 1000 V. Diameter of the metal was 0.5 mm to make a pn junction, nitrogen ion was implanted with Va of 30 KeV to p-type substrate. Carrier concentration of the p-layer was 2E15 cm-3. After high temperature annealing, pn junction was formed. Typical diode characteristics were obtained. To make a pn junction, boron ion was made using BC solid and B ion was implanted into n-type epilayer. Characteristics of the diodes is discussed.

SESSION J6: Extended Defect Characterization I

Chair: M. Dudley
Thursday Morning, April 15, 2004
Room 2009 (Moscone West)

8:30 AM *J6.1
Microstructural Aspects and Mechanism of Degradation of 4H-SiC PIN Diodes under Forward Biasing. Pirouz Pirouz2

Devices fabricated from the wide bandgap semiconductor SiC have many advantages over those made from conventional semiconductors. Thus, performance characteristics of some 4H-SiC devices can be two or more orders of magnitude better than the equivalent devices made from silicon. On the other hand, many unexpected problems have crept up with the operation of some SiC devices that need to be understood and solved before further progress can be made in this area. One of the most intriguing problems has been the degradation of n-p-n PIN diodes that, because of conductivity modulation and lower on-resistance, have many advantages over unipolar Schottky barrier diodes at high blocking voltages. The electrical degradation of the diode was noticed after prolonged reliability tests and refers to a drop in voltage under extended forward current operation. The degradation appears to be associated with the appearance of stacking faults in the entire base region of the diode. The formation of the stacking fault is one of the many puzzling aspects of stacking fault formation in such diodes. Electroluminescence as well as TEM has been used to investigate the degradation problem and, based on experimental results, the formation of partial dislocations within the device, their enhanced motion under electron-hole recombination and the possible sources of partial dislocations will be considered.

9:00 AM J6.2
Thermoplastic Deformation and Residual Stress Topography of 4H- and 6H-SiC Wafers. Robert S Okoje1, Ming Zhang2 and Pirouz Pirouz2; 1Sensors and Electronics Branch, NASA Glenn Research Center, Cleveland, Ohio; 2Department of Mater. Sci. & Eng., CWRU, Cleveland, Ohio.

Optical reflectometry was used to measure stress relaxation via thermoplastic deformation in as-received 4H- and 6H-SiC substrates. Thermoplastic deformation was characterized using 3D mapping features, or contour maps, to locate differences in wafer bow or wafer warp across the surface. In all cases, during thermal excursion to 900 C in vacuum, the radii of curvature of the substrates increased (i.e., the wafers became flatter) with increasing temperature starting from 350 C. This change in curvature corresponded to a relaxation of the residual stress in the substrates. Upon cooling down to room temperature, the radii of curvature of all the substrates retained their high-temperature (900 C) values, thus exhibiting thermoplastic inelastic behavior. Further cyclic excursion to 900 C did not yield any significant changes in the curvature, thus indicating that the changes from the first anneal were irreversible. The change in internal stress following thermoplastic deformation at 900 C in vacuum was estimated to be greater than 0.7 GPa with an activation energy of deformation of 3.1±0.8 eV. Subsequent measurements of residual stresses were performed on n-type 4H-SiC epilayers with different nitrogen-doping level that were grown homoepitaxially on the n- or p-type 4H-SiC substrates relaxed by thermal anneal in nitrogen at 1150 C prior to growth. The 3D stress measurements on the as-grown epilayer on the substrate indicated the existence of compressive stresses in the epilayers. The samples were further annealed at 1150 C in nitrogen for thirty minutes and their microstructure was investigated by transmission electron microscopy (TEM), specifically to look for the possible generation of stacking faults (SFs). TEM investigations revealed dense SFs bands in annealed 4H-SiC epilayers, which had an n-type epilayer doping as low as 5 x 1015 cm-3. This epilayer doping level is approximately two orders of magnitude below the reported threshold value (3 x 1016 cm-3) previously suggested for the onset of the generation of SFs in annealed epilayers. This work provides evidence for the existence of significant compressive stresses in 4H-SiC epilayers. Thus, it is possible that stacking faults and SFs bands observed in many recent experiments are due to the motion of pre-existing partial dislocations.

9:15 AM J6.3
The Driving Force of Stacking Fault Formation in Silicon Carbide p-n-i-Diodes. Seoyong Ha1, Marek Skowronski2, Joseph Sumakeris2 and Michael Paisley2; 1Carnegie Mellon University, Pittsburgh, Pennsylvania; 2Cree, Inc, Durham, North Carolina.

The driving force of stacking fault formation in 4H silicon carbide p-n-i diodes has been investigated using optical emission microscopy and transmission electron microscopy. The forward voltage drop has been observed to increase with time due to expansion of single-layer Shockley-type stacking faults in the blocking layer. It has been suggested that the phenomenon is driven by a mechanical stress in the epilayer/substrate structure. The results presented below indicate that stress cannot be the driving force. The p-n-i diodes examined in this study were fabricated on 3 inch diameter, 4H-SiC, n-type substrates (n > 8 X 1018 cm-3). The substrates were off-cut by 8 degrees from the [0001] toward the [1[1-20] direction and the diodes were processed on the silicon-face. The low-doped (n > 1015 cm-3) blocking layer (30 nm) and the p-type anode were deposited by chemical vapor deposition technique. The substrate temperature during anodic oxidation was in the range of 1100 C. The p-n-i diodes were fabricated at 100 degrees C and annealed in nitrogen at 1150 C for 30 seconds in anode contact area.
deposition. Standard metal contacts were formed on the diode surface and substrate backside. Diode mesa were defined by reactive ion etching. The partial dislocation motion was recorded by optical emission microscopy during the diode operation. The deformed diodes were analyzed by transmission electron microscopy in order to determine the Burgers vector and the line direction of the partial dislocations. From these dislocation characteristics, one can deduce the type of the shear stress driving the fault expansion. The stress direction was determined for over 20 different partial dislocations. The partial dislocations moved as if there were positive as well as negative shear stresses in the blocking layer of the single diode. We also have observed several examples of two partials with the same sign of Burgers vector moving in opposite directions within several microns of each other. This could not be explained by stress either uniform or local in nature. These dislocations indicate that the stacking fault expansion in diodes under forward bias is inconsistent with a stress acting as the driving force. This argument leaves the thermodynamic energy difference between the perfect and the faulted structure as the only plausible driving force. In other words, 4H-SiC crystals are metastable at room temperature and would convert spontaneously into faulted structure. For such process to occur, however, the nucleation sites and the activation energy in the form of electron-hole recombination are needed. At this point, the best approach to elimination of the junction degradation appears to be control of pre-existing defects serving as nucleation sites.

9:30 AM *J6.4
Mechanisms of Stacking Fault Growth in SiC PIN Diodes.
R. E. Stahlbush, Naval Research Laboratory, Washington, District of Columbia.

Power devices fabricated in SiC offer many advantages over their present-day Si counterparts. However, SiC technology is not as mature and there are outstanding material and processing problems that need to be resolved. One of the most significant material problems is the formation of stacking faults (SFs) during forward-biased operation of bipolar devices. The stacking faults degrade the minority carrier lifetimes and increase the forward voltage drop Vf. Furthermore, the formation of stacking faults is erratic. For example, PIN diodes from the same wafer can have Vf drifts that vary more than order of magnitude. While some of the mechanisms of the degradation are understood, others remain unclear. It is known that electron-hole recombination is necessary to provide the local energy for moving the partial dislocations that bound the SFs. It is also clear that there must be nucleation sites where SF growth starts. The recombination overcomes the energy barrier to SF growth possible. The thermodynamic driving forces are less clear; three have been proposed. The first is lowering of the electronic energy as electrons fall into the quantum wells formed by the SFs. The second is relief of mechanical stress, and the last is the preference near room temperature for the 3C polytype over the 4H polytype. Studying the SF growth dynamics by light emission imaging provides insight into these open questions. Nucleation sites are distributed throughout the diode drift region and many of them originate from faulting of basal plane dislocations present after the epitaxial growth. The SF growth patterns can also distinguish among the possible driving forces. The electronic energy lowering can be neglected while nonuniform stress appears to play a significant role and the 3C polytype preference may also be contributing to the drive force.

SESSION J7: Extended Defect Characterization II
Thursday, April 15, 2004
Room 2009 (Moscone West)

10:30 AM *J7.1
Extended Defects in SiC Substrates and Epilayers.
Marc Skowronska, Carnegie Mellon University, Pittsburgh, Pennsylvania.

The driving force behind the development of silicon carbide technology is the potential for major energy savings due to use of high voltage switching devices. The first of such devices, namely Schottky diode rated for up to 1.2 kV, is already available commercially. However, the development of high voltage bipolar devices still faces numerous challenges. From the materials point of view, this is possible the most demanding application requiring utmost in doping control, low extended defect densities, and long carrier diffusion lengths. This presentation will focus on extended defects in SiC substrates and epitaxial layers and will describe their morphology and allure to their origin. The sources of three types of dislocations silicon carbide wafers will be discussed. The elementary screw dislocations are either inherited from the seed crystal or nucleate at the initial stage of growth on basal plane surfaces. They serve as step sources on the surfaces of boules and determine the stacking sequence. Threading edge dislocations are mostly grown-in but some evidence suggests possibility of prismatic slip. These dislocations appear to be mobile at high temperatures and undergo partial polygonization forming low angle grain boundaries. The partial dislocations are mostly grown-in but some evidence suggests that the stacking fault expansion in diodes under forward bias is inconsistent with a stress acting as the driving force. This argument leaves the thermodynamic energy difference between the perfect and the faulted structure as the only plausible driving force. In other words, 4H-SiC crystals are metastable at room temperature and would convert spontaneously into faulted structure. For such process to occur, however, the nucleation sites and the activation energy in the form of electron-hole recombination are needed. At this point, the best approach to elimination of the junction degradation appears to be control of pre-existing defects serving as nucleation sites.

11:00 AM J7.2
First Direct Measurements of Dynamic Constants of Dislocations Introduced in (11-20) 4H-SiC by X-Ray Diffraction.
Maryse Lancin1, Joel Douzn2, Gabrielle Regalin3 and Bernard Pichaud1.
1TCESEN, University III, Marseille, France; 2LEM, CNRS-ONERA, Chatillon cedex-20, France.

Despite the essential role of dislocations and the increasing importance of silicon carbide in the high-power electronic industry, no direct experimental values on either perfect or partial dislocations velocity in SiC have been published so far, whatever their core.

Nevertheless, transmission electron microscopy (TEM) observations show that partial dislocations with silicon core have a higher mobility than those with a carbon core. This is actually in contradiction with ab initio calculations which demonstrate that partials containing core Si atoms are strongly reconstructed whereas partials containing core C atoms are more weakly reconstructed indicating that the latter partials are more mobile. The purpose of this work is to derive the stress exponent m and the activation energy Q of dislocation velocity [1] from introducing and developing fresh dislocation by cantilever bending in as-received high quality (11-20) 4H-SiC. V = A(1 - exp(-Q/kT)) [1] A is a constant and s is the resolved shear stress in the gliding basal plane. The wafer orientation is selected because of its most suitable geometry for deformation (high Schmid factor). The stress along the sample length is measured by determining the local radius of curvature. The plastic deformations are carried out at temperatures ranging from 823K to 1333K under neutral atmosphere. The dislocation propagation distance and the mechanical stop of the dislocation by transmission Topography (XRTT) or chemical etching. In addition, TEM studies are carried out to characterize the Burger's vector and the dislocation cores. XRTT observations and chemical etching reveal straight lines parallel to the basal plane with asymmetric location as compared to the position of the nucleation centres (edges or scratches of the samples). These lines correspond to faulted half loops consisting of i) one 90 Shockley partial dislocation with a carbon core, parallel to the surface and located close to the neutral plane at half the thickness of the sample and ii) two 30 Shockley partial dislocations with a silicon core, one of them emerging at the sample surface and the other linked to the 30 Shockley partial dislocation with a carbon core bending to the dislocation segment. The observed stresses derive from the low mobility, if any, of the 30 Shockley partial dislocation with a carbon core. We will give the first set of curves of dislocation velocities as a function of temperature and as a function of the resolved shear stress in 4H-SiC for a temperature range below 1273K.

11:15 AM J7.3
Characterization of SiC epilayers using high-resolution X-ray diffraction and synchrotron topography imaging.
Xiaorong Huang1, Michael Dudley1, Wondong Cho2 and Robert S Okoije2.
1Dept. of Materials Sci. & Eng., Stony Brook University, Stony Brook, New York; 2NASA Glenn Research Center, Cleveland, Ohio.

A series of advanced X-ray diffraction and imaging techniques, including double-axis HRXRD, triple-axis diffraction, reciprocal space mapping (RSM), and synchrotron white-beam X-ray topography (SWXRT) are used to investigate the extremely small lattice mismatch and misorientation in n-type 4H SiC epilayers grown homoepitaxially on p-type 4H SiC. It is found that the basal planes of the doped epilayers are usually tilted against those of the substrate (around 50 seconds). Using triple-axis RSM, we successfully separate the contribution of lattice tilts from that of lattice constant variation in the diffraction pattern. The dependence of the lattice constant and crystalline quality of the epilayer on different doping levels and annealing treatments is thus accurately obtained. The doping-induced lattice constant variation is attributed to the substitutional nitrogen incorporated preferentially in the host carbon site. Annealing can also change the lattice parameters due to the generation of stacking faults in 4H SiC epilayer.

11:30 AM J7.4
Optical Studies of Porous GaN/SiC and GaN/porous SiC
Results of optical studies of porous GaN/SiC structures and single- and multi-layer GaN-based structures grown on porous SiC (SC) substrates are presented. In porous GaN/SiC structures, the most remarkable feature is strong photoresponse (PS) in visible part of the spectrum. This feature demonstrates peculiarities typical of persistent photoconductivity effect in GaN, including non-exponential decay with characteristic times of thousands of seconds. Detailed PS, photoluminescence and electron microscopy studies allowed us to relate the PS to trapping/detrapping processes at the SiO2/SiC interface in porous GaN/SiC structures. On single GaN epitaxial layers grown on SC substrates, a PL study was performed. It appeared that layers grown on SC substrates demonstrated increased PL intensity in comparison to layers grown on non-porous SC substrates. All peaks were blue shifted by approximately the same amount; this indicates that a mechanism of the increase is a reduction in density of non-radiative recombinative centers in the layers grown on SC. As a result, the PS of GaN layers is related to the density of non-radiative recombinative centers in SiC layers grown on SC substrates, and the surface orientation can be related to the density of non-radiative recombinative centers in SiC layers grown on SC substrates. Finally, results of electroluminescence (EL) measurements on a DH GaN/AlGaN LED with mobility gap are presented. Luminescence properties of GaN layers and GaN-based device structures are used to discuss the advantages of epitaxial growth on porous substrates.

SESSION J8: MOS Structures
Thursday Afternoon, April 15, 2004
Room 209 (Moscone West)

1:30 PM *J8.1
Comparison of electrical properties for MOS structures fabricated on the 4H-SiC (0001), (11-20), (000-1) faces.
Koji Fukuda, Power Electronics Research Center, National Institute of Advanced Industrial Science and Technology, Tsukuba, Ibaraki, Japan.

SiC MOSFET is expected to be available for next-generation switching devices. However, at present, the on-resistance (Ron) of the SiC power MOSFET is much higher than the theoretical value of SiC, the performance of SiC is not sufficiently demonstrated. This is attributed to several defects at the SiO2/SiC interface, and to the presence of self-passivated traps at the SiO2/SiC interface, which leads to difficulties with respect to the current flow. A channel mobility 100-200 cm2/Vs is required for the realization of the SiC power MOSFET, with the limitation of Ron for SiC. However, the inversion channel mobility is much higher than the channel mobility is necessary. Gate oxide reliability is also very severe problem for the realization of SiC power MOSFET. The oxidation rate strongly depends on the surface orientation. It is considered that optimum gate oxidation condition changes with the surface orientation. We are investigating techniques by which to systematically improve the interface trap density (Dit), the inversion channel mobility, gate oxide reliability such as TSSD, TDDJ, hot-carrier degradation and the Ron of lateral recess MOSFET for the (0001) face, the (11-20) face and the (000-1) face. We have reported that the inversion channel mobility of SiC MOSFET fabricated on the (0001) face was increased using pyrogenic re-oxidation, that the Dit and the inversion channel mobility of MOS structures fabricated on the (11-20) face and (000-1) face was much improved using pyrogenic gate oxidation followed by hydrogen post annealing (POA), which resulting in the peak value of inversion channel mobility of 160 cm2/Vs and 127 cm2/Vs, respectively.

2:00 PM *J8.2 MOS Interface Properties and MOSFET Performance on 4H-SiC (0001) and Non-Basal Faces Processed by N2O Oxidation.
John Palmour; Cree Inc, Durham, North Carolina.

Although silicon carbide (SiC) MOSFETs are recognized as ideal power switches, SiC MOSFETs have suffered from low effective channel mobility. In recent years, N2O oxidation has been proposed to improve SiO2/4H-SiC(0001) interface properties and thereby to increase effective channel mobility of MOSFETs. Recent investigations have revealed that 4H-SiC(0001) and non-basal faces such as (11-20) and (03-38) possess much potential to further improve the quality of MOS structure. In this study, characterization and MOSFET fabrication have been investigated on 4H-SiC(0001), (11-20), and (03-38) by using N2O oxidation. The oxidation has been performed in N2-diluted N2O at 1300°C. The thermal oxide thickness was 50-70 nm. The crystal face dependence of oxidation rate was also studied. In MOSFET fabrication, planar inversion-type MOSFETs were processed on p-type epilayers doped to 1E16-1E17 cm-3 to investigate the influence of p-body doping on SiC MOSFET performance. The source/drain regions were formed by high dose phosphorus ion implantation followed by annealing at 1000°C. The interface state density (Dit) was estimated by low- and high-frequency C-V curves of n-type MOS capacitors. Although the Dit for the 4H-SiC(0001) MOS structure showed a rapid increase near the conduction band edge, the MOS structures on the other faces exhibit a rather flat Dit distribution. The 0.2 eV is well below 1E2 cm-2eV-1. The effective channel mobility of the (0001) MOSFET remained 18-24 cm2/Vs. However, (11-20) and (11-20) MOSFETs showed much higher mobilities of 50-62 cm2/Vs and 50-62 cm2/Vs, respectively, for p-body-type epilayers. It should be noted that the (11-20) MOSFET showed a reasonably high mobility of 56 cm2/Vs even on epilayers with an acceptor concentration of 2E17 cm-3, which is more realistic for power MOSFET fabrication. On the other hand, the mobilities of (0001) MOSFET significantly decreased to 12 cm2/Vs by increasing the p-body doping. The crystal face/p-body doping dependencies of channel mobility is discussed. Although rapid progress has been made on SiC (0001) MOSFETs, power MOSFETs on (0001) trench MOSFETs with the (11-20) sidewalls is promising in the future.

2:15 PM *J8.3 Interface Trap Defects Observed in 6H SiC Metal Oxide
Semiconductor Field Effect Transistors via Spin Dependent Recombination.
David J. Meyer1, Morgan S. Dautrich1, Patrick Lenahan1 and Aivars Lelis2; Engineering Science and Mechanics, The Pennsylvania State University, University Park, Pennsylvania, 1U.S. Army Research Laboratory, Adelphi, Maryland.

We utilize a particularly sensitive form of electron spin resonance (ESR) signal spin dependent recombination (SDR) to observe deep level defect defects at or near the interface of 6H SiC and the SiO2 gate dielectric in SiC MOSFETs. We find that the SDR response is strongly correlated to SiC/SiO2 interface recombination currents and also find that the magnitude of the SDR response is correlated with processing induced changes in interface trap density, an extremely strong indication that we are observing the dominating interface/near interface trapping defects. The SDR response is extremely large, as large as one part in 350. To the best of our knowledge, this is the largest SDR signal on a semiconductor device at room temperature. To the best of our knowledge, this is the first observation of SDR in a SiC MOSFET and arguably the first direct observation via magnetic resonance of a defect certain to be involved in traps in SiC MOSFETs. Investigation about two axes demonstrates that the g-tensor is isotropic and g = 2.0027 for all orientations. In addition to observation of the strong center line, we also observe weaker superhyperfine and hyperfine side peaks. The superhyperfine peaks are almost certainly associated with nuclear magnetic moments of 28Si, the hyperfine peaks are associated with 13C. These results quite strongly suggest that the defect under study involves a silicon vacancy site. We are presently adding conventional ESR measurements as a function of gate bias to provide a fuller description of the electronic properties of these defects.

2:30 PM *J8.4 Reliability of Nitried Oxides in N- and P-type 4H-SiC MOS Structures.
Sumi Krishnaswami, Mininal Das, Ananta Agarwall and John Palmour; Cree Inc, Durham, North Carolina.

One of the attractive features of MOS-based silicon carbide devices is their potential use for high temperature and high power applications. Earlier problems with high interface trap density (D1T) and low mobility on (0001) 4H-SiC MOS structures have been overcome via nitridation annealing with D1T reported as low as 1E11 cm-2 eV-1 near Ec and mobility approaching 100 cm2/Vs/1. However, the use of such devices will ultimately be limited by oxide integrity and reliability. This paper presents high temperature time dependent dielectric breakdown (TDDB) results from both n-type and p-type MOS capacitors with thermal oxides grown under different nitridation conditions. Reliability measurements on n-type MOS capacitors biased into strong n-type conduction enable us to evaluate the oxide integrity under electron injection from the semiconductor where the barrier is relatively low due to the wide 4H-SiC bandgap. This emulates the on-state mode of operation thereby predicting the maximum allowable gate voltage (i.e., the minimum on-resistance). Reliability measurements on p-type MOS capacitors in the other...
hand, predicts the maximum allowable field in the semiconductor (i.e., the maximum blocking voltage) by simulating the oxide stress during the MOSFET blocking mode of operation which is governed by hole injection. TDDM measurements of MOS capacitors (120 °C dry oxide with 1300 °C N2O anneal) were performed at 175 °C and 300 °C under high positive bias stress. The devices are biased into strong accumulation mode such that the field in the oxide is high enough to collect breakdown data in a reasonable period of time. We observe that at 175 °C, a 100-year MTTF is obtained if the field in the oxide is kept below 6.5 MV/cm. The TDDM measurement has also been performed at 300 °C where lifetime has been reduced by a few orders of magnitude. Recent reliability results on similarly oxidized MOSFETs have shown failures along the same trend as the n-type capacitors, indicating that MOSFETs and MOS capacitors can have similar reliability despite inherent processing and structural differences. PMOS capacitors fabricated with the aforementioned dry + N2O process as well as capacitors fabricated using the low DyT4 introduction technique were evaluated [4], [5]. Das, “Recent Advances in (2001) 4H-SiC MOS Devices,” International Conference on Silicon Carbide and Related Materials, Lyon, France, October, 2003. [2] G. Godnjornsson, H.O. Olafsson, E. O. Svennhjornsson, ”Enhancement of inversion channel mobility in 4H-SiC MOSFETs using a gate oxide grown in nitrous oxide (N2O).” International Conference on Silicon Carbide and Related Materials, Lyon, France, October, 2003.

2:45 PM J18.5

Electronic devices based on single crystal silicon carbide represent a good choice for fast, high frequency and high power devices for use as sensors, switches, pressure devices and control electronics in high temperature applications such as inside fuel cells. The challenge is to develop a package that is resistant to thermal degradation in harsh environments. The package must protect the die and allow it to maintain functionality for durations of at least 1000 hours. Elevated temperatures place severe loads on both the device and package. The thermal cycle is extreme and this all but rules out many of the materials and materials systems. Polycrystalline silicon carbide is the material that we have chosen to study as a suitable package and materials suitability/compatibility has been considered on several levels. The packaging must be able to withstand prolonged exposure to harsh environments. We have demonstrated that quenching polycrystalline SiC can reduce fracture toughness and we have used indentation methods to determine the effect of thermal cycling on the mechanical properties of SiC. Sealing the package would be accomplished using a glass. The seal must be mechanically strong and hermetic. The maximum processing temperature for package joining using SiC electronics is 1088 °C and the package should operate up to 1000 °C. This requirement is in contrast to that of thermodynamic stability place severe restrictions on the glass. We will describe our results in selecting suitable glasses for this application. Electrical connections between the device and package are required to be ohmic and stable. This includes metal wire bond oxide growth, with rates up to 700 Å per minute. The wire must be stable at high temperatures and resistant to thermal cycling. The bonding system that we will describe uses diffusion and transient liquid phase bonding. A copper interlayer is used to form a bond between the metal tungsten pads and the nickel wire lead. This method has produced some very promising results in recent long-term aging studies.

SESSION J9: Growth and Characterization Thursday Afternoon, April 15, 2004 Room 209 (Moscone West)

3:30 PM J19.1
Device Critical Defects in SiC. Peder Bergman, Christer Hallin, Luitaurus Storasta, Bjorn Magnusson and Erik Janzen; Department of Physics and Materials Technology, Linkoping University, 58183 Linkoping, Sweden.

SiC devices, such as schottky barrier diodes and MOSFET, are today available for different applications. Further development also in other applications requires improved material quality. Both in order to make the devices functional, but also for improved yield and general performance. Critical defects are today structural defects such as micropipes, stacking faults and dislocations. But also the role and influence of point defects, both impurities and intrinsic defects, remains to be understood. In this presentation we will review known properties and influence of these defects. In particularly the properties of dislocations, the properties and influence on point defects on for example carrier lifetime, and the role of intrinsic defects both as recombination centers and as responsible for semi insulating properties of high purity material.

4:00 PM J9.2
A correlation between implantation induced defects and dopant profiles in p implanted (0001) and (11-20) oriented 4H-SiC. Jennifer Wong-Leong1, Margareta K. Linarsson2 and Bengt Gunnar Svensson3; 1Dept. of Electronic Materials Engineering, Australian National University, Canberra, Australian Capital Territory, Australia; 2Solid State Electronics, Department of Microelectronics and Information Technology, Royal Institute of Technology, Kista-Stockholm, Sweden; 3Department of Physics/Physical Electronics, University of Oslo, Oslo, Norway.

In this study, both (11-20) and (0001) n-type 4H-SiC substrates were implanted with 400 keV P and then annealed at different temperatures namely 1300°C and 1700°C. The various samples, both as implanted and annealed, were studied by secondary ion mass spectrometry (SIMS), Rutherford backscattering spectroscopy (RBS-C) and transmission electron microscopy (TEM) to understand the damage evolution and defect structures resulting from different crystal orientations and different implantation damage. TEM analysis of the (0001) wafer shows the presence of precipitates close to the loops. The (11-20) wafer showed some larger voids faceted on the (1-100) planes, some loops with basal plane as habit plane and other loops with the (11-10) habit plane. Some elongated loops the impact ionization coefficients were observed to be pinnned by precipitates. SIMS profiles show in some cases distinct differences between the two crystal directions. A comparison between the TEM and the SIMS results suggests a relation between the accumulation of P at certain and precipitation close to dislocation loops.

4:15 PM J9.3
Comprehensive Study of Impact Ionization Coefficients of 4H-SiC. Tetsuo Hatakeyama1, Takatshi Watanabe1, Kazuomi Kojima2, Nobuyuki San3, Takashi Shinoh1 and Kaza Arai2; 1Corporate R&D Center, Toshiba corporation, Kawasaki, Japan; 2Power Electronics Research Center, National Institute of Advanced Industrial Science and Technology, Tsukuba, Japan; 3Institute of Applied Physics, University of Tsukuba, Tsukuba, Japan.

Impact ionization coefficients are important physical properties for power devices, because avalanche breakdown caused by impact ionization limits the voltage blocking capabilities of a power device. However, our knowledge of the impact ionization coefficient of 4H-SiC is limited, and the reported coefficients differ one another. Further, anisotropy of breakdown field of 4H-SiC was reported and it was shown that there is a significant reduction of the breakdown field when the electric field is applied perpendicular to the c-direction. In order to understand avalanche breakdown behavior of 4H-SiC power devices, reliable parameter sets of impact ionization coefficients are needed. In this talk, we present the parameter sets of impact ionization coefficients of 4H-SiC for <0001> and <11-20> directions that reproduce avalanche breakdown behavior of p+n diodes on (0001) and (11-20) epitaxial 4H-SiC wafers. The impact ionization coefficients show large anisotropy; the breakdown voltage of a p+n diode on (11-20) wafer is 60% of that on (0001) wafer. We also discuss the origin of anisotropy of impact ionization coefficient of 4H-SiC based on the microscopic description of the breakdown and the transport physics under high electric field; impact ionization coefficients can be obtained by integrating the product of impact ionization scattering rate, the distribution function and density of state. Impact ionization rate and density of state are independent of electric field. Distribution function varies according to a carrier temperature, and carrier temperature is proportional to saturation velocity and electric field. Saturation velocity varies according to the dimension of the electric field, in general. Thus, the anisotropy of the impact ionization coefficients is attributable to the anisotropy of the electron density originated from the electronic structure of 4H-SiC. The experimental results of the anisotropic saturation velocity and temperature coefficients of impact ionization coefficients will be presented at the meeting.

4:30 PM J9.4
Growth and Metrology of Silicon Oxides on Silicon Carbide. Andrew M Hoff, Nanomaterials and Nanomanufacturing Research Center, University of South Florida, Tampa, Florida.

Thermal oxidation of SiC by the afterglow method has opened new pathways of opportunity to address both thin film growth and defects that hinder electronic device development with this important semiconductor material. In this presentation we will review known properties and influence of these defects. In particularly the properties of dislocations, the properties and influence on point defects on for example carrier lifetime, and the role of intrinsic defects both as recombination centers and as responsible for semi insulating properties of high purity material.
non-contact charge-voltage (Q-V) metrology approach. This instrument employs a combination of incremental contact potential difference values obtained in response to applied corona charge generated from air. The slope of the Q-V characteristic within a bias range corresponding to accumulation of the semiconductor provides an effective dielectric permittivity value for the grown film. Effective permittivity values for afterglow oxides grown on SiC approach that of SiO$_2$ grown on silicon substrates whereas the values for oxides grown on SiC in an atmospheric steam oxidation process are always depressed relative to SiO$_2$ on silicon, indicating that the latter process always produces low-k oxides. A mechanistic discussion regarding these observed differences between the two oxidation methods is presented along with suggestions for an integrated process and metrology approach to reduce defects in oxide films on SiC.