SYMPOSIUM B
Silicon Materials—Processing, Characterization, and Reliability
April 1 – 5, 2002

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*Invited paper
TUTORIAL

B: INTEGRATED CIRCUIT FABRICATION AND YIELD CONTROL
Monday, April 1, 2002
8:00 a.m. - 12:00 p.m.
Salon 11/12 (Marriott)

This course, starting from buying the wafer up to the final interconnect structure made by Cu wire, discusses techniques in a step-by-step fashion. Yet, logic circuits are built and what are the associated yield control/metrology steps encountered during the build. The build basics which are applicable to any state of the art facility will be described in such detail that the student will understand the reason for each step, and the logic of the sequence used, as well as systematic and random defects encountered.

Additionally, a discussion of an active yield control strategy is described taking into account the impact of design, process metrics, and tools, use of CD, overlay and AFM, both now and in the near future. Cross sections, top down defect appearance, etc., at each step will be used to illustrate the build process and the defects found. The instructor, Professor Ernest Levine of the School of Nanosciences and Nanoengineering of the University of Albany, has spent 24 years working in the field which will be explored in this tutorial.

Instructor: Ernest Levine, SUNY-Albany

SESSION B1: SILICON MATERIALS AND PROCESSING
Chair: Janice L. Veteran

Monday Afternoon, April 1, 2002
Salon 16L2 (Marriott)

1:15 PM B1.1
SUPPRESSION OF PARASITIC BJTs ACTION IN SINGLE POCKET THIN FILM DEEP SUB-MICRON SOI MOSFETS.
Najeebuddin, Anish Kumar, Mohan V. Dungo, V. Ramgopal Rao, J. Vasis, Dept of Electrical Engineering, Indian Institute of Technology, Bombay, INDIA

A study of parasitic bipolar junction transistor effects in Single Pocket (SP) thin-film SOI n-MOSFETs is reported. Characterization and simulation results show that parasitic BJTs action is suppressed in SP-SOI MOSFETs when compared to the conventional (CON) SOI technologies. SP-SOI MOSFETs used in this study are fabricated by the standard CMOS process, except the Vth implant is done after the poly-silicon gate patterning. Pocket implant is done from the source side. Both the CON and SP-SOI MOSFETs are fabricated on the same wafer with channel lengths down to 10nm, and with different silicon film thicknesses, 35, 50 and 65nm. The gate oxide thickness for all the MOSFETS is 3.9 nm. Gate-Induced Drain-Leakage (GIDL) current has been used for characterization of parasitic BJTs gain. GIDL current is independent of channel length and depends on the area of gate-drain overlap region and the electric field within it. At high drain biases, when impact ionization is high, the impact generated electrons flow towards the drain while the holes lead to charging of the body in SOI. In long channel devices these holes recombine before reaching the source, whereas in short channel devices the hole current gets amplified by the factor $\beta$ (BJT gain) depending upon the base width (channel length). This amplified current gets added to the drain current. By taking the ratio of currents in short channel to long channel device, we can estimate the value of $\beta$ for the parasitic BJT. The experimentally evaluated value of $\beta$ for the parasitic BJT in deep sub-micron SOI devices is found to be an order of magnitude lower as compared to the CON SOI technologies. The suppression of parasitic BJTs effect in SP-SOI devices is also analyzed from detailed 2-D simulations and calculated for lower electric field near the drain junction. Further insight is gained by detailed process and device simulations using an accurate BJTs structure with similar technology parameters as in SP-SOIs. The results obtained from simulations excellently corroborate the experimental findings.

1:30 PM B1.2
MICROSTRUCTURAL EVOLUTION AND DEFECTS IN ULTRA-ThIN SIMOX MATERIALS DURING ANNEALING. Jun Sk. Jeong, Rachel Evans, and Sipanjan Sengpliyun, The University of Arizona, Department of Materials Science and Engineering, Tucson, AZ.

Ultra-thin SIMOX processes are creating increased interest as a long-term solution for ULSI due to its advantages: low cost, better heat dissipation, and short channel effect over standard SIMOX. Ultra-thin SIMOX materials were prepared by implantation of the oxygen ions into p-type (100) Si wafers at an implantation energy of 65 keV and 100 keV with a dose range of 2.0 - 8.0 $\times$ $10^{15}$ O+ cm$^{-2}$ using an 8160 high-current oxygen implanter. As-implanted wafers were subsequently annealed at 1100°C, 1200°C, 1300°C and 1350°C each for 0 hrs and 4 hrs in an Ar (+1%O$_2$) atmosphere. Microstructural evolution, oxygen redistribution and crystalline quality of the Si films of SIMOX structure after post implantation thermal ramping and high temperature annealing were characterized using a Transmission Electron Microscope (TEM), Rutherford Backscattering Spectroscopy (RBS), and Auger Electron Spectroscopy (AES). The defect microstructures and their evolution upon high temperature annealing were investigated using XTEM and PTEM. The density of the Si-rich films of ultrathin Si$_3$O$_7$X were measured using an optical microscope after a chemical etching. Results of the micro-structural analysis shows that a dose range of 3.0 - 3.5 x $10^{15}$ O+ cm$^{-2}$ at an implantation energy of 100 keV produces a silicon island-free continuous buried oxide layer (BOL) after 1350°C and 4 hrs annealing. The thickness of silicon overlayer and BOX layer was about 10 nm and 15 nm respectively. The effects of a strong electric field and dose on defect density in a fully annealed SIMOX are discussed.

1:45 PM B1.3
X-RAY REFLECTIVITY STUDY OF EXOTIC MATERIALS FOR ELECTRONIC APPLICATIONS. C.H. Russell, Bede Scientific Inc., Englewood, CO.

As device size decreases, new challenges arise regarding shrinking dimensions, creating the need for thin, high k dielectric materials, low k copper interconnects and other exotic materials. This is in turn creating a need for new design and evaluation tools which can interface between traditional metrology tools. Critical physical parameters such as density, interfacial roughness and thickness of a layer can be resolved with x-ray reflectivity. The quickest and a very reliable method of study regarding these materials is to base work on simulations using a very robust fitting program. This work incorporates a largely theoretical study of exotic materials of interest, including SiON, low k (silicon-oxynitride) and high k dielectrics ($\text{TiO}_x$, $\text{ZrO}_x$, $\text{HfO}_x$, $\text{SrTiO}_3$), with a few selected experimental results.

2:00 PM B1.4
ABSORPTION SPECTROSCOPY ON COPPER TRACE IMPURITIES ON SILICON WAFERS. Andy Singh, Khushwant Baur, Sean Brennan, Piero Pinnetta, Stanford Synchrotron Radiation Laboratory, Stanford, CA; Takayuki Homma, Waseda University, Tokyo, JAPAN.

Trace metal contamination during wet cleaning processes on silicon wafer surfaces is a detrimental effect that impacts device performance and yield. Currently, total reflection x-ray fluorescence (TXRF) using synchrotron radiation is one of the most powerful techniques for trace impurity analysis on silicon wafer surfaces and has been used to better understand the deposition mechanisms of Cu trace impurities on silicon wafers. Recent studies investigating silicon wafers immersed in copper contaminated ultrapure water have explored a strong correlation between the deposited copper concentration and the amount of oxygen present in ultrapure water. In addition, TXRF has been combined with x-ray adsorption near edge spectroscopy (XANES) using pre-contaminated silicon samples that were dipped in UPW solutions with copper concentrations ranging from 2 to 200 ppb. Results showing the oxidation state of the deposited metal will be shown for both oxygenated and deoxygenated solutions. Finally, XANES experiments using a cell with a syringe water delivery system to observe samples directly beneath a water layer were also conducted. Higher concentrations of copper were used in the solutions to overcome degraded sensitivities due to the presence of the water layer, but the deposition processes could be monitored without environmental interference.

2:15 PM B1.5
PORE SIZE DISTRIBUTIONS IN LOW-k THIN FILMS BY X-RAY REFLECTIVITY AND SMALL ANGLE NEUTRON SCATTERING. Barry J. Bauer, Hye-Jeong Lee, Christopher Sorensen, Ronald C. Hedden, Dae-Wei Liu, Wendy Liu, NIST, Gaithersburg, MD; Jeffrey A. Lee, Jeff Wessel, International Sematech, Austin, TX.

New methods have been developed to measure of pore size distributions in 1 mm films deposited on silicon wafers. X-ray reflectivity (XR) and small angle neutron scattering (SANS) have been carried out on samples surrounded by a controlled partial pressure of toluene vapor. As the vapor pressure increases, increasingly larger pores become filled with toluene liquid and XR is used to measure the amount adsorbed as a function of pressure. The Kohlrausch equation can be used to calculate the pore size distributions from the adsorption data. SANS is carried out in various mixtures of saturated toluene and toluene-d₈ in air. The SANS signal goes through a minimum at a toluene-d₈/toluene ratio which is the "mixed phase" time. When this time the wall material is matched by the toluene mixture. The wall density can...
be calculated from this composition directly, without assuming any particular morphology type. The match point mixture is then used to fill the internal pressure in the samples provides an independent measure of pore size distribution.

3.30 PM B1.6
LINEWIDTH DEPENDENCE OF THE REVERSE BIAS JUNCTION LEAKAGE FOR CO-SILICIDED SOURCE/DRAIN JUNCTIONS. Anne Lauwers, Muriel de Potter, Richard Lindsay, Ocena Charguin, Caroline Demersresse, Christ Vanrecken, Karen Maxe, IMEC, Leuven, Belgium.

At the moment Co-silicide is the preferred self-aligned silicide for sub 0.25 um technology. To be comparable with the results and trend decreasing junction depth, the Co-silicide film thickness is being scaled down to lower the Si consumption at the expense of a higher sheet resistance. To optimally balance the trade-off between sheet resistance and junction leakage, it is crucial to minimize the silicide film thickness and the roughness. The sheet resistance can be improved by optimising the silicide pre-clean and the thermal budget of silicidation. In this work the reverse bias junction leakage is studied for Co-silicided 100 nm deep As and B source/drain junctions defined by shallow trench isolation. Dedicated test structures were designed to study the junction leakage as a function of the junction width and spacing. The width of the silicided junctions is varied between 0.15 and 3.0 um, the trench width is varied between 0.3 and 3.0 um. The Co-silicide is formed from a Co(Ti) bilayer and resulting Co-silicide film thickness is 25 nm. Different silicide pre-clean conditions are compared. The temperature of the second RTP step of Co-silicidation is varied between 850 and 900°C. The junction leakage is studied as a function of the junction width for different trench widths. The leakage current dependence on silicidation thermal budget is found to be different for large square diodes and diodes with narrow linewidth.

3.15 PM B1.7

We propose a modified self-aligned silicide (CoSi) process that uses Ge implantation and a silicon cap to reduce the silicon substrate consumption by 75% as compared with a conventional silicide process. We have used Ge implants to increase the cobalt silicide formation temperature. This forces the cobalt to react primarily with a deposited silicon cap, thus minimizing consumption from the silicon substrate. We expect this process to be useful for making silicide on shallow junctions and thin SOI films, where silicon consumption is constrained. To experimentally determine the effect of Ge implantation on silicide formation, we monitored silicide phase evolution using x-ray diffraction. We tested different Ge implantation doses having energies of 10, 15 and 20 nA. The implant dose was 2E15 cm^-2, which roughly corresponds to a Ge content of 0%. The obtained Ge profile and dose were verified using SIMS. Since the implants amorphized the top portion of the silicon film, we investigated the role of the amorphization on the silicide formation during the Ge implantation step with and without a 900°C RTA re-crystallization anneal. Following the implant, a Co layer capped by a TiN film was deposited on all samples. The samples were then annealed at temperate range of 930°C to 1000°C. We monitored the silicide phase using x-ray diffraction. The results were compared with a control sample, which was not implanted. Our main observation is that in Ge implanted wafers the formation temperature of the CoSi2 phase is 122°C higher than the control sample. There is no significant change in the formation temperature of the CoSi phase. We also found that in amorphous silicon the formation of the CoSi2 phase is not affected. Yet, if the amorphous portion of the film is thin enough so it is consumed by the CoSi phase, then the resulting formation temperature of the CoSi2 phase is similar to that of a fully re-crystallized wafer, which is reported to be 930°C. Based on our study we propose a new silicide process having reduced silicon consumption: (1) Implant Ge and junction dopants. (2) Re-crystallize amorphized silicon and activate dopants by RTA. (3) Deposit Co and anneal to form CoSi. (4) Deposit a process metal and Si film. (5) Anneal to form the CoSi2 phase, and etch the unreacted portion of the Si cap. The second anneal temperature should be lower than the formation temperature of CoSi2 in the Ge implanted Si. This limits the silicon consumption to the top portion of the wafer, thus reducing the silicon consumption from the substrate by 75%.

3.30 PM B1.8
THICKNESS EFFECT ON NICKEL SILICIDATION FORMATION AND THERMAL STABILITY FOR ULTRA SHALLOW JUNCTION MOS. P.J. Zhao, X.Z. Shen, Physics Department, National University of Singapore, SINGAPORE; J.Y. Zheng, P.S. Lee, Chartered Semiconductor Manufacturing Limited, SINGAPORE; C.H. Peng, School of Materials Engineering, Nanyang Technological University, SINGAPORE.

NiSi is a promising candidate for CMOS device fabrication due to its low resistivity, low formation temperature and one-step annealing. Compared with TiSi2, the resistivity of NiSi remains constant to 0.1 μm, while it consumes about 20% less silicon to form a silicide film of the same thickness when compared with CoSi2. These two major advantages are of crucial importance for realizing low temperature formation and sub-quarter micron CMOS fabrication. Nickel silicide samples are formed from sputtered Ni films on (100) Si substrates with thicknesses to be 0.1 μm and annealed between 300°C and 500°C for 30s by rapid thermal annealing. Electrical measurements by four-point-probe method show that the sheet resistance of thinner films start to increase at a lower temperature, indicating that thinner films are thermally less stable. Island agglomeration occurs more easily. The result is confirmed by the surface roughness data from AFM micrographs. Micro-Raman spectroscopy, which is sensitive to chemical composition and structure, is applied to identify phase formation, uniformity and orientation of nickel silicide films. For thinner films, the NiSi phase forms at lower temperature than the thicker ones. For samples of the same thickness, the NiSi films formed at higher temperatures have a higher degree of epitaxy with the Si substrate. Ion channelling experiments using Rutherford backscattering spectroscopy is also used to study the orientation of the NiSi films. The interface will be characterized by cross section TEM. And thermal stability of NiSi with different thickness will be investigated.

3.45 PM B1.9

Nickel monosilicide (NiSi) has been demonstrated to be a potential candidate for deep sub-0.1um CMOS devices because of its linewidth-independent sheet resistance and low consumption of Si. However, the thermal stability of NiSi is a major concern for backend process due to the transition of NiSi to the high-resistance NiSi2 phase at an elevated temperature. In this study, we have investigated the effect of RTA silicidation duration on the NiSi to NiSi2 transition during Ni-silicidation reaction of thin Ni (20 nm thick) film on (100) Si. The NiSi to NiSi2 transition temperature was increased from 700°C to >800°C with decreasing the annealing time from 60s to 1s. When the annealing temperature was fixed on 700°C, the critical time for NiSi to NiSi2 transition was identified as 3s-4s. Agglomeration of the silicide films was observed to depend not only on the film thickness but also the annealing time. The time-dependent agglomeration phenomenon can be explained in terms of the kinetics of grain growth. Agglomeration-induced nickel dissipation was also characterized by HRTEM. The mechanism of the kinetics of nucleation and faceted growth of disilicide has been developed, by constructing a temperature-time transformation diagram, to elucidate the important roles of the film thickness and the RTA time in determining the NiSi to NiSi2 transition temperature.

4.00 PM B1.10
ANALYSIS OF SILICIDE/DIFFUSION CONTACT RESISTANCE MAKING USE OF TRANSMISSION LINE STRUCTURES. A. Akeparg, Infineon Technologies, Munich, GERMANY (affiliated to IMEC); Anne Lauwers, Richard Lindsay, Muriel de Potter, Geert Tempel and Karen Maxe, IMEC, Leuven, Belgium.

The performance of MOS circuits depends strongly on transistor current drive. The drive current of the transistor is determined by the total device resistance, which consists of the channel resistance and the parasitic resistances associated with diffusions and contacts. As device dimensions shrink in each new technology generation, it is expected that the contact resistance between silicide and diffusion will ultimately dominate the total device resistance. For ohmic silicide/silicon contacts the contact resistivity is determined by the barrier height and the concentration of electrically active dopants at the silicide/silicon interface. The analysis of the contact resistance of a silicided junction is complicated by the fact that part of the junction is consumed during silicidation. As a result the dopant concentration at the silicide/silicon interface decreases as the silicide thickness is increased and the sheet resistance of the remaining part of the junction increases. In this work the contact resistance of Co-silicided As and B junctions was investigated in the influence of implant and anneal conditions, silicide thickness and silicidation temperature. The contact resistance between silicide and diffusion is studied using making use of dedicated transmission line structures. The structures line consist of alternating silicided and unsilicided diffusion segments, obtained by making use of
a saline blocking mask. The specific contact resistivity and the sheet resistance of the remaining diffusion under the silicide are extracted from resistance measurements on transmission line structures with segments of varying length.

4:15 PM BI.11
CHARACTERISATION OF NOVEL, RELAXED Ge AND SiGe, PSEUDO BUFFER LAYERS GROWN BY CHEMICAL VAPOUR DEPOSITION. A. Jey P. Jacob, T. Myrberg, O. Nur, M. Willander, Physical Electronics and Photonics, Physics Department, Microelectronics and Nanotechnology Center (MC2), Chalmers University of Technology and Gothenburg University, C.J. Peters, Y. Campigelli, B. Benzel, STMicroelectronics, Colles, FRANCE; R.N. Kiytt, F. Ioffe Physical-Technical Institute of the Russian Academy of Science, St Petersburg, RUSSIA.

Relaxed SiGe and pure relaxed Ge pseudo-substrates have attracted global interest recently. They are of great importance for providing suitable substrates, the intrinsic strain Si as well. The University will present HV compound semiconductors with Si technology. We have used the strain sensitive high resolution two dimensional reciprocal space mapping (3D-RSM) tool to characterize novel high quality fully relaxed SiGe and Ge buffer layers grown on Si [100] substrates by chemical vapour deposition. Both symmetric and asymmetric reflections were used to characterize these buffer layers. The effect of the Ge layer thickness and the post-growth temperature annealing on the over-all quality regarding relaxation and threading dislocation density is investigated. In addition, the advantage of growing buffer layers on low temperature grown initial Si buffer layers is also studied. The 3D-RSMs are used to extract layer tilt relaxation factors, as well as to assess the layer quality. These results indicate that fully relaxed Ge buffer layer with low threading dislocations. We have observed improved crystalline quality with increasing layer thickness up to an epitaxial layer of 5 micrometers. On contrary to what has been previously shown previously no improvement regarding the relaxation and threading dislocation density reduction by using the initial low temperature SiGe buffer layer. The overgrowth on these relaxed buffer layers is also monitored. These measurements were complemented by secondary ion mass spectrometry (SIMS). The SIMS results show that at the Si/Ge interface a considerable intermixing have taken place. This intermixing was also observed in High resolution rocking curves as a twin peak high angle shoulder of the Ge peak in agreement with the SIMS results.

4:30 PM BI.12
PREVENTION OF BUCKLING DURING SiGe RELAXATION ON COMPLIANT SUBSTRATES. Hairian Zin, Rui Huang, Princeton University, Center for Photonics and Optoelectronic Materials, Princeton, NJ; K.W. D. Hoiberg, Naval Research Lab, Washington, DC; Zhiqiang Sun, Princeton University, Center for Photonics and Optoelectronic Materials, Princeton, NJ; Steven B. Sheib, Tom Duffy, Princeton University, Dept of Geosciences, Princeton, NJ; James C. Strum, Princeton University, Center for Photonics and Optoelectronic Materials, Princeton, NJ.

There has been increasing interest in compliant substrates for integration of heterogenous epitaxial materials. In our experiments, borophosphosilicate glasses (BPSG) on silicon is used as a compliant substrate to host a relaxed silicon-germanium (SiGe) layer initially grown pseudomorphically on Si[100] substrate and then transferred to the BPSG by a bond and etch process[1]. Buckling of SiGe during relaxation has been observed[2] and analyzed[3]. Here, we first develop a fundamental quantitative model and understanding of the stress/hysterax between the desired lateral relaxation and the undesired vertical (buckling) process, and then demonstrate an experimental method to overcome the buckling issue. Large and thin islands cause slower lateral relaxation, which in turn enhances the buckling rate. Relaxation and buckling are measured by Raman spectroscopy and AFM respectively. Experiments confirmed that thin SiGe layers buckle much faster. Furthermore, lowering the viscosity of the BPSG by a factor of five lowers the time required for both the lateral relaxation and buckling process, but the amount of buckling for any given amount of desired lateral relaxation does not change. Island size is a critical parameter, however, with buckling amplitude on 60nm islands of Si0.25Ge0.75 being ten times as large as that on 140nm islands. This technique overcomes the problem of samples of temperature thicker with an epitaxial cap, or buckling can be removed by long anneals at 850°C after the initial buckling. The buckling amplitude decreases dramatically from more than 10um to 0.5um (RMS).

We observe for small islands that buckling faster than high islands and islands flatten faster at higher temperature. In addition, flattening process slows down over time, which is explained by the fact that the flattening process is driven by the residual strain in the islands. With high temperatures, it should be possible to make relaxed SiGe islands with zero dislocation density. This work is supported by DARPA (N66001-06-1-8557) and ARO (DAAD19-98-1-2070). I.R. Hoiberg, F.J. Kub, M. Fartun, M.E. Tweep, P. Thomson, T.S. Khan and C.K. Inoki, J. Electron. Mater. 39, 857 (2010).


4:45 PM BI.13
THE ROLE OF EXCESS SILICON OR FREE VOLUME AT THE GROWING OXIDE INTERFACE. Ralph Jacobsen, Lehigh University, Sherman Fairchild Laboratory, Bethlehem, PA; S.J. Kilpatrick, IBM Microelectronics Division, Essex Junction, VT.

In the seminal work on Si oxidation by Deal and Grove [DiG] the early stage of oxidation. <100> does not follow an expected simple linear relationship entailing [liner] reaction coefficient and time. This coefficient encompasses the conversion of crystalline Si into SiO2 with an over 2X cell size. This gives rise to the model of a large excess of SiO2 on top of the oxide. Alternatively the need for the creation of “free volume” at the interface. One of the earliest detailed models was done by W. Tiller et al. The existence of interstitial [excess] Si was given particular cogency by the success in explaining oxidation related phenomena like OSP, OED [OSD]. This paper discusses the issues that arise when excess Si or SiO flux is used to adjust the D&G model to the observed growth. The authors use the experience of modelling the oxidation of SiGe alloys with the variation of over nine orders of oxygen partial pressure as a background to the discussion. A recent suggestion of the thin oxide problem by M. Ummass et al. invokes the effect of “excess Si” near the interface to adjust the D&G reaction coefficient and an additional flux to the growing oxide. This paper will assess some of the critical points in the model as well as compelling ion of sub-band Si to the oxidation mechanism. A recent proposal by Pasquarello et al. opens new insight into how the interface adjusts to the growing oxide which challenges our previous mechanistic notions.

SESSION B2: GATE DIELECTRICS AND DEVICES
Chair: Jane P. Chang and Venita Misra
Tuesday Morning, April 2, 2002
Salon 10-12 (Marriott)

8:00 AM B2.1
PLASMA ENHANCED ATOMIC LAYER DEPOSITION OF ZrO2 GATE DIELECTRIC. Jeehyung Koo, Yangsoo Kim, Teo-Han Doh, Jiwoong Han, Sungwoong Choi and Hyesung Jeon, Division of Materials Science and Engineering, Yonsei University, SEOUL, KOREA; Yunsoo Kim, Thin Film Materials Laboratory, Advanced Materials Division, Korea Research Institute of Chemical Technology, Yuseong, Daejeon, KOREA; Si-Woo Rhee, Laboratory for Advanced Materials Processing (LAMP), Department of Chemical Engineering, Pohang University of Science and Technology (POSTECH), Pohang, KOREA.

As the gate oxide thickness of metal-oxide-semiconductor (MOS) devices is scaled down to less than 3 nanometers, leakage current through gate dielectrics and reliability become serious problems. Thus, the high-k gate dielectrics become one of the solutions in providing increased capacitance and reduced leakage currents without significantly increasing the actual equivalent oxide thickness (EOT) of gate dielectrics. Among the high-k materials, zirconium oxide (ZrO2) is considered to be one of the potential replacements of SiO2 gate oxide due to its high dielectric constant and good reliability in contrast with silicon. In this study, we investigated the ZrO2 gate dielectric deposited by plasma enhanced atomic layer deposition (PEALD) method using three different zirconium sources. ZrO2 were deposited on p-type Si (100) substrate using Zr(tetrahydro)6(\(\text{O}\)Bu)4 and Zr[net(H2)2] as Zr precursor and oxygen as reactant gas. Oxygen reactant gas was introduced both as in normal gas phase and plasma state. All samples were rapid thermal annealed at 80°C for 10 seconds in nitrogen ambient. Platinum (Pt) electrode layer with the thickness of about 100nm was deposited by e-beam evaporator and patterned to form the gate electrodes.

Post metallization annealing was carried out in H2 + N2 ambient at 450°C for 30 minutes. The physical and chemical characteristics of ZrO2 film were analyzed by cross-sectional transmission electron microscopy (XTEM), atomic force microscopy (AFM), Auger electron spectroscopy (AES) and X-ray photoelectron spectroscopy (XPS). The electrical properties and reliability characteristics including I-V, hysteresis, leakage current and capacitance were analyzed by LV and CV measurements.

8:15 AM B2.2
ATOMIC LAYER CHEMICAL VAPOR DEPOSITION OF HAFNIUM OXIDE USING ANHYDROUS HAFNIUM NITRATE PRECURSOR. J.E. Conley Jr., Y. Ono, D.J. Tweet, W. Zhang, W. Guo, Shu-Cheng, Lee of Amherst, Amherst, WA; S.K. Mohammed, R. Slinski, Oregon Graduate Institute, Department of Electrical and Computer Engineering, Beaverton, OR.

It is generally believed that scaling of SiO2 will not be possible much
below 1.0 mm and that a high-k replacement material for SiO₂ will be necessary. Since an EOT of less than 1.0 mm will be needed and an interference coating is needed, the uniformly deposited film on the backside of the wafer is ideal to reduce the EOT. However, a high-k film with a sufficient dielectric constant and low leakage current is required. The high-k film must be stable at high temperatures and have good adhesion to the silicon substrate.

Alumina films deposited on the backside of the wafer were used as the high-k replacement material. The alumina films were deposited using a plasma-enhanced chemical vapor deposition (PECVD) process. The alumina films were deposited on the backside of the wafer to reduce the EOT. The alumina films were deposited at a temperature of 300°C to 400°C. The resulting film properties were measured using an X-ray photoelectron spectroscopy (XPS) and a high-resolution transmission electron microscopy (HRTEM). The resulting film properties were measured using an X-ray diffractometer (XRD). The XRD results showed that the alumina films were amorphous. The XPS results showed that the alumina films had a high-k dielectric constant.

As the scaling of silicon CMOS technology continues, high-k gate dielectrics are required to provide improved gate capacitance while reducing gate leakage current. One candidate material that is receiving considerable attention is hafnium silicate. As shown by [1, 2], results on the formation of hafnium silicate using UV oxidation of hafnium silicate. Hafnium silicate films were deposited on hydrogen terminated silicon wafers at room temperature using a magnetron sputtering system. The hafnium silicate films were subsequently oxidized to hafnium silicate by exposing the wafers to an oxidant.

The electrical behavior of the as-deposited and annealed silicate films was determined with current-voltage (I-V) and capacitance-voltage (C-V) measurements. The effect of post-annealing on electrical properties using N₂, O₂, N₂O, NO, NH₃, and forming gas was also presented. Comparison of the UV oxygen oxidized hafnium silicate films will be made with those prepared using conventional annealing techniques.

As for the evaluation of the hafnium silicate films, the results from the XPS and HRTEM measurements will be presented. The electrical properties of the as-deposited and annealed silicate films will be compared with those of the reference samples.

8:45 AM B2.4 METAL-ORGANIC CVD OF Ru AND RuO₂: THIN FILM FOR GATE ELECTRODE APPLICATIONS. Filippos Papagiannakis, Spyros Sakazis, Zuhin Pard, Steve Casagrande, Eric Eisenbraun, Utrecht Institute for Materials, Albany, NY

Ruthenium-based thin films are of interest for emerging CMOS gate electrode applications owing to their low resistivity, excellent thermal stability, and high work function suitable for use as work functions in metal-oxide-semiconductor field-effect transistors (MOSFETs). Ru and RuO₂ films were deposited on SiO₂ by chemical vapor deposition (CVD) and low pressure plasma enhanced CVD (PECVD) in a 288 mm wafer deposition chamber using a metal deposition mixture containing Ru and RuO₂. The resulting film properties were measured using X-ray photoelectron spectroscopy (XPS), high resolution transmission electron microscopy (HRTEM), and x-ray diffraction (XRD). Both Ru and RuO₂ films were deposited at a temperature of 300°C to 500°C. The resulting film properties were measured using X-ray photoelectron spectroscopy (XPS), high resolution transmission electron microscopy (HRTEM), and x-ray diffraction (XRD). Both Ru and RuO₂ films were deposited at a temperature of 300°C to 500°C. The resulting film properties were measured using X-ray photoelectron spectroscopy (XPS), high resolution transmission electron microscopy (HRTEM), and x-ray diffraction (XRD).
better film uniformity than the batch process. We have recently developed single-wafer furnace RTP (rapid thermal processing) modules for both thermal oxidation and low pressure chemical vapor deposition (LPCVD) of silicon nitride. Uniform oxide films of sub-20Å can be grown by thermal oxidation and NO nitridation. The RTCVD system also provides consistent film deposition performance for silicon nitride thin films in terms of thickness and uniformity. This paper further extends the application of the hot-wall single-wafer RTCVD system to gate dielectric applications. The system provides silicon nitride films of equivalent oxide thickness below 20Å. The film deposition processes, the post-deposition anneal and the electrical characterization of the gate dielectrics will be discussed.

11:15 AM B2.11 HIGH PURITY SILICON AMIDO PRECURSORS FOR LOW TEMPERATURE CVD OF GATE DIELECTRICS
Alexander S. Borovik, Cheongying Xu, Bryan C. Hendrick, Jeffrey F. Roeder and Thomas H. Baum, ATMI, Inc., Danbury, CT.

Early transition metal silicides, such as those containing zirconium and hafnium, are of great interest for use in the next generation gate dielectrics. To minimize the formation of an internal silicon oxide layer, a low temperature CVD process is required. Generally, metal amides are promising low temperature CVD precursors. However, until recently, their silicon analogues were not readily available in high purity, a fundamental requirement for their use in electronic applications. We have developed direct synthetic methods for the production of high purity Si[N(CH$_3$)$_2$]$_4$, Si[NMe$_3$]$_4$, HSi[NMe$_3$]$_3$ and HSi[N$_2$Et]$_2$ in high yield. These compounds were further characterized by NMR, XPS and ICP-MS.

In this paper, we report the synthesis, characterization of the new precursors and their use for the low temperature CVD of silicon metal silicides.

11:30 AM B2.12 METROLOGY STUDY OF SUB 20 Å OXYNITRIDE BY CORONA-OXIDE-SILICON (COS) AND CONVENTIONAL C-V ABRASSIONS. Pui-Yee Hung, George A. Barnwell, 4th, and Xiaofang Zhang, a.
International SEMATECH, Inc. Metrology Yield Management Tools, Austin, TX; "KLA-Tencor Corporation, Film and Surface Technology Division, San Jose, CA.

This work aims to develop a non-contact corona-oxide-silicon (COS) measurement strategy for the monitoring of sub 20Å oxide gate dielectrics. The oxynitride used in this study is composed of two batches of In-Stu Steam Generated oxide [BSG] oxide (20/18 Å) which are exposed to Remote Plasma Nitridation (RPN) for various time durations. First, the nitrogen concentration and profile of the samples are established by SIMS and nuclear reaction analysis. Then, the COS measurement using Quantum was carried out on comparison wafers, extending the follow for five electrical parameters: interface trap density ($D_i$), flatband voltage ($V_F$), total charge, effective charge and equivalent oxide thickness (EOT). Both the pre-annual $D_i$ and total charge are promising parameters because of their correlation with the oxide performance. However, the $V_F$, effective charge, and EOT measurements appear to be affected by the ambient environment or the leakage characteristics of the oxynitride. In addition, the integrity of the oxynitride is verified by measuring the COS tunnelling voltage, leakage current and oxide resistivity. A comparison of the C-V/COS measurements of EOT, $V_F$ and current density is included; however, no simple linear relationship exists between these parameters.

SESSION B2: HIGH-K DIELECTRICS
Chair: Roy G. Gordon and Yeena Mira
Tuesday, Afternoon, April 2, 2002
Salon 10-12 (Marriott)

1:30 PM B2.10 SILICON NITRIDE - THIN FILM DEPOSITION FOR GATE DIELECTRICS USING SINGLE-WAVER HOT-WALL RAPID THERMAL OXIDATION. G.C. Reddy, V. Lokesh, S. Barrel, Robert Herring, ASM-IV, Thermal Division, Scotts Valley, CA.

Rapid thermal processing (RTP) is an emerging technology in integrated circuits manufacturing, and could be an alternative to batch furnace processing as future wafer production moves to 300mm diameter size. RTP requires shorter process time and can achieve
has been used to investigate the crystallization behavior of metal silicates and alloys. A model describing the crystallization behavior of La and Zr-containing glasses has been used to predict the time and temperature dependencies of crystallization. This model has been used to optimize a dielectric and a process able to withstand temperature excursions in excess of 1000°C.

In general, appropriate combinations of temperature and oxygen partial pressure can be found which minimize unwanted interface reactions, and hence maintain a high dielectric interface layer with high temperature exposure. Models for reactions between these materials will be presented in the context of oxygen rich and oxygen poor atmospheres. Specifically, a new model will be presented which attempts to describe the decomposition of oxides in contact with silicon. Finally, data will be shown comparing materials prepared with and without in situ deposited Ti metal gates. These results demonstrate the sensitivity of ultrathin capacitors layers to atmospheric exposure.

2:00 PM B3.2

THERMODYNAMIC STABILITY OF HIGH-K DIELECTRIC METAL OXIDES ZrO2 AND HfO2 IN CONTACT WITH Si AND SiO2

Mieczyslaw G. Kowalski, John E. Jaffe, Pacific Northwest National Laboratory, Champaign, IL; Matt Stoller, Rama I. Hegde, Rahul S. Rai, and Philip J. Tobin, Motorola Inc.

We present theoretical and experimental results regarding the thermodynamic stability of the high-k dielectrics MZO2 (M = Zr and Hf) in contact with Si and SiO2. The HfO2/Si interface is found to be stable with respect to formation of silicides and to have a low interface roughness value, whereas the MZO2/SiO2 interface is not. The MZO2/Si interface is marginally unstable with respect to formation of silicides. Cross-sectional transmission electron micrographs illustrate the orientation of columns of silicides, identified as silicides, across the polycrystalline ZrO2/Si interface. The HfO2/Si interface is not stable with respect to formation of silicides. For both ZrO2 and HfO2, the X-ray photoemission spectra illustrate formation of silicide-like compounds in the MZO2/SiO2 interface.

2:15 PM B3.3

EFFECT OF TECHNOLOGY SCALING ON MOS TRANSISTORS WITH HIGH-K DIELECTRICS

Mohan R. Banakar, R. Chandrasekaran, and P. Desai, V. Ramaprasad Rao, Indian Institute of Technology Bombay, Department of Electrical Engineering, Mumbai, INDIA.

High-K materials like Al2O3 (K = 10), ZrO2/HfO2 (K = 25), and TiO2 (K = 60) have received much attention recently as alternative gate dielectrics for CMOS applications. A few papers have been published recently on the effect of fringing capacitances in these high-K gate dielectric MOS transistors due to their higher physical dielectric thickness. However, no work has been done to study the effect of technology scaling parameters on the fringing field effects. In this work, we have studied the effect of gate overlap length, spacer dielectric material and other technology parameters on the device and circuit performance. We have investigated the behavior of high-K gate dielectrics with high-K gate dielectrics using a high-dimensional device simulator. In high-K gate dielectric transistors, the ratio of physical thickness of the gate dielectric exceeds 10, which increases with the increase in K. As the dielectric constant increases, the threshold voltage increases. Thus, this 2-D effects become dominant leading to poor short channel performance. For Kg/d greater than Kg, we observe a substantial reduction in the ON current. However, using a high-dimensional device simulator, we have shown that this 2-D effects become dominant leading to poor short channel performance. For Kg/d greater than Kg, we observe a substantial reduction in the ON current. However, using a high-dimensional device simulator, we have shown that this 2-D effects become dominant leading to poor short channel performance. For Kg/d greater than Kg, we observe a substantial reduction in the ON current. However, using a high-dimensional device simulator, we have shown that this 2-D effects become dominant leading to poor short channel performance. For Kg/d greater than Kg, we observe a substantial reduction in the ON current. However, using a high-dimensional device simulator, we have shown that this 2-D effects become dominant leading to poor short channel performance.
observed that the ZrSe$_2$ formation was substantially restrained by inserting Si$_3$N$_4$ instead of SiO$_2$. This result means that the formation and diffusion of Si-O at the stack is the dominant process promoting the reaction. Based on these experimental results, we think the thermal stability of the poly-Si/ZrO$_2$/ZrSiO$_4$/Si stack is mainly due to the nitrogen incorporation into the ZrSiO$_4$ interfacial layer, in which Si-O cannot crystallize as effectively supported.


3:45 PM B3.7 STRUCTURE AND STABILITY OF ALTERNATIVE HIGH-$k$ DIELECTRIC LAYERS ON SILICON. S. Steiner, Z. Chen, Rice University, Houston, TX; D. Nie, R. Ashraf, C.N. Persson, D. Wicksman, J.P. Merin, A.I. Kingon, North Carolina State Univ, Raleigh, NC.

We use electron energy-loss spectroscopy (EELS) in scanning transmission electron microscopy with a sub-0.2 nm probe and atomic resolution transmission electron microscopy to investigate the structure and stability of Y$_2$O$_3$ grown by remote plasma chemical vapor deposition (CVD) and of ZrO$_2$ layers grown by reactive evaporation in a molecular epitaxy system (MBE). We investigated CVD Y$_2$O$_3$ films as a function of film thickness and pre-treatment of the silicon surfaces after post-deposition anneals. We show that thin films on clean silicon form a silicon film with a thin interfacial oxide, whereas a nitrogen plasma-treated Si substrate reduces the amount of silicon wafer from the interface and Y$_2$O$_3$ is found as the top-most layer in a film of the same thickness (7 nm). We also show that the amount of silicon in the film determines the crystallography of the 25% in post-deposition anneals at 900°C and the formation of a thin interfacial oxide is difficult to avoid under atmospheric, non-capped annealing conditions. MBE-ZrO$_2$/Si structures were investigated before and after rapid thermal annealing (RTA) treatments at 1000°C under different oxygen partial pressures. We identified a critical partial pressure of approximately 10$^{-7}$ torr that can preserve a thin (1 nm) interfacial silicon oxide layer for high equivalent oxide thicknesses. At higher oxygen partial pressures (about 10$^{-2}$ torr) the interfacial oxide thickness increases through oxygen diffusion through the ZrO$_2$ layer and silicon consumption at the interface. At lower oxygen partial pressures (about 10$^{-7}$ torr), silicon formation at the interface is observed. ZrO$_2$ films resulted in the optimal partial pressure for a thin interfacial oxide were found to crystallize and contain no silicon, whereas silicon diffusion and partial amorphization takes place at higher partial pressures. The results show the relationship between crystallization and silicon diffusion as a function of annealing atmosphere, and also show that oxide crystallization is important in determining the overall formation behavior. We will also discuss the application of EELS fine-structure analysis to provide an additional measure of interface composition in these very thin layers.

4:00 PM B3.8 ATOMIC LAYER DEPOSITION OF ZIRCONIUM DIOXIDE THIN FILMS USING NEW ALKOXIDE PRECURSORS. T.J. Leedham, A.C. Jones, P.A. Williams, H.O. Davies, Inorganix Ltd, Miltonen, UNITED KINGDOM; M. Riehle, R. Mastro, M. Leskam, Department of Chemistry, University of Helsinki, FINLAND.

Zirconium dioxide has a high permittivity and is stable in contact with silicon, making it a prime candidate as the gate dielectric in next generation MOSFET devices. Atomic layer deposition (ALD) allows the deposition of conformal films at low substrate temperatures with control of layer thickness to the monolayer level. Zirconium tetrachloride and zirconium tetraethoxide have been used as precursors but halide contamination is a potential problem. Zeolites may offer process advantages and Zr tetrathionate-hydroxide has been investigated for the ALD of zirconium dioxide. However, this mononuclear precursor contains a four coordinate unsaturated Zr(IV) centre making it more sensitive and susceptible to decomposition during storage and use. The use of donor functionalised alkoxide ligands containing more than one oxygen or nitrogen donor group (e.g. dimethylminoethoxide) leads to more fully saturated and less reactive Zralkoxide complexes. Here we report the ALD of zirconium dioxide using a number of donor functionalised alkoxide precursors. Results are compared to conventional sources and the implications are discussed for the future design of ZrO$_2$ ALD precursors.

SESSION B4: POSTER SESSION

DIELECTRIC CHARACTERIZATION

Tuesday Evening, April 2, 2002

8:00 PM

Salon 1.7 (Merceret)

B4.1 CHARACTERIZATION OF Si NANOCRYSTALS ON DIELECTRIC SURFACES FOR MEMORY APPLICATIONS. Ran Liu, X.D. Wang, Q. Xie, Motorola SPS, Advanced Process Development & External Research Laboratory, Mesa, AZ; R. Rao, and B.E. White, Motorola SPS, Advanced Process Development & External Research Laboratory, Austin, TX.

One of the promising application of nanocrystalline Si materials is the nonvolatile memory using Si nanocrystals grown on dielectrics as a floating gate. The characterization of the size and density of Si nanocrystals is crucial for understanding the device performance, and as the nanocrystals presents great challenges even to the powerful structural characterization techniques such as atomic force microscopy (AFM) and transmission electron microscopy (TEM). Since the electron and phonon structures strongly depend on the size of nanocrystal Si, optical spectroscopy can be used as nondestructive characterization and metrology tool. In an effort to correlate the optical properties with the nanocrystal structure and density, we have performed UV-Raman spectroscopy and spectroscopic ellipsometry in conjunction with AFM and TEM on thin layers of Si nanocrystals of different sizes and densities on dielectrics. The extremely small optical penetration depth strongly suppresses the UV-Raman signals from the substrate and thus allows characterization of the thin nanocrystal Si layer by correlating the phonon frequency shift to the particle size. Ellipsometry spectra have been found to be sensitive to both the size and the density of Si particles. The energy gap obtained from ellipsometry seems to increase with decreasing Si particle size, possibly due to quantum confinement effect.

B4.2 HIGH-$k$ GATE DIELECTRIC PREPARED BY LOW-TEMPERATURE WET OXIDATION OF ULTRATHIN METAL NITRIDE. Sunyoung Chi, Sungjung Bae, Hyoung Hwang, Kwangju Institute of Science and Technology, Dept of Materials Science and Engineering, Bukuku, Kwangju, KOREA.

Although Ta$_2$O$_5$ has been investigated in terms of MOS gate dielectric applications, it is difficult to obtain an equivalent oxide thickness of less than 2 nm with acceptable leakage current. Since an approximately 1 nm-thick interfacial SiO$_2$ oxide layer is necessary to minimize the interface state density and the intermixing of silicon and Ta$_2$O$_5$, the dielectric constant of Ta$_2$O$_5$ is not sufficient to obtain an equivalent dielectric thickness of less than 2 nm. Recently, we have reported an excellent electrical characteristics of Ta$_2$O$_5$ prepared by nitridation and wet oxidation of Ta$_2$O$_5$. In this presentation, we report on high-$k$ gate dielectrics prepared by low temperature wet oxidation of TaN layers. TaN layer was directly deposited on bare silicon using RF magnetron sputtering. Wet oxidation of TaN was performed at 400°C. After the deposition of a 150nm-thick layer of Pt, MOS devices with a gate area of 9 x 10$^{-6}$ cm$^2$ were defined. Compared with Ta$_2$O$_5$, N$_2$O$_4$ prepared by NH$_3$ nitridation of Ta$_2$O$_5$, Ta$_2$O$_5$.N$_2$O$_4$ prepared by wet oxidation of TaN shows excellent electrical characteristics such as equivalent oxide thickness as thin as 13Å, leakage current density of less than 100µA/cm$^2$ at V$_{FB}$ = 1.5V, and acceptable interface state density which was confirmed by CV and conductance method. The improvements of electrical characteristics can be explained by the reduction of interfacial oxide layer due to the direct deposition of metal nitride. [1] H. Jung, K. Im, D. Yang, H. Hwang, Appl. Phys. Lett., 76, 3610 (2000).

B4.3 ELECTRICAL AND MATERIALS PROPERTIES OF ALD-GROWN ZrO$_2$ AND HfO$_2$ GATE DIELECTRICS. Hyeongsik Kim, Paul C. McIntyre, Stanford Univ, Dept of Materials Science and Engineering, Stanford, CA; Krishna Narayanan, Stanford Univ, Dept of Electrical Engineering, Stanford, CA.

As MOS transistor size decreases and higher speeds are required, the gate oxide must be aggressively decreased down to 1.5nm for 0.1µm channel length transistor. However, as the thickness of SiO$_2$ decreases, the leakage current across the dielectric increases enormously through direct tunneling. At present, in order to reduce the leakage current, high-$k$ materials, including ZrO$_2$ and HfO$_2$ have been widely investigated because they offer the opportunity to scale dimensions further, while retaining sufficient physical thickness of the dielectric to avoid direct tunneling. Among many possible deposition techniques, ALD (Atomic Layer Deposition) is drawing a lot of attention because it can produce high quality films with precise thickness control and near-perfect conformity owing to its adsorption-controlled deposition mechanism. For these experiments, we used a cold wall ALD system with ZrCl$_4$/H$_2$O and HfCl$_4$/H$_2$O precursors for each processes. The deposition was carried out at 250~300°C on a thermally-grown thin SiO$_2$ underlayer. Platinum gate electrodes were deposited through a shadow mask by e-beam evaporation for electrical characterization of the gate dielectric. In this presentation, we will compare the electrical and microstructural
properties of ALD-grown ZrO₂ and HfO₂ using CV, I-V, and H-T-TEM. The microstructure and leakage current properties of ZrO₂ and HfO₂ were measured before and after thermal annealing. In addition, electrical and material properties as a function of thickness will be discussed. As a possible candidate for high-k gate dielectric applications, data on ZrO₂-HfO₂ nanosilicate structures will be also presented.

**B4.4**

**METALITO MODELING OF BORON DIFFUSION IN POLYCRYSTALLINE HfO₂ FILMS.** Tran,Li Lin. Advanced Process Development and External Research Lab., Motorola, Inc., Mesa, AZ.

We present an initio modeling results including formation, migration, and activation energies for B diffusion through bulk and grain boundaries in polycrystalline HfO₂ films. Modeling results clearly indicate that B can penetrate through in a 10 Å HfO₂ film via grain boundary diffusion, but not by bulk diffusion. SIMS analysis of B concentrations at the grain boundaries of polycrystalline HfO₂/Ge samples in different anneals showed double B peaks at the interfaces and thus confirmed the modeling predictions.

**B4.5**


As the search for an alternative gate dielectric for the currently used SiO₂ continues, numerous high-k materials have been investigated as possible candidates. Among them, zirconium dioxide, hafnium dioxide and hafnium trioxide have shown great promise. In a comparative study, nanometer thick samples were grown by both conventional pulsed laser deposition (PLD) and by an ultraviolet-assisted pulsed laser deposition (UVPLD) technique. In the UVPLD technique, low power Hg lamps were added to the PLD chamber. With the addition of the 185-nm UV radiation sources, molecular oxygen is broken down into highly reactive oxygen and atomic oxygen which can incorporate more readily into the growing films. The effects of this enhanced oxygenation process resulted in higher crystalline quality, more stoichiometric films due to lower oxygen vacancies. A variety of characterization techniques were used to investigate the effects of the ultraviolet radiation. The structural properties were analyzed by transmission electron microscopy, x-ray diffraction, and x-ray reflectivity. Chemical analysis was performed via x-ray photoelectron spectroscopy and Fourier transform infrared spectroscopy. Finally, electrical characterization in the form of capacitance-voltage and current-voltage measurements was performed. In each of the cases, samples grown with and without ultraviolet illumination were compared and the oxygen content was analyzed. The main benefit of this UV-assisted process is the ability to grow higher quality films, or otherwise equivalent films but at lower processing temperatures.

**B4.6**

**PROPERTIES OF HAFNIUM OXIDE UPON DEPOSITION METHOD.** Suheen Nam, Seok Woon Nam, Jong Ho Yoo, Hae Hong Ko, Dept of Ceramic Engineering, Yonsei Univ., Seoul, KOREA; Ja Ham Ku, Sijoyong Choi, Samsung Electronics Co., Ltd., KOREA.

The SiO₂ dielectrics have been a subject of intensive studies for several decades. According to the past trends in mass production, however, reliability problems were considered to limit the physical thickness of gate SiO₂. Therefore, extensive research is underway to meet the challenge of moving beyond the SiO₂ era, that is, to replace the conventional SiO₂ with high-k gate dielectrics. The advantages of HfO₂ over SiO₂ are: It is a more effective barrier to migrating impurities; its high dielectric constant, and high band gap of 5.55 eV with favorable band alignment with silicon. We studied and optimized the characteristics of hafnium oxides deposited by different kinds of methods. Generally, reactive sputtering method is used to deposit the oxide thin films. However, there exists substantial interlayer between oxide and silicon, causing serious degradation to fully achieve the potential of high permittivity. In order to testify these problems, we examined the films using simple reactive sputtering method and compared them with the other films deposited by the modified sputtering method. During hafnium sputtering, O₂ flow was modulated to control the interface quality and to suppress the additional growth of the interfacial layer. If hafnium metal is removed before going through the reactive sputtering step, it acts as an oxygen barrier; thus interlayer, which is thought to be SiO₂, reduced down to ~5Å. Electrical properties of hafnium oxides were evaluated using capacitance-voltage (CV) and current-voltage (I-V) measurements. It showed high CV characteristics, indicating low level of interface trap charge. The equivalent oxide thickness was calculated to be ~1.6Å using modified

reactive sputtering method. Besides, leakage current level was quite low comparing to SiO₂ with same physical thickness, accounting for the superiorities of hafnium oxide as a gate dielectric.

**B4.7**

**IS IT A RIGHT ASSUMPTION THAT B AND Ge ARE DISTRIBUTED RANDOMLY AFTER GROWING A STRAINED Hf/BIT-STRUTURE?** V.I. Kolygin, PDF/Solutions Inc., FEOL Dept, San Jose, CA.

A comprehensive review of the main experimental features of the B and Ge segregation onto Si substrates during growing a fully strained SiGe layers is carried out. The main feature of the segregation process is that surface B and Ge clustering is observed. The simplest case is the segregation of B or a couple of the atoms on the surface of SiGe in the form of Se, and along 1D chains or 2D areas are also seen with some sort of symmetry. This can be explained since the surface diffusion of B and Ge is enough for collision of atoms and clustering during a layer growth. The 2D reconstructed Ge structure still like a dislocation are precursors for such a clustering on the H-passivated surface. These observations are strongly against the assumption that B and Ge are randomly incorporated into a strained layer rather suggesting a strong correlation of B and Ge distribution. Another observation is that surface Ge atoms are considered to be responsible for the surface B segregation process. A set of original experiments is carried out showing that at certain conditions B is taking initiative and determine the Ge surface segregation process. Basic assumptions are suggested to self-consistently explain these original experimental features and what is observed in the literature. These results have a strong implication for modeling the B diffusion in SiGe where the initial conditions should be formulated accounting for the correlation in B and Ge distribution. A new assumption for the initial condition to be "all B atoms are captured by Ge" is regarded as a right one implicating that there is no apparent diffusion controlled by the B capturing kinetics.

**B4.8**

**IMPROVEMENT OF GATE DIELECTRIC QUALITY OF MNS CAPACITOR BY HYDROGEN ETCHING ON ULTRA THIN GATE DIELECTRICS.** Purn C. Waghmare, Samahad B. Patil, Rajiv O. Dusane, V. Ramgapal Rao, Dept of Metallurgical Eng and Materials Science, IIT Bombay, INDIA.

Silicon nitride is being considered as a promising candidate to replace thermal gate oxide dielectric, as the latter is reaching its scaling limit due to excessive increases in the gate tunneling leakage current. A novel technique called, the Hot Wire Chemical Vapor Deposition (HW-CVD), had shown promise to synthesize high quality silicon nitride films at 250°C while maintaining their primary advantage of higher dielectric constant. The deposition was carried out for one minute. However it was found that the fixed charges and the interface states were of the order of 5 x 10¹². To improve the gate quality of the device due to the increase in fixed charges and interface states, hydrogen etching is carried out. This etching is carried for 1 min at a hydrogen flow rate of 5ccm with 250°C as substrate temperature. Our exhaustive characterization shows the reduction in fixed charges and the interface states to about 1.2 x 10¹². This could be due to bonded silicon atoms getting passivated by hydrogen atoms.

**B4.9**

**THE CHARACTERISTICS OF SILICON NITRIDE THIN FILMS BY ALD AND LAYER DEPOSITION.** Joo-Hyon Lee, Dept of Materials Science and Engineering, KAIST, Daejeon, KOREA; Hyuk Kim, Dept of Materials Engineering, Hankuk National Univ, Daejeon, KOREA; Yeon-Seong Lee, Dept of Multimedia Engineering, Hankuk National Univ, Daejeon, KOREA; Seok-Kyun Rha, Dept of Material Engineering, Hankuk National Univ, Daejeon, KOREA; Chung-Ock Park, Dept of Materials Science and Engineering, KAIST, Daejeon, KOREA; Won-Joo Lee, Dept of Advanced Materials Engineering, Sejong Univ, Seoul, KOREA.

Recently, atomic layer deposition (ALD) attracts much interest in silicon integrated circuit processing owing to its accurate thickness control, conformal coverage, high film quality, and low-temperature process. Silicon nitride films have been widely used as the interlayer dielectrics (ILD), and are deposited by conventional low-pressure chemical vapor deposition (LPCVD) in the front-end processing or by plasma-enhanced chemical vapor deposition (PECVD) in back-end processing. However, high process temperature of LPCVD and poor film quality of PECVD are being expected to limit the processability and the reliability of the state-of-the-art IC in the near future. In the present paper, silicon nitride films were deposited by ALD, and effects of process parameters on the film properties were examined. Silicon tetrachloride (SiCl₄) and dichlorosilane (DCS) were compared as the silicon source gases. Ammonia (NH₃) was used as the nitrogen source gas, and nitrogen was used as the purge gas between the pulse of SiCl₄ and NH₃. Using silicon tetrachloride as the
precursor, silicon nitride thin films were deposited controlling process parameters, such as chamber pressure, temperature, the time and number of the cycles, and the properties of deposited films were characterized by various techniques. Based upon the leakage current data, we optimized the ALD process parameters for the silicon nitride deposition.

**B4.10**

**ARGON ANNEALING-BASED IMPROVEMENTS OF THE PROPERTIES OF ULTRATHIN OXYNITRIDE POST-NITRIDE WITH SiOx / SiO2 / SiOx**

Christopher G. Tskoidze, University of Illinois at Chicago, Department of Chemical Engineering, Chicago, IL.

Thermally grown Si3N4 films in NH3 are known to have a higher dielectric constant and a higher N concentration than silicon oxynitrides, but they incorporate hydrogen atoms that induce hot electron carriers during subsequent high temperature processing. Further, silicon nitride is difficult to grow over 6nm thick, due to self-limiting growth. A low-temperature alternative is SiO2 and Si3N4:O2 films post-nitrided with NH3.

In this work, we study the improvement of the properties of Ar-annealed nitrided oxynitrides as a function of annealing temperature and duration. Secondary ion mass spectroscopy (SIMS) study of the nitrogen profile suggests that there is increased nitrogen removal with increasing annealing time and temperature. Electrical characterization has been performed to find out the total charge density (q/m²) and interface trap density (Dit/cm²) at different processing conditions before and after the annealing step. A post-annealing step is found to remove unwanted hydrogen atoms and improve electrical properties but at the expense of nitrogen removal. An optimization of the annealing process is, therefore, essential in designing nano-electronics with desired nitrogen amount and concentration profiles and in understanding related process-structure-function relationships.

**B4.11**

**LOW TEMPERATURE METAL ORGANIC CHEMICAL VAPOR DEPOSITION OF AL2O3 FOR ADVANCED CMOS GATE DIELECTRICS:**


A low-temperature, metal organic chemical vapor deposition (MOCVD) process for the growth of aluminum oxide (Al2O3) as a potential alternative gate dielectric layer has been developed on 300mm Si wafers. Amorphous Al2O3 films were deposited on [100] oriented p-type silicon [Si] samples employing an aluminum -di-ketoester metal organic precursor [aluminum(III)] 2.4-pentanedionate) and water (H2O) as the aluminum and oxygen sources, respectively. A design-of-experiment (DOE) approach was employed for process optimization. The chemical, microstructural, electrical, and thermal stability properties of the resulting Al2O3 films grown over a temperature range of 250-450°C via this route were studied by x-ray photoelectron spectroscopy (XPS), X-ray diffraction (XRD) measurements, Rutherford backscattering spectrometry (RBS), nuclear reaction analysis (NRA) for hydrogen profiling, scanning electron microscopy (SEM), transmission electron microscopy (TEM), atomic force microscopy (AFM), capacitance-voltage (C-V) and current-voltage (I-V) measurements. An optimized processing window was defined for the growth of dense, amorphous ultrathin Al2O3 films with carbon incorporation as low as 1 atomic % and hydrogen incorporation as low as 0.2 atomic %. The deposited films possess typical dielectric constant values of 7-10. Post-deposition annealing studies indicate that the films chemical and structural properties are stable to temperature of at least 600°C. Thickness control was demonstrated for films as thin as 1.5 nm. Various post-deposition annealing methods were employed in order to improve the electrical properties of ultrathin films. The resulting dielectric constant was as high as 10 and the leakage current behavior was comparable to that of silicon dioxide films of equivalent electrical thickness.

**B4.12**

**TUNING THE MATERIAL AND ELECTRICAL CHARACTERSISTICS OF ZrOx Film Obtained by Plassma Enhanced Chemical Vapor Deposition.**

Byeong Ok Cho, Jieun Kang, and Jane P. Chang, University of California at Los Angeles, Dept. of Chemical Engineering, Los Angeles, CA.

ZrO2 was investigated as a dielectric to replace SiO2 for dynamic random memory (DRAM) capacitor. ZrO2 films were deposited on p-type Si (100) surface using PECVD tetra-borate Zr[OC4H4(O)]4 as an organometallic precursor. Ar to carry the precursor vapor, and O2 as oxidant. We used optical emission spectroscopy (OES), Langmuir probe, and quadruple mass spectrometry (QMS) to characterize the gas phase. Using QMS, we identified all oxidation states of Zr and found that the compositional abundance shifted from Zr metal and monoxide to Zr oxide and trioxide with the increase in O2/Ar flow rate ratio (O2/Ar). Atomic force microscopy and x-ray diffraction results show the Zr02 surface to be smooth with rms 1.4Å as long as O2/Ar was set to over one. X-ray diffraction showed that the films were amorphous. X-ray photoelectron spectroscopy (XPS) and secondary ion mass spectrometry indicated that stoichiometric Zr02 film was obtained with various growth conditions of carbon incorporation depending on the electron temperature and the O2/Ar. We obtained a linear dependence of the carbon content determined by XPS upon the OES intensity ratio of molecular carbon and atomic oxygen. High resolution transmission electron microscopy was used to observe the interfacial layer formation between the deposited ZrO2 and the substrate Si. Fourier transform infrared spectroscopy indicated that the thin non-SiO2. The electrical properties of the non-deposited ZrO2 were assessed by forming Al/ZrO2/Si capacitor structures. We obtained the maximum dielectric constant of 16 at O2/Ar=1. C-V curves shifted to higher bias voltage with increasing O2/Ar, which indicated more negative fixed charges were introduced into the film growth. We observed that the leakage current density decreased drastically with increasing O2/Ar. ZrO2 film at O2/Ar=4 showed 3x10^-10 A/cm² at equivalent oxide thickness of 25Å.

**B4.13**

**ZrO2 GATE DIELECTRICS PREPARED BY ATOMIC LAYER DEPOSITION.**

Jun Park, Bonguk Choi, Nobhak Park and Jiyong Kim, Dept. of Materials Engineering, Kookmin University, Seoul, KOREA.

According to 1999 ITRS roadmap, ultra-thin gate oxide with EOT of less than 12Å are needed for beyond 0.1um CMOS technology. Unfortunately, SiO2 as a gate dielectric has been facing the scaling limitation due to its direct tunneling currents and reliability problems. Therefore, alternative gate dielectric materials have been extensively investigated such as TiO2, Ta2O5 and ZrO2 because of their high dielectric constants. While TiO2 and Ta2O5 have lower barrier heights and they thermodynamically unstable directly on Si during dopant activation annealing, ZrO2 exhibits good thermal stability and high dielectric constant (about 20). In this study, atomic layer deposition (ALD) was used for ZrO2 thin film depositions because its excellent thickness controllability and uniformity due to self-limiting process. At the same time, this method makes it possible to obtain formation of undesirable interface layer during process due to its low process temperature and less of any energetic atom (or ion) bombardment. Zirconium t-butoxide and water were used as Zr and oxygen precursors, respectively. In addition, combinations of NH3, H2 and NH4O or O3 were also evaluated as a co-oxidizer source. The ZrO2 films deposited on p-type (100) silicon were annealed in various ambient, top electrodes were deposited using DC sputtering and a patterned device size is 2x10^-3cm² and then the microstructures of ZrO2 and interface were investigated by ellipsometry, XRD, AFM, TEM, RBS. Also, the electrical properties were assessed by C-V and I-V measurements of Metal-Oxide-Semiconductor (MOS) capacitor structure of Pt/ZrO2/(100) silicon.

**B4.14**


The thermal stability of NiSi films formed on 20 keV BF2+-implanted (100) Si has been investigated. Phosphorus-doped (100) Si wafers with a resistivity of 1-10 Ωcm were used in this study. 20 keV BF2+-implanted was performed at implantation doses of 5 x 1015/cm2 and 5 x 1016/cm2. Some of the wafers implanted at a dose of 5 x 1015/cm2 underwent rapid thermal annealing (RTA) at 850°C for 60s in order to rework the surface amorphous layer (<10hnm thick) and activate the dopants. 350nm thick Ni films were deposited on all samples, including control samples (Si wafers not implanted), by without implanting, by without implanting, by without implanting. Samples were then subjected to 60s RTA at 850-875°C for silicidation. X-ray diffraction (XRD), scanning electron microscopy (SEM), transmission electron microscopy (TEM) and secondary ion mass spectrometry (SIMS) were employed in the analysis of the silicide films. Significant enhancement of NiSi thermal stability by the presence of fluorine in NiSi has been observed. The didecide metal nitride temperature increases to >750°C when NiSi forms on (100) Si implanted with 20 keV BF2+ at an implant dose of 5x1013/cm2. The NiSi films formed on BF2+-implanted Si also exhibit much improved morphological stability. The observed enhancement of NiSi thermal stability is attributed to the retardation of the grain growth, promoted by fluorine decoration of NiSi grain boundaries and NiSi/Si interface. The retardation in the grain growth improves the morphological stability of NiSi films and the improvement in the morphological stability, in turn, suppresses the formation of intermetallic Ni2Si by reducing the number of the favourable sites for Ni2Si nucleation.
D4.15 COMPOSITE X-RAY WAVEGUIDE-RESONATOR AS A BACKGROUND FOR THE NEW GENERATION OF MATERIAL TESTING EQUIPMENT FOR FILMS ON SI SUBSTRATES
Vladimir K. Egorev, Evgeniy V. Egorev, IPMT RAS, Chernogolovka, Moscow Dist., RUSSIA

Planar X-ray waveguide-resonator (PXWR) functioned on total X-ray reflection phenomenon is formed by two plane parallel polished Si plates, previously aligned to be parallel to the dielectric mirrors. PXWR is characterized by a high degree of an X-ray beam compression ($P \sim 1000 \div 10000$) and by low level of its intensity attenuation. The waveguide-resonator captures an X-ray radiation in the angle spread area $\Delta \theta_{\text{in}} \leq 2\theta_{\text{c}}$, where $\theta_{\text{c}}$ is the total reflection critical angle. Classical PXWR design assumes the identity of inlet and outlet waveguide angle apertures and an emergent beam is submitted to limitation $\Delta \theta_{\text{out}} \leq 2\theta_{\text{c}}$. Composite planar X-ray waveguide-resonator (CPXWR) with length $L$ and waveguide separation by distance $\Delta L \leq L$ allow to decrease divergence of its emergent beam. The angle area contraction of CPXWR emergent beam without falling of its total intensity is connected with abrupt decreasing of capture angle for second PXWR inlet of the composite waveguide. There are discussed examples of CPXWR practical applications for diffractometry of polycrystal and epitaxial film structures on Si substrates, TXRF spectrometry and X-ray reflectometry of the thin film materials.

D4.16 EFFECT OF POLYSILICON ANNEAL ON GATE OXIDE CHARGING DAMAGE IN POLYSILICON GATE PATTERNING PROCESS, Daniel Chong, Wen Jong Yoo, National University of Singapore, Dept of Electrical and Computer Engineering, SINGAPORE; Lap Chan, Alex See, Chartered Semiconductor Manufacturing Ltd, Technology Development, SINGAPORE

Polysilicon film anneal is performed prior to polysilicon gate etch in certain process flows to achieve part of the implanted dopants inside the polysilicon gate oxide. This technique forms the first part of a two-step annealing/activation process for the polysilicon gate oxide. The second part of this two-step annealing process is performed during the source and drain junctions anneal. The reason for having a two-step polysilicon gate electrode annealing process is such that the thermal budget required to activate the source and drain junctions can be kept relatively low without affecting the resistivity of the gate electrode. Thermal budget for source and drain junctions anneal/activation is kept low to obtain shallow junction devices. Device or transistor wafers are fabricated using the 0.15 μm technology process flow. Transistors in the test structures are n-channel devices with gate oxide thickness of 20Å. The dimension of the gate oxide is 0.15 μm x 1.0 μm. The thickness of polysilicon film is 2000Å and the implanted phosphorus dose is 5.5x10^10 cm^-2. An experimental split is performed at the polysilicon film anneal step. One set of wafers undergoes this step, while another set skips it. Polysilicon film anneal is carried out in N2 ambient at 800°C for a 15 minutes time duration. Our study shows that this two-step polysilicon gate electrode annealing process does have some effect on gate oxide charging damage. Gate oxide charging damage is increased with the inclusion of the polysilicon film anneal step prior to gate patterning.

D4.17 ELECTRICAL CHARACTERISTICS OF SILICON IMPLANTED NANOCRYSTAL MEMORY IN SILICON NITRIDE-SILICON DIOXIDE STRUCTURES, T.S. Kalmar, Department of Electrical and Computer Engineering, University of Colorado, Colorado Springs, CO; Nathaniel M. Pendley, Armel Corporation, Colorado Springs, CO.

Recently, metal-oxide-semiconductor structure field effect transistors based on silicon implanted nano-crystals are attracting the attention of many researchers for the fabrication of nonvolatile memories. In this paper we are presenting the results of non-volatile memory characteristic of heavy dose silicon implanted (1e16 per cm²) silicon nitride-silicon dioxide structures.

Polysilicon-implanted nano-crystal-silicon dioxide structures were fabricated with silicon implanted nano-crystals have been fabricated and were characterized by capacitance-voltage and current-voltage measurements. These structures show hysteresis in their capacitance vs voltage characteristics which might be due to charge trapping at the silicon nano-crystal-silicon dioxide interface.

D4.18 DEGRADATION STUDY OF ULTRA-TIN JVD SILICON NITRIDE MNSFETS, K.N. ManjulaRani, V. Rangopal Rao and J. Vani, Department of Electrical Engg, Indian Institute of Technology, Mumbai, INDIA

Jet Vapour Deposited (JVD) silicon nitride has emerged as a viable alternative to SiO₂. It has been shown that JVD silicon nitride has excellent hot-carrier capabilities. In this paper, we report the degradation due to current limited constant voltage stress in JVD Metal-Nitride-Semiconductor FETS (MNSFETS). The devices used in this study are n-channel MNSFETS with an Equivalent Oxide Thickness (EOT) of 3 nm. The devices were fabricated in UCLA with the JVD deposition done at Yale University. Breakdown stress or slow traps seem to play an important role in silicon nitride MNSFETS. We have developed a simple but accurate method of characterizing border traps using hysteresis in drain current of MNSFETS. This method can be used to characterize border traps in similar devices as well. We will compare these results with those obtained by variable frequency charge pumping method. In addition to the border traps, the effect of stressing on $V_{th}$ and $N_{ox}$ are also reported. In ultrathin MNSFETS, the effect of Stress Induced Leakage Currents (SILC) and Soft Breakdown (SB) also become very important. SILC causes increase in leakage currents at low fields and is especially important for JVD MNSFETS. We have observed that the JVD MNSFETS show very little increase in SILC after stressing. Next we look at Soft Breakdown characteristics of JVD MNSFETS. Noise in the gate current (observed in the Ig-Vg characteristics) is the most widely used method to characterize SB. In addition to this, we have also used gate current transients before and after stress at sufficiently low voltages to detect SB. We have observed Random Telegraph Noise (RTN) like behaviour after soft breakdown. In ultrathin SiO₂ MOSFETS, it is observed that although soft-breakdown increases the noise in currents, it does not effect the device performance. We have also observed that there is hardly any effect of SB on the device performance of JVD MNSFETS.


The use of high-κ materials as gate dielectric has received considerable attention for CMOS scaling. For successful scaling into the mainstream technology, the short channel performance of MOS transistors with high κ gate dielectrics must be compared with the conventional SiO₂ at identical equivalent oxide thickness. It has been shown recently that the short channel performance worsens for High-κ dielectric MOSFETS as the physical thickness to the channel length ratio increases, even when the effective oxide thickness is kept identical to SiO₂. In this work, we have systematically evaluated using 2D simulations the effective dielectric thickness for different Kₚₑₜ, to achieve the targeted threshold voltage ($V_{th}$), drain-induced barrier lowering (DBL) and $I_{OFF}/I_{on}$ ratio for different technology generations down to 50 nm, following the SIA roadmap specifications. Our results clearly show that high-κ and SiO₂ follow different trends and the fringing field effects play a major role. The variation of $V_{th}$ and SiO₂ follows different trends and the fringing field effects play a more significant role for high-κ dielectrics than for SiO₂. This degradation becomes even more significant for sub 50 nm technologies. This paper summarizes the possible scaling limits for high-κ dielectrics with the help of systematic 2D simulations for channel lengths down to 50 nm, and with gate dielectric constant varied over a wide range, keeping in mind the high-κ dielectrics currently being investigated by various research groups.

D4.20 CHARACTERIZATION FOR HIGH-K AND POROUS LOW-K THIN FILMS BY GRAZING INCIDENCE X-RAY SCATTERING, K. Nomura, A. Takasa, and Y. Ito, X-Ray Research Laboratory, Rigaku Corporation, Tokyo, JAPAN

Atomic scale structure of thin high-k dielectric is essential to the properties of films. It is believed that amorphous structure is suited for the gate dielectrics. Although X-ray scattering technique is useful to characterize such a structure, it is hard to measure the diffraction peaks of ultra-thin film with thickness below 10 nm by conventional 2θ-ω method. Grazing incidence in-plane diffraction has high surface sensitivity and able to detect film peaks even though the thickness is less than 1 nm. By using in-plane geometry, we have successfully obtained the SiO₂ diffraction down to 1 nm film thickness and detected the structural change by thermal annealing. In addition, we have also analyzed film stacking and interfacial structure of the ZrO₂ film in subnanometer scale by grazing incidence x-ray diffraction and x-ray reflectivity measurement (XRR). Combination of these two techniques, we could determine precise structure of ultrathin high-k dielectric films.
will also present the method for determining pore-size distribution in porous low-k dielectric films by grazing incidence x-ray scattering. The technique is added to use the methylene blue adsorption (MSA) films. The pore size distributions determined by the x-ray scattering technique agree with that of the commonly used gas adsorption technique. The x-ray technique has successfully determined small pores down to sub-micrometers in diameter, which is well below the lowest limit of the gas adsorption technique.


Current silicon transistor technologies are nearing the physical limits of miniaturization using SiO2 as the gate dielectric, therefore alternate high-k dielectric materials are desired. Pulsed laser deposition (PLD) is an important tool for formation of thin films of these potential alternate high-k dielectric layers on silicon wafers. However, during deposition and annealing of ZrO2 and Y2O3 films by PLD, an interfacial layer formation was noted. This layer has detrimental effects on the overall capacitance properties of the film. This presentation explores the kinetics of the formation of this interfacial layer and ways to impede its formation. Samples of both ZrO2 and Y2O3 films were deposited using a pulsed laser deposition technique and were post-annealed in various atmospheres, at different temperatures, and with increasing times. Using several characterization techniques, the thickness, uniformity, and bonding environment of the interfacial layer were determined. The results were used to model the kinetics of the formation of high-k dielectric films. These comparisons were made of samples deposited on top of a thin nitride layer formed by heating in a nitrogen environment to study the nitride effectiveness in slowing the interfacial layer growth.

D4.22 REDUCTION PLASMA-ENHANCED CHEMICAL VAPOR DEPOSITION OF SILICON NITRIDE AT ATMOSPHERIC PRESSURE. Greg Nowling, Steve Babayan, Vladimir Jacklevic, and Robert Hicks, University of California, Los Angeles, Dept of Chemical Engineering, Los Angeles, CA.

Silicon nitride is widely used in silicon microelectronics as barrier layers, packaging, insulation, and novel dielectric structures. We have deposited high-quality silicon nitride films using a novel atmospheric-pressure plasma source. This source is operated without vacuum chambers and associated hardware, and represents a low-cost alternative to the equipment currently used for semiconductor processing. The atmospheric-pressure discharge was produced by flowing nitrogen and helium through two perforated metal electrodes that were driven by 13.56 MHz radio frequency power. Deposition occurred by mixing the plasma effluent with silicon and directing the flow onto a rotating silicon wafer heated to between 1000 and 5000 degrees C. Films deposited ranged in thickness from 100 angstroms to 1000 nm. Varying the nitrogen/Air/H2 feed ratio from 43,000 to 4,300 caused the film stoichiometry to shift from Si3N4 to SiN2. Minimum impurity concentrations of 0.04 ppm carbon, 3.03 ppm oxygen and 13.0 ppm hydrogen were achieved at 5000 degrees C and an nitrogen/Air/H2 feed ratio of 17,000. The growth rate increased with increasing silicon and nitrogen partial pressures, but was invariant with respect to substrate temperature and rotational speed. The deposition rate also decreased with distance from the plasma. These results, combined with emission spectra taken of the afterglow suggest that the plasma effects between nitrogen atoms and silicon play an important role in this process. At the meeting, we will further discuss the properties of the films, and their potential application in Si devices.

D4.23 HIGH-K FILMS FORMED BY THERMAL AND UV ASSISTED INJECTION LIQUID SOURCE, CVD. PK. Hurley, B.J. O'Sullivan, NIMRC, University College, Cork, IRELAND; H. Rousell, F. Rousell, J.P. Semenauer, M. Audier, C. Desbadeleau, INPG, Grenoble, FRANCE, Q. Fang, J. Wang, University of Toronto, LONDON, London, UNITED KINGDOM; T.L. Leedham, Inorganic, Suffolk, UNITED KINGDOM; C. Jimenez, J. Pichel, Crolles, FRANCE.

In this abstract we present the first results of HfO2 films formed by thermal and UV assisted injection liquid source, chemical vapour deposition. Using a liquid injection system HfO2 films have been fabricated using a mixture of tetrakis(hydrazono) hafnium (Hf(CH2NH2)4) precursor in a hexane solvent. HfO2 films with thicknesses varying from 20-100 nm were formed over a range of temperatures (320-550°C) and deposition environments (O2, Ar, Ar+O2, Ar+H2). HfO2 films have also been formed (10-20 nm) using UV excimer lamp (242 nm) assisted, injection liquid source, CVD. For the initial studies relatively thick films (20-100 nm) were deliberately chosen to minimize interface effect and allow analysis of the bulk film composition. In both cases the substrates were Si(100), with approximately 1 nm chemical oxide present prior to deposition. The liquid injection source can control the HfO2 growth rate determined to be in the range of 0.1 nm per injection, demonstrating atomic layer control using this technique. The films were analysed physically using XRD, FTIR, SIMS, N2MS and RBS, identifying the films as HfO2 with carbon at 1-2 at.

Both polycrystalline (T>365°C) and amorphous films (T<320°C) were formed. The polycrystalline structure is identified as monoclinic. The deposition efficiency (deposited film thickness/precursor mass in) is estimated to be a strong function of temperature, but essentially independent of ambient. Electrical characterisation was performed using either a mercury probe or aluminium dots evaporated through a shadow mask. High frequency C-V analysis reveals effective electric constants in the range 16-20, with breakdown fields in excess of 5MV/cm. The effect of post deposition UV O2 annealing (350°C), and the effect of injection frequency, will also be presented.

D4.24 ELECTROLUMINESCENCE PROPERTIES OF INDUMIN-TIN-OXIDE/EMBEDDED SI NANOCRYSTALLITES IN SiO2. P TYPE SI/METAL STRUCTURE PREPARED BY PULSED LASER DEPOSITION. Jong Hoon Kim, Kyung Ah Jeon, Jin Back Choi, Seol Yool Lee, Department of Electrical and Electronic Engineering, Yonsei University, Seoul, KOREA.

Nano-crystalline Si (nc-Si) on p-type Si substrate and indium-tin-oxide (ITO) have been prepared by pulsed laser deposition technique using a Nd:YAG laser with the wavelength of 355 nm. Biaxial pressure was maintained at 1-10^5 Torr. Nano-crystalline Si thin films are deposited in a CVD chamber, using a thermal source, as well as in nitrogen gas. Strong violet-indigo luminescence from Si nanocrystallites has been observed at room temperature by photoluminescence (PL). Dependence of the electroluminescence (EL) properties on various deposition conditions will be discussed using ITO/nc-Si/p-type Si/metal structure.

D4.25 EVOLUTION OF SPUTTERED HfO2 THIN FILMS UPON ANNEALING. Seok Won Nam, Jung Ho Yoo, Seohun Nam, Dae Hong Ko, Dept. of Ceramic Engineering, Yonsei Univ., Seoul, KOREA; Jn Hnm Ku, Siyoung Choi, Samsung Electronics Co., Ltd., KOREA.

We investigated the evolution of the physical and electrical properties of HfO2 thin films deposited by the reactive DC magnetron sputtering method on the (100) silicon substrate upon annealing. The HfO2 thin films deposited at room temperature were amorphous, while the films after annealing were polycrystalline. The crystallization temperature of the HfO2 thin films was dependent on the annealing methods (RTA or Furnace) and ambient (nitrogen or oxygen). The microstructures of HfO2 thin gate oxides <15A thick were analyzed by HRTEM, XRD and AES. We also focussed on the interfacial layer between HfO2 thin films and silicon substrates. Due to its high oxygen diffusivity, any antrigogs lead to oxygen diffusion out of 15A to 25A. The EOT decreased upon annealing due to the increased SiO2-containing layer. The HfO2 thin films deposited at room temperature have the undesirable interfacial states due to the surface damage by sputtering. We found that the HfO2 thin films <15A thick were oxidized by RTA or furnace annealing.

D4.26 FLAT BAND VOLTAGE, HYSTERESIS AND BREAKDOWN OF HAFNIUM SILICATE PREPARED BY PVD TECHNIQUE. Hong-Hua Zhang, Guang-Ping Sun, Mei-Mei Quevedo-Lopez, Prakapen Chaketch, Bruce E. Grade, Robert M. Wallace, The Lab of Electronic Materials and Device, Dept. of Materials Science, Univ. of North Texas, Denton, TX.

The shift in flat band voltage (Vb) and hysteresis observed on MOS capacitors prepared by PVD techniques are examined for [100] orient nitric-silicon substrate. Using a Pt/Al gate C-V system, the Vb shift can be attributed to changes in the working function of gate metal and the electronic properties of oxide layer, as had previously been reported. In addition, this work indicates that the Vb shift results from a reduction of interface state and oxide fixed charge due to the different forming gas annealing temperatures. The obvious hysteresis shows that the existence of large amount of trapping or detrapping defects in the oxide layer. The interface state and oxide charge densities are calculated and related to the available bands at the interfaces. The breakdown experiments confirm that the Vb shift for the MOS samples is mainly due to a reduction of oxide fixed charge in the oxide annealed in higher temperature, and to a lesser degree, to a reduction of interface charge.

D4.27 THE METAL INDUCED LATERAL CRYSTALLIZATION OF AMORPHOUS SILICON THIN FILMS BY ALTERNATING...
In silicon doping in transistor the Fick’s law of Diffusion is not adequate representation. This is because; a) mathematically it is poorly convergent at the short time limit for surface flux and b) physically it implies a infinite velocity of mass. The hyperbolic mass wave equation can represent the finite speed of propagation of mass which is realistic. Nothing is faster than the speed of light. The ‘only’ modification that will retain the single and derive second derivative in time in the hyperbolic partial differential equation. The problem of quenching a finite slab with both the ends of 1 dimension brought to Cl the bath temperature from a initial C. The non-dimensionalized vars in the form of x = x/Λ, t = t/Λ², u = U/Λ. The symmetry boundary condition at the center of the slab yields a slope of zero. The separation of variables technique is used to get the cosine series in x with bounds being 2(1/2π) and t = (t/Λ²)/α. The time domain is represented by a second ODE. The solution gives a complex representation whose real part yields a cosine term in which yields a periodicity to the temperature solution damped by a decaying exponential. This boundary value problem is solved for by integration and is (1 + t⁻¹)/n. This analytical solution can be used to predict the transient heat transfer in 1-dimension.

B4.41 GRAZING ANGLE INCIDENCE X-RAY DIFFRACTION BY THE SiGe/Si HETEROJUNCTION WHERE THE GERMANIUM AND THE CARBON CONCENTRATIONS ARE PERIODICALLY VARYING ALONG THE FLAT LAYER SURFACE.

Hayed H. Bezinджyanyan [ Jr.], Yerevan State Univ, Faculty of Informatics and Applied Mathematics, Yerevan, ARMENIA; Siranush E. Bezinʤyanyan, Hakob P. Bezinʤyanyan, Yerevan State Univ, Faculty of Physics, Yerevan, ARMENIA.

Evolution of the coherent part of x-radiation scattered by strained or relaxed crystalline, as well as amorphous flat Si[1x]Ge[4-x] layer deposited on the silicon substrate is presented in [1], and it is pointed out the possibility of the direct Grazing-angle Incidence X-ray Diffraction (GIXD) experimental investigations of the long-period structured intermediate transformation states of Si[1x]Ge[4-x] layer, which are emerging due to periodicity of the strain field along the substrate-layer interface. The measurement was done based on the theoretical method presented in [2]. The Si:C bond length is much smaller than the bond lengths in a Si[1x]Ge[4-x] alloy, therefore a small amounts of carbon atoms provided an additional design parameter in manipulating the strain [e.g. see [3]], i.e. the effect of the increase of the average lattice constant due to germanium atoms can be compensated by adding the carbon atoms in the heterostructure. While studying the influence of carbon in Si[1-x]Ge[4-x] layer, it is also important the investigation of the behavior of the ternary strained Si[1-x]Ge[4-x] layers [e.g. see [4, 5]]. In this paper we present the GIXD theoretical curves of a thin flat Si[1-x]Ge[4-x] layer deposited on a thick silicon perfect-crystal substrate. The diffraction curves due to a specific long-range order in a layer e.g. through harmonic variations of the germanium and carbon composition coefficients in the heterostructure. References: 1. P.A. Bezinʤyanyan [ Jr.], A.P. Bezinʤyanyan, SE. Bezinʤyanyan and K.O. Hrnciar, Grazing Angle Incidence X-ray Diffraction Curves of Si[1x]Ge[4-x] Thin Layer if the Composition Coefficient x is Varying Harmonically Along the Film Layer Surface, the Book of Abstracts of 10th International Conference on X-ray Optics and Microanalysis (ICXOM XVI), Vienna, Austria 2001, p.57. 2. A.P. Bezinʤyanyan and P.A. Bezinʤyanyan, Solution of the Two-dimensional Stationary Schrödinger Equation with Cosine-Like Coefficient [in View of X-ray Diffraction], Phys. Stat. Sol. (a), 105 (1988) 353-355. 3. B. Dietrich, H.J. Osten, H. Bückler, M. Methfessel, and P. Zmuidzinas, Lattice Distortion in a Strain-Compensated Si[1-x]Ge[4-x] Layer in Silicon, Phys. Rev. B, 34/2 (1994) 1785-1790. 4. G.G. Fischer, P. Zmuidzinas, E. Bugiel, and H.J. Osten, Investigation of the High Temperature Behaviour of Strained Si[1-x]Ge[4-x] Layers, J. Appl. Phys., 77/5 (1995) 1964-1937. 5. H.J. Osten, D. Endisch, E. Bugiel, B. Dietrich, G.G. Fischer, Myungcheol Kim, D. Kruger, and P. Zmuidzinas, Strain Relaxation in Ternary-Strained Si[1-x]Ge[4-x] Layers on Si[001], Semicond. Sci. Technol., 11/11 (1996) 1626-1628.

SESSION B5 - DIELECTRIC CHARACTERIZATION
Chair: David O’Meara
Wednesday Morning, April 3, 2002
Salon 10-12 (Marriott)

8:00 AM B5.1
effect of CARBON AND POROSITY ON ADHESION AND DEBINDING OF CARBON-DOPED OXIDE FILMS.

Dong-Ick Lee, Reinhold H. Dunschmidt, Materials Science and Engineering Dept, Stanford Univ, Stanford, CA.

B4.28 THERMAL STABILITY AND DIELECTRIC PROPERTY OF STACKED HIGH-K DIELECTRICS ON SILICON Y-S. Lin and J.P. Chang, Department of Chemical Engineering, University of California, Los Angeles, Los Angeles, CA.

Recognizing the need of using novel high-k dielectric materials for the next generation of high-density memory devices, we have been developing silicon nitride based thin films deposited by plasma-enhanced chemical vapor deposition. The thermal stability of SiO₂, the electric stability of the material and the dielectric breakdown will be discussed.
As the size of microelectronic devices decreases dramatically, the RC delay above the bias decreases in the VLSI technology. Accordingly, large effort is being made on the interlayer dielectrics such as carbon-doped oxides which have the lower dielectric constant than the silicon dioxide constant, \( \varepsilon_r = 3.9 \). However, since the alky group in the silicon dioxide backbone, the volume expansion and the interface characteristics are becoming inferior. This is caused by the disruption of the glass network. This phenomenon is led to inferior mechanical properties such as the fracture toughness, modulus and hardness which are closely related to the reliability of the microelectronic devices. On my study the interface debonding and failure between the dielectric and adjacent layers in the multi-layer stack of thin film will be focused. Those failures are caused by the film stress and residual stress between the films. Within the Linear Fracture mechanics technique the energy, termed as the critical strain energy release rate or the interface debonding energy, which is needed to detach the dielectric film from the adjacent film can be determined. The energy is calculated from the deformation of the bond around the interface as well as the plasticity in adjacent layers. Since inorganic silicate behaves like a completely brittle material, the carbon-doped oxide film is expected to behave in the same manner. Therefore the fracture energy of the interface is sensitive to the interface chemistry and glass composition. The subcritical debonding is also concerned in terms of reliability. Under the environment of high humidity and temperature crack can be growing with much less driving forces. This can cause the problem to the microelectronic devices. Two kinds of ways of making carbon-doped oxide film are used. Those are spin-on glass and CVD method. To measure the critical strain energy release rate, 4-point bending and other method have been confirmed. Those methods are characterized, the resulting fracture surfaces were characterized by XPS scans to determine the debonding path. From the data obtained it was clarified that the fracture toughness is decreasing with the carbon content in glass matrix whatever kind of alky group is. Moreover the debonding interface for CVD method is mostly happened on the lower interface between dielectric and silicon nitride layer by XPS scanning. It is explained that the fracture mode is the mixed mode so that the crack is growing downward as well as forward. For future work, the various kinds of functional groups can be grafted in the silicate and tested and moreover the subcritical cracking can be induced by many degrees of humidity and temperature situation. Finally, the relationship between the glass composition and structure and the resulting mechanical properties can be elucidated.

8:15 AM D5.2 SYNTHESIS OF ORDERED NONPOROUS SILICA FILM WITH HIGH STRUCTURAL STABILITY. Norikazu Nishiyama, Shunaku Tanaka, Kokekusu Uemaya, Osaka University, Dept. of Chemical Engineering, Osaka, JAPAN; Yoshihiko Oka, MIYAL-SET, Tukuba, JAPAN; Akira Kanamatsu, Rohm Co Ltd, Tokyo, JAPAN.

In this study we synthesized nonporous silica films with high structural stability on a silicon wafer. The silica wafer was coated with a precursor solution by a spin-coating method. The XRD pattern of the films showed that highly ordered silica was formed on the silicon wafer. The [110] reflection peak was not observed in the XRD pattern showing that the straight pore channels were oriented parallel to the support surface. This result is contrary to the ordinary viewpoint of the requirement of the orientation of the surface molecule. The film formation on silicon wafer was investigated. The formation of a silica network is thought to be insufficient because the reaction rate of the condensation of silanol groups is not high at low temperature. To complete the condensation of a silica network, a post-synthesis treatment was carried out. Then the calcination was conducted at 620 K for 5 h to remove surfactant molecules. No peak shift of the [100] reflection was observed in the calcined silica film. The peak intensity did not decrease, indicating high structural stability of the treated silica film. The FE-SEM images of the cross section of the treated silica film showed that its thickness is about 300 nm. The periodic porous structure can be observed in the cross section of the silica film. This can be attributed to the results of the XRD patterns, which indicate that the straight pores were oriented parallel to the surface of the silicon wafer. The periodic ordered structure of nonporous silica gradually collapses under water vapor in the atmosphere. In this study, the silica films were synthesized under water vapor to enhance the resistance against water vapor. The pore surface effectively increased its hydrophobicity by silylation. The ordered structure of the silylated silica film was maintained under saturated water vapor at 333 K.

8:30 AM D5.3 HIGH QUALITY ZrO_2 GATE DIELECTRIC FOR SiGe MOS DEVICES. Chaegyu Lee, Sae-Bum Hong, Sung-Hoon Jeon, and Hyunseung Herang, Kwangju Institute of Science and Technology, Dept. of Materials Science and Engineering, Kwangju, KOREA.

Considering high hole mobility of strained SiGe/Si heterostructure, CMOSFET utilizing SiGe/Si heterostructure is promising for future high speed device. However, a conventional high temperature thermal oxidation for gate dielectric is not compatible with SiGe heterostructure because of strain relaxation and Ge segregation effect. Improvement of carrier mobility of SiGe MOSFET, SiGe/Si heterostructure, is limited because silicon capping layer reduces Ge segregation and interface roughness during the thermal oxidation. Recently, the ZrO_2 film was investigated as a promising alternative gate dielectric for silicon MOS devices. We report on the silicon oxide electrical characteristics of ZrO_2 on SiGe MOS with silicon capping layer. Epitaxial 35nm-thick Si$_x$Ge$_{1-x}$ strained layer was grown on p-type silicon wafer. For comparison, 7nm-thick epitaxial silicon capping layer was grown for some samples. Various thicknesses of ZrO$_2$ layer was deposited by atomic layer deposition followed by wet vapor annealing at 820°C. After the deposition of a 15nm-thick layer of Pt MOS devices with a gate area of 9 $\times$ 10$^{-4}$ cm$^2$ were defined. The wet vapor annealing of ZrO$_2$ which can be explained by the reduction of oxygen vacancy of as-deposited ZrO$_2$. Compared with ZrO$_2$ directly deposited on SiGe, ZrO$_2$ deposited on silicon capping layer exhibits a significant improvement of electrical characteristics such as leakage current, low hole charge density, and low interface state density. The improvement of electrical characteristics of sample with silicon capping layer can be explained by negligible Ge segregation.

8:45 AM D5.4 CHARACTERISTICS OF ZIRCONIUM BASED AMORPHOUS THIN FILMS FOR GATE DIELECTRIC APPLICATIONS. Chang-Hye Jeon, Seong-Hee Kang and Jiyoung Kim, Dept. of Materials Engineering, Koekjin University, Seoul, KOREA.

Considering high leakage currents of thermal SiO$_2$ films with thickness less than 20 nm, development of high-$k$ films for gate dielectric applications is necessary to scale device dimension down to 10 nm. Alternative gate dielectrics should simultaneously satisfy several harsh requirements, such as a high dielectric constant, a low leakage current, a good thermal stability on Si substrate and, excellent interface characteristics, etc. Even though various high-$k$ materials have been studied in order to replace conventional thermal oxide, most of them show a trade-off. Uninary metal oxides such as TiO$_2$ and ZrO$_2$ are easily transformed from amorphous to crystalline during dopant activation annealing. Since polycrystalline thin films have lots of grain boundaries, amorphous phase is relatively preferred. On the other hand, silicon such as ZrSiO$_2$ shows excellent thermal stability. However, the siliconites have relatively low dielectric constants (13-14). In order to realize use of the siliconite as an alternative dielectric, dielectric constant should be improved. In this study, we evaluate the effects of composition between Zr and Si on thermal stability and dielectric constants. In addition, effect of Al and Bi as novel glass network formers are also evaluated. Amorphous thick films were deposited by reactive co-sputtering because of its easiness on compositional change. However, reactive sputtering easily causes undesirable interfacial layers. In this study, various treatments such as nitridation were employed in order to reduce the interface layer. The deposited films are annealed at various ambient and then Pt top electrodes are formed. We will extensively report the effects of composition of Zr based glassy thin films on thermal stability and dielectric behaviors on Si substrate.

9:00 AM D5.5 MOLEULAR LAYER DEPOSITION OF ULTRATHIN ZIRCONIA FILMS ON SI CONDUCING POLYNUCLEAR METAL ALKoxide PRECURSORS. Jason Lee, Walter G. Klemperer, University of Illinois, Frederick Seitz Materials Research Laboratory and Department of Chemistry, Urbana, IL; Erik A. Urban, David A. Pogue, University of Illinois, Frederick Seitz Materials Research Laboratory and Department of Materials Science and Engineering, Urbana, IL.

Conventional atomic layer deposition provides a viable route to high-$k$ dielectric films on silicon. In order to reduce the number of growth cycles required, we have investigated the use of polymeric metal alkoxide precursors capable of reacting in a single reaction step. Ultrathin zirconia films have been deposited on silicon using a tetrameric zirconium alkoxide precursor, Zr$_4$(OPr$_3$)$_4$, in fluid solution. Films with equivalent oxide thickness less than 2.0 nm and low leakage currents less than 1.0 x 10$^{-6}$ A/cm$^2$ at 2.0 V were obtained using this process.


Currently there is still no clear front runner for the next alternative gate dielectric despite extensive efforts. Much of the material
research and integration development are focused on transition metal oxides and silicates, rare earth metal oxides and other oxides. This paper addresses some recent experimental studies on the optical properties of HfO$_2$ films grown on Si by CVD and ALD. Extensive structural, compositional, and optical characterization has been performed using TEM, AFM, RBS, SIMS, AES, XRD, XPS, and optical transmission and reflectance spectroscopy techniques. Issues related to impurities, interfacial layers, and thermal stability will be addressed.

New characterization method such as tunneling AFM has been developed to correlate electrical “hot spots” with film structures.

**10:00 AM B5.7**

**ATOMIC LAYER DEPOSITION (ALD) OF METAL SILICATES AND OXIDES FOR HIGH-K INSULATORS IN GATES AND Capacitors**

Roy G. Gordon, Jill Becker, Eric Greynson, Dennis Hausmann, Esther Kim, Segi Suh and Ying Wang, Harvard University, Dept of Chemistry and Chemical Biology, Cambridge, MA.

New processes are studied for ALD of silicates and oxides of the metals lanthanum, zirconium, hafnium, and tantalum. For deposition of metal silicates, the silicon and oxygen source is tris(tertiobutylsilanediyl)hafnium (Hf$_3$(O)$_4$(Si)$_2$). Pulses of silane vapor and metal alkyl vapor are introduced alternately and separately into the heated deposition zone where they react on the surfaces of substrates. For the deposition of metal oxides, the metal alkyls are reacted with water vapor instead of the silane. Each of these reactions is shown to be self-limiting within a certain range of substrate temperatures. Excellent step coverage and high uniformity of thin films are found for films deposited within temperature ranges. By using both silane and water pulses in various ratios, various compositions are deposited with silicon to metal ratios ranging from zero up to about 4. The surfaces of the films are quite smooth, with rms roughness by AFM less than 1% of the thickness. The stoichiometry and kinetics of the surface reactions are studied with a quartz crystal microbalance. The oxide reactions may be remarkable fast, while the silicate reactions require a higher flux to reach saturation.

**10:30 AM B5.8**

**CHARACTERIZATION AND ELECTRICAL PROPERTIES OF ULTRA THIN HfO$_2$ GATE DIELECTRICS PREPARED BY ATOMIC LAYER DEPOSITION**

Tae Ho Lee, Joemin Oh, Hanyung Univ, Dept of Materials Science & Engineering, Seoul, KOREA; Younghee Kim, Dongki Choi, Hanyung Univ, Dept of Ceramic Engineering, Seoul, KOREA; Jiahun Jung, Eunheuk Corp, Sungnam-City, Kyunggi-Do, KOREA; Jinho Ahn, Hanyung Univ, Dept of Materials Science & Engineering, Seoul, KOREA.

For the future integrated circuit manufacturing, new materials and thin film deposition methods will be needed for gate dielectric preparation. Among the various deposition methods, atomic layer deposition (ALD) is the method of the most promise for meeting the strict requirements in the future IC manufacturing. However, the evolution of this ultra thin dielectric film is cumbersome and sometimes difficult. In this research we have investigated the growth mechanism of ultra thin HfO$_2$ film using several analytical techniques. HfO$_2$ films were deposited in a traveling wave type ALD reactor (Puls 200) using HfCl$_4$/H$_2$O as precursors and N$_2$ as a carrier/gas gaseous. HfCl$_4$ was volatilized in a carrier at 200°C and injected into the reaction chamber, where N$_2$ carrier gas. H$_2$O carrier was kept at 120°C and carrier gas was not used. The films were grown on 8-inch [100]-type silicon wafer in the temperature range of 200-400°C after standard RCA cleaning. Spectroscopic ellipsometry, XRD and TEM were used to investigate the initial growth mechanism and microstructure. The chemical composition of deposited film was analyzed by RBS and XPS. The electrical properties of the film were measured and compared with the physical and optical properties. The electrical properties of the film are dependent on substrate effects, deposition temperature, and precursor injection time. The breakdown field strength of the films will be discussed. Also, the comparison of the evaluation results from the several analytical techniques will be addressed. The effects of oxides or silicides on the electrical properties will be discussed based on the bulk and interfacial structure of the HfO$_2$ film.

**10:45 AM B5.9**

**REACTION BETWEEN POLYSILICON GATE ELECTRODES AND HIGH-K La$_2$O$_3$-Si LAYERS:**

M.J. Kelly, T. Gougoussi, K. Berg, W.S. Burns, J.M. Bennett, T.L. Schmit, and G.N. Parsons, Dept. of Chemical Engineering, NC State University, Raleigh, NC.

Stability of gate electrode materials on high-k dielectrics is a critical issue for advanced gate stacks. For this study, lanthanum silicate dielectrics were prepared by oxidation of PVD La on silicon using two slightly different preparation processes. At the same time, Process (A) resulted in film with no visible OH in the infrared absorption spectrum, and Process (B) resulted in a film with a small amount of OH visible in the IR. The only difference between process A and B was the change in preparation before deposition of synchrotron vacuum ultraviolet (UV) photoelectron spectroscopy (UPS) and X-ray Photoelectron Spectroscopy (XPS) analysis of as-prepared films indicated no significant difference between the two processes. Two samples of each process were prepared, and all samples showed consistent results. Thin (300Å) amorphous La$_2$O$_3$ layer was deposited on all samples. AFM analysis indicated that the thickness was sufficient to achieve complete surface coverage, but the film was thin enough to enable analysis of the top poly dielectric interface by XPS. XPS data was collected with the top metal deposited, and after several high temperature annealing steps (temperatures ranging from 650 to 1050°C) when the polysilicon on the bare wafer sample (process B) was amorphous, XPS showed oxidation of the exposed polysilicon surface, with no significant change in the lanthanum related features. However, for the films that contained hydroxide (process B), XPS results show significant changes in the Si 2p spectrum, suggesting that the thin polysilicon layer reacts with the oxide polymer layer during the anneal step leading to consumption of the polysilicon. These results are consistent with excess oxygen (in the form of water vapor) promoting a reaction between the metal oxide and polysilicon. Impedance stability between high-k dielectrics and polysilicon gate electrodes will be discussed.

**11:00 AM B5.10**

**INTERFACE PROPERTIES OF YTTRIUM OXIDE HIGH DIELECTRIC CONSTANT INSULATORS DEPOSITED BY OXYGEN PLASMA ASSISTED CHEMICAL VAPOR DEPOSITION:**

D. Niu, R.W. Ashcraft, and G.N. Parsons, Dept. of Chemical Engineering, NC State University, Raleigh, NC.

Controlling interfacial and bulk chemical stability of CVD high-k dielectrics is a critical issue for advanced gate stacks, but the mechanisms that control the interfacial stability are not well understood. We have studied deposition of yttrium-based high-k dielectrics formed by oxygen plasma assisted CVD at temperatures between 350 and 450°C using a yttrium diloxaneate precursor introduced downstream from a remote oxygen plasma. Physical film thickness ranged from <40Å to >1000Å, and films were characterized using HR XPS, TEM, EELS, and IV and CV electrical analysis, before and after annealing at temperatures up to 1000°C. XPS and TEM analysis indicate that during initial film deposition, significant mixing occurs between the initial deposited Y-containing layers and the silicon substrate, leading to a mixed Y-O-Si (silicate) layer at the interface with thickness >10Å. Continued film growth result in Y$_2$O$_3$ formation on top of the interface silicate. Over a wide range of thickness, as deposited films show evidence for O-H and C-H bonds in the IR spectra, and the O-H peaks grow over time. After annealing at 900°C in N$_2$ (with >15 Torr O$_2$ pressure), the IR shows almost complete removal O-H and C-H bonds, and for thin (<100Å) dielectric layers, XPS indicates further consumption of the substrate silicon. Thicker dielectric layers show a measurable decrease in net film thickness, also consistent with substrate consumption during post-deposition annealing. High resolution TEM/EDS analysis shows results consistent with XPS and CV analysis. While results to date do not allow unambiguous linkage between OH reduction and silicon surface oxidation, the results suggest the post-deposition OH absorption is a critical issue for interfacial stability of oxygen plasma deposited post-deposition reactivity in high-k dielectrics deposited on silicon. Approaches to control hydroxide incorporation and improve material stability will be presented and discussed.

**11:15 AM B5.11**

**CONTROL OF A METAL-ELECTRODE WORK-FUNCTION BY SOLID-STATE DIFFUSION OF NITROGEN**


Metal gate electrodes are increasingly attractive for future CMOS technologies as, they eliminate poly-Si gate depletion, reduce gate resistance, improve matching behaviour etc. It is generally accepted that the conventional plane CMOS will require gate electrodes with two-workfunctions in order to achieve suitable Vt for both n- and p-MOSFETs. The integration issues could be greatly eased if the electrode work-function at the dielectric interface could be selectively adapted for a single metal. This would allow using the the threshold voltages and might give the dual-workfunction gate electrodes without the need to remove one metal and redeposit a second. Several groups have reported the influence of nitrogen content at the metal-dielectric interface on the work-function of TiN metal gates. In these studies the nitrogen was selectively introduced by low energy ion implantation. In this report we demonstrated that a substantial concentration of nitrogen can be achieved at a low-temperature/SiO$_2$/interface by dielectric diffusion. Preliminary results show that a TiN/overlayer. Patterning of this overlayer prior to diffusion is straightforward and it is shown that only moderate diffusion...
temperatures (800°C/30min) result in measurable nitrogen concentrations at the metal dielectric interface (from Rutherford back-scattering measurements) and substantial changes in film thickness (~0.25V from capacitance-voltage measurements).

11:30 AM B5.12 ELECTRICAL AND STRUCTURAL PROPERTIES OF ULTRA-
THIN ZIRCONIA DIELECTRICS. Shirish Ramathan, Paul C. McIntyre, Stanford University, Dept of Materials Science and Eng., Stanford, CA; David A. Muller, Bell Laboratories, Lucent Technologies, Murray Hill, NJ.

Ultra-thin ZrO₂ films are currently being investigated as a potential candidate to replace SiO₂ in future complementary metal-oxide-semiconductor devices. In order to integrate them into future transistors, a fundamental understanding of their electrical properties is desired. This requires a thorough investigation of the microstructural interface chemistry of these films in conjunction with studies of their dielectric behavior, which will enable the development of processing methods to grow high-quality zirconia films. This paper deals with studies on thin films of zirconia grown by ultraviolet ozone oxidation of Zr metal films at room temperature. The effects of oxidation time, oxygen partial pressure, the underlayer and annealing conditions have been studied in detail. It was found that partially-oxidized films exhibited significant frequency dispersion in both the depletion and accumulation regions, while fully oxidized films showed negligible frequency dependence. A model based on the Maxwell – Wagner interfacial polarization mechanism has been used to interpret such phenomena and will be presented in detail. The electrical studies of the oxygen energy levels in the zirconia films have been complemented with detailed studies of the electronic structure using atomic resolution EELS in a STEM. It was found that the oxygen stoichiometry of the zirconia films has a significant effect on the O-K edge structure and this will be discussed using a molecular orbital description. Studies on CV hysteresis revealed that the flatband shift scaled with zirconia thickness. It was found that the leakage current could be modeled as direct tunneling at low voltages while Poole-Frenkel conduction dominated at higher voltages. The trap energy levels were calculated from modeling the IV data measured as a function of temperature and found to agree with values reported for AlD₃-grown SiO₂ / ZrO₂ stacks. It is suggested that the electrical traps in the zirconia films may be responsible for CV hysteresis. References: S. Ramathan et al., [a] Appl. Phys. Lett. (in press, 2001), [b] Jl. Appl. Phys. (submitted, 2001).

SESSION B6 GATE OXIDES AND INTERFACES
Chair: David O’Meara and Jon-Paul Maria

1:30 PM B6.1 SUBSURFACE REMOVAL OF SiO₂ TO CREATE A DIRECT SILICATE/SILICON INTERFACE. Andrew Carrier, Venkat Narayanan, S. Gahn, N. Bojarszuk, P. Bissess and M. Grilbeuy, IBM T.J. Watson Research Center, Yorktown Heights, NY.

In order to reduce parasitic capacitance in alternative gate dielectrics, it is quite common to remove surface SiO₂ prior to deposition of a metal oxide dielectric. A typical procedure involves aqueous HF etching to create an oxide free substrate. Using medium energy ion scattering we have investigated a novel approach, where interfacial oxide is removed after deposition by high temperature annealing in ultra-high vacuum. Surprisingly, there is a temperature window in which silicidation formation does not occur, but oxide containing species can freely migrate out through a silicide overlayer. An examination of the kinetics shows a similarity to SIO desorption from SiO₂/Si(001), suggesting that the same mechanism occurs for an SiO₂ layer embedded underneath a silicide. The results confirm stability predictions for silicide/dielectric, i.e. for the proper choice of materials, the metal-oxide bonds have greater stability than the silicon-oxide bonds.


The removal of native silicide using a beam of Sr atoms and the resulting Sr/Si(100) surface phases have been studied by LEED, AES and STM. The conditions for the formation of Sr/Si(100) template, namely the "2eV" phase, for epitaxial MBE SrTiO₃ growth have been identified. It has been found that the resulting Sr/Si surface phases depend upon the substrate temperature during the Sr flux desorption process, in agreement with earlier findings that the Sr/Si(100) phase is dependent on deposition starting temperature and Sr(100) surface [10]. Post annealing of a simple oxide obtained with the substrate at a lower temperature resulted in the slow adsorption of Sr atoms from the silicide surface and a progression of Sr phases with time. Similar results can also be obtained with the silicide substrate held at higher temperatures. Sr flux cleaning of a silicon wafer pretreated with HF has also been studied and similar Sr/Si phases can be obtained by adjusting the substrate temperatures or annealing conditions. [1] Z. Yu, J.L. Edwards, J.Z. Yu, M. Finder, C. Droopad, K.W. Eisenbeiser, J.A. Hallmark, and W.J. Ooms, J.R. Coon and V.S. Krishik. "Epitaxial perovskite thin films grown on silicon by MBE," J. Vac. Sci. Tech. 15 (2000) 1367. [2] Xiaoming Hu, Z. Yu, J.A. Curless, C. Droopad, K. Eisenbeiser, J.L. Edwards Jr., W.J. Ooms, D. Sarl, "Comparative study of Sr and Ba adsorption on Si(100)", Applied Surface Science, 181 (2001) 103.


We investigated the characteristics of the gadolinium oxide thin films controlled by interfacial layers. Ultrathin ZrO₂ and SiO₂ layers grown on Si (111) were used to modify the surface of the Si substrate. The characteristics of the films were assessed using various characterization techniques, such as reflection high energy electron diffraction (RHEED), x-ray diffraction (XRD), x-ray photoelectron spectroscopy (XPS). We found out that the structural transition from cubic Gd₂O₃ to monoclinic phase occurred in substrate temperature higher than 825°C. In particular, the transition was enhanced at the existence of ZrO₂ buffer layer. The crystallinity of the films was significantly affected by whether the buffer layer was inserted or not. The interfacial reaction between Gd and Si or Gd₂O₃, and Si critically affected the growth. The buffer layers successfully controlled the interfacial reaction and high quality epitaxial film were grown.

2:15 PM B6.4 PREPARATION AND OH ABSORPTION IN LANTHANUM SILICATES FORMED BY OXIDATION OF PVD La ON SILICON. T. Gougeon, M.J. Kelly, W.S. Burnside, J.M. Bennett, T.L. Schmidt, Advanced Research, Dept. of Chemical Engineering, NC State University, Raleigh, NC.

We have prepared La-based amorphous Ln₂O₃-Si alloys, i.e. "silicates", by sputter depositing La onto Si in a UHV sputter chamber, then oxidizing in N₂O at temperatures ranging from 400°C to 900°C. Because lanthana is reactive in air, target preparation and handling is critical to maintain high purity La deposition. When La is deposited on Si and oxidized, X-ray Photoelectron Spectroscopy indicates that the La reacts very rapidly with the silicon, leading to predominantly La₂O₃-Si bonding units in the film. The mechanisms are similar to those detailed previously for Y-PVD and oxidation, but the rate of reaction between La and Si is significantly faster than that of Y and Si. The relative concentration of La and Si in the resulting film depends on initial La layer thickness, substrate pretreatment, and oxidation time and temperature. By controlling these parameters, we have been able to achieve La₂Si₃ thin films with equivalent oxide thicknesses as small as ~15Å based on capacitance voltage measurements. CV show good behavior, with evidence for positive fixed charge, similar to most other reports of metal oxide high-k dielectrics. After deposition, infrared absorption of thicker silicate films showed evidence for OH absorption from the ambient. The rate of OH absorption depended strongly on the annealing temperature, suggesting a structural compaction of the dielectric layer upon annealing, similar to other well-known processes in SiO₂. The La-SiO₂ dielectric layers can help promote reactions between metal oxides and silicon, resulting in unwated lower-layer formation at the high-k/silicon interface. Details of the material preparation and stability to OH absorption will be discussed in terms of the understanding of the mechanism of interface reactions during CVD of high-k dielectrics on semiconductor surfaces.

3:00 PM B6.5 OXIDES, SILICIDES, AND SILICATES OF ZIRCONIUM AND HAFNIUM: DENSITY FUNCTIONAL THEORY STUDY. Maciej Gierakowski, John E. Jaffe, Pacific Northwest National Laboratory, Environmental Molecular Sciences Laboratory, Theory, Modeling & Simulations, Richland, WA; Chun-Li Liu, Matt Stoker, Antal Miklos, Advanced Process Development and External Research Laboratory, Motorola, Mesa, AZ.

It is known that the chemistries of hafnium and zirconium are more
center. Since these amido precursors do not contain oxygen, the oxygen activity of the process is controlled independently from the precursors. The process of deposition of silicon on silicon (Si/Si) or on a gate dielectric as a gate dielectric. We have recently found that there is an important difference between the Si/Si and Si:H/Si interfaces. The former was found to be unstable with respect to formation of silicides whereas the latter is stable. This surprising difference led us to study differences between oxides, silicides, and silicides of hafnium and zirconium. The calculations were performed in the framework of density functional theory with the Perdew-Wang 91 exchange correlation functionals. Ionic compounds were found to be more stable for hafnium than for zirconium with the heats of formation of oxides and silicides being larger by ca. 0.5 eV for hafnium. The higher ionization of hafnium compounds is also reflected by the band gaps that are larger by 0.5 oxides and 0.9 silicides eV for hafnium than for zirconium. The higher ionization of hafnium compounds is consistent with a smaller electronegativity of atomic hafnium (1.3) than zirconium (1.4). The incipient oxides and silicides are similar and with atomic ionization potentials 3.9 and 7.0 for silicon and Zr, respectively. Silicides were found to be more stable for zirconium than for hafnium with the heats of formation of disilicides being larger by ca. 0.3 eV for zirconium. Both monosilicides and disilicides were found to be metallic with no quantitatively differences in densities of states between hafnium and zirconium compounds.

3:15 PM B6.6
DOPANT DIFFUSION STUDIES FROM As, B, AND P-DOPED POLYSILICON THROUGH CVD DEPOSITED HF-H SILICATE THIN FILMS. M. Quevedo-Lopez, P. Puchniach, G. Pant, M. El-Bouzaani, M. Ken, B.E. Grade, and R.M. Wallace, Department of Materials Science and Engineering, University of North Texas, Denton, TX. I. Colombo, M. Bevin, M. Douglass, A. Liščot, and M. Visokay, Si Technology Research, Texas Instruments Incorporated, Dallas, TX.

As the aggressively scaling of CMOS technology continues, high-κ gate dielectrics become one of the solutions in the provided increased capacitance with remarkable increase in gate leakage current. However, issues such as thermal stability[1] and dopant penetration[2] still require further study. Dopant penetration into the channel region from doped polysilicon is an increasingly important issue in MOSFETs. Under high temperature processing, such as dopant activation annealing, dopants can diffuse out of the doped polysilicon gate, through the thin gate dielectrics and into the Si substrate, causing a shift in the threshold and flat-band voltages of the device.

Diffusion studies of boron, arsenic, and phosphorus from doped polysilicon through the high-κ gate dielectric thin film (4-5 nm) candidate HfSiOₓ into Si will be presented. The Polysilicon/ HfSiOₓ/Si stack was subjected either to rapid thermal processing (RTP) or standard furnace annealing in an N₂ atmosphere. After annealing, the polysilicon and dielectric films were chemically etched prior to depth profiling using Secondary Ion Mass Spectrometry (SIMS) methods. As-deposited and annealed films were studied using X-ray Photoelectron Spectroscopy (XPS) and High Resolution Transmission Electron Microscopy (HRTEM) to determine structural changes or growth of interface layers. Dopant penetration after aggressive annealing was observed. Polysilicon removal and dielectric film removal issues after annealing will also be discussed.


This work supported by Texas Advanced Technology Program, the Semiconductor Research Corporation, and DARPA.

B7.1
STUDY OF SUB-NANOMETER GATE OXIDE IN FIELD EFFECT TRANSISTORS BY ATOMIC SCALE SCANNING TRANSMISSION ELECTRON MICROSCOPY. Tetsu Tagurin, Nigel D. Browning, University of Illinois at Chicago, Dept of Physics, Chicago, IL; Zhiyong Ma, Kevin Johnson, Intel Corporation, Hillsboro, OR.

Gate oxide is arguably the most critical part of contemporary nanoscale MOSFETs. Continuous improvement in device performance requires further scaling of gate oxide to achieve desired drive current. Oxide thickness has reached a level where the properties of high-k gate dielectrics are determined by the interfacial oxide, which is very different from the bulk oxide in terms of structural, electrical and optical properties. Thus a good understanding of gate oxide both structurally and electronically is of paramount importance for its application in future transistors. In this work we present a comprehensive study of subnanometer gate oxide in MOSFETs using atomic resolution Z-contrast imaging coupled with spatially resolved electron energy loss spectroscopy (EELS) in the scanning transmission electron microscope (STEM). Interface composition, thickness, and strain are characterized and correlated to its electrical properties and electronic structure. Here we report an existence of local interface strain between Si and SiO₂, and a quantitative characterization in terms of the maximum atomic displacement and the spatial extent. EELS analysis of Si 2p, L edge, and oxygen K edges across the ultrathin gate oxide provided information on the spatial extent of the oxides, dielectric properties of the
oxide and leakage current. A presence of pronounced but not
overlapping interfacial states were identified.

B7.2 DEVICE SCALING EFFECTS ON SUBSTRATE ENHANCED DEGRADATION IN MOS TRANSISTORS. Nair R., Mahapatra, S., & Mahapatra, S., Department of Electronics Engineering, Indian Institute of Technology Bombay, INDIA; Bell Laboratories, Lucent Technologies, NJ.

Recently enhancement of electron injection with reverse substrate bias (V_Sn) is observed due to impact ionization feedback mechanism, which is helpful for realizing fast and low power non-volatile memories. The reduction of I_EOT and T_90 of the transistor affects the internal electrical characteristics and carrier heating and injection process. The damage creation and the resulting device degradation thus become a strong function of device dimensions and therefore merit attention. Till date, no work has been done to study the effect of substrate bias on I_EOT (dependence on V_Sn). In this paper, we have studied the reliability issues of n-channel MOS transistors having different I_EOT and T_90 for different reverse V_Sn under identical bias and gate current (programming time for flash memories) conditions. The I_EOT and T_90 dependence studies are performed on devices having T_90 of 10m. The T_90 dependence studies are performed on devices having L_EOT of 0.2 μm. With increase in negative V_Sn, impact ionization feedback occurs, which increases carrier heating thereby gate current. Also, for higher negative V_Sn, the injected carriers are not confined to a narrow zone but spread out. We observe an increase in ΔV_T and ΔG for 1.16 and 1.72 when the device is stressed at V_Sn = -2V. The higher ΔG can be attributed to an increase in electron injection. With a decrease in I_EOT from 0.4 to 0.1 μm, ΔV_T, I_EOT, and ΔG are increased by a factor of 4.3, 231 and 2.88 respectively for V_Sn = 0 and by a factor of 3.7, 3.96 and 2.88 respectively for V_Sn = -1V. This is because if I_EOT of a MOSFET is reduced at a constant bias, the E_T increases whereas the E_F decreases due to higher S/C ratios. Since the injection and thermal degradation at negative V_Sn has a very strong dependence on E_F, we observe higher I_EOT and degradation for V_Sn = -2V. The increased I_EOT can be attributed to large number of secondary holes in the substrate and the higher degradation is due to higher gate injection and larger spread of carriers with a factor of two equal. We have also studied the degradation for different I_EOT and T_90 under constant gate injection and generation efficiency.

B7.3 USE OF SMALL GATE VOLTAGE PULSES FOR THE EXTRACTION OF THE INTERFACE TRAPS DENSITIES IN MOS STRUCTURES USING THE CHARGE PUMPING TECHNIQUE. E. Lin, E. Missy, and D. Baur. Laboratoire de Physique des Composants Semicconducteurs, UMR CNRS 5231, ENSERG, Grenoble, FRANCE.

In MOS structures with ultrathin oxides, the determination of the interface trap densities, D_It, with conventional interface trap characterization techniques is difficult due to the small gate voltage excursions allowed before Fowler-Nordheim injection or direct tunneling of the minority carrier. Using charge pumping, the most widely used technique for interface trap characterization, large gate voltage pulses imply such currents. The use of high frequencies to increase the CP current magnitude has been proposed [1]. In this paper, small gate pulses are proposed for the extraction of D_It. They strongly limit the leakage currents and extend the experimental conditions which can be used (the frequency can also be used to increase CP signal magnitude). For this, and as the theoretical derivations that allow the extraction of D_It require large gate pulses (pulses larger than (V(temp) > V(temp) + V(temp)), where V(temp) and V(temp) are the device threshold and flat band voltage) [2], the extraction D_It is extended to the case of small gate pulses, i.e., pulses smaller than (V(temp) < V(temp)). To that end, the theoretical derivations are reconsidered in order to account for both emission and capture in various situations. This provides equations that 1) more accurately describe the CP current when large gate pulses are used, 2) generalize the description of the CP current to a wide range, and 3) allow D_It to be calculated whatever the gate pulse is. These results are applied for characterizing MOS device with thick and ultrathin oxides. This work is also relevant to this end, and with respect to the above results, the large distribution of trap time constants evidenced at the interface cannot be overlooked when using small gate pulses and only a fraction of the interface traps are expected to be probed. The interface trap densities measured, effectively decrease when reducing the pulse height, especially for higher values than (V(temp) > V(temp)), but with pulse heights as small as (V(temp) > V(temp)/2), that is 0.6 V, the D_It values obtained within a factor of two equal, are measured conventionally. This is a fully acceptable result if one accounts for all the uncertainties on the determination of D_It (for instance, the differences between the values obtained using different characterization techniques). [1] P. Masson, J. L. Austrasz, and J. Beini, IEEE Electron Device Lett. 12, 92 (1991). [2] Van de Veire et al., IEEE Trans. Electron Devices 38, 1820 (1991). [3] D. Bauza and Y. Mhiri, IEEE Trans. Electron Devices 44, 2262 (1997).

B7.4 THE SOLUTION OF GOI IMPROVEMENT ON HIGH VOLTAGE DEVICE. S-Y. Kao, H. M. Gung, Y. P. Tsay, Y. J. You, Taiwan Semiconductor Manufacturing Co. Ltd., Hsin-Chu, Taiwan, ROC.

The thicker thickness of gate oxide is required to make sure the product can work on high voltage condition. However, the traditional dry oxidation method doesn't meet the testing requirement. The aim of this paper is to provide a quality method to produce a high quality gate oxide for mass production. There are three process factors were studied for this gate oxide quality improvement on dual voltage product. The first gate oxide is to form a thick oxide and make a thin oxide on the brief summary (dominate in the HV product) as list: 1) Oxidation methodology. The low temperature (850°C) and three steps (dry-wet-dry) get the better VBD performance than 920°C/860°C or two steps (dry-wet) conditions. The mechanism is annealing, dewelling bond and crystal original pins effect. 2) Stack gate formation methodology. The prior gate oxide forming method changed from oxidation to LPCVD is considered. HTO replaces dry-wet-dry oxidation will get better VBD result. It is believed COP effect. But, TEOS didn't have the similar result since carbon element impact. 3) Wafer material source. Above two experiments were done on CZ polishe wafer. AR named wafer performance is slightly better than H2 annealed wafers. But both annealed wafer performances was better than wafer according. The studying above, COP effect plays the major determinant of the gate oxide quality on high voltage devices. Oxidation method, stack gate formation and wafer material are proved out the advantages and audience. This paper provides some solutions on gate oxide quality improvement for mass production.

B7.5 DEGRADATION IN A POLYBENZENIUM GATE MOS STRUCTURE CAUSED BY N + ION IMPLANTATION FOR THE WORK FUNCTION CONTROL. Tatsuki Amada, Nobushide Menda, Kentaro Shibahara, Research Center for Nanodevices and Systems, Hiroshima Univ., Hiroshima, JAPAN.

Work function control technique of the Mo gate by annealing or N + ion implantation has been reported by Banade et al.[1] with the aim of dual work function CMOS fabrication with a single metal material. We also fabricated the Mo gate MOS diodes with 5-20 nm SO2 gate oxides and found that the gate leakage current were increased as N + implantation dose and implantation energy were increased. Though work function shift was observed in CV characteristics, the hump due to the high-density interface states was found for high-dose specimens. Nitrogen SIMS depth profile showed that nitrogen was implanted much deeper than calculated depth obtained by SRIM simulator. Charging of the N + ions implanted nearly vertically (90°) into columnar crystal structure Mo film is the considerable origin of this deep profile. To reduce N + ions that pass though the gate oxide, we have compared angled implantation with the nearly vertical one. In the case of tilt angle of 30°, the gate leakage current was reduced compared with the 7° case. Since the decrease in projected range of N + ions for the 30° angled dose was only 15%, the deep profile and gate leakage increase seems to be attributed to the channeled effect. [1] P. Banade et al. J. Vac. Sci. Technol., Vol. 611. 2000. C3.2. 1 Acknowledgement: Part of this work was supported by STARC (Semiconductor Technology Academic Research Center).

B7.6 ELECTRICALLY INDUCED JUNCTION MOSFET (EJMOS) IS DIFFERENT FROM CONVENTIONAL CMOS DEVICES IN THAT THE SHALLOW SOURCE/DRAIN (S/D) JUNCTIONS ARE ELECTRICALLY INDUCED BY THE GATE VOLTAGE. In such a device that shallow extensions are realized in such a way that the device is self-aligned to the gate regions of opposite conductivity as is the case for S/D. In order to turn ON the device a voltage is applied at the gate of an EJMOS, such that the shallow doped regions below poly gate are inverted and serve as shallow S/D extensions. Consequently, the effective channel length in this condition is the distance between these shallow doped regions. On the contrary, at any gate voltage less than that required to invert these regions, no S/D extension is induced, and the effective channel length is equal to the physical separation between the deep S/D junctions. Our proposed structures also reduce the series resistance
effects when compared to the recently published devices based on a similar concept.

In this work, we compare 4nm gate length EJMOs and conventional devices using ISET-TCAD process and device simulations. In the EJMOs process, shallow extension regions under the gate are achieved by a compensation doping using a large angle tilt implant from both source/drain sides. As a result, the resulting MOSFET is symmetric in nature and can be fabricated using conventional CMOS processes. From extensive 2D process and device simulations, we observe over an order of magnitude increase in Ion/Ioff, improved sub-threshold characteristics, and better short-channel performance. Overall, our simulation results show, the EJMOs structure offers significant advantages over the conventional CMOS technologies in the sub-5nm regime.

**B7.7 APPLICATIONS OF AFM/SCM IN PROCESS CONTROL AND FAILURE ANALYSIS OF SEMICONDUCTOR DEVICES**


As the minimum feature size of semiconductor devices continues to shrink, analyses of the engineered structures and materials of semiconductor devices are increasingly critical in manufacturing and in the development of new generation devices. Furthermore, the performance of a modern device is significantly influenced by its dopant distribution in depth and laterally. Scanning capacitance microscopy (SCM) is one of the techniques that have been developed to reveal the dopant distribution in a non-destructive and non-invasive way. In this work, SCM was applied to both process control and failure analysis of semiconductor devices. Two types of semiconductor devices, Si based and GaAs based, were studied. In the process control area, two examples are presented. To investigate the lateral diffusion of dopants after a thermal annealing process is evaluated. A GaAs substrate is masked and patterned by a layer of SiN4, then Zn dopants are thermally diffused through a line-opening in the nitride layer into the substrate. By imaging the AFM image on top of the SCM image, the lateral diffusion of dopants is observed. The amount of n-type Zn dopants is found to be about 2.2 μm away from the edges of the exposed GaAs region. Another important application of AFM/SCM is in device failure analysis. In this work, a failed p-channel transistor is investigated by AFM/SCM. Two levels of dopant concentration are found in the corresponding source and drain regions by SCM.

Another approach to identify the cause of failures is directly compare a failed device with a properly functioning one. The use of AFM/SCM to study the same N-well structures in two devices, one good and the other failed, determined that the depth of the N-well for the failed device is about 0.4 μm shorter than in the good device.

**B7.8 SILICON SURFACE CHEMICAL TREATMENTS IN OXIDE/NDRITE DIELECTRIC STACK PROPERTIES**

David Jacques, Sebastien Petitdidier, Jorg L. Bogdani, Kathy Burgh, STMicroelectronics, Orles, FRANCE.

The ‘oxide’ terminated silicon surface may be chemically grown through many methods compatible with the ULSI technologies. These methods include equivalent water (SiO2)/nitride (Si3N4) stacks as a dielectric for memory cell. In the present work, we studied the dielectric oxide/nitride (ON) stack performance after different chemical treatments of the Si starting material through dielectric leakage current and change to breakdown measurements on the ON stack on single crystal Si surfaces. Three main steps are followed to obtain the complete ON stack: (i) the wet chemical surface treatment. Two main treatments are used to use a chemical before the thermal deposition: surface cleaning and surface passivation. The RCA cleaning, the ozonized water D113, and the HF last were independently used. (ii) the surface nitridation. The chemical oxides have been thermally nitridated transforming the layer oxide into some SiOxNy layer over which the SiN will be deposited. (iii) the nitride deposition. SiN film was deposited using DC/NBD plasma. The RCA cleaning uses ambient pressure of H2O in a batch vertical furnace. The RCA cleaning was not compatible with the surface treatment (Atomic Force Microscopy) and SiN incubation time for growth are comparable for all the studied oxides, SiOxNy, and in Poly-Si substrates. Three main steps are followed to obtain the complete ON stack: (i) the wet chemical surface treatment. Two main treatments are used to use a chemical before the thermal deposition: surface cleaning and surface passivation. The RCA cleaning, the ozonized water D113, and the HF last were independently used. (ii) the surface nitridation. The chemical oxides have been thermally nitridated transforming the layer oxide into some SiOxNy layer over which the SiN will be deposited. (iii) the nitride deposition. SiN film was deposited using DC/NBD plasma. The RCA cleaning uses ambient pressure of H2O in a batch vertical furnace. The RCA cleaning was not compatible with the surface treatment (Atomic Force Microscopy) and SiN incubation time for growth are comparable for all the studied oxides, SiOxNy, and in Poly-Si substrates. Three main steps are followed to obtain the complete ON stack: (i) the wet chemical surface treatment. Two main treatments are used to use a chemical before the thermal deposition: surface cleaning and surface passivation. The RCA cleaning, the ozonized water D113, and the HF last were independently used. (ii) the surface nitridation. The chemical oxides have been thermally nitridated transforming the layer oxide into some SiOxNy layer over which the SiN will be deposited. (iii) the nitride deposition. SiN film was deposited using DC/NBD plasma. The RCA cleaning uses ambient pressure of H2O in a batch vertical furnace. The RCA cleaning was not compatible with the surface treatment (Atomic Force Microscopy) and SiN incubation time for growth are comparable for all the studied oxides, SiOxNy, and in Poly-Si substrates.
bake step to successfully achieve integration in ILD layer. To prepare a dense and defect-free SiO2/Si film, the furnace loading temperature must be kept below 500°C and ramping rate was higher than 30°C/min, respectively. There were no crack and lifting problems due to sudden surface oxidation. Consequently, the properties of SiO2/Si ILD application were successfully optimized for the first time. The proposed SiO2/Si could be attractive in applications such as future DRA and LOGIC device because of its excellent gap-filling property and thermal oxide like film qualities.

B7.12 CHARACTERIZATION OF CVD LOW-k α-SiCO-H FILMS PREPARED FROM TRIMETHYLSILANE. Hae-Jeong Lee, Eric K. Lin, Barry J. Bauer, Wen-li Wu, National Institute of Standards and Technology, Polymers Division, Gaithersburg, MD; Byung Keun Hwang, William D. Gray, Electronics Industry & Advanced Materials Business, Dow Corning, USA.

In next generation devices, increases in propagation delay, cross-talk noise, and power dissipation of the interconnect structure become limiting factors for integrated circuits. To address these problems, new low dielectric constant (low-k) interlayer dielectric materials prepared by both spin-on and chemical vapor deposition (CVD) techniques are being developed to replace the traditional silicon dioxide. Low-k CVD films have attracted interest due to their physical rigidity, superior mechanical strength, and compatibility with current Si technology. One of the candidates for CVD low-k thin films is trimethylsilane (3 MS) based carbon doped silicon film (α-SiCO-H). This process is especially attractive because films with dielectric constants ranging from 2.5 to 3.5 can be used in a wide range of applications including plasma enhanced chemical vapor deposition (PECVD) equipment with uniform deposition characteristics in different device applications that are comparable to Si3N4 based SiO2. In this work, we characterize the structure of Dow Corning ZIMs based α-SiCO-H low-k thin films deposited by different processing conditions. Samples with dielectric constants ranging from 2.5 to 2.9 were prepared using single or dual frequency modes with different oxidants, O2 or N2/Ox. X-ray porosimetry is employed to characterize the porosity, average density, wall density and density profile of the thin films. These results are compared with high angle neutron scattering (SANS), high resolution x-ray reflectivity (XRR), and x-ray scattering. The influence of the process conditions on the chemical bonding structures and electrical properties were investigated using Fourier transform infrared (FTIR) spectroscopy and electrical measurements.

B7.15 CHALLENGES INETCHING OF OSG LOW-k MATERIALS FOR DUAL-DAMASCENE METALLIZATION Vladimir N. Bliznetsov, Mstislav Muksheev, Ryong Yew Yung, Woen Hwa Chua, Institute of Microelectronics, Dept Deep Submicron Integrated Circuits, SINGAPORE; Ng Beng Teck, Nanyang Technological University, Singapore, Dept Material Science, SINGAPORE.

Issues associated with OSG low-k dual damascene etching and in particular with resist stripping and integration in this process are the focus of this study. Usually during etch process three basic requirements should be met simultaneously. These are profile control, selectivity to barrier layer and minimal post-etch residues. The high hot plasma decomposition and residue generation in low-k silicon transitions makes it more difficult to achieve these as compared to conventional USG films. Moreover, if trench stop-layer is not used additional issues such as micro-trenching, across-wafer non-uniformity, micro-loading, and RIE leg may appear. This study was done mainly on Black DiamondTM of Applied Materials with some comparison to CorumTM of Novellus. TEL dipole-ring type magnetron etcher was used for etch development based on C4F8:N2Ar plasma. After preliminary screening experiments and the etch window DOE was performed which gave the dependence of OSG etch rates, selectivity to barrier layers, sidewall slope, RIE leg, micro-loading and non-uniformity versus process parameters. The dependence of factor was further optimized to realize sidewall profiles of 88.8°, minimized non-uniformity, RIE leg, and micro-loading. Selectivity obtained was enough to pursue etch processes using plasma etch BARC for etch. A combination of different types of BARC was used. The viscosity of BARC and fill depth in wafers were optimized for obtaining an optimal thickness for bottom protection and generating the least amount of polymer during etch. BARC opening time was fine-tuned accordingly. Different combinations of dry/wet clean recipes were evaluated for removal of post-etch residues without significant changes in OSG k-value. The sequence of optimized processes were successfully implemented for creating dual damascene structure complying with integration requirements for 0.13 design rules.


This study is part of Japanese national project to develop a PEC-free and energy-saving ILD (interlayer dielectric) process. In this project, we have also been investigating an ILD process that does not require a barrier film to prevent Cu diffusion. Thus, a clear understanding of the mechanism by which Cu diffuses into an ILD is essential. A simulated potential energy shows that when Cu penetrates SiO2, it must be converted to Cu+. One possible driving force is Schottky defects (crystal defects). The estimated current density was less than 0.3-2 A/cm² (observed value > 1 E-12). From this value, it is clear that diffusion through defects is not the dominant process. The current density of a Cu-electrode/TEOS/Si structure was measured with a probe in a vacuum chamber, which allowed the ambient conditions to be controlled. The expected current density was obtained when degazed TEOS formed by vacuum annealing was used and the LV characteristics were measured just after deposition of the Cu electrodes. The current density was found to be the same exposed to N2, though it did increase after exposure to dry air. It should be noted that degased TEOS film contains hardly any water or oxygen molecules. In contrast, conventional TEOS not subjected to annealing contains both, and samples made with this material exhibited the highest current density. These results demonstrate that Cu diffusion cannot be made to TEOS is exposed to oxygen or TEOS contains oxygen molecules. Atomic Cu has a magnetic moment, and oxygen molecules exhibit strong paramagnetism. The interaction between the magnetic moments of Cu and O2 lowers the potential. That means that the interface allows Cu to TEOS. Studies of simultaneously annealed 10-15°C were divided into two groups just after formation of the Cu electrode. One set was kept in a magnetic field for 2 days, and the other set was kept in air. The samples kept in a magnetic field generated lower current densities than the other. This demonstrates that one cause of Cu diffusion into an insulator is the presence of O2 in the annealing chamber. Acknowledgments: This work was performed under the management of ASET in a METI R&D program supported by NEDO.


We studied the effect of porogen content on the film properties of porous poly(silsesquioxane) material. Organic/inorganic aerogels prepared by using a thermally stable poly(ethylene oxide) as a template, and SOG (silicidioxane or organic) as a matrix material. The as-prepared poly(silsesquioxane) aerogel films were used as precursors to obtain porous poly(silsesquioxane) films. It is found that the dielectric constant depended on the porogen content and hardness of the thin film were affected by the porogen content. The thin films had dielectric constant of 2.2 with good mechanical strength.

B7.17 EVALUATION OF LOW-k POLYMER THIN FILM CONTAINING BORAZINE UNIT. Masaaki Iizuka, Tetsuya Fukuda, Arama Matsuo, Hiroshi Yamasawa, JAPAN, K. Kanzawa, Kyoto University, JAPAN, Yoko Uchimaru, Naoko Koda, Hiroshi Yamashita, AIST, Tsukuba, Ibaraki, JAPAN.

It was predicted that the polymers containing borazine unit were low-k materials, because a dielectric constant was simulated by both molecular polarizability and number of molecular in a unit volume through the use of the molecular orbital and band calculations. Two hybrid polymers containing borazine unit, such as borazine-carboline unit and borazine-siloxane unit, were evaluated on electrical characteristics. These polymers were synthesized by hydroxylfunctionalization of B,b'-tristriethylsilyln-N,N,N'-trimethyldiborazine with p-bis(dimethylamino)benzene or tetramethylcyclotetrasiloxane. Polymerization under diluted conditions gave a homogenous solution of borazine polymer. From measurement of dielectric constant on homogeneous films of the polymer were made on a silicon wafer by spin-casting method, followed by annealing at 380-500°C under argon gas. The dielectric constants of these thin films were evaluated to be 2.8-3.1, with a dependence on the film thickness and annealing conditions. The thermal resistance was good, because the temperature of weight decreasing to
MULTILEVEL INTERCONNECTS BY ION IMPLANTATION
Alic Nandi, U. Boy, G.S. Shelkdar, R. Geer, Katherine 
Dowdendael, Eric Addin, H. Bakhsh, New York at Albany, Dept of Physics, Albany, NY; A. Malikzaynez, A. Kumar, J. 
Furin, T.-M. Lu, Remsole Polytechnic Institute, Center for 
Integrated Electronics and Electronics Manufacturing, Troy, NY.

Thin films of xerogel and SILK (Low-k materials) were implanted with 
argon, nitrogen and helium etc. with 2E15 and 1E16 doses at energies 
varying from 50 to 150 keV at room temperature. In this work we 
discuss the improvement of ion implantation accuracy determination 
for dielectric materials by ion implantation. Ultrasonic Force Microscopy 
(UFM) and Nano indentation technique have been used for qualitative 
and quantitative measurements respectively. The hardness increased 
with increasing ion energy and dose (fluence), the hardness improvement varied with ion 
species. Dramatic improvement of hardness is seen for multi-dose 
implantation. Characterization of xerogel and SILK using ion beam 
technique will be presented.

B.7.20
STUDY OF POROUS SILICA BASED FILMS AS LOW K 
DIELECTRIC MATERIAL AND ITS INTERFACE WITH COPPER 
METALLIZATION. L. Fischer, M. Eisenberg, Dept. of Materials 
Engineering, Technion-Israel Institute of Technology, Haifa, ISRAEL; 
M. Nuss, and T. Weidman, Applied Materials, Santa Clara, CA.

The success of future gigascale integrated circuit (IC) chip technology 
depends critically upon the reduction of the interconnect RC delay 
time. This calls for the development of new low dielectric constant 
interconnect materials with low RC delay. A porous silica film 
composed of hydrogenated amorphous silicon nitride 
(HASiN) was deposited on a copper interconnect film and 
metallized using low-k films. "Wet" processes (evaporated 
and sputtering) in the k=2.2 region 

B.7.18
RELATIONSHIP BETWEEN ELECTRICAL PROPERTY AND 
STRUCTURE OF POROUS SiO FILM WITH LOW DIELECTRIC 
CONSTANT: Yoon-Hoe Kim and Hyung Joon Kim, Seoul National 
Univ., School of Materials Science and Engineering, Seoul, KOREA; 
Hae-Jeong Lee and Jin Yong Kim, Eric K. Lin, Barry J. Bauer and 
Wen-li Wu, NIST, Materials Science and Engineering Laboratory, 
Gaithersburg, MD; Young Lee, Jeung Engineering Ltd., R&D 
Division 3, Kyungui-Do, KOREA.

As ultralarge scale integrated circuits (ULSIs) are reduced in size to 
smaller submicron dimensions, there has been a strong demand for low 
dielectric constant inter-metal dielectric materials instead of 
SiO2 that is conventionally used to improve the performance of devices, 
such as signal propagation delay, cross talk, and power consumption. 
Recently, SiOxNy, which is hybrid between organic and inorganic 
materials, is very promising inter-metal dielectric, since it has higher 
thermal and mechanical stability than organic materials as well as 
low dielectric constant. Despite many researches, the reasons for 
increasing dielectric constant upon carbon incorporation remain 
under debate. Generally, it is accepted that the carbon incorporation in the 
SiO network leads to the porous structure and the decrease of film 
density results in the decrease of dielectric constant. In this 
investigation we focused on the electrical properties affected by 
porosity, using a porous SiO film with dielectric constant of 2.0. 
develop is a combination of high-resolution x-ray reflectivity (HRXR), 
and time-of-flight elastic recoil detection (TOF-ERD) to determine 
important structural information about the film. X-ray reflectivity 
measurements provide an accurate determination of the film 
thickness, electron density, and average film density. The dielectric 
constant is calculated from capacitance-voltage (CV) measurement 
at 1MHz. The (average) film density was reduced with increasing carbon 
content in the films, resulting in the decrease of dielectric constant of SiO film. Though 
the average film density was reduced by incorporating of carbon in film, the porosity was 
almost unchanged. On the other hand, the refractive index of the film 
materially reduced with increasing of carbon content. This result indicates 
that low dielectric constant of SiO film results from the decrease of 
matrix wall density by incorporating carbon in film.

B.7.19
MODIFICATION OF LOW K MATERIALS FOR ULSI 

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in the surface roughness increased with the bias voltage. A thick fluorocarbon surface layer was observed on the HOSP film after etching at 90 °C. The layer formation was enhanced at high bias voltages due to the redeposition of particles emitted from the bottom surface. When the HOSP film etched in CHF₃ plasma was subsequently exposed to O₂ plasma for ashing, the film surface became more reflective than before thermal oxidation, except for when the film was etched at 250 °C and at low bias voltages.

B7.23 POLARITY DEPENDENCE OF DEGRADATION IN ULTRA THIN OXIDE AND JVD NITRATE DIELECTRICS. Yasin Mehta, K.N. Marjubharsi, J. Vasi, V. Ramgopal Rao, Indian Inst of Tech-Bombay, Mumbai, INDIA.

We have studied Jet Vapor Deposited (JVD) silicon nitride MNSFETs and compared their degradation under identical field conditions with conventional MOSFETs. The devices used in this study are n-channel transistor. The gate oxide thickness of the gate dielectric is 3.3 nm for MOSFETs and 3.1 nm for nitride. The technology used for both devices is same except the dielectric deposition process. Silicon nitride is deposited using jet vapor deposition technique, whereas the oxide is thermally grown at 850°C. In this work, the evolution of the interface state density Nᵢₛ with stress for both nitrides and oxides is systematically investigated. Charge pumping method at 1 MHz is used to calculate Nᵢₛ. We have observed that in both oxide and nitride device, the degradation is higher under negative gate polarity. Also, in case of oxides, the degradation in Nᵢₛ is always lower compared to oxides for both positive and negative stressing. The results are analyzed in detail with the well-known hydrogen transport and trapped-hole recombination models. We conclude that trapped hole recombination is the more dominant mechanism of degradation. The devices under real operating conditions are subjected to bipolar or AC stress rather that DC conditions normally used for such degradation studies. This paper presents results using AC stress experiments on these ultra thin oxide and nitride MOS transistors. The frequency, peak-to-peak voltage and offset voltage of the applied stress signal are some of the parameters that are varied. The resulted characteristic results and analysis of the same will be presented.

B7.25 SYNTHESIS AND CHARACTERIZATION OF METHYLTHIETHYLXOSILANE BASED LOW PERMITTIVITY (LOWk) POLYMERIC DIELECTRICS. Z. Gu, Department of Chemical Engineering, R. Jayakumar, S. Sivoththanam, A. Nath, Department of Electrical and Computer Engineering, University of Waterloo, Waterloo, Ontario, CANADA.

Low-permittivity (lowk) polymeric dielectrics are potentially very attractive as interconnection materials in a wide range of semiconductor structures. In this work, a low-k polymeric material has been synthesized using methylthiethylxosilane as base material, and the material properties have been characterized. The material synthesis was carried out using an experimental set-up that involved refluxing, hydrolysis, nucleation, and polymerization steps. The final product is a high-flowing brownish liquid, that is spin-coatable to yield uniform films after coating and curing treatments. The film properties were measured using the standard methods. The microstructure of the material will be discussed. Test structures on silicon were fabricated to measure the dielectric constant (κ) of the material. The values of κ were found to be in the range of 1.9 - 2.7 (± 1 MHz) for annealing temperatures 250°C - 450°C. The annealed films as well as the initial material were found to be very stable. Fourier Transform InfraRed (FTIR) spectroscopy was used for the structural characterization. Prominent peaks, (Si-CH₃ stretch, Si-O stretch, Si-C, etc.) are observed in their dependence on film annealing conditions as well as material formation conditions will be discussed. In addition to the electrical and structural properties of the films, the paper will also report on integration-related issues such as planarization, film-stress, etc. (ref: Yamada et al., J. Electrochim. Soc. Vol. 147, p. 1477, 2000).

B7.24 EFFECT OF ION ACCELERATED PLASMA HYDROGENATION AND THERMAL TREATMENTS ON HYDROGEN SILESQUIOXANE (HSQ) LOWK DIELECTRIC FILMS. R. Jayakumar, L. Ren, and S. Sivoththanam, Electronic and Computer Engineering, University of Waterloo, Waterloo, Ontario, CANADA.

Hydrogen silexquioxane (HSQ) is a very promising polymeric dielectric with a low permittivity (k). However, higher curing temperatures and presence of oxygen tend to increase the k value. In this work, the effect of ion-accelerated hydrogen plasma exposure, film annealing temperature, and annealing ambient on the permittivity and structural properties of HSQ low-k dielectric films have been investigated. Experiments were performed on test structures fabricated using spin-on HSQ low-k films. The curing temperature was varied from 275°C to 575°C. The k values were found to be increasing with increasing curing temperature, and stayed below 3.2 for temperatures up to 410°C. Fourier transform infrared (FTIR) spectroscopy showed a reduction in intensity of Si-H peaks with increasing temperature. The presence of oxygen in the curing ambient was also found to have a strong influence on the dielectric constant as well as in the intensity of Si-H peaks with the reduction in Si-H peak intensities starting to occur at lower temperatures (~280°C). When the cured films were subjected to an ion accelerated hydrogen plasma treatment (250°C, 13.56 MHz RF plasma, 45 minutes), a very significant reduction in k was observed for all curing temperatures. (up to 45 percent reduction in k). The paper will report on the dependence of electrical, structural, and mechanical properties of the HSQ films on different thermal and plasma treatments.

SESSION B8: METALS AND INTERFACES

Chairs: Janice L. Veteran and Mehmet C. Ozturk
Thursday, March 4, 2010
8:00 AM - 11:45 AM
S90-12 (Marriott)

B8.1 SELF-ALIGNED PASSIVATED COPPER INTERCONNECTS: A NOVEL TECHNIQUE FOR MAKING INTERCONNECTIONS IN ULSI DEVICE APPLICATIONS. Amit Chugh, Ashutosh Tiwari, A. Keit, J. Nayar, NSF Center for Advanced Materials & Smart Structures, Department of Materials Science and Engineering, North Carolina State University, Raleigh, NC.

We have developed a technique to grow self-aligned epitaxial Cu/MgO
films on Si (100) using a Pulsed Laser Deposition Method. In this method we deposit a uniform film of Cu/Mg (5:7) alloy over Si (100) at room temperature using a pulsed laser. As a result of HRTEM (with spatial resolution of 0.18 nm) and STEM-Z investigations we observed that when this film is annealed at 500°C in a controlled oxygen environment, in less than 30 minutes time, all the Mg segregates at the top and at the bottom surface of Cu. This is understood to be the consequence of lower surface energy of Mg. At 500°C Mg is quite sensitive to oxygen and a thin layer of MgO is immediately formed at the top surface, we also observed a thin layer of MgO at the Cu/TiN interface. Thickness of the upper MgO layer was found to be 15 nm while that of lower layer was 10 nm. Lower MgO layer acts as a diffusion barrier and inhibits the diffusion of Cu in the system. Upper MgO layer acts as a passivating layer and improves the quality of copper against oxidation. Electrical resistivity measurements (in the temperature range 123-300K) showed MgO/Cu/MgO/Ti/Si (100) sample to be highly conducting. We also observed that the resistivity of the system is insensitive to ambient oxygen environment. Self-assembled MgO (110) nanorods displays a means to grow several interesting materials over it. This technique can be used to integrate high temperature superconductors like YBa2Cu3O7-δ with silicon chip.

8:15 AM DS.2

RESISTIVITY OF AND ELECTROMIGRATION IN Cu-Alg

A.G. V. Bansore, K.S. Hsu, Chandrak, Department of Mechanical Engineering, Salt Lake City, UT.

Cu films have been implemented by some chip manufacturers recently for interconnects and other components replacing的传统interconnects. Upper MgO layer acts as a passivating layer and improves the quality of copper against oxidation. Electrical resistivity measurements (in the temperature range 123-300K) showed MgO/Cu/MgO/Ti/Si (100) sample to be highly conducting. We also observed that the resistivity of the system is insensitive to ambient oxygen environment. Self-assembled MgO (110) nanorods displays a means to grow several interesting materials over it. This technique can be used to integrate high temperature superconductors like YBa2Cu3O7-δ with silicon chip.

9:00 AM DS.5

GROWTH MECHANISMS AND PROPERTIES OF TANTALUM PHASE FILMS GROWN BY PLASMA ENHANCED ATOMIC LAYER DEPOSITION. H. Kim, C. Calabro Jr., C. Lavoie, S.M. Rossnagle, IBM Thomas J. Watson Research Center, Yorktown Heights, NY.

Ta films were grown by plasma-enhanced atomic layer deposition (PE-ALD) at temperatures from 20°C up to 500°C using TaCl₅ as source gas and RF plasma-activated atomic H as the reducing agent. Post-deposition chemical analyses showed that the main impurity is oxygen, incorporated during the air exposure prior to analysis. The films had typically low Cr concentration below 1 at.% X-ray diffraction shows broad diffraction features, indicating that the ADL Ta films are composed of nanocrystallites. The typical resistivity of ADL Ta films was 150-180 μΩ-cm, which corresponds to that of Ta3Ni, for a wide range of growth parameters. The maximum value of thickness per cycle was below 0.1 ML, due to the stochastic nature of TaCl₅ film formation. Post-deposition analysis was performed using X-ray diffraction, elastic light scattering, and resistance analysis. The results were compared with Ta thin films deposited by sputtering with comparable thicknesses.

9:15 AM DS.6

THE EFFECTS OF NITROGEN ON ELECTRICAL AND STRUCTURAL PROPERTIES OF TaS₂/N₂ SiO₂ DEPOSITS. Y. Song, S. Shen, J. Hoon Lee, and Y. Miura, Department of Electrical Engineering, North Carolina State University, Raleigh, NC.

As gate oxide thickness decreases, the capacitance associated with the depletion layer at the poly-Si/gate dielectric interface becomes significant, making it necessary to consider alternative gate electrodes. The research many challenges to solving these problems, one of which is the need to have compatible work functions, process compatibility and thermal/chemical interface stability with underlying dielectric. Most met at low gate electrodes studied to date suffer from high temperature instability, resulting in low gate dielectric breakdown voltage. This work has shown that TaS₂/N₂ (Si > Ta) films on SiO₂ have excellent thermal stability at high temperatures and the
work function of Ta$_2$N$_7$N$_5$ is compatible with NMOS devices. In this work, Ta$_2$N$_7$N$_5$ films were deposited on the Si$_2$O$_4$ gate oxides using reactive cosputtering of Ta and Si$_2$N$_4$. The Ta$_2$N$_7$N$_5$ films on Si$_2$O$_4$ substrates with different compositions have been studied to investigate the effects of the nitrogen in the Ta$_2$N$_7$N$_5$ gate on the electrical and structural properties. The role of nitrogen in the Ta$_2$N$_7$N$_5$ gate was studied by comparing flatband voltage and the equivalent oxide thickness with nitrogen. The thermal stability of Ta$_2$N$_7$N$_5$ on Si$_2$O$_4$ stacks was studied at annealing temperatures of 700°C and 900°C in Ar. XPS and TEM analysis were performed to get the bonding information in the films and interfacial reaction between Ta$_2$N$_7$N$_5$ film and Si$_2$O$_4$.

10:00 AM B8.7 NON-DESTRUCTIVE MONITORING OF COBALT SILICIDE USING PICOSECOND ULTRASONIC MEASUREMENTS.

Amit Nangia, Texas Instruments Inc, DMOS, Dallas, TX, Chi-Kong Cheng, University of California, Berkeley, Dept of Chemical Engineering, Berkeley, CA, Niall McCasker, Rudolph Technologies, Flanders, NJ.

Silicides in CMOS technology have historically been monitored by measuring sheet resistance at different stages of the metal-silicon reaction. Sheet resistance being destructive in nature, requires that these measurements be made on non-product wafers. As contacts continue to shrink in size with more stringent processing requirements, the use of a non-destructive technique to gauge the silicidation process directly on product devices becomes increasingly important. Elimination of non-production material also has processing cost and time reduction benefits which can be significant at 300nm and smaller wafer fabrication. In this study, we investigated the use of picosecond ultrasonics to assess thickness and density of cobalt metal and silicide phases over the different stages of silicidation. An ultrafast optical "pump and probe" technique was used to excite the films and measure the maximum optical reflection as a function of time. Samples of different thickness were measured after cobalt stack deposition, CoSi formation, cap layer strip and Co$_9$Si$_3$ anneal. Models were developed to extract the thickness and density of the films at each step, on both single crystal silicon and poly-silicon substrates. A correlation was obtained between sheet resistance and thickness for the different stages of the cobalt silicide formation.

10:15 AM B8.8 SINGLE CRYSTAL TaN THIN FILMS ON TiN/Si HETERO-STRUCTURE.

Haigun Song, Ashutosh Tiwari, Alexander Kibbel, Xingzhong Zhang, Jagdish Narayan, Department of Materials Science and Engineering, North Carolina State University, Raleigh, NC.

We have successfully grown epitaxial cubic [H112011] tantalum nitride films on Si (100) and (111) substrate using a pulsed laser deposition technique. A thin layer of titanium nitride was used as a buffer medium. We characterized these films using X-ray diffraction, high resolution transmission electron microscopy and scanning transmission electron microscopy [Conostar X-ray diffraction and high-resolution transmission electron microscopy confirmed the single crystalline nature of these films with cube-on-cube epitaxy. The epitaxial relations follow TaN(111)|TiN(111)|Si(111) on Si(111) and TaN(111)|TiN(111)|Si(100) on Si(100). We observed sharp interface between TaN/TiN and TiN/Si without any indication of interfacial reaction. We checked the diffusivity barrier characteristics of these films by growing a thin layer of copper on the top and subsequently annealing the films at 1000°C. Even after annealing for 30 minutes we did not observe any diffusion of copper in the system. Rutherford backscattering experiments showed these films to be slightly nitrogen deficient [TaN$_{0.9}$]. High precision electrical resistivity measurements showed excellent metallic nature of these films. We also tried to deposit TaN directly on silicon, the films were found to be polycrystalline. In our method, TiN plays a key role in facilitating the epitaxial growth of TaN. This method exploits the concept of lattice matching to grow epitaxial TaN in TiN/Si system. The growth of TaN and epitaxial growth of TaN and TiN on Si(111) were observed. This work provides a promising way to grow high quality TaN diffusion barrier on silicon for copper interconnection.

10:30 AM B8.9 MICROSTRUCTURAL EVOLUTION OF THE INITIAL PHASE FORMATION OF COBALT SILICIDE WITH AN ULTRA-TIN THIN TITANIUM UNDERLAYER.

Kevin D. Johnson, Julie Tsai, Zhiyong Ma, Intel Corporation Hilsboro, OR, Kim Sin Sim, Intel Corporation, Penang, MALAYSIA.

Co silicide has been a predominant candidate for deep sub-micron process technology owing to its low resistivity and scalability. This work investigates ultra-thin Ti underlayer assisted median of the phase formation for cobalt silicide and addresses the role of Ti in the various stages of the phase evolution. The Ti underlayer is spatter deposited as a thin 100Å layer prior to Co deposition. A rapid thermal anneal (400°C-550°C) is then implemented to initiate silicidation. Although the reaction sequence for Co silicide is Co > Co$_2$Si > Co$_3$Si, the interdiffusion underlayer after allowing Co$_2$Si to form directly below the Ti underlayer and a more Co-rich phase to form above the Ti underlayer. The thickness of the Ti underlayer also alters the initial phase formation and the reaction path for Co silicidation affecting the reaction kinetics. There are practical advantages for Ti underlayer that mitigate some of the difficulties of silicide processing.

11:00 AM B8.11 ON THE MORPHOLOGY CHANGES OF Ni AND Ni(Pt)-SiCLES.

Pooi See Lee, Dept of Materials Science, National University of Singapore, SINGAPORE, Dominique Mangelinck, LAM-P-CNRS, FRANCE, Jun Ding, Dept of Materials Science, Dang Zhi Chi, Institute of Materials Research and Engineering, SINGAPORE, Thomas Osipov, Dept of Physics, National University of Singapore, SINGAPORE, Alex See, Chartered Semiconductor Manufacturing, SINGAPORE.

NiSi is a promising silicide material due to one step low temperature formation, low resistivity and low Si consumption. To enhance the phase stability of NiSi, addition of Pt has been shown to form Ni(Pt)Si up to 900°C [1]. The application of Ni(Pt)Si onto devices at silicidation temperature above 700°C has also been demonstrated [2]. The issues of agglomeration and layer inversion has remained critical since conductivity of thin silicide films is sensitive to the degradation of the film morphology. The purpose of this work is to study the morphology degradation that includes agglomeration and layer inversion of NiSi and Ni(Pt)Si. Rutherford Backscattering Spectroscopy (RBS), Scanning Electron Microscopy (SEM), Cross Transmission Electron Microscopy (XTEM) and electron diffraction analysis were employed. Layer inversion leads to the reversal in position of polycrystalline silicon (polys-Si) and silicon. It was found that the addition of Pt has led to an improvement in the agglomeration behavior of NiSi but has little influence on the layer inversion on the undoped polysilicon. Suggestion of layer inversion was attained by silicidation on Phosphorus doped polysilicon or with the use of thin Ni(Pt) (~10 nm). The agglomeration behavior and layer inversion are discussed in terms of the controlling factors of grain boundary energy and interface energies. [1] D. M. Duy, J. S. Pan and S. Laih, Appl. Phys. Lett. 75 (12), 1736 (1999). [2] P. S. Lee, K. L. Pey, D. Mangelinck, J. Ding, D. Z. Chi, L. Chan, Electron Dev. Lett., to be published in Dec, 2001.

11:15 AM B8.12 AC-INDUCED DAMAGE IN Cu INTERCONNECTS.

R. Weinig, S. Orso, C. Volkert, R.R. Keller, and E. Arzt, Max Planck Institute for Metal Research, Stuttgart, GERMANY.

We have recently observed the formation of severe damage in Cu interconnects during in-situ testing in an SEM with 100 Hz alternating current at 60 Hz. The change in temperature and change appearance surface wrinkles within single grains, which grow in amplitude and extent,
and eventually lead to electrical failure of the lines. The damage bears no resemblance to typical electromigration damage generated by DC testing conditions and is probably caused by thermal fatigue. Because of Joule heating in the interconnects, the alternating currents used in these studies (rms 10-15 mA/cm²) generate temperature swings as large as 150°C which cause thermal mechanical stress cycles and the creation of fatigue damage within as few as 10¹⁰ cycles. The formation of the fatigue damage is not hindered by the presence of soft encapsulating films, such as a polymer-based low k dielectric. Since the temperature swings generated by the tests are not much larger than those expected in devices during normal operation, thermal mechanical fatigue may become a serious reliability threat in Cu-based devices with soft underlay dielectric. We will present results on the effect of the current density (or temperature amplitude), grain orientation and encapsulating layers on the formation of fatigue damage and the time to cause an electrical failure. In addition, the damage accumulation process, including the formation of cracks, will be described.


Presently, most modeling and experimental analyses for circuit-level interconnect reliability focus on straight stud-to-stud test lines. However, in reality, multiple segments of straight lines are connected in junctions in the interconnect circuits. An interconnect tree has been defined as a unit of continuously connected high-conductivity metal lying within one layer of metallization. Standard reliability assessment methods are based on analysis of individual segments, using the results from straight junction-free lines rather than trees. This method is generally inaccurate as material within an interconnect tree can diffuse freely among connected segments, and the stress evolution in different segments of a tree is coupled. Tree-based experiments and assessment methodologies have been developed for Al-based interconnects. However, experiments have not been previously carried out on Cu-based interconnect trees. Electromigration experiments have been carried out on simple Cu-dual-damascene interconnect tree structures consisting of straight stud-to-stud lines with an extra via in the middle of the line. As with Al-based interconnects, the reliability of a segment in this tree strongly depends on the stress conditions of the connected segment. Beyond this, there are important differences in the results obtained under similar test conditions for Al-based and Cu-based interconnect trees. These differences are thought to be associated with variations in the architectural schemes of the two metallization systems. An example of a complex interconnect tree overlay in Cu technology, and the possibility of liner rupture at stressed vias, lead to important differences in tree reliability in Cu compared to Al. Although liner rupture may increase the reliability of the stressed segments, it also lead to a decrease in the overall reliability of the circuit. This work demonstrates that while segments are not the fundamental reliability unit for circuit-level reliability assessments for Al or Cu via, rather than trees, might be the appropriate fundamental units for assessment of Cu reliability.

11:45 AM B8.14 COMPARISON OF TiN THIN FILMS DEPOSITED BY METAL ORGANIC ATOMIC LAYER DEPOSITION (MOALD) USING TDMAT AND TDEAT: Ju Youn Kim, Sung Won Seo, Jin Yong Park, Youngdo Kim, Young Do Kim and Youngtaek Jeon, Division of Materials Science and Engineering, Hanyang University, Seoul, KOREA.

Among the transition metal nitrides, titanium nitride (TiN) has been widely used as a diffusion barrier in ultra scale integrated devices. Barrier layers were deposited predominantly by the physical vapor deposition (PVD) and chemical vapor deposition (CVD) techniques, but they suffer from the poor step coverage and have limited their applicability in the new generation of integrated circuits with very high interconnections in ultra thin film transistor devices. Atomic layer deposition (ALD) is a new deposition technique to improve the combined problems of PVD and CVD methods. Many researches have been carried out to grow TiN, mainly using halide precursors, by ALD method. However, there is no uniform method using halide precursors in some problems such as very low growth rate and high chlorine content which makes ALD difficult to be applied in an industrial device process. Therefore, as recent, many experiments have been performed to alternate halide precursors with metal organic precursors. In this study, TiN films grown by metal organic ALD (MOALD) method using tetramethyl-diethylamino-titanium (TDMAT) and tert-butyl-amino-titanium (TDEAT) at T precursor and NH₃ as reactant gas were investigated. The physical, chemical and electrical properties of TiN films grown by MOALD using TDMAT and TDEAT precursors have been systematically analyzed and compared.
resulting across-wafer thermal gradient offsets the effects of preferential edge deposition on within-wafer thickness uniformity. Accurate estimation of thermal gradient and silicon nitride deposition rate dependence on temperature and process chemistry allow for precise calculation of temperature setpoints for best uniformity. Both of these requirements are met using Adaptive Real-Time Tempcontrol and associated single-chamber nitride deposition models. The ability of current vertical LPCVD batch reactors to precisely control process temperatures, even during ramping, insures repeatable results. Typically, additional test runs are required to qualify silicon nitride deposition processes and parameters. These times increase when Adaptive Real-Time Tempcontrol is utilized. However, Adaptive Real-Time Tempcontrol is intended for critical processes where yield demands thinner film thickness specifications, where batch sizes must be reduced to achieve acceptable thickness uniformity. The use of Adaptive Real-Time Tempcontrol allows acceptable film thickness uniformity to be achieved over the entire furnace load area and ultimately increases process throughput.

2:00 PM B10.2
Si/SiO₂ INTERFACE ROUGHNESS STUDY BY SCANNING TUNNELING MICROSCOPY. Jie Xu, Logan Li, Thomas W. Sorsch*, William M. Marrsfield*, Gregory L. Timp, and Joseph W. Lyding, Beckman Institute, University of Illinois, Urbana, IL; “Agera System, Murray Hill, NJ.

There is a tremendous interest in determining the Si/SiO₂ interface roughness, which is believed to account for the degradation of the effective mobility of an inversion layer at high transverse field. Two parameters are usually used to characterize the interface roughness: the rms-roughness Δ, and the correlation length Λ. For the first time, we demonstrate that ultrahigh vacuum scanning tunneling microscopy (STM) can be used to directly examine the Si/SiO₂ interface and extract Δ and Λ from the STM topography. The rms-roughness Δ can be required from the Gaussian fit of the apparent height distribution, and the correlation length Λ is obtained from an exponential fit to the in-plane autocorrelation function. A smooth wafer and a rough wafer have been examined, both with a nonmonolayer oxide grown at 1000°C by standard industry procedure. We find Δ=0.11nm and Λ=2.60nm for the smooth wafer and Δ=0.26nm and Λ=2.41nm for the rough one. These results are consistent with those extracted from angular dark field scanning transmission electron microscopy data and X-ray diffraction data taken on similarly processed wafers.

2:15 PM B10.3
TRANSPORT PROPERTIES OF HETEROSTRUCTURE ZrSO₄ / Al₂O₃ / ZrSO₄ AND SiN₄ / Al₂O₃ / SiN₄ ON Si. Julie D. Capperman, Harry A. Atwater, California Institute of Technology, Watson Laboratory of Applied Physics, Pasadena, CA; L. Douglas Bell, Jet Propulsion Laboratory, Pasadena, CA; Brett W. Busch, Lilith Menchaca, Martin L. Green, Agera Systems, Murray Hill, NJ.

Among the main performance limitations of floating gate nonvolatile memory devices, such as flash memories and nanocrystal memories, are the long program time (~1 ms) and erase time (~1 ms) achievable via a Fowler-Nordheim tunneling mechanism. A novel technology, the floating gate through a homogeneous tunnel barrier. An interesting alternative to homogeneous dielectric tunnel barriers is a silicon compatible layered tunnel barrier, which enables a large drop in the barrier height with applied voltage. We have fabricated dielectric constant and band offsets with respect to silicon in order to help identify possible materials from which to construct these layered barriers. Based on this survey, we have determined that some of the most promising materials heterostructures are SiN₄ / Al₂O₃ / SiN₄ and ZrSO₄ / Al₂O₃ / ZrSO₄. We have fabricated the metal-insulator-semiconductor layered barrier structure of SiN₄ / Al₂O₃ / SiN₄ on silicon. The SiN₄ was made by low-pressure chemical vapor deposition at 200°C. The Al₂O₃ and SiN₄ were made by atomic layer deposition using sequential exposures of trimethylaluminum and H₂O at 500°C. High-temperature annealing was found to greatly reduce the leakage currents and thus enhance the barrier lowering. We have also fabricated single-layer barriers of Al₂O₃ and double barriers of SiN₄ / Al₂O₃ / SiN₄. A comparison of the current-voltage (IV) and capacitance-voltage (CV) characteristics of these structures will be discussed. The IV measurements were performed on dielectrics that were deposited on degenerately doped n⁺ and p⁺ silicon in order to minimize band-bending. To assess the electrical performance of our layered tunnel barriers, we performed simulations to the ionization temperature of the electric field as a function of the leakage current. Tunneling probability simulations for layered tunnel barriers are performed using an effective-mass model. With this theory we are able to predict the LV curves for our tunnel barriers and can determine if barrier lowering is achieved. In addition, the characterization, values of the band offsets for Al₂O₃ and ZrSO₄ relative to n-type silicon will be presented. These values are found by ballistic electron emission microscopy (BEEM) and by photocurrent measurements that utilize a variable energy tunable light source.

3:00 PM B10.4
DIFFUSION CHARACTERISTICS OF COPPER IN TiN THIN FILMS. Akshay Goga, Alex V. Kvit, Gerd Duscher and J. Noranjan, NSF Center for Advanced Materials and Smart Structures, Department of Materials Science and Engineering, NCSU, Raleigh, NC.

We have investigated the diffusion characteristics of copper in an amorphous, polycrystalline, and single crystal TiN thin films, which is used as a diffusion barrier for sub-quarter-micron microelectronics. These films were synthesized on Si <100> substrate by first sputtering amorphous TiN and then sputtering copper targets using Pulse Laser Deposition. The three different crystalline structures of TiN were achieved by growing the films at different substrate temperatures, where higher temperatures (>700°C) evolved to cubic phase. Then a uniform thin layer of copper was deposited at 400°C for all the three deposition temperatures. Each sample is annealed at three different temperatures (400°C, 500°C and 600°C) to study the diffusion barrier characteristics of TiN. Study of diffusion profile and the copper concentration measurements were performed using Scanning Transmission Electron Microscopy-Z contrast (0.1μm resolution). Secondary Ion Mass Spectroscopy, Electron Energy Loss Spectroscopy and Rutherford Backscattering Spectroscopy techniques. These data were used to plot the measured concentration of copper with respect to the temperatures for the three crystal structures of TiN to calculate the diffusion coefficients and were compared to study the influence of microstructure of TiN thin film on the diffusion of copper after annealing.

3:15 PM B10.5
EFFECT OF AN APPLIED Ti LAYER ON CoSi₂ SALICIDE FORMATION. G.Z. Pan, E.W. Chang, S.A. Prusak and Y. Rohmir-Samii, University of California at Los Angeles, Dept of Electrical Engineering, Microelectronics Fabrication Laboratory, Los Angeles, CA.

Integration of self-aligned metal silicide into metal-oxide-semiconductor transistors and short diffusion lengths technology nodes is crucially difficult in order to achieve low sheet/contact resistance on ultra-thin junction source/drain as well as narrow gate. CoSi₂ silicide, in comparison with TiSi₂ and NiSi, is advantageous in terms of low sheet resistance, independent formation on narrow gate length, suitable formation temperature in control of ultra-thin junctions and thermal stability as well as readily epitaxial growth to improve contact resistance. We studied extensively the formation of ultra thin CoSi₂ silicide with/without an applied Ti mediating or capping layer by using rapid thermal and isochronal annealing in N₂ ambient. Four-point-probe sheet resistance measurements and electron microscopy were used to characterize the ultra thin silicide films as well as their formation kinetics. We found that the formation temperature of CoSi₂ and CoSi₃ as well as their existing duration are strongly influenced by the presence of an applied Ti mediating or capping layer. Under Ti capping, Co directly reacts with Si followed by a similar to a single layer Co silicidation. However, Ti capping favors the formation of CoSi₂ and the diffusion of Ti from the capping layer delays the phase transformation of CoSi₂ into CoSi₃ from 525°C to 675°C. An applied Ti mediating layer acting as diffusion barrier suggests that the supply of Co so that it limits the formation of high Co concentration silicide CoSi₃ but favors that of low Co concentration silicide CoSi₂ under a Co diffusion-controlled process. Electron microscopy studies indicate that CoSi₂ formed with an applied Ti mediating layer exhibits better epitaxial characteristics.

3:30 PM B10.6
FUNDAMENTAL BEAM STUDIES OF RADICAL ENHANCED ATOMIC LAYER DEPOSITION OF TITANIUM NITRIDE. Frank Greer, D. Fraser, J.W. Cobb, and David B. Graves, U.C. Berkeley, Dept of Chemical Engineering, Berkeley, CA.

Atomic Layer Deposition (ALD) has been proposed as one way to deposit highly conformal thin films for copper diffusion barriers due to the self-limiting, layer-by-layer growth that can be achieved with this technology. One problem with thermally activated ALD is that the deposition temperatures that are required to achieve reasonable growth rates and good quality films with low impurity concentrations can be relatively high. This may make the integration of these barriers with future low temperature, low leakage, low noise, low power CMOS processes challenging. One potential alternative to thermal ALD is to use more reactive species such as radicals to catalyze film deposition at lower substrate temperatures. In this work, TiN films are deposited using Radical Enhanced Atomic Layer Deposition (REAMD) using alternating pulses of TETCH and various combinations of hydrogen and/or nitrogen radicals with or without additional pulses.
of NiS. By directing independent beams of each of these species at a given surface (in this case, silicon coated on Quartz Crystal Microbalance), parameters of interest such as the sticking and reaction probabilities of these species have been measured as a function of surface temperature, and will be used to predict the conformality of films deposited using RE-ALD in features of arbitrary aspect ratio. Raman XPS analysis of the deposited films will be presented, paying particular attention to the low residual chlorine content that can be achieved with sufficient hydrogen radical exposure (>0.5%) at deposition temperatures as low as 100°C. In-situ Angle Electron Spectroscopy measurements will be presented from different stages during the deposition process. Various measurements of the film quality will also be presented including the films' resistivity and crystallinity.

3:45 PM B10.7 NICKEL, PLATINUM AND ZIRCONIUM GERMANOSILICIDE CONTACTS TO ULTRA-SHALLOW, P+ TN JUNCTIONS FORMED BY SELECTIVE SiGe TECHNOLOGY FOR CMOS TECHNOLOGY NODES BEYOND 70NM Jing Liu, Hongqing Mo, Mehmet C. Ozurk, North Carolina State University, Department of Electrical and Computer Engineering, Raleigh, NC.

One of the key challenges for future CMOS technology nodes beyond 100 nm is formation of ultrashallow junctions with a series resistance contribution limited to five percent of the channel resistance. The future junctions are expected to possess extremely low sheet, contact and spreading resistance values requiring fundamentally different methods for junction formation. Recently, this laboratory reported a new technology based on selective deposition of doped SiGe on silicon using plasma-enhanced chemical vapor deposition (PECVD) etched to the desired depth, which showed promise for technology nodes down to 30 nm. Of particular interest to this paper is the smaller bandgap of SiGe resulting in a smaller energy loss at the junction, which is a key advantage over conventional SiGe technology. In this paper, we present our recent results on Pt and Ni germanosilicide contacts to p+ SiGe. We show that both contacts can provide a resistivity near 10^-6 ohm-cm needed for technology nodes beyond 70 nm. However, the stability of the materials were found to be limited to ~550°C for Ni and ~800°C for Pt. This was attributed to Ge desorption from germanosilicide to segregate at the grain boundaries and/or at the contact/nitride interface. Trapping was proposed as an alternative germanosilicide for better stability. Another possibility, considered for the first time here is the use of a thin Zr layer as an intermediate layer between Pt or Ni and the junction. The films were characterized by four-point-probe, XRD, SIMS and AFM. The results indicated that both Zr alone or Zr with Pt or Ni are viable contact materials to p+ SiGe. Using Zr alone results in a ternary germanosilicide with good stability at least up to 900°C. Using Zr as an intermediate layer improves the stability by reducing the Ge loss from the germanosilicide.

4:00 PM B10.8 MICROSTRUCTURE AND ELECTRICAL PROPERTIES OF Cu/TiN INTERFACE FOR CMOS COPPER INTERCONNECT Qi Wang, Qingguo Tao, Tong Wang and Chunmei Chen, Tsinghua Nonferrous Metals Shenzhen Company, Shenzhen, PRC; Xiaomin Duan, MIT, Dept. of Materials Science & Eng., Cambridge, MA.

The interface between Cu and barrier layer is important key to the CMOS copper interconnection. An ideal interface of Cu/Barrier metal has to ensure low alloying with a uniform homogeneous copper barrier layer in order to suppress the interfacial electromigration of copper. In this study, a TiN layer with a thickness of 800 Å was deposited onto a typical dielectric SiOx layer using conventional Physical Vapor Deposition technique. On the barrier layer, a 200 Å layer of copper was then, sputtered at room temperature. Afterwards, low temperature annealing for Cu/barrier metal interface was carried out at 350 to 550°C for 30 to 60 minutes in order to form a uniform interface and to reduce residual stress in the layers formed during deposition. We have systematically studied the wetting and agglomeration of copper layer on TiN substrate and the texture of Cu film using Transmission Electron Microscopy (TEM) and X-ray Diffraction (XRD). It was found that the lattice interface and the copper agglomeration occurred during low temperature annealing, and the roughness of the Cu/TiN interface increased with the annealing temperature. It was also found that the (111) copper texture had increasing deposition and the degree of the texture decreased with increasing of annealing temperature and time. The result showed that the electromigration of copper in CMOS interconnects was related with the microstructure of Cu/barrier interface, in turn with the annealing procedures. The relationship between electromigration resistance and texture degree of copper is reported in this paper.

SESSION B11: POSTER SESSION

Thursday, April 4, 2002

B11.1 MICRO-RAMAN SPECTROSCOPIC STUDY OF NICKEL SILICIDE FILMS. S.K. Dhandu, D.Z. Chi, S. Tripathy*, A.S.W. Wong and S.J. Chua, Institute of Materials Research and Engineering, Singapore, SINGAPORE; *Centre for Optoelectronics, Singapore, SINGAPORE.

Micro-Raman technique was used to investigate vibrational properties of NiSi thin films formed on three different substrates: unimplanted (100) Si, 20keV BF2+ implanted (100) Si, and 2keV B+ implanted (100) Si. Nickel films, 30-nm thick, were deposited by sputtering technique and were subsequently rapid thermal annealed for 60 sec at 500-800°C for silicidation. Secondary ion mass spectroscopy was employed to study dopant redistribution during silicidation. Raman spectroscopy was performed in backscattering geometry corresponding to either z(1), z(2) or z(3) configuration. Raman spectroscopy was also performed on NiSi powder to identify various phonon modes associated with different silicon rules of group theory. Eight characteristic phonon peaks of NiSi phase were identified of which four at 214 cm^-1, 288 cm^-1, 360 cm^-1 and 395 cm^-1 were assigned to A1 phonon modes, the two at 195 cm^-1 and 335 cm^-1 to B2 phonon modes and the remaining two at 295 cm^-1 and 314 cm^-1 to either B2g or B3g phonon modes. It was found that Raman peaks of NiSi thin films formed on B2^+ implanted substrate were broader and shifted to lower frequency side compared to films formed on other substrates. The broadening of the Raman peaks in these films, which also exhibit much improved thermal stability, is attributed to small grains resulting probably from fluorine segregation to grain boundaries and interface. SIMS analysis showed that fluorine rapidly segregates to silicide interfaces on deposition, at a concentration of about 1.3 at %, it is proposed that in addition to grain boundary segregation, some structural modification in silicide film is induced by the presence of excess fluorine inside the grains, resulting in shift of phonon peak positions.

B11.2 Abstract Withdrawn

B11.3 OPTIMIZATION OF ULTRATHIN ALD TANTALUM NITRIDE FILMS FOR ZERO-THICKNESS LINER APPLICATIONS. Oscar van der Sloot, Yu Zhu, Frits Eisenbraun, Alain Kaldyeros, UAlbany Institute for Materials, Albany, NY.

A metallicorganic atomic layer deposition (ALD) tantalum nitride process has been demonstrated for very-thin film applications in advanced copper metallization schemes employing a commercial ALD reactor. This process employs a liquid tantalum source (tert-butyltrihydrido trichloro tantalum - TBHTDT) and ammonia as the reactants. Key functionality data addressing the self-limiting nature of ALD film growth with respect to key process parameters including substrate surface exposure to TBHTDT and ammonia will be presented. Surface roughness data as well as conformality data of ALD tantalum nitride in high aspect ratio vias as measured by atomic force microscopy (AFM) and transmission electron microscopy (TEM), respectively, will also be presented. Results of research to evaluate the barrier performance of thermally and bias stressed Cu/ALD tantalum nitride stack using both compositional and electrical measurements will be discussed, as well limiting barrier thickness metrics and determination of the barrier failure mechanisms.

B11.4 THE USE OF CV TECHNIQUES TO INVESTIGATE INSTABILITY MECHANISMS IN 11.1.5 STRUCTURES. S. Paul, W.I. Milne and J. Robertson, Engineering Department, Cambridge University Cambridge, UNITED KINGDOM.

In the field of flat panel displays, the current leading technology is the Active Matrix Liquid Crystal Display; this uses n-Si based thin film transistors (TFT) as the switching element in each pixel. However, under gate bias n-Si H TPT's suffer from instability, as is evidenced by a shift in the gate threshold voltage. Two possible sources of this instability are the creation of midgap states in the n-Si channel and changes in the gate insulator. The shift in the gate threshold voltage is generally measured from the gate transfer characteristics, after subjecting the TFT to prolonged gate bias. However, a major drawback of this measurement technique is that it cannot distinguish whether the shift is caused by the change in the midgap states in the n-Si channel or by charge trapping in the gate insulator. In view of this, we have developed a capacitance-voltage (CV) method to measure the shift in threshold voltage. We employ Metal-Insulator-
Semicrystalline [MIS] structures to investigate the threshold voltage shift as they are much more simple to fabricate than TFTs. We have investigated a large number of Metal/a-Si:H/SiON/SiOx/... Metal/a-Si:H/SiON/SiOx/... structures using our C-V technique. From the C-V data for the MIS structure, we have found that the relationship between the thermal energy and threshold voltage shift is similar to that reported by Weber and Schropp (Appl. Phys. Lett. 144, 87, 2000). The a-Si:H and SiON layers were grown using radio-frequency plasma-enhanced chemical vapor deposition and the SiOx layer was deposited thermally.

**B1.15 CHARACTERIZATION OF THE ELECTRONIC STRUCTURE OF SiC/METAL INTERFACES USING PHOTOELECTRON SPECTROSCOPY**

C. T. Watanabe, John T. Watson, Stephen E. Saddow, Rudy Schaf, Univ. of South Florida, Center for Microelectronics Research, Tampa, FL; Ghyong Chang, Ole Kordina, Sterling Semiconductor Inc, Tampa, FL.

We are presenting results of the investigation of SiC/metal interfaces interesting for device applications. X-ray and ultraviolet photoemission spectroscopy (XPS; UPS) combined with multi-step in-situ thin film growth were used for the determination of the electronic structure and interface chemistry of these systems. In our experiments, the interface was built up in a number of deposition steps during which the metal was grown on SiC substrates. During the growth procedure, the sample surface was characterized by XPS and UPS before deposition and after each deposition step. The resulting set of spectra allowed detailed insight into the interface formation. Inclusion barriers, band bending and interface dipole were determined as well as the chemical structure of the interface.

**B1.16 INTERFACIAL SLIDING IN BACK-END INTERCONNECT STRUCTURES AND ITS MECHANISM**

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High stresses can develop in back-end interconnect structures (BEIS) of micro-electronic devices during thermal excursions because of the large differences in thermal expansion coefficients (CTE) between Si, the interlayer dielectric (ILD) and the interconnect lines. These stresses may induce local plasticity, creep or interfacial sliding within the interconnect structure. These effects are expected to become more prominent with decreasing line dimensions, and increasing ILD cooling, necessitating fundamental studies of the involved deformation mechanisms. Here we report the results of atomic force microscopy (AFM) studies of plastic deformation and interfacial sliding in stand-alone copper interconnect lines on Si, and single- and bi-layer CuAlO2 KILD structures on Si. The AFM measurements demonstrated that plasticity of interconnect lines, accommodated by diffusionally-controlled interfacial sliding occurs in the interconnect structure, resulting in dimensional instability. Further, studies of the cross-sectional density of dislocations and grain boundaries showed evidence of plastic deformation. To understand the mechanism of interfacial sliding, creep experiments were conducted on model planar interfaces between Al and Si, where the kinetics of diffusively accommodated sliding at an interface are expected to be more comprehensively characterized. This phenomenon is proposed, and the role of interface morphology is discussed. It is suggested that future micro-mechanical models of BEIS must incorporate interfacial sliding in order to capture all the possible deformation mechanisms. This research was supported by NSF grant [DMR 0072581] and an SPAWAR Graduate Student Fellowship.

**B1.17 ELECTRONIC TRANSPORTS ACROSS POROUS-CRYSTALLINE SILICON HETEROJUNCTIONS**

M. I. Islam, Sunjay K. Ram, Satyendra Kumar, Dept. of Physics, Indian Institute of Technology, Kharagpur, INDIA.

The understanding of electronic transport properties of porous silicon (PS)/crystalline silicon (c-Si) heterojunctions is crucial in improving the photoluminescence efficiency of metal/PS/c-Si structures. The property of a heterojunction is determined by the interplay of the band-edge offsets and the density of defect states (DOS) within the bandgap. In order to analyze the electrical behavior of PS/c-Si heterojunction, we studied the current-voltage (I-V) characteristics of a series of PS/c-Si junctions as a function of temperature. We found that Al/PS junctions are non-rectifying and quasi-linear whereas Al/PS/c-Si junctions are weakly rectifying h having rectification ratio varying from 2 to 20 at 250 °C for an applied bias voltage for different PS samples. Thus the rectifying behavior is due to PS/c-Si heterojunction, not Al/PS junction. Fitting the I-V data to the conventional diode equation, the diode ideality factor n was found to be about 8 for n = 1 for n < 0.5 V at forward bias, and nearly 1 for 0.5 V < reverse bias. As the temperature decreases, η at both forward and reverse bias increases. At reverse bias, (η) is inversely proportional to temperature and the reverse current exceeds forward current at small biases. These results suggest that the current transport mechanisms operating across the PS/c-Si junctions under forward and reverse biases. We found that the barrier height measured from I-V data for <0.5 V is higher for forward bias than that for reverse bias. For reverse biases, the reverse current increases slowly following ln I ∝ Vβ law. Considering the inhomogeneous nature of PS layer and large DOS distributed spatially and as well as energetically, we tried to explain our I-V results on PS/c-Si junctions by a multi tunneling recombination model for improved efficiency, while carrier generation-recombination and barrier lowering effects for reverse bias.

**B1.18 NEW TECHNOLOGIES FOR SOLAR GRADE SILICON PRODUCTION**

Sergey Kuznetsov, Hyun Metal Ceramics Instrumentation Plant JSC, Russia.

This paper deals with the analysis of different methods for solar-grade silicon production: traditional silane technology, direct carbothermic reduction of silicon from SiO2, chlorine-free silicium technology, silicon production from fluoride. The experimental researches resulted in the development of the technology for solar-grade silicon production using the method of carbothermic reduction with the subsequent cleaning. The research results of physical-chemical properties of the silicon obtained are given. The evaluation of ecological indices of the developed technology is presented.

**B1.19 PHENOMENOLOGICAL AND ELEMENTARY REACTION ANALYSIS OF POLY-SILICON CVD PROCESS**

Ryosuke Shimizu, Toshiaki Jusuma, Masaaki Ogino, Fuji Electric Corporate Research and Development, Ltd., Matsusumo, JAPAN; Yukiharu Shimogaki, Masaaki Sugiyama, Misako Koshi, Univ. of Tokyo, School of Engineering, Tokyo, JAPAN.

Thickness distribution of poly-silicon thin-film was investigated by phenomenological and elementary reaction analysis in a longitudinal type CVD reactor of 30'' manufacturing scale for the first time. Sample wafers were fully charged on the quartz boat and 100% SiH4 and 0.8% PH3 gases with nitrogen carrier gas were introduced from the bottom of the reactor. The deposition temperature and pressure were 550°C and 100Pa, respectively. The thickness profile was measured with a spectroscopic ellipsometer. To analyze the experimental result phenomenologically, concentration distributions of film precursors were examined by solving basic diffusion equation for the CVD system. The analytical solution was a modified Bessel function and the experimental thickness distribution was simulated very well with this solution by optimizing the sticking probability of film precursors. Three kinds of film precursors with different sticking probabilities were found to contribute the polycrystalline deposition. They are SiH4 gas with the sticking probability 1 x 10^{-6} and two kinds of radical species with 7 x 10^{-5} and 5 x 10^{-5} respectively. Subsequently, elementary chemical reaction analysis of poly-silicon CVD process was performed based on elementary reaction mechanisms using ChemKin® and two chemical species, SiH2 and Si, were identified as the possible candidates for the radicals. According to these analyses, the basic deposition of polycrystalline silicon film is due to the source precursor, SiH4, and the profile is almost flat because of its extremely low sticking probability. While the generation rate of SiH2 from the SiH4 gas is very low, the extraordinary deposition around the peripheral region of wafers is explained by the large sticking probability of SiH2. This result is important not only for improving the growth rate uniformity on the wafers, but for the filling up of poly-silicon into a high aspect ratio trenches and vias, and will contribute to the improvement of device performances.

**B1.10 PERIODIC HEATING IN SL-SI**

Kal Renganathan Sharma, Vellore Institute of Technology [Deemed University], Vellore, Tamil Nadu, INDIA.

The temperature of the surface of the IC chip used in VLSI/LSI undergoes (BSL, 1960) a periodic variation by virtue of the fluctuations in the current passing through as a result of the arithmetic operations. Take the surface of the board to be a plane we find the expression for τ = T - τ (τ = (the temperature measured after T = τ max at t = 0), and w (the frequency of fluctuations that are assumed to be sinusoidal). By postulating a solution in the form of complex temperatures and using separation of variables, he showed that the equations governing the temperature may lend itself to an expression for T. However, the parabolic equations that are used in this problem imply an infinite speed of propagation of heat. This can be corrected by the hyperbolic wave propagative equations. Using the hyperbolic partial differential equations the
expression for \( d \) is derived. These solutions are compared with other effects and significance discussed.

**B11.11**

**EVALUATION OF CONTACT AND VIA STEP COVERAGE USING A NOVEL TWO-STEP TITANIUM NITRIDE BARRIER DEPOSITION PROCESS**

Ardy Siddiqi, Choo Spinelli, Todd Grady, STMicroelectronics Inc., Phoenix, AZ; William Brown, Simon Ang, Hamed Naeem, and Richard Ulrich, University of Arkansas, Department of Electrical Engineering, Fayetteville, AR.

Aluminum plug technologies are still used for many different semiconductor device applications and are cost-effective processes. However, there are some disadvantages associated with them. The key disadvantage is aluminum junction spiking caused by aluminum diffusing down into the silicon substrate and silicon diffusing up into the aluminum plug, due to a poor titanium nitride (TiN) barrier. The tungsten plug process is mainly used for 0.5 mm and smaller technologies. A titanium nitride barrier material plays an important role as an underliner for tungsten plugs to prevent the tungsten hexafluoride (WF6) from attacking the titanium (Ti) film. The role of the TiN barrier is to retard or prevent diffusion of the materials that the TiN layer separates. All TiN barriers are not perfect and have limited thermal budgets. Some TiN barriers may not be suitable in via levels because of high deposition temperature or chemistry. In this work, the authors investigated the TiN barrier film properties with respect to nitrogen flows at different power settings and nitrogen gas flows. Different experiments were performed to understand the properties of the TiN film with respect to process variables. Changes in process parameters TiN barrier films were recorded for different process variables and process powers, high chamber pressures. Also, the impact of Rapid Thermal Anneal (RTA) processing on the stress behavior of different TiN barrier films was investigated. This work reports an approach to control the grain size of TiN barrier films as a result of optimizing and minimizing the deposition process. The shift in the columnar grain sample step for any interdiffusion through the grain boundaries. Furthermore, the dual- or two-step barrier process provides a thinner sidewall and bottom TiN step coverage than a standard one-step barrier process, particularly for high aspect ratio conditions for contact and via openings.

**B11.12**

**SOLUTION-BASED PRECURSOR DELIVERY FOR COPPER CVD**

Lixiong Wang, Greg Griffin, Louisiana State University, Dept. of Chemical Engineering, Baton Rouge, LA.

We have measured the growth rates for copper CVD using Cu(far)2 dissolved in isopropanol as the precursor delivery method. This approach offers the convenience and control associated with liquid precursor delivery, while avoiding the high melting point of this precursor. The new method provides similar growth rates to those observed using conventional delivery (i.e., sublimation of solid precursor), but these rates are achieved using a much lower partial pressure of precursor in the reactor. The deposition rate is initially first-order with respect to precursor pressure, but saturates at high values. The rate is also first-order with respect to hydrogen partial pressure. Increasing the hydrogen pressure also shifts the point at which precursor consumption occurs. The isopropanol component improves the uniformity and eliminates nucleation sites. These results suggest that surface diffusion is primarily responsible for initial film morphology.

**B11.13**

**POSSIBLE RELATIONSHIP BETWEEN FermI LEVEL PINNING AND INDUCED NET CHARGE DENSITY AT NON-INTIMATE METAL/SILICON INTERFACE**

Bruno Civid, Faculty of Civil Eng., University of Maribor, Maribor, SLOVENIA; Stefan Institute, Ljubljana, SLOVENIA

It has been recently shown that the reverse biased excess capacitance of various metal/Si/oxide interfaces can be used as a direct measure of the existence of the net charge density that is induced in the interface region. This net charge density has been found to be time dependent and its magnitude appears to be strongly related to the Fermi level pinning at the oxide/metal interface. The net charge density provides the basis for the calculated effective density of states, EDOs, of the pertinent charge carriers, respectively. The deduced effective density of states quantitatively characterizing the charge distribution at the interface, extends over the semiconductor energy gap and is characterized by sharp spikes. The amplitude of spikes is periodically modulated and their envelopes appear as identical, decoupled-like form. The finite number of kramersians slightly overlap and are uniformly distributed over the energy gap, however the spikes density within each kramersian monotonically increases on approaching the conduction band minimum. In this work the question is to what extent the above described spikes densities specify the effective density of gap states at the metal/silicon interface, could be associated with Fermi level pinning in silicon will be examined. In this respect the correlation of various published values of Schottky barrier heights for Ag and Pt metal contacts vs. Schottky barrier voltages, appears to be rather well with the peak positions of the calculated EDOs is being investigated in detail. In the study, our results as obtained by the ionization cluster beam deposition method for various values of the Ag and Pt metal ion beam deposition voltages, appear to be rather well with the peak positions of the calculated EDOs values. It is also for this reason that the findings are to be contrasted with the Drummond’s [2] predictive model for various near surface defects in GaAs claimed to be the origin of several Fermi level pinning levels for this compound. Some possible applications of the findings above as related to physics of semiconductor devices will be also discussed. [1] B. Civid and D. Koroljuk, J. Appl. Phys., to be published. [2] T. J. Drummond, Phys. Rev. B50, 8182 (1999).

**B11.14**

**NEARFIELD ULTRASONIC IMAGING: A NOVEL METHOD FOR NONDESTRUCTIVE SUBSURFACE IMAGING OF IC INTERCONNECTS**

Gajendra S. Shethkarni, Huimin Xie, Yueqin Zheng, and R.E. Green, Univ. at Albany Institute for Materials, Albany, NY.

Nondestructive subsurface imaging is of great interest for backend-of-line (BEOL) integrated circuit (IC) interconnect structures due to the need to reliably identify subsurface flaws in nanoscale metal lines and mechanical defects in metal/low-k structures. Conventional acoustic microscopy has found limited application in subsurface imaging of BEOL interconnect structures due to its poor spatial resolution (um) and the necessity results from high-frequency transmission losses in field acoustic lenses that limit spatial resolution. In this work we report on the development of an alternate approach to nondestructive, noncontact, subsurface imaging for IC interconnect structures: Near-field ultrasonic imaging. This approach utilizes a heterodyne interferometer based on a scanning probe microscope, similar to so-called heterodyne force microscopy (HFM). Ultrasonic excitation of subnanometer vibrations in an SPM cantilever probe tip modulated with ultrasonic waves applied to an IC interconnect test structure. Subsequent heterodyne interference between these two signals is observed assuming a nonlinear tip-sample interaction. This interaction is sensitive to the relative phase difference of the two ultrasonic excitations and enables phase-sensitive imaging. Proof-of-principle demonstrations of this technique are presented for ultrasonic phase-imaging of Cu/low-k interconnect structures for a range of ultrasonic carrier frequencies. Spatial resolution <10 nm is demonstrated. These results are compared to simulations based on the Johnson-Kendall-Roberts (JKR) model for the mechanical interactions of a scanning probe tip with a surface. Calculations for deep/sub-surface mechanical resolution with respect to surface and subsurface contributions to the phase image for Al/low-k and Cu/low-k IC interconnect test structures.

**B11.15**

**STUDY OF Ta2O5 BASED MOS CAPACITORS, WITH Ta3O7 OXIDIZED IN O2/NIH AMBIENT.**

Pallavi Krishnammohi, A.N. Chander, Dept. of Electrical Engineering, IIT Bombay, INDIA

Tantalum pentoxide, an alternative to SiO2, is a high-k dielectric for DRAM and MOS applications, faces the problem of interface mismatch as silicon. SiO2/SiTa2O5 interface layer were suggested to overcome the interface problem. Here we study the physical and electrical characteristics of Ta3O7 oxidized in O2/NIH ambient, and without any other interface layer. This is done to check if N/H moves to the interface, and thus improves the electrical properties. However XRD studies of the film, showed the presence of Ta2O5, unoxidized Ta and TaN in the film. But the intensity of these peaks decreased with the increase of NIH content. The maximum capacitance was reduced, compared to that of pure Ta2O5 films. Vp varied from 1.1-1.9 V. Oxide changes in the films varied from 3.6-12 J/cm². But the traps in these films were found to be almost negligible as observed from the hysteresis of C-V characteristics. Films with N/H showed lesser oxide charges by one order of magnitude, as compared to pure Ta2O5 films.

**B11.16**

**CHARACTERISTICS OF REMOTE OXYGEN AND HYDROGEN PLASMA DRY CLEANING OF FLUOROCARBON RESIDUES FORMED AT THE CONTACT HOLES**

Hae-kyun Yoon, Sung Bae
Kim, Hyunguk Seo, Jongnook Song, Yangdo Kim, Hyoeung Jeon, Hanyang Univ, Div of Materials Science and Engineering, Seoul, KOREA; Hyun Soi, Young Chi Kim, Hanyang Univ, Dept of Chemical Engineering, Seoul, KOREA.

Reactive ion etching (RIE) using fluorocarbons is widely used to open contact holes due to its high anisotropic and selective silicon etching characteristics. However, the RIE process induces nonvolatile and chemically stable fluorocarbon residues and these residues typically cause high contact resistance at the metal-silicon interface. Moreover, it is very time consuming to remove such residues. A new aspect ratio ratio structure especially with sub-micron diameter contact hole size. In previous reports, the oxidizing process followed by wet chemical stripping, dipping in hydro sulfuric acid (H2SO3) and hydro fluorid (HF) acid based scheme, was the most effective method to remove fluorocarbon residues. However, a large quantity of these wet chemicals increased the process cost and caused significant environmental problems. In this study, low temperature remote plasma dry cleaning process that removes both the PR and polymer residues containing carbon and fluorine after RIE process has been investigated. The cleaning efficiencies of remote oxygen and hydrogen plasma were systematically evaluated at various conditions such as plasma power, exposure time, gas flow rate and sample temperature. Remote plasma was used to minimize plasma damage by keeping the substrate distant from discharge region. Preliminary results showed that the hydrogen plasma cleaning was essentially required to remove the residual carbon contaminants on silicon surface after oxygen plasma cleaning. Also, two step cleaning, oxygen plasma ashing and subsequent hydrogen plasma cleaning, was very effective to remove carbon residues and polymer without forming SiO2 layer on silicon surface after cleaning process.

B11.17 EFFECTS OF BOROPHOSPHOSILICATE GLASS DOPANT CONCENTRATIONS ON ISOTROPIC ETCH PROFILE. Chris Gibson, Bradley R. Williams, Stacey Evans, AMI Semiconductor, Inc, Piscataway, NJ.

In the process of chemically etching contact openings, film characteristic of the borophosphosilicate glass (BPSG) film strongly effect the formation of an ideal contact profile. Ideal contact profile requires a smooth glass shape to provide better metal step coverage in to the contact opening in comparison to a vertical sidewall profile. The rounded shape of the glass is etched chemically (isotropic) allowing for etch in the vertical and horizontal direction. As the addition of dopants to the oxide film effect the etch rate, the profile of the isotropic etch will change which in turn effect electrical device properties, down stream processes and device reliability. BPSG film characteristics are the area of investigation. Characteristics of concern are weight percent concentrations of boron and phosphorus, film density and dopant concentration profiles in relation to depth. To evaluate the entire contact formation module, chemical etch characteristics including etch rate in relation to film depth for thermal oxide films were also investigated. Experiments were conducted in the form of a response surface design was used to model effects of previously discussed BPSG film characteristics. To achieve the desired and predictable etch rate of BPSG in buffered oxide etch (BUE) calculated control limits were placed on the boron and phosphorous dopant concentrations. Results showed that dopant effects on the isotropic etch process exceeded the control capability of dopant concentrations in the deposition process. In relating process control capabilities to these limits, a Cpk (6) is considered capable. To eliminate previously discussed defects created in the isotropic etch process, reject limits for dopant concentrations in BPSG film deposition process would need to be set well within the typical 3S giving a Cpk below 1.5.

B11.18 EPITAXIAL GROWTH OF CoSi2 ON Si(100). Ryan Chong, Mark Vendron, Shue Yin Chow and Chaw Sing Ho.

Epitaxial silicides are of interest in advanced CMOS front-end technology for its larger thermal stability and lower interfacial roughness than their polycrystalline counterparts. We report the synthesis of epitaxial CoSi2 on Si(100) by a reactive deposition technique. Using real-time in-situ transmission electron microscopy and XRMV conditions (MIELSYSTEM) we observe the direct formation of CoSi2 on the Si(100) surface with no intermediate phase formation. The experimental data will be compared with the deposition and anneal of Co on the clean (3x1) reconstructed Si(100) surface. Under these conditions, the formation of polycrystalline CoSi2 was observed, as expected. The mechanisms of epitaxial silicide formation were elucidated from video recordings of the growth process which will be discussed.

B11.19 Cu PATTERNING USING A SELF-ALIGNED Mo O MASK Yeonkyu Ko, Hojeong Yang, Jaegul Lee, Roomkin Univ, School of Metallurgical and Materials Engineering, Sungbuk-Gu, Seoul, KOREA.

Development of a Cu patterning method has been one of the most important technical procedures that need to apply for the gate electrodes of thin film transistor liquid crystal display (TFT-LCD). A self-aligned surface MoO layer was used as a mask in the new process. The surface MoO was formed by diffusion from Cu film to surface. Cu(4.5% Mo) film having thickness of 4000 Å was annealed in O2 ambient at 15 mTorr, 500° for 30min, followed by patterning of the MoO layer using photolithography and HF wet etch process. The patterned MoO was reduced in an H2 ambient and the (H2fo) gas was simultaneously flowed toward the film for dry etching. Total pressure of O2 and H2fo in the reactor was constantly maintained at 200 mTorr (O2/H2fo=1:1). The self-aligned MoO films successfully played a role of mask for dry etching the Cu(Mo) films with a taper slope. As a SiH2 TFFT was fabricated with the dry etching process. The n-SiH TFFT using the MoO mask showed good subthreshold slope, on/off current ratio, and output characteristic.

B11.20 THE EFFECT OF THE MICROSTRUCTURE OF DIFFUSION BARRIERS ON THE PALLADIUM ACTIVATION FOR ELECTROLESS COPPER DEPOSITION. Seeck Woo Hong, Yong Sun Lee, Jong-Won Park, Div. of Materials Science and Engineering, Hanyang University, Seoul, KOREA; Ki-Chul Park, Samsung Electronics, Kyungki-Do, KOREA.

Cu is being widely used in ULSI metallization process as a replacement for Al due to its lower resistivity and higher electrochemical resistance. Electroless Cu deposition is one of the most promising candidates for Cu processing because of low cost and high quality of electrolytic Cu films. Copper can be deposited on a catalytic surface from an ionic solution without any external power supply by electrolytic plating. The electrolytic copper reaction is an autocatalytic reaction. This means that once there is an initial layer of copper, the reaction continues indefinitely. Since the surface on which electrolytic copper is not deposited, an activation process is usually necessary in order to start electrolytic copper deposition. Gold, platin, and palladium is required as catalytic layer for reliable electroless copper deposition, so the activation process is a key process for successful copper electroless plating. In this paper, palladium activation on Cu magnetron sputtered TiN and TaN as diffusion barriers for autocatalytic electrolytic copper deposition has been investigated by using X-ray diffraction, sheet resistance measurement, field emission scanning electron microscopy, photoemission transmission electron microscopy (TEM). The density of palladium nuclei on TaN diffusion barrier was decreased with the increasing grain size of TaN films which was caused by increasing nitrogen content in TaN films. Plan view TEM results showed that palladium nuclei formed mainly on the triple points of the grain boundaries of the TiN diffusion barriers.

B11.21 FIRST BLAST COMPONENT CLEANING TECHNIQUES TO REDUCE PARTICLE GENERATION IN ETCH AND DEPOSITION SYSTEMS. Ronald Burgess, Dave Lamee, BOC Edwards-Kochlin, Phoenix, AZ; Andy Silliman, Chuck Spacer, Sven Zheng, Tim Ben Chew, Todd Grady, Steve Melroy, Jerome Vetier, ST Microelectronics, Phoenix, AZ.

Particles emanating from wall, shields and other components of the chambers in which integrated circuit wafers are processed are a major factor which has been shown to contribute to the formation of defect sites on completed wafers. Typically, the generation rate of particles is influenced by the final treatment that the surface of these components receive prior to installation in the chamber. Quartz components, prepared from material characteristic of contemporary bell jar manufacture, were subjected to typical post cleaning steps. These were surface texturing, post blast etching, pressure washing and ultrasonic rinsing. The relative effectiveness of these steps was assessed with a conventional experimental matrix. The chambers were evaluated for potential particle generation by two methods. First, carbon lift-off techniques were used to evaluate relative numbers of weakly attached particles on the surface of the coupons. Secondly, laserscans were prepared to examine the depth and type of substrate damage capable of contributing to particle generation. Current methods to promote adhesion of deposits to PVD shielding require increasing surface roughness by abrasive blasting. This technique is known to embed fractured grit particles into the metal substrate. Cleaning processes intended to remove micro-particles following grit blast are only marginally successful. This experiment was designed to optimize grit blast processing for unintended grit removal. Stainless steel spheres, prepared from used shell.

The thermal stability on porous low-k, P-SiLK with dielectric constant about 2.4, has been studied. The effects of thermal cycles on porous low-k film such as shrinkage, refractive index, dielectric constant, porosity, hardness, and particle size distribution were examined. Film is spun on silicon substrate, baked and cured in the vertical furnace for 1 hour at 430°C under N₂ ambient. Thermal cure is done in the vertical furnace with oxygen level less than 10 ppm. Two curing temperatures (430°C and 450°C) are applied and compared in the thermal stability after several thermal cycles. Each thermal cycle is one hour but the film is checked for every alternate cycle. We observed that after the first thermal cycle of 450°C and 430°C cured, the refractive index is increased and about 0.8% and 0.4% respectively. Dielectric constant is slightly increased after 450°C cured but that is no significant change for 430°C cured. Change in film properties investigated by using optical profile, FTIR, mercury probe, refractive index and TEM. Organic low k material SiLK with dielectric constant about 2.8 is used as a baseline for comparison.

8:30 AM B12.3
CHARACTERISTICS OF LOW- K AND ULTRA-LOW- K PECVD DEPOSITED SiCOH FILMS: A. Grill, V. Patel, K. Rodbell, S. Christensen and E. Simony, IBM Research Division, T.J. Watson Research Center, Yorktown Heights, NY.

We have shown previously that the dielectric constants of PECVD SiCOH dielectrics can be extended to ultralow-k values of k~1.5. The reduction in the dielectric constant has been achieved by adding an organic precursor to the tetramethylethylene(tetramethylethylene (TMCTE) used for the preparation of the SiCOH dielectric and amending the films to remove the thermally less-stable organic CH₃ functions from the films to add porosity and reduce the density of the films. In order to estimate the effects of the reduction of the value of the dielectric constant on the properties of the material, the films have been characterized by IR and FTIR, positron annihilation spectroscopy, TEM, AFM, nanodispersion measurements, stress vs. temperature and photothermal deflection measurements. The obtained characteristics of the films will be presented and discussed as a function of the deposition conditions and in relation to the dielectric constants.

8:45 AM B12.4
A NEW ULTRA-LOW- K ILD MATERIAL BASED ON ORGANIC-INORGANIC HYBRID RESINS: Ben Zhang, Cory Borgerman, Ken Weidner, Herman Meynen, Paul Schalk, Alan Peck, Stephane Malhousiere, Marleen Van Hove, Karen Mues, Dow Corning Corporation, Midland, MI. Dow Corning Corporation, Seneffe, Belgium; TMIC, Heverlee, Belgium.

A ULK material based on a silicon resin has been developed that can be coated on silicon wafers by spin coating, and both cured and reprocessed porous by a simple thermal treatment in an inert atmosphere. The chemical bonds between the resin and porogen groups prevent the phase separation of the porogen from the resin during curing and lead extremely small pores. The highly hydrophilic thin films made from this material display Dk of 1.8, breakdown volt of 4 MV/cm, a cohesive strength > 60 MPa, excellent crack resistance, and an average pore size of 2 km by PALS and 2.5-3.0 nm by EP. In this presentation, our strategy for designing low-k materials, the material properties and integration results for this new material will be discussed.

9:00 AM B12.5
A NEW APPROACH OF THIN-FILM X-RAY REFLECTANCE/SCATTERING ANALYSIS FOR ULTRA- LOW-K DIELECTRICS WITH PERIODIC POLE STRUCTURES: N. Hara, MRAL-AIST, Tsukuba, Japan; Y. Oku, K. Yamada, MRAL-AIST, Tsukuba, Japan; Y. Azuma, I. Kojima, NML-AIST, Tsukuba, Japan; T. Kikkawa, MRAL-AIST and Hiroshima Univ., Highashi-Hiroshima, Japan.

We propose and demonstrate experimentally a new structural characterization technique for ultra-low-dielectric-constant thin films with periodic porous structures by employing a new analytical approach to X-ray reflectance / scattering data. The analytical approach which we propose here takes specular reflection, incoherent scattering from random distribution of, and coherent scattering from periodically modulated distribution of electron density into account. Thin-film measurements by reflectance and scattering of X-ray are known for their advantages in sensitivity and non-intrusiveness. Interlayer dielectrics with dielectric constant (k) less than 1.5 will be required in future integrated circuit technology for high enough transmission speed of signal and low enough energy consumption. On the other hand, candidate materials ever studied, do not
show k values well below 2 without inclusion of pores or open volume structures in them. As the pore volume fraction is increased for lower k values, there are increases in the resulting in increase of average (connected) pore volume and hence in deterioration of film mechanical properties. Efforts to introduce periodicity in pore structure are undertaken to resolve the problem. Once the porosity is introduced, however, the X-ray measurement technique starts to suffer from the signal associated with the anisotropy and coherent scattering or diffraction from the periodic modulation of electron density, and new approaches become necessary for information about the internal structure itself, but also about the residual random structure in the “wall” material as well as about the overall structural disorders; all those parameters are important in assessing relationship between k and such essential properties for integration as mechanical properties, stability and reliability. By comparing the experimental data taken under specular reflection and off-angle scattering both in cut-off plane and in-plane geometries with the proposed model calculation, the contributions from the origins are successfully separated.

9:15 AM B12.6
NOVEL PERIODIC NANOPORE SILICATE GLASS WITH HIGH STRUCTURAL STABILITY AS LOW-k THIN FILMS.
Yoshihiko Oku, MIRAI-ASET, Ibaraki, JAPAN; Norikazu Nishiyama, Shimatsu Trusnak, Korekane Oya, Osaka Univ, Dep. of Chemical Engineering, Osaka, JAPAN; Nobutomo Hara, MIRAI-ASET, Ibaraki, JAPAN; Takamara Kikkan, MIRAI-ASET, Ibaraki, JAPAN and Hiroshima Univ, Research Center for Nanodevices and Systems, Hiroshima, JAPAN.

Reduction of interconnect parasitic capacitances has become more important to fabricate high-speed ULSI’s for 100 nm technology node and beyond. In order to meet with this requirement, various interconnect architectures with low (<2.6) thermal conductivity (<5 W/m·K) were explored. Introducing pores into dielectric material is an effective method to fabricate low-k films with dielectric constant of less than 2.6. The dielectric constant of air is 1.0. Conventional porous films, however, did not have enough mechanical strength and electrical properties as expected. Therefore, pore formation technology in dielectric film must be improved for development of low-k (k ≈ 1.5) for 70 nm technology node. We have developed a novel periodic nanoporous silicate glass with high structural stability as a low-k thin film by spin-coating method. Conventional porous silicate glass films have caused structural shrinkage (>20%) or more) by calcination of the spin-coated films. In this investigation we adopt special treatment before calcination. Our novel nanoporous film shows no shift of XRD peak position after calcination at 673K, indicating that both the ultimate mechanical strength and the minimization of stress at the interface between the prepared film and the underlying substrate can be achieved. Such shrinkage-free periodic nanoporous silicate film can possess higher VBD (break down voltage) and lower L_EAR (leak current). In this study we evaluated electrical properties (dielectric constant, V_BD and L_EAR) by IV and CV measurements, structural properties (including information on pores) by XRD, XRR, TEM, and mechanical properties (hardness and Young’s modulus) of this special-treated nanoporous silicate film. The dielectric constant was evaluated to be around 1.5 at 1MHz.

10:00 AM B12.7
POROUS METHYLSILSESQUIOXANE LOW-k DIELECTRIC FILMS: MECHANICAL BEHAVIOR, MOISTURE SENSITIVITY, ABDO REHAB, University of Michigan, USA; Abraham Bud and Malcolm Muderspach, IBM Materials Science and Engineering, Stanford, CA; Robert Miller, Willi Volkeme, IBM Almaden Research Center, San Jose, CA; Reinhold Drauckard, Dept of Materials Science and Engineering, Stanford, CA.

Methylsilsesquioxanes (MSQ) films are primary candidates to replace silicon as the interlayer dielectric in future generations of microelectronic devices. More importantly, the dielectric constant of MSQ is continuously tuned with the increase of porosity at nanometer length scale. However, before integration is possible it is necessary to understand and quantify the mechanical and fracture behavior of these thin films. Specifically, the addition of porosity may have detrimental effects on many of the required mechanical properties, which will reduce survivability during CMP and lower the resistance to electromigration back stresses during operation. The effect of porosity on a range of salient mechanical properties including inherent fracture resistance, adhesion, and elastic modulus will be addressed for several resin formulations. Various other factors, including surface modification with UV-cure, will be presented. The implications of different matrix microstructures and pore architectures are discussed.

10:15 AM B12.8
THERMAL STABILITY STUDIES ON 2,4,6,8-TETRA-METHYLCYCLOTETRAEOSXANE (TMCTS). Chongying Xu, Alexander S. Boroviak, Ziyun Wang, Jose Armo and Thomas H. Eatman, ATMI Inc., Danbury, CT.

2,4,6,8-Tetramethylcyclooctasiloxane (TMCTS) is being considered as a precursor for CVD of low dielectric constant (k) thin films as interlayer dielectrics in an integrated film mechanical properties. Efforts to introduce periodicity in pore structure are undertaken to resolve the problem. Once the porosity is introduced, however, the X-ray measurement technique starts to suffer from the signal associated with the anisotropy and coherent scattering or diffraction from the periodic modulation of electron density, and new approaches become necessary for information about the internal structure itself, but also about the residual random structure in the “wall” material as well as about the overall structural disorders; all those parameters are important in assessing relationship between k and such essential properties for integration as mechanical properties, stability and reliability. By comparing the experimental data taken under specular reflection and off-angle scattering both in cut-off plane and in-plane geometries with the proposed model calculation, the contributions from the origins are successfully separated.

10:30 AM B12.9
ELECTROMIGRATION IN SUBMICRON DUAL-DAMASCENE Cu/Low-k INTERCONNECTS. KiDon Lee, Xin Lu, Emiss T. Ogawa, Hideki Matsushita, and Paul S. Ho, The University of Texas at Austin, Microelectronics Research Center, Austin, TX; Victor A. Bhatkhe, and Rod Augur, International SEMATECH, Austin, TX.

Electromigration (EM) lifetime characteristics and failure mechanism have been investigated for Cu/SiLK and Cu porous MSQ interconnects as compared to Cu/oxide interconnects. SiLK is an organic polymer developed by the Dow Chemical Company with k of 2.7 and Porous MSQ is a spin-on porous silicate with k of 2.4. The activation energies were found to be 0.97 eV for SiLK and 0.80 eV for the porous MSQ, similar to that of oxide. This range of activation energies suggests a similar mass transport mechanism, interfacial diffusion. The current exponent of SiLK and oxide were found to be 1.1 and 1.2, respectively. In the low-k interconnects, distinct failure mechanism for Cu/low-k interconnects due to internal Cu extrusion at the anode under the capping layer has been observed and it seems to be related to thermomechanical properties of low-k materials. The short lifetime characteristics of low-k interconnects can be attributed to a smaller back stress due to smaller confinement effect. The critical length effect has been found to be smaller for Cu/low-k than for Cu/oxide. Results obtained in this study indicated that thermomechanical properties of low-k interconnects, including interfacial adhesion, failure mode of low-k material, Joule heating, mechanical strength (E) and CTE are important parameters in controlling EM reliability of Cu/low-k interconnects.

10:45 AM B12.10

The results of an experiment designed to investigate the effects of post deposition ultraviolet (UV) assisted O2 annealing on the properties of high-permittivity (ε) films on silicon are reported. Although previous work has demonstrated low temperature (350-400°C) post deposition UV O2 annealing can improve the physical and electrical properties of high-ε films [1], the mechanism is not fully understood. The high-ε film chosen for the experiment was Ta2O5 fabricated by UV assisted Injection Liquid Source Chemical Vapour Deposition (UVILS-CVD) on Si(100) substrates. The UVILS CVD technique allows the high-ε deposition and post deposition annealing to be performed in the same reaction chamber. Leakage current densities are reduced by up to six orders of magnitude as a result of a 350°C post deposition UV O2 anneal. The anneal step increases both the refractive index (2.01 to 2.21) and film stoichiometry (TaO2.1 to 2.47). From SIMS analysis, this improvement has been attributed to the removal of Si, N and C from the film leading to a decrease in the inplane and out-of-plane defects. The UV anneal in O2 creates oxygen free radicals and oxide (the bond strength is 5.17 eV; the UV photon energy is 5.68 eV). It is proposed that these contaminants are removed in the gas phase (CO, CO2, SiO, NO, N2, O2), followed by hydrogen gas radicals. In addition, the UV O2 irradiation provides O free radicals to the redeposited suboxide, which is evidenced by the increase in the stoichiometry of the film after the 350°C UV O2 anneal. Results will be presented in these experiments performed in vacuum conditions, which support this theory. The technique is currently being extended to alternative high-ε dielectrics, including HfO2 and mixed Ta2O5-Ta2O5 layers, using carbon-based metalorganic precursors [1]. J. Zhang et al., J. Phys. D. Appl Phys, 32, L91, [1999].

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11:40 AM B12.11
POROSITY EFFECT ON THERMOMECHANICAL PROPERTIES OF ORGANIC-METALLIC FILMS. Dongwan Gwon, Jianjun Liu, Paul S. Ho, The University of Texas at Austin, Microelectronics Research Center, Austin, TX, Willi Volksen and Robert D. Miller, IBM Almaden Research Center, San Jose, CA.

Degradation of the thermal and thermomechanical properties with porosity is a key concern regarding the implementation of ultra low dielectric constant (low-k) porous materials. In this study, a bending beam method was employed to measure the Young's modulus, coefficient of thermal expansion (CTE) and Poisson's ratio of thin films. 1 was used to investigate the thermomechanical behavior of the porous Methylhexaethoxysilane (MSQ) films prepared by incorporation of macromolecular 'porogens'. 2 The stress of the films with a porosity range from 0% to 50% was measured during thermal cycling at a ramping rate of 2°C/min. It was shown that the stress decreased linearly with the increase of temperature and could be measured at any temperature. As a function of the film modulus and CTE the film, the slope of the temperature-stress curve was calculated as a function of porosity. It decreased with porosity and a sharp drop appeared around 20% porosity. Compared with the thermal conductivity measured by the 3 technique, and the dielectric constant of the films, the modulus demonstrated a much more profound transitional behavior. It is suggested that the sharp drop is due to a transition in pore morphology from closed cell to interconnected open cell structure at the percolation limit.


11:15 AM B12.12
INTERFACIAL ADHESION STUDY OF POROUS LOW-K TO CVD BARRIER LAYERS. Caroline C. Merrill, Paul S. Ho, Univ. of Texas, Microelectronics Research Center, Austin, TX, Jeffrey A. Lee, Jeffrey T. Wetzel, International Sematech, Austin, TX.

The drive for smaller and faster microelectronic devices has led to the introduction of low-k dielectrics for interconnect applications. The weak thermomechanical properties of low-k dielectric causes serious concerns on reliability and integration of Cu/low-k interconnects. Indeed, during fabrication, thermal stress rise due to mismatching in coefficients of thermal expansion (CTE) and elastic properties of the materials. The interfacial adhesion of thin film becomes critical to the integration and reliability of low-k interconnects. This paper will present the results from an application of the 4-point bending technique to characterize the adhesion strength of ultra low-k dielectric materials to CVD barrier layers. Adhesion energy between an ultra low-k dielectric material and a barrier layer was measured as a function of coverage (0 < k < 2.3). It was found that the adhesion energy decreases with the dielectric constant which correlates with mechanical properties such as Young's modulus and hardness. Adhesion measurement data were also obtained for different low-k / Barrier layer interfaces. The independence of energy on the type of interface suggests that the fracture is actually occurring in the low-k material and not at the interface. In addition, the very low fracture energies (G < 3 J/m²) confirm the weak mechanical properties of such materials. Recent failure analysis studies with failure surface analysis using Auger electron spectroscopy and scanning electron microscope.

11:30 AM B12.13
SILICONE-DURING THIN FILMS. Joseph B. Vella, Alex A. Vologny, Indira S. Adhithy, Motorola, Digital DNA of Labs, Process and Materials Characterization Lab, Mesa, AZ, William W. Gerberich, University of Minnesota, Dept. of Chem. Eng. and Materials Science, Minneapolis, MN.

Due to the radical compromise in thermal and/or mechanical properties that the migration from silicon dioxide to novel low-k dielectric films necessarily incur, the IC industry is motivated to better understand the failure modes of low-k dielectric films. These failure modes include thermal instability, poor mechanical strength, and chemical-mechanical polishing (CMP) failure due to low cohesive and adhesive fractures. The failures studied at SEMATECH have indicated that CMP reliability of low-k can be correlated with the elastic modulus of the film. However, we believe that the modulus is only one of many critical mechanical properties that will be impacted by the film materials. Silicon- and porous films typically have low elastic modulus of 1 to 10 GPa and relatively high hardness of 0.5 to 1.5 GPa. With the high hardness to modulus ratio, low fracture toughness can be also expected. In this study we outline other properties of silicon-
2:00 PM B13.2
EBIC AND STEM ANALYSIS OF HIGH VOLTAGE SAMOS
RELIABILITY FAILURES. Larry Rice, Motorola, Inc., Process and Materials Characterization Laboratory, Mesa, AZ.

Microscopes are faced with many challenges in locating and examining failure sites in the ever-shrinking semiconductor device. The site must be located using electrical characterization techniques like electron beam induced current (EBIC), photo emission microscopy (PEM), or liquid contact (LC) then cross-sectioned with a focused ion beam (FIB). Both PEM and LC require the semiconductor circuit to be in an operating condition which has been observed to locally melt the area of interest frequently destroying evidence of the failure mechanism. In contrast, EBIC typically performed at low or no applied voltage eliminating further damage to the circuit. EBIC has been applied to locate leakage sites in high voltage metal oxide semiconductor (MOS) electrostatic discharge (ESD) reliability failures. In addition to a brief review of the basic principles of EBIC and describing a technique to successfully cross section ‘hot spots’ for transmission electron microscopy (TEM) observation, focus will be placed on a case study of the reliability testing failure analysis of ESD power transistors using EBIC, scanning electron microscopy (SEM), FIB, and transmission electron microscopy (TEM).

2:15 PM B13.3
LENGTH EFFECTS ON THE RELIABILITY OF DUAL-DAMASCENE Cu INTERCONNECTS. F.L. Wei, Massachusetts Institute of Technology, Department of Materials Science and Engineering, Cambridge, MA; C.L. Gon, Singapore-MIT Alliance, Advanced Materials for Micro- and Nanosystems Programme, SINGAPORE; H.K. Woon, Massachusetts Institute of Technology, Department of Materials Science and Engineering, Cambridge, MA; and Singapore-MIT Alliance, Advanced Materials for Micro- and Nanosystems Programme, SINGAPORE; J.J. Clement, Sandia National Laboratory, Albuquerque, NM; and Singapore-MIT Alliance, Advanced Materials for Micro- and Nanosystems Programme, SINGAPORE; and National University of Singapore, Department of Electrical & Computer Engineering, SINGAPORE.

We have carried out experiments on dual-damascene Cu interconnects with different lengths. We find that, unlike Al-based interconnects, the reliability of Cu-based interconnects improves at short lengths. For Al, some short Cu lines do not form voids that cause failure before back-side stress causes void growth to stop. However, unlike Al-based interconnects, there does not appear to be a minimum current density-line length product (JL) for which all lines are immune. It is thought that this is related to the absence of a conducting refractory overlayer in Cu technology that can shunt current around small voids, as conducting anti-reflection coating layers do in Al technology. Also, unlike Al, Cu interconnects have a shorter time to failure and the deviation in the time to failure increases for longer lines. A sub-population of long lines survive for very long times. It is thought that this is the result of rupture of the thin refractory metal liner at the interconnect level rather than Cu. In the presence of this complex behavior, there are intermediate line lengths with minimum median lifetimes and minimum lifetime variations in Cu metallization.

3:00 PM B13.4
EFFECT OF METALLIC CONTAMINATION ON INTERFACE PROPERTIES AND OXIDE RELIABILITY. Elena Oberoi, Center for Microelectronics Research, University of South Florida, Tampa, FL; Scott Campbell, Department of Chemical Engineering, University of South Florida, Tampa, FL; Drew Hoff, Center for Microelectronics Research, University of South Florida, Tampa, FL; Richard Gilbert, Department of Chemical Engineering, University of South Florida, Tampa, FL; Eric Persson, Darrell Simpson, Agere Systems, Orlando, FL.

New and emerging process technologies are creating contamination control challenges for current and future generations of integrated circuits. Damascene interconnects, metal gate and metal silicide processes are representative of many potential sources of metallic contamination to wafer structures. In this work, we studied contamination of oxidized silicon wafers by several metals of industrial importance including copper, cobalt, sodium, iron and nickel. Contamination experiments were conducted at temperatures ranging from 200 to 850°C, and oxidation times of 10 to 300 minutes. The concentration of the contamination was estimated using XPS-ICPMS and SIMS. The effects of contamination on interface and oxide reliability were quantified by non-contact COCOS (Corona Oxide Characterization of Semiconductor) and SLIC (Stress Induced Leakage Current) techniques. We discuss the relationships identified between surface analysis results and the non-contact measurement of oxide reliability and interface properties.

3:15 PM B13.5
MECHANICAL-STRESS CONTROLLED SILICIDE INTERCONNECTIONS FOR HIGHLY RELIABLE SEMICONDUCTOR DEVICES. Hiromi Shimizu, Hideki Muray, Hiroshi, Ltd., Mechanical Engineering Research Laboratory, Tokyo, JAPAN.

Silicidation is one effective way of reducing contact resistance between a metal and silicon. Titanium silicide is one of popular material for highly reliable interconnect applications. Titanium film is deposited on poly-Si plugs, which are embedded in a silicon dioxide layer, and annealed at about 800°C to form titanium silicide between the poly-Si plug and the metal interconnect. The first reaction from Ti to TiSi2 starts at about 500°C, and the second reaction from TiSi to TiSi2 starts at about 600°C. However, this silicidation technique causes higher tensile stress than 1 GPa in the reacted silicide film due to volume shrinkage during the silicidation; thus, it sometimes causes delamination between the reacted silicide and the remaining silicon. The stress developed near the interface between the poly-Si and the reacted silicide film was analyzed using a finite element method by considering the silicidation-induced stress. The developed stress near the interface strongly depends on both the thickness of the newly grown silicide and the diameter of the contact. It increases with increasing thickness of the silicide and decreasing the contact diameter. The developed stress reached the critical stress for delamination at the interface when the thickness of TiSi2 was thicker than 75 nm and the diameter of the contact was smaller than 0.3 μm. It is, therefore, very important to minimize the thickness of the silicide in order to eliminate delamination at the interface. Increasing the annealing temperature for the silicidation higher than 800°C is another effective way for reducing the stress, because the developed stress reduces due to viscoelasticity of the silicide film. We have made clear the developing process during titanium-silicide formation and an effective design rule for the highly reliable silicide interconnection.

3:30 PM B13.6

Aluminum-wire/tungsten-plug based multi-level interconnect technology for VLSI circuits in the semiconductor industry. The early interconnect failure in the W-plug via structure has been recognized as a generic phenomenon. In this work, we present detailed studies of two integration schemes for high density multi-level interconnect module for sub-quarter-micron CMOS technologies, and discuss the benefits and drawbacks of each of them primarily from a process integration point of view. We demonstrate that an etch stop integration scheme in the via etch step is the most practical integration scheme. As a result of significant improved via electromigration performance compared to an over etch integration scheme in which the via and etch into the underline AlCu, we also identified several highly detrimental early failure modes associated with the over etch structure, which showed that such early failure modes could be prevented in the etch stop integration scheme. All test structures were processed using manufacturing tool sets at a state-of-the-art eight-inch silicon fab of Agere Systems. Detailed information regarding metallization compositions for metal wires and via liners, electromigration failure distributions, FMA (failure mode analysis) of early interconnect failures, via contact resistances, metal sheet resistances, interconnect yields, and their correlation with different integration schemes will be presented. Even though there are some small penalties in the device performance in the etch stop integration scheme, the benefits in the reliability and the better tolerance to manufacturing process variations clearly justify the adoption of this robust multi-level ULSI interconnect module for sub-quarter-micron CMOS technologies.

3:45 PM B13.7
INTERFACE ADHESION OF PATTERNED INTERCONNECT STRUCTURES. Christopher S. Littke and Reinhold H. Dauskardt, Department of Materials Science and Engineering, Stanford University, Stanford, CA.

Recent studies of the adhesion of blanket thin-film interconnect structures have established that plastic energy dissipation in thin metal and polymer films, such as copper and low dielectrics, is related to the thickness of the metal film and the in-plane stress parameters. However, there is currently little understanding of how the geometry and size of
interconnect features utilized in technologically relevant structures will influence plasticity and hence the fracture resistance of such patterned structures. Accordingly, to investigate the role of feature size and shape, selected patterned structures containing arrays of polymer and metal lines with varying aspect ratios have been investigated. Macroscopic adhesion values were determined by measuring the critical strain energy release rate, $G_c$, for debonding of a selected interface. The significant contribution to $G_c$ values from local plastic energy dissipation in the polymer and metal lines was examined and used to demonstrate the effect of patterned structure geometry on interfacial adhesion. Trends in adhesion and fracture behavior related to the patterned structures will be discussed in terms of the prevailing plastic deformation mechanisms and form the basis from which simple design rules for improved mechanical reliability may be developed.