SYMPOSIUM B
Silicon Materials—Processing, Characterization, and Reliability
April 1 – 5, 2002

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*Invited paper
TUTORIAL

B: INTEGRATED CIRCUIT FABRICATION AND YIELD CONTROL
Monday, April 1, 2002
8:00 a.m. - 12:00 p.m.
Salon 11/12 (Marriott)

This course, starting from buying the wafer up to the final interconnect structure made by Cu, Aluminum techniques, details in a
step by step fashion how a logic chip is built and what are the associated yield control/technology steps encountered during the build.
The build basics which are applicable to any state of the art chip facility will be described in such detail that the student will
understand the reason for each step, and the logic of the sequence used, as well as systematic and random defects encountered.
Additionally, a discussion of an active yield control strategy is described utilizing in-line inspection techniques and tools, use of CD,
overlay and AFM, both now and in the near future. Cross
sections, top down defect appearance, etc., at each key step will be used to illustrate the build process and the defects found.
The instructor, Professor Ernest Levine of the School of Nanoscience and Nanoengineering of the University of Albany, has spent 24 years
working in the field which will be explored in this tutorial.

Instructor: Ernest Levine, SUNY-Albany

SESSION B1: SILICON MATERIALS AND PROCESSING
Chair: Janice L. Veteran
Monday Afternoon, April 1, 2002
Salon 11/12 (Marriott)

1:15 P.M. B1.1
SUPPRESSION OF PARASITIC BJTF ACTION IN SINGLE POCKET THIN FILM DEEP SUB-MICRON SOI MOSFETS.
Najeebuddin, Antosh Kumar, Mohan V. Dungo, V. Ramapogopal Rao,
J. Vasu, Dept of Electrical Engineering, Indian Institute of Technology, Bombay, INDIA.

A study of parasitic bipolar junction transistor effects in Single Pocket (SP) thin-film SOI n-MOSFETs is carried out. Characterization and simulation results show that parasitic BJTF action is suppressed in SP-SOI MOSFETs when compared to the conventional (CON) SOI technologies. SP-SOI MOSFETs used in this study are fabricated by the standard CMOS process, except the Vth implant is done after the poly-silicon gate patterning. Pocket implant is done from the source side. Both the CON and SP-SOI MOSFETs are fabricated on the same wafer with channel lengths down to 100nm, and with different silicon film thicknesses, 35, 50 and 65 nm. The gate oxide thickness for all the MOSFETs is 3.9 nm. Gate-Induced Drain-Leakage (GIDL) current has been used for characterization of parasitic BJTF gain. GIDL current is independent of channel length and depends on the area of gate-drain overlap region and the electric field within it. At high drain biases, when impact ionization occurs, the impact ionized electrons flow toward the drain while the holes lead to charging of the body in SOI. In long channel devices these holes recombine before reaching the source, whereas in short channel devices the hole current gets amplified by the factor β (BJTF gain) depending upon the base width (channel length). This amplified current gets added to the drain current. By taking the ratio of currents in short channel to long channel device, we can estimate the value of β for the parasitic BJTF. The experimentally evaluated value of β for the parasitic BJ TF in deep sub-micron SP-SOI devices is found to be an order of magnitude lower as compared to the CON SOI technologies. The suppression of parasitic BJTF effect in SP-SOI devices is also analyzed from detailed 2D simulations and attributed to lower peak electric field near the drain junction. Further insight gained by detailed process and device simulations using a BJTF like structure with similar technology parameters as in SP-SOI. The results obtained from simulations excellently corroborate the experimental findings.

1:30 P.M. B1.2
MICROSTRUCTURAL EVOLUTION AND DEFECTS IN ULTRA-TIN SI SIMOX MATERIALS DURING ANNEALING. Jun Sk. Jeong, Rachel Evans, and Sipanjan Senghin, The University of Arizona, Department of Materials Science and Engineering, Tucson, AZ.

Ultra thin SIMOX processes are creating increased interest as a long-term solution for ULSI due to advantages: low cost, better heat dissipation, and short channel effect over standard SIMOX. Ultra thin SIMOX materials were prepared by implantation of the oxygen ions into p-type (100) 8-inch Si wafers at an implantation energy of 65 keV and 100 keV with a dose range of 2.0 - 8.0 x 10^15 O+ cm^-2 using an argon ion source. The wafers were subsequently annealed at 1100°C, 1200°C, 1300°C and 1350°C each for 0 hrs and 4 hrs in an Ar +4%SiO2 atmosphere. Microstructural evolution, oxygen redistribution and crystalline quality of the Si films of SIMOX structure after post implantation thermal annealing and high temperature annealing were characterized using a Transmission Electron Microscope (TEM), Rutherford Backscattering Spectroscopy (RBS), and Auger Electron Spectroscopy (AES). The defect microstructures and the induced high temperature annealing were investigated using XTEM and PTEM. The density distribution in the Si-rich films of ultra thick SIMOX were measured using an optical microscopy after a chemical etching. Results of the microstructural analysis shows that a dose range of 3.0 - 3.5 x 10^15 O+ cm^-2 at an implantation energy of 100 keV produces a silicon island-free continuous buried oxide layer (BOL) after 1350°C and 4 hrs annealing. The thickness of silicon overlayer and the BOL thicknesses are about 100 nm and 78 nm respectively. The effects of implantation energy and dose on defect density in a fully annealed SIMOX are discussed.

1:45 P.M. B1.3
X-RAY REFLECTIVITY STUDY OF EXOTIC MATERIALS FOR ELECTRONIC APPLICATIONS. C.H. Russell, Bede Scientific Inc., Englewood, CO.

As device size decreases, new challenges arise regarding shrinking dimensions, creating the need for thin, high k dielectric materials, low k copper interconnects and other exotic materials. This in turn creates both physical and chemical interface issues, which cannot be solved with traditional metrology tools. Critical physical parameters such as density, interface roughness and thickness of a layer can be resolved with x-ray reflectivity. The quickest and a very reliable method of study regarding these materials is to base work on simulations using a very robust fitting program. This work incorporates a largely theo retical study of exotic materials of interest, including SiON, low k (silicon based films) and high k dielectrics (ThOx, ZrO2, HfO2, SrTiO3), with a few selected experimental results.

2:00 P.M. B1.4
ABSORPTION SPECTROSCOPY ON COPPER TRACE IMPURITIES ON SILICON WAFERS. Andy Singh, Katharina Bau, Sean Brennan, Piero Pimentel, Stanford Synchrotron Radiation Laboratory, Stanford, CA; Takayuki Homma, Waseda University, Tokyo, JAPAN.

Trace metal contamination during wet cleaning processes on silicon wafer surfaces is a detrimental effect that impairs device performance and yield. Currently, total reflection x-ray fluorescence (TXRF) using synchrotron radiation is one of the most powerful techniques for trace impurity analysis on silicon wafer surfaces and has been used to better understand the deposition mechanism of Cu trace impurities on silicon wafers. Recent studies investigating silicon wafers immersed in copper contaminated ultra pure water solutions show a strong correlation between the deposited copper concentration and the amount of oxygen present in ultra pure water. In addition, TXRF has been combined with x-ray adsorption near edge spectroscopy (XANES) in a pre-consumed silicon samples that were dipped in UPW solutions with copper concentrations ranging from 2 to 200 ppb. Results showing the oxidation state of the deposited metal will be shown for both oxidized and deoxidized solutions. Finally, XANES experiments using a cell with a spring water delivery system to observe samples directly beneath a water layer were also conducted. Higher concentrations of copper were used in the solutions to overcome degraded sensitivities due to the presence of the water layer, but the deposition processes could be monitored without environmental interference.

2:15 P.M. B1.5
PORE SIZE DISTRIBUTIONS IN LOW-k THIN FILMS BY X-RAY REFLECTIVITY AND SMALL ANGLE NEUTRON SCATTERING. Barry J. Bauer, Hie-Young Lee, Christopher Sols, Ronald C. Hedden, Du Wei Lin, Wen-Li Wu, NIST, Gaithersburg, MD; Jeffrey A. Lee, Jeff Wietel, International Sematech, Austin, TX.

New methods have been developed to measure of pore size distributions in 1 mm films deposited on silicon wafers. X-ray reflectivity (XR) and small angle neutron scattering (SANS) have been carried out on samples surrounded by a controlled partial pressure of toluene vapor. As the vapor pressure increases, increasingly larger pores become filled with toluene liquid and XR is used to measure the amount adsorbed as a function of pressure. The Kelvin equation can be used to calculate the pore size distributions from the adsorption data. SANS is carried out in various mixtures of saturated toluene and toluene-d8 in air. The SANS signal goes through a minimum at a toluene-d8 to toluene ratio of 1:1 and at this point the wall material is matched by the toluene mixture. The wall density can

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NiSi is a promising candidate for CMOS device fabrication due to its low resistivity, low formation temperature and one-step annealing. Compared with TiSi₂, the resistivity of NiSi remains constant down to 0.1 μm, while it consumes about 20% less silicon to form a silicide film of the same thickness when compared with CoSi₂. These two major advantages are of crucial significance for silicon film formation and sub-quarter micron CMOS fabrication. Nickel silicide samples are formed from sputtered Ni films on (100) Si substrates with thickness. To be uniform and thin, and annealed between 300°C and 900°C for 30s by rapid thermal annealing. Electrical sheet resistance of thinner films start to increase at a lower temperature, indicating that thinner films are thermally less stable. Agglomeration occurs more easily. The result is confirmed by the surface roughness data from AFM micrographs. Micro-Raman spectroscopy, which is sensitive to chemical composition and structure, is applied to identify phase formation, uniformity and orientation of nickel silicide films. For thinner films, the NiSi phase forms at a lower temperature than the thicker ones. For samples of the same thickness, the NiSi films formed at higher temperatures have a higher degree of epitaxy with the Si substrate. Ion channeling experiments using Rutherford backscattering spectroscopy is also used to study the orientation of the NiSi films. The interface will be characterized by cross section TEM. And thermal stability of NiSi with different thickness will be investigated.

3:45 PM B1.9
SUPPRESSION OF NiS-TO-NiSi TRANSITION USING VERY SHORT-PERIOD TiSiN RIF SILICIDATION D. M. D. Chi, W. D. Wong, A. S. W. Weng and S. J. Chua, Institute of Materials Research and Engineering, Singapore, SINGAPORE.

Nickel monosilicide (NiSi) has been demonstrated to be a potential candidate for deep sub-0.1 μm CMOS devices because of its linewidth-independent sheet resistance and low consumption of Si. However, the thermal stability of NiSi is a major concern for back-end process due to the transition of NiSi to high-resistive NiSi₂ at an elevated temperature. In this study, we have investigated the effect of TiSiN silicidation duration on the NiSi-NiSi₂ transition during Ni-silicidation reaction of thin Ni (20 nm thick) film on (100) Si. The NiSi-NiSi₂ transition temperature was increased from 700 to >800°C with decreasing the annealing time from 300s to 1s. When the annealing temperature was fixed on 700°C, the critical time for NiSi-NiSi₂ transition was identified as 35-40s. Agglomeration of the silicide films was observed to depend on not only the film thickness but also the annealing time. The time-dependent agglomeration phenomenon can be explained in terms of the kinetics of grain growth. Agglomeration-induced dislocation nucleation was also characterized by HREM. The results of the kinetic measurements of nucleation and faceted growth of disilicide has been developed, by constructing a temperature-time transformation diagram, to elucidate the important roles of the film thickness and the RTA time in determining the NiSi-NiSi₂ transition temperature.

4:00 PM B1.10
ANALYSIS OF SILICIDE/DIFFUSION CONTACT RESISTANCE MAKING USE OF TRANSMISSION LINE STRUCTURES. Anil Alekar, Infineon Technologies, Munich, GERMANY [affiliated to IMEC]; Anne Lauwers, Richard Lindsay, Muriel de Potter, Georg Tempel and Karen Mes, IMEC, Leuven, BELGIUM.

The performance of MOS circuits depends strongly on transistor current drive. The drive current of the transistor is determined by the total device resistance, which consists of the channel resistance and the ohmic resistances associated with diffusion and the contacts. As device dimensions shrink in each new technology generation, it is expected that the contact resistance between silicide and diffusion will ultimately dominate the total device resistance. For ohmic silicide/silicon contacts the contact resistivity is determined by the barrier height and the concentration of electrically active dopants at the silicide/silicon interface. The analysis of contact resistance of a silicided junction is complicated by the fact that part of the junction is consumed during silicidation. As a result the dopant concentration at the silicide/silicon interface decreases as the silicide thickness is increased, and the sheet resistance of the remaining part of the junction increases. In this work the contact resistance of CoSi₂, NiSi and A and B junctions is investigated and the influence of implant and anneal conditions, silicide thickness and silicidation temperature on the contact resistance between silicide and diffusion is studied making use of dedicated transmission line structures. The transmission line structures consist of alternating silicided and unsilicided diffusion segments, obtained by making use of
a nucleating blocking mask. The specific contact resistivity and the sheet resistivity of the remaining diffusion under the silicide are extracted from resistance measurements on transmission line structures with segments of varying length.

4:15 PM B1.11
CHARACTERISATION OF NOVEL RELAXED Ge AND Si1-x/Gex PSEUDO BUFFER LAYERS GROWN BY CHEMICAL VAPOUR DEPOSITION. A. P. J. Myerberg, I. M. Williams, \( \text{Physical Electronics and Photonics, Physics Department, National Institute of Standards and Technology, Gaithersburg, USA.} \)

Relaxed SiGe and pure relaxed Ge pseudo substrates have attracted global interest recently. They are of great importance for providing suitable substrates for strained silicon minority carrier devices. Heterogeneous HV-LV compound-semiconductors with Si technology. We have used the strain sensitive high resolution two dimensional reciprocal space mapping (3D-RSM) tool to characterize novel high quality fully relaxed SiGe and Ge buffer layers grown on Si (100) substrates by chemical vapour deposition. Both symmetric and asymmetric reflections were used to characterize these buffer layers. The effect of the Ge layer thickness and the post-growth temperature annealing on the over all quality regarding relaxation and threading dislocation density is investigated. In addition, the advantage of growing buffer layers on low temperature grown initial Si buffer layers is also studied. The 3D-RSMs are used to extract layer tilt relaxation factors, as well as to assess the quality of the SiGe or Ge layers. All these results indicate that fully relaxed buffer layer with low threading dislocations. We have observed improved crystalline quality with increasing layer thickness up to an upper limit of 5 micrometers. On contrary to what has been supposed previously, we have found no improvement regarding the relaxation and threading dislocation density reduction by using the initial low temperature Si buffer layer. The overgrowth on these relaxed buffer layers in also monitored. These measurements were complemented by secondary ion mass spectrometry (SIMS). The SIMS results shows that at the Si/Ge interface a considerable intermixing have taken place. This intermixing was also observed in High resolution rocking curve as two full width at half of the Ge peak in consistence with the SIMS results.

4:30 PM B1.12
PREVENTION OF BUCKLING DURING SI/Ge RELAXATION ON COMPLIANT SUBSTRATES. Hui-chun Tsai, Rui Huang, Pratt University, Center for Photonics and Optoelectronic Materials, Princeton, NJ; K.D. Hobart, Naval Research Lab, Washington, DC; Zhiqiang Song, Princeton University, Center for Photonics and Optoelectronic Materials, Princeton, NJ; Sen R. Shieh, Tom Duffy, Princeton University, Dept. of Geosciences, Princeton, NJ; James C. Sturm, Princeton University, Center for Photonics and Optoelectronic Materials, Princeton, NJ.

There has been increasing interest in compliant substrates for integration of heterogeneous epitaxial materials. In our experiments, borophosphosilicate glass (BPSG) on silicon is used as a compliant substrate to relax Si and SiGe layers. A thin layer of SiGe (100) substrate and then transferred to the BPSG by a bond and etch process. Buckling of SiGe during relaxation is observed and analyzed. Here, we first develop a fundamental quantitative model and understanding of the tradeoff between the desired lateral relaxation and the undesired vertical (buckling) process, and then demonstrate an experimental method to overcome the buckling issue. Large and thin islands cause slower lateral relaxation, which in turn enhances the buckling rate. Reheating and buckling are measured by Raman spectroscopy and AFM, respectively. Experiments confirmed that thin SiGe layers buckle much faster. Furthermore, lowering the viscosity of the BPSG by a factor of five lowers the time required for both the lateral relaxation and buckling process, but the amount of buckling for a given amount of desired lateral relaxation does not change. Small island size is a critical parameter, however, with buckling amplitude on 600 nm islands of SiGe being 10 times as large as that on 4000 nm islands. To overcome buckling, small sample preparation are temporarily thicker with an epitaxial cap, or buckling can be removed by long anneals at 850°C after the initial buckling. The buckling amplitude decreases dramatically from more than 100 to 5 nm (50% of the cap thickness) for small islands and islands flatten faster at higher temperature. In addition, flattening process slows down over time, which is explained by the fact that the flattening process is driven by the residual strain in the islands. With high temperature anneal, it should be possible to make SiGe layers with zero dislocation density. This work is supported by DARPA (N66001-00-1-8557) and ARO (DAAD55-98-1-2720). K.D. Hobart, F.J. Kub, M. Freti, M. E. Tsigopoulos, C. Thompson, T. S. Kuan and C.K. Inoue, J. Electron. Mater. 29, 857 (2000).
below 1.0 nm and that a high-k replacement material for SiO₂ will be necessary. Since an EOT of less than 1.0 nm will be needed and an interface between the film and the Si substrate is needed, a new technique for scale control of the interface is critical when depositing a high-k film. Although atomic layer chemical vapor deposition (ALCVD) inherently allows for monolayer control, researchers using HCF₄ as a precursor has reported difficulty in forming high-quality films on hydrogen-terminated Si. We find that the use of H(NO₃)₄ as a precursor allows for ALCVD of H₂O₂ directly on hydrogen-terminated silicon without the need for an SiO₂ layer. H₂O₂ films were characterized using spectroscopic ellipsometry, x-ray diffraction (XRD), x-ray photoelectron spectroscopy (XPS), CV, and TDDQ measurements were made on capacitors and transistors with evaporated Pt electrodes. A single cycle deposition resulted in a uniform film covering the entire surface, demonstrating a clear advantage of H(NO₃)₄ over H₂O₂. XRD analysis indicated that as-deposited films were amorphous and uniform; film structure could be altered by a post-deposition anneal. Thin films remained amorphous at anneals below 700°C. XPS analysis indicated that films are oxygen rich, contain silicon, and that residual NO₃ and NO₂ from the precursor could be eliminated by an anneal. HNO₃ films had lower leakage than SiO₂ of similar EOT but also lower BD strength. For a ~1.5 nm H₂O₂ film, k = 100 and equivalent thickness, a 1-nm film (neglecting quantum effects) was obtained. The lower than expected dielectric constant is likely due to both the presence of an interfacial layer (such as silicate) and excess oxygen.

8:30 AM B2.3
HAFNIIUM SILICATE FORMATION BY THE UV-OZONE CVD METHOD: HAFNIIUM SILICATE FOR CMOS, P. H. E. Magid, B. M. Quevedo-Lopez, E. M. Bouzid, T. M. Wallace and Bruce Grade, Department of Materials Science, University of North Texas, Denton, TX.

As the scaling of silicon CMOS technology continues, high-k gate dielectrics are required to provide increased capacitance while reducing gate leakage current. One candidate material that is receiving considerable attention is hafnium silicate. We present results on the formation of hafnium silicate using UV-ozone oxidation of hafnium silicide. Hafnium silicide films were deposited on hydrogen termininated silicon wafers at room temperature using magnetron sputtering of HfSiON. These hafnium silicide films were subsequently oxidized to hafnium silicate by exposing the wafers to UV-ozone. We find evidence for an oxidation rate consistent with metal enhanced oxidation of silicon with yttrium and lanthanum, as seen by Parsons et al. X-ray photoelectron spectroscopy, Rutherford back-scattering spectrometry, and Fourier transform infrared spectroscopy were employed to examine the extent of oxidation. The electrical behavior of the as-deposited and annealed silicate films were determined with current-voltage (LV) and capacitance-voltage (CV) measurements. The effect of post-annealing on electrical properties using N₂, O₂, N₂O, NO, NH₃, and forming gas will also be presented. Comparison of the UV ozone oxidized hafnium silicate films will be made with those prepared reaction deposition techniques.

8:45 AM B2.4

Ruthenium-based thin films are of interest for emerging CMOS gate electrode applications owing to their low resistivity, excellent thermal and electrical stability, and suitable work function changes. Ru and RuO₂ films were deposited on SiO₂ by chemical vapor deposition (CVD) and low power plasma enhanced CVD (PECVD) in a 208-mm wafer deposition cluster tool using a metal beta-diketonate precursor [Bis [2,2'-bidentylmethylene] 2,2'-bidentylmethane] (1,3-bis-bidentyl diene) ruthenium [1]. Hydrogen and oxygen were employed as the reactive gases to deposit, respectively, Ru and RuO₂. The deposition temperature used ranged from 320⁰C to 480⁰C. The resulting film properties were analyzed using cross-sectional scanning electron microscopy (CS-SEM), four-point resistance probe, x-ray photoelectron spectroscopy (XPS), and x-ray diffraction (XRD). Both Ru and RuO₂ films exhibited a deposition rate of less than 0.5 Å/s and a deposition uniformity of less than 5% at 9.5 Å/nm. The purity of the films was reflected in the resistivity of the as-deposited films, which was found to vary from 47 to 3800 μΩ·cm, depending on processing conditions. The films were subsequently annealed in both forming gas and oxygen environments for one hour at 650°C. It was observed that the thermal CVD-deposited RuO₂ films were stable in oxidizing ambient and annealing in a reducing ambient resulted in significant film densification and reduction of the film resistivities by approximately 70% (to as low as 45 μΩ·cm). The ruthenium film deposition in high vacuum scale control of the interface is critical when depositing a high-k film. Although atomic layer chemical vapor deposition (ALCVD) inherently allows for monolayer control, researchers using HCF₄ as a precursor has reported difficulty in forming high-quality films on hydrogen-terminated Si. We find that the use of H(NO₃)₄ as a precursor allows for ALCVD of H₂O₂ directly on hydrogen-terminated silicon without the need for an SiO₂ layer. H₂O₂ films were characterized using spectroscopic ellipsometry, x-ray diffraction (XRD), x-ray photoelectron spectroscopy (XPS), CV, and TDDQ measurements were made on capacitors and transistors with evaporated Pt electrodes. A single cycle deposition resulted in a uniform film covering the entire surface, demonstrating a clear advantage of H(NO₃)₄ over H₂O₂. XRD analysis indicated that as-deposited films were amorphous and uniform; film structure could be altered by a post-deposition anneal. Thin films remained amorphous at anneals below 700°C. XPS analysis indicated that films are oxygen rich, contain silicon, and that residual NO₃ and NO₂ from the precursor could be eliminated by an anneal. HNO₃ films had lower leakage than SiO₂ of similar EOT but also lower BD strength. For a ~1.5 nm H₂O₂ film, k = 100 and equivalent thickness, a 1-nm film (neglecting quantum effects) was obtained. The lower than expected dielectric constant is likely due to both the presence of an interfacial layer (such as silicate) and excess oxygen.
The need in future devices for gates with sub-ann EOT and/or extreme low leakage implies the use of high-k dielectrics with an interfacial silicon oxide thickness as close as possible to zero because the interfacial silicon oxide thickness directly affects the overall EOT of the dielectric stack. Formation of these layers is pursued with various deposition techniques such as ALVD, MCCVD. In addition to the intrinsic properties of the high-k stack, it is essential that the interfacial layer is controlled (minimized) as good as possible. The presence of an interfacial (SiOx) layer depends on several factors, e.g., the silicon surface preparation prior to the high-k deposition, the high-k deposition process and the post-deposition air exposure, or thermal treatment. Understanding the mechanism of formation and the control of the interfacial oxide are therefore key issues for the successful implementation of high-k dielectrics in future devices.

Moreover, composition, crystallization behavior, stability upon anneal and poly-deposition are all aspects which need to be looked at very carefully in order to assess the intrinsic properties of the high-k stacks. The successful understanding of the layer deposition and growth mechanism (layer by layer growth, islanding, phase separation, oxygen diffusion, ...) relies on the ability to probe these layers very precisely. As no technique has the ability to fully characterize the layers with respect to e.g. layer thickness and composition, surface and interfacial crystallization (crystalline defective and/or SOI) of an interfacial layer, a combined effort with complementary analysis techniques is required. This paper discusses the results of such an effort as applied to the characterization of high-k layer stacks based on Zr, Al and SiAlN+silox oxides. The physical analysis is done by ellipsometry, X-ray photo-electron spectroscopy (XPS), X-ray fluorescence (XRF) and reflectivity (XRR), inductively coupled plasma optical emission spectroscopy (ICP-OES), FT-IR, time-offlight SIMS (TOF-SIMS), Rutherford backscattering (RBS) and Elastic recoil detection, low energy ion scattering (LEIS) and transmission electron microscopy (TEM). Procedures have been developed to rapidly screen growth behavior, silicon formation, phase separation, crystallization behavior.


Current constant stress (CCS) is conducted to investigate the Stress-Induced Leakage Current (SILC) effects to clarify the influence of boron penetration and nitrogen incorporation on the breakdown of sub-2.0 nm Oxide/Nitride (O/N) and oxynitride dielectrics prepared by remote plasma-enhanced (R-P) CVD process. The breakdown and degradation of MOSFET characteristics were closely related to soft breakdown (SBD) and hard breakdown (HBD) mechanisms. Analog mode gate noise and post-breakdown voltages are monitored for both gate and substrate injection in CCS up to 10k sec in order to detect D. The monitored gate voltages are gradually decreased during SBD, and a continuous increase in SILC at low gate voltages is shown between stress interval. HBD was observed to result in resistive L-V characteristics and device failure, and can be detected by a significant drop in gate voltages during CCS. Compared to SILC in the thermal oxide, the reduced SILC effect of O/N and oxynitride dielectrics is observed, which is due to the suppression of positive trap generation by nitrogen incorporation at the Si/SiO2 interface. Hard bonding of gate dielectrics due to charged traps is found to influence the SILC effect and degradation mechanisms. Furthermore, we also demonstrate the stacked O/N and oxynitride dielectrics show similar breakdown and degradation properties to the SILC/ HBD interface. The degradation and the improved Si/SiO2 interface and gate-oxidation overlap region up to 11:00 AM B2.10 SILICON NITRIDE THIN FILM DEPOSITION FOR GATE DIELECTRICS USING SINGLE-WAFER HOT-WALL RAPID THERMAL TWIN CHAMBER. Jianjun Song, Sanjiv Bhattacharya, Robert Herring, ASM-III Thermal Division, Scotts Valley, CA.

Rapid thermal processing (RTP) is an emerging technology in integrated circuit fabrication, and can be an alternative to batch furnace processing as future wafer fabrication moves to 300mm diameter size. RTP requires shorter process time and can achieve better film uniformity than the batch process. We have recently developed single-wafer furnace RTP modules for both thermal oxidation and low pressure chemical vapor deposition (LPCVD) of silicon nitride. Uniform oxide films of sub-20Å can be grown by thermal oxidation and NO nitridation. The RTCVD system also provides consistent film deposition performance for silicon nitride thin films in terms of thickness and uniformity. This paper further extends the application of the hot-wall single-wafer RTCVD system to gate dielectric applications. The system provides silicon nitride films of equivalent oxide thickness below 20Å. The film deposition process, the post-deposition anneal and the electrical characterization of the gate dielectrics will be discussed.

11:15 AM B2.11 HIGH PURITY SILICON AMIDOPRECURSORS FOR LOW TEMPERATURE CVD OF GATE DIELECTRICS. Alexander S. Borovik, Chengying Xu, Bryan C. Hendrick, Jeffrey F. Reeder and Thomas H. Baum, ATMI, Inc., Danbury, CT.

Early transition metal silicides, such as those containing zirconium and hafnium, are of great interest for use in the next generation gate dielectrics. To minimize the formation of an initial silicon oxide layer, a low temperature CVD process is required. Generally, metal amides are promising low temperature CVD precursors. However, until recently, their silicon analogues were not readily available in high purity, a fundamental requirement for electronic applications. We have developed direct synthetic methods for the production of high purity Si[2(CH3)2]4, Si[NEt3]4, HS[NEt3]2 and HS[NEt2]2 in high yield. These compounds were fully characterized by NMR, IR and MS and ICP-MS and ICP-OES. In this paper, we report the synthesis, characterization of the new precursors and their use for the low temperature CVD of metal silicides, gate dielectrics.

11:30 AM B2.12 METROLOGY STUDY OF SUB 20Å OXYNITRIDE BY CORONA-OXIDE-SILICON (COS) AND CONVENTIONAL C-V ATRACHES. Pui Yue Hung, George A. Brown, and Xufang Zhong, "International SEMATECH, Inc. Metrology Yield Management Tools, Austin, TX, "KLA-Tencor Corporation, Film and Surface Technology Division, San Jose, CA.

This work aims to develop a non-contact corona oxide-silicon (COS) measurement strategy for the monitoring of sub-20Å oxide-gate dielectric. The oxynitride used in this study is composed of two bunches of In-Situ Steam Generated oxide [SBG] oxide (20/16 A) which are exposed to Remote Plasma Nitridation (RPN) for various time durations. First, the nitrogen concentration and profile of the samples are established by SIMS and nuclear reaction analysis. Then, the COS measurement using Quanta was carried out on comparator wafer, extracting the following five electrical parameters: interface trap density (Dit), flatband voltage (Vfb), total charge, effective charge and equivalent oxide thickness (EOT). Both the pre-anneal Dit and total charge are promising parameters because of their strong correlation with the nitrogen content. However, the VB, Dit, effective charge, and EOT measurements appear to be affected by the ambient environment or the leakage characteristics of the oxynitride. In addition, the integrity of the oxynitride is verified by measuring the C-V tunneling voltage, leakage current and oxide resistivity. A comparison of the C-V/COS measurements of EOT, Vfb and current density is included; however, no simple linear relationship exists between these parameters.
has been used to investigate the re-crystallization behavior of metal silicates and alloys. A model describing the re-crystallization behavior of Ni and Zr-containing silicates has been presented in detail. This model will be used in conjunction with a photo diagram survey of metal oxide-SiO$_2$ systems to categorize potential gate dielectrics for crystallization behavior. Electrical and structural characterization of the layers will be presented. The new model will be used to optimize a dielectric and a process able to withstand temperature excursions in excess of 1000°C. In general, appropriate combinations of temperature and oxygen partial pressure can be found which minimize unreacted interface reactions, and hence minimize interfacial layer formation at high temperature exposure. Models for reactions between these materials will be presented in the context of oxygen rich and oxygen poor atmospheres. Specifically, a new model will be presented which attempts to describe the cleavage of oxides in contact with silicon. Finally, data will be shown comparing materials prepared with and without in situ deposited Ti metal gates. These results demonstrate the sensitivity of ultrathin capacitor layers to atmospheric exposure.

2:00 PM B3.2

**THERMOELECTRIC STABILITY OF HIGH-K DIELECTRICS**

Metal Oxides: ZrO$_2$ and HfO$_2$ in Contact with Si and SiO$_2$


We present theoretical and experimental results regarding the thermodynamic stability of the high-k dielectrics MO$_2$ (M = Zr and Hf) in contact with Si and SiO$_2$. The HfO$_2$/Si interface is found to be stable at room temperature with respect to formation of silicon oxides whereas the SiO$_2$/Si interface is not. The MO$_2$/SiO$_2$ interface is marginally unstable with respect to formation of silicon oxides. Cross-sectional transmission electron micrographs of epitaxial layers of SiO$_2$ on Si substrates with the poly-Si/ poly-ZrO$_2$/poly-Si interface have been presented. The HfO$_2$/Si interface is also unstable with respect to the formation of silicon dioxide. For both ZrO$_2$ and HfO$_2$, the X-ray photoemission spectra illustrate the formation of silicate-like compounds in the Mo$_2$/SiO$_2$ interface.

2:15 PM B3.3

**EFFECT OF TEMPERATURE SCALING ON MOS TRANSISTORS WITH HIGH-K DIELECTRICS**

M. Desai, V. Ramagopal Rao, Indian Institute of Technology Bombay, Department of Electrical Engineering, Mumbai, India.

High-K materials like Al$_2$O$_3$ (K 10), ZrO$_2$ (K 25) and TiO$_2$ (K 60) have received much attention recently as alternative gate dielectrics for CMOS applications. A few papers have been published recently on the effect of fringe capacitances in these high-K gate dielectric MOS transistors due to their higher physical dielectric thickness. However, no work has been done to study the effect of temperature scaling parameters on the fringe field effects. In this work, we have studied the effect of gate overlap length, spacer dielectric material and other technology parameters on the device and circuit performance of aggressively scaled CMOS transistors with high-K gate dielectrics by extensive two-dimensional device simulations. In high-K gate dielectric transistors, the ratio of physical thickness of gate oxide to that of silicon dioxide decreases as the dielectric constant increases. Thus the 3-D effects become dominant leading to shorter channel performance. For $K_{gat}$ greater than $K_{gii}$, we observe a substantial reduction in the overlap length between source-drain region due to the gate dielectric thickness rather than through silicon. Our results show that for an increase in $K_{gat}$ from 3.9 to 60, $\lambda_{gat} / \lambda_{gii}$ ratio decreases by a factor of 9 for $V_{DD}=0.5V$ and by a factor of 17 for $V_{DD}=1V$. Also, DBL increases by a factor of 2.5 when $K_{gat}$ is increased from 3.9 to 60. In future aggressively scaled MOS technologies the control of overlap region is going to be a major challenge. Since much of the coupling between source-drain occurs through the gate dielectric, it is observed that overdrive length is an important parameter for optimizing DC performance of MOS transistors. The results of a comprehensive 2-D device simulation results to prove this point. We have also studied the effect of spacer dielectric material and channel length on the performance of high-K gate dielectric MOS transistors.

3:00 PM B3.4

**Si[100] SURFACE CLEANING USING SR AND SRO.**

Yi Wei, Xinxiang Hu, D.C. Jordan, Brian Craig, Ravi Droopad, Jiminy Z. Yu, Alex Demkov, John L. Edwards Jr., WJ. Ooms, Physical Science Research Laboratory, Motorola Labs, Motorola Inc., Tempe, AZ.

A method for removing SiO$_2$ and producing an ordered Si(100) surface using Sr or SRO has been developed. In this technique, a few monolayers of Sr or SRO are deposited onto the as-received Si(100) wafer in a ultrahigh vacuum (UHV) molecular beam epitaxy (MBE) system. The substrate is then heated to ~800°C for about 5 minutes, the SRO is removed by a few nanometers behind a Sr or SRO terminated ordered Si(100) surface with a mostly (2X1) reconstruction. This Sr or SRO terminated Si[100] surface is well suited for the growth of crystalline high-k dielectric SrTiO$_3$[1]. To understand the mechanism of removing SiO$_2$ from Si(100) using Sr or SRO, we have performed programmed temperature desorption (TPD) measurements on SrO covered Si(100) substrates. The species observed coming off the surface during the temperature cycle was mainly SiO and O$_2$ to a significant amount of Sr adsorbates. We conclude that the removal of SiO$_2$ is due to the catalyzed reaction SiO$_2$ + Sr (or SRO) → [SiO (g) + O (g) + Sr (or SRO)]. The reaction SiO$_2$ + Si → 2SiO (g) at the SiO$_2$/Si interface is limited and the pit formation is suppressed. The main role of Sr or SRO is likely to promote the growth of SrTiO$_3$ films on the substrate. The Sr/Si films on SrTiO$_3$ grown by the Sr/Si films on the substrate. The Sr/Si films on SrTiO$_3$ grown by the Sr/Si films on the substrate.
observed that the ZrSi₂ formation was substantially restrained by inserting Si₃N₄ instead of SiO₂. This result means that the formation and diffusion of 2SiO at the stack is the dominant process promoting the reaction. Based on these experimental results, we think the thermal stability of the poly-Si/ZrON/ZeSiON/Si stack is mainly due to the nitrogen incorporation into the ZeSiON interfacial layer, in which Si-O-Crystallites is as its diffuse as effectively supported.[1] M. Koyama et al., to be published in EIDM001. [5] T.S. Jeon, J.M. White and D.L. Kwong, Appl. Phys. Lett. vol. 78, 2001, p. 368.

3:45 PM B3.7 STRUCTURE AND STABILITY OF ALTERNATIVE HIGH-k DIELECTRIC LAYERS ON SILICON: S. Stemmer, Z. Chen, Rice University, Houston, TX, J. Nie, R. Asherfield, G.N. Petersen, D. Wicksman, J.-P. Merin, A.I. Kingon, North Carolina State Univ, Raleigh, NC.

We use electron energy-loss spectroscopy (EELS) in scanning transmission electron microscopy with a sub-0.2 nm probe and atomic resolution transmission electron microscopy to investigate the structure and stability of Y₂O₃ grown by remote plasma chemical vapor deposition (CVD) and of ZrO₂ layers grown by reactive evaporation in a molecular beam epitaxy system (MBE). We investigated CVD Y₂O₃ films as a function of film thickness and pre-treatment of the silicon surfaces after deposition anneals. We show that thin films on clean silicon form a silicon film with a thin interfacial oxide, whereas a nitrogen plasma pre-treated Si surfaces reduces the amount of silicon wafer from the interface and Y₂O₃ is found as the topmost layer in a similar thickness (7 nm). We also show that the amount of silicon in the films determines the cristallization behavior in post-deposition anneals at 900°C and the formation of a thin interfacial oxide is difficult to avoid under anodic, non-capped annealing conditions. MBE-ZrO₂/Si structures were investigated before and after rapid thermal annealing (RTA) treatments at 1000°C under different oxygen partial pressures. We identified a critical partial pressure of approximately 10⁻² torr that can preserve a thin (1 nm) interfacial silicon oxide layer for high equivalent oxide thicknesses. At higher oxygen partial pressures (about 10⁻¹ torr) the interfacial oxide thickness increases through oxygen diffusion through the ZrO₂ layer and silicon consumption at the interface. At lower oxygen partial pressures (about 10⁻² torr), silicon formation at the interface is observed. ZrO₂ films remained the optimal partial pressure for a thin interfacial oxide were found to crystalize and contain no silicon, whereas silicon diffusion and partial amorphization takes place at higher partial pressures. The results show the relationship between crystallization and silicon diffusion as a function of annealing atmosphere, and also show that oxide crystallization is important in determining the overall phase formation behavior. We will also discuss the application of EELS fine-structure analysis to provide an additional measure of interface composition in these very thin layers.

4:00 PM B3.8 ATOMIC LAYER DEPOSITION OF ZIRCONIUM DIOXIDE THIN FILMS USING NEW ALKOXYDE PRECursors. T.J. Leeddar, A.C. Jones, P.A. Williams, H.O. Davis, Inotech Ltd, Miltonkey, UNITED KINGDOM; M. Riesb, R. Mestre, M. Leshak, Department of Chemistry, University of Helsinki, FINLAND.

Zirconium dioxide has a high permittivity and is stable in contact with silicon, making it a prime candidate as the gate dielectric in next generation metal-oxide-semiconductor devices. Atomic layer deposition (ALD) allows the deposition of conformal films at low substrate temperatures with control of layer thickness to the monolayer level. Zirconium tetra-chloride and zirconium tetraiodide have been used as precursors but halide contamination is a potential problem. Zr alkoxides may offer process advantages and Zr tetrathox-butoxide has been investigated for the ALD of zirconium dioxide. However this mononuclear precursor contains a four coordinate ununsaturated ZrIV centre making it more sensitive to oxygen and volatile decomposition during storage and use. The use of donor functionalised alkoxide linkers containing more than one oxygen or nitrogen donor group (e.g. dimethylaminoethoxide) leads to more fully saturated and less reactive Zralkoxide complexes. Here we report the ALD of zirconium dioxide using a number of donor functionalised alkoxide precursors. Results are compared to conventional sources and the implications are discussed for the future design of ZrO₂ ALD precursors.

SESSION B4: POSTER SESSION
DIELECTRIC CHARACTERIZATION
Tuesday Evening, April 2, 2002
8:00 PM Salon 1-7 (Merriott)
properties of ALD-grown ZrO2 and HfO2 using C-V, I-V, and HP-LISS. The microstructure and leakage current properties of ZrO2 and HfO2 will be presented before and after thermal annealing. In addition, electrical and material properties as a function of thickness will be discussed. As a possible candidate for high-k gate dielectric applications, data on ZrO2-HfO2 nanocomposite structures will be also presented.

B4.4
MÉTHODOLOGIE Modeling OF BORON DIFFUSION IN POLY-CRYSTALLINE SiO2 FILMS
Chun-Lang Li, Advanced Process Development and External Research Labs., Motorola, Inc., Mesa, AZ.
We present ab-initio modeling results including formation, migration, and activation energies for B diffusion through bulk and grain boundaries in polycrystalline SiO2 films. Modeling results clearly indicate that B can penetrate through a 40 Å SiO2 film via grain boundary diffusion, but not by bulk diffusion. SIMS analysis of B concentration versus distance of polycrystalline SiO2 relaxed and different anneals showed double B peaks at the interfaces and thus confirmed the modeling prediction.

B4.5
ENHANCED OXYGEN INCORPORATION IN HIGH k DIELECTRIC MATERIALS DEPOSITED BY AN ULTRAVIOLET-ASSISTED GROWTH TECHNIQUE
As the search for an alternative gate dielectric for the currently used SiO2 continues, numerous high-k materials have been investigated as possible candidates. Among them, zirconium dioxide, hafnium dioxide and barium strontium titanate have shown great promise. In a comparative study, nanometer thick samples were grown by both conventional pulsed laser deposition (PLD) and by an ultraviolet-assisted pulsed laser deposition (UVPLD) technique. In the UVPLD technique, lower energy KrF laser beams were added to the PLD chamber. With the addition of the 193 nm UV radiation sources, molecular oxygen is broken down into highly reactive oxygen and atomic oxygen which can incorporate more readily into the growing films. The effects of this enhanced oxygenation process resulted in higher crystalline quality, more stoichiometric films due to lower oxygen vacancies. A variety of characterization techniques were used to investigate the effects of the ultraviolet radiation. The structural properties were analyzed by transmission electron microscopy, x-ray diffraction, and x-ray reflectivity. Chemical analysis was performed via x-ray photoelectron spectroscopy and Fourier transform infrared spectroscopy. Finally, electrical characterization in the form of capacitance-voltage and current-voltage measurements was performed. In each of the cases, samples grown with and without UV illumination were compared and the oxygen content was analyzed. The main benefit of this UV-assisted process is the ability to grow higher quality films, or otherwise equivalent films but at lower processing temperatures.

B4.6
PROPERTIES OF HAFNIUM OXIDE UPON DEPOSITION
Method.
Suheun Nam, Seok Woon Nam, Jong Ho You, Dae Hong Ko, Dept of Ceramic Engineering, Yonsei Univ., Seoul, KOREA; Ja Hum Ku, Sjooyng Choi, Samsung Electronics Co., Ltd., KOREA.
The SiO2 dielectrics have been a subject of intensive studies for several decades. According to the past trends in mass production, however, reliability problems were considered to limit the physical thickness of gate SiO2. Therefore, extensive research is underway to meet the challenge of moving beyond the SiO2 era, that is, to replace the conventional SiO2 with high-k gate dielectrics. The advantages of HfO2 over SiO2 are greater densification which makes it more effective barrier to migrating impurities - its high dielectric constant, and high band gap of 5.66 eV with favorable band alignment with silicon. We studied and optimized the characteristics of hafnium oxides deposited by different kinds of methods. Generally, reactive sputtering method is used to deposit the oxide thin films. However, there exists substantial interlayer between oxide and silicon, causing serious degradation to fully achieve the potential of high permittivity. In order to testify these problems, we examined the films using simple reactive sputtering method and compared with the other films deposited by the modified sputtering method. During hafnium sputtering, O2 flow was modulated to control the interface quality and to suppress the additional growth of the interfacial layer. If hafnium metal existed before going through the reactive sputtering step, it acts as an oxygen barrier; thus interlayer, which is thought to be SiO2, reduced down to ~5Å. Electrical properties of hafnium oxides evaluated using capacitance-voltage (C-V) and current-voltage (I-V) measurements. It showed improved C-V characteristics, indicating low level of interfacial trap charge. The equivalent oxide thickness was calculated to be ~1.6 Å using modified reactive sputtering method. Besides, leakage current level was quite low comparing to SiO2 with same physical thickness, accounting for the superiorities of hafnium oxide as a gate dielectric.

B4.7
A comprehensive review of the main experimental features of the B and Ge segregation onto Si substrate during growing a fully strained SiGe layers is carried out. The main feature of the segregation process is that surface B and Ge clustering is observed. The simplest models are the model of B or a couple of the model of Ge on the surface sites and along 1D chains or 2D areas are also seen with some sort of symmetry. This can be explained since the surface diffusion of B and Ge is enough for collision of atoms and clustering during a layer growth. The [281] reconstructed region is considered to be situation like a dislocation with precursors for such a clustering on the H-passivated surface. These observations are strongly against the assumption that B and Ge are randomly incorporated into a strained layer rather suggesting a strong correlation of B and Ge distribution. Another observation is that surface Ge atoms are considered to be responsible for the surface B segregation process. A set of original experiments is carried out showing that at certain conditions B is taking initiative and determine the Ge surface segregation process. Basic assumptions are suggested to self-consistently explain these original experimental features and what is observed in the literature. These results have a strong impact for modeling of the B diffusion in SiGe where the initial conditions should be formulated accounting for the correlation in B and Ge distribution. A new assumption for the initial condition to be "all B atoms are captured by Ge" is regarded as a right one implying that there is no any transient diffusion controlled by the B capturing kinetics.

B4.8
IMPROVEMENT OF GATE DIELECTRIC QUALITY OF MnSi CAPACITOR BY HYDROGEN ETCHING ON ULTRA THIN GATE DIELECTRICS
Silicon nitride being considered as a promising candidate to replace thermal gate oxide dielectric, as the latter is reaching its scaling limit due to excessive increases in the gate tunneling leakage current. A novel technique called, the Hot Wire Chemical Vapor Deposition (HW-CVD), had shown promise to synthesize gate quality silicon nitride films at 250°C while maintaining their primary advantage of higher dielectric constant. The deposition was carried out for one minute. However, it was found that the fixed charges and the interface states were of the order of 5e12. To improve the gate quality of the device due to the increase in fixed charges and interface states, hydrogen etching is carried out. This is carried for 1 min at a hydrogen flow rate of 5 sccm with 250 °C as substrate temperature. Our exhaustive characterization shows the reduction in fixed charges and the interface states to about 1e12. This could be due to unbounded silicon atoms getting passivated by hydrogen atoms.

B4.9
THE CHARACTERISTICS OF SILICON NITRIDE THIN FILM BY ALD/MCLEAYER DEPOSITION
Recently, atomic layer deposition (ALD) attracts much interest in silicon integrated circuit processing owing to its accurate thickness control, conformal coverage, high film quality, and low temperature. Silicon nitride films have been widely used as the interlayer dielectrics (ILD), and are deposited by conventional low-pressure chemical vapor deposition (LPCVD) in the front-end processing or by plasma-enhanced chemical vapor deposition (PECVD) in back-end processing. However, high process temperature of LPCVD and poor film quality of PECVD are being expected to limit the performance and the reliability of the state-of-art IC in the near future. In the present paper, the silicon nitride films were deposited by ALD, and effects of process parameters on the film properties were examined. Silicon tetrachloride (SiCl4) and dichlorodimethylsilane (DCS) were compared as the silicon source gas. Ammonia (NH3) was used as the nitrogen source gas, and nitrogen was used as the purge gas between the pulse of SiCl4 and NH3. Using silicon tetrachloride as the
precursor, silicon nitride thin films were deposited controlling process parameters, such as chamber pressure, temperature, the time and number of the precursors, and the properties of deposited films were characterized by various techniques. Based upon the leakage current data, we optimized the ALD process parameters for the silicon nitride deposition.

B4.10
ARGON ANNEALING-BASED IMPROVEMENTS OF THE PROPERTIES OF ULTRATHIN OXYNITRIDE POST-NITRIDED WITH Si(P,As,N)
Christopher T. Kozicki, University of Illinois at Chicago, Department of Chemical Engineering, Chicago, IL.

Thermally grown Si3N4 films in NH3 are known to have a higher dielectric constant and a higher N concentration than silicon oxides/oxydrides, but they incorporate hydrogen atoms that induce hot electron carriers during subsequent high temperature processing. Further, silicon nitride is difficult to grow over 6 nm thick, due to self-limiting growth. An alternative is SiO2 and Si3N4O2 films post-nitrided with NH3.

In this work, we study the improvement of the properties of Ar annealed nitrided oxydrides as a function of annealing temperature and duration. Secondary ion mass spectroscopy (SIMS) study of the nitrogen profile suggests that there is increased nitrogen removal with increasing annealing time and temperature. Electrical characterizations have been performed to find out the total charge density (q/cm2) and interface trap density (Dit/cm2) at different processing conditions before and after the annealing step. A post annealing step is found to remove unwanted hydrogen atoms and improve electrical properties but at the expense of nitrogen removal. An optimization of the annealing parameters is, therefore, essential in designing nanodielectrics with desired nitrogen amount and concentration profiles and in understanding related process-structure-function relationships.

B4.11
LOW TEMPERATURE METAL ORGANIC CHEMICAL VAPOR DEPOSITION OF Al2O3 FOR ADVANCED CMOS GATE DIELECTRICS: APPLICATIONS TO HIGH-K DIELECTRICS, Skordar, Skordas, Zohin Patel, Filippos Pappasinos, Steve Consiglio, Gerry Nienas, and Eric Eisenbaum, The University at Albany Institute for Materials (UAIM), Albany, NY.

A low-temperature, metal organic chemical vapor deposition (MOCVD) process for the growth of aluminum oxide (Al2O3) as a potential alternative gate dielectric layer has been developed on 300-mm Si wafers. Amorphous Al2O3 films were deposited on (100) oriented p-type silicon [Si] samples employing an aluminum-diketontetra metal organic precursor [aluminum(III)] 2,4-pentanedionate] and water (H2O) as the aluminum and oxygen sources, respectively. A design-of-experiment (DOE) approach was employed for process optimization. The chemical, microstructural, electrical, and thermal stability properties of the resulting Al2O3 films grown over a temperature range of 250-450°C via this route were studied by x-ray photoelectron spectroscopy (XPS), X-ray diffraction (XRD), Rutherford backscattering spectrometry (RBS), nuclear reaction analysis (NRA) for hydrogen profiling, scanning electron microscopy (SEM), transmission electron microscopy (TEM), atomic force microscopy (AFM), capacitance-voltage (C-V) and current-voltage (I-V) measurements. An optimized processing window was defined for the growth of dense, amorphous ultrathin Al2O3 films with carbon incorporation as low as 1 atomic % and hydrogen incorporation as low as 0.3 atomic %. The as-deposited films possess typical electric constant values of 7-10. Post-deposition annealing studies indicate that the films chemical and structural properties are stable to temperature of at least 600°C. Thickness control was demonstrated for films as thin as 1.5 nm. Various post-deposition annealing methods were employed in order to improve the electrical properties of ultrathin films. The resulting dielectric constant was as high as 10 and the leakage current behavior was comparable to that of silicon dioxide films of equivalent electrical thickness.

B4.12
TESTING THE MATERIAL AND ELECTRICAL CHARACTERISTICS OF ZrO2 FILM OBTAINED BY PLASMA ENHANCED CHEMICAL VAPOR DEPOSITION. Hyung-Guk Cho, Jieun-Won Kang, and Jane P. Chang, University of California at Los Angeles, Dept. of Chemical Engineering, Los Angeles, CA.

ZrO2 was investigated as a dielectric to replace SiO2 for dynamic random memory (DRAM) capacitor. ZrO2 films were deposited on p-on-Si [100] Wafers by plasma enhanced chemical vapor deposition (PECVD) amid-bicarbonate [Zr(OH)4][H+] as an organometallic precursor. Ar was used as a carrier gas. The precursor vapor, and O2 as the oxidant. We used optical emission spectroscopy (OES), line width, and quadripole mass spectrometry (QMS) to characterize the gas phase reactions. Using QMS, we identified all oxidation states of Zr and found that the compositional

abundance shifted from Zr metal and monooxide to Zr dioxide and trioxide with the increase in O2/Ar flow rate ratio (O2/Ar). Atomic force microscopy (AFM) results indicate that the ZrO2 surfaces are smooth with rms 1.4 Å as long as O2/Ar was set to over one. X-ray diffraction showed that the films were amorphous. X-ray photoelectron spectroscopy (XPS) and secondary ion mass spectrometry indicated that the X-ray photoelectron spectroscopy of carbon incorporation depending on the electron temperature and the O2/Ar. We obtained a linear dependence of the carbon content determined by XPS upon the O2/Ar concentration ratio. The X-ray photoelectron spectroscopy data indicated that the carbon atoms near the SiO2/ZrO2 interface were not detected by XPS, which indicated more separation. EDS analysis produced thin films with measured properties. We observed that the leakage current density decreased drastically with increasing O2/Ar ZrO2 film at O2/Ar=4 showed 3.6x10^-7 A/cm² at equivalent oxide thickness of 25 Å.

B4.13
ZrO2 GATE DIELECTRICS PREPARED BY ATOMIC LAYER DEPOSITION. Junsun Park, Bongsik Choi, Nobhcon Park and Jooyang Kim, Dep. of Materials Engineering, Kookmin University, Seoul, KOREA.

According to 1999 ITRS roadmap, ultra thin gate oxide with EOT of less than 12Å are needed for beyond 0.1mm CMOS technology. Unfortunately, SiO2 as a gate dielectric has been facing the scaling limitation due to its direct tunneling currents and reliability problems. Therefore, alternative gate dielectric materials have been extensively investigated such as TiO2, Ta2O5 and ZrO2 because of their high dielectric constants. While TiO2 and Ta2O5 have lower barrier heights and they thermodynamically unstable directly on Si during dopant activation annealing, ZrO2 exhibits good thermal stability and high dielectric constant (about 20). In this study, atomic layer deposition of ZrO2 thin film was deposited in order to improve the scalability of the film. The ZrO2 films deposited on p-type [100] Si wafer were annealed in various ambient, top electrodes were deposited using DC sputtering and a patterned device size is 2 x 10^-6 cm² and then the microstructures of ZrO2 and interface were investigated by ellipsometry, XRD, AFM, RBS. Also, the electrical properties were measured by C-V and I-V measurements of Metal-Oxide-Semiconductor (MOS) capacitor structure of Pt/ZrO2/[100] silicon.

B4.14
ENHANCED THERMAL STABILITY OF NiSi FILMS ON 20kV BE+ IMPLANTED [100] Si. S.A. Smith, B. L. Echols, D. E. Chui, M. E. Loomans, D. H. W. Tijou and S. J. Chu, Institute of Materials Research and Engineering, SINGAPORE.

The thermal stability of NiSi films formed on 20 kV BF+ implanted [100] Si has been investigated. Phosphorus-doped [100] Si wafers with a resistivity of 1-10 Ω cm were used in this study. 20 kV BF+ implantation was performed at an implant dose of 5 x 10^11/cm² and 5 x 10^12/cm² Some of the wafers implanted at a dose of 5 x 10^11/cm² underwent rapid thermal annealing (RTA) at 850°C for 60 s in order to regrow the surface amorphous layer (<40 nm thick) and activate the dopants. 300-nm-thick Ni films were deposited on all samples, including control samples [Si wafers implanted at 5 x 10^11/cm² without implantation], by standard vacuum deposition. After standard RCA cleaning and dilute HF dipping, the samples were then subjected to 60 s RTA at 850-950°C for silicidation. X-ray diffraction (XRD), scanning electron microscopy (SEM), transmission electron microscopy (TEM) and secondary ion mass spectrometry (SIMS) were employed in the analysis of the silicide films. Significant enhancement of NiSi thermal stability by the presence of fluorine in NiSi was observed. The direct NiSi atomic density increases to >75% at 950°C when NiSi forms on (100) Si implanted with 20 kV BF+ at an implant dose of 5 x 10^11/cm². The NiSi films formed on BF+ implanted Si also exhibit much improved morphological stability. The observed enhancement of NiSi thermal stability is attributed to the retardation of grain growth, production of columnar growth with the introduction of NiSi grain boundaries and NiSi/Si interface. The retardation in the grain growth improves the morphological stability of NiSi films and the improvement in the morphological stability, in turn, suppresses the formation of intermetallic NiSi2 by reducing the number of the favourable sites for NiSi2 nucleation.
D4.15 COMPOSITE X-RAY WAVEGUIDE-RESONATOR AS A BACKGROUND FOR THE NEW GENERATION OF MATERIAL TESTING EQUIPMENT FOR FILMS ON SI SUBSTRATES. Vladimir K. Egorov, Evgeniy V. Egorov, IMST RAS, Chernogolovka, Moscow Dist., RUSSIA.

Planar X-ray waveguide-resonator (PXWR) functioned on total X-ray reflection phenomenon is formed by two plane parallel polished dielectric strips. A variation of the dielectric constant is divided into two inhomogenous strips separated by distance $\Delta L < L$ allows to decrease divergence of emerging beam. The angle between contraction of PXWR beam without filling of its internal intensity is connected with abrupt decreasing of capture angle for second PXWR inlet of the composite waveguide. There are discussed examples of PXWR practical applications for diffractometry of polycrystal and epitaxial film structures on Si substrates, TRIF spectrometry and X-ray reflectometry of the thin film materials.

D4.16 EFFECT OF POLY SILICON ANNEAL ON GATE OXIDE CHARGING DAMAGE IN POLY SILICON GATE PATTERNING PROCESS. Daniel Chong, Won Jong Yoo, National University of Singapore, Dept of Electrical and Computer Engineering, SINGAPORE, Lip Chin, Alex See, Chartered Semiconductor Manufacturing Ltd, Technology Development, SINGAPORE.

Poly silicon film anneal is performed prior to poly silicon gate etch in certain process flows to activate part of the implanted dopants inside the poly silicon gate oxide film. This film is the first part of a two-step annealing/activation process for the poly silicon gate oxide film. The second part of this two-step annealing process is performed during the source and drain junctions anneal. The reason for having a two-step poly silicon gate oxide annealing process is such that the thermal budget required to activate the source and drain junctions can be relaxed without affecting the resistivity of the poly silicon gate oxide. Thermal budget for source and drain junctions annealing is kept low to obtain shallow junction devices. The 0.15 μm technology process flow. Transistors in the test structures are n-channel devices with gate oxide thickness of 20Å. The dimension of the gate oxide is 0.15 μm x 10 μm. The thickness of the poly silicon is 2000Å and the implanted phosphorus dose is 5.5x10¹⁰ cm⁻². An experimental split is performed at the poly silicon film anneal step. One set of wafers undergoes this step while another set skips it. Poly silicon film anneal is carried out in N₂ ambient at 800°C for a 15 minutes time duration. Our study shows that this two-step poly silicon gate electrode annealing process does have some effect on gate oxide charging damage. Gate oxide charging damage is increased with the inclusion of the poly silicon film anneal step prior to gate patterning.

D4.17 ELECTRICAL CHARACTERISTICS OF SILICON IMPLANTED NANOCRYSTAL MEMORY IN SILICON NITRIDE SILICON DIOXIDE STRUCTURES. T.S. Kulkar, Department of Electrical and Computer Engineering, University of Colorado, Colorado Springs, CO; Nathaniel M. Pendergast, Amel Corporation, Colorado Springs, CO.

Recently, metal-oxide semiconductor memory structure field effect transistors based on silicon implanted nanocrystals are attracting the attention of many researchers. The use of nanocrystals provides a new avenue for incorporating volatile memories. In this paper we are presenting the results of non-volatile memory characteristic of heavy dose silicon implanted (1e16 cm⁻²) silicon nitride-silicon dioxide structures. Poly silicon-oxide-silicon dioxide structures were fabricated with silicon implanted nano-crystals have been fabricated and were characterized by capacitance-voltage and current-voltage measurements. These structures show hysteresis in their capacitance vs voltage characteristics which might be due to charge trapping at the silicon nano-crystal-silicon dioxide interface.

D4.18 DEGRADATION STUDY OF ULTRA-THIN JVD SILICON NITRIDE MNSFETS. K.N. ManjulaRani, V. Ramgopal Rao and J. Vani, Department of Electrical Engg, Indian Institute of Technology, Mumbai, INDIA.

Jet Vapour Deposited (JVD) silicon nitride has emerged as a viable alternative to SiO₂. It has been shown that JVD silicon nitride has excellent hot-currer capabilities. In this paper, we report the degradation due to current limited constant voltage stressing in JVD Metal-Nitride-Semiconductor FETs (MNSFETS). The devices used in this study are n-channel MNSFETS with an Equivlent Oxidation Thickness (EOT) of 3.8 nm. The devices were fabricated in UCLA with the JVD deposition done at Yale University. Non shorts or slow transistors seem to play an important role in silicon nitride MNSFETS. We have developed a simple but accurate method of characterizing border transistors using hysteresis in drain current of MNSFETS. This method can be used to characterize transistors in smaller chip geometries also. We will compare these results with those obtained by variable frequency charge pumping method. In addition to the border transistors, the effect of stressing on $V_{th}$, $R_{on}$, $N_{L}$ are also reported. In ultrathin MNSFETS, the effect of Stress Induced Leakage Current (SILC) and Soft Breakdown (SB) also become very important. SILC causes increase in leakage currents at low fields and is especially important for JVD MNSFETS in memory applications. We have observed that the JVD MNSFETS show very little increase in SILC after stressing. Next we look at Soft Breakdown characteristics of JVD MNSFETS. Noise in the gate current (observed in the Ig-Vg characteristics) is the most widely used method to characterize SBH. In addition to this, we have also used gate current transients before and after stress at sufficiently low voltages to detect SBH. We have observed Random Telegraph-Noise (RTN) like behaviour after soft-breakdown. In ultrathin SI₂O₃ MNSFETS, it is observed that although soft-breakdown increases the noise in currents, it does not effect the device performance. We have also observed that there is hardly any effect of SBH on the device performance of JVD MNSFETS.

D4.19 EFFECTIVE DIELECTRIC THICKNESS SCALING FOR ULTRA-SHORT GATE LENGTH MOSFETS. Krishna K. Bhandarkar, Nikhil C. Mohapatra, Dept of Electrical Engineering, Indian Institute of Technology, Bombay, INDIA; Siv G. Narendra, Microprocessor Research Lab, Intel Corporation, Hillsboro, OR; V. Ramgopal Rao, Dept of Electrical Engineering, Indian Institute of Technology, Bombay, INDIA.

The use of high-$K$ materials as gate dielectric has received considerable attention for CMOS scaling. For successful integration into the mainstream technology, the short channel performance of MOS transistors with high-$K$ gate dielectrics must be compared with the conventional SiO₂ at identical oxide thickness. It has been shown recently that the short channel performance worsens for High-$K$ dielectric MNSFETS as the physical thickness to the channel length ratio increases, even when the effective oxide thickness is kept identical to SiO₂. In this work, we have systematically evaluated using 2D simulations the effective dielectric thickness for different $K_{eff}$, to achieve the targeted threshold voltage ($V_{th}$), drain-induced barrier lowering (DBL) and $I_{off}/I_{on}$ ratio for different technology generations down to 50 nm, following the ITRS roadmap specifications. Our results clearly show that high-$K$ and SiO₂ follow different trends and the fringing field effects taken into account for estimation of effective oxide thickness when $SiO₂$ is replaced by a high-$K$ dielectric. For example, with a $T_{ox}$ (effective) of 1.5 nm for the 70nm technology node, $V_{th}$ decreases by about 5%, DBL increases by 38%, and $I_{off}/I_{on}$ decreases by almost a factor of 2 if SiO₂ is replaced by a high-$K$ dielectric of dielectric constant 30. This degradation becomes even more significant for sub 50 nm technologies. This paper summarizes the capacitance scaling trends for high-$K$ dielectrics with the help of systematic 2D simulations for channel lengths down to 50 nm, and with gate dielectric constant varied over a wide range, keeping in mind the high-$K$ dielectrics currently being investigated by various research groups.

D4.20 CHARACTERIZATION FOR HIGH K AND POROUS LOW K THIN FILMS BY GRAINING INCIDENT X-RAY SCATTERING. K. Oreste, A. Takase, and Y. Hto, X-Ray Research Laboratory, Rigaku Corporation, Tokyo, JAPAN.

Atomic scale structure of thin high-$K$ gate dielectrics is essential to the properties of films. It is believed that amorphous structure is suited for the gate dielectrics. Although x-ray scattering technique is useful to characterize such a structure, it is hard to measure the diffraction peaks of ultra thin film with thickness below 10 nm by conventional 0-2θ method. Grazing incident in-plane diffraction has high surface sensitivity and able to detect film peaks even though the thickness is less than 1 nm. By using in-situ geometry, we have successfully obtained the ZeO₂ diffusion down to 1 nm film thickness and detected the structural change by thermal annealing. In addition, we have also analyzed film stacked and interfacial structure of the ZeO₂ film by grazing incidence high angle grazing incidence measurement (XHR). Combination of these two techniques, we could determine precise structure of ultra thin high-$K$ dielectric films. We
will also present the method for determining pore-size distribution in porous low-dielectric films by grazing incidence x-ray scattering. The technique is related to small-angle x-ray scattering (SAXS) and small-angle neutron scattering (SANS) in that it involves the scattering of the incident beam by the sample. The current x-ray scattering technique agrees with that of the commonly used gas adsorption technique. The x-ray technique has successfully determined small pores down to sub-micron in diameter, which is well below the lowest limit of the gas adsorption technique.

D4.21 KINETICS OF INTERFACIAL FORMATION DURING POSTANNEALING OF PULSED LASER DEPOSITED HIGH-DIELECTRIC ELEcTRONICS ON Silicon, C. Essary, N. Bassim, V. Craciun, and R.K. Singh, Univ of Florida, Gainesville, FL.

Current silicon transistor technologies are nearing the physical limits of miniaturization using SiO₂ as the gate dielectric, therefore alternate high-k dielectric materials are desired. Pulsed laser deposition (PLD) is an important tool for formation of thin films of different potential alternate high-k dielectric layers on silicon wafers. However, during deposition and annealing of ZrO₂ and Y₂O₃ films by PLD, an interfacial layer formation process was noted. This layer has detrimental effects on the electrical capacitance properties of the film. This presentation explores the kinetics of the formation of this interfacial layer and ways to impede its formation. Samples of both ZrO₂ and Y₂O₃ films were deposited using a pulsed-laser deposition technique and were post-annealed in various atmospheres, at different temperatures, and with increasing times. Using several characterization techniques, the thickness, uniformity, and bonding environment of the interfacial layer were determined. The results were used to model the kinetics of the formation of the interfacial layer. Comparisons were made of samples deposited on top of a thin nitride layer formed by heating in a nitrogen environment to study the nitride effectiveness in slowing the interfacial layer growth.

D4.22 RECENT PLASMA-ENHANCED CHEMICAL VAPOR DEPOSITION OF SILICON NITRIDE AT ATMOSPHERIC PRESSURE. Greg Nowling, Steve Babayan, Vladan Jankovic, and Robert Hicks, University of California, Los Angeles, Dept of Chemical Engineering, Los Angeles, CA.

Silicon nitride is widely used in silicon microelectronics for barrier layers, packaging, isolation, and novel dielectric structures. We have deposited high-quality silicon nitride films using a novel atmospheric-pressure plasma source. This source is operated without vacuum chambers and associated hardware, and represents a low-cost alternative to the equipment currently used for semiconductor processing. The atmospheric-pressure discharge was produced by flowing nitrogen and helium through two perforated metal electrodes that were driven by 13.65 MHz radio frequency power deposition. He was mixed with the plasma effluent and from outside the reactor and directed the flow onto a rotating silicon wafer heated to between 1000 and 5000 degrees C. Films with thicknesses ranging from 1 to 1000 angstroms were grown at deposition rates ranging from 1 to 1000 angstroms per minute. A nitrogen/Alumina feed ratio of 43:100 was used to obtain a silicon nitride/deposition product of less than 1%. The crystallographic orientation was determined using x-ray diffraction. Crystallographic orientations of the films were determined to be <100> or <110> orientation. These results were obtained by the diffraction of the x-ray source from the plasma. The x-ray source provided emission spectrum of the afterglow suggests that gas-phase reactions between nitrogen molecules and the plasma play an important role in this process. At the meeting, we will further discuss the properties of the films, and their potential application in Si-devices.


In this abstract we present the first results of H₂O films formed by thermal and UV assisted injection liquid source, chemical vapor deposition. Using a liquid injection system H₂O films have been formed using metal organic deposits, metal alkoxides (H₂C₂H₇O₂Ar) precursor in a hexane solvent. H₂O films with thicknesses ranging from 20-100 nm were formed over a range of temperatures (320-550°C) and deposition environments (O₂, Ar, Ar-O₂, Ar-H₂). H₂O films have also been formed (20 nm) using UV excimer lamp (222 nm) assisted, injection liquid source, CVD. For the initial studies relatively thick films (20-100 nm) were deliberately chosen to minimize interface effect and allow analysis of the bulk film composition. In both cases the substrates were Si(100), with approximately 1 nm chemical oxide present prior to deposition. Metal alkoxide (H₂C₂H₇O₂Ar) showed high reactivity towards O₂, and metal alkoxide (H₂C₂H₇O₂Ar) showed high reactivity towards H₂O.

D4.24 ELECTROLUMINESCENCE PROPERTIES OF INDUMINTOXIDE/EMBEDDED SI NANOCRYSTALITES IN SiO₂ / P TYPE Si/METAL STRUCTURE PREPARED BY PULSED LASER DEPOSITION. Jong Hoon Kim, Kyung Ah Jeon, Jin Buck Choi, Sung Yeol Lee, Department of Electrical and Electronic Engineering, Yonsei University, Seoul, KOREA.

Noncrystalline Si (nc-Si) on p-type Si substrate and indium-tin-oxide (ITO) have been prepared by pulsed laser deposition technique using a Nd:YAG laser with the wavelength of 355 nm. Biaxial pressure was maintained at 1-10⁵ Torr. Noncrystalline Si thin films are deposited in a nitrogen-helium ambient. nc-Si thin films are heteroepitaxially grown on ITO for nc-Si and are annealed in nitrogen gas. Strong violet-indigo luminescence from Si nanocrystalites has been observed at room temperature by photoluminescence (PL). Dependence of the electroluminescence (EL) properties on various deposition time and film structure will be discussed using ITO/nc-Si/p-type Si/metal structure.

D4.25 EVOLUTION OF SPUTTERED H₂O-ThIN FILMS UPON ANNEALING. Seok Woon Nam, Jung Ho Yoo, Seokun Nam, Dae Hong Ko, Dept. of Ceramic Engineering, Yonsei Univ., Seoul, KOREA; Jin Hua Ku, Sinyoung Choi, Samsung Electronics Co., Ltd., KOREA.

We investigated the evolution of the physical and electrical properties of H₂O thin films deposited by the reactive DC magnetron sputtering method on the (100) substrate upon annealing. The H₂O thin films deposited at room temperature were amorphous, while the films after annealing were polycrystalline. The crystallization temperature of the H₂O thin films was dependent on the annealing methods (RTOP or Furnace) and ambient (nitrogen or oxygen). The microstructures of H₂O thin films were determined using X Rays (X-RAy) and AES. We also focused on the interfacial layer between H₂O thin films and silicon substrates. Due to its high oxygen diffusivity, any contamination lead to oxygen diffusion from the H₂O layer. The EOT decreased upon annealing due to the increased SiO₂-containing layer. The H₂O thin films deposited at room temperature have the undesirable interfacial states due to the surface damage by sputtering. We found that the H₂O thin films <150°C thick were optimized by RTOP or furnace annealing.

D4.26 FLAT BAND VOLTAGE, HYSTERESIS AND BREAKDOWN OF HAFNIUM SILICATE PREPARED BY PVD TECHNIQUE. Hongguo Zhang, Guangtong Pant, Manuel Quevedo-Logar, Prakapetch Pungpapit, Bruce E. Grade, Robert M. Wallace, The Lab of Electronic Materials and Device, Dept. of Materials Science, Univ. of North Texas, Denton, TX.

The shift of flat band voltage Vfb and hysteresis observed on MOS capacitors prepared by PVD techniques are examined for (100) orient n+ silicon-silicon substrate. Using a Pt/Al gate CV system, the Vfb shift can be attributed to changes in the working function of gate metal and the electronic properties of the oxide layer, as had previously been reported. In addition, we show that the hysteresis results from a reduction of interface state and oxide fixed charge due to the different forming gas annealing temperature. The obvious hysteresis shows that the existence of large amount of trapping defects inside the oxide layer. The interface state and oxide fixed charge densities are calculated and related to the available bonds at the interface. The breakdown experiments confirm that the Vfb shift for the MOS samples is mainly due to a reduction of oxide fixed charge in the oxide annealed in higher temperature, and to a lesser degree, to a reduction of interface charge.

D4.27 THE METAL INDUCED LATERAL CRYSTALLIZATION OF AMORPHOUS SILICON THIN FILMS BY ALTERNATING
In silicon doping in transistor the Fick’s law of Diffusion is not adequate representation. This is because; a) mathematically it is poorly convergent at the short time limit for surface flux and b) it physically implies an infinite velocity of mass. The hyperbolic mass wave equation can represent the finite speed of propagation of mass which is realistic. Nothing is faster than the speed of light. The ‘only’ modification that will return singularity to the second derivative in time in the hyperbolic partial differential equation. The problem of quenching a finite slab with both the ends of 1 dimension brought to –1 C to the bath temperature from a initial C0. The non-dimensionalized variable (t) is defined as the time of zero. The separation of variables technique is used to get cosine series in X with boundary conditions being 2(1-1/m) and u = (c1-1/m)(c2x) the time domain is represented by a second ODE. The solution gives a complex representation whose real part x-axis and imaginary part y-axis which provides a period to the temperature solution damped by a decaying exponential. This is for values of b) > 1/2 solved for by integration and is 1/m. This analytical solution can be used to predict the transient heat transfer in 1-dimension.

B4.31 GRAZING-ANGLE INCIDENCE X-RAY DIFFRACTION BY THE SiGe/Si HETEROJUNCTION WHERE THE GERMANIUM AND THE CARBON CONCENTRATIONS ARE PERIODICALLY VARYING ALONG THE FLAT-LAYER SURFACE.

Hayk H. Bez ingiany (Jr.), Yerevan State Univ., Faculty of Physics, Yerevan, ARMINIA; Siranush E. Bez ingianyan, Hakob P. Bez ingianyan, Yerevan State Univ., Faculty of Physics, Yerevan, ARMINIA; Prof. E. Bez ingianyan (Jr.), R. Engineering Univ of Armenia, Dept of Computer Science, Yerevan, ARMINIA

Evaluation of the coherent part of x-radiation scattered by strained or relaxed crystalline, as well as amorphous thin Si(x)Ge(y) layer deposited on the silicon substrate is presented in [1], and it pointed out the possibility of the direct Grazing-Angle Incidence X-ray Diffraction (GIXD) experimental investigations of the long-period structured intermediate transmission states of Si(x)Ge(y) layer, which are emerging due to periodicity of the strain field along the substrate-layer interface. The measurements were done based on the theoretical method presented in [2]. The Si-C bond length is much smaller than the bond lengths in Si(x)Ge(y) monolayer, therefore a small amount of carbon atoms provided an additional design parameter in manipulating the strain (e.g. see [3]), i.e. the effect of the increase of the average lattice constant due to germanium atoms can be compensated by adding the carbon atoms in the heterostructure. While studying the influence of carbon in Si(1-x)Ge(x) layer, it is also important the investigation of the behavior of the tensile strained Si(1-x)Ge(x) layers [e.g. see [4, 5]]. In this paper we present the GIXD theoretical curves of a thin film Si(1-x)Ge(x) layer deposited on a silicon perfect-crystal substrate. The diffraction curves due to a specific longitudinal order in a layer e.g. through harmonic variations of the germanium and carbon composition coefficients in the heterostructure. References: 1. P.A. Bez ingianyan (Jr.), A.P. Bez ingianyan, S.E. Bez ingianyan and K.O. Hovsepian, Grazing-Angle Incidence X-ray Diffraction Curves of Si(x)Ge(y) Thin Layer if the Composition Coefficient |x| is Varying Harmonically Along the Flat Layer Surface, the Book of Abstracts of 10th International Conference on X-ray Optics and Microanalysis (ICXOM XVI), Vienna, Austria, 2001, p. 57. 2. A.P. Bez ingianyan and P.A. Bez ingianyan, Solution of the Two-dimensional Stationary Schrodinger Equation with Cosine-Like Coefficient in View of X-ray Diffraction, Phys. Stat. Sol. (a), 105 (1988) 354–553. 3. B. Dietrich, H.J. Osten, H. Bucker, M. Methfessel, and P. Zaussmil, Lattice Distortion in a Strain-Compensated Si(1-x)Ge(x) Crystal, in Silicon, Phys. Rev. B, 49 (94) (1994) 17185–17190, 4. G.G. Fischer, P. Zaussmil, E. Bugiel, and H.J. Osten, Investigation of the High Temperature Behavior of Strained Si(1-x)Ge(x) Crystals, J. Appl. Phys., 77(5) (1994) 1364–1367. 5. H.J. Osten, D. Endisch, E. Bugiel, B. Dietrich, G.G. Fischer, Myungchul Kim, D. Kruger, and P. Zaussmil, Strain Relaxation in Ternary-Strained Si(1-x)Ge(x) Layers on Si(001), Semicond. Sci. Technol., 11 (11) (1996) 1626–1627.
As the size of microelectronic devices decreases dramatically, the RC delay and the capacitance per area become critical for VLSI technology. Accordingly, large effect is being made on the interlayer dielectrics such as carbon-doped oxides which have the lower dielectric constant than the silicon dioxide constant of about 4. However, since the SiO2 group is used in the silicon oxide-based, the volume expansion and the interface characteristics are becoming inferior. This is caused by disruption of the glass network. This phenomenon is known to affect mechanical properties such as the fracture toughness, modulus, and hardness which are closely related to the reliability of the microelectronic devices. On my study the interfacial debonding and failure between the dielectric and adjacent layers in the multi-layer stack of thin film will be focused. Those failure are caused by both the stress and residual stresses between the films. Within the Linear Fracture mechanics technique the energy, termed as the critical strain energy release rate or the interface debonding energy, which is needed to debond the dielectric film from the adjacent film can be determined. Fracture energy, which is obtained from the lines around the interface as well as the plasticity in adjacent layers. Since inorganic silicate behaves like a completely brittle material, the carbon-doped oxide film is expected to behave in the same manner. Therefore the fracture energy of the interface is sensitive to the interface chemistry and glass composition. The subcritical debonding is also concerned in terms of reliability. Under the environment of high humidity and temperature crack can be growing with much less driving forces. This can cause the problem to the microelectronic devices. Two kinds of ways of making carbon-doped oxide film are used. Those are spin-on glass and CVD method. To measure the critical strain energy release rate, 4-point bending and other methods have been considered. These methods are characterized testing, the resulting fracture surfaces were characterized by XPS scans to determine the debonding path. From the data obtained it is clarified that the fracture toughness is decreasing with the carbon content. However, we have not yet determined what kind of influence the carbon content influence. Moreover the debonding interface for CVD method is mostly happened on the lower interface between dielectric and silicon nitride layers by XPS scanning. It is explained that the fracture mode is the mixed mode so that the crack is growing downward as well as forward. For future work, the various kinds of functional groups can be attached to the polysilicon and tested and moreover the subcritical cracking can be induced by many modes of humidity and temperature situation. Finally, the relationship between the glass composition and structure and the resulting mechanical properties can be elucidated.

8:15 AM B5 2
SYNTHESIS OF ORDERED NONPOROUS SILICA FILM WITH HIGH STRUCTURAL STABILITY. Noriko Kishiyama, Shin-ICHI Ikeyam, Osaka University, Osaka, JAPAN; Yoshiaki Oku, MIYAZAKI; Tsubasa, Japan; Akira Nakamura, Roko Co., Ltd, Tokyo, JAPAN

In this study, we synthesized nanoscopic silica films with high structural stability on a silicon wafer. The silicone wafer was coated with a precursor solution by a spin-coating method. XRD patterns of the films showed that highly ordered silica was formed on the silicon wafer. The [101] reflection peak was not observed in the XRD pattern showing that the straight pore channels were oriented parallel to the support surface. The precursor probably mainly consisted of surfactant molecules on the silicone wafer. However, the formation of a silicate network is thought to be insufficient because the reaction rate of the condensation of silanol groups is not high at low temperature. To complete the condensation of a silicate network, the post-synthesis treatment was carried out. Then the calcination was conducted at 670 K for 5 h to remove surfactant molecules. No peak shift of the [100] reflection was observed in the calcined silica film. The peak intensity did not decrease, indicating high structural stability of the treated silicate film. FE-SEM images of the cross section of the treated silica film showed that its thickness is about 300 nm. The periodic porous structure can be observed in the cross section of the silica film. This result is consistent with the results of the XRD patterns, which indicate that the straight pores are oriented parallel to the surface of the silicon wafer. Normally, the periodic ordered structure of nanoscopic silica gradually collapses under water vapor in the atmosphere. In this study, the silica films were silanized with organic vapor to enhance the resistance against water vapor. The pore surface effectively increased its hydrophobicity by silanization. The organized structure of the silanized silica film was maintained under saturated water vapor at 333 K.

8:30 AM B5 3
HIGH QUALITY ZrO2 GATE DIELECTRIC FOR SiGe MOS DEVICES Kwon, Jonguk, Sungsoo Jeon, and Hyounguk Hwang, Kwangju Institute of Science and Technology, Dept of Materials Science and Engineering, Kwangju, KOREA

Considering high hole mobility of strained SiGe/Si heterostructure, CMOSFETs with SiGe MOSFETs are promising for future high speed device. However, a conventional high temperature thermal oxidation for gate dielectric is not compatible with SiGe heterostructure because of strain relaxation and Ge segregation effect. Improvement of carrier mobility of SiGe MOSFETs with poor passivation layer is expected because silicon capping layer reduces Ge segregation and interface roughness during the thermal oxidation. Recently, the ZrO2 film was investigated as an alternative gate dielectric for SiGe MOS devices. On the oxide dielectric characteristics of ZrO2 on SiGe with silicon capping layer, Epitaxial 30-nm-thick Si$_x$Ge$_{1-x}$ strained layer was grown on p-type silicon wafer. For comparison, 70-nm-thick epitaxial silicon capping layer was grown for some samples. Various thicknesses of ZrO2 layer was deposited by obelisk evaporation followed by wet vapor annealing at 820°C. After the deposition of a 150-nm-thick layer of Pt, MOS devices with a gate area of 9x10^-3 cm$^2$ were defined. The wet vapor annealing of ZrO2 reduces stresses, which can be explained by the reduction of oxygen vacancy of as-deposited ZrO2. Compared with ZrO2 directly deposited on SiGe, ZrO2 deposited on silicon capping layer exhibits a significant improvement of electrical characteristics such as low leakage current, low interface state density, and lower surface roughness. The improvement of electrical characteristics of sample with silicon capping layer can be explained by negligible Ge segregation.

8:45 AM B5 4
CHARACTERISTICS OF ZIRCONIUM BASED AMORPHOUS THIN FILMS FOR GATE ELECTRIC APPLICATIONS. Chang-Ho Jeon, Seung-Ho Kong and Jiyong Kim, Dept. of Materials Engineering, Kookmin University, Seoul, KOREA

Considering high leakage currents of thermal SiO2 films with thickness less than 2.0 nm, development of high-k films for gate dielectric applications is necessary to scale device dimension down to 10nm. Alternative gate dielectrics should simultaneously satisfy several harsh requirements, such as high dielectric constant, a low leakage current, a good thermal stability on Si substrate, and excellent interface characteristics, etc. Even though various high-k materials have been studied in order to replace conventional thermal oxide, most of them show a trade-off. Uranium metal oxides such as TiO$_2$ and ZrO$_2$ and are easily transformed from amorphous to crystalline during dopant activation annealing. Since polycrystalline thin films have lots of grain boundaries, amorphous phase is relatively preferred. On the other hand, silicium such as SiC$_x$O$_{3-x}$ shows excellent thermal stability. However, the silicium have relatively low dielectric constants (1-12). In order to realize use of the silicium as an alternative dielectric, dielectric constant should be improved. In this study, we investigate effects of composition between Zr and Si on thermal stability and dielectric constants. In addition, effect of Al and Bi as novel glass network formers are also evaluated. Amorphous thin films were deposited by reactive co-sputtering because of its easiness on compositional change. However, reactive sputtering easily causes undesirable interfacial layers. In this study, various treatments, such as nitridation were employed in order to reduce the interface layer. The deposited films were annealed at various ambient and then Pt top electrodes are formed. We will extensively report the effects of composition of Zr based glass in thin films on thermal stability and dielectric behaviors on Si substrate.

9:00 AM B5 5
MOLECULAR LAYER DEPOSITION OF ULTRATHIN ZIRCONIA FILMS ON SILICON USING POLYNUCLEAR METAL ALCOXIDE PRECURSORS. Jason Lee, Walter G. klempner, University of Illinois, Frederick Seitz Materials Research Laboratory and Department of Chemistry, Urbana, Illinois, A. G. Khan and David A. Payne, University of Illinois, Frederick Seitz Materials Research Laboratory and Department of Materials Science and Engineering, Urbana, Illinois.

Conventional atomic layer deposition provides a viable route to high-k dielectric films on silicon. In order to reduce the number of growth cycles required, we have investigated the use of polynuclear metal alkoxide precursors capable of growing at atomic scale in a single reaction step. Ulzriconia thin films have been deposited on silicon using a tetrameric zirconium alkoxide precursor, Zr(OC$_2$)$_4$(OMe)$_4$, in fluid solution. Films with equivalent oxide thickness less than 2.0 nm and low leakage currents less than $10^{-7}$ A/cm$^2$ at -2.0 V were obtained using this process.

9:15 AM B5 6

Currently there is still no clear front runner for the next alternative gate dielectrics despite extensive efforts. Much of the material
research and integration development are focused on transition metal oxides and silicates, rare earth metal oxides and other oxides. This paper presents recent advances in the synthesis, characterization, and application of transition metal oxides. The primary focus is on the application of transition metal oxides in various fields, such as catalysis, energy storage, and optics.

**10:00 AM B5.7**

**ALTERNATING LAYER DEPOSITION (ALD) OF METAL SILICATES AND OXIDES FOR HIGH-DIELECTRIC INSULATORS IN GATES AND CAPACITORS**

Roy G. Gordon, Jill Becker, Eric Greynson, Dennis Hausmann, Esther Kim, Seiji Suh, and Ying Wang, Harvard University, Dept. of Chemistry and Chemical Biology, Cambridge, MA.

New processes are developed for ALD of silicon oxides and oxides of the metals lanthanum, zirconium, hafnium, and tantalum. For deposition of metal silicates, the silicon and oxide sources are triethanolamine (TEA), TEOS, and the metal precursors are metal alkylamides such as tetrakis(dimethylamido)hafnium, [MnN]. Alkoxides. Pulses of silicon vapor and metal alkyl silica vapor are introduced alternately and separately into the heated deposition zone where they react on the surfaces of substrates. For the deposition of metal oxides, the metal alkylamides are reacted with water vapor instead of the silanol. Each of these reactions is shown to be self-limiting within a certain range of substrate temperatures. Excellent step coverage and high uniformity of thickness and compositions are found for films deposited within these temperature ranges. By using both silanol and water pulses, various compositions are deposited with siloxane to silicon ratios ranging from zero up to 4:1. The surfaces of the films are quite smooth, with an rms roughness by ALD HfO2 less than 1% of the thickness. The stoichiometry and kinetics of the surface reactions are studied with a quartz crystal microbalance. The oxide reaction is found to be remarkably fast, while the silicate reactions require a higher flux to reach saturation.

**10:30 AM B5.8**

**CHARACTERIZATION AND ELECTRICAL PROPERTIES OF ULTRA THIN HfO2 GATE DIELECTRICS PREPARED BY ATOMIC LAYER DEPOSITION.**

Tae-Ho Lee, Joon-Min Oh, Han-Yong Huh, Dept. of Materials Science & Engineering, Seoul, KOREA; Young-Chae Kim, Dae-Wook Cho, Han-Yong Huh, Dept. of Ceramic Engineering, Seoul, KOREA; Jin-Hee Jung, Bae-Taeuk Kim, Sung-Mo City, Kyungsugi-Do, KOREA; Jin-Ho Ahn, Han-Yong Huh, Dept. of Materials Science & Engineering, Seoul, KOREA.

For the future integrated circuit manufacturing, new materials and thin film deposition methods will be needed for gate dielectric preparation. Among the various thin film deposition methods, atomic layer deposition (ALD) is one of the most promising technologies because of meeting the strict requirements of the future IC manufacturing. However, the evaluation of this ultrathin high dielectric film is cumbersome and sometimes difficult. In this research, we have investigated the characteristics of ultra-thin HfO2 films using several analytical techniques. HfO2 films were deposited in a traveling wave tube ALD reactor (Plas 200T) using HfCl4/H2O gas as precursors and N2 as a carrier gas. HfCl4 was volatilized in a carrier gas at 100°C and introduced into the reaction chamber with pure N2. H2O carrier gas was kept at 120°C and carrier gas was not used. The films were grown on 8-inch [100]-type silicon wafer in the temperature range of 200-400°C after standard RCA cleaning.

Spectroscopic ellipsometry, XRD and TEM were used to investigate the initial growth mechanism and microstructure. The chemical composition of deposited film was analyzed by RBS and XPS. The electrical properties of the film were measured and compared with the physical properties such as thickness, deposition temperature, and precursor injection time on the ALD HfO2 films. The TEM analysis results show consistent with XPS and CV analysis. While results to date do not allow unambiguous linkage between OH reduction and silicon surface oxidation, the results suggest that the post-deposition OH- absorption is a critical issue. The conclusion is to improve the controlled post-deposition reactivity in high dielectric deposited silicon on.
temperatures (800C/35min) result in measurable nitrogen concentrations at the metal dielectric interface (from Rutherford back-scattering measurements) and substantial changes in fixed capacitance–voltage measurements.

11:30 AM B5.12
ELECTRICAL AND STRUCTURAL PROPERTIES OF ULTRA-
THIN ZIRCONIA DIELECTRICS. Shriram Ramasubramanian, Paul C.
McIntyre, Stanford University, Dept. of Materials Science and Eng.,
Stanford, CA; David A. Muller, Bell Laboratories, Lucent
Technologies, Murray Hill, NJ.

Ultra-thin ZrO2 films are currently being investigated as a potential
material for replacement of SiO2 in future complementary metal-
oxide-semiconductor devices. In order to integrate them into future
transistors, a fundamental understanding of their electrical
properties is desired. This requires thorough investigation of the
microstructural and interface chemistry of these films in conjunction
with studies of their dielectric behavior, which will enable the
processing methods to grow high-quality zirconia films. This paper
deals with studies on thin films of zirconia grown by ultraviolet ozone
crystallization of Zr metal films at room temperature. The effects of
oxidation time, oxygen partial pressure, the underlayer and annealing
conditions have been studied in detail. It was found that
partially-oxidized films exhibited significant frequency dispersion
in both the depletion and accumulation regions, while fully-oxidized
films showed negligible frequency dependence. A model based on the
Maxwell–Wagner interfacial polarization mechanism has been used to
type such phenomena and will be presented in detail. The electrical
studies show that electric energy storage properties of these films have been complemented with detailed studies of the electronic structure using atomic resolution EELS in STEM. It was found that the oxygen
stoichiometry of the zirconia films had a significant effect on the O-K
near edge structure and this will be discussed using a molecular orbital
description. Studies on CV hysteresis revealed that the flatband shift varied with zirconia thickness. It was found that the
leakage current could be modeled as direct tunneling at low voltages while Poole-Frenkel conduction dominated at higher voltages. The
hysteresis behavior is consistent with a model based on two-mos
effects. A simple model for the CV hysteresis is presented. References: S. Ramasubramanian et al., [a] Appl. Phys. Lett. (in

SESSION B6. GATE OXIDES AND INTERFACES
Chair: David O’Meara and Jon-Paul Maria
Wednesday Afternoon, April 3, 2002
Salon 106/12 [Marriott]

1:30 PM B6.1
SUBSURFACE REMOVAL OF SiO2 TO CREATE A DIRECT
SILICATE/SILICON INTERFACE. A. Careri, V. Naryan, S. G. Kim,
K. L. Carver, V. Naryan, S. G. Kim, K. L. Carver, V. Naryan, S. G.

In order to reduce parasitic capacitance in alternative gate dielectrics, it is quite common to remove surface SiO2 prior to deposition of a metal oxide dielectric. A typical procedure involves aqueous HF etching to create an oxide free surface. Using medium energy ion
scattering we have investigated a novel approach, where interfacial oxide is removed after deposition by high temperature annealing in ultra-high vacuum. Surprisingly, there is a temperature window in which silicide formation does not occur, but oxygen containing species can freely migrate out through a silicide overlayer. An examination of the kinetics shows a similarity to SIO desorption from SiO2/Si(001), suggesting that the same mechanism occurs for an SiO2 layer embedded underneath a silicide. The results confirm stability predictions for silicide–silicate dielectrics, i.e. for the proper choice of materials, the metal-oxide bonds have greater stability than the silicon-oxide bonds.

1:45 PM B6.2
Sr FLUX CLEANING OF Si AND THE FORMATION OF
TEMPLATES FOR SrTiO3 GROWTH. Xiaoming Hu, Yi Wei, B.
Ooms, Physical Research Laboratories - Motorola Labs, Tempe,
AZ; D. Sard, Optical Sciences Center, University of Arizona,
Tucson, AZ.

The removal of native silicon dioxide using a beam of Sr atoms and the resulting Sr/Si(100) surface phases have been studied by LEED, AES and STM. The conditions for the formation of Sr/Si(100) template, namely the “2eV” phase, for epitaxial MBE SrTiO3 growth [1] have been identified. It has been found that the resulting Sr/Si surface phases depend upon the substrate temperature during the Sr flux desorption process, in agreement with earlier findings that the Sr/Si(100) template is formed when deposited Sr/Si is dehydrated during Sr desorption from Sr/Si(100) [2]. Post annealing of a sample obtained with the substrate at a lower temperature resulted in the slow absorption of Sr atoms from the silicon surface and a progression of Sr phases with time. Similar results could also be obtained with the silicon substrate held at higher temperatures. Sr flux cleaning of a silicon wafer pre-treated with HF has also been studied and similar Sr/Si phases can be obtained by adjusting the substrate temperatures or annealing conditions. [1] Z. Yu, R. Ranadhe, J-A. Curless, J. M. Cade, C. E. Dinari, and R. Droopad, K. W. Eisenbeisser, J. A. Hallmark, and W-J Ooms, J. R.

In this work, we investigated the characteristics of the gadolinium oxide thin films controlled by interfacial layers. Ultrathin ZrO2 and SiO2 layers grown on Si (111) were used to modify the surface of the Si substrate. The characteristics of the films were assessed using various characterization tools, such as electron diffraction (LEED) and x-ray diffraction (XRD), atomic force microscopy (AFM) and X-ray photoelectron spectroscopy (XPS). We found that the structural transition from cubic GdO2 to monoclinic GdO2 occurred in lower layers. In particular, the transition was enhanced at the existence of ZrO2 buffer layer. The crystallinity of the films was significantly affected by the buffer layer was inserted or not. The interfacial reaction between Gd and Si or GdO2 was determined using XPS analysis. The buffer layers successfully controlled the interfacial reaction and high quality epitaxial growth were formed.

2:15 PM B6.4
PREPARATION AND OH ABSORPTION IN LANTHANUM
SILICATES FORMED BY OXIDATION OF PVD La ON Si.
T. Goyteut, M. J. Kelly, W. S. Burns, A. M. Bennett, T. J.
Schmit, and J. Y. Pettin, Dept. of Chemical Engineering, NC State
University, Raleigh, NC.

We have prepared La-based amorphous La-O-Si alloys, i.e. "silicates", by sputter depositing La onto Si in a UHV sputter chamber, then oxidizing in O2 at temperatures ranging from 400C to 900C. Because lanthanum is reactive in air, target preparation and handling is critical to maintain high purity La deposition. When La is deposited on Si and oxidized, X-ray Photoelectron Spectroscopy indicates that the La reacts very rapidly with the silicon, leading to predominately La-O-Si bonding units in the film. The mechanisms are similar to those detailed previously for Y PVD and oxidation, but the rate of reaction between La and Si is significantly faster than that of Y and Si. The relative concentration of La and Si in the resulting film depends on initial La layer thickness, substrate pretreatment, and oxidation time and temperature. By controlling these parameters, we have been able to achieve La-Si-O thin films with equivalent oxide thickness as small as 1.5A based on capacitance–voltage analysis. CV show good behavior, with evidence for positive fixed charge, similar to most other reports of metal oxide high-k dielectrics. After deposition, infrared absorption of thicker silicate films showed evidence for OH absorption from the ambient. The rate of OH absorption depended strongly on the annealing temperature, suggesting a structural compensation of the dielectric layer upon annealing, similar to well-known processes in SiO2. The knowledge of silicate and silicide–silicate dielectrics can help promote reactions between metal oxides and silicides, resulting in unmasked lower-k layer formation at the high-k/silicon interface. Details of the material preparation and stability to OH absorption will be discussed in terms of advancing the understanding of controlling interface reactions during CVD of high-k dielectrics on semiconductor surfaces.

3:00 PM B6.5
OXIDES, SILICIDES, AND SILICATES OF LANTHANUM AND
HAFNIUM. DENSITY FUNCTIONAL THEORY STUDY. Mucie
Yurdakul, John D. Jaffe, Pacific Northwest National Laboratory, Environmental Molecular Sciences Laboratory, Theory, Modeling &
Simulations, Richland, WA; Chun-Li Liu, Michael Bloemer, and
Environmental Molecular Sciences Laboratory, Theory, Modeling &
Simulations, Richland, WA; Chun-Li Liu, Michael Bloemer, and

It is known that the chemistry of hafnium and zirconium are more
nearly identical than for any other two congeneric elements. Thus, both zirconium, with the dielectric constant K of 21, and hafnium (K = 21) have chemical and physical properties very similar to those of a gate dielectric. We have recently found that there is an important difference between the zirconium/Si and hafnium/Si interfaces. The former was found to be unstable with respect to formation of silicides whereas the latter is stable. This surprising difference prompted us to study differences between oxides, silicides, and silicides of hafnium and zirconium. The calculations were performed in the framework of density functional theory with the Perdew-Wang 91 exchange correlation functional. Ionic compounds were found to be more stable for hafnium than for zirconium with the heats of formation of oxides and silicides being larger by ca. 0.5 eV for hafnium. The higher ionization of hafnium compounds is also reflected by the band gaps that are larger by 0.5 (oxides) and 0.9 (silicates) eV for hafnium than for zirconium. The higher ionization of hafnium compounds is consistent with a smaller electron negativity of atomic hafnium (1.2) than zirconium (1.4). It is also consistent with atomic ionization potentials 7.9 and 7.7 for Zr and Hf, respectively. Silicides were found to be more stable for zirconium than for hafnium with the heats of formation of disilicides being larger by ca. 0.3 eV for zirconium. Both mono and disilicides were found to be metallic with no quantitave differences in densities of states between hafnium and zirconium compounds.

3:15 PM B6.6 DOPANT DIFFUSION STUDIES FROM As, B, AND P-DOPED POLYSILICON THROUGH CVD DEPOSITED HF/SILICATE THIN FILMS. M. Quevedo-Lopez, P. Puchnirachet, G. Pant, M. El-Boumairi, J. Ken, B.E. Grade, and R.M. Wallace, Department of Materials Science, University of North Texas, Denton, TX; J. Colombo, M. Bevan, M. Doyle, A. Liutkous, and M. Visokay, Si Technology Research, Texas Instruments Incorporated, Dallas, TX.

As the aggressively scaling of CMOS technology continues, high-k gate dielectrics become one of the solutions in the providing increased capacitance without remarkable increase in gate leakage current. However, issues such as thermal stability[1] and dopant penetration[2] still require further study. Dopant penetration into the channel region from doped polysilicon is an increasingly important issue in MOSFETs. Under high temperature processing, such as dopant activation annealing, dopants can diffuse out of the doped polysilicon gate, through the thin gate dielectric and into the Si substrate, causing a shift in the threshold and flat-band voltages of the device. Diffusion studies of boron, arsenic, and phosphorus from doped polysilicon through the high-k gate dielectric thin film (4.5 nm) candidate HfO2/HSiOx into Si will be presented. The Polysilicon/ HfO2/HSiOx/Si stack was subjected either to rapid thermal processing (RTP) or standard furnace annealing in an N2 atmosphere. After annealing, the polysilicon and dielectric films were chemically etched prior to depth profiling using Secondary Ion Mass Spectroscopy (SIMS) methods. As-deposited and annealed films were studied using X-ray Photoelectron Spectroscopy (XPS) and High Resolution Transmission Electron Microscopy (HRTEM) to determine structural changes or growth of interfacial layers. Dopant penetration after aggressive annealing was observed. Polysilicon removal and dielectric film removal issues after annealing will also be discussed.


SESSION 57 POSTER SESSION DELECTRIC CHARACTERIZATION Wednesday Evening, April 3, 2002


Hafnium silicides are leading contenders for replacing silicon oxynitride as the gate dielectric material in CMOS devices. Silicides as defined herein cover the entire composition range from SiO2 to HfO2 and are regarded as a homogenous mixture of the binary oxides. Silicides offer advantages over the binary oxides that include maintaining an amorphous nature (at least as-grown or during subsequent thermal processing below 1000°C) and etching comparable to SiO2 of VLSI CMOS equipment. The as-deposited film deposition of Hf silicate is used in the dielectric properties of Hf oxide. A variety of appropriate metallic precursors are being evaluated. This study investigates and compares the deposition of Hf silicate films from two suites of metalorganic CVD precursors. The first precursor suite has oxygen-coordinated Hf metalorganic precursors and includes β-diketonate, Alkoxide and nitrosy ligands. The second precursor suite has alkylamido ligands, which have nitrogen coordinated to the Hf or Si center. Since these amido precursors do not contain oxygen, the oxygen activity of the process is controlled independently from the precursor. The process has increased Hf oxide (HFO) composition in the precursor solution. The composition of the films, including Hf/oxide, oxygen, carbon, and nitrogen content were measured by XPS. Both suites of precursors provide routes by which composition can be controlled in fully oxidized films with low carbon and nitrogen content. Very thin interfacial layers (HRTEM) are also shown.

3:45 PM B6.8 INVESTIGATION OF LIGHT INITIATED OXIDATION OF HYDROGEN PASSivated SILICON SURFACES: H2-Si[100] AND H2-Si[111]. Kathleen A. Morse, Stanford University, Dept of MS&E, Stanford, CA; Peter Filippetti, Dept of Electrical Engineering, Stanford University, Stanford, CA.

Factors present in cleanroom air that may lead to contamination prior to processing need to be better understood in order to meet future requirements for atomically clean surfaces prior to gate oxidation. This paper identifies the conditions that initiate room temperature oxidation of fluoride prepared hydrogen passivated silicon surfaces by using X-ray Photoelectron Spectroscopy (XPS). Possible oxidation factors investigated include lighting conditions and gaseous ambient. Both H2-Si[100] and H2-Si[111] surfaces do not oxidize under dark lighting conditions for 100% humid and dry air atmospheres. These surfaces oxidize in the dry air and 100% humid conditions when the substrate is directly exposed 250um light. Wavelength dependence for oxidation on both surfaces is confirmed. In addition, the level of oxidation is observed to depend on substrate orientation but not dopant type.

4:00 PM B6.9 SILICON NANOSTRUCTURES THROUGH NEAR-FIELD OPTICAL LITHOGRAPHY. Yadiang Xin, Yuanxin Xin, Univ of Washington, Dept of Chemistry, Seattle, WA.

Near-field optical lithography with an electromagnatic phase-shift mask has now been combined with a high-aspect ratio (90:1) nanoscale metalorganic [2] vapor monolayer to generate nanosstructures of single crystal silicon with well-defined shapes and dimensions. We have demonstrated the capability and feasibility of this approach by fabricating nanowires, nanorings, and interconnected triangles with lateral dimensions of 100 nm. This dimension could be further reduced to 20 nm by adding self-aligned oxidation to this process. These silicon nanostructures are potentially useful as active components in fabricating nanoscale electronic devices. They also provide a class of model systems to study nanoscale mechanics and electrochemistry.
B7.2 DEVICE SCALING EFFECTS ON SUBSTRATE ENHANCED DEGRADATION IN MOS TRANSISTORS. Neer R. Mahapatra, Sourav M. Majhi, and Ramgopal Rao, Department of Electrical Engineering, Indian Institute of Technology Bombay, MUMBAI; Bell Laboratories, Lucent Technologies, NJ.

Recently, enhancement of electron injection in reverse substrate bias (V_{sub}) is observed due to impact ionization feedback mechanism, which is helpful for realizing fast and low power non-volatile memories. The reduction of L_{opt} and T_{on} of the transistor affects the internal electrical characteristics, hence carrier heating and injection process. The damage creation and the resulting device degradation thus become a strong function of device dimensions and therefore merit attention. Till date, no work has been done to study the effect of substrate bias on (V_{sub}) in this paper, we have studied the reliability issues of n-channel MOS transistors having different L_{opt} and T_{on} for different reverse V_{sub} under identical bias and gate current (programming time for flash memories) conditions. The L_{opt} dependence studies are performed on devices having T_{on} of 3μm. The T_{on} dependence studies are performed on devices having L_{opt} of 0.2 μm. With increase in negative V_{sub}, impact ionization feedback occurs, which increases carrier heating thereby gate current. Also, for higher negative V_{sub} the injected carriers are not confined to a narrow zone but spread out. We observe an increase in ΔV_{th} and ΔG_{m} by 1.6 and 1.72 when the device is stressed at V_{sub} = -2V. The higher ΔG_{m} can be attributed to an increase in substrate current. With a decrease in L_{opt} from 0.4μm to 0.1μm, ΔV_{th}, I_{on}, and ΔG_{m} are increased by a factor of 4.3, 2.31 and 2.88 respectively for V_{sub}=-0 and by a factor of 3.7, 3.08 and 2.95 respectively for V_{sub}=-2. This indicates that if L_{opt} of a MOSFET is reduced at a constant bias, the ΔV_{th} increases whereas the ΔG_{m} decreases due to higher SCLs. Since the injection and thermal degradation at negative V_{sub} has a very strong dependence on E_{opt}, we observe higher I_{on} and degradation for V_{sub} = -2V. The increased I_{on} can be attributed to large number of secondary holes in the substrate and the higher degradation is due to higher gate injection and larger spread of carriers in the traps. We have also studied the degradation for different L_{opt} and T_{on} under constant gate injection and generation efficiency.

B7.3 USE OF SMALL GATE VOLTAGE PULSES FOR THE EXTRACTION OF THE INTERFACE TRAPS DENSITIES IN MOS STRUCTURES USING THE CHARGE PUMPING TECHNIQUE. E. Lin, E. Moussy, and D. Baurt, Laboratoire de Physique des Composants Semi-conducteurs, UMR CNRS 5231, ENSERG, Grenoble, FRANCE.

In MOS structures with ultrathin oxides, the determination of the interface trap densities, D_{it}, with conventional interface trap characterization techniques is difficult due to the small gate voltage excursions allowed before Fowler-Nordheim injection or direct tunneling occurs in the trap. Using the charge pumping technique, the most widely used technique for interface trap characterization, large gate voltage pulses imply such currents. The use of high frequencies to increase the CP current magnitude has been proposed [1]. In this paper, small gate pulses are proposed for the extraction of D_{it}. They strongly limit the leakage currents and extend the experimental conditions which can be used (the frequency can also be used to increase CP signal magnitude). For this, and as the theoretical derivations that allow the extraction of D_{it} also require large gate pulses (pulses larger than (V_{G} + V_{th}) where V_{G} and V_{th} are the device threshold and flat band voltage) [2], the extraction of D_{it} is extended to the case of small gate pulses, i.e. pulses smaller than (V_{G} + V_{th}). To this end, the theoretical der-derivations are reconsidered in order to account for both emission and capture in various situations. This provides equations that: 1) more accurately describe the CP current when large gate pulses are used, 2) generalize the description of CP current to a wide range of situations including reduced high and/or low bias levels and the effect of small trap cross-sections and 3) allow D_{it} to be calculated whenever the gate pulse is. These results are applied for characterizing MOF device with thick and ultrathin oxides. Due to this end, and with respect to the above results, the large distribution of trap time constants evidenced at the interface cannot be overlooked when using small gate pulses and only a fraction of the interface traps is expected to be probed [3]. The interface trap densities measured, effectively decrease when reducing the pulse height, especially for high values smaller than (V_{G} + V_{th}), but with pulse heights as small as (V_{G} - V_{th})/2, that is ≤ 0.6 V, the D_{it} values obtained in a factor of two equal or measured conventionally. This is a fully acceptable result if one accounts for all the uncertainties on the determination of D_{it} for instance, the differences between the values obtained using different characterization techniques. [1] P. Masson, J.L. Austram, and J. Brini, IEEE Electron Device Letters 20, 92 (1999). [2] Van den Broeck et al. IEEE Trans. Electron Devices 38, 1820 (1991). [3] D. Baurt and Y. Mreghi. IEEE Trans. Electron Devices 44, 2262 (1997).

B7.4 THE SOLUTION OF GOI IMPROVEMENT ON HIGH VOLTAGE DEVICE. S.Y. Ko, H.M. Guo, Y.F. Tsay, Y.J. You, Taiwan Semiconductor Manufacturing Co. Ltd., Hsin-Chu, Taiwan, ROC.

The thicker thickness of gate oxide is required to make sure the product can work on high voltage condition. However, the traditional dry oxidation method can not meet the testing requirement. The aim of this paper is to provide a quality method to produce a high quality gate oxide for mass production. There are three process factors were studied for this gate oxide quality improvement on dual voltage product. The first gate oxide is to form a thick oxide and then a thin oxide. The brief summary (dominance of Product-HV product) as list: 1) Oxidation methodology. The low temperature (850°C) and three steps (dry-wet-dry) get the better VBD performance than 920°C/860°C or two steps (dry-wet) conditions. The mechanism is annealing, dewetting bond and crystal original pin effect. 2) Sack gate formation methodology. The prior gate oxide forming method changed from oxidation to LPCVD is considered. HTO replaces dry-wet-dry oxidation will get better VBD result. It is believed COP effect. But, TEOS didn’t have the similar result since carbon element impact. 3) Wafer material source. Above two experiments were done on CZ polisher wafers. AR anodised wafer performance is slightly better than H2 anodised wafers, but both anodised wafers performance was better than wafer. According the studying above, COP effect plays the major dominance of the gate oxide quality on high voltage devices. Oxidation method, sack gate formation and wafer material are pointed out the advantages and shortages (this paper provides some solutions on gate oxide quality improvement for mass production.

B7.5 DEGRADATION IN A POLYBENZENUM GATE MOS STRUCTURE CAUSED BY N+ ION IMPLANTATION FOR THE WORK FUNCTION CONTROL. Tatsuki Amada, Nobuhide Mochi, Kentaro Shibahara, Research Center for Nanodevices and Systems, Hiroshima Univ, Hiroshima, JAPAN.

Work function control technique of the Mo gate by annealing or N+ ion implantation has been reported by Ramade et al.[1] with the aim of dual work function CMOS fabrication with a single metal material. We also fabricated the Mo gate MOS diodes with 5-20 nm SiO2 gate oxides and found that the gate leakage current were increased as N+ implantation dose and implantation energy were increased. Though work function shift was observed in CV characteristics, the hump due to the high-density interface states was found for high-dose specimens. Nitrogen SIMS depth profile showed that nitrogen was implanted much deeper than calculated depth obtained by SIMS simulator. Chroming of the N+ ions implanted nearly vertically [1,2] into columnar structure Mo film is the considerable origin of this deep profile. To reduce N+ ions that pass through the gate oxide, we have compared angled implantation with the nearly vertical one. In the case of tilt angle of 30 degrees, the gate leakage current was reduced compared with the 7 degree case. Since the decrease in projected range of N+ ions for the 30 degrees angled implantation is only 15%, the deep profile and gate leakage increase seems to be attributed to the channel et effect. [1] P. Ramade et al., Jpn. J. Appl. Phys., Vol. 61, 2000. C3.2. 1 Acknowledgement: Part of this work was supported by STARC (Semiconductor Technology Academic Research Center).

B7.6 ELECTRICALLY INDUCED JUNCTION MOSFET (EIJMOS) FOR HIGH PERFORMANCE SUB-90NM CMOS TECHNIQUE. A. Bhat, R. O. Dassaneh, and R. Ramgopal Rao, "Department of Electrical Engineering, Indian Institute of Technology Bombay, MUMBAI; 3Department of Metallurgical Engineering and Materials Science, Indian Institute of Technology, Bombay, INDIA.

An electrically induced junction MOSFET (EIJMOS) is different from conventional CMOS device in that the shallow source/drain (S/D) junctions are electrically induced by the gate voltage. In such a device, the shallow extensions and the doped regions of opposite conductivity as that of deep S/D. In order to turn ON the device a voltage is applied at the gate of a EIJMOS, such that the shallow doped regions below poly gate get inverted and serve as shallow S/D extensions. Consequently, the effective channel length in this condition is the distance between these shallow doped regions. On the contrary, at any gate voltage less than that required to invert these regions, no S/D extension is induced and the effective channel length is equal to the physical separation between the deep S/D junctions. Our proposed structures also reduce the series resistance.
effects when compared to the recently published devices based on a similar concept.

In this work, we compare 4um gate length EJMOs and conventional devices using 1SC-TCPAD process and device simulations. In the EJMOs process, shallow extension regions under the gate are achieved by a compensation doping using a large angle tilt implant from both source and drain sides, after patterning the gate. The resulting MOSFET is symmetric in nature and can be fabricated using conventional CMOS processes.

From extensive 5D process and device simulations, we observe over an order of magnitude increase in Ion/Ioff, improved sub-threshold characteristics, and better short-channel performance. Overall, our simulation results show, the EJMOs structure offers significant advantages over the conventional CMOS technologies in the sub-5um regime.

B7.7 APPLICATIONS OF AFM/SCM IN PROCESS CONTROL AND FAILURE ANALYSIS OF SEMICONDUCTOR DEVICES

As the minimum feature size of semiconductor devices continues to shrink, analyses of the engineered structures and materials of semiconductor devices are increasingly critical in manufacturing and in the development of new generation devices. Furthermore, the performance of a modern device is strongly influenced by its dopant distribution in depth and laterally. Scanning capacitance microscopy (SCM) is one of the techniques that has been developed to reveal the dopant distribution in both directions. In this work, Al0.3 Ga0.7N doped EJMOs were investigated. Two p-channel devices, Si based and GaAs based, were studied. In the process control area, two examples are presented. The interface between the AlGaN/GaN buffer layer and the GaAs substrate is an important issue for the reliability of the device. The resistance of the ohmic contact on the p-doped GaAs layer was found to be about 2.2 μm away from the edges of the exposed GaAs region. Another important application of SCM is in device failure analysis. In this work, a failed p-channel transistor was investigated by SCM. Two levels of dopant concentration are found in the corresponding source and drain regions by SCM. Another approach to identify the cause of failures is to directly compare a failed device with a properly functioning one. The use of SCM to study the same N-well structures in two devices, one good and the other failed, determined that the depth of the N-well for the failed device is about 0.4 μm shorter than in the good device.

B7.8 SILICON SURFACE CHEMICAL TREATMENTS IN OXIDE/NITRIDE DIELECTRIC STACK PROPERTIES. David Jacques, Sebastian Petittidier, J. L. Bogdani, Kathy Buhl, STMicroelectronics, Orleans, FRANCE.

The ‘oxide’ terminated silicon surface may be chemically grown through several methods compatible with the ULSI technologies. These methods include oxidation, nitridation, silicon dioxide (~SiO2)/nitride (~Si3N4) stacks as a dielectric for memory cell. In the present work we studied the dielectric oxide/nitride (~ON) stack performances after different chemical treatments of the Si starting material through dielectric leakage current and charge to breakdown measurements on the ON stack on single crystal Si (~Si0) and in Poly-Si substrates. Three main steps are followed to complete the ON stack: (1) the wet chemical surface treatment. Two main methods available to us to achieve this were before a chemical deposition: surface cleaning and surface passivation. The RCA cleaning, the ozonized water DI/W03, and the HF last were independently used. (ii) the surface nitridation. The chemical oxides have been thermally nitridated transforming the silane oxide in some SiOxNy layer over which the SIN will be deposited. (iii) the nitride deposition. SiN 5 nm thick was deposited using DC/SiH4 gas mixture, below 1 Torr total pressure and at 500°C in a batch vertical furnace. Morphological analysis of the silicon nitride surface (Atomic Force Microscopy) and SIN incubation time for growth are comparable for all the studied cases on ~Si. However, Tod-SiOxNy shows a higher oxygen content at the stack interface following the different chemical treatments. Electrical measurements show comparable CV and I-V results, for the same Equivalent Oxide Thickness (same capacitance at strong accumulation) the different interfaces bring the same interfaces and devices with lower space charge losses for higher interface oxygen content. However, for DRAJ applications, a clear improvement in electrical characteristics is obtained under low interfacial oxygen content conditions. Results are compared in embedded-DRAM cells for which we developed an industrially compatible process to achieve minimum leakage current with maximum speed capacitance and no particular linking constraints.


We describe the preparation and properties of the (LPD) SiO2 films deposited by liquid phase deposition from supersaturated solutions with both silicon powder and silicic acid. From the both solutions the resulting (Si(OH)2)n rich supersaturated solution, when slightly diluted with De-ionized (DI) water deposits SiO2 on to silicon [1]. Our work was motivated by the search for the conditions of the optimum condition for device quality oxide growth within a low (<300°C) thermal budget, for large area device fabrication, on inexpensive substrates such as glass and plastic. The net growth of the LPD oxide layer is result of competition between deposition and etching; the balance and hence the rate of growth being controlled simply and reproducibly by the addition of de-ionised (DI) water [2]. We have produced device grade SiO2 from the solution at 48°C onto both n and p type Si substrates. Control of the oxide properties is achieved in the amount of DI water added to the supersaturated solution. Oxide layers of optimum quality being obtained by the titration of 60ml DI water to 100ml of supersaturated solution. FTIR, ellipsometry, and C-V/L-V measurements were used to characterise the films deposited from solutions of silicon powder and silicic acid. The resistivity of the optimum layers from a saturated solution of silicic acid were found to be 10sm2/cm with breakthrough field strengths of the order of 3.5 x 10^6 V/cm. The resistivity of the optimum layers prepared using (silicic acid were much higher (10^8 Sm2/cm) with breakthrough field strengths of the order of (9-11) x 10^6 V/cm. The results approach those of thermally grown silicon dioxide, suggesting that the LPD oxide have the potential of device quality insulator on large area substrate such as glass and plastic. References [1] C.F. Yeh et al., IEEE Electron Device Letters, vol. 14, No. 8, Aug. 1993, [2] Chung-Fan Yeh et al. J. Electrochemical Soc., 141(11), pp. 3177-3181, 1994.

B7.10 DEVELOPMENT OF SPIN-ON PRE-METAL DIELECTRICS (PMD) FOR 0.11UM DESIGN RULE AND BEYOND. Zhongtao Li, Xinhong Zhou, Dave Wyman, Mike Spaulding, Gunm Kim, Stelian Gregores, DK Choi, Eric Meyer Semiconductors Fabrication Materials, Dow Corning Corp., Midland, MI.

Spin-on pre-metal dielectric (PMD) materials are being developed for memory and logic devices at 0.11um design rules and beyond. The strong design rules require a PMD material with a low dielectric constant, low loss, short patternable window, excellent gap fill capability, and etch resistance similar to that of a thermal oxide. A novel Spin-on PMD has been developed to meet these requirements in current PMD technologies of HDP CVD or BLC PMD. These constraints are imposed by void formation and high thermal budget requirements. One common challenge that faces spin-on PMD is inhomogeneous densification, or “corner etch”. In this paper EELS/STEM, FTIR, SEM and HF wet etching were used to study the mechanism of this phenomenon. The spin-on PMD resin based on this information will be presented.

B7.11 THE OPTIMIZATION OF UNIT PROCESSES IN A INTER LAYER DIELECTRIC APPLICATION USING NOVEL POLY SILAZANE-BASED SOG. Jung-Ho Lee, Jung-Sik Choi, Dai-Won Kang, Dong-Jun Lee, Sang-Moon Choon, Samsung Electronics Co., LTD., Material Technology PJT, Kyung-Do, KOREA.

Currently borophosphosilicate glass (BPSG) has been widely used to integrate the inter layer dielectric (ILD) to fill gaps between word lines. However, there are a lot of problems in using BPSG for manufacturing very large scale integration (VLSI) devices. To solve these problems, a novel polysilazane-based spin-on glass (SZ-SOG) method is evaluated to apply to ILD layer. In this paper, the unit process conditions were optimized. The main spin revolution was fixed at 1000rpm, because when the film was prepared lower than 1000rpm caused crack problem after the main bake, and the film under high rpm condition had no enough thickness margin for chemical mechanical polishing (CMP). When the susceptor was used wedge bond removal (EBR) process was used to minimized microscratches and defects due to particles provided from wafer level. The pre-bake temperature was selected in the range from 150 to 200°C to keep film flowability property of next process. Finally, one PMD film must be formed not only of perfect silicon film but also a dense film through the main
B7.14 ONETRICE DRIVING Cu DIFFUSION INTO INSULATOR.

This study is part of Japanese national project to develop a FCF-free and energy-saving ILD (interlayer dielectric) process. In this project, we have also been investigating ILD process that does not require a barrier film to prevent Cu diffusion. Thus, a clear understanding of the mechanism by which Cu diffuses into an ILD is essential. A simulated potential energy shows that when Cu penetrates SiO2, it must be converted to Cu++. One possible driving force is Schottky defects (crystal defects). The estimated current density was less than 3 E-14A/cm² (Observed value > 1 E-12). From this value, it is clear that diffusion through defects is not the dominant process.

The current density of a Cu-electrode/TEOS/Si structure was measured with a probe in a vacuum chamber, which allowed the ambient conditions to be controlled. The lowest current density was obtained when degassed TEOS formed by vacuum annealing was used and the LV characteristics were measured just after deposition of the Cu electrodes. The current density was found to be the same exposed to N2, though it did increase after exposure to dry air. It should be noted that degassed TEOS film contains hardly any water or oxygen molecules. In contrast, conventional TEOS not subjected to annealing contains both, and samples made with this material exhibited the highest current density. These results demonstrate that Cu diffusion contributes to oxygen or TEOS and oxygen molecules exhibit strong paramagnetism. The interaction between the magnetic moments of Cu and OZ lowers the potential. That means that the insulation allows Cu to TEOS. Small-angle X-ray diffraction showed that ZnO films were divided into two groups just after formation of the Cu electrode. One set was kept in a magnetic field for 2 days, and the other set was kept in air. The samples kept in a magnetic field had higher magnetic field densities than the others. This demonstrates that one cause of Cu diffusion into an insulator is the presence of O2 in the insulation. Acknowledgments: This work was performed under the management of ASET in a METI R&D program supported by NEDO.

B7.15 CHARACTERIZATION OF POLYISILSESQUIOXANE) SPIN-ON FILMS FOR LOW-DIELECTRIC APPLICATIONS.
MICROSTRUCTURE, ELECTRICAL PROPERTIES AND MECHANICAL PROPERTIES.
Jeyung Hyeon-Lee, Yi Yeol Iyu, Sang Kock Min, Jin-Hoong Yim, Hyun-Dam Jeong, Samsung Advanced Institute of Technology, E-Polymer Laboratory, Tucson, KOREA, Mong Sup Lee, Sang Youl Kim, Korea Advanced Institute of Science and Technology, Dept of Chemistry, Tucson, KOREA.

We studied the effect of porogen content on the film properties of porous poly(isilsesquioxane) material. Organic/inorganic nanohybrids were prepared by using a thermally stable poly(epichlorohydrin) as a template, and SOG-silesquioxane polymer as a matrix material. The template was removed by thermal decomposition. The SOG-silesquioxane polymer is a new type of highly porous films. It is found that the dielectric constant depended on the porogen content and hardness of the thin film were affected by the porogen content. The thin films had dielectric constant of 2.2 with good mechanical strength.

B7.16 EVALUATION OF LOW-K POLYMER THIN FILM CONTAINING BORAZINE-UNIT.
Masahiro Inoue, Tkuya Fukuda, Arumia Matsuura, Hiroshi Yamasawa, ASET, Yokohama, Kanagawa, JAPAN, Yuko Uchimaru, Naoko Kodai, Hiroshi Yamashita, AIST, Tsukuba, Ibaraki, JAPAN.

It was predicted that the polymers containing borazine unit were low-k materials, because a dielectric constant was simulated by both molecular polarizability and number of molecule in a unit volume through the moiety of the molecular orbital band calculations. Two hybrid polymers containing borazine unit, such as borazine-carboline unit and borazine-siloxane unit, were evaluated on electric characteristics. These polymers were synthesized by hydrolysis/lactonization polymerization of B[3][B[3]]-triethyleneN N N'-trimethylborazine with p-(dimethylamil)[dimethyl]benzene or tetramethylethylicarboline. Polymerization under diluted conditions gave a homogenous solution of the polymer. From measurement under these conditions, the homogeneous films of the polymer were made on a silicon wafer by spin-coating method, followed by annealing at 300–500°C under argon gas. The dielectric constants of these thin films were evaluated to be 2.8–1.8, lower than values and annealing conditions. The thermal resistance was good, because the temperature of weight decreasing to
MULTILEVEL INTERCONNECTS BY ION IMPLANTATION
Thin films of xerogel and SILK (Low-k materials) were implanted with argon, nitrogen and helium etc. with 2E5 and 1E6 doses at energies varying from 50 to 150 keV at room temperature. In this work we describe the improvement of electrical as well as the improvement of device properties by implantation of dielectric materials by ion implantation. Ultrasonic Force Microscopy (UFM) and Nano-indentation technique have been used for qualitative and quantitative measurements respectively. The hardness increased with increasing ion energy and dose (fluence), the hardness improvement varied with ion species. Dramatic improvement of hardness is seen for multi-dose implantation. Characterization of xerogel and SILK using Ion beam technique will be presented.

B7.20
STUDY OF POROUS SILICA BASED FILMS AS LOW-K DIELECTRIC MATERIAL AND ITS INTERFACE WITH COPPER METALLIZATION
L. Fisher, M. Eisenberg, Dept. of Materials Engineering, Technion-Israel Institute of Technology, Haifa, ISRAEL; M. Naik, and T. Weidman, Applied Materials, Santa Clara, CA.
The success of future gigascale integrated circuit (IC) chip technology depends critically upon the reduction of the interconnect RC delay time. This calls for the development of new low dielectric constant interconnect materials, which have lower loss and higher performance. Porous silica based films prepared by surfactant templated self-assembly spin-on deposition is an attractive candidate as a low-k material. In this research, we have studied the structure, the electromagnetic properties, and the bonding of the films as their interface with copper metallization. The decomposition and vaporization of the structure in the last step of the film deposition results in a film with an amorphous structure as determined by X-ray diffraction and TEM analysis and its high porosity (35-55%) is confirmed by X-ray reflectivity measurements. XPS analysis of the Si2p transition indicates three types of bonding: Si-O, O-Si-C and Si-C. The effect of various plasma post-treatments on oxidation (evaluated by hardness and adhesion) on the film topography and bonding was determined by AFM and XPS, respectively. It was found that direct H2 plasma exposure exerted a significant effect of surface roughness of the film (rms 111 Å; ≈ 87 Å) and bonding strength (high Si-O vs Si-C bonding percentage). The structure and properties of various PECVD deposited capping layers were also studied, as was the interface between the porous dielectric and Ta, TaN, Cu (PVD deposited diffusion barriers) and Cu after annealing at 200-700°C. The 200°C and 500°C annealing treatments did not indicate any diffusion of Cu or Ta into the porous film, as determined by AES and SIMS. However, the 700°C anneal resulted in complete Cu penetration into the porous film, when deposited directly on it, whereas when used in a thin (~50 Å) TaN diffusion barrier layer was interposed between the Cu and the porous film, the Cu penetration was insignificant.

B7.21
SURFACE PROPERTIES OF LOW-k HYBRID-ORGANIC SILICONE-POLYMER (HOSP) FILMS ETCHED WITH IONS OF DIFFERENT INCIDENT ANGLES IN CHF3, PLASMA
Sumin Lee, Hwang, Gyeongnam Institute of Electronics and Semiconductor, Seoul, KOREA; W. Suchow, Meun, National Seoul University, School of Chemical Engineering and Institute of Chemical Processes, Seoul, KOREA; Yu Chang Kim, Hyun-Kyu Ryu, Yun Seok Cho, Jin Woong Kim, Hynix Semiconductor Inc; Memory R&D Division, Kyongik-do, KOREA.
Hybrid-organic-silicone-polymer (HOSP), a representative spin-on-glass low-k material, was etched in CHF3 plasma while ions were incident on the substrate at specific angles for the purpose of understanding the practical conditions of plasma etching. HOSP films contacting another HOSP bottom surface at different angles were placed in a Faraday cage, which allowed ions to travel in a pre-determined direction independent of the substrate alignment in the cage, and then the films were etched in CHF3 plasma at 5mTorr while the bias voltage was varied between -100V and +400V. As a whole, the etch yield, defined as the etch rate/incident ion, showed a cosine dependency on the ion angle. However, the etch yield slightly deviated to higher values from those predicted by the cosine-dependency curve when the ion angle was lower than 80°, and fell below the cosine curve at angles higher than 80°. To understand the different behaviors of the etch yield dependency on the ion angle, we visualized different etching at two different angles, 70° and 90°, representing the low and the high angle regions respectively. Atomic force microscopy (AFM), Auger electron spectroscopy (AES), and X-ray photoelectron spectroscopy (XPS) were used for the analysis. The surface of the HOSP film was rougher after etching at 90° than at 70°, and the difference
in the surface roughness increased with the bias voltage. A thick fluoroacrylate surface layer was observed on the HOSP film after etching at 900 V/um. This film formation was enhanced at high bias voltages due to the redeposition of particles emitted from the bottom surface. When the HOSP film etched in CHF₃ plasma was subsequently exposed to O₂ plasma for ashing, the film surface became more rough than before the etching, except for when the film was etched at 70° and at low bias voltages.

B7.23
POLARITY DEPENDENCE OF DEGRADATION IN ULTRA THIN OXIDE AND JVD NITRIDE GATE DIELECTRICS. Yasir Metha, K.N. Manjubhusan, J. Vasu, V. Ramgopal Rao, Indian Inst of Tech-Bombay, Mumbai, INDIA.

We have studied Jet Vapor Deposited (JVD) silicon nitride MNSFETs and compared their degradation under identical field conditions with conventional MOSFETs. The devices used in this study are n-channel transistors with 7.1 nm of the gate dielectric of either a 3.9 nm for MOSFETs and a 3.1 nm for nitrides. The technology used for both devices is same except the dielectric deposition process. Silicon nitride is deposited using jet vapor deposition technique, whereas the oxide is thermally grown at 650°C. In this work, the evolution of the interface state density NISS with stress for both nitrides and oxides is systematically investigated. Charge pumping method at 1 MHz is used to calculate NISS. We have observed that in both oxide and nitride device, the degradation is higher under negative gate polarity. Also, in case of nitrides, the degradation in NISS is always lower as compared to oxides for both positive and negative stress. The results are analyzed in detail with the well-known hydrogen transport and trapped-hole recombination models. We conclude that trapped hole recombination is the more dominant mechanism of degradation. The devices under real operating conditions are subjected to bipolar or AC stress rather that DC conditions normally used for such degradation studies. This paper presents results using AC stress experiments on these ultrathin oxide and nitride MOS transistors. The frequency, peak-to-peak voltage and off voltage of the applied AC signal are some of the parameters that are varied. Detailed characterization results and analysis of the same will be presented.

B7.24
SYNTHESIS AND CHARACTERIZATION OF METHYLTRIETHYLSILANOL BASED LOW PERMITTIVITY (LOWk) POLYMER GATE DIELECTRICS. Z. Gu, Department of Chemical Engineering, R. Jeyakumar, S. Sivoththaman, A. Nafieh, Department of Electrical and Computer Engineering, University of Waterloo, Waterloo, Ontario, CANADA.

Low-permittivity (lowk) polymeric dielectrics are potentially very attractive as interconnection material in a wide range of semiconductor circuits. In this work, a lowk polymeric material has been synthesized using methyltriethoxysilane as base material, and the material properties have been characterized. The material was synthesized using an experimental set-up that performed refluxing, hydrolysis, gelation, and polymerization steps. The final product is a high-flowing brownish liquid, that is spin-coatable to yield uniform films after coating and curing treatments. The film properties were used for structural characterization of the material. Test structures on silicon were fabricated to measure the dielectric constant (k) of the material. The values of k were found to be in the range of 1.9 - 2.7 (at 1 MHz) for annealing temperatures 250°C - 450°C. The annealed films as well as the initial material were found to be very stable. Fourier Transform Infrared (FTIR) spectroscopy was used for the structural characterization. Prominent peaks, (Si=CH3 stretch, Si-O stretch, Si-C, etc.) are observed and their dependence on film annealing conditions as well as material formation conditions will be discussed. In addition to the electrical and structural properties of the films, the paper will also report on integration-related issues such as planarization, film-stress, etc. (ref: Yamada et al., J. Electrochem. Soc. Vol. 147, p. 1477, 2000).

B7.25
EFFECT OF ION-ACCELERATED PLASMA HYDROGENATION AND THERMAL TREATMENTS ON HYDROGEN SILSESQUIOXANE (HSQ) LOWk DIELECTRIC FILMS. R. Jeyakumar, L. Ren, and S. Sivoththaman, Electrical and Computer Engineering, University of Waterloo, Waterloo, Ontario, CANADA.

Hydrogen silsesquioxane (HSQ) is a very promising polymeric dielectric with a low permittivity (k). However, higher curing temperatures and presence of oxygen tend to increase k. In this work, the effect of ion-accelerated plasma hydrogen exposure, film annealing temperature, and annealing ambient on the permittivity and structural properties of HSQ lowk dielectric films have been investigated. Experiments were performed on test structures fabricated using spin-on HSQ lowk films. The film curing temperature was varied from 275°C to 575°C. The k values were found to be increasing with increasing curing temperature, and stayed below 3.2 for temperatures up to 400°C. Fourier transform infrared (FTIR) spectroscopy showed a reduction in Si-H peaks with increasing temperature. The presence of oxygen in the curing ambient was also found to have a strong influence on the dielectric constant as well as in the intensity of Si-H peaks with the reduction in Si-H peak intensities starting to occur at lower temperatures (~180°C). When the cured films were subjected to an ion accelerated hydrogen plasma treatment (250°C, 13.56 MHz RF plasma, 45 minutes), a very significant reduction in k was observed for all curing temperatures. (up to 45% reduction in k). The paper will report on the dependence of electrical, structural, and mechanical properties of the HSQ films on different thermal and plasma treatments.

B7.26
USING CARBON NANO TUBE CANTILEVERS IN SCANNING PROBE METROLOGY OF INTEGRATED CIRCUIT STRUCTURES. Y.N. Emerson, S. Sivoththaman, Center for Microelectronics Technology Research, D. A. Walters, R. Metha, University of Central Florida, Physics Department; Z.P. Huang, Z.F. Ren, Boston College, Physics Department; B.B. Rosiu, Agere Systems; and R. Schulz, University of South Florida, Center for Microelectronics Research.

Carbon nanotubes (CNT) are among the candidates for atomic force microscopy probes for use in high aspect ratio critical dimension metrology (CDM). Their mechanical strength at small diameters makes them ideal high resolution probes for narrow and deep features. The synthesis of CNT has been making great progress in recent years. The use of CNT in scanning probe microscopy, however, has been limited due to a number of problems. While the CNT probes generally appear to be lasting, the manufacture of precisely aligned CNT of defined length, diameter and number of walls poses a number of challenges. Yet, such precisely defined CNT probes appear to be required if the cantilevers are to be used for CDM. Our results demonstrate, for example, that the attachment angle of CNT with respect to the cantilever beam is crucial for their application in CDM.

We report about our efforts to overcome these problems by growing well-defined CNT on standard Si cantilevers.

SESSION B8: METALS AND INTERFACES

Chair: Janice L. Veteran and Mehmet C. Ozturk
Thursday, Morning, April 4, 2002
Skol 10-12 (McKnight)
8:00 AM BS.1
SELF-ALIGNED PASSIVATED COPPER INTERCONNECTS: A NOVEL TECHNIQUE FOR MAKING INTERCONNECTIONS IN ULSI DEVICE APPLICATIONS. Amit Chhug, Ashutosh Tiwari, A. Kev, J. Narayan, NSF Center for Advanced Materials & Smart Structures, Department of Materials Science and Engineering, North Carolina State University, Raleigh, NC.

We have developed a technique to grow self-aligned epitaxial Cu/MgO
films on Si (100) using a Pulsed Laser Deposition Method. In this method we deposit a uniform film of Cu/Mg (5:75) alloy over Si (100) at room temperature using TMS311 reactor. As a result of HRTEm (with spatial resolution of 0.18 nm) and STEM-Z investigations we observed that when this film is annealed at 500°C on a controlled oxygen environment, in less than 30 minutes time, all the Mg segregates at the top and at the bottom surface of Cu. This is understood to be the consequence of lower surface energy of Mg. At 500°C Mg is quite sensitive to oxygen and a thin layer of MgO is immediately formed at the top surface, we also observed a thin layer of MgO at the Cu/TiW interface. Thickness of the upper MgO layer was found to be 15 nm while that of lower layer was 10 nm. Lower MgO layer acts as a diffusion barrier and inhibits the diffusion of Cu in the system. Upper MgO layer acts as passivating layer and improves the quality of copper oxidation. Electrical resistivity measurements (in the temperature range 123-0.0) showed MgO/MgO/Ti/Si (100) sample to be highly conducting. We also observed that the resistivity of the system is insensitive to ambient oxygen environment. Self-aligned MgO (15nm) layers were used to grow several interesting materials over it. This technique can be used to integrate high temperature superconductors like YBa2Cu3O7-δ with silicon chip.

8:15 AM **DB.2**

**RESISTIVITY AND ELECTRODEPOSITION IN Cu-AG ALLOYS** V. Brosseau, K.S. Hwang, Cleveland, Department of Metallurgical Engineering, Salt Lake City, UT.

Cu has been implemented by some chip manufacturers recently for interconnects. It is anticipated that replacement of Cu by Cu-Ag alloys may improve some properties. Recently there have been attempts to look beyond Cu and some Cu alloys have been proposed for future interconnects. In this study, the viability of Cu-Ag alloy as a possible interconnect is explored since it is the only alloy that offers a lower cost and higher reliability as compared to pure Cu. The sputter deposited Cu-Ag alloy films have been characterized in terms of resistivity, composition, microstructure, adhesion, electromigration lifetimes and electromigration activation energies. The (Cu/Ag) alloy films were deposited by sputtering Cu/Ag alloy targets of different compositions. The films were annealed in situ in vacuum at 400°C for 30 minutes. The resistivities for the deposed and annealed films were relatively higher and lower respectively than Cu interconnections. The microstructures of the films were evaluated and possible microstructural mechanisms for the resistivity decrease and electromigration resistance were discussed. Adhesion of Cu-Ag alloy films seemed to be poor when compared to Cu on Si oxide, but showed good adhesion with a Ta under layer. Interconnect structures were etched out with Ta/Cu and Ta/Cu/Ag bilayers for electromigration reliability testing. The accelerated lifetime tests were conducted by passing high density current through the structures while maintaining the test structures at a constant temperature by a temperature controlled hot and cold chuck system specially assembled for the purpose. The resistivity changes as a function of time at different temperatures are recorded and the analysis shows that the activation energies for electromigration were determined.

8:30 AM **DB.3**


The use of lowly dielectric and for Cu metallization is chiefly responsible for the reduction in the interconnect delay time in deep submicron integrated circuits. Cu contamination during back end of line (BEOL) processing is considered a serious issue by the industry. Under binuclear Cu contamination has been shown to pose no serious problems in Cu process integration (K. Prasad et al., MRS 2008 Spring Meeting, San Francisco, USA, April 24-28 2008, Symposium D). However, there are reports of Cu contamination induced degradation of MOSFETs when a thin layer of oxide is present between Si wafer and Cu metallization (Hozawna et al., 2000 Symposium on VLSI Technology, Honolulu, USA, June 13-15 2000). It is obvious that the diffusion kinetics of Cu is very different in oxide and Si. In this study we will study the diffusion of Cu in lowly dielectric materials such as Black Diamond (Applied Materials Inc.) and CORAL (Novaceus Systems Inc.). MOS structures with Cu [deposited by ionized metal plasma] lowly dielectric (Black Diamond, CORAL, etc.) were used. The MOS structures using conventional silicon dioxide and silicon nitride are also fabricated. They are subjected to thermal annealing in the temperature range typically used for BEOL processes, for various times. Cu contamination and diffusion depth in silicon substrate and in lowly dielectric material and Si substrate are studied using SIMS and TXRF analyses. The electrical stability of MOS structures with Cu contamination is studied using LV and CV measurements. A correlation between Cu contamination and MOS electrical stability will be established. Diffusion properties of Cu in different lowly dielectric materials are compared and possible diffusion mechanisms in these dielectric materials will be reported. This work is supported through the award of a joint research grant from NSERC/IFOR.

8:45 AM **DB.4**

**MODELLING COPPER DIFFUSION IN SILICON OXIDE, NITRIDE, AND CARBIDE.** Vladimir Zibrov, Sheldon Aronowitz, LSI Logic, Sunnyvale, CA; Joseph Han, Charles Musgrave, Dept of Chemical Engineering, Stanford, CA.

High diffusivity of Cu through low k and regular oxides is well established. However, nitrides and carbides exhibit effective barriers for the Cu drift. Ab initio methods and cluster approximation were applied to explore the barriers to Cu diffusion in oxide, nitride, and carbide. Since copper penetration in oxide is significantly enhanced by negative bias, copper ions are used to simulate oxidation. In this work interactions of copper cation, Cu+, with molecular clusters modeling basic units of the silicon oxide, nitride, and carbide materials were considered. Most of the results obtained for clusters involving one or two rings each bearing four Si atoms and four X groups where X contains O, N, or C atom. Calculations revealed strong interactions of Cu+ with model clusters. Copper diffusion should proceed as elementary hops between stable structures. Stable structures resulting from interaction of Cu+ with the oxide, nitride, and carbide clusters were found. Estimated low bounds for activation energies for Cu+ hops between stable structures and their agreement with experimental results Affect of spatial arrangement variations in amorphous oxide, nitride and carbide on Cu+ diffusion is discussed. The diffusion of neutral copper in oxide was also considered. In this case interaction of Cu with the model clusters is weaker and implies a high barrier for penetration of neutral Cu atoms from bulk copper into oxide. The results suggest that the barrier to copper diffusion in these materials is determined by their intrinsic properties. A possible technologically effective approach to raising the oxide barrier to Cu+ diffusion is discussed.

9:00 AM **DB.5**

**GROWTH MECHANISMS AND PROPERTIES OF TANTALUM THIN FILMS GROWN BY PLASMA ENHANCED ATOMIC LAYER DEPOSITION.** H. Kim, C. Calhur Jr., C. Lawie, S.M. Rosanogl, IBM Thomas J. Watson Research Center, Yorktown Heights, NY.

Ta films were grown by plasma-enhanced atomic layer deposition (PE-ALD) at temperatures from 20°C up to 500°C using TaCl5 as source gas and RF plasma-produced atomic H as the reducing agent. Post-deposition chemical analyses showed that the main impurity is oxygen, incorporated during the air exposure prior to analysis. The films had typically low Cl concentration below 1 at%. X-ray diffraction shows broad diffraction features, indicating the ALD Ta films are composed of nanocrystals. The typical resistivity of ALD Ta films was 150-180 μΩ cm, which corresponds to that of Ta-20%, for a wide range of growth parameters. The conformality was up to 1000%, in trenches with aspect ratio of 15. The thickness per cycle, corresponding to the growth rate measured by Rutherford backscattering spectrometry and for quartz crystal microbalance as a function of various key growth parameters, including TaCl5 and H exposure time and growth temperature. The maximum values of thickness per cycle were below 0.1 μm, due to the steric hindrance for TaCl5 adsorption. Based upon these results, the basic growth mechanisms for Ta PE-ALD are discussed. The diffusion barrier properties of ALD Ta films were investigated using bilayer structures consisting of Ta films deposited by sputtering and ALD Ta of various thickness on Si. Various analysis techniques were applied during heating, including X-ray diffraction, elastic light scattering, and resistance analysis. The results were compared with Ta films deposited by sputtering with comparable thicknesses.

9:15 AM **DB.6**

**THE EFFECTS OF NITROGEN ON ELECTRICAL AND STRUCTURAL PROPERTIES OF TaSx, Nbx, /SiO2 SLAB CAPACITORS.** You Sok, Su, Greg House, Joon-Ho Lee, and Yoon Mira, Department of Electrical Engineering, North Carolina State University, Raleigh, NC.

As gate oxide thickness decreases, the capacitance associated with the depleted layer at the poly-Si/gate dielectric interface becomes significant, making it necessary to consider alternative gate-electrodes. However, there are many challenges when they must have compatible work functions, process compatibility and thermal/chemical interface stability with underlying dielectric. Most gate electrode studies to date suffer from high temperature instability resulting in low performance, and low thermal stability. Our recent work has shown that TaSxNry (Si > Ta) films on SiO2 have excellent thermal stability at high temperatures and the
workfunction of TaSi\_2N\_4 is compatible with NMOS devices. In this work, TaSi\_2N\_4 films were deposited on the SiO\_2 gate oxides using reactive co-sputtering of Ta and Si. Both Ta and Si target electrodes with different compositions have been used to investigate the effects of the nitrogen in the TaSi\_2N\_4 gate on the electrical and structural properties. The role of nitrogen in the TaSi\_2N\_4 gate was studied by comparing flatband voltage and the equivalent oxide thickness with nitrogen. The thermal stability of TaSi\_2N\_4 on SiO\_2 stacks was studied at annealing temperatures of 700°C and 900°C in Ar. XPS and TEM analysis were performed to get the bonding information in the films and interfacial reaction between TaSi\_2N\_4 film and SiO\_2.

10:00 AM DB.7
NON-DESTRUCTIVE MONITORING OF COBALT SILICIDE USING PICOSECOND ULTRASONIC MEASUREMENTS.
Amit Nandan, Texas Instruments Inc., DMOS, Dallas, TX; Chi-Kong Cheng, University of California, Berkeley, Dept of Chemical Engineering, Berkeley, CA; Niall Mc Caucas, Rudolph Technologies, Flinders, NJ.

Silicides in CMOS technology have historically been monitored by measuring sheet resistance at different stages of the metal-silicon reaction. Sheet resistance being destructive in nature, requires that these measurements be made on non-product wafers. As contacts continue to shrink in size with more stringent processing requirements, the use of a non-destructive technique to gauge the silicidation process directly on product devices becomes increasingly important. Elimination of non-production material also has processing cost and time reduction benefits which can be significant at 300mm diameter wafer fabrication. In this study, we investigated the use of picosecond ultrasonics to assess thickness and density of cobalt metal and silicide phases over the different stages of silicidation. An ultrasonic technique was used to examine the film and measure the thickness of the film and thickness of the cobalt silicide as a function of time. Samples of different thickness were measured after cobalt deposition, CoSi reaction, cap layer strip and CoSi anneal. Models were developed to extract the thickness and density of the films at each step, on both single crystal silicon and polycrystalline silicon substrates. A correlation was obtained between sheet resistance and thickness for the different stages of the cobalt silicide formation.

10:15 AM DB.8.8
SINGLE CRYSTAL TaN THIN FILMS ON TiN/SI HETERO- STRUCTURE. Haiyan Wang, Ashutosh Tiwari, Alexander Kiv, Xingdong Zhang, Jeafslah Narayan, Department of Materials Science and Engineering, North Carolina State University, Raleigh, NC.

We have successfully grown epitaxial cubic (H1-111) structure tantalum nitride films on Si (100) and (111) substrate using a pulsed laser deposition technique. A thin layer of titanium nitride was used as a buffer medium. We characterized these films using X-ray diffraction, high resolution transmission electron microscopy and scanning transmission electron microscopy (Z-contrast) X-ray diffraction and high resolution transmission electron microscopy confirmed the single crystalline nature of these films with cubic-on-cubic epitaxy. The epitaxial relations follow TaN(111)||TiN(110)||Si(100) and TaN(111)||TiN(110)||Si(111). We observed sharp interfaces between the super lattice of TaN/TiN and TiN/Si without any indication of interfacial reaction. We checked the diffusion barrier characteristics of these films by growing a thin layer of copper on the top and subsequently annealing the films at 800°C. Even after annealing for 30 minutes we did not observe any diffusion of copper in the system. Rutherford backscattering experiments showed these films to be slightly nitrogen deficient [TaN\_0.9]. High precision electrical resistivity measurements showed excellent metallic nature of these films. We also tried to deposit TaN directly on silicon, the films were found to be polycrystalline. In our method, TiN plays a key role in facilitating the epitaxial growth of TaN. This method exploits the concept of lattice matching between TaN and Si, which is achieved by introducing a buffer of TiN on top of TaN and Si. This work opens a promising way to grow high quality TaN diffusion barrier on silicon for copper interconnection.

10:30 AM DB.9
MICROSTRUCTURAL EVOLUTION OF THE INITIAL PHASE FORMATION OF COBALT SILICIDE WITH AN ULTRA-TIN TITANIUM UNDERLAY. Kevin D. Johnson, Julie Tan, Zhiyang Mo, Intel Corporation, Hillsboro, OR; Ken Sin Sim, Intel Corporation, Penang, MALAYSIA.

Co silicide has been a prominent candidate for deep sub-micron process technology because of its low resistivity and scalability. This work investigates ultra-thin Ti underlayer assisted mediation of the phase formation for cobalt silicide and addresses the role of Ti in the various stages of the phase evolution. The Ti co-sputtered as a sputtered deposit as a thin (20 Å) amorphous layer prior to Co deposition. A rapid thermal anneal (400°C-550°C) is then implemented to initiate silicidation. Although the reaction sequence for Co silicide is Co + CoSi\_2 + Co\_3Si\_2 + Co\_5Si\_4, the inter diffusion of Co underlayer after allowing Co\_3Si\_2 to form directly below the Ti underlayer and a more Co-rich phase to form above the Ti underlayer. The thickness of the Ti underlayer also alters the initial phase formation and the reaction path for Co silicidation. By using EXAFS, theoretical kinetics, there are practical advantages for Ti underlayer that mitigate some of the difficulties of silicide processing.

10:45 AM DB.10
A STUDY OF LEAKAGE CHARACTERISTICS IN SILICIDED SHALLOW JUNCTIONS USING TRANSMISSION ELECTRON MICROSCOPY (TEM). Tae-Yoon Song, Min-Soo Chung, Department of Materials Science and Engineering, Kwangju Inst of Science and Technology, (K.I.S.T.), Kwangju, KOREA; Key-Min Lee, Joo-Hyoung Lee, Young-Jin Park, Memory R&D Div, Hynix Semiconductor Inc, Cheongju, KOREA; H-Dook Lee, Dept of Electronics Engineering, Chungnam National Univ, Taejon, KOREA.

A cobalt self-aligned-silicide process has been widely used to realize high performance ultra-large-scale integrated (ULSI) circuits. As the dimension of ULSI devices continues to scale down, a junction leakage problem caused by a Co-silicidation process can be a key issue for the fabrication of next generation integrated circuits. However, the precise leakage model remains still unclear due to the complex characteristics of the junction leakage. In this work, two-dimensional [2D] junction profiling using transmission electron microscope [TEM] combined with a selective chemical etching & used to investigate the junction leakage mechanism in p+/n+ and n+/p+ shallow junctions which were fabricated using the Co-silicidation process. To directly reveal 2D profiles in the junctions, ion-milled cross-section thin foil specimens are chemically etched using a mixture of HF, HNO\_3, and CH\_3COOH. TEM and TSUPREM4 simulations reveal that a decrease in the Si intermixing near the edges of the active regions causes junction profiles to bend upward near the active edges, namely, the formation of shallower junctions in these regions. Based on the TEM and electrical results, it is suggested that the n+/p+ junction profiles near the edges of the active regions could be a main cause for the junction leakage in the silicided perimeter samples with the p+/n+ junctions.

11:00 AM DB.11
ON THE MORPHOLOGY CHANGES OF Ni AND Ni(Pt); ON THE Ni/Pt INTERFACE. Poo Se Lee, Dept of Material Science, Keimyung University, Dept of Electrical and Computer Engineering, National University of Singapore, SINGAPORE; Dominique Mangelinck, L2MP-CNRS, FRANCE, Jun Ding, Dept of Material Science, Deng Zhi Chi, Institute of Materials Research and Engineering, SINGAPORE; Thomas Ospinoz, Dept of Physics, National University of Singapore, SINGAPORE; Alex See, Charterd Semiconductor Manufacturing, SINGAPORE.

NiSi is a promising silicide material due to its step low temperature formation, low resistivity and low Si consumption. To enhance the phase stability of NiSi, addition of Pt has been shown to form Ni(Pt)Si up to 900°C [1]. The application of Ni(Pt)Si onto silicon devices at silicidation temperatures above 700°C has also been demonstrated [2]. The issue of agglomeration and layer inversion has remained critical since conductivity of thin silicide films is sensitive to the degradation of the film morphology. The purpose of this work is to study the morphology degradation that includes agglomeration and layer inversion of NiSi and Ni(Pt)Si. Rutherford Backscattering Spectroscopy (RBS), Scanning Electron Microscopy (SEM), Cross Transmission Electron Microscopy (XTEM) and electron diffraction analysis were employed. Layer inversion leads to the reversal in position of polycrystalline silicon (polysilicon) and Si. It was found that the addition of Pt has led to an improvement in the agglomeration behavior of NiSi but have little influence on the layer inversion on the undoped polysilicon. Suppression of layer inversion was attained by silicidation on Phosphorus doped polysilicon or with the use of thin Ni(Pt) (~10 nm). The agglomeration behavior and layer inversion are discussed in terms of the controlling factors of grain boundary energy and interfacial energies. [1] D. Mangelinck, H. Y. Dui, J. S. Pan and S. L. Khiri, Appl. Phys. Lett. 75 (12), 1736 (1999). [2] P.S. Lee, K.L. Pey, D. Mangelinck, J. Ding, D.Z. Chi, L. Chen, Electron Dev. Lett., to be published in Dec, 2001.

11:15 AM DB.12

We have recently observed the formation of severe damage in Cu interconnects during in-situ testing in an SEM with 100 Hz alternating current. Room temperature current injection appears as surface wrinkles within single grains, which grow in amplitude and extent,
and eventually lead to electrical failure of the lines. The damage bears no resemblance to typical electromigration damage generated by DC test conditions and is probably caused by thermal fatigue. Because of Joule heating in the interconnects, the alternating currents used in these studies (rms 10-15 mA/c㎡) generate temperature swings as large as 150°C which cause thermal mechanical strain cycles and the formation of fatigue damage within as few as 10^6 cycles. The formation of the fatigue damage is not hindered by the presence of soft encapsulating films, such as a polymer-based low-k dielectric. Since the temperature swings generated by the tests are not much larger than those expected in devices during normal operation, thermal mechanical fatigue may become a serious reliability threat in Cu-based devices with soft interlevel dielectrics. We will present results on the effect of the current density (or temperature amplitude), grain orientation, and encapsulating layers on the formation of fatigue damage and the time to cause an electrical failure. In addition, the damage accumulation process, including the formation of cracks, will be described.


Presently, most modeling and experimental analyses for circuit-level interconnect reliability focus on straight-stub-to-stub test lines. However, in reality, multiple segments of straight lines are connected in junctions in interconnect circuits. An interconnect tree has been defined as a unit of continuously connected high-conductivity metal lying within one layer of metallization. Standard reliability assessment methods are based on analysis of individual segments, using the results from straight-junction-free lines rather than trees. This method is generally inaccurate as material within an interconnect tree can diffuse freely among connected segments and the stress evolution in different segments of a tree is coupled. Tree-based experiments and assessment methodologies have been developed for Al-based interconnects. However, experiments have not been previously carried out on Cu-based interconnect trees. Electromigration experiments have been carried out on simple Cu dual-damascene interconnect tree structures consisting of straight-stub-to-stub lines with an extra via in the middle of the line. As with Al-based interconnects, the reliability of a segment in this tree strongly depends on the stress conditions of the connected segment. Beyond this, there are important differences in the results obtained under similar test conditions for Al-based and Cu-based interconnect trees. These differences are thought to be associated with variations in the interconnect schemes of the two materials, and may relate to a combination of an interconnect material with a different stress-rupture curve in Cu technology, and the possibility of liner rupture at stressed vias, leading to important differences in tree reliability in Cu compared to Al. Although liner rupture may increase the reliability of the structure, it may also lead to a breakdown of the circuit. This work demonstrates that while segments are not the fundamental reliability unit for circuit-level reliability assessments for Al or Cu, trees, rather than trees, might be the appropriate fundamental units for assessment of Cu reliability.

11:45 AM B8.14 COMPARISON OF TiN THIN FILMS DEPOSITED BY METAL ORGANIC ATOMIC LAYER DEPOSITION (MOALD) USING TDMA AND TDEAT, Ju Youn Kim, Sang Won Seo, Jin Young Park, Yungdo Kim, Young Do Kim and Hyongtak Jeon, Division of Materials Science and Engineering, Hanyang University, Seoul, KOREA.

Among the transition metal nitrides, titanium nitride (TiN) has been widely used as a diffusion barrier in ultra large scale integrated devices. Barrier layers were deposited predominantly by the physical vapor deposition (PVD) and chemical vapor deposition (CVD) techniques, but they suffer from the poor step coverage and have limited their applicability in the new generation of integrated circuits with very high intermetal dielectric dielectric constant materials. Atomic layer deposition (ALD) is a new deposition technique to improve the combined problems of PVD and CVD methods. Many researches have been carried out to grow TiN, mainly using halide precursors, by ALD methods. However, the method using halide precursors has some problems such as very low growth rate and high chlorine contents which makes ALD difficult to be applied in an industrial device process. Therefore, in the recent, many experiments have been performed to alternate halide precursors with metal organic precursors. In this study, TiN films grown by metal organic ALD (MOALD) method using tetraethyl(dimethyl)amino-titanium (TDMA) and tert-butyl(dimethyl)amino-titanium (TDEAT) as Ti precursor and NH3 as reactant gas were investigated. The physical, chemical and electrical properties of TiN films grown by MOALD using TDMA and TDEAT precursors have been systematically analyzed and compared.

SESSION B9/CE JOINT SESSION CHARACTERIZATION OF SURFACE ANALYSIS TECHNIQUES

Chair: Daniel F. Downey and Janice L. Veteran
Thursday Afternoon, April 4, 2002
Salon 10-12 (Merriott)

1:00 PM B9.1/CE.1 ROUTINE Dopant/Impurity and Stoichiometry CHARACTERIZATION of SiGe and SiON USING SURFACE ANALYSIS TECHNIQUES, Charles W. Magee, Evans Estes, [A Member of the Evans Analytical Group], Fort Windsob, NJ.

A critical technological benchmark of the SiGe HBT is its maximum oscillation frequency fmax, which is dependent on the base sheet resistance of the transistor. Reduction of the base sheet resistance results in a higher operating frequency. However, the peak boron concentration in the base is limited by boron out-diffusion. Incorporation of carbon into the SiGe has been shown to reduce this out-diffusion. 1-2 These properties are characterized for SiGeC using SIMS characterization for measuring the changes in the B distribution with growth and anneal, as well as determining the substitutional C concentration. The depth profile characterization by SIMS however, demands carefully set analytical protocols involving standards calibrated by other techniques for accurate quantification. In addition, the requirement to measure layer thicknesses or junction depths makes achieving good depth resolution during the analysis also important. A high dose C implant across the interface between an RBS-calibrated, B-doped SiGe epi layer and the Si wafer substrate was prepared as a quantification reference material to characterize SiGeC epilayer films. The protocol developed using a series of SiGe samples implanted with various elements and concentrations determinations for these elements with an accuracy of 5±10%. Several experimental conditions show that a low energy oxygen primary ion beam has to be used to measure an accurate B distribution in the sample, which is often used to determine the base layer thickness. Although C primary ion bombardment allows the accurate quantification of total B, C, O, P and Ge, using ion yield corrections, in a single analysis for cost effectiveness, the oxygen bombardment is necessary to obtain better depth resolution. A second part of this presentation focuses on silicon oxynitride-SiON gate dielectrics. As the thickness of these gate dielectrics is reduced, the demands on the analytical techniques used to characterize these films have increased. The characterization of the SiON films, which currently range from 1-5nm thickness and 1-25 atom% N, necessitates a combination of near surface characterization techniques and reference materials. Currently, Nuclear Reaction Analysis (NRA) is used in the calibration of reference materials. NRA is used to generate total N concentration and thickness using these reference materials, and SIMS is used in combination with results of XPS to determine the nitrogen distribution.


SESSION B10: OXIDES AND SILICIDES

Chair: Janice L. Veteran
Thursday Afternoon, April 4, 2002
Salon 10-12 (Merriott)

1:45 PM B10.1 CONTROLLED SIO/NITRIDE THICKNESS USING ADAPTIVE REAL-TIME TEMPERATURE CONTROL, John Gunther, Tokyo Electron America, Diffusion Systems, Richardson, TX, Wayne Bather, Darin Weidel, Texas Instruments, Silicon Technology Development Group, Dallas, TX.

A novel method to achieve very uniform thick silicon nitride depositions using dichlorosilane and ammonia is demonstrated in a LPCVD batch furnace system. Adaptive real-time temperature control, coupled with model-based process temperature optimization, can significantly improve both wafer-to-wafer and within-wafer silicon nitride thickness uniformity. Improvement in within-wafer thickness uniformity is achieved by thermal ramping during deposition. The
resulting across wafer thermal gradient offsets the effects of preferential edge deposition on within-wafer thickness uniformity. Accurate estimation of thermal pointwise and silicon nitride deposition rate dependence on temperature and process chemistry allow for precise calculation of temperature setpoints for best uniformity. Both of these requirements are met using Adaptive Real-Time Temperature control and associated nitride deposition models. The ability of current vertical LPCVD batch reactors to precisely control process temperatures, even during ramping, insures repeatable results. Typically, additional test runs are required to qualify silicon nitride deposition processes and times increases when Adaptive Real-Time Temperature control is utilized. However, Adaptive Real-Time Temperature control is intended for critical processes, where demand for film thickness specifications, where batch sizes must be reduced to achieve acceptable thickness uniformity. The use of Adaptive Real-Time Temperature control allows acceptable film thickness uniformity to be achieved over the entire furnace load area and ultimately increases process throughput.

2:00 PM B10.2
Si/SiO2 INTERFACE ROUGHNESS STUDY BY SCANNING TUNNELING MICROSCOPY. Jien Xu, Logan Li, Thomas W. Schrock, William M. Marisfled*, Gregory L. Temp, and Joseph W. Lyding, Beckman Institute, University of Illinois, Urbana, IL; *Agere Systems, Murray Hill, NJ.

There is a tremendous interest in determining the Si/SiO2 interface roughness, which is believed to account for the degradation of the effective mobility of an inversion layer at high transverse field. Two parameters are used to characterize the interface roughness: the rms-roughness, and the correlation length . For the first time, we demonstrate that ultrahigh vacuum scanning tunneling microscopy (STM) can be used to directly examine the Si/SiO2 interface and extract the rms-roughness and correlation length from the topography. The rms-roughness can be determined from the Gaussian fit of the height distribution, and the correlation length is determined from an exponential fit to the in-plane autocorrelation function. A smooth wafer and a rough wafer have been examined, both with a normally 

2:15 PM B10.3
TRANSPORT PROPERTIES OF HETEROSTRUCURE SrTiO3 / Al2O3 / ZrO2 on Si. Julie D. Caperci, Harry A. Atwater, California Institute of Technology, J. douglas bell, J. propulsion laboratory, Pasadena, CA; Brett W. Busch, Lilina Menchavez, Martin L. Green, Agere Systems, Murray Hill, NJ.

Among the main performance limits of floating gate nonvolatile memory devices, such as flash memories and nanocrystal memories, are the long program time ( >1ms) and erase time ( >1ms) achievable via a Fowler-Nordheim tunneling mechanism. These limits are due to the floating gate through a homogeneous tunnel barrier. An interesting alternative to homogeneous dielectric tunnel barriers is a silicon compatible layered tunnel barrier, which enables a large drop in the barrier height with applied voltage. We have correlated dielectric constant and band offsets with respect to silicon in order to help identify possible materials from which to construct these layered barriers. Based on this survey, we have determined that some of the most promising materials are SiO2/Al2O3/Si3N4 and SiO2/Al2O3/ZrO2/Si3N4. We have fabricated the metal-insulator-semiconductor layered barrier structure of Si3N4/Al2O3/Si3N4 on silicon. The Si3N4 was made by low-pressure chemical vapor deposition (LPCVD) at 800°C. The Al2O3 was made by atomic layer deposition using sequential exposures of trimethylaluminum and H2O at 300°C. High-temperature annealing was found to greatly reduce the leakage currents and thus enhance the barrier lowering. We have also fabricated single-layer barriers of Al2O3 and double barriers of SrTiO3/Al2O3 and SrTiO3/Al2O3/SrTiO3/Al2O3/SrTiO3. A comparison of the current-voltage (LV) and capacitance-voltage (CV) characteristics of these structures will be discussed. The LV measurements that were performed on dielectrics that were deposited on degenerately doped n+ and p+ silicon in order to minimize band-bending. To assess the electrical performance of our layered tunnel barriers, we performed simulations of their temperature dependent current-voltage characteristics. Tunneling probability simulations for layered tunnel barriers are performed using an effective-mass model. With this theory we are able to predict the LV curves for our tunnel barriers and can determine if barrier lowering has been achieved. In addition to electron and hole currents, tunneling characteristics, values of the band offsets for Al2O3 and ZrTiO4 relative to n-type silicon will be presented. These values are found by

3:00 PM B10.4
DIFFUSION CHARACTERISTICS OF COPPER IN TiN THIN FILMS. Abdullah Gogus, Alex V. Keiz, Gerd Discher and J. Narayan, NSF Center for Advanced Materials and Smart Structures, Department of Materials Science and Engineering, NCSU, Raleigh, NC.

We have investigated the diffusion characteristics of copper in nanocrystalline, polycrystalline and single crystal TiN thin films, which is being used as a diffusion barrier for sub-quarter-micron metalization. These films were crystallized on Si < 100 substrate by first ablating smooth TiN and then ablating amorphous copper targets using Pulse Laser Deposition. The three different crystalline structures of TiN were achieved by growing the films at different substrate temperatures, where the higher temperatures (~700°C) result in formation towards epitaxy. Then a uniform thin layer of copper was deposited at room temperature for all the three deposition samples. Each sample is annealed at three different temperatures (400°C, 500°C and 600°C) to study the diffusion barrier characteristics of TiN. Study of diffusion profile and the copper concentration measurement were performed using Scanning Transmission Electron Microscopy- Z contrast (0.1nm resolution). Secondary Ion Mass Spectroscopy, Electron Energy Loss Spectroscopy and Rutherford Backscattering Spectroscopy techniques. These data were used to plot the measured concentration of copper with respect to the temperatures for the three crystalline structures of TiN to calculate the diffusion coefficients and were compared to study the effects of microstructure on diffusion of TiN film on the diffusion of copper after annealing.

3:15 PM B10.5
EFFECT OF AN APPLIED Ti LAYER ON CoSi2 SALICIDE FORMATION. G.Y. Lang, H. Chang, S.A. Pruszynski and Y. Roh,M-Sumii, University at California at Los Angeles, Dept. of Electrical Engineering, Microelectronics Laboratory, Los Angeles, CA.

Integration of self-aligned metal silicide into metal-oxide-semiconductor transistor technology nodes is crucially difficult in order to achieve low sheet/contacts resistance on ultra-shallow junction source/drain as well as narrow gate. CoSi2 silicide, in comparison with TiSi2 and NiSi, is advantageous in terms of low sheet resistance, independent formation of narrow gate width, suitable formation temperature control in ultra-shallow junctions and thermal stability as well as readily epitaxial growth to improve contact resistance. We studied extensively the formation of ultra thin CoSi2 silicide with/without an applied Ti mediating or capping layer by using rapid thermal and isochronal annealing in N2/ambient. Four-point-probe sheet resistance measurements and electron microscopy were used to characterize the ultra thin silicide films as well as their formation kinetics. We found that the formation temperature of CoSi2 and CoSi3 as well as their existing duration are strongly influenced by the presence of an applied Ti mediating or capping layer. Under Ti capping, Co directly reacts with the substrate in a way similar to a single layer Co silicidation. However, Ti capping favors the formation of CoSi and the diffusion of Ti from the capping layer delays the phase transformation of CoSi into CoSi2 from 525°C to 675°C. An applied Ti mediating layer acting as a diffusion barrier suggest that the supply of Co so that it limits the formation of high Co concentration silicide CoSi but favors that of low Co concentration silicide CoSi2 under a Co diffusion-controlled process. Electron microscopy studies indicate that CoSi2 formed with an applied Ti mediating layer exhibits better epitaxial characteristics.

3:30 PM B10.6
FUNDAMENTAL BEAM STUDIES OF RADICAL ENHANCED ATOMIC LAYER DEPOSITION OF TITANIUM NITRIDE. Frank Greer, D. Fraser, J.W. Coburn, and David B. Graves, U.C. Berkeley, Dept of Chemical Engineering, Berkeley, CA.

Atomic Layer Deposition (ALD) has been proposed as one way to deposit highly conformal thin films for copper diffusion barriers due to the self-limiting, layer-by-layer growth that can be achieved with this technology. One problem with thermally activated ALD is that the deposition temperatures that are required to achieve reasonable growth rates and good quality films with low impurity concentrations can be relatively high. This may make the integration of these barrier films with future high-performance transistors, such as magnetic low temp, impossible. One potential alternative to thermal ALD is to use more reactive species such as radicals to catalyze film deposition at lower substrate temperatures. In this work, TiN films are deposited using Radical Enhanced Atomic Layer Deposition (HEALD) to electro-deposition levels of 100 nm and beyond by feeding hydrogen and/or nitrogen radicals with or without additional pulses.
of Ni3S. By directing independent beams of each of these species at a given surface, this experiment silicon coated on Quartz Mill Powder of interest such as the sticking and reaction probabilities of these species have been measured as a function of surface temperature, and will be used to predict the conformality of films deposited using RE-ALD in features of arbitrary aspect ratio. Raman XPS analysis of the deposited films will be presented, paying particular attention to the low residual chlorine content that can be achieved with sufficient hydrogen radical exposure (≤0.5%) at deposition temperatures as low as 100°C. In-situ Anger Electron Spectroscopy measurements will be presented from different stages during the deposition process. Various measurements of the film quality will also be presented including the films’ resistivity and crystallinity.

3:45 PM B10.7
NICKEL, PLATINUM and ZIRCONIUM GERMANOSILICIDE CONTACTS TO ULTRA-SHALLOW, P+ N JUNCTIONS FORMED BY SELECTIVE SiGe TECHNOLOGY FOR CMOS TECHNOLOGY NODES BEYOND 70NM Jing Liu, Hongxing Mo, Mehmet C. Ozurk, North Carolina State University, Department of Electrical and Computer Engineering, Raleigh, NC.

One of the key challenges for future CMOS technology nodes beyond 100 nm is formation of ultrashallow junctions with a series resistance contribution limited to five percent of the channel resistance. The future junctions are expected to possess extremely low sheet, contact and spreading resistance values requiring fundamentally different methods for junction and contact formation. Recently, this laboratory reported a new technology based on selective deposition of doped SiGe alloys in such a fine grain resolution as shown in Figure 1, which is a key advantage reducing the contact resistivity for future technology nodes. In this paper, we present our recent results on Pt and Ni germanosilicide contacts to + SiGe. We show that both contacts can provide a resistivity near 10−8 Ω·cm2 needed for technology nodes beyond 70 nm. However, the stability of the materials were found to be limited to ~550°C for Ni and ~800°C for Pt. This was attributed to Ge departure from germanosilicide to segregate either at the grain boundaries or to the metal-junction interface. Zr was proposed as an alternative germanosilicide for better stability. Another possibility, considered for the first time here is the use of a thin Zr layer as an intermediate layer between Pt or Ni and the junction. The films were characterized by four-point-probe, XRD, SIMS and AFM. The results indicate that both Zr alone or Zr with Pt and Ni are viable contact materials to + SiGe. Using Zr alone results in a ternary germanosilicide with good stability at least up to 900°C. Using Zr as an intermediate layer improves the stability by retarding the Ge loss from the germanosilicide.

4:00 PM B10.8
MICROSTRUCTURE AND ELECTRICAL PROPERTIES OF Cu/TiN INTERFACE FOR CMOS COPPER INTERCONNECTION Qi Wang, Qinggao Tao, Tong Wang and Chumei Chen, Tongji Nonferrous Metals Shanghai Company, Shanghai, PRC; Xiaomin Guan, MIT, Dept of Materials Science & Eng, Cambridge, MA.

The interface between Cu and barrier layer is important key to the CMOS copper interconnection. An ideal interface of Cu/Barrier metal has to be developed to form a uniform homogeneous copper layer in order to suppress the interfacial electromigration of copper. In this study, a TiN liner with a thickness of 800 Å was deposited onto a typical dielectric SiO2 layer using conventional Physical Vapor Deposition technique. On the barrier layer, a 200 Å Cu layer was then, sputtered at room temperature. Afterwards, low temperature annealing for Cu/Barrier metal interface was carried out at 350 to 550°C for 30 to 60 minutes in order to form a uniform interface and to reduce residual stress in the layers formed during deposition. We have systematically studied the wetting and agglomeration of copper layer on TiN substrate and the texture of Cu film using Transmission Electron Microscopy (TEM) and X-ray Diffraction (XRD). It was found that the better wetting interface and less copper agglomeration occurred during low temperature annealing, and the roughness of the Cu/TiN interface increased with the annealing temperature. It was also found that the [111] copper texture formed during deposition and the degree of the texture decreases with increasing of annealing temperature and time. The result showed that the electromigration of copper in CMOS interconnects was related with the microstructure of Cu/barrier interface, in this paper with the annealing procedures. The relationship between electromigration resistance and texture degree of copper is reported in this paper.

SESSION B11: POSTER SESSION
METALS AND MODELING
Thursday Evening, April 4, 2002
8:00 PM
Sala I-7 (Moskito)

B11.1
MICRO-RAMAN SPECTROSCOPIC STUDY OF NICKEL SILICIDE FILMS. S.K. Dhanuka, D.Z. Chi, S. Tripathy*, A.S.W. Wong and S.J. Chua, Inst of Materials Research and Engineering, Singapore, SINGAPORE; *Centre for Optoelectronics, Singapore, SINGAPORE.

Micro-Raman technique was used to investigate vibrational properties of NiSi thin films formed on three different substrates: unimplanted (100) Si, 20keV BF2+ implanted (100) Si, and 20keV BF2+ implanted (100) Si. Nickel films, 30nm thick, were deposited by sputtering technique and were subsequently rapid thermal annealed for 60 sec at 500-800°C for silicidation. Secondary ion mass spectroscopy was employed to study dopant redistribution during silicidation. Raman spectroscopy was performed in backscattering geometry corresponding to either z(e)-z(x)-y or z(y)-z(x)-y configuration. Raman spectroscopy was also performed on NiSi powder to identify various phonon modes associated with different silicon rules of group theory. Eight characteristic phonon peaks of NiSi phase were identified of which four at 214 cm−1, 288 cm−1, 306 cm−1 and 319 cm−1 are assigned to A3 phonon modes, the two at 197 cm−1 and 335 cm−1 to B1g phonon modes and the remaining two at 295 cm−1 and 341 cm−1 to either B2g or B3g phonon modes. It was found that Raman peaks of NiSi thin films formed on BF2+ implanted substrate were broader and shifted to lower frequency side compared to films formed on other substrates. The broadening of the Raman peaks in these films, which also exhibit much improved thermal stability, is attributed to small grain resulting probably from fluorine segregation to grain boundaries and interface. SIMS analysis showed that fluorine progressively segregates to silicon in the substrate with a concentration of about 1.3 at.%. It is proposed that in addition to grain boundary segregation, some structural modification in silicide film is induced by the presence of excess fluorine inside the grains, resulting in shift of phonon peak positions.

B11.2
Abstract Withdrawn

B11.3
OPTIMIZATION OF ULTRATHIN ALD TANTALUM NITRIDE FILMS FOR ZERO-THICKNESS LINER APPLICATIONS. Osamu van der Steen, Yu Zhou, Fer van Eerdenwegen, Alain Kegelers, ULfamy Institute for Materials, Albany, NY.

A metalorganic atomic layer deposition (ALD) tantalum nitride process has been demonstrated for zero-thickness liner applications in advanced copper metallization schemes employing a commercial ALD reactor. This process employs a liquid tantalum source (tetrabutyltitanooctylammonium tetrafluoroantimonic acid - TBDET) and ammonia as the reactants. Key functionality data addressing the self-limiting nature of ALD film growth with respect to key process parameters including substrate surface exposures to TBDET and ammonia will be presented. Surface roughness data as well as conformality data of ALD tantalum nitride in high aspect ratio structures as measured by atomic force microscopy (AFM) and transmission electron microscopy (TEM), respectively, will also be presented. Results of research to evaluate the barrier performance of thermally and bias stressed Cu/ALD tantalum nitride stacks using both compositional and electrical measurements will be discussed, as well limiting barrier thickness metrics and determination of the barrier failure mechanisms.

B11.4
THE USE OF CV TECHNIQUES TO INVESTIGATE INSTABILITY MECHANISMS IN Ni-SI Structures. S. Paul, W.I. Milne and J. Robertson, Engineering Department, Cambridge University Cambridge, UNITED KINGDOM.

In the field of flat panel displays, the current leading technology is the Active Matrix Liquid Crystal Display; this uses n-Si based thin film transistors (TFT) as the switching element in each pixel. However, under gate bias n-Si H TFT’s suffer from instability, as evidenced by a shift in the gate threshold voltage. Two possible sources of this instability are the creation of midgap states in the n-Si channel and charge trapping in the gate insulator. The shift in the gate threshold volt age is generally measured from the gate transfer characteristics, after subjecting the TFT to prolonged gate bias. However, a major drawback of this measurement is that it cannot distinguish whether the shift is caused by the change in the midgap states in the n-Si channel or by charge trapping in the gate insulator. In view of this, we have developed a capacitance-voltage (C-V) method to measure the shift in threshold voltage. We employ Metal-Insulator-
Semiconductor [MIS] structures to investigate the threshold voltage shift as they are much more simple to fabricate than TFTs. We have investigated a range of number $\text{AlSiN/AlN/SiO}_2$ and $\text{AlN/AlSiN}/\text{SiN}/\text{SiO}_2$ structures using our C-V technique. From the C-V data for the MIS structures, we have found that the relationship between the thermal energy and threshold voltage shift is similar to that observed by Webber and Khilko [Appl. Phys., 144, 87, 2000]. The $\text{AlN/AlSiN}$ layers were grown using radio-frequency plasma-enhanced chemical vapour deposition and the $\text{SiO}_2$ was deposited thermally.

**B1.15 CHARACTERIZATION OF THE ELECTRONIC STRUCTURE OF SiC/METAL INTERFACES USING PHOTOELECTRON SPECTROSCOPY**

John J. Bokros, John T. Watson, and Stephen E. Sadow, Dept. of Physics, University of California, San Diego, CA.

By using the new technique of electron energy-loss spectroscopy (EELS) we have been able to determine the electronic structure of the SiC/Metal interfaces. The EELS results show that the interface states are localized at the SiC/Metal interface and that the Fermi level is pinned at the interface. The EELS results are in good agreement with the theoretical calculations.

**B1.16 INTERFACE SLIDING IN BACK-END INTERCONNECT STRUCTURES AND ITS MECHANISM**

K. A. Peterson, C. Park and I. Dutta, Center for Materials Science and Engineering, University of California, Berkeley, CA.

High strains can develop in back-end interconnect structures (BEIS) of micro-electronic devices during thermal excursions because of the large differences in thermal expansion coefficients (TEC) between Si, the interlayer dielectric (ILD) and the interconnect lines. These stresses may induce local plasticity, creep or interfacial sliding within the interconnect structure. These effects are expected to become more prevalent as the circuit density increases. In this study, we have investigated the effect of the interconnect line on the mechanical properties of the BEIS. The AFM measurements demonstrated that the interconnect lines are accommodated by diffusionally-controlled interfacial sliding in the interconnect structure, resulting in a higher strain limit. Further, studies of the cross-sections showed evidence of dislocation due to interfacial sliding. To understand the mechanism of interfacial sliding, creep experiments were conducted on model planar interfaces between Al and Si. The kinetics of diffusionally accommodated sliding at an interface with the Si substrate was determined. A creep law was proposed to explain this phenomenon. The results suggest that diffusionally-controlled sliding may be responsible for the observed phenomena.

**B1.17 ELECTRONIC TRANSPORTS ACROSS POROUS/CRYSTALLINE SILICON HETEROJUNCTIONS**

M. N. Islam, Sunjoy K. Ram, Satyendra Kumar, Dept. of Physics, Indian Institute of Technology, Kharagpur, INDIA.

The understanding of electronic transport properties of porous silicon (PS)/crystalline silicon (c-Si) heterojunctions is crucial in improving the efficiency of these devices. In this study, we have investigated the electronic transport properties of PS/c-Si heterojunctions by studying the current-voltage characteristics of a series of PS/c-Si heterojunctions. We found that the current-voltage characteristics are determined by the interband transitions between the conduction and valance bands in the PS and c-Si. The PS/c-Si heterojunctions showed rectifying behavior with a rectification ratio of about 500 for a bias of about 1 V. The rectification ratio was found to increase with an increase in the bias voltage.

Finally, we have investigated the effect of the PS/c-Si heterojunction on the electronic transport properties of PS/c-Si heterojunctions. We found that the PS/c-Si heterojunction reduces the rectification ratio significantly.

The temperature of the surface of the chip used in VLSI/SLSI undergoes (BSI, 1990) a periodic variation by virtue of the fluctuations in the current passing through as a result of the anharmonic interactions. Take the surface of the board to be a plane we find the expression for $u(T - T_{max})/(T_{max} - T_{avg})$ as a function of $T$, $t$ (the time measured after $T = T_{max}$ at $t = 0)$, and $w$ (the frequency of fluctuations that are assumed to be sinusoidal). By postulating a solution in the form of complex temperatures and using separation of variables, DeMoivre’s theorem the real part of the temperature may lend itself to an expression for $T$. However, the sinusoidal equations that are used in this problem imply a infinite speed of propagation of heat. This can be corrected by the hyperbolic wave propagation equations. Using the hyperbolic partial differential equations the
expression for $u$ is derived. These solutions are compared with each other and significance discussed.

**B1.11**
EVALUATION OF CONTACT AND VIA STEP COVERAGE USING A NOVEL TWO-STEP TITANIUM NITRIDE BARRIER DEPOSITION PROCESS

Andy Smith, Chad Simpson, Todd Gandy, STM Microelectronics, Inc., Phoenix, AZ; William Brown, Simon Ang, and Richard Ulrich, University of Arkansas, Department of Electrical Engineering, Fayetteville, AR.

Aluminum plug technologies are still used for many different semiconductor device applications and are cost-effective processes. However, there are some disadvantages associated with them. The key disadvantage is aluminum junction spiking caused by aluminum diffusing down into the silicon substrate and silicon diffusing up into the aluminum plug, due to a poor titanium nitride (TiN) barrier. The tungsten plug process is mainly used for 0.5-mm and smaller technologies. Material properties play an important role as an underlayer for tungsten plugs to prevent the tungsten hexalfluoride (WF₆) from attacking the titanium (Ti) film. The role of the TiN barrier is to retard or prevent diffusion of the materials that the TiN layer separates. All TiN barriers are not perfect and have limited thermal budgets. Some TiN barriers may not be suitable as via levels because of high deposition temperature or chemistry. In this work, the authors investigated the TiN barrier film properties with respect to nitrogen flows at two different power set points and argon gas flows. Different experiments were performed to understand the properties of the TiN film with respect to process variables. Changes in stress of different TiN barrier films were recorded for different process parameters, process powers, and chamber pressures. Also, the impact of Rapid Thermal Anneal (RTA) processing on the stress behavior of different TiN barrier films was analyzed. This work represents a significant shift of the TiN barrier stress in the results of studying and reinitiating the deposition process. The shift in the columnar grains acts as a trap for any interdiffusion through the grain boundaries. Furthermore, the dual- or two-step barrier process provides a thinner sidewall and bottom TiN step coverage than a standard one-step barrier process, particularly for high aspect ratio conditions for contact and via openings.

**B1.12**
SOLUTION-BASED PRECURSOR DELIVERY FOR COPPER CVD

Libong Wang, Greg Griffin, Louisiana State University, Dept of Chemical Engineering, Baton Rouge, LA.

We have measured the growth rates for copper CVD using Cu(III)Cl₂ dissolved in isopropyl alcohol as the precursor delivery method. This approach offers the convenience and control associated with liquid precursor delivery, while avoiding the high melting point of this precursor. The new method provides similar growth rates to those observed using conventional delivery (i.e., sublimation of solid precursor), but these rates are achieved using a much lower partial pressure of precursor in the reactor. The deposition rate is initially first-order with respect to precursor pressure, but saturates at high values. The rate is also first-order with respect to hydrogen partial pressure. Increasing the hydrogen pressure also shifts the rate at which precursor pressure becomes an important factor. The isopropyl alcohol added forms a smaller, more complex and more effective film on the kinetic. Measurements of surface roughness and film resistivity indicate that the initial films are discontinuous (i.e., for film thickness less than 100 nm). The film properties also do not appear to depend strongly on the gas phase reactant composition. These results suggest that the surface diffusion is primarily responsible for initial film morphology.

**B1.13**
POSSIBLE RELATIONSHIP BETWEEN FERMION LEVEL PINNING AND INDUCED NET CHARGE DENSITY AT NON-INTIMATE METAL/SILICON INTERFACE

Bruce Cudell, Faculty of Civil Eng., University of Maribor, Maribor, SLOVENIA; and Stefan Institute, Ljubljana, SLOVENIA.

It has been shown recently that the reverse biased excess capacitance of various capacitor processes, such as sideways, check-spaced, and inverted structures, is due to the manifestation of the existence of the net charge density as induced at the appropriate interface. This net charge density has been shown to be external field dependent and its magnitude appears to be strongly related to the net charge density at the metal-semiconductor junction formation. The induced, interfacial net charge density, provides the basis for the calculated effective density of states, EDOS, of the pertinent charge carriers, respectively. The deduced net charge density is characteristic of the chemical composition at the interface, extends over the semiconductor energy gap and is characterized by sharp spikes. The amplitude of spikes is periodically modulated and their envelopes appear as identical, krypton-like patterns. The number of krypton-like patterns is finite and uniformly distributed over the energy gap, however the spikes density within each krypton monotonically increases on approaching the conduction band minimum. In this work the question is to what extent the above described spikes and krypton density, effective density of gap states at the metal-semiconductor interface, could be associated with the Fermi level pinning position in silicon will be examined. In this respect the correlation of various published values of Schottky barrier heights for Ag and Pb metal contacts with EDOS, has been investigated. The peaks of the calculated EDOS values are also for this reason that the findings are to be compared with the Drummond's [2] predictive model for various near surface defects in GaAs is claimed to be the origin of several Fermi level pinning levels for this compound. Some possible applications of the findings above as related to physics of semiconductor devices will be also discussed. [1] B. Cudell and D. Korošak, J. Appl. Phys., to be published. [2] J.T. Drummond, Phys. Rev. B36, 8182 (1987).

**B1.14**
NEARFIELD ULTRASONIC IMAGING: A NOVEL METHOD FOR NONDESTRUCTIVE SUBSURFACE IMAGING OF IC INTERCONNECT STRUCTURES

Gajendra S. Shekhawat, Huimin Xie, Yuegui Zheng, and R.E. Greg, Univ. of Albany for Materials, Albany, NY.

Nondestructive subsurface imaging is of great interest for backend-of-line (BEOL) integrated circuit (IC) interconnect structures due to the need to accurately identify subsurface defects in demarcate metal lines and mechanical defects in metal/low-k structures. Conventional acoustic microscopy has found limited application in subsurface imaging of BEOL interconnect structures due to its poor spatial resolution (< μm). The main challenge results from high-frequency transmission losses in field acoustic lenses that limit spatial resolution. In this work we report on the development of an alternate approach to nondestructive, noninvasive, subsurface imaging for IC interconnect structures: Near-field ultrasonic imaging. This approach utilizes a heterodyne interferometer based on a scanning probe microscope, similar to so-called heterodyne force microscopy (HFM). Ultrasonic excitation of suspended site vibrations in an SiM cantilever probe is transmitted with ultrasonic waves applied to an IC interconnect test structure. Subsequent heterodyne interference between these two signals is observed assuming a nonlinear tip-sample interaction. The measurement is sensitive to the relative phase difference of the two ultrasonic excitations and enables phase-sensitive imaging. Proof-of-principle demonstrations of this technique are presented for ultrasonic phase-imaging of Cu/low-k interconnect structures for a range of ultrasonic carrier frequencies. Spatial resolution <10 nm is demonstrated. These results are compared to simulations based on the Johnson-Kendall-Roberts (JKR) model for the mechanical interactions of a scanning probe tip with a surface. Calculations for deeper in-plane mechanical resolution are presented for near-surface and subsurface contributions to the phase image for Al/low-k and Cu/low-k IC interconnect test structures.

**B1.15**
STUDY OF TOb₂ O₃ BASED MOS CAPACITORS, WITH TaN, OXIDIZED IN O₂/NO AMBIENT. Paliwal Krishna moorthy, A.N. Chaudhary, Dept of Electrical Engineering, IIT Bombay, INDIA.

Tantalum pentoxide, as an alternative to SiO₂, is a high-k dielectric for DRAM and MOS applications, faces the problem of interface mismatch as silicon. SiO₂/SiO₂ interface layer were suggested to overcome the interface problem. Here we study the physical and electrical characteristics of TaN, oxidized in O₂/NO ambient, and without any other interface layer. This is done to check if N/H moves to the interface, and thus improves the electrical properties. However XRD studies of the film, showed the presence of TOb₂₂, oxidized Ta and TaN in the film. But the intensity of these peaks decreased with the increase of NH₃ content. This can be due to the presence of N₂O₅. However, the presence of TaN and oxidized TaN FTIR analysis at the interface showed strong TOb₂ and SiO₂ peaks. For the MOS capacitors, due to the presence of resistive components, the maximum capacitance was reduced, compared to that of pure TOb₂₂O₃ films. Vₚ varied from 1.1-1.9. Oxide charges in the films varied from 3-6.12*10¹⁵ cm⁻². But the traps in these films varied from 3 to 6.12*10¹⁵ cm⁻². But the traps in these films were found to be almost negligible as observed from the hysteresis of C-V characteristics. Films with NH₃ showed less oxide charges by one order of magnitude, as compared to pure TOb₂₂O₃ films.

**B1.16**
CHARACTERISTICS OF REMOTE OXYGEN AND HYDROGEN PLASMA DRY CLEANING OF FLUOROCARBON RESIDUES FORMED AT THE CONTACT HOLES

Hongkwan Yoon, Sung Bae
Kim, Hyungtak Seo, Jongrok Song, Yongsu Kim, Hyoeng Jeon, Hanyang Univ, Dev of Materials Science and Engineering, Seoul, KOREA. Hyun Suh, Young Chi Kim, Hanyang Univ, Dept of Chemical Engineering, Seoul, KOREA.

Reactive ion etching (RIE) using fluorocarbon is widely used to open contact holes due to its high anisotropic and selective silicon etching characteristics. However, the RIE process induces nonvolatile and chemically stable fluorocarbon residues and these residues typically cause high contact resistance at the metal-silicon interface. Moreover, it is very difficult to remove such residues except for silicon nitride from the etched surface of the silicon substrate. Several authors have reported a method to etch silicon and remove fluorocarbon residues. However, a large amount of these wet chemicals increased the process cost and caused significant environmental problems. In this study, low-temperature remote plasma dry cleaning processes that remove both the PR and polymer residues containing carbon and fluorine after RIE processes was investigated. The cleaning efficiencies of remote oxygen and hydrogen plasma were systematically evaluated at various conditions such as plasma power, exposure time, gas flow rate, and sample temperature. Remote-plasma laser was used to minimize plasma damage by keeping the substrate distance from the discharge region. Preliminary results showed that the hydrogen plasma cleaning was specifically required to remove the residual carbon contaminants on silicon surface after oxygen plasma cleaning. Also, two-step cleaning, oxygen plasma ashing and subsequent hydrogen plasma cleaning, was very effective to remove carbon residues and polymer without forming SiO$_2$ layer on silicon surface after cleaning process.

**B11.17**

**EFFECTS OF BOROPHOSPHOSILICATE GLASS DOPANT CONCENTRATIONS ON ISOTROPIC ETCH PROFILE.**

Chris Gibson, Bradley R. Williams, Stacey Evans, AMI Semiconductor, Inc., Pocatello, ID.

In the process of chemically etching contact openings, film characteristics of the borophosphosilicate glass (BPSG) film strongly effect the formation of an ideal contact profile. Ideal contact profiles reveal a wide glass shape to provide better metal step coverage in to the contact opening in comparison to a vertical sidewall profile. The bounded shape of the glass is etched chemically (isotropic) allowing for etch in the vertical and horizontal direction. As the addition of dopants to the oxide film effect the etch rate, the profile of the isotropic etch will change which in turn effect electrical device properties, down stream processes and device reliability. BPSG film characteristics are the area of investigation. Characteristics of concern are weight percent concentrations of boron and phosphorus, film density and dopant concentration profiles in relation to depth. To evaluate the entire contact formation module, chemical etch characteristics including etch rate in relation to film depth for thermal oxide films were also investigated. Experimentation in the form of a response surface design was used to model effects of previously discussed BPSG film characteristics. To achieve the desired and predictable wet etch rate of BPSG in a buffered oxide etch (BOE) calculated control limits were placed on the boron and phosphorous dopant concentrations. Results showed that dopant effects on the isotropic etch process exceeded the control capability of dopant concentrations in the deposition process. In relating process control capabilities to factor levels, the etch rate limits in Cpk are considered to be 1.5. To eliminate previously discussed defects created in the isotropic etch process, reject limits for dopant concentrations in BPSG film deposition process would need to be set well within the typical limits giving a Cpk below 1.5.

**B11.18**

**EPITAXIAL GROWTH OF Co$_3$Sn ON Si(100).**

Ryan Chong, Mark VenDron, Shou Yin Choy and Chaw Sing Ho.

Epitaxial silicides are of interest in advanced CMOS front-end process technology for the advantages of higher thermal stability and lower interfacial roughness than their polycrystalline counterparts. We report the synthesis of epitaxial Co$_3$Sn on Si(100) by a reactive deposition technique. Using real-time in-situ transmission electron microscopy and Rutherford backscattering (RBS) techniques, we observe the direct formation of Co$_3$Sn on the Si(100) surface with no intermediate phase formation. The experimental data will be compared with the deposition and annealing of Co on the clean or defect-terminated Si(100) surface. Under these conditions, the formation of polycrystalline Co$_3$Sn was observed, as expected. The mechanisms of epitaxial silicide formation were elucidated from video recordings of the growth process which will be discussed.

**B11.19**

**CU PATTERNING USING A SELF-ALIGNED MgO MASK.**

Yonekyu Ko, Heejang Yang, Janghe Bae, Rookman University, Dept of Metallurgical and Materials Engineering, Sungbuk-Gu, Seoul, KOREA.

Development of a Cu patterning method has been one of the most important technical processes that need to apply for the gate electrodes of thin film transistor liquid crystal display ( TFT-LCD). A self-aligned surface MgO layer was used as a mask in the new process. The surface MgO was formed by diffusion of Mg from Cu film to free surface. Cu(4.5% Mg) film having thickness of 4000 A was annealed in O$_2$ ambient at 10 mTorr, 500˚C for 30 min, followed by patterning of the MgO layer using photolithography and RIE etch process. The patterned MgO film was cleaned at ambient and H$_2$ gas was simultaneously flowed toward the film for dry etching. Total pressure of O$_2$ and H$_2$ in the reactor was constantly maintained at 200 mTorr (O$_2$/H$_2$ = 1:1). The self-aligned MgO films successfully played a role of mask for dry etching the Cu(Mg) films with a taper slope. A n-Si H FET was fabricated with the dry etching process. The n-Si H FET using the MgO mask showed good subthreshold slope, on/off current ratio, and output characteristic.

**B11.20**

**THE EFFECT OF THE MICROSTRUCTURE OF DIFFUSION BARRIERS ON THE PALLADIUM ACTIVATION FOR ELECTROLESS COPPER DEPOSITION.**

Seok Woong Hong, Yong Seun Lee, Jong-Wei Park, Div. of Materials Science and Engineering, Hanyang University, Seoul, KOREA. Ki-Chul Park, Samsung Electronics, Kyungkido, KOREA.

Cu is being widely used in ULSI metallization process as a replacement for Al due to its lower resistivity and higher electromigration resistance. Electroless Cu deposition is one of the most favorable candidates for Cu processing because of low cost and high quality of electroless Cu films. Copper can be deposited on a catalytic surface from an ionic solution without any external power supply by electroless plating. The electroless copper reaction is a autocatalytic reaction. This means that once there is an initial layer of copper, the reaction continues indefinitely. Since the surface on which electroless copper is deposited is not catalytic, an activation process is usually necessary to start the electroless reaction. Gold, platinium is required as catalytic layer for reliable electroless copper deposition, so the activation process is a key process for successful copper electroless plating. In this paper, palladium activation on electroless copper catalyst layer of electroless copper deposition has been investigated using X-ray diffraction, sheet resistance measurement, field emission scanning electron microscopy, photoevaporation transmission electron microscopy (TEM). The density of palladium nuclei on Ta2N diffusion barrier was increased with decreasing the grain size of Ta2N films which was caused by increasing nitrogen content in Ta2N films. Plan view TEM results showed that palladium nuclei formed mainly on the triple points of the grain boundaries of the TiN diffusion barriers.

**B11.21**

**FIRST LAYER COMPONENT CLEANING TECHNIQUES TO REDUCE PARTICLE GENERATION IN ETCH AND DEPOSITION CHAMBERS.**


Particles emanating from walk, shields and other components of the chambers in which integrated circuit wafers are processed, are among factors which have been shown to contribute to the formation of defect sites on completed wafers. Typically, the generation rate of particles is influenced by the final treatment that the surfaces of these components receive prior to installation in the chamber. Quartz components, prepared from material characteristic of contemporary bell jar manufacture, were subjected to typical post cleaning steps. These were surface texturing, post blast etching, pressure washing and ultrasonic rinsing. The relative effectiveness of these steps was assessed with a conventional experimental matrix. The chambers were evaluated for potential particle generation by two methods. First, carbon lift-off techniques were used to evaluate relative numbers of weakly attached particles on the surface of the coupons. Secondly, cross sections were prepared to examine the depth and type of subsurface damage capable of contributing to particle generation. Current methods to promote adhesion of deposits to PVD shieldings require increasing surface roughness by abrasive blasting. This technique is known to embed fractured grit particles into the metal substrate. Cleaning processes intended to remove micro-particles following grit blast are only marginally successful. This experiment was designed to optimize grit blast processing for melded grit removal. Stainless steel samples, prepared from unused shield.
components, were utilized in a matrix to evaluate the effectiveness of ultrasonic agitation, chemical etching, and CO2 pellet blasting at removing embedded grid. These samples were analyzed using both backscattered electron imaging. Subsequently, samples were subjected to thermal cycling representative of that experienced in chamber operation, to determine whether any remaining grid would be released as a result of these stressors. Electrical contact resistance and leakage current data were obtained from actual production operations, to present the effectiveness of post blast cleaning techniques.

D11.22
A NOVEL Cu/LOW-k INTEGRATION TECHNOLOGY BY Cu LINE-PILLAR PROCESS. Seichi Shoiguki, Takuya Fukuda, Hiroaki Koishy, Hiroshi Yamazaki, Association of Super-Advanced Electronics Technologies (ASET), Yokohama, JAPAN.

The Cu/LOW-k integration has become essential in order to reduce RC-delay of interconnect lines. In this regard, a Cu-dunk damascene process has been studied, and has been actually deployed into high-end ULIS-s. As the device size shrinks toward 10nm technology-node, the damascene structure will require more difficult technologies, such as the etching of low-k material and the deposition of conformal and thinner metal layers into the smaller feature size. The need to reduce the k value of dielectric will make the CMP process more difficult, because materials become more fragile as k becomes smaller. This paper describes a new concept of Cu/LOW-k integration that solves the above problems. The technology does not employ CMP, and involves the following three process steps. First, photoresist is patterned on a Cu seed layer and photoresist spaces are filled by the electroplated Cu. Cu lines or pillars are formed by the removal of the Pdseed/adhesion layer through the low-k film transfer by STP (spin coating, film transfer, and hot pressing), which involves spin-coating a low-k material on a bare film, and then transferring it to the Cu line/pillar substrate by pressing and heating in a vacuum. Gap-filling and surface-planarization are realized after the removal of the base film. Third, the top surface of the Cu line/pillar is revealed by the etch back technique. In experiments, X-ray lithography was used for the photoresist patterning. Pulse current mode was applied for the Cu electroplating to relax the Cu phasing stress. An organic low-k material (k=2.9) was used for the STP process. The formation of Cu lines and the low-k gap fill as well as the surface planarization were successfully demonstrated. This work was performed under the management of ASET in METI’s R&D program supported by NEDO.

SESSION D12: LOW-k DIELECTRICS
Chair: Jeffrey A. Lee and Paul S. Ho
Friday Morning, April 5, 2002
Salon 1D12 (Marriott)

8:00 AM D12.1
CROSS-SECTIONAL ELECTOMIC IMAGING OF COPPER AND LOW-k IC INTERCONNECT STRUCTURES FOR MECHANICAL ANALYSIS/METROLOGY AND DEFECT IDENTIFICATION. Lam Mathunamwani, Huimin Xi, G.S. Shilchuk, Katherine Dommers, B.E. Geer, University at Albany Institute for Materials, Albany, NY.

One of the most difficult challenges in the integration of Cu and low-k materials in high-performance integrated circuit (IC) processes concerns the significant mismatch of mechanical properties (Young’s modulus, shear modulus, Poisson’s ratio, coefficient of thermal expansion) between metals and low-k dielectrics. Recently, a technique based on ultrasonic force microscopy (UFM) has been developed to enable nondestructive, nanometer-scale elastic imaging of processed structures. UFM has successfully been used to image RIL-induced hardening of patterned low-k dielectrics and mechanical modification of such dielectrics due to chemical mechanical planarization (CMP). To complement this technique we report on the development of cross-sectional elastic imaging of IC interconnect structures via cross-sectional UFM (CS-UFM). A CS-UFM protocol has been developed to successfully image the elastic profiles of cross-sectioned Al/Silicon oxide, Cu/Silicon nitride, and Cu/lowk interconnect structures with a spatial resolution <5 nm. CS-UFM imaging reveals mechanical defects and non-uniformities in low-k dielectrics. Specifically, inter-strain variation of mechanical response is shown. Also, subsurface compositional defects have been imaged within low-k dielectrics. Likewise, CS-UFM has been used to image voids in Cu-filled trenches/voids. The cross-sectional elastic imaging maps of the IC interconnect structures are compared to finite element analysis (FEA) models as well as empirical elastic response models to estimate the mechanical sensitivity of CS-UFM and calibrate the nanoscale image intensity to the elastic moduli of the interconnect metal, barrier, and dielectric. A modulus sensitivity <2% is demonstrated.

8:15 AM D12.2
A CORRELATION STUDY OF THERMAL STABILITY ON POROUS LOW-k. Y.F. Chow, T.H. Foo, Y.J. Yun, Y.H. Wang, A.Y. Du, S.Y. Wu, C.Y. Li, P. Kumar, P.D. Foo. The thermal stability on porous low-k, P-SiLK with dielectric constant about 2.4, has been studied. The effects of thermal cycles on porous low-k film such as shrinkage, refractive index, dielectric constant, pore size, hardness etc. were performed by X-ray and AFM. Film is spun on silicon substrate, baked and cured in the vertical furnace for 1 hour at 340oC under N2 ambient. Thermal cure is done in the vertical furnace with oxygen level less than 10 ppm. Two curing temperatures (340oC and 450oC) and 4 types of O2 level were performed and compared to the thermal stability after several thermal cycles. Each thermal cycle is one hour but the film is checked for every alternate cycle. We observed that after the first thermal cycle of 340oC and 450oC cured, the refractive index increase and about 0.8% and 0.4% respectively. Dielectric constant is slightly increased after 450oC cured but that is no significant change for 340oC cured. Change in film properties are investigated and evaluated by using x-ray, FTIR, mercury probe, nanoindentation and TTM. P-SiLK low-k material SiLK with dielectric constant about 2.8 is used as a baseline for comparison.

8:30 AM D12.3
CHARACTERISTICS OF LOW-k AND ULTRA-LOW-k PECVD DEPOSITED SiCOH FILMS. A. Grill, V. Patel, K. Rodbell, S. Christiansen and E. Simonzy, IM Research Division, T.J. Watson Research Center, Yorktown Heights, NY.

We have shown previously that the dielectric constants of PECVD SiCOH dielectrics can be extended to ultralow-k values of k=2.0. The reduction in the dielectric constant has been achieved by adding an organic precursor to the tetramethylethanoloxirane (TMETO) used for the preparation of the SiCOH dielectric and amending the films to remove the thermally lossy-state organic CH4 fractions from the films to add porosity and reduce the density of the films. In order to estimate the effects of the reduction of the values of the dielectric constant on the properties of the material, the films have been characterized by XPS and FRes, FTIR, position annihilation spectroscopy, TEM, AFM, nanocurrent measurements, stress vs. temperature and photothermal deflection measurements. The obtained characteristics of the films will be presented and discussed as a function of the deposition conditions and in relation to the dielectric constants.

8:45 AM D12.4
A NEW ULTRA-LOW-k ILD MATERIAL BASED ON ORGANIC-INORGANIC HYBRID RESINS. Ben Zhong, Cory Burger, Ken Weinberg, Herman Myehn, Paul Schalk, Alan Peck, Stephanie Mulhozier, Marley Von Howe, Karen Mien, Dow Corning Corporation, Midland, MI. Dow Corning Corporation, Seneffe, BELGIUM. TMEC, Heverlee, BELGIUM.

A ULK material based on a silicone resin has been developed that can be coated on silicon wafer by spin coating, and both cured and reflowed porosities by a simple thermal treatment in normal atmosphere. The chemical bonds between the resin and porogen groups prevent the phase separation of the porogen from the resin during curing and lead extremely small pores. The highly hydrophilic thin films made from this material displayed Dk of 1.8, breakdown voltage of 4 MV/cm, a cohesive strength >60 MPa, excellent crack resistance, and an average pore size of 2.2 mm by PALS and 2.5-3.0 mm by EP. In this presentation, our strategy for designing low-k materials, the material properties and integration results for this new material will be discussed.

9:00 AM D12.5
A NEW APPROACH OF THIN-FILM X-RAY REFLECTANCE/SCATTERING ANALYSIS FOR ULTRA-LOW-k DIELECTRICS WITH PERIODIC PORE STRUCTURES. N. Haga, MIRAL-AIST, Tsukuba, JAPAN; Y. Oka, K. Yamada, MIRAL-AIST, Tsukuba, JAPAN; Y. Aizuma, I. Kojima, NM-AIST, Tsukuba, JAPAN; T. Kikkawa, MIRAL-AIST and Hiroshima Uni., Higashi-Hiroshima, JAPAN.

We propose and demonstrate experimentally a new structural characterization technique for ultra-low-dielectric constant thin films with periodic porous structures by employing a new analytical approach to X-ray reflectance / scattering data. The analytical approach which we propose here takes specular reflection, incoherent scattering from random distribution of, and coherent scattering from periodically modulated distribution of electronic density into account. Thin-film measurements by reflectance and scattering of X-ray are known for their advantages in sensitivity and non-intrusiveness. Interlayer dielectric with dielectric constant (k) less than 1.5 will be required in future integrated circuit technology for high enough transmission speed of signal and for low enough energy consumption. On the other hand, candidate materials ever studied, do not
show k values well below 2 without inclusion of pores or open volume structures in them. As the pore volume fraction is increased for lower k, pore volume fraction increases for random resulting in increase of average (connected) pore volume and hence in deterioration of film mechanical properties. Efforts to introduce periodicity in pore structure are undertaken to resolve the problem. Once the periodicity is introduced, however, the above-mentioned X-ray measurement techniques start to suffer from the signal associated with the anisotropy and coherent scattering or diffraction from the periodic modulation of electron density, and new approaches become necessary for the information obtained about the structure itself, but also about the residual random structure in the "wall" material as well as about the overall structural disorders; all these parameters are important in assessing the relationship between k and such essential properties for integration as mechanical properties, stability and reliability. By comparing the experimental data taken under specular reflection and off-angle scattering both in out-of-plane and in-plane geometries with the proposed model calculation, the contributions from the origins are successfully separated.

9:15 AM B12.2
NOVEL PERIODIC NANOPOROUS SILICATE GLASS WITH HIGH STRUCTURAL STABILITY AS LOW-k THIN FILMS.
Yoshikazu Oka, MIRAI-ASET, IBM research, Japan; Norikazu Nishiyama, Shimane University, Kuronaki, Oeyama, Osaka; Dept. of Chemical Engineering, Osaka, Japan; Nobuyuki Hori, MIRAI-ASET, IBM, Japan; Takamasa Kikawa, MIRAI-ASET, IBM, Japan; and Hiroshi Univ, Research Center for Nanodevices and Systems, Hiroshima, Japan.

Reduction of interconnect parasitic capacitances has become more important to fabricate high-speed ULSIs for 100 nm technology node and beyond. In order to meet with this requirement, various interconnect dielectrics, including silicate glass, with low k (dielectric constant) have been developed. Introducing pores (air) into dielectric materials is an efficient method to fabricate low-k film with dielectric constant less than 2.0, because the dielectric constant of air is 1.0. Conventional porous films, however, did not have enough mechanical strength and electrical properties as expected. Therefore, pore formation technology in dielectric film must be improved for development of low-k (k=1.5) for 70 nm technology node. We have developed a novel periodic nanoporous silicate glass with high structural stability as a low-k film by spin-coating method. Conventional porous silicate glass films have caused structural shrinkages (10-20%) or more by calcination of the spin-coated films. In this investigation we adopt special treatment before calcination. Our novel nanoporous film shows no shift of XRD peak position after calcination at 650°C, indicating that both the ultimate mechanical strength and the minimization of stress at the interface between the prepared film and the underlying substrate can be achieved. Such a shrinkage-free periodic nanoporous silicate film can possess higher Vｃd (break down voltage) and lower Iｅa (leak current). In this study we evaluated electrical properties (dielectric constant, Vｃd and Iｅa) and the MFM images (at low and high resolution) of this special-treated novel nanoporous silicate film. The dielectric constant was evaluated to be around 1.5 at 1MHertz.

10:00 AM B12.7
POROUS METHYLSIQUOXANE LOW-k DYELECTRIC FILMS: MECHANICAL BEHAVIOR, MOISTURE SENSITIVITY, AND ENVIRONMENTAL CONSIDERATIONS.
Abdi Rehman, IBM Almaden Research Center, San Jose, CA; Reinhold Dressel, Dept. of Materials Science and Engineering, Stanford, CA; Robert Miller, Willi Volkman, IBM Almaden Research Center, San Jose, CA; and Matthew R. Kunz (IBM, Almaden Research Center, San Jose, CA; Robert Miller, Willi Volkman, IBM Almaden Research Center, San Jose, CA; Reinhold Dressel, Dept. of Materials Science and Engineering, Stanford, CA.)

Methylsiquoxane (MQS) films are primary candidates to replace silica in the interlayer dielectric in future generations of microelectronic devices. More importantly, the dielectric constant of MQS is continuously increasing with the increase of porosity at nanometer length scale. However, before integration is possible it is necessary to understand and quantify the mechanical and fracture behavior of these thin films. Specifically, the addition of porosity may have detrimental effects on many of the required mechanical properties, which will reduce survivability during CMP and lower the resistance to electromigration back stresses during operation. The effect of porosity on a range of relevant mechanical properties including inherent fracture resistance, adhesion, and elastic modulus will be addressed for several resin formulations. Various other factors, including surface modification with UV-curing, will be presented. The implications of different matrix microstructures and porosity are discussed.

10:15 AM B12.8
THERMAL-STRUCTURAL STUDIES ON 2,4,6,8-TETRAMETHYLICYCLOTRETRAOXANE (TMCTS).
Chongyang Xu, Alexander S. Borovik, Ziyun Wang, Jose Arno and Thomas H. Bam, ATML, Inc., Danbury, CT.

2,4,6-TETRAMETHYLICYCLOTRETRAOXANE (TMCTS) is considered as being a precursor for CVD low dielectric constant (k) thin films as interleaver dielectrics in an integrated circuit technology. Recently, it was reported that TMCTS polymerizes in delivery lines in a CVD process tool. To accommodate this problem, we conducted a series of chemical studies on TMCTS thermal behaviors under various process conditions. For instance, TMCTS was heated in the presence of 3010, stainless steel, acids, bases, water and various drying agents. The TMCTS then was studied by NMR, FT-IR, XRD, and thermal analysis. These results showed that TMCTS is readily polymerized in the presence of moisture with acids and bases. We have developed an ultra-dry TMCTS and a new method to determine water contents in TMCTS that allows us to control TMCTS quality. In this paper, we will report our results on TMCTS thermal stability studies.

10:30 AM B12.9
ELECTROMIGRATION IN SUBMICRON DUAL-DAMASCENE Cu/Low-k INTERCONNECTS.
Kedon Lee, Xia Li, Emiss T. Ogawa, Hideki Monushahi, and Paul S. Ho, The University of Texas at Austin, Microelectronics Research Center, Austin, TX; Vierk A. Bhasale, and Rod Augur, International SEMATECH, Austin, TX.

Electromigration (EM) lifetime characteristics and failure mechanism have been investigated for Cu/SiLK and Cu/porous MQS interconnects as compared to Cu/oxide interconnects. SiLK is an organic polymer developed by the Dow Chemical Company with k of 2.7 and porous MQS is a spin-on porous silicate with k of 2.4. The accelerated tests were found to be 0.97 eV for SiLK and 0.80 eV for the porous MQS similar to that of oxide. This range of activation energies suggests a similar mass transport mechanism, interfacial diffusion. The current exponent of SiLK and oxide were found to be 1.30 and 1.2, respectively focused ion beam (FIB) analysis of distinct failure mechanism for Cu/low-k interconnects due to interfacial Cu extrusion at the anode under the cap layer has been observed and it seems to be related to thermomechanical properties of low-k materials. The short lifetime characteristics of low-k interconnects can be attributed to a smaller back stress due to smaller confinement effect. The critical length effect has been found to be smaller for Cu/low-k than for Cu/oxide. Results obtained in this study indicated that thermomechanical properties of low-k interconnects, including interfacial adhesion, failure mode of low-k material, Joule heating, mechanical strength (E) and CTE are important parameters in controlling EM reliability of Cu/low-k interconnects.

10:45 AM B12.10
EFFECT OF ULTRA-VIOLET ANNEALING ON PHYSICAL AND ELECTRICAL PROPERTIES OF HIGH-PERMITTIVITY DIELECTRICS DEPOSITED BY PHOTO-ASSISTED CHEMICAL VAPOUR DEPOSITION.
D.J. O’Sullivan, P.R. Hurley, N.R.%
University College, Cork, Ireland; P. Feng, J.Y. Zhang, I.W. Boyd, Dept. of ECE, University College-London, London, United Kingdom; G. Wilke, J.-P. Semet, INM, Gelsenkirchen, Germany; L. Leedham, IncoTech, Suffolk, United Kingdom; C. Jimenez, JIPELEC, Creteil, France.

The results of an experiment designed to investigate the effects of post deposition ultraviolet (UV) assisted O2 annealing on the properties of high-permittivity (ε) films on silicon are reported. Although previous work has demonstrated low temperature (350-400°C) post deposition UV O2 annealing can improve the physical and electrical properties of high-ε films [1], the mechanism is not well understood. The high-ε film chosen for the experiment was Ta2O5 fabricated by UV assisted Injection Liquid Source Chemical Vapor Deposition (UVILS-CVD) on Si(100) substrates. The UVILS CVD technique allows the high-ε deposition and post deposition annealing to be performed in the same reaction chamber. Leakage current densities are reduced by up to six orders of magnitudes as a result of a 350°C post deposition UV O2 anneal. The anneal step increases both the refractive index (2.01 to 2.21) and film stoichiometry (TaO2:1.2 to 2.47). From SIMS analysis, this improvement has been attributed to the removal of Si, N and C from the Ta2O5 film during the anneal. The UV anneal in O2 creates oxygen free radicals and oxide (the bond strength is 5.17 eV; the UV photon energy is 5.68 eV). It is proposed that these contaminants are removed in the gas phase (CO, CO2, SiO, NO, NO2, etc.) following the creation of oxygen free radicals. In addition, the UV O2 irradiation provides O free radicals to the re-deposited oxide, which is evidenced by the increase in the stoichiometry of the film after the 350°C UV O2 anneal. Results will be presented on post deposition UV O2 annealing experiments performed in vacuum conditions, which support this theory. The technique is currently being extended to alternative high-ε dielectrics, including HfO2 and mixed Ta2O5-TiO2 layers, formed using carbon based metalorganic precursors [1]. J. Zhang et al., J. Phys. D: Appl. Phys., 32, L91, (1999).
11:00 AM B12.11
POROSITY EFFECT ON THERMOMECHANICAL PROPERTIES OF ORGANIC LIGHT-EMITTING FILMS. Dongseun Guan, Junlan Liu, Paul S. Ho, The University of Texas at Austin, Microelectronics Research Center, Austin, TX; Willi Volksen and Robert D. Miller, IBM Almaden Research Center, San Jose, CA.

Degradation of the thermal and thermomechanical properties with porosity is a key concern regarding the implementation of ultra low dielectric constant (low-k) porous materials. In this study, a bending beam containing porosity was measured to measure modulus and Poisson's ratio of the films. Coefficient of thermal expansion (CTE) and Poisson's ratio of thin films were used to investigate the thermomechanical behavior of the porous methylsiloxane (MSQ) films prepared by incorporation of macro-molecular poly[(phenyl)phosphazene] (pph) in the film. The slope of the temperature vs stress was calculated as a function porosity and the stress drop appeared around 20% porosity. Compared with the low-k films, the modulus demonstrated a much more pronounced transition behavior. It is suggested that the sharp drop is due to a transition in porosity morphology from close cell to interconnected open cell structure at the percolation limit.


11:15 AM B12.12
INTERFACIAL ADHESION STUDY OF POROUS LOW-k TO CVD BARRIER LAYERS. Caroline C. Merrill, Paul S. Ho, Univ. of Texas, Microelectronics Research Center, Austin, TX; Jeffrey A. Lee, Jeffrey T. Wetzal, International Sematech, Austin, TX.

The drive for smaller and faster microelectronic devices has led to the integration of high density interconnects, low-permittivity (low-k) dielectric materials for interconnect structures. The weak thermomechanical properties of low-k dielectric cause serious concerns on reliability and integration of Cu/low-k interconnects. Indeed, during fabrication, thermal stress may arise due to mismatching in coefficients of thermal expansion (CTE) and elastic properties of the materials. The interfacial adhesion of thick films becomes critical to the integration and reliability of low-k interconnects. This paper will present the results from an application of the 4-point bending technique to characterize the adhesion strength of ultra low-k dielectric materials to CVD barrier layers. Adhesion energy between an ultra low-k dielectric material and a barrier layer was measured as a function of $k$ (k $< 3.0$) and found that the adhesion energy decreases with the dielectric constant which correlates with mechanical properties such as Young's modulus and hardness. Adhesion measurement data were also obtained for different low-k/Barrier layer interfaces. The independence of energy on the type of interface suggests that the fracture is actually occurring in the low-k material and not at the interface. In addition, the very low fracture energies (G $< 3.4$ J/m$^2$) confirm the weak mechanical properties of such materials. Research illustrated with failure surface analysis using Auger electron spectroscopy and scanning electron microscope.

11:30 AM B12.13
SILICIDATION OF SILICATE LOW-k DIELECTRIC THIN FILMS. Joseph B. Vella, Alex A. Volinsky, India S. Adhikary, Motorola, Digital DNA/T Labs, Process and Materials Characterization Lab, Mesu, AZ; William W. Gerberich, University of Minnesota, Dept. of Chem. Eng. and Materials Science, Minneapolis, MN.

Due to the radical compromise in thermal and mechanical properties that the migration of silicon dioxide to novel low-k dielectric films necessarily incur, the IC industry is motivated to better understand the failure modes of low-k dielectric films. These failure modes include thermal instability, poor mechanical strength, and chemical-mechanical polishing (CMP) failure due to low cohesive and adhesive fracture toughness. Studies performed at SEMATECH have indicated that CMP reliability of low-k can be correlated with the elastic modulus of the film. However, we believe that the modulus is only of modest importance mechanical properties that stem from the films interacted silicate interconnect network or non-porous. Silicided porous films typically have low elastic modulus of 1 to 10 GPa and relatively high hardness of 0.5 to 1.5 GPa. With the high hardness to modulus toughness can also be expected. In this study we outline other properties of silicided low-k films that must be understood for proper low-k dielectric film screening. CVD deposited low-k films of different thicknesses were deposited on Si wafers and tested for porosity measured with nanoindentation. An indentation method utilizing a cubic corner indenter was used to induce radial cracks in these low-k films. Based on the indentation load and radial crack length, measured optically, fracture toughness of thin films was extrapolated. Film fracture was also observed during nanoindentation adhesion testing. These tests were intended to measure interfacing fracture toughness, however interfacing cracks linked into the film itself, indicating that adhesive failure mechanisms compete in the event of device failure. Given that the crack propagates along the low-k and based on resultant stress energy release rate calculations, film toughness on the order of 0.05 MPa m$^{1/2}$ is estimated. This is corroborated by strain energy release rate calculations based on spontaneous film fracture to residual stress at a critical film thickness of 3 microns.

11:45 AM B12.14
LOW-k THIN FILMS DEPOSITED BY PECVD USING DECAHYDROPHENALANE AND TETRAETHYLOORTHOSILICATE AS THE PRECURSORS. Sunguk Yeo, Jeoyang Yang, Osoonnam Shim and Donghoon Jung, Department of Physics, Brain Korea 21 Physics Research Division and Institute of Basic Science, Sungkyunkwan University, Suwon, REPUBLIC OF KOREA.

Plasma enhanced chemical vapor deposition (PECVD) using a mixture of decahydronaphthalene (DHN) and tetraethylorthosilicate (TEOS) as the precursors was used to deposit low dielectric constant plasma polymer thin films. The films were referred to as plasma polymerized decahydronaphthalene tetraethylorthosilicate (PPDDN-TEOS) films. Properties of PPDDN-TEOS thin films were dependent significantly upon the plasma power. The deposition power was varied from 30 to 90 W. As the plasma power increased, except for the deposit at 70 W, the relative dielectric constant $k$ decreased, thermal stability degraded, and leakage current decreased. The PPDDN-TEOS thin film deposited at 70 W showed the minimum $k$ value, the poorest thermal stability, and the minimum leakage current among the PPDDN-TEOS films deposited with plasma power of 30, 50, 70, and 90 W. We investigated the chemical structure of PPDDN-TEOS by Fourier transform infrared (FT-IR) spectroscopy. FT-IR absorption analysis revealed that as the content of DHN increased species decreases in the PPDDN-TEOS films, the $k$ value decreases, and thermal stability degrades. The thin film deposited at 70 W showed leakage current of $5\times10^{-4}$ A/cm$^2$ at 1 V/cm. In order to improve the $k$-value and thermal stability of the 70W-deposited PPDDN-TEOS films, we performed the post deposition in situ heat treatment. After the heat treatment at 450°C, the relative dielectric constant of the film decreased from 3.1 to 3.7. The 450°C heat treated PPDDN-TEOS film has higher thermal stability than the not-treated film. Removal of reactive species in the film and increase of cross-linking among film-forming species by heat treatment are thought to contribute to the decrease of $k$ value and improvement of the thermal stabilities, respectively.

SESSION 185 RELIABILITY
Chair: Stefan P. Haas-Riuge and Paul S. Ho
Friday afternoon, April 5, 2002
San Antonio 10-12 (Marriott)

1:30 PM 3B1.2
TECHNOLOGY FOR LOCALIZATION OF IC INTERCONNECTION DEFECTS. Edward I. Cole Jr, Sandia National Laboratories, Albuquerque, NM.

The advances in integrated circuit technology has made fault site localization extremely challenging. Charge-Induced Voltage Alteration (CIVA), Low Energy CIVA (LECTIVA), Light-Induced Voltage Alteration (LIVA), Seebeck Effect Imaging (SEI) and Thermally-Induced Voltage Alteration (TIVA) are five recently developed failure analysis techniques which meet the challenge by rapidly and non-destructively localizing interconnection defects on ICs. The techniques take advantage of voltage fluctuations in a current constant power supply as an electrical path or photon beam is scanned across an IC. CIVA and LECIVA are scanning electron microscope (SEM) techniques that yield rapid localization of open interconnections. LIVA is a scanning optical microscopy (SOM) method that yields quick identification of damaged semiconductor interconnect junctions and determines transistor logic states. SEI and TIVA are SEM techniques that rapidly localize open interconnections and shorts respectively. LIVA, SEI, and TIVA can be performed from the backside of ICs by using the proper photon wavelength. Each technique will be described in terms of the physics for signal generation, sample preparation requirements, and advantages over existing analysis methods. Examples of each technique will be shown demonstrating its utility in locating defects.
2:00 PM B13.2
EBIC AND XTEM ANALYSIS OF HIGH VOLTAGE SAMOS RELIABILITY FAILURES. Larry Rice, Motorola, Inc., Process and Materials Characterization Laboratory, Mesa, AZ.

Microscopists are faced with many challenges in locating and examining failure sites in the ever-shrinking semiconductor device. The site must be located using electrical characterization techniques like electron beam induced current (EBIC), photo emission microscopy (PEM), or liquid conduction with a focused ion beam (FIB). Both PEM and LC require the semiconductor circuit to be at its operating conditions which has been observed to locally melt the area of interest frequently destroying evidence of the failure mechanism. In contrast, EBIC tip is usually low or no applied voltage eliminating further damage to the circuit. EBIC has been applied to locate leakage sites in high voltage metal oxide semiconductor (MOS) electro static discharge (ESD) reliability failures. In addition to a brief review of the basic principles of EBIC and describing a technique to successfully cross section ‘hot spots’ for transmission electron microscopy (TEM) observation, focus will be placed on a case study of the reliability testing failure analysis of ESD power transistors using EBIC, scanning electron microscopy (SEM), FIB, and transmission electron microscopy (TEM).

2:15 PM B13.3
LENGTH EFFECTS ON THE RELIABILITY OF DUAL-DAMASCENE Cu INTERCONNECTS. F. Li, Wei, Massachusetts Institute of Technology, Department of Materials Science and Engineering, Cambridge, MA; C. L. Gan, Singapore-MIT Alliance, Advanced Materials for Micro-Nano Systems Programme, SINGAPORE; C. V. Thompson, Massachusetts Institute of Technology, Department of Materials Science and Engineering, Cambridge, MA; and Singapore-MIT Alliance, Advanced Materials for Micro-Nano Systems Programme, SINGAPORE; J. J. Clement, Sandia National Laboratory, Albuquerque, NM; S. P. Hua-Riege, Intel Corp., Portland, OR, now with Lawrence Livermore National Laboratory, Livermore, CA; K. L. Pey, W.K. Choi, Singapore-MIT Alliance, Advanced Materials for Micro-Nano Systems Programme, and National University of Singapore, Department of Electrical & Computer Engineering, SINGAPORE; H. L. Tsai, B. Yu, M.K. Ruhakurbone, Institute of Microelectronics, SINGAPORE.

We have carried out experiments on dual-damascene Cu interconnects with different lengths. We find that, like Al-based interconnects, the reliability of Cu-based interconnects improves at short lengths. Like Al, some short Cu lines do not form voids that cause failure before back-stresses cause void growth to stop. However, unlike Al-based interconnects, there does not appear to be a minimum current density-line length product (jL) for which all lines are immune. It is thought that this is related to the absence of a conducting refractory overlayer in Cu technology that can shunt current around small voids, as conducting anti-reflection coating layers do in Al technology. Also, unlike Al-based Cu interconnects, it is the time to failure and the deviation in the time to failure increase for longer lines. A sub-population of long lines survive for very long times. It is thought that this is the result of the rupture of the thin refractory metal layer at the Cu/intermetallic interface. The significance of this complex behavior, there are intermediate line lengths with minimum median lifetimes and minimum lifetime variations in Cu metallization.

3:00 PM B13.4
EFFECT OF METALLIC CONTAMINATION ON INTERFACE PROPERTIES AND OXIDE RELIABILITY. Elena Ostroumova, Center for Microelectronics Research, University of South Florida, Tampa, FL; Scott Campbell, Department of Chemical Engineering, University of South Florida, Tampa, FL; Drew Hoff, Center for Microelectronics Research, University of South Florida, Tampa, FL; Richard Gilbert, Department of Chemical Engineering, University of South Florida, Tampa, FL; Eric Person, Darrell Simpson, Agere Systems, Orlando, FL.

New and emerging process technologies are creating contamination control challenges for current and future generations of integrated circuits. Damascene interconnect, metal gate and metal interconnect processes are representative of many potential sources of metallic contamination to wafer structures. In this work, we studied contamination of oxidized silicon wafers by several metals of industrial importance, including copper, cobalt, sodium, iron and nickel. Contamination levels ranged from 0.1 to 300 ppb of metal as indicated by XPS measurement. These levels were representative of exposure in chemical processes such as CMP cleans. Contaminating ions were driven into the oxide layer by corona temperature stress (CTS). The presence of incorporated metallic agencies within the oxide was determined using VPD-ICP-MS and SIMS. The effects of contamination on interface and oxide reliability were quantified by non-contact COCOS (Corona Oxide Characterization of Semiconductors) and SILC (Stress Induced Leakage Current) techniques. We discuss the relationships identified between surface analysis results and the non-contact measurements of oxide reliability and interface properties.

3:15 PM B13.5
MECHANICAL-STRESS CONTROLLED SILICIDE INTERCONNECTS FOR HIGHLY RELIABLE SEMICONDUCTOR DEVICES. Hiromi Shimada, Hideki Murak, Hitachi, Ltd., Mechanical Engineering Research Laboratory, Enbara, JAPAN.

Silicidation is one effective way of reducing contact resistance between a metal and silicon. Titanium silicide is one of popular material for this kind of applications. titanium film is deposited on poly-Si plugs, which are embedded in a silicon dioxide layer, and annealed at about 800°C to form titanium-silicide between the poly-Si plugs and the metal interconnects. The first reaction of Ti to TiSi2 starts at about 500°C, and the second reaction of TiSi2 to TiSi starts at about 600°C. However, this silicidation method results higher tensile stress than 1 GPa in the reacted silicon film due to volume shrinkage during the silicidation, thus it sometimes causes delamination between the reacted silicide and the remaining silicon. The stress developed near the interface between the poly-Si and the reacted silicide film was analyzed using a finite element method by considering the silicidation-induced stress. The developed stress near the interface strongly depends on both the thickness of the newly grown silicide and the diameter of the contact. It increases with increasing thickness of the silicide and decreasing the contact diameter. The developed stress reaches the critical stress for delamination at the interface where the thickness of TiSi2 was thinner than 75 nm and the diameter of the contact was smaller than 0.3 μm. It is therefore, very important to monitor the thickness of the silicide in order to eliminate delamination at the interface. Increasing the annealing temperature for the silicidation the higher than 800°C is another effective way for reducing the stress, because the developed stress reduces due to viscoelasticity of the silicon film. We have made clear the developing process during titanium-silicide formation and an effective design rule for the highly reliable silicide interconnect.

3:30 PM B13.6

Aluminum-wire/tungsten-plug based multi-level interconnect technology for VLSI circuits in the semiconductor industry. The early interconnect failure in the W-plug via structure has been recognized as a generic phenomenon. In this work, we present detailed studies of two integration schemes for such a multi-level ULSI interconnect module for sub-quarter-micron CMOS technologies, and discuss the benefits and drawbacks of each of them primarily from a process integration point of view. We demonstrate that an etch stop integration scheme in the via etch stop layer, which is a significant improvement over the prior etch integration scheme, is an significantly improved via electromigration performance compared to an over etch integration scheme in which the via is over etched into the underline AlCu. We also identified several highly detrimental early failure modes associated with the over etch structure, and showed that such early failure modes could be prevented in the etch stop integration scheme. All test structures were processed using manufacturing tool sets at a state-of-the-art eight-inch silicon fab of Agere Systems. Detailed information regarding metallization compositions for metal wires and via liners, electromigration failure distributions, FMA (failure mode analysis) of early interconnect failures, via contact resistance, metal sheet resistance, interconnect yields, and their correlation with each other will be presented. Even though there are some small penalties in the device performance in the etch stop integration scheme, the benefits in the reliability and the better tolerance to manufacturing process variations clearly justify the adoption of this robust multi-level ULSI interconnect module for sub-quarter-micron CMOS technologies.

3:45 PM B13.7
INTERFACIAL ADHESION OF PATTERNED INTERCONNECT STRUCTURES. Christopher S. Litten and Reinhold H. Disdierski, Department of Materials Science and Engineering, Stanford University, Stanford, CA.

Recent studies of the adhesion of blanket thin film interconnect structures have established that plastic energy dissipation in thin metal and polymer films, such as copper and low dielectrics, is related to the thickness of the interfacial layers. However, there is currently little understanding of how the geometry and size of
interconnect features utilized in technologically relevant structures will
influence plasticity and hence the fracture resistance of such patterned
structures. Accordingly, to investigate the role of feature size and
shape, selected patterned structures containing arrays of polymer and
metal lines with varying aspect ratios have been investigated.
Macroscopic adhesion values were determined by measuring the
critical strain energy release rate, $G_c$, for debonding of a selected
interface. The significant contribution to $G_c$ values from local plastic
energy dissipation in the polymer and metal lines was examined and
used to demonstrate the effect of patterned structure geometry on
interfacial adhesion. Trends in adhesion and fracture behavior related
to the patterned structures will be discussed in terms of the prevailing
plastic deformation mechanisms and form the basis from which simple
design rules for improved mechanical reliability may be developed.