SYMPOSIUM B
Materials, Technology, and Reliability of Advanced Interconnects
March 28 - April 1, 2005

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* Invited paper
Wafer Level Packaging (WLP) has gained momentum in the small chip arena, driven by needs for cost reduction, form-factor shrinkage, and enhanced performance. Advantages in performing burn-in and test at the wafer level will lower the IC cost and resolve the known good die (KGD) issues that are concerns to the electronic industry. WLP will merge the front-end IC fabrication with the back-end discrete packaging, and provide a paradigm shift in the electronic packaging industry. This course will provide an overview of the recent advances on WLP, the advantages and challenges in terms of materials (conventional polymers as well as nano functional materials), processes (with ultra fine pitch flip chip interconnects), and reliability in these new packaging technologies.

**COURSE OUTLINE**

- Overview of Electronic Packaging: Present and Future Trends
- Definition of Wafer-Level Packaging
- Market Drivers for WLP
- Overview of Various WLP Configurations and Process Techniques in the Industry
- Barriers and Challenges with WLP Technologies
- Fundamentals of Polymers and their Physical and Mechanical Properties and Measurements
- Overview of Inorganic and Organic Polymers for Electronic Packaging
  - Silicon Dioxides, Nitrides & Oxy nitrides
  - Epoxy resins, Polyimides, Silicone-Polyimides, Polyurethanes
  - Benzocyclobutene, Parylenes, BT Resins, Sycars, Polyessters, High Temperature & Liquid-Crystal Polymers, Low-k, Low Loss and Nonfunctional and Foam Materials
- Recent Advances on Low Cost Flip Chip: Materials, Processes and Reliability
- Lead-free Interconnect Alternative Materials- Electrically Conductive Adhesives
- Next Generation WLPS

This tutorial will be of interest to engineers, scientists, and managers involved in the design, process, and manufacturing of IC electronic components, modules, and hybrid packaging, as well as electronic materials suppliers involved in materials manufacturing and research & development.

**Instructors:**

- C. P. Wong, Georgia Institute of Technology
- Luu Nguyen, National Semiconductor Corp.

**SESSION B1: Characterization of Low-K Dielectrics**

**Chairs:** Andrew McKerrow and Todd Ryan

Tuesday Morning, March 29, 2005
Room 2004 (Moscone West)

**9:00 AM B1.1**

A New Technique for the Characterization of the Adhesion in Patterned Films. **Ion Ocana**, Jon Molina, Diego Gonzalez, M. Reyes Elizalde, J. Manuel Sanchez, J. Martinez-Esnaola, Javier Gil-Sevillano, Tracey Scherbani, Daniel Pantuso, Brad Sun, Jessica Xu, Barbara Mines, Jim He and Jose A. Maiz,

**3EEIT (Centro de Estudios e Investigaciones Tecnica de Gipuzkoa) and TECNUN (University of Navarra), San Sebastian, Gipuzkoa, Spain:**

**Intel Corporation, Hillsboro, Oregon.**

The thermo-mechanical robustness of interconnect structures is a key reliability concern for integrated circuits. The miniaturization process and the package/silicon interaction result in an increase of the thermo-stresses whilst the use of new low-k materials, both degraded mechanical properties, makes it more and more difficult to predict their in-service behavior. Cross-sectional nanoindentation (CSN) has been successfully used so far to characterize interfacial adhesion in blanket thin films. In this paper, a modification of this technique is introduced to characterize adhesion and crack propagation in interconnect structures. The new technique is called modified cross-sectional nanoindentation (MCSN) and, as in conventional CSN, a Berkovich indenter is used to initiate fracture in the interconnect structure near the interconnect structure. The cracks propagate through this structure, preferentially along the weakest interfaces in the system. In this novel technique, an FIB (Focused Ion Beam) workstation is used for sample preparation, to machine a trench parallel to the indented surface. In this way, crack growth can be better controlled, and the process may be modeled in two dimensions. The technique has been applied to test chips simulating interconnect structures, with different types of etch-stop (ES) films and different metal densities. The results obtained using this technique correlate well with the interfacial adhesion measured by four-point bending (4 PB) in blanket films. The MCSN technique proposed in this paper is better suited to study local adhesion in patterned structures and has also proven useful for the study of crack propagation through the interconnect structure, making it possible to assess the effect of metal density on the overall behavior of the crack. FE modeling of the stress fields in the immediate vicinity of the crack tip has been carried out to understand the crack paths observed.

**9:15 AM B1.2**

Mechanics of Advanced Interconnect Structures. **Zhigang Suo,**

Division of Engineering and Applied Sciences, Harvard University, Cambridge, Massachusetts.

This talk draws on recent experiments and theories concerning the mechanics of integrated structures (Jun He and Z. Suo, Statistics of Electromigration lifetime analysis using a deterministic transient model, Jun He, Guanghai Xin, Z. Suo, Experimental determination of crack driving forces in integrated structures, Preprints are available online: www.deas.harvard.edu/suo, publication 163 and 164). The interconnect structures on the microprocessor chips are undergoing significant changes in recent years. In particular, a family of low-permittivity dielectrics, the organosilicate glasses (OSGs), have been integrated into the interconnect structures. The OSGs have low toughness and low elastic moduli, so that the interconnects are susceptible to cracking and electromigration damage. In principle, the crack driving force G can be calculated by solving an elasticity boundary value problem. In practice, however, such a calculation is prohibitively difficult for integrated structures of complex geometry, diverse materials and small features. On the other hand, this costs little to make many replicates of an integrated structure, so that massive testing is affordable. We describe an experimental method to measure G. We will also describe a new approach to analyze electromigration.

challenges for next technology nodes involve the introduction of low and ultra-low-k dielectric materials, smooth and non-stoichiometric interfaces from atomic layer deposition, and the effect of interconnect architecture including length-scales, aspect ratios, and metal density. These problems are compounded by the generic problem of packaging fragile interconnect structures. Materials and interfaces are nearly always optimized for other desired properties (e.g. dielectric properties or diffusion resistance) and the resulting effects on mechanical performance can be significant. In this presentation, the mechanical and fracture behavior of representative blankets and patterned thin-film structures including dielectrics, barriers and underlayers are examined. The acceleration of crack growth in complex chemical environments and under thermomechanical loading is typically encountered during processing is discussed. The effects of interface parameters and material composition and porosity will also be considered. Novel strategies to toughen fragile materials and interfaces in discussed. Finally, the effect of more complex patterned thin-film structures are examined where length scales are restricted in more than one dimension. Implications for device reliability, integration of new materials, and life prediction are discussed.
Semiconductor industry needs a continuously improving of integrated circuits performance and an increase of integrated density on silicon. The International Technology Roadmap for Semiconductors (ITRS) Roadmap underlines the need of dielectric silica nanocomposite material for ILD with dielectric constant (k) lower than 3 for the 90 nm node and than 2.4 for the 45 nm node. In this work, porous films with k value lower than 2.2 were deposited using a mixture of tetraethoxysilane (TEOS) and organic nanoparticles as porogen. After deposition and baking, this composite was thermally cured to allow the porogen degradation and matrix crosslinking and then form the porous structure. Different k values were obtained by varying the porogen percentage in the composite. In this work, mechanical properties of the composite and the porous films (before and after porogen removal respectively) were investigated using nanoindentation analysis and FTIR for different porogen loading (between 0 % and 40 %). It is shown that the composite modulus is higher than the porous film modulus for high porogen loading. The evolution of hardness versus porogen loading underlines that the porous films mechanical properties are better than dense one for each porogen loading due to better matrix crosslinking. The mechanical properties were modeled using foam mechanical models. Different configurations were investigated to simulate the film structure (cubic or tetraalkylated cubical cells, open or closed porosity, compression or tension axis). In porous film, the hardness analysis underlines that a good model agreement is obtained with closed cells for the low porosity film and with open cells for high porosity samples. The best Young modulus fitting is obtained with tetraalkylated cubical cells. This works in good agreement with porogen content. For each film, the nanoindentation measurements were performed in order to obtain precise informations of the matrix crosslinking. This analysis allows to propose a correlation between the matrix crosslinking and the mechanical properties of porous MSQ films. The Young modulus, average density, average pore size, and pore connectivity are investigated. For each sample, the same porogen loading contents show more obvious adsorption/desorption hysteresis loop in the XRP isotherms, suggesting that pores in those samples are more interconnected. In addition, adsorption and desorption of TP samples occur at narrow range of partial pressure, while NG samples display broader adsorption curves over wide partial pressure range. These results indicate that TP samples have a narrow PSD. TP samples show prominent peaks in the SANS and XRR data, characteristic of ordered structures. The pore spacings are 140 Å and 158 Å for the 20 % and 40 % porogen loading respectively. NG samples display relatively low scattering intensities, indicating smaller pore size. Average pore size of 20 % and 50 % NG samples are analyzed to be 17 Å and 80 Å in diameter, respectively.
SESSION B1: Low-K Dielectrics: Integration Issues

11:30 AM B1.1

Nanoporous low-k materials are critical for advancing microprocessor performance along the path of Moore's Law. Today, resistance-capacitance (RC) delay in back-end-of-line (BEOL) interconnects can limit microprocessor operation, necessitating improvements in both transistor and interconnect performance. BEOL performance enhancement has motivated the industry's transition from Al to Cu interconnects, and it also drives the integration of dielectric materials with lower dielectric constant (k-value). For decades, silicon dioxide (which has a k-value of ~4.0 - 4.2) was the insulator of choice. Fluorine-doped oxide was then introduced to lower the k-value to ~3.7, but adhesion and corrosion limited the F doping and k-value reduction. Carbon-doped oxide (or organosilicate glass (OSG)) allow for greater C doping and k-values as low as ~2.5. OSG materials with k < 3.0 in production now or will be soon, but future technologies are demanding even lower k-values. Further reducing the k-value of OSG materials requires the introduction of air into the film in the form of nanopores, but the introduction of pores creates many integration challenges. This talk will focus on some of the key challenges of using nanoporous materials as dielectric insulators in advanced microprocessors. These challenges include 1) controlling etch profiles, 2) difficulties in integrating nanoporous films due to their low mechanical strength, 3) difficulties in depositing a continuous metal layer onto a nanoporous surface, and 4) the susceptibility of nanoporous materials to damage by reactive plasmas used during microfabrication and methods to repair this damage. The talk will review research into controlling trench bottom roughness induced by etching and its relationship to pore size, maximizing mechanical strength by engineering optimal pore structures, sealing nanoporous surfaces, and repairing plasma damage using silylation chemistry.

2:00 PM B1.2

Hydrogen containing plasmas are being used to replace damaging oxidizing plasma for resist ashing in the integration of low to ultralow-k SiCOH dielectrics in the interconnect structures of ULSI devices. While the reducing hydrogen plasmas are less damaging to the SiCOH material than the oxidizing plasmas, they interact nevertheless with the dielectric and modify its characteristic. The current work investigated the interactions of hydrogen plasmas with ultralow-k porous SiCOH (pSiCOH) films and the dependency of these interactions on the values of the dielectric constant and on the porogen used for the pSiCOH film. The effect of the substrate temperature has also been investigated. pSiCOH films of similar dielectric constants have been prepared by plasma-enhanced chemical vapor deposition (PECVD) using the same SiCOH precursor but two different organic porogens. The films exposed to the hydrogen plasmas have been characterized by optical techniques (FTIR spectroscopy and n&k measurements), shrinkage characterization, and electrical measurements on MIS structures. It was found that the hydrogen plasma modifies the structure of pSiCOH's oxide skeleton and reduces the concentration of the Si-CH3 bonds, resulting in an increase of the dielectric constant. The degree of modification, for films prepared from same precursors, is larger for films with lower dielectric constants (k<) and is affected by the porogen used to prepare films with similar k values.
To metallization H. nm) pore interconnection length Thickness RH barrier silica films results in increased Roy, 10°. The differential IR spectrum, 9%) in amide degrading of Low-k (k~2.2). W. W is about 17% of the total absorbance of the initial Induced by He Plasllla. Ken-ichi Yanai, Tadayoshi that., 00 (~300 helieven Requirement of nm in from the PM B2.4 Lei charact.eri7,at.ion filmls often exhibit extensive loss of carbon species after plasnla treatment. The EFM images on cross sections and feather sections which the photoresist was removed by an oxygen plasnla (ash) treatment. The EFM inlages on cross sections and feather sections that allows a high fraction of the positronium (Ps) to diffuse into vacuunl. With optinlized plasma time, a very thin skin layer (~10 nm) can be formed without causing noticeable damage to the bulk of the low-k films (confirmed by FTIR). Substantial performance improvement was observed in the thin Ti barriers formed on the plasma induced non-porous skin layers.

First Pass Study of Surface Modified Porous Low-k by Ion Implantation for Zero Thickness Barrier Requirement of Cu/MSQ/Si Stacks in Copper Metallization Scheme. Akira Nishimura, U. Sato, Zobin F. Patel and H. Bakhru; Physics, SUNY, Albany, Albany, New York. Thin films of Ultra-Low k materials such as porous MSQ (k=2.2) were implanted with argon 1 x 1016 cm-2 dose at energies varying from 20 to 200 keV at room temperature. The surface hardness of the porous films can be improved five times as compared to the as-deposited porous films by implanting Ar with 1 x 1016 cm-2 doses at 20 keV, sacrificing only a slight increase (~6%) in dielectric constant (e.g., from 2.2 to 2.4). The hardness persists after 450 OC annealing. The ion implantation process suppressed the moisture uptake in the porous low k films. Surface chemical modification made the films hydrophobic. In this paper, ion implantation strategy was pursued to create a Si02-like surface on MSQ. The effects of implantation parameters on the barrier property and bulk stability of MSQ were then studied. The results reveal one possible route to attain the zero barrier thickness requirement for interconnect systems.

2:45 PM B2.5 Surface Pore-Sealing in Porous MSQ Low-k Film using NH3 Plasma Treatment. Weide Wang1, Donghui Chi1, Jun Liu1, Lei Wang1, Soojin Chua1, David W. Gildey2 and Albert F. Yee2. 1Institute of Materials Research & Engineering, Singapore, Singapore; 2Department of Materials Science and Engineering, University of Texas, Austin, Texas; 3MEMS of Texas Instruments, Dallas, Texas. Films with interconnected mesopores pose a serious challenge for the integration of porous low-k dielectric films into low-k/Cu interconnect scheme due to the difficulty of forming a thin, effective Cu diffusion barriers (e.g., Ta) on the sidewalls of vias/trenches. To improve the integrity of the Cu diffusion barrier, the sidewalls of the vias and trenches must be sealed before barrier deposition. In this paper, we report the formation of a thin, non-porous surface layer on a porous methyl-silanesilazane (MSQ)-based dielectric film by NH3 plasma treatment. The porous MSQ films used in this study are Shipley’s Zirkon 2200 low-k (k=2.2). Depth profiling using beam-PALS (positronium annihilation lifetime spectroscopy) characterization showed that the pores in the thin layer have an average diameter of 2.7 nm but with a much longer (~300 nm) pore interconnection length that allows a high fraction of the positronium (Ps) to diffuse into vacuunl. For the surface modification of the film, a low frequency (50.0 Hz, 400.0 kH) NH3 plasma treatment was carried out. The formation of a thin non-porous surface layer by NH3 plasma treatment was deduced based on the observations of (1) the curvature of Ps diffusion into vacuumn at every implantation energy and (2) an implantation energy-independent Ps/Ps capture value also matching well with that of Ps formed in the non-plasma treated films with a 100 nm Si capping layer. From the SIMS depth profiling, it was found that the surface region is C-depleted, but with N incorporation, after NH3 plasma treatment. Cross-sectional TEM clearly showed the presence of modified surface layer with the thickness almost equal to that of C-depleted layer. It is believed that the C-depleted layer is indeed non-porous in nature, thus preventing the escape of Ps from the film into vacuunl. With optimized processing parameters, e.g., 300 oC substrate temperature and 10 s plasma time, a very thin skin layer (~10 nm) can be formed without causing noticeable damage to the bulk of the low-k films (confirmed by FTIR). Substantial performance improvement was observed in the thin Ti barriers formed on the plasma induced non-porous skin layers.

2:15 PM B2.8 Double-layered Structure of Surface Modification of Low-k Dielectric film by He Plasma and NH3~NH3 Plasma Treatment. Yoshiaki Hasebe, Kouji Suniya, Seiichi Ogumi and Kazutake Koga; Consortium for Advanced Semiconductor Materials and Related Technologies, Kokubunji-shi, Tokyo, Japan. Helium (He) plasma treatment of low-k dielectrics is usually used in Cu/low-k interconnect integration to improve adhesion to the cap Si02 layer. To control this treatment precisely without degrading the dielectric film, a fundamental understanding of surface modification induced by He plasma is essential. Thus, the changes in chemical bonds and atomic composition of the modification layer induced with different He plasma powers were investigated using infrared spectroscopy (IR), X-ray photoelectron spectroscopy (XPS) at different take-off angles, 90° and 10°. The differential IR spectrum measured at the SiOC film treated with He plasma, compared to the reference of that without the plasma treatment, exhibits a decrease in the absorption peaks at 1272 and 1077 cm-1, which arise from the Si-CH3 bond, and an increase in the absorbance of the peaks at 892 and 992 cm-1, which arise from the H-Si-O bond. With increasing He plasma power, the peaks of the Si-CH3 bond decrease and those of the H-Si-O bond increase monotonically. The decrease in the absorbance of the Si-CH3 bond of the SiOC film irradiated by He plasma at 300 W is about 17% of the total absorbance of the initial SiOC film when it is 92 nm thick. The surface modification layer is etched away with the mixed H2 solution, whereas the SiOC film is not etched. The thickness of the modification layer, estimated from the etch depth, is 17 – 18 nm in the case of the He plasma at 300 W. In contrast, the decrease of the absorbance of the Si-CH3 bond evaluated from IR, almost all of the Si-CH3 bonds in the modification layer are broken using the He plasma. The etching behavior at the beginning of the treatment changes largely with the plasma power. Etching starts at some time interval in the case of the samples irradiated at over 300 W, whereas etching starts immediately in the case of irradiation at 100 W. This suggests that some further modification on the top surface takes place with the irradiation over 300 W. The atomic ratio of O/Si estimated from XPS spectra increases with He plasma treatment, resulting in a Si02-like composition. The atomic ratio of C/Si decreases with the irradiation by He plasma at 100 W, indicating that some carbon species, which originate from the broken Si-CH3 bond, are sputtered away from the film. In the case of the irradiation at 300 W, the respective ratios of C/Si, estimated from the spectra at the take-off angles of 90° and 10°, are almost the same as or larger than that of the film without He plasma, indicating the depth profile is not homogeneous. In consideration of the escape depth of the photoelectron at each take-off angle, the top surface to be less than 1 nm of the modification layer changes to a carbon-rich composition, causing a double-layered structure in the modification layer. This work was supported by NEDO.

Nanoscale Observation of Dielectric Damage to Low k MSQ Interconnects from Reactive Ion Etching and Ash Treatment. Todd S. Grong1, Shuoning Yao1 and Sri Satyanarayana2; 1Mechanical Engineering, New University of Hampshire, Durham, New Hampshire; 2SEAMECH, Austin, Texas.

Electrostatic force microscopy (EFM) was used to measure the extent of dielectric damage from plasma processing of nanoporous, low k materials. Reactive ion etching (RIE) was used to etch nanoporous MSQ interconnect structures with approximately 50 nm spatial resolution. Single layer patterns were formed in 200 nm thick MSQ films by reactive ion etching (RIE) and were subsequently backfilled with an MSQ layer that was not exposed to plasma to act as a reference. The backfill was performed on as-etched structures with the photoresist intact and on structures in which the photoresist was removed by an oxygen plasma (ash) treatment. The EFM images on cross sections and feather sections show that the RIE penetrates ~100 nm into the sidewall and that the redeposited polymer had a higher k than the MSQ (k~2.2). The ash treatment damaged the MSQ everywhere. Experiments are underway to determine if the ash damage results from diffusion of oxygen through the nanoporous network or through the SiC hardmask.

Observation of Intrusion Rates of Hexamethyldisilazane during Supercritical Carbon Dioxide Functionalization of Triethyloxysilane. P. M. Cap1, B. P. Gorman1, R. F. Reidy1, D. W. Mueller2,1, E. R. Walter2, P. D. Matz3, J. T. Rhond4, and E. L. Burch5; 1Materials Science and Engineering, University of North Texas, Denton, Texas; 2Physics, University of North Texas, Denton, Texas; 3Silicon Technology Development, Texas Instruments, Inc, Dallas, Texas; 4S EM ATECH, Austin, Texas.

Water adsorption by porous low-k silica films results in increased dielectric constants and is often due to silanol groups on the pore surfaces. Reacting the silanols with silylating agents (e.g., hexamethyldisilazane (HMDS) and trimethylchlorosilane (TMCS)) in supercritical CO2 (SC-CO2) can increase film hydrophobicity and can other groups have shown that the silylating agents do not deeply penetrate the porous films by implanting Ar with 1 x 1016 cm-2 doses at 20 keV, sacrificing only a slight increase (~6%) in dielectric constant (e.g., from 2.2 to 2.4). The hardness persists after 450 OC annealing. The ion implantation process suppressed the moisture uptake in the porous low k films. Surface chemical modification made the films hydrophobic. In this paper, ion implantation strategy was pursued to create a Si02-like surface on MSQ. The effects of implantation parameters on the barrier property and bulk stability of MSQ were then studied. The results reveal one possible route to attain the zero barrier thickness requirement for interconnect systems.
S-CH$_3$ (1275 cm$^{-1}$) and CH$_2$ (2980 cm$^{-1}$) because all carbon related IR absorptions result from silylation. To observe these changes as a function of time, Celgard films have been treated with SC-CO$_2$ at 7 MPa and HMDMS (and other silylating agents) at different temperatures and pressures in an in-situ (supercritical) Fourier transform infrared (FTIR) spectrophotometer cell. After supercritical silylation, the TES films have been treated with FTIR spectroscopy to note improvements in film hydrophobicity, capacitance-voltage (C-V) measurements to determine dielectric constants, ellipsometry to study changes in film porosity, and dynamic secondary ion mass spectrometry (DSIMS) and X-ray photoelectron spectroscopy (XPS) to chemically characterize the films as a function of depth.

4:00 PM B2.8


Materials Science and Engineering, University of North Texas, Denton, Texas; $^2$Physics, University of North Texas, Denton, Texas; $^3$SEMATECH, Austin, Texas; $^4$Silicon Technology Development, Texas Instruments, Inc., Dallas, Texas.

To integrate porous low-κ films into the 45 nm technology node, metal intrusion into film pores must be prevented because it diminishes the insulating properties of the film by increasing its conductivity. Metal species penetration into porous films can be prevented by reacting film surface silanes with silylating solutes in a supercritical CO$_2$(SC-CO$_2$) solvent. It has been shown by our and other research groups that SC-CO$_2$ provides effective transport of bulky organic groups into low κ pore surfaces. In this study, a series of heat and chemical treatments were performed to observe the effectiveness of using SC-CO$_2$-based silylation agents and their effect on processing temperatures. The samples were heated to 400 °C to condense adjacent or vicinal silano groups into bridged oxygen species. C-V measurements were conducted to observe the change in κ with respect to silane treatments. The experiments were then treated with a series of silylating agents (R$_2$Si-CI) with R=CH$_3$, C$_2$H$_5$, CH$_3$C$_2$H$_4$, CH$_3$H$_2$, and C$_2$H$_4$ to observe their relative abilities to react with the remaining surface hydroxyls. Surface coverage of the silylating agents was examined using contact angle and X-ray photoelectron spectroscopy (XPS) measurements. In addition, contact angle experiments revealed that the hydrophobicity of the films was diminished by heating the films to 400 °C due to the presence of available reaction sites used in the SC-CO$_2$ treatments. To study the impact of surface coverage, a TiN CVD precursor was used to assess the ability of heat treatments and silylation to seal the pores. Cross-sectional scanning electron microscopy (SEM) and dynamic secondary ion mass spectroscopy (DSIMS) were used to view TiN penetration into the pores and capacitance-voltage (C-V) measurements were performed on the samples to calculate the change in κ value.

4:15 PM B2.9

The Deposition of Alkynylene Oxide Sealing Layers on Porous Methylsilsesquioxane Films Using Supercritical CO$_2$. Bo Xie and Anthony Muscat.

Chemical & Environmental Engineering, University of Arizona, Tucson, Arizona.

Porous methylsilsesquioxane (p-MQS) films (JSR LKD 5109) were treated with alkylidymethylchlorosilanes with alkyl chain lengths of one to six carbons and dissolved in supercritical carbon dioxide to repair oxygen ashing damage and seal the pores in the film. Monochlorosilanes were delivered by using supercritical CO$_2$ at 150-300 atm and 50-60 °C for 2 min. Porous transform infrared (FTIR) spectroscopy showed that there were no carbon atoms dissolved in supercritical carbon dioxide to repair oxygen ashing damage and seal the pores in the film. Monochlorosilanes in the range 78-103 ppm were delivered in supercritical CO$_2$ at 150-300 atm and 50-60 °C for 2 min. Fourier transform infrared (FTIR) spectroscopy showed that the trimethylsilylchloro (TMSC), butylidymethylchlorosilane (BDMCS), octyldimethylchlorosilane (ODMCS), decylidimethylchlorosilane (DDMCS) and octadecylidimethylchlorosilane (ODDCMCS) reacted with both Si-OH and Si-H bonded (Si-OH) silanol groups on the surfaces of the pores. The TES films were treated with Si-O-Si bonds with the surface. The FTIR analysis indicated that self-condensation of alkysiloxanes produced a liquid film on the surface, which was partially removed by a second treatment with SC-CO$_2$. The contact angle increased with the peak at 1116 cm$^{-1}$ and a distinct shoulder at 1010 cm$^{-1}$, which are characteristic of the O-Si-CH$_3$ stretching band. The enhancement in the intensity of the peak at 1116 cm$^{-1}$ and a distinct shoulder at 1010 cm$^{-1}$, which are characteristic of the O-Si-CH$_3$ stretching band. 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porous low k layer were investigated. Electrical performance of the second level of metal was used to choose a dual damascene etch process. Cyclic or not, seenS not to have an impact on the dielectric constant. While achieving low k through the nano-porous approach, it is critical to maintain the mechanical strength at a level that will ensure stable integrated multi-level metal structure. Carbon doped dielectrics have a fairly uniform composition distribution through its thickness but has a significant depth gradient in pore structure. There is no porous structure on the top layer and the average pore size gradually increases with depth. The top dense layer provides strong adhesion to cap layers of SiC and SiCN as there is no delamination of the dielectric and metal layers. Continued scaling poses even greater obstacles, requiring innovative films and integration techniques. Good mechanical properties for both the bulk low k dielectric and related dielectrics comprising the film stack remain essential to produce a stable integral multi-level metal structure. Carbon doped dielectrics used in 50nm node devices achieved k<3.0 through the lower K decrease after cure, showing the porosity in the film. This work clearly demonstrates the ability of achieving an ULK by a PECVD process and approach using different precursors for the matrix and the porogen sacrificial phase. It also permits a better material behaviour understanding during hybrid deposition and during the curing.

SESSION B3: Low-K Dielectrics: Process and Integration Issues
Chair: Ting Tsui and Joost Vlassak
Wednesday Morning, March 30, 2005
Room 4004 (Moscone West)

8:30 AM B3.1
The Pore Structure and Integration Performance of a Porous CVD Ultra Low k Dielectric. Yufan Liu, Andreas Knorr1, Wen-Li Wu, David Gidldui and Bernd Kastenmeier; Intel Associate at SEMATECH, Austin, Texas; Intelmos Associate at SEMATECH, Austin, Texas; NIST, Gaithersburg, Maryland; University of Michigan, Ann Arbor, Michigan; IBM Associate at SEMATECH, Austin, Texas.

Low dielectric constant (k) materials are required for future generation integrated circuit technologies. The updated projection of k for 45 nm technology nodes and beyond would be less than 2.2. Introducing porosity and minimizing the atomic bond polarization in dielectric materials would allow the reduction in the dielectric constant of the materials. However, creating porous structures could have significant impacts on its property and integration performance in multilevel interconnect systems. Therefore, understanding pore structures and their impacts on property and integration performance is essential for material and integration process development. This paper presents the evaluation results on a porous PECVD ultra low k dielectric material ðk<2.5Þ. We have integrated the low k dielectric into a one level metal (copper) system and have evaluated the electrical characteristics and the integration performance during hybrid integration processing such as chemical mechanical planarization (CMP), plasma etch and ash. We have also conducted film structure studies and investigated the implication of the structure on integration performance. This SICOH based porous PECVD material has a fairly uniform composition distribution through its film thickness but has a significant depth gradient in pore structure. There is no porous structure on the top layer and the average pore size gradually increases with depth. The top dense layer provides strong adhesion to cap layers of SiC and SiCN as there is no delamination of patterned Cu/low k structures during the integration CMP process. The larger/open pore structures at the lower parts of the trench sidewalls received severe damages such as voids and carbon depletions during plasma patterning, which result in an unexpected high product of comb capacitance and resistive properties and high k effective of the integrated structure. Alternative patterning process, sidewall pore sealing, and modifying pore structures would be required to minimize the sidewall damages.

8:45 AM B3.2
Ultra Low K Pecvd Porogen Approach: Matrix Precursor Comparison and Porogen Removal Treatment Study. Laurent Faveau, Jean-Louis Vincent, Vincent Roussou; STMicroelectronics, Crolles, France; CEA / Leti, Grenoble, France; IEM, Montpellier, France.

The introduction of new dielectrics into silicon chip interconnection technology is marked by continuous revisions to meet the ITRS projection. Amorphous α-SiO(CH=K>2.9) deposited by Plasma Enhanced Chemical Vapor Deposition (PECVD) from silane-like precursors (was) could be used towards production. Using other precursors like silicones, K value can be reduced till to 2.5. However, sub-65nm technologies need K values below 2.5 but also an extendable material to further K values reduction. Introducing porosity is the only way to reduce the dielectric constant. This paper presents results concerning a two steps PECVD porogen approach to perform Ultra Low K (K<2.5). Firstly a dual-phase thin film is deposited by PECVD using two advanced precursors: a siloxane one, to create a α-SiO(CH=K>0.9) based matrix, and an organic precursor, i.e. the porogen, to create the sacrificial phase. The goal of this first step is to obtain a hybrid material: a matrix containing organic inclusions. In a second step, the porogen is removed by a suitable curing to generate porosity. In this work, cyclic and non-cyclic silicones were evaluated to create the matrix. Thin films were then fully characterized to understand chemistry influence. It is shown that it is possible to deposit hybrid material with both precursors. The silicone choice, cyclic or not, seems to have an impact on the dielectric constant. But FTIR analysis indicates that it may be determinant for interactions inside hybrid material and cross-linking phenomenon. Process study and physical characterisations were performed to well control ratio of organic phase incorporation. To better understand the porogen removal mechanism, different cures were investigated. Traditional cures under different resist conditions (N2, N2 plus O2, plasma with or without O2, different thermal ramp) were compared to a thermally assisted UV cure. Curing post treatments were done on different hybrid films (different precursors and porogen ratio). Using FTIR spectra and mechanical characterizations, it is shown that the curing step is a critical point because it combines two different phenomena: porogen removal (pores creation) and material cross-linking. The K value can be tuned by varying the porogen ratio and dielectric constant, lower than 2.3 are obtained. Nitrogen adsorption/desorption analysis and Grazed Incidence Small Angle Scattering allow to explain the K decrease after cure, showing the porosity in the film. This work clearly demonstrates the ability of achieving an ULK by a PEVCD process and approach using different precursors for the matrix and the porogen sacrificial phase. It also permits a better material behaviour understanding during hybrid deposition and during the curing.

9:00 AM B3.3
Film Properties and Integration Performance of a Nano-Porous Carbon Doped Oxide. Lester D’Arrigo, Sang Ahn, Yi Zheng, Josephine Chung, Nagarajan Ragujanpal, Thomas Nowak, Alex Demos, Girish Dixit, Derek Witty, and Hichem M’Saad; Dielectric Systems and Modules, Applied Materials, Inc., Santa Clara, California.

The semiconductor industry has witnessed a successful introduction of copper based interconnects and low permittivity insulators with 130nm node devices. The advent of 90nm node devices with even lower permittivity insulators such as carbon doped oxide (CDO) films resulted in increasingly complex integration challenges related to interfaces between the different dielectric layers, as well as between the dielectric and metal layers. Continued scaling poses even greater obstacles, requiring innovative films and integration techniques. Good mechanical properties for both the bulk low k dielectric and related dielectrics comprising the film stack remain essential to produce a stable integral multi-level metal structure. Carbon doped dielectrics used in 50nm node devices achieved k<3.0 through the lower K decrease after cure, showing the porosity in the film. This work clearly demonstrates the ability of achieving an ULK by a PECVD process and approach using different precursors for the matrix and the porogen sacrificial phase. It also permits a better material behaviour understanding during hybrid deposition and during the curing.

9:15 AM B3.4
Determining Pore Structure and Growth Mechanisms in Templated Nanoporous Low-k Films. Hua-Gen Peng1, Richard S. Valley1, Ming Liu1, David W. Gidldui2 and Jin-Hoong Yim2; IME, University of Michigan, Ann Arbor, Michigan; 2Materials Lab, Samsung Advanced Institute of Technology (SAIT), Yongin-Si, Gyeonggi-Do, South Korea.

Templating is one of the most popular methods for generating nanocomposite and nanoporous films and the resultant pore size and pore interconnection length depend strongly on the combination of host matrix and porogen used. Positronium Annihilation Lifetime Spectroscopy (PALS) analysis has been performed on carbosilane films produced using several cyclodextrin (CD) and Calix-arene (CA) porogen in a modified MSQ host matrix. PALS reveals the role of functional groups on the CD’s and CA’s in modifying the resulting pore structure, both size and interconnection length, as well as their stability. In this systematic study, three different pore growth modes were observed depending on the porogen-porogen and porogen-matrix interactions. A CD-based porous material (CSDC) and a CA-based porous material (CADC) exhibit different pore size distributions, with the former showing a broad distribution and the latter a bimodal distribution. These differences in pore size and pore interconnection length were attributed to differences in the cross-linking properties of the macromolecular templates. Further studies are required to understand the relationship between template structure and the resulting pore morphology.
producing longer interconnected pores of constant cross section. A second CD porogen with only methoxyl functional groups (tCD) has weakened Van der Waals interactions. The aggregation of the porogen domains is expected to be more 3-dimensional (pseudo-random), with isolated pores consistent with a template of the tCD molecular size at low porosity which then gradually increase in pore size and interconnectedness as the porosity is increased. Nanoparticle simulations using a random pore growth and nucleation model show consistent trends for pore size growth. The CA system, being amphotropic, acts like a surfactant and beyond some critical concentration should promote a larger pore domain growth. Experimental pore size distributions between 7% and 15% porosity is detected by PALS. These results clearly demonstrate three different aggregation modes with porogen concentration for the resulting nanopores; from isolated molecules to interconnected networks which is a key demonstration of the usefulness of PALS in untangling the fundamental pore structure and its evolution in porosity. PALS characterization of porosities provides novel feedback in understanding and design of nanomaterials.

9:30 AM B3.5

Nanometer-scale Pore Formation in a Polyphenylene Low-k Dielectric. Michael S. Silverstein1, Barry J. Bauer2, Ronald C. Heiden2, Hae-Jeong Lee3 and Brian G. Landers3, 1Materials Engineering, Technion - Israel Institute of Technology, Haifa, Israel; 2Polymers Division, National Institute of Standards and Technology, Gaithersburg, Maryland; 3Dow Chemical Company, Midland, Michigan.

Nanometer-scale porosity is being introduced into low-k dielectrics in an attempt to achieve interlevel metal insulators with permittivities of less than 2.0. This paper presents an extensive study of the pore formation and to characterize the porous structure. This work investigates pore formation in a low-k dielectric based on pyrolysis of a porogen (20 % by volume) in a polyphenylene matrix. One unique aspect of this work is the description of the nanoscale pore formation at various stages of pore formation through the use of a deuterated porogen. The combination of x-ray reflectivity (XRR) and small angle neutron scattering (SANS) was found to be a powerful technique for describing the changes in the material during porogen degradation and pore formation. The average radius of the porogen domains was approximately 90 Å and the size distribution was relatively broad. The smaller nanoscale pore domains collapse during degradation, while the larger domains tend to yield stable pores. The collapse produces a significant reduction in film thickness, a porosity that is significantly smaller than the porogen content, a pore size distribution that is narrower than the porogen domain size distribution and an average pore size of approximately 80 Å SANS porosimetry using a match point solvent and XRR porosimetry were used to provide more information regarding the pore size distribution.

10:15 AM *B3.6

Channel Cracking in Low-k Interconnect Structures. T. M. Shaw1, Xino Hu Liu1, Michael Lane3, Robert Rosenberg2, Sarah L. Laro3, James Doyle1, Darryl Restaino2, Steven Vogt3 and Daniel Edelstein2; 1IBM Research, Yorktown Heights, New York; 2Axcelis Technologies, Inc., Woburn, Massachusetts; 3Polymers Division, National Institute of Standards and Technology, Gaithersburg, Maryland.

The drive to reduce the dielectric constant of dielectrics for backend of the line structures has resulted in a corresponding reduction in their mechanical strength. As a result of this reduction in strength dielectric films have become more susceptible to channel cracking driven by tensile stresses in the films. Recent theoretical studies have suggested that the critical thickness for cracking can be substantially reduced by the presence of patterned structures under a blanket dielectric film. In particular, narrow gaps between metal features are expected to greatly reduce the critical thickness for channel cracking. As such features are common in multilayer interconnect structures, it is important to quantitatively establish the conditions in which to establish channel cracking for specific interconnect geometries. We have used finite element analysis to examine the susceptibility of different geometries to channel cracking and shown that for realistic interconnect structures the crack driving force can be enhanced by more than an order of magnitude over that for a blanket film. Thickness and modulus of the dielectric underlayer as well the location and spacing of metal features all contribute to the enhancement. Based on the analysis we have built multi-layer test structures exhibit the predicted enhancement. From measurements of crack velocities under controlled environments we have been able to confirm the key features of the model. In particular we have shown that the behavior is quantitatively in agreement with an elastic model which stresses arise from thermal expansion mismatch of the dielectric and the metal interconnect. Details of our analysis and experiments will be given in the talk and used to discuss the effects that grain structure and plasticity have on the crack driving force with different interconnect geometries.

10:45 AM B3.7

The Size Effect of Nanoporous Porogen on the Mechanical Properties of Nanoporous Low-k Dielectric Films. Sung-Kyu Min1, Jae Jin Shin1, Se Jung Park1, Dongjin Moon2, Do Young Yoon2 and Hae-Woo Rhee2; 1Department of Chemical & Biomolecular Engineering, Sung-Ang University, Seoul, South Korea; 2Department of Chemistry, Seoul University, Seoul, South Korea.

Although there are a lot of nanoporous low dielectric materials prepared by organosilica matrix and sacrificial porogen, for example, star-shaped poly(copolyalactone) and surfactants, they have been limited to use as interlayer dielectrics for the next generation semiconductor because the increase in the porosity seriously decreases the mechanical strengths of nanoporous low-k films such as elastic modulus and surface hardness. Therefore, it is important to minimize the decrease in the mechanical strengths upon the porosity by controlling pore morphologies like pore size and its size distribution. In search of this, we used two different sizes of nanoparticulate porogen based on the glucose unit. The porogens were functionalized through allylation and hydroxylation reactions and the matrix used was poly(methyltrimethoxy silane-co-bistriethoxysilyl) ethane) (poly(MTMS-co-BTSE)) Ethane. Even though the increase in the porosity led to decrease in the k value, triethoxysilylethane (TESGC) resulted in much higher mechanical strengths than triethoxysilyl 1-cyclohexadetrin (TESCD) due to the smaller pore size.

11:00 AM B3.8

Fracture Property Improvements of a Nanoporous Thin Film in the Presence of Deposition Bond Modifications. Joseph M. Jacques1, Timothy T. Teui2, Andrew J. McKenna1, David H. Kraft1 and Steven Vogt3; 1Materials Science and Engineering, Texas Instruments, Inc., Dallas, Texas.

As silicon-based microelectronic devices continue to aggressively scale down in size, traditional high-k dielectric materials are no longer feasible due to their relatively high dielectric constant. For 90 nm node devices, the group of materials known as organosilicate glass (OSG) has emerged as the predominant choice for intermetal dielectrics. A potential failure mechanism for this class of low-k dielectric films during the manufacturing process is catastrophic fracture due to channel cracking. The driving force for channel cracking is dependent on several film properties, including the modulus and residual tensile stress. The use of an electron beam curing process is being evaluated within the semiconductor industry as a means for improving the mechanical strength of these silicon-based materials. Within this work, the effects of curing dose (micro-C/cm²) upon the mechanical properties of OSG thin films were characterized. For a set process voltage and current, linear relationships exist between the dose and several mechanical film properties. However, at very high curing doses, a highly concentrated surface region forms, resulting in dramatically different film behavior. Channel crack growth velocities were also measured for these cured materials. As the cure dose is increased, the crack growth rate decreases according to a power-low relationship. The structural film changes induced by the electron beam cure process are addressed, focusing on their impact upon the mechanical strength of OSG thin films.

11:15 AM B3.9


The introduction of considerable amounts of porous volume in dielectric films is the most promising route for achieving low-k materials for microelectronics, but it leads invariably to a substantial decrease of the mechanical strength of such films. This issue poses serious constraints onto the overall mechanical stability of low-k based interconnects. One ideal solution to enhance the stiffness of porous films and still preserve their low-k characteristics, would be to maximize the degree of cross-linking of the matrix material without affecting the porous volume. Exposure of dielectric thin films with appropriately chosen energy levels can be used to promote such cross-linking mechanisms in a controlled fashion, so to avoid significant film densification. This study looks into the effects of UV cure onto the properties of 300 to 700nm thick blanket microporous SiOC:H films with various pristine k values. The most effective cure condition investigated leads to about 50% increase in elastic modulus and hardness. The same increase trends in elastic modulus are observed with both nanoindentation and Surface Acoustic Waves, although the SAWs values are typically 20-30% lower.
than those from nanoindentation. Strain energy release rates upon fracture as measured with four-point bending show a clear increase for stacks containing UV-cured SiOCH films. Only minor film shrinkage (~4%) and increase in film density (from 1.48 g/cm³ to 1.52 g/cm³) are associated with this cure condition, as well as a minor increase of the k value to about 3.15. Structural and compositional changes in the SiOCH film are studied by Ion Elastic Recoil Detection and solid state Nuclear Magnetic Resonance analysis.

11:00 AM B3.10
Effect of Plasma Treatment and TMCTS Vapor Annealing on the Reinforcement of Porous low-k Films. Kazuo Kohnara1, Hirofumi Tanaka2, Shunsoke Oike1, Massami Murakami1, Tetsuo Ono1, Yutaka Seino2 and Takamakiko Kikawa1,2,3; 1 MIRAI-ASET, Tsukuba, Japan; 2MIRAI-ASRC-AIST, Tsukuba, Japan; 3RCNS, Hiroshima, Japan.

The aim of the present study is to improve the elastic modulus of the porous silica used in the BEOL (buried-oxide) dielectric layer, by creating the stress in the dielectric layer to be compressive, and by increasing the hardness of the dielectric layer. It is shown that the mechanical strength of the porous silica films was significantly enhanced by a novel process of TMCTS vapor annealing combined with a plasma treatment. The TMCTS treatment was performed at 400°C in nitrogen ambient followed by the argon plasma treatment under the pressure range of 0.3 to 2.0 Pa for 40 sec. The elastic modulus of the porous silica film with TMCTS treatment significantly increased after the plasma treatment. Furthermore, after the second TMCTS treatment was carried out, both the elastic modulus and the hardness of the film were enhanced by a factor of 4, as compared with those of the starting film. FT-IR analysis indicated that Si-CH3 and Si-H groups on the porous silica wall surfaces were converted to Si-OH groups after the argon plasma treatment, indicating that the pore wall surface became more reactive with TMCTS vapor after the argon plasma treatment. Thus the porous silica wall surface was covered by TMCTS polymer network and became more hydrophobic. Consequently the refractive index increased by about 5 % and the elastic modulus increased by a factor of 4, while k-value was kept almost constant.

11:45 AM B3.11
High Strength Low Dielectric Constant Aromatic Thermosets. Yongqing Huang and James Cho, Ravi Saxena, William N. Gill and Joel L. Plawsky; Department of Chemical and Biological Engineering, Rensselaer Polytechnic Institute, Troy, New York.

Continuing miniaturization of microelectronic devices requires development of low dielectric constant materials to lower the RC delay, power dissipation and crosstalk. Although spin-on polymer dielectrics have better potential for extendability to lower dielectric constant (k) values compared to chemical-vapor-deposited dielectrics, their low mechanical properties prevent them from being successfully integrated with copper metal lines. Recent evaluation of a new thermosetting oligomer shows high thermal stability, low moisture pick-up and low dielectric constant. Techniques to optimize the solubility and spin coating characteristics of the oligomer have been developed. Thermally cured polymer displayed a thermal stability up to 480°C in nitrogen and 400°C in air. The cured polymer displayed a dielectric constant of 2.7 at 1 MHz and a breakdown strength larger than 230 V/μm. Non-oxidative testing showed that it had an extraordinarily high Young's modulus of 16.8 GPa and a hardness of 3.5 GPa. By use of porogens, a dielectric constant as low as 1.85 was obtained while still maintaining an acceptable high Young's modulus of 7.7 GPa and hardness of 2.0 GPa. Nonossratch testing indicated that this material had good adhesion to the Si substrate, and Ta which is a diffusion barrier for copper. These results appear unique compared to all commercially available low-k candidates.

SESSION B4: Reliability of Low-K Dielectrics
Chair: Tom Shaw
Wednesday Afternoon, March 30, 2005
Room 2004 (Mocone West)
1:30 PM B4.1
Constraining Effects on Cohesive Failures in Low-K Dielectric Thin Films. Ting Y. Tsui and Andrew J. McKerrow; Silicon Technology Development, Texas Instruments Inc, Dallas, Texas.

With increasing demands on interconnect performance the semiconductor industry is replacing traditional BEOL dielectrics with materials characterized by a lower dielectric constant. At the 90 nm node organosilicate glasses (OSGs) are one class of materials that have been extensively evaluated as candidate intermetal dielectrics. A potential mechanical failure mode for these silicon-based, low-k dielectric thin films during interconnect fabrication is channel crack formation, of which the major driving force is residual tensile stress in the film. Even if the film does not crack catastrophically immediately after deposition, time-dependent failures can occur via stress-corrosion cracking. This phenomenon is commonly referred to as environmentally-assisted crack growth. In this work, next generation ultra low k dielectrics are expected to be more compliant and fragile than the materials used for the 90 nm technology node. To demonstrate this, a five-metal-layered dielectric stack was built using a low-cK dielectric that has a measured crack velocity of 10^-3 mm/s, for an OSG film deposited on top of this stack. Results show that crack growth rate was 1000 times faster than the equivalent experiment performed on a film stack prepared using low-k dielectrics. The implication of this significant increase in crack opening force will be discussed.

2:00 PM B4.2
Integration and Reliability Issues Using Novel ULK Spin-on Dielectric Schemes. Neil H. Schmitz, Gregory Smith3, Ward Engbrecht1,2, Sanjit Das1,2, Kyle Neuman and Mike Gaughen2; 1 Texas Instruments, Dallas, Texas; 2IBM, Hopewell Junction, New York; 3SEMA TECH, Austin, Texas; 4Freescale Semiconductor, Austin, Texas; 5 Rohm and Haas, Marlborough, Massachusetts.

Reliability (BTS/EM/SM) of various integration schemes of porogen activated mesoporous ULK spin-on ILD/hard mask (kint=2.5) are examined. Correlations are drawn between ramped breakdown voltage, packaged wafer level reliability testing methods. A promising ULK scheme is shown and discussed. Wafer level BTS measurements were made in a tester with a 300nm thermally controlled chuck, at temperatures ranging from 25-300°C, and voltages ranging from 12-23V. Packaged BTS data was run in either hermetically sealed packages, or in an N2 ambient at 250°C/15V. Integration schemes tested included ILD/low-k organic etch stop layer, and ILD/spin on silsesquioxane hard mask. Various barrier thicknesses were also tested in the integrations. A good correlation between leakage at low voltages in the ramped breakdown voltage tests on sputter structures, and lifetimes at temperature in BTS is found. With the proper integration scheme, high reliability can be achieved with an ultra low-k process flow.

2:15 PM B4.3

This work is aimed at understanding the nature of the interactions between metal interconnects and SiO2 in integrated circuits. Cu diffuses readily in SiO2 and Si creating a reliability concern. The mechanism of Cu diffusion in SiO2 and low-k dielectrics is still a matter of controversy. We have shown that the diffusion of Cu in inorganic dielectrics depends strongly on the moisture content and defect concentration of the dielectric. In this paper we study the time dependence of Cu oxidation in SiO2 using solid-state impedance spectroscopy. In an experiment, bias-thermal-stressing is applied to Metal-insulator-Capacitors to induce oxidation and diffusion of Cu mobile charges into the dielectric. The frequency response of the dielectric layer is studied before and after stressing. An equivalent circuit model to describe the system is developed and constants for the mechanism of Cu diffusion at the interface and bulk of the dielectric are derived.

2:30 PM B4.4
Barrier Integrity Effect on Leakage Mechanism and Reliability of Copper/OSG Interconnects. Yunlong Li1,2, Zsolt Tokoi1 and Karen Macx1,2; 1IMEC, Leuven, Belgium; 2Department of Electrical Engineering, Katholieke Universiteit, Leuven, Leuven, Belgium.

With the introduction of low-k dielectric into on-chip interconnects, leakage under use condition is becoming a significant reliability concern. Possible leakage paths in copper damascene structure include the one through bulk dielectric plus copper diffusion barriers and other integration interfaces. In this paper, the dominant leakage path is restricted to the former one by modulating the barrier integrity: sealing and sub-critical barriers are compared. The low-k is a micro porous organo silicate glass (OSG, k=5). In TDDB measurements,
As modern copper/low-k interconnects continue to scale, both the dielectrics and metallization faces increasing challenges. To maintain the 90 nm node, dielectrics, a further reduction of the k-value necessitates the introduction of porosity. This puts stringent requirements on both sealing techniques and mechanical integrity. In order to minimize compaction effects on the effective k-value, processing damage and sidewall sealing need to be sufficiently (and increasingly) shallow. As the effective resistivity of interconnect lines continues to increase with decreasing dimensions, optimization and novel solutions are needed to address this challenge. These include ALD, overburden ingrowth, plating chemistry and processing parameter changes, novel filling mechanisms, and a new growth mode known as super-secondary-grain-growth. The most promising integratable and scalable solutions will be highlighted.

Optimization of interconnect microstructure for improved manufacturability and reliability has long been a subject of ongoing research, initially for AI structures and now for Cu metallization. This research remains critical as minimum feature sizes continue to shrink in increasingly complex integrated circuits. Failures in Cu interconnects, either stress induced or from electromigration processes, are likely a function of the Cu microstructure that evolves during processing. Optimization of this structure requires a fundamental understanding of both structure/property relationships as well as microstructural evolution during processing. As typical interconnects go through many processing steps that involve temperatures up to 400 degrees C, it is important to understand the effects of elevated temperature on the evolution of Cu microstructures. This structural evolution is a function of sub-layer materials, bath chemistry for electroplated films, and initial deposition conditions. Electron backscatter diffraction analysis of Cu films processed by various methods reveals differences in microstructural evolution during in-situ annealing.

The Cu grain size distribution and morphological analysis has increasingly become one of important parameters impacting interconnect resistivity, electromigration and stress migration (EM/SM) device reliability in the Cu interconnect era. There is a need for a robust and automated grain boundary (GB) characterization mechanism in the early stages of process development. SEMVision G2 FIB is an automated dual beam SEM and FIB tool which enables enhanced visibility of grain boundaries by focused ion beam (FIB) sputtering right after copper plating. The selected area is imaged with a high resolution secondary electron microscope (SEM). QPM (Quantified Process Monitoring), a novel automated application on the SEMVision G2 FIB, is used to analyze the SEM images and yields a grain boundary (GB) density result. The GB density under a wide variety of process conditions such as anneal temperatures and different plating recipes along with wafer level (center to edge) uniformity can be easily characterized and monitored with this simple and robust technique. Another major advantage of the GB analysis is its capability to perform Cu grain boundary metrology on dense pattern, where it matters most for parametric and reliability performance. This capability opens new directions to accelerate process development and improve EM/SM device reliability. The experiments described in this paper explored the impact of a wide range of pulse ECP frequencies and amplitudes, as well as a wide range of post-ECP in-situ anneal temperatures and durations on copper film grain boundary density and shear resistance. For the pulse plating experiment, the baseline process, together with a 10Hz pulse plating process yielded the lowest GB density. Higher frequency pulse plating caused a rapid increase of GB density as well as significantly higher variance in GB density with 50Hz 7 200Hz. No sensitivity of GB density to the pulse amplitude was observed. In the anneal experiments, for a one-step (30 sec) anneal, the GB density decreased with increasing anneal temperature. Two-step anneal processing decreased the GB density significantly. The lowest GB density was achieved with 1 hour anneal at 250°C. Copper GB density had a very high correlation to electrical sheet resistance, as measured by the four-point-probe method. In addition, we characterized the dependence of grain boundary on Cu.
feature size and showed a systematic increase in GB density with decreasing feature size. Automated CB analysis on the SEM/Zeiss QFEG 225 with electron microprobe analysis jointly developed by process diagnostics and copper plating R&D teams, tailored for the unique advanced process control needs of the ECP process. This automated metrology has the potential to shorten the learning curve, offer a process capability, monitor loss in thickness, and provide in-line ECP process monitoring capability, and should significantly enhance device EM/SM testing outcomes.

4:30 PM B5.4
The Effect of Temperature on Spontaneous Morphology Change in Electrodeposited Copper Metallization
Shafat Ahmed1, D. N. Buckley1, S. Nakahara1 and Y. Kuo2;
1Department of Physics, Materials and Surface Science Institute, University of Limerick, Limerick, Ireland; 2Department of Chemical Engineering, Texas A&M University, College Station, Texas.

The results of a detailed investigation by atomic force microscopy (AFM) of the nanostructure and morphology of electrodeposited copper metallization and its evolution with time is presented. Copper films were galvanostatically electrodeposited on various substrates from acidic CuSO4 baths. A spontaneous morphology change (SMC) was observed in real time by in situ AFM during room temperature aging of these films. The phenomenon involves the formation, usually quite suddenly, of new features, smaller than the existing features on the surface. It has been shown that this occurs in copper films electrodeposited under many different conditions and is quite reproducible. The actual morphological change event was captured in real time when it occurred during the scan of an AFM image and the density of new features was observed to increase with time as indicated by the variation from top to bottom in the micrographs. Measurements of surface roughness obtained from AFM images showed a similar increase during SMC. An incubation period was observed between the end of electrodeposition and the onset of SMC. The length of the incubation time was found to depend on the temperature. It is assumed that a process, which we call recovery, occurs in the film during the incubation period at a temperature-dependent rate. A systematic investigation of annealing time and temperature was carried out. A series of films were deposited and, beginning a short time (~20-35 s) after electrodeposition, each sample was annealed by immersion in a thermostatted bath for a predetermined period of time. The sample was then removed from the bath and, after rinsing and drying, AFM images of the surface were scanned repeatedly until SMC was observed. Samples were annealed for various times at each of a series of temperatures and the total time after electrodeposition at which SMC occurred was noted for each sample. In experiments at a given value of annealing temperature, values of the remaining incubation time at room temperature were observed to decrease linearly as the annealing time was increased. The measured rates of decrease gave a linear Arrhenius plot. After appropriate iteration to correct for variations in room temperature, the Arrhenius analysis gave a value of 0.48 eV for the activation energy of the recovery process. It is further shown that the incubation period of SMC arises from a volume contraction in the copper film due to the out-diffusion of excess vacancies. This leads to a tensile stress in the near-surface region. At some critical thickness, the near-surface region can no longer support this elastic stress. If its elastic compliance and surface undulation occurs to relieve the stored elastic energy, the observed activation energy is consistent with this mechanism.

4:45 PM B5.5
Cu Resistivity in Narrow Lines: Effect of Metallization Scheme
Sylvain Maitrejean1, Anne Roule1, Jean-Frederic Guilloumond1,2, Murielle Fayolle1, Anthony Roman2, Thierry Morel2, David Bouchu1, Paul-Henry Haunesser1, Lucile Arnaud1 and Gerard Passenoud2;
1CENA-LETI, Grenoble, France; 2STMicroelectronics, Crolles, France.

In order to reduce RC delay and to enhance electron–resistance tolerability of interconnects, Cu has been introduced in the late nineties, replacing Al alloy lines. Nowadays, as interconnects critical dimensions reach values under 100 nm, an increase of Cu resistivity has been observed in narrow lines. This can be attributed either to higher electron scattering along grain boundary and Cu/barrier interfaces in small dimension and to an increase of impurity content in narrow lines. This work is conducted to understand metallization scheme impact on resistivity. Narrow trenches are performed by deposition of a conformal PECVD held on standard patterned structures (back fill techniques). Trench widths down to 50 nm are thus obtained. Several metallization schemes have been optimized to properly fill these small features: Cu Barrier / Cu seed layers stack can be either PVD Ta/TaN/PVD Cu, MOCVD/TIN/MOCVD Cu or PVD TaN/TaNTA/Electrochemical Cu Seed. Cu fill is performed by electrochemical deposition (ECD). Chemistries with high or medium acid level are used. Finally, various Cu anneals are achieved. Cu grain size is characterized with respect to line width and metallization scheme. Cu crystallographic orientation is evaluated. Electrical measurements are conducted to determine Cu resistivity versus line width. For each metallization, good Cu filling is obtained. Moreover, electrical data show good within wafer uniformity. As expected, Cu resistivity dramatically increases for line dimensions below 150 nm. Concerning the impact of metallization scheme performance, the ECD Cu fill chemistry and Cu anneal is observed whereas high Cu resistivity variations are obtained with respect to barrier/Cu Seed stacks. Lowest resistivity is measured for structures using MOCVD TIN/MOCVD Cu barrier/seed. It is worth to notice that this behavior is line width independent. These results are correlated with grain size measurements and structural characterization of the patterned structures.

SESSION B6: Barrier Metal Films
Chair: Sywert Bronsgrasma and David Field
Thursday Morning, March 31, 2005
Room 2004 (Moscone West)

8:30 AM B6.1
Atomic Layer Deposition (ALD) of Barrier/Adhesion/Seed Layers for Interconnects
Zhengwen Li1, Huazhi Li1, Youbo Lin2, Roy G. Gordon1 and Josee J. Vlassak2; 1Chemistry and Chemical Biology, Harvard University, Cambridge, Massachusetts; 2Engineering and Applied Sciences, Harvard University, Cambridge, Massachusetts.

ALD was used to deposit highly uniform and conformal diffusion barriers of tungsten nitride (WN), adhesion layers of ruthenium or cobalt, and copper seed layers for copper interconnects and for a low temperature processing of a variety of applications including MEMS/Sensor. CuCo2(CO)8 produced the pure Cu films with negligible contamination, showing low resistivity of about 6 μΩ·cm after annealing at 400°C. However, the degraded conformal deposition of Co films has been obtained at the temperature between 200 and 400°C, possibly due to the gas-phase reaction between the molecules. Lowering the temperature significantly improved the conformity, and thus developing a very low temperature CVD processing for highly conformal deposition of pure Cu films over high aspect ratio (3:1) trenches using cobalt carbonyls (Co2(CO)8) as the precursor. In addition, the temperature regime reveals the activation energy of about 1 eV. Further, the as-deposited Cu film exhibited the low resistivity of 12 μΩ·cm, which dropped to 8 μΩ·cm after annealing at 400°C. Oxygen and carbon contamination were within AES detection limits. These films appear to be suitable as adhesion/seed layers in copper interconnects and for a low temperature processing of a variety applications with complex structures.

8:45 AM B6.2
MOCVD of Highly Conformal Cobalt Metal Films
Jeonggil Lee, Heejung Yang and Jaegab Lee; School of Advanced Materials Engineering, Korea University, Seoul, South Korea.

Co2(CO)8 produced the pure Cu films with negligible contamination, showing low resistivity of about 6 μΩ·cm after annealing at 400°C. However, the degraded conformal deposition of Co films has been obtained at the temperature between 200 and 400°C, possibly due to the gas-phase reaction between the molecules. Lowering the temperature significantly improved the conformity, and thus developing a very low temperature CVD processing for highly conformal deposition of pure Cu films over high aspect ratio (3:1) trenches using cobalt carbonyls (Co2(CO)8) as the precursor. In addition, the temperature regime reveals the activation energy of about 1 eV. Further, the as-deposited Cu film exhibited the low resistivity of 12 μΩ·cm, which dropped to 8 μΩ·cm after annealing at 400°C. Oxygen and carbon contamination were within AES detection limits. These films appear to be suitable as adhesion/seed layers in copper interconnects and for a low temperature processing of a variety applications with complex structures.

9:00 AM B6.3
Atomic Layer Deposition of Ruthenium Thin Films for the 45-nm Era
Jin Yong Kim1, Sang Yeol Kang1, Beom Seok Se02, Jung Hyun Lee2, Kwanghee Lee3, Han Jin Lim1, Cha-Young Yoo1, Sung-Tae Kim1, U-In Chung1 and Joo-Tae Moon1; 1Process Development Team, Samsung Electronics Co., Ltd., Yongin-Si, Yongin, Yongin-Si, Gyeonggi-Do, South Korea.

As the semiconductor industry heads toward the 45 nm technology node, the need for conformal and conductive barrier layer for copper has led the atomic layer deposition (ALD) technique to be a promising alternative to conventional physical vapor deposition (PVD) techniques. ALD-ruthenium has shown great promise to plate copper directly on a diffusion barrier. Not only could ruthenium potentially replace a two-step Ta/TaN process commonly used for diffusion barriers, but it could replace the seed layer as well. One of the most widely researched applications of ruthenium thin film is a capacitor electrode in memory devices such as gigabit DRAMs and FRAMs. Another potential application of ruthenium is as a PMOS gate electrode in conjunction with high-k gate dielectric films. However, it was shown that vapor deposited ruthenium may not be adequate as a copper diffusion barrier. Hence, ruthenium film composition, morphology, adhesion characteristics, and step coverage should be optimized to meet the requirements. In this study,
Thin (10-100 nm) films of boron-carbon nitride (BC$_3$N$_x$) were grown by chemical vapor deposition (CVD) for potential use as copper diffusion barriers between copper interconnect lines and the interlayer dielectric. Films were grown using dimethylamine borane as the CVD precursor and with no co-reactant, ethylene, or ammonia. Adjusting the co-reactant gas choice and flow rate allowed for a tunable film composition and dielectric constant. When ethylene was used as a
360°C given current of 1.12 A/cm² at 0.5 MV/cm (compared to 5.50 x 10⁻³ A/cm² for SiCo.7Ga.08 sputter-deposited Ta layers of similar thickness. The reasons for this behavior are discussed in the paper. The dielectric properties of the molecular nanolayers with that of conventional barriers, particularly in small metal structures in microelectronic applications will be discussed.

Cyclic loading of metals can lead to the formation of damage and to failure even at loads that are well within the elastic range. In fact, the loading conditions present in the thin metal films and small metal structures used in many applications are often severe enough to lead to fatigue failure. In this study, TEM and in-situ SEM observations of thermal fatigue damage in sub-micron thick Cu films have been performed. As the crystal dimensions of the samples are decreased below 1 micron, by decreasing film thickness and grain size, a clear deviation from the characteristic fatigue damage of bulk metals is observed. The changes in dislocation structures, damage morphology, and failure lives are attributed to decreased dislocation movement and increased interface contributions. In particular, in samples with small metal structures in microelectronic applications.
Thin films of sputtered aluminum were deformed by two distinctly different experimental techniques. One experiment comprised of passing high electrical AC current density, 12.2 MA/cm² at 100 Hz, through 800 micron long X 3.3 micron wide and 0.5 micron thick patterned interconnect Al lines deposited on SiO₂/Si substrates. The other consisted of intergranular tensile deformation of a thin film Al line 50 micron long X 5 micron wide and 0.5 micron thick at a strain rate of about 10⁻⁴/sec. In the electrical tests approximately 3X10⁷ W/cm² of energy was deposited at 250 Hz resulting in cyclic Joule heating, which increased a total thermal strain of about 0.3 % per cycle. The mechanical test showed a fracture strain of only 0.5 % but did display ductile chisel point fracture. In both experiments, certain grains exhibited large, greater than 30 degrees, rotation away from an initial ⟨111⟩ orientation towards ⟨001⟩, based on EBSD measurements. TEM analysis of specimens from both experiments showed an unusually high density of prismatic dislocation loops. In the mechanically-tested samples, a high density of loops was seen in the chisel point fracture zone. While in the electrical tests, only prismatic dislocations were observed. These results suggest very high incidence of intersecting dislocations creating jogs and subsequently vacancies before exiting the sample. A discussion of this and other possible sources of the high vacancy concentration will be presented.

2:15 PM B7.3/011.3 Employing Thin Film Failure to Form Templates for Nano-Electronics. Rainer Adelung, Eldbahi Shiva, Kuma Rudra, Abhijit Biswas, Sahid Jibril, Rainer Kunz, Sebastian Wille and Michael Schamburg; Materials Science, CAU Kiel, Kiel, Germany.

Recently, we showed that thin film stress can be used to form well aligned and complex nanowire structures [1]. Within this approach we used stress to introduce cracks in a thin film. Subsequent vacuum deposition of metal leads the formation of a metal layer on the thin film and of metal nanowires in the cracks of the substrate. Removal of the thin film together with the excess metal cover finishes the nanowires [2]. These structures were electrostatically operated at the resonance mode by applying an AC voltage with a frequency, a two-step sacrificial-layer removal process was applied. Then static and dynamic loads much larger than electrostatic forces were applied by piezoelectric-driven microtensile techniques. Both tests were conducted in the same loading mode as the resonance test so as not to change failure mechanism, as is essential in accelerated life or degradation tests. Uniaxial stress-strain measurement results showed that tensile and fracture properties degraded with operation time at the resonance mode. Fatigue properties were measured by applying a pulse wave to a piezoelectric actuator: fatigue tests were conducted and fatigue lifetimes measured various stress amplitudes. S-N curves showed that fatigue lifetime and fatigue limit degraded with operation time at resonance mode and fracture properties. These results suggest that fatigue damage accumulated during cyclic loading and increased with subsequent loading cycles. The dependencies of the measured properties on operation time were quantified, and fatigue damage was confirmed by failure analysis. Finally, the fatigue damage accumulation and materials degradation due to cyclic loading were discussed in terms of stress and materials.

2:45 PM B7.5/011.5 Electrical and Mechanical Reliability of Cu Alloy Thin Film for Future Technology Node. Seol Min Yi1, Jeong-Uk An2, Young-Hok Hah3, Young-Bae Park3 and Young-Chang Joo2; 1School of Materials Science and Engineering, Seoul National University, Seoul, South Korea; 2School of Materials Science & Engineering, Andong National University, Andong-si, Kyungsangbuk-do, South Korea.

With miniaturization of advanced integrated circuits fabricated using the Cu damascene process, the higher current density is applied to and the thinner barrier layers are used in the lines therein. The high current density and the thin barrier layer may give rise to significant reliability problems, electromigration and drift of Cu into dielectric, respectively. Use of Cu alloy, as far as there is no significant increase in the electrical resistivity compared to that of pure Cu, has been used as an effective measure to characterize the surface or interface. Cu alloys such as Mg and self-passivating Mg oxide layer is formed to block Cu drift into dielectric material and to enhance adhesion with a capping layer, Ru, which has the electrical resistivity lower than Ta(N) and negligible solid solubility with Cu, is expected not to increase resistivity of the corresponding Cu alloy. To characterize the effect of alloying elements on resistance to electromigration in the Cu damascene structure is along the surface or interface, i.e. between Cu and a capping material, adhesion may be used as an effective measure to characterize the surface or interface. With the results of the microstructural and compositional analysis, the role of each alloy element in its alloy will be identified and discussed.

3:30 PM B7.6/011.6 Effect of Microstructure and Dielectric Materials on Stress-Induced Damages in Damascene Cu/Low-K Interconnects. Young-Chang Joo; Materials Sci. & Eng., Seoul National University, Seoul, South Korea.

The use of copper and low-k dielectrics led to various reliability concerns which were not issues in the interconnects with aluminum...
and silicon oxide. For Cu/low-k interconnects, stress-voiding of Cu has been addressed to the main failure mechanism. Damascene Cu interconnects show significant differences in both microstructural and stress behavior compared to those of the Al interconnects patterned using the etching process. Large thermal stresses may build up during the successive thermal cycles due to the differences in the coefficients of thermal expansion (CTE) of the materials and substrates. The use of various low-k materials in nanoscale integration is crucial to reduce the thermal stresses, considerable amount of growth stress that is originated from growth may develop in damascene Cu interconnects as well. Furthermore, use of various low-k materials having lower thermal expansion and higher CTE similar to the voided thermal stresses, considerable amount of growth stress that is originated from growth may develop in damascene Cu interconnects as well. Furthermore, use of various low-k materials having lower thermal expansion and higher CTE similar to the voided thermal stresses.

4:00 PM B7.7/O11.7

Comparison of Line Stress Predictions with Measured Electromigration Failure Times, Rao R. Morupoulou1, William D. Nix2, Jannesh R. Patel3,4, and Arif S. Budiman1; 1Materials Science and Engineering, Stanford University, Stanford, California; 2Advanced Light Source (ALS), Lawrence Berkeley National Laboratory (LBNL), Berkeley, California.

Reliability of today’s interconnect lines in microelectronic devices is critical to product lifetime. The metal interconnects are carriers of large current densities and mechanical stresses, which can cause void formation or metal extrusion into the passivation leading to failure. The modeling and simulation of stress evolution caused by electromigration in interconnect lines and via can provide a means for predicting the time to failure of the device. A tool was developed using MatCAD for simulation of electromigration-induced stress in VLSI interconnect structures using a model of electromigration-induced stress evolution. The tool solves the equations governing atomic diffusion and stress evolution in one dimension. A numerical solution scheme has been implemented to calculate the atomic fluxes and the evolution of mechanical stress in interconnects. The effects of line geometries and overhangs, material properties and electromigration stress conditions have been included in the simulation. The tool has been used to simulate electromigration-induced stress in pure Cu interconnects and a comparison of the stress predictions with measured electromigration failure times is studied. Two basic limiting cases were studied to place some bounds on the results. For a lower bound estimate of the stress it was assumed that the interface can be treated like a grain boundary in Cu. For an upper bound estimate it was assumed that the stress can be treated like a free standing film. Existing data from experimental samples with known structure geometries and electromigration failure times were used to compare the electromigration failure times with predicted stress build-up in the interconnect lines.

4:15 PM B7.8/O11.8

Stress-Induced Void Formation in Passivated Cu Film during Thermal Cycling and Isothermal Annealing, Dongwen Gan, Bin Li and Paul S. Ho; Laboratory for Interconnect and Packaging, University of Texas at Austin, Austin, Texas.

Stress voicing in Cu metallization is a critical yield and reliability concern. Stress-induced void formation in a passivated electropolishing (EP) Cu film was studied during thermal cycling and isothermal annealing with the film stress measured using a bending beam technique. An optical microscope was used for in-situ observation of the void formation and to determine the void density while SEM was employed to measure the void size and AFM for the topography analysis. In thermal cycling, voids were found to form under tensile stress and close under compressive stress, similar to the void formation observed by T.N.M.Shaw at al [1] in wide copper lines. The ramping rate, film stress as well as the thermal history were found important factors affecting the void formation in thermal cycling. During isothermal annealing, the void density and size were measured as functions of annealing temperature, and the void size as a function of time when the film was annealed at 250 degrees were measured. A critical temperature and stress were found for the void formation with the void density being proportional to the film stress, and an activation energy of 0.7 eV deduced for the void growth. Finite element analysis (FEA) models were set up to evaluate the local stress gradients in Cu films due to the mechanical anisotropy of Cu crystal, and that in a void vicinity as a function of void size, which was believed to account for the observed initial growth of a void.

Stress generation in silicon is becoming one of the major knobs in boosting performance of the leading edge metal-oxide-semiconductor field effect transistor (MOSFET) technology. Substantial increase in device speed has been achieved by an application of highly stressed silicon nitride liner (SiN) films, which in turn produce an uniaxial stress in Si channel leading to electron and hole mobility enhancement. Thin SiN films (about 50nm) deposited by plasma-enhanced chemical vapor deposition (PECVD) have been analyzed by a variety of analytical techniques including Fourier Transform infrared spectroscopy (FTIR), X-ray reflectivity (XRR), and Rutherford backscattering (RBS) to collect data on bonding, density and chemical composition respectively. Both tensile and compressive SiN films have been deposited and analyzed. Mechanisms of stress formation in SiN thin films are discussed. It has been found that amount of bonded hydrogen as detected by FTIR is higher for compressive films and correlates with higher film density as determined by XRR. Both the density and number of interfaces in a film, characterized by XRR, affect the stress. Effect of deposition temperature and other process parameters on stress have been studied. Exposure of SiN films to elevated temperature after deposition lead to increase in tension and degradation in compressive stress. Process parameters, such as post-deposition treatments that result in modification of film structure and magnitude of tensile and compressive stress have been delineated.
Low dielectric constant (low-k) materials are needed to reduce signal delays, crosstalk noises and energy consumption in the next generation faster and more powerful microprocessors. The sub-90 nm technology is expected to influence only the low-k materials and have been shown to be effective in lowering $k$ values by taking advantage of the low dielectric constant of air ($k=1$). However, the trade-off between $k$ value and mechanical strength raises concerns. Based on our previous reported work on PSZ thin films prepared with spin coating, we exploited this possibility of extending the $k$ value to below 2 by different methods without significantly lowering the mechanical strength. Low-k films prepared by spin coating from Pure-Silsica-Zeolite (PSZ) MFI nanoparticle suspensions with high crystallinity have a k value around 1.6. We also report for the first time low-k films prepared from PSZ MEL nanoparticle suspensions. MEL small nanoparticles (~50 nm) with high yield (>50%) were obtained by using a two-stage synthesis method. The spin-on film with this yield has a $k$ value of 1.8-2.0 and a low surface roughness (Ra=3.41 nm). High crystallinity MEL films have a $k$ value around 1.5 and a good elastic modulus (~10 GPa).

**B8.2**

Pure-Silsica-Zeolite Low-k Films from Nanoparticle Suspension. Zilian Li, Shuang Li, Christopher Lew and Yushan Yan; Chemical and Environmental Engineering, University of California, Riverside, Riverside, California.

Isolating and tailoring the structural properties of metal-dielectric interfaces is a critical challenge for realizing high performance interconnect wiring in nanodevices. We have recently demonstrated the potential of organosilane and polyelectrolyte nanolayers to inhibit Cu diffusion and enhance adhesion at Cu-SiO$_2$ interfaces$^1$. The barrier properties of 0.7 to 3.5-nm-thick molecular layers are superior compared to the sputter-deposited barriers of Ta of similar thickness. However, little is known regarding the thermal stability of structures modified with molecular layers and the effects of annealing on the properties of the cured layers. Here we report that 3-Mercaptopropyltrimethoxysilane (MPTMS) molecular layers in Cu/Atomic Layer Deposited (ALD) SiO$_2$ structures are stable only within the temperature range from 400°C, but also result in a remarkable ~5-fold increase in debond energy (measured by 4-point bending) compared to debond energies measured for untreated interfaces. The effects of pristine and sulfonated MPTMS nanolayers and the nature of the siloxane bond on the adhesion enhancement mechanism are revealed by X-ray photoelectron spectroscopy of fracture surfaces. Thiol-terminated layers result in a factor-of-3 increase in debond energy at room temperature, followed by a 60% decrease upon annealing >400°C. Sulfonated nanolayers show negligible effect on the debond energy in this temperature range. Annealing >400°C, however, results in monotonic debonding increase reaching up to ~15 J/m$^2$, which is a ~2-fold of greater than unsupplemented Cu-SiO$_2$ interfaces. Cu fracture surfaces showing Si 2p, Si 2s and O 1s signatures corresponding to thick and siloxane indicate debonding at the MPTMS-SiO$_2$ interface. Cu 2p and O 1s spectra reveal Cu-SiO$_2$ bond formation, which increase above 400°C. Si 2p and O 1s spectra showed an increased siloxane bond density in samples annealed to >400°C, suggesting siloxane bond stabilization by irreversible dehydration of silanoid groups. This was experimentally verified by kinetic measurements of the dehydration process using thermal gravity spectroscopy. Thus, strengthening of bonding interactions at both Cu-MPTMS and MPTMS-SiO$_2$ interfaces contribute to enhanced interfacial adhesion. Our results showing enhanced adhesion and thermal stability of molecular layers at elevated temperatures is promising for integrating organic nanolayers into future nanodevices.

Peter G. Ganesan, A. P. Singh and G. Ramanath; Department of Materials Science and Engineering, Rensselaer Polytechnic Institute, Troy, New York.

As the IC design rules continue to get smaller, trench dimensions are getting narrower and trench aspect ratios are increased. Traditionally, chemical vapor deposition (CVD) has been the technology of choice for the gap filling applications, including shallow trench isolation (STI) and pre-metal dielectric (PMD) trenches. However, for the technology nodes 70 nm and beyond, the CVD technologies including H2FCD are facing various challenges, including high shrinkage and higher aspect ratio gaps. Although new CVD technology is evolving, the throughput could still be a major issue. Alternatively, spin-on dielectric (SOD) materials provide feasible pathways for the high aspect ratio gap filling with the potentials of easy process and high throughput. We have investigated a number of hydrogen silsesquioxane and methyl silsesquioxane materials for gap filling. The trench gaps range from 20 to 250 nm in width with aspect ratio varying from 1 to 7. Generally, the SOD materials can achieve good gap fills, even in the 20 nm gap with the aspect ratio of 7. While a decent gap fill by a SOD material is relatively easy to accomplish, the greatest challenge remains in material densification in a narrow trench. The narrow opening in such a trench limits the material flow while the SOD material is shrinking during the cure. Typically, the bottom of a gap is not as dense as the top part. Wet etch selectivity serves as a screening method for trench densification. Different processing and cure conditions are used to increase material densification in the trenches. We will discuss the effects of various thermal cure schemes, plasma cure, and alternative cure methods of SOD materials in these nano-scale trenches. While the SOD materials can be cross-linked in the gaps, different schemes significantly impact wet etch selectivity.

**B8.6**

Annealing-Induced Adhesion Enhancement at Cu-SiO$_2$ Interfaces Modified with Organosilane Nanolayers. Darchan D. Gauldii, P. G. Ganesan, A. P. Singh and G. Ramanath; Department of Materials Science and Engineering, Rensselaer Polytechnic Institute, Troy, New York.

New Methodology to Characterize and Model Cure Stress in Packaging Based on a Thermal Expansion - Cure Shrinkage Analogy. Hong Ya’, S. G. Mhaisalkar$^1$ and E. H. Wong$^2$; School of Materials Engineering, Nanyang Technological University, Singapore, Singapore; $^2$School of Chemical and Environmental Engineering, University of California, Riverside, Riverside, California.

Annealing-Induced Adhesion Enhancement at Cu-SiO$_2$ Interfaces Modified with Organosilane Nanolayers. Darchan D. Gauldie, P. G. Ganesan, A. P. Singh and G. Ramanath; Department of Materials Science and Engineering, Rensselaer Polytechnic Institute, Troy, New York.

Mesoporous low dielectric poly(silsesquioxane) thin films have been fabricated by templating various surfactants such as cetyltrimethyl ammonium bromide or 4-octylphenol polyethylene in the silsesquioxane polymer matrix and their properties of the thin films characterized by chemical, mechanical and structural characterization. Depending on the types of the surfactants, mesoporous poly(silsesquioxane) thin films with different mesostructures and morphologies have been formed via self-assembly and calcination induced structural transformation. The dielectric constant ($k$) of the films depended on the content or porosity of the surfactants. The dielectric constants of $k=1.9-2.1$ were obtained for the films with relative porosities of about 30-40 vol. % to the polymer matrix itself. The elastic modulus of the films showed a dependency on the type, content of the surfactants and was ca. 0 GPa with the $k$ value of ca. 2.30.
One of the most challenging aspects of C wafer fabrication is obtaining uniformly clear via holes following etch and clean. Residues and excess CuOx growth are common sources of high resistance and electro migration failure. Today, there is no effective method for identifying these residues before etch and clean. SEM lacks resolution capability, and TEM preparation is costly and lengthy. Electrical test necessitates complete fabrication of structures, requiring long cycle time and convolting results with variations from the wafer processing steps after etch and clean. We describe a method of characterizing via bottoms in dense 0.12 nm via structures that have been etched and cleaned prior to barrier/seed deposition. This technique, based on a two-laser power absorption method, is fast (3-4 min per test structure), non-destructive and has a 2 nm spatial resolution, enabling in-line local and wafer-scale uniformity measurements for process development and process monitoring. The results reported in this paper focus on the detection of thin residuals and oxide films at the bottom of the via. We present studies of via conditioning as a function of time after wet clean processing, showing sensitivity to CuOx growth at the bottom of the via (M1 metal exposed to ambient). This paper also provides experimental results for different post-etch clean process parameters, including both wet and dry processing, showing how metrology shortens the process optimization cycle time to deliver improved uniformity and performance of the post-etch clean process.

The Effect of Film Composition on the Properties of PECVD Low-k a-SiCO:H Films. Byung Kee Hwang, M. Tzou, A. Dixit, Derek Witty and Hichem MSaad; Applied Materials, Santa Clara, California.

Amorphous silicon oxycarbide (a-SiCO:H) films with dielectric constants ranging between 3.0 to 2.5 were grown on a conventional plasma-enhanced CVD (PECVD) reactor using various organosilanes as CVD precursors. By changing CVD precursors and the conditions of PECVD processes, the composition of a-SiCO:H films and, as a result, the thin film properties of resulting films could be tailored. Especially, in this study, as an alternative to adding porogen into films during process, the C/Si ratio in the film was manipulated in a way to change the dielectric constant of films as well as other film properties. The films grown with different CVD precursors and PECVD processes were characterized by Fourier transform infrared (FTIR), Rutherford backscattering (RBS), Hysteron tribometer, stand-up test, modified edge lift test (m-ELT) and electrical measurements of metal-insulator-semiconductor (MIS) structures. With new CVD precursors and control of process conditions, it is possible to get a-SiCO:H films with k of 3.0 to 2.5 and modulus of 15 to 3 GPa without any post treatment. We found that by using different CVD precursors we could get Si:C-H films which had the same k of 2.8, but with modulus values ranging from 4 to 13 GPa. Also the carbon enriched a-SiCO:H films showed improved toughness and adhesion properties. The results imply that the selection of the right CVD precursor for low-k application would be very important to develop a robust PECVD low-k film. In this paper we will discuss the effect of composition and bonding structures of a-SiCO:H films grown with different CVD precursors on the thin film properties.
films confirm that the hermetic oxide layers can be deposited with excellent conformality.

**BS.12** The Effect of Methylating Treatments on the Dielectric Reliability of Low-k/Cu Structures. Swarnal Barthakur, S. Sri Satsan, J. E. Novak, Jr., Knorre, Paul S. Hoy; Sematech, Austin, Texas; 2The University of Texas at Austin, Austin, Texas; 3Infinion Technologies, Munich, Germany.

As scaling approaches nanometer levels, the RC delay of interconnects has become a dominant factor in determining the total delay. Etching, ashing and cleaning processes damage the dielectric [1]. In general, porous low-k materials are more prone to damage compared to dense ILD. This damage leads forward steps and ultimately leads to higher effective dielectric constant [2]. The damage also increases the leakage current through the inter-level dielectric (ILD) and compromises the reliability of the interconnect structures. In this paper, we investigate dielectric breakdown which can be used to repair the damage to the dielectric and recover the k-value. The same chemicals could also act as a pore sealant that will prevent copper penetration into the ILD and improve the reliability. The chemicals used in this study are organic compounds with methyl groups because the ILD is a methyl silsesquioxane (MSQ) material [3]. We will present physical (SEM/EELS, AFM, FTIR) and electrical (k-value, leakage current, ramp-voltage-breakdown and TDD) characteristics of single damascene structures (0.13 μm on 300nm) with different chemical post-ash treatments. The RC delays will be compared among different treatments. The breakdown field is determined from ramp-voltage-breakdown tests performed on copper damaged structures [4]. The breakdown field is determined over a wide range of pitch. In addition, annealing effects are being studied. Dielectric reliability characteristics will be compared. The structures were stressed at RT and high fields (3-6 MV/cm). The effectiveness of the dielectric damage treatment and the breakdown characteristics. The high field and RT test conditions may cause breakdown to occur due to barrier lowering (charge injection) at the interfaces as well as molecular degradation of the ILD. Furthermore, it will be provided in this paper: [1] J. Peters, Semiconductor International, Oct 1st 2002. [2] P.G. Clark et al., Science International 4th World Conference on Microelectronic Reliability, in Jeju Island, Korea, May 3-4, 2002.


The widely known Method of Mercury Porosimetry (MPP) has several substantial disadvantages, for example, the necessity to apply high pressures of mercury, which can lead to destruction of samples and to a distortion of the porosimetric curves (porograms). Other drawbacks MPP are: distortion of the results owing to amalgamation of metal metals, different values of the mercury wetting angle for different samples of mercury, the development of a new method - the Method of Standard Porosimetry (MSP) and Automated Standard Porosimetry (ASP). MSP and ASP have none of these disadvantages and give the possibility of measurements in a widest range of pore sizes from 0.3 to 300660 nm for any materials, including soft or frail materials or amorphous materials. MSP is based on the laws of capillary equilibrium. If two (or more) porous bodies are in contact with one another and partially filled with a wetting liquid (hydrocarbons, water, etc.) then in the state of capillary equilibrium the values of the capillary pressure P of the liquid in these bodies are equal. The capillary pressure can be represented by the Laplace equation if for one of the porous bodies (the standard sample) the pore size distribution is known, then by determining an equilibrium dependence of liquid content for a test sample on liquid content for standard sample, the pore size distribution for the test sample can be calculated. The amount of liquid in the samples is determined by weighing. The standards and test samples are new preliminarily (under vacuum) filled with a liquid. The stack of porous samples is assembled in a special clamping device in which the samples are tightly pressed to each other. From this assembly a small portion of the liquid is separated by interconnection with a chamber or by a flow of dry inert gas. The ASP includes a automatic manipulator for the assembling and disassembling of the stack of samples and for the transfer of the samples to the balance. Any porous and dispersed bodies can be predetermined by MSP, porosimetry, membranes, separators, filters, catalysts, carbon nano-tubes, adsorbents, ceramics, metallic ceramics, textiles, pharmacueticals, construction materials, polymers, geological strata, etc. MSP/ASP allows for determination of a variety of porosimetric properties of porous and dispersed bodies: pore volume and specific surface distribution in terms of pore radii, specific surface area, information about a shape (correlation) of pores, liquid distributions in terms of values of its free binding energy and capillary pressure with the testing mercury, sorption isotherms, differential characteristics of swelling, contact angle and its dependence on pore radii, characteristics of hydrophobic-hydrophilic properties, etc.

**BS.14** Capacitance Measurement Technique for Determining the Out-of-Plane Coefficient of Thermal Expansion for Low-k Dielectrics. Swarnal Barthakur, 4Andreas Knorre, 5Paul S. Hoy; 1Semitex, Austin, Texas; 2The University of Texas at Austin, Austin, Texas; 3Infinion Technologies, Munich, Germany; 4IPST, Gaithersburg, Maryland.

As scaling approaches nanometer levels, the RC delay of interconnects has become a dominant factor in determining the total delay. The low-k dielectrics that are being investigated for reducing the capacitance are based on organic or are based on inorganic materials. A major concern in the integration of low-k materials is the thermal stress generated in the structure due to the thermal expansion mismatch between the low-k material and its adjacent surroundings. The out-of-plane thermal expansion of these dielectric materials can be determined by X-ray reflectivity technique (XRR) [1]. In this paper we present a characterization technique for determining the out-of-plane CTE of low-k materials from capacitance measurements. This technique relies on accurate capacitance measurements over a wide range of temperature (25-300°C) and measurements are made in a N2 environment. By combining the equations for a parallel plate capacitor and coefficient of thermal expansion we get the equation [2] \[ \alpha = -\frac{1}{3}\left(\frac{1}{E_2} \frac{dE_2}{dT} + \frac{1}{E_1} \frac{dE_1}{dT}\right) \] This equation does neglect the temperature dependency for the material's k-value. We will discuss measurement corrections and instrumental limitations. The data obtained for both carbon-doped films and organic films. The CTE values obtained by this technique will be compared with those obtained from XRR technique. The dependence of the dielectric constant on temperature and its effect on the calculated CTE values will be provided in this paper.


Quantitative nanometer-scale estimations of mechanical properties are important in the development of multilevel interconnect technology for ultra-large-scale integrated circuits. Recently, a convenient nanoindentation technique based on the development of a new method has been widely used for evaluating the hardness and elastic modulus of thin films. This technique has some limitations in estimating elastic properties in the elastic deformation range and yield stress due to plastic deformation. Although these properties are indispensable to determine the mechanical strength of multilevel interconnect structures, up to now, for example, macro-meter-scale mechanical properties obtained from bulk materials have still been applied in computer simulations for estimating stress distributions on a nanometer scale. In our recent studies, we have successfully developed a spherical nanodentation method for determining the yield stress of tribofilms on a nanometer scale [1]. In this work, we applied this spherical nanodentation method to evaluate the elastic modulus in the elastic deformation range and the yield stress of ultra-thin Cu and low-k films. A spherical indenter with a radius of 1 μm was chosen because this shape is conducive to mechanical analysis in terms of the Hertz contact theory and the Tresca yield criterion. Measurement effectiveness was examined by using two differently oriented single crystals Cu (111) and Cu (100). The Cu (111) plane exhibited initial plastic deformation in the load-depth curve at 9.5 μN and the Cu (100) plane exhibited initial plastic deformation in the load-depth curve at 17.5 μN. The elastic modulus and yield stress of Cu, both of which were similar to the values of Cu by XRR method; Cu = 130 GPa and shear modulus of Cu = 430 GPa, were estimated for the Cu (100) plane. This anisotropic nature of these mechanical properties, which were never seen on a macro-meter scale, agreed with metallurgical considerations of an active f.c.c. slip system. This method was also applied to Cu and low-k films of Cu films and low-k dielectrics. The Cu films possessed anisotropic elastic modulus and shear yield stress due to the different crystallographic orientations present in the film plane. By using an indenter with a small radius of less than 150 μm, this method makes it possible to evaluate the elastic modulus and yield stress of 20-nm-thick ultra-thin films. [1] Jiping Ye, Makoto Kau and


Chemical vapor deposition (CVD) low-k films using tri-methyl-silane (3MS) and tetra-methyl-cyclo-tetra-siloxane (TMCTS) precursors were studied. A four-point bend test (4PBT) was performed to assess the adhesion property of the low-k films to Si substrates and the results were compared with that of simpler method, nanoscratch test (NST), as a quality control tool despite its drawbacks. Adhesion strength, G_c, of films measured by 4PBT test was a critical scratch load, Pc, as obtained by NST display a linear relationship with hardness and modulus of the low-k film. The lowering of Gc as the hardness of the film decreases can be explained by the effects of the C introduction into the Si-O networks found in these films. Lower Carbon content for higher hardness films is thought to cause them to be more silica-like and thus exhibit better adhesion with the Si substrate. Two failure modes were observed for specimens under 4PBT. On one hand, films with low hardness (<5 GPa) exhibit low Gc (<10 J/m2) with an adhesive separation of low-k from the Si substrate. On the other hand, films of high hardness (>5 GPa) display interfacial energies in excess of 10 J/m2 with delamination of epoxy from the substrate, thus indicating excellent adhesion between the low-k films and Si substrate. Under 4PBT, initially the load increases linearly as the specimen deforms elastically. At some point, the load decreases abruptly which signifies the point at which the vertical crack initiated by the notch begins to propagate through the Si. When it reaches an interface, it might be either deflected to propagate along the interface or continue through the next material in its vertical path. The crack takes the path that has the least energy dissipation. Thus, the crack path would be determined by the adhesion at the interface and the toughness of the material ahead. For the low hardness films good correlation exists between Pc and Gc. However the two data points of the high hardness films that gave the highest Pc and Gc values do not lie on the correlation line drawn for the low hardness film data points due to different factors governing the failure in both tests and a change in the 4PBT failure mechanism. Therefore correlating results obtained by the 4PBT to other empirical tests must be done with caution.

Application of Nanoindentation to Characterize Fracture in ILD Films used in the BEOL. Eva Erika Simonyi1, Eric Liniger1, Michael Lane1, Christos D. Dimitrakopoulos1 and Christy S. Tyberg2; 1IBM TJ Watson RC, Yorktown Heights, New York.

It is of importance to measure the so called critical film thickness, above which spontaneous cracking could occur. Nanoindentation method is presented as a reliable technique to estimate the critical film thickness for ILD films used in the BEOL. This allows to calculate cohesive energies and fracture toughness of the films. Several materials were investigated using nanoindentation combined with AFM imaging. The results were compared to data acquired by four point bend methods.

B8.19 Role of Friction and Loading Parameters in Four-Point Bend Adhesion Measurements. David M. Gage1, Kyungboon Kim2, Christopher S. Littke1 and Reinhold H. Dusskard1; 1Materials Science and Engineering, Stanford University, Stanford, California; 2Mechanical Engineering, Stanford University, Stanford, California.

The 4-point bend method has become a widely established technique to quantitatively examine the cohesive and adhesive fracture energies of thin film structures. In the present work we report on the effects of loading point position, applied loading geometry and loading rate on four-point bend fracture measurements. To date, these effects together with other salient loading parameters have received little attention and have not been systematically studied. Technologically relevant interconnect thin film structures containing either carbon doped oxide or thermal oxide low-k dielectrics and selected barrier layers were prepared and tested in four-point bending to determine the dependence of the measured fracture energy, G_c, on loading parameters and specimen geometry including the loading rate, load point separation, and specimen surface condition. Fracture energy measurements were found to be sensitive to applied loading geometry and displacement rate, particularly for specimens with G_c values of 5 J/m2. We show that this behavior is due to a combination of Coulomb friction and stress corrosion effects. Good practice testing guidelines are suggested to improve the accuracy and precision of four-point bend measurements.

B8.20 Abstract Withdrawn

B8.21 Rapid Characterization of the Electrical and Micro-Structural Properties of Molybdenum-Tungsten Electrodes using a Combinatorial Thin Film Spattering Technique. Seong-Ik Jun1, Timothy E. McKnight2, Anatoli V. Melechk02,1, Michael L. Simpson1,2 and Philip D. Rack1; 1Materials Science and Engineering, The University of Tennessee, Knoxville, Tennessee; 2Molecular Scale Engineering and Nanoscale Technologies Research Group, Oak Ridge National Laboratory, Oak Ridge, Tennessee.

Molybdenum-tungsten (MoW) alloys have great potential uses for high temperature and low resistivity electrodes. These alloys are particularly useful in inverted metal-oxide-semiconductor field-effect transistors (MOSFET) devices where a small etch taper angle is desirable for device reliability. In order to investigate the electrical characteristics and micro-structural properties of MoW as a function of the binary composition, a combinatorial RF magnetron sputter deposition technique was employed. Additionally, we investigated the effects of substrate bias and temperature. The electrical resistivity of MoW thin films deposited at room temperature and without bias followed the typical Nordheim’s rule as a function of composition. The resistivity increases with deposition temperature and decreases with increasing bias power. The electrical resistivity of MoW thin films deposited at room temperature and with bias showed a significant increase due to the lattice mismatch between stable Mo and metastable W. MoW films deposited at higher temperature (250°C) also followed Nordheim’s rule as a function of composition, however it didn’t contain the metastable β-W phase and consequently had a lower resistivity than the room temperature deposition. MoW thin films deposited with substrate bias had a considerably lower resistivity over the overall composition range and its resistivity as a function of composition obeyed the rule of mixtures. The β-W phase is not present in films sputtered samples even room temperature as the tungsten phase was entirely stable α-W. Additionally, unlike bulk molybdenum and tungsten, biased tungsten-rich films had higher resistivity than biased molybdenum-rich films. This phenomenon was attributed to the fact that the dissociation resistivity of tungsten is two orders of magnitude higher than that of molybdenum. The results from high resolution scanning electron microscopy revealed that a denser micro-structure was realized in the biased films, which correlated to the significantly lower electrical resistivity of the biased films.
Additionally, the copper plating rates for invented Stress on 6” wafers are effective for copper interconnects. This is due to their good thermal stability, low resistivity, suitable work function and diffusion barrier properties. Physico-chemical and electrical properties of Ru oxides are intimately dependent on the oxidation state of Ru, and are determined by the resulting microstructure, oxidation state and impurities/contaminants. 5 to 7 nm Ru films were deposited on Si and SiO2 substrates by DC magnetron sputtering in Ar atmosphere. The films were then exposed to UV/Ozone radiation and oxygen at room temperature for a duration ranging from 15 min to 60 min. In situ X-ray photoelectron spectroscopy (XPS) is used to investigate Ru oxidation state and the bonding environment. A comparison with Ru oxide prepared via reactive DC sputtering in an Ar/O2 mixture will be presented.

Advanced Al Damascene Process for Fine Trench under 70nm Design Rule. Sung Hoo Han, Kyung-in Choi, Seerah Yun, Jeong Heon Park, Sang Wook Lee, GilHyun Choi, Sang Tae Kim, U-In Chung and Joo-Tae Moon; Samsung Electronic Co. Ltd., Yongin-City, Kyungki-Do, South Korea.

As interconnect geometry shrinks beyond 100nm technology, tungsten bit-line could be thin due to high line resistance. In order to reduce the line resistance, the stack height needs to be increased, while it causes an increase in parasitic capacitance. The parasitic capacitance reduction becomes more important in high-speed device such as NAND flash memory. Thus, Al interconnect may effectively reduce line resistance, but Al RIE has a difficulty in the filling characteristic of the new CVD-Al metallization scheme. We observed a superior Al filling capability in trench with a width of 40nm by the “bottom up growth of CVD-Al”. This shows Al damascene process by ‘bottom up growth of CVD-Al’ could be a promising technology for advanced Al Damascene process by ‘bottom up growth of CVD-Al’.

A Study of Copper Electroplating in the Submicron Scale Patterns. Ui-hyoung Lee, Hyo-Jong Lee and Tak Kang; Material Science and Engineering, Seoul National University, Seoul, South Korea.

Copper electroplating process has many advantages of gap-fill performance, low cost and easy process. Therefore most manufacturers have accepted the electroplating process as one of their copper metallization processes. The most important thing of these benefits is the superfilling behavior of the electroplating which is controlled by three organic additives, accelerator, suppressor and leveling. In spite of these wide applications, its superfilling mechanism has not been studied enough for the submicron scale patterns. In this paper, additive diffusions and the concentration overpotential effect in the submicron scale pattern are discussed and the limitation of copper ion supply is explained. Favorable sacrificial etching, copper sulfate bath will be presented for the understanding of superfilling mechanisms. For these experiments we design 1-D pattern for one directional growth from the bottom of trench during electroplating. It has similar pattern with the copper damascene process which makes the three directional growths during the electroplating. This pattern can be seen in LIGA [lithography, galvanik, abformung; lithography, electroforming and molding] method MEMS [micro-electro-mechanical system] structures, TEOS 300nm/TaN 25nm/Cu 120nm/SiN 100nm/PR 470nm are sequentially deposited on Si substrate, and then the photo-lithography and SiN etch is preprocessed. The SiN interlayer is essential for the adhesion between copper and PR. From the experimental results for the invented pattern which has seed layer only in the pattern bottom, no superfilling is found at 200nm pattern during electroplating in case of insufficient of the surface. For that reason, it seems that superfilling in the damascene pattern results from the accelerometer accumulation. Additionally the copper plating rates for invented patterns and various width and space patterns are almost same, and it means that concentration overpotential of organic additives’ sticking, the concentration overpotential in submicron scale may be negligible. Hence, it seems that copper damascene electroplating for ULSI can be regarded as the simple electroplating system controlled by the activation overpotential of organic additives’ sticking, the concentration overpotential in submicron scale.
and tribological properties are investigated using nanoscratch testing and polishing on the CETF CMP bench top tribometer. The temperature affects the chemical and tribological properties of the material. The performance of the BCB dielectric material with different curing conditions has been compared with fully cured polyimide which is also a candidate dielectric material. The results of these investigations need to be taken into account before development of a CMP process for dielectric planarization.

Porosity Content Dependence of TDDB Lifetime and Flat-Band Voltage Shift by Cu Diffusion in Porous Spin-on Low-k Materials

Yeong Yoon1, Young-Bae Park1 and Young-Chang Joo2

1School of Materials Science & Engineering, Seoul National University, Seoul, South Korea; 2School of Chemistry, Seoul National University, Seoul, South Korea. School of Material Science & Engineering, Andong National University, Andong, South Korea.

Low-k dielectric materials have been widely used in advanced metallization to reduce RC delay. In order to further decrease the dielectric constant (k), porosity is introduced into low-k materials. In general, the poor the mechanical properties as well as the electrical reliability are expected with the higher porosity. Ogawa et al. [1] studied the effect of porosity in low-k materials on Cu diffusion through the dielectric. Low-k materials with higher porosity had lower breakdown voltage, β (Weibull slope), and τ0.2 (the characteristic parameter of Weibull plot); however, they used different low-k materials and different values of porosity, which lacks understanding on the porosity dependence of the same low-k material. In this paper, time-dependent dielectric breakdown (TDDB) and capacitance-voltage (C-V) tests were performed to evaluate porosity dependence of Cu diffusion in porous low-k materials. The low-k materials used in this study were consisted of the same matrix with different porogen contents. τ0.2 and β were acquired from TDDB tests, while flat-band voltage (VFB) shift was obtained from C-V measurements before and after the bias-temperature stressing (BTS). The activation energy of Cu diffusion in the spin-on low-k dielectric without pore was calculated as well. The time to dielectric breakdown (τ0.2) of the spin-on low-k dielectric decreased as the porosity was increased. We observed not only an increase in time to dielectric breakdown but also a significant increase in VFB shift when the porosity was increased from 20% to 30%. Our observation was consistent with others’ [2], in which they used the position annihilation lifetime spectroscopy (PALS) to find that the intensity of positronium escaping into vacuum increased abruptly with the porosity higher than 20%. All of these results provide a strong piece of evidence that the cross-linking of the pores begins to occur when the porosity is higher than 20%. The cross-linking of pores may result in either of change in the dominant path of Cu diffusion, i.e. from bulk to surface, or instability of the electronic and mechanical properties of the dielectric with incorporation of ambient gas. [1] E. T. Ogawa et. al., Proceedings of EPS, 169 (2003) 1-5; Do Y. Yoon et. al. Mat. Res. Soc. Symp. Proc. 766, pp. 241-251 (2003).

Structure and Interfacial Reliability of Low Dielectric Constant Organosilicate Glass (OSG) Thin Films

Yutaka Lin and Joost Vlassak, DEAS, Harvard University, Cambridge, Massachusetts.

As one of the leading candidates for inter-layer dielectric (ILD) materials in the next generation of integrated circuits, OSG films fabricated by plasma enhanced chemical vapor deposition (PECVD) are by far superior to spin-on low-k materials due to better mechanical properties and compatibility with current fabrication process. OSG is obtained through incorporation of organic groups, such as methyl and methylene groups, into silicon dioxide matrices. The organic groups reduce the dielectric constant, but also degrade the mechanical properties of the material compared to that of silicon dioxide. The low fracture toughness and poor adhesion to barrier layer, in particular, make the material difficult to integrate and sensitive to crack initiation and propagation during processing. It is important to understand the effect of the organic groups on the bonding structure, hence the mechanical behavior of the material. Structure of OSG films of different carbon content is analyzed using Fourier Transform Infrared Spectroscopy (FTIR). Compositional information is derived from Rutherford Backscattering Spectroscopy (RBS) and Forward Roccio Elastic Spectroscopy (FRES). The interfacial reliability of OSG films is evaluated using a four-point bend testing system in ambience of different relative humidity and in aqueous conditions of various pH values. The results are rationalized in light of a structure-correlated kinetic model.

Analysis of the Interfacial Reaction between Sn-3.5Ag and Electroplating Interlayers

Steve H. Kilgore1, Craig A. Gav2, Haldane Henry2, Darrell Hill2 and Dieter K. Schroder3

1Quality Organization, Freescale Semiconductor, Tempe, Arizona; 2Technology Solutions Organization, Freescale Semiconductor, Tempe, Arizona; 3School of Electrical Engineering, Arizona State University, Tempe, Arizona.

Electromigration of Electroplated Gold Interconnects.

Wei Shao, Zhenghao Gan, Chandrasekar Materials on Stress Induced Voiding in Cu Dual-Damascene Interconnects

Wei Shao, Zhenghao Gan, Chandrasekar

Analysis of the Interfacial Reaction between Sn-3.5Ag and Electroplating Interlayers

Sheng-Min You1, Yinyin Chang2, Young Bae Park3 and Young Chang Joo4

1School of Materials Science & Engineering, Seoul National University, Seoul, South Korea; 2School of Chemistry, Seoul National University, Seoul, South Korea; 3School of Material Science & Engineering, Andong National University, Andong, South Korea.

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Yeong Yoon1, Young-Bae Park3 and Young-Chang Joo2

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CDO samples showed open circuit failures after a 1,000 hour test, whereas the maximum resistance change in the USG samples was only 1%. Failure analysis on failing paths showed the same stress-induced failure in both CDO & USG were very similar in nature with voids forming symmetrically at the bottom of the via. The effect of M1 & M2 extensions on stress induced voiding was also studied. The M2 extension in particular did not show any effect on stress induced voiding. However, M1 extensions of 0.0067 μm and 0.12 μm showed a significant change in both CDO and USG wafers. This observation may be explained based on the changes in the stress distributions in the via region in interaction with the barrier layer. Finite Element Analysis (FEA) indicated that the location, gradient, and concentration of hydrostatic as well as normal stresses could explain the stress induced voiding at the via bottom. Failure analysis also indicated that the integrity of the Ta barrier in the via bottom area was of significance to stress induced voiding reliability.

SESSION B8: Interconnect Reliability Issues
Chairs: Paul Besser and Young-Chang Joo
Friday Morning, April 1, 2005
Room 2004 (Moscone West)
9:30 AM B9.1
Passivation Effect on Stress Relaxation and Mass Transport in Electropotted Cu Films, Paul S. He, Dongwen Gao, Rui Huang, Jinghong Liang, Joseph Mark, Suresh Seshia, 1Mechanical Engineering, The University of Texas at Austin, Austin, Texas; 2Intel Corporation, Hillsboro, Oregon.

Electromigration in Cu damascene lines is dominated by mass transport at the Cu/cap layer interface. Stress relaxation measurements were performed using a bending beam technique to investigate the effect of passivation layer on mass transport in electropotted Cu films. Passivation layers investigated included SiN, TaN, and a metal cap layer and the effect on stress relaxation rates were compared with no passivation in order to study the effect of interfacial chemistry on mass transport. A significant effect due to different interfacial layers was observed and can be correlated to electromigration lifetime and interfacial adhesion.

9:00 AM B9.2
Fundamentals of Cu/Barrier Layer Adhesion in Microelectronic Processing, Harsono Samsudin1, Sadasivan Shankar1, Carolyn Duran2, and Michael Haverty1, 1Technology CAD - Logic Technology Development, Intel Corp., Santa Clara, California; 2Polymer Memory Group, Intel Corp., Hillsboro, Oregon.

Copper is most widely used interconnect material in current silicon microelectronic technologies. As such, multiple interfaces formed by a thin Cu layer between Cu and various materials have to be engineered to achieve the desired chemical, mechanical, and electrical properties. Adhesion between Cu and the barrier layer, as well as within Cu and the dielectric, is of particular interest, due to its role in controlling interfacial stability and Cu electromigration behavior. This talk will focus on understanding how the chemistry of interfaces affects adhesion. First-principles density functional theory (DFT) calculations were used to determine chemical adhesion energies of interfaces formed by Cu and various metals considered as a diffusion barrier, including Ta, TiN, and W. Calculations predicted increasing adhesion strength in the order of TiN < Si-doped TiN < TaN < Ta, consistent with wetting experiments done using 100Å thick Cu layer samples. Effects of doping of the interface using light elements (C, N, O) were determined. Calculations were also done for interfaces of Cu with two different classes of amorphous dielectric materials, i.e. silicon nitride and silicon carbide, for which detailed material characterizations are often difficult and time consuming. Quantum calculations predicted Cu/Si-nitride and Cu/Si-carbide adhesion strengths consistent with 4-pb tunneling experiments, including the improvement in adhesion energies when Al or Si was used to dope the interface. These dopant effects could be explained in terms of local lattice mismatch between Cu and the dielectric layer in the interface. In addition, weaker interfaces provide low resistance diffusion paths for Cu atoms during electromigration. The first-principles based modeling, validated by select adhesion experiments, provides a predictive and predictive approach to determine adhesion strengths and predict electromigration reliability in interconnects. Reference: 1. M.W. Lane, E.G. Linger, and J.R. Lloyd, J. Appl. Phys., 93, 2003, p. 1417-1421

9:15 AM B9.3
Effect of Current Direction on the Reliability of Different Capped Cu Interconnects, Chee Lip Gan1, Chin Yong Low1, Cheng Kuo Cheng2 and Jeffrey Gambino2, 1School of Materials Engineering, Nanyang Technological University, Singapore, Singapore; 2Institute of Microelectronics, Singapore, Singapore; 3IBM Microelectronics, Essex Junction, Vermont.

It is widely acknowledged that the reliability of Cu-based interconnects can be improved significantly by replacing the present SiN cap layer with a different material which will slow down Cu electromigration across Cu cap layers. As such, the reliability of Cu/Wo and Cu/TiN interconnects with different lifetime of interconnect remains. In this report, the reliability of Cu M1-V1-M2-V2-M3 interconnects with SiN and Cu WP cap layers was investigated. As expected, the reliability of Cu WP capped structures is much better than that of Cu/SiN capped structure. However, it was also found that the reliability of Cu WP capped interconnects was independent of the direction of electrical current flow. This phenomenon was not observed for SiN capped structures, where electron current flow from “via-below“ structures lived about 3 times longer in terms of time-to-failure than lines with current flow from “via-above”. This is because the Cu/SiN interface is void nucleation site and the fastest diffusion pathway in such architecture. Failure analysis has shown that fatal voids consistently formed directly below the via for “via-above” configuration, and in the lines above the via for “via-below” configuration. On the other hand, failure analysis for Cu WP coated structures show that voids do not necessary form below the via for “via-above” testing direction. This is because the adhesion of the Cu/Cu WP interface may be just as good, if not better, than the Cu/TiN interface. As a result, voids do not nucleate at the Cu WP interface and thus show partial spatial voiding in lines may form directly below the via in “via-above” configuration. In both testing directions, a full span defect is required to cause a failure, and thus an interconnect lifetime is independent of whether the current is flowing from “via-above” or “via-below”. This phenomenon is important and its effects must be incorporated into circuit-level reliability analyses for advanced Cu-based interconnects with improved cap layers.

9:30 AM B9.4
Multi-Via Electromigration Test Structures for Identification and Characterization of Different Failure Mechanisms, Zhe-Jun Sun Chou1, Chao Wai Chang2, Joon Hoon Loo1, 1Materials Science and Engineering, Nanyang Technological University, Singapore, Singapore; 2Electrical Engineering and Computer Science, MIT, Cambridge, Massachusetts.

Experiments on doped-1 structures (copper metal lines with vias at both ends and an additional via at the center) showed that the shorting of a single segment not only depends on the values of its current density and length but also on the stress state on the via link segment. The current density in one 25 μm (um) long segment was fixed at 0.5MA/cm2, with electron flow toward the central via. In the other segment, the current magnitude and sign were varied for different test patterns, with the current density fixed at 2.5MA/cm2 to -2.5MA/cm2 with intermediate values including zero. For all cases, some test structures survived for the full 780 hours of testing and some did not. The percent of the lines that failed increased monotonically with an effective J L product defined as the maximum of the sum of the J L products from all paths through the structure. However, some lines with very small effective J L products still failed, and some lines with relatively large effective J L products did not. Simulations of electromigration and electromigration-induced failures for all test conditions are currently underway. We find that test conditions leading to extreme values of the effective J L product probe different failure mechanisms than those associated with intermediate effective J L products. Multi-via test structures in the doped-1 test structures specifically, are shown to be versatile tools for identification and characterization of different failure mechanisms and length effects through the use of different test conditions with a single fixed structure.

9:45 AM B9.5
Microstructure Evolution during Electric Current Induced Thermomechanical Fatigue of Interconnects, Robert Wilsker1, Roy Geiss1, Yi-wen Cheng2 and David Reed1, 1Materials Reliability Division, NIST, Boulder, Colorado; 2Protiro, Inc., Denver, Colorado.

We demonstrate the evolution of microstructure and material deformation associated with the use of electrical methods for evaluating the thermomechanical reliability of patterned interconnects on rigid substrates. Thermomechanical fatigue in aluminum and copper interconnects was induced by means of low-frequency (100 Hz),
The accelerated electromigration of metals can be observed in both aluminum and copper exposed to stress current densities ranging from 5 to 9 MA/cm². A grounded external resistor of either 47 ohm or 19,980 ohm was connected to the electromigration test results support the conclusion that the diffusion of atomic transport pathways can cause a self-healing process to accelerate the electrolysis of Sn or Sn on Sn. The self-healing process accelerates as the electrical stress condition eventually takes place by melting at a region of severely reduced interfacial free energy, which in turn nucleates and propagates through the grain boundary. The numerical simulations show that capillary forces alone can cause a self-healing process to occur, while the addition of the electromigration-induced void formation accelerates the dissolving process in agreement with our experimental observations. Our findings suggest continuous monitoring of the leakage current between the test line and neighboring circuits and the use of a high data-sampling frequency are necessary to detect this soft failure mode. We are grateful for funding support from the BC Advanced Systems Institute.

11:15 AM A9.8
Analysis of Electromigration-Induced Void Motion and Surface Oscillation in Metallic Thin-Film Interconnects.
Jaejoon Chung, M. Rauf Gungor and Dimitrios Marcoudas; Department of Chemical Engineering, University of Massachusetts, Amherst, Massachusetts.

Electromigration-induced void dynamics in metallic thin films is a problem of major interest for fundamental understanding of driven mass transport and for addressing important interconnect reliability concerns. Recent theoretical work in this area has described nonlinear dynamical phenomena induced by electromigration and emphasized the role of the anisotropic surface diffusivity and current crowding effects in void morphological evolution. In this presentation, we focus on electromigration-induced motion of morphologically stable voids and wave propagation on morphologically stable void surfaces. Our analysis emphasizes systematic parametric study of current-induced void morphological response based on the self-consistent numerical simulations of morphological evolution of voids in metallic thin films; our simulations account rigorously for current crowding effects, surface curvature effects, and the strong anisotropy of adatom diffusion on void surfaces. The mass transport problem on the void surface is coupled self-consistently with the electric field distribution in the conducting film, which is computed using a novel boundary-element method. Our analysis demonstrates that as the morphological stability limit is approached, the migration speed of a stable void deviates substantially from being inversely proportional to the void size, a well-known result that is rigorously valid in an infinite conductor with isotropic materials properties. A non-linear shape function that includes both current crowding and diffusion anisotropy effects is derived and is used to rescale properly the void migration speed resulting in a universally valid relationship for the migration speed as a function of void size. Furthermore, in grain characterized by high symmetry of surface diffusional anisotropy, our analysis predicts the onset of stable time-periodic states for the void surface morphology as either the applied electric field strength, or the void size, or the strength of the diffusional anisotropy increases over a critical value. These critical values correspond to waves propagating on surfaces of voids that migrate along the metallic film at constant speeds; for parameter values below the critical ones, void morphological evolution leads to stable steady states. The examined nonlinear void dynamics were rich, leading to different sequences of morphological transitions and instabilities as different operating conditions are varied.

11:30 AM A9.9
The Effect of Immersion and Evaporated Sn Coating on the Electromigration Failure Mechanism and Lifetimes of Cu Dual Damascene Interconnects.
Miyu Yan¹, King Ning Hu¹, Anand Vishwanath Vairagur², Subodh Gautam Mhasalkar² and Abha Krishnanmooty¹; ¹Department of Materials Science and Engineering, UCLA, Los Angeles, California; ²School of Materials Engineering, Nanyang Technological University, Singapore, Singapore; ³Institute of Microelectronics, Singapore, Singapore.

In sub-micron dual damascene Cu interconnects, electromigration occurs mainly along the interfaces between Cu and dielectric-capped metal lines. Many reports have shown that the interface of Cu/dielectric cap is the dominant diffusion pathway for electromigration. Here we report on electromigration tests carried out recently by A. V. Vairagur et al [APPL. PHYS. LETT., 85, 2902 (2004)] to investigate the electromigration failure mechanisms in the upper and lower layers in dual-damascene Cu test structures. It was found that electromigration-induced void first nucleates at locations which are far from the cathode, then moves along the Cu/dielectric cap interface in opposite direction of electron flow and eventually causes void coalescence. We have conducted immersion tests at 300 °C and 350 °C and at a stress current density ranging from 5 to 9 MA/cm². A grounded external resistor of either 47 ohm or 19,980 ohm was connected to the electromigration test results support the conclusion that the diffusion of atomic transport pathways can cause a self-healing process to accelerate the electrolysis of Sn or Sn on Sn. The self-healing process accelerates as the electrical stress condition eventually takes place by melting at a region of severely reduced interfacial free energy, which in turn nucleates and propagates through the grain boundary. The numerical simulations show that capillary forces alone can cause a self-healing process to occur, while the addition of the electromigration-induced void formation accelerates the dissolving process in agreement with our experimental observations. Our findings suggest continuous monitoring of the leakage current between the test line and neighboring circuits and the use of a high data-sampling frequency are necessary to detect this soft failure mode. We are grateful for funding support from the BC Advanced Systems Institute.

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White Sn (β-Sn) thin film stripes shows a voltage drop about 10% when subjected to electromigration testing. Since β-Sn has an anisotropic crystal structure, it possesses different resistivity along a-, b- and c-axis. The direction of the axes determines the resistance in each grain. Under electromigration, low resistance grains tend to grow in the direction of high current density and high resistance grains shrink, leading to the changes of grain orientation in the Sn stripe before and after electromigration was studied by synchrotron X-ray microdiffraction (~1μm in beam diameter) to achieve grain-by-grain analysis. Grain growth involves grain boundary migration and rotation of neighboring misoriented grains. A model different from normal grain growth is proposed to describe the condition and mechanism of microstructural evolution under electromigration.

SESSION B10: Advanced Packaging Challenges

Chair: Paul Ho and Ray Pearson
Friday, April 1, 2005
Room 2004 (Moscone West)

1:30 PM *B10.1
Flip Chip Reliability of GaAs on Si Thin Film Substrates Using Au/Sn Solder Bumps. Hermann Oppermann, Matthias Hutter, Gunter Engelmann and Herbert Reichl; Fraunhofer IZM, Berlin, Germany.

An Au/Sn solder bump is commonly used for flip chip assembly of compound semiconductors in optoelectronic and RF applications. They allow a fluxless assembly which is required to avoid contamination of optical interfaces and the metallurgy is well suited to the final gold metallization on GaAs or InP semiconductors. The discussed Au/Sn solder bumps are manufactured by electroplating gold and tin in subsequent process steps on GaAs wafers. After the deposition process the bumps consist of a thin gold layer and a thinner Sn layer on top. When the bumps are heated up above 280°C a liquid solder cap forms and after solidification it consists of a gold-rich Au80Sn20 with an eutectic microstructure and a Au layer which is separated from eutectic by a layer of the intermetallic Au3Sn-phase. During flip chip assembly only the eutectic cap melts while the socket stays solid. The remaining gold acts as a compliance layer thus enhancing reliability. We will compare bumps as plated or aged with those which have been reflowed prior to assembly. The yield analysis suggest that bumps in the as plated condition or aged at elevated temperature shall be used rather than reflowed ones. The flip chip assembly using Au/Sn solder bumps of 30 to 125 micron in diameter will be presented in various optoelectronic and RF applications. An RF and reliability test vehicles comprise a GaAs chip which was flip chip soldered to a silicon substrate having impedance controlled microstrip transmission lines produced by Cu/BCB/Au thinfilms. A multichannel and four-point Kelvin tests structures were designed for monitoring of the electrical contact resistance of the flip chip solder joints. Temperature cycling tests with and without underfiller were performed and the integrity of solder interconnect was electrically measured after cycled cycles. Mechanical shear tests and cross-sectioning revealed the different failure modes found in underfilled and non-underfilled test samples.

2:00 PM B10.2
Effect of Electromigration on Mechanical Behavior of Solder Joints. Po Ren1, Jae-Woong Nah1, Jong-ok Sub1, Hoon Gun1, Young-Ki1, Bingshou Xiong1, Lubin Xu2 and John H. Pang2.

1Materials and Science and Engineering, University of California, Los Angeles, Los Angeles, California; 2Mechanical and Production Engineering, Nanyang Technological University, Singapore, Singapore.

Polarity effect of electromigration on mechanical behavior in lead-free and composite solder joints was studied. Electromigration causes a thickness change and metallographic change in intermetallic compounds (IMC) at cathode and anode. To combine electromigration and mechanical test, one dimensional metal(wire)-solder(ball)-metal(wire) structure was developed with the size of 300 μm diameter. The advantage of this structure is that mechanical stress and electromigration current could be applied serially or simultaneously. The current density of electromigration was 1×10^-6 A/cm². The working temperature was 100°C. Tensile stress and shear stress were applied either before or after electromigration. The tensile strain rate was 3 μm/min. We observed that, without electromigration, tensile stress caused a break at the middle of solder because the solder was softer. On the other hand, if combined with electromigration, the failure mode occurred at the interface during tensile test. The tensile strength decreased with longer electromigration time or higher current density. In shear test, the shear chain of solder failed alternatively at the cathodes after electromigration. The combination effects of electrical force and mechanical force on solder joint failure will be discussed.

2:15 PM B10.3
Morphology and Flux-Driven Ripening of Cu6Sn5 Intermetallic Compound during Solder Reaction. Jong-ok Sub1, Andriy Gusak2 and King-Ning Tu1; 1Materials Science and Eng., University of California, Los Angeles, Los Angeles, California; 2Theoretical Physics, Cherkasy State University, Cherkasy, Ukraine.

In flip chip technology, spalling of intermetallic compound due to consumption of thin film under bump metallization (UBM) is an important reliability issue. It is known that ripening of intermetallic compound is the major mechanism of UBM consumption. However, conventional ripening theory was not able to interpret the ripening of intermetallic compound. To provide a better understanding, a new kinetic theory of non-conservative ripening was proposed in our previous study (Phys. Rev. B66, 115403, 2002). In present study, we compared our kinetic model with experimental data for the case of reaction between Sn6Pb60 and Cu. First, a systematic study of intermetallic compound morphology was performed, because morphology of intermetallic compounds provides kinetic path of the ripening. We observed a transition from anisotropic to isotropic morphology of Cu6Sn5 intermetallic compound, according to composition of solder. When Sn6Pb solder composition was about Sn40Pb60 to Sn60Pb40, Cu6Sn5 intermetallic compounds showed isotropic morphology, while partly anisotropic at other compositions. When the solder was pure tin, all the Cu6Sn5 showed nanotwinned morphology. Size distribution of intermetallic compound scallops showed very good agreement with our theory. Growth rate of scallops also followed our prediction, which was r~t2/3.

2:30 PM B10.4
Development of C-ring Technique for Studying Effect of Stress on Growth of Interfacial Intermetallic Compounds. Wei Zhou1, S. L. Nho1, H. L. Schaefer2; 1Materials Science and Engineering, University of California, Los Angeles, Los Angeles, California; 2Mechanical and Production Engineering, Nanyang Technological University, Singapore, Singapore.

Reliability of solder joint interconnects is a most critical issue in electronic packaging. There is the urgent need to understand reliability of lead-free solder joints because lead-free solders are replacing the conventional tin-lead solders due to legislation to ban lead usage in electronic products. In soldering process, formation of thin intermetallic compounds due to reaction between the solder and substrate is essential to achieve a good metallurgical bond. However, excessive intermetallic growth in service would lead to premature failure of the joint. Stress is known to influence growth of intermetallic compounds, but existing experimental work is not able to study effect of stress on the intermetallic growth in a controlled manner. Therefore, we developed a novel technique to make it easy to carry out a quantitative study of the stress effect on intermetallic compounds. We machined copper substrate into an open ring in the shape of letter C, drilled two holes in the lower and upper ends of the C-ring and used a bolt to tighten the C-ring. When the C-ring is tightened, its diameter is reduced, so the tensile stress on the outer surface and compressive stress on the inner surface can be calculated quantitatively from the amount of reduction in diameter. We coated the C-ring with Cu6Sn5-3.8Ag-0.7Cu lead-free solder, tightened the ring to apply stress to the solder-substrate interface, and used the stressed C-rings for isothermal annealing at various temperatures. We demonstrated that the specially designed specimens provide consistent and reliable results for studying effect of in-plane stress on intermetallic formation at the interfaces. It is interesting to note that compared to the results in significantly faster interfacial intermetallic growth than tensile stress.
The drop impact induced solder joint fracture has become one of the critical system failure modes of interest in the electronics industry due to the migration of market focus to portable applications. For example, cellular phones might be broken due to impact by dropping. To evaluate the impact resistance between BGA ball and UBM pad metallization (UBM) pad, industry widely uses shear test and pull test. Unfortunately, these tests are not suitable to evaluate the impact reliability of solder joints, because the testing speed is typically lower than 1 mm/s, well below the velocity of impact applied to solder joints by dropping. Some previous study by Chiu et. al. proved there is a very strong correlation between drop reliability and voiding at the UBM/solder interface. However, ball shear testing does not correlate to drop test performance, and ball pull strength is not a good indicator of shock reliability either. Therefore, how to characterize the impact reliability induced by dropping becomes very crucial. Recently, the research group from Hitachi Metals, Ltd., Japan proposed a miniature impact test for solder bumps by adopting the principle of the classic Charpy impact test. Based on their work, we have designed a micro-impact testing machine to quantitatively study the bonding strength between BGA ball and UBM pad. The sample is placed in the impactor with adjustable positive position parameter of the hammer and its final position after impact is recorded by an angle encoder with accuracy of ±0.5 degree. Since the measured angle difference in a typical impact test is about 10 degree, the resolution is about 5 to 10% of the measured energy change. Lead-free solder balls are used in this study with 760μm size. The UBM structure is deposited Au/Ni/Cu metallization. Scanning electron microscopy is employed to study the fractured surface of the solder joints. In the study, we observed a ductile-to-brittle fracture on the impacted area, due to interfacial intermetallic compound formation caused by aging. The effect of solder composition, aging temperature and time on the ductile-to-brittle transition will be further discussed. The distribution of fracture toughness of area array of solder bumps on 3cm×3cm square substrate will be reported.

3:15 PM B10.6
A New Approach for Predicting the Onset of Disbands in Flip-Chip Assemblies. Ray Pearson and Brian J. McAdams; Materials Sci. & Eng., Lehigh University, Bethlehem, Pennsylvania.

Reliability studies on flip-chip assemblies point to the need for a study of the initiation of interfacial disbands. A standard method for evaluating the propensity of disband formation does not formally exist. Therefore, we propose the use of a stress singularly approach to this problem. The approach uses a fracturing mechanics-like picture parameter, the critical stress intensity factor for the stress singularity, to serve as a criterion for the onset of delamination. Testing of this kind requires no measurement of pre-existing flaws, only that the geometry has a stress singularity that induces disbands. Commercial flip-chip packages contain a variety of stress singularities of varying strengths that can promote disbands. For our purpose, a simple geometry utilizing a butt tensile joint is employed to examine the effect of free-edge and free-corner singularities on the initiation of disbands. This approach is used to study disband initiation under monotonic and cyclic loading conditions. Interestingly, a strong correlation is found between disband initiation and disband propagation. Moreover, the ranking of the stress intensity factor among the different geometries is consistent with the values predicted by the fracture mechanics.

3:45 PM B10.7
Low Temperature Ultra-Thin Titanium-Based Wafer Bonding. Jian Yu1, Yimin Wang2, Hassa Bakhrui1, Jian-Qiang Lu1 and Ronald J. Gutmann1, 1Rensselaer Polytechnic Institute, Troy, New York; 2Lawrence Livermore National Laboratory, Livermore, California; 3University of Albany-SUNY, Albany, New York.

Three-dimensional (3D) wafer-scale integration is receiving increased attention with various bonding approaches, including oxide-to-oxide, dielectric adhesive and copper-to-copper. In this study, an alternative metal-based wafer bonding using an ultra-thin titanium (Ti) coating was investigated. An oxidized silicon wafer was successfully bonded with a prime silicon wafer at low temperature (400°C) with 30 nm sputtered Ti as adhesive. The bonded pairs evaluated with scanning acoustic microscopy (SAM) and a series of mechanical integrity tests including 200 μm diameter wafer probed with a pin and 10% of the measured energy change. Lead-free solder balls are used to protect the devices from fracture. The elastic substrate exposed between the islands, with and with the metal interconnects, accommodate most of the stretching deformation. At a high fill factor by subtract island, the stretching deformation of the metal interconnects becomes very large. Oxide-based substrates have been used to make highly and reversibly stretchable interconnects at high pitch. Because of their susceptibility to organic solvents, elastomeric substrates must be processed very differently from silicon-integrated circuits. Here we describe the steps we have taken so far to develop patterning techniques for the interconnect metal. Absent from any process technology, we started out by using shadow masks, which resulted in interconnects with a smallest width of 200 micrometers. Rasion patternable dry resist brought the width down to 100 μm. After
developing a modified photoresist process that does not require the use of organic solvents, we now have obtained 2-um wide conductors. We will just describe this patterning process. Then we will show the electrical, structural, and mechanical evaluation of the interconnects, relaxed, during mechanical cycling, and under large mechanical strain. This research is supported by the Packard Foundation, DARPA, and NSF.

4:30 PM B10.10

Wafer-to-wafer or chip-to-chip stacking is one of the key enablers for three-dimensional (3-D) integrated circuits; heterogeneous integration of devices and advanced packaging applications. The advantages of this approach include performance improvements due to decrease of the interconnect delays, integration advantages from the opportunity of integrating divergent process flows, and reduced form factors arising from geometrical advantages of 3-D wafer (or chip) stacking. Wafer bonding (or die bonding) utilizing high-density interconnections between the two wafers is one the key steps in the overall process flow to fabricate such 3-D structures. Voids in bonded interfaces can create severe problems during further processing of such stacked wafers beside yield loss. In this paper, we discuss and benchmark different metrology techniques to analyze and quantify the quality of bonded interfaces. Acoustic microscopy (CSAM) is used to investigate interconnections between bonded wafers at high resolution. The imaging resolution is shown to critically depend on the wafer thickness through which the acoustic waves have to traverse to form the images. We present detailed theoretical analysis which shows the effect of lens aberrations on the image formation and the corresponding resolution degradation. We have also performed detailed thermal microscopy to characterize the bonded interfaces: voided regions can be imaged as localized hot spots. The temperature rise at the hot spot is shown to be primarily dependent on the defect depth and size. We show examples on how the thermal imaging can be used as a complementary metrology technique to acoustic microscopy to inspect the buried interfaces. Infra-red imaging, besides being used to analyze wafer-to-wafer alignment accuracy can also be used to investigate the quality of bonded interfaces. The void size can be calculated from the number of interference fringes arising due to the voids; however the metalization in the wafers can minimize the contrast due to the defect. We discuss both experimental results and theoretical studies of each of these different techniques to analyze buried interfaces and discuss their relative capabilities for inspection of advanced interconnect and packaging architectures.

4:45 PM B10.11

As materials, structures and phenomena continue to shrink, and the micro/nanofabrication paradigms move from planar to 3-D/stacked platforms, there is an acute need to image and analyze surface/sub-surface features and phenomena at ultra-high resolution and sensitivity, coupled with usual ergonomic/economic considerations. Keeping view of these technological challenges and to overcome those, we have developed a turn-key Near-Field Acoustic Holography (NFAH) system. This unique system will address emerging issues in imaging and analysis of diverse embedded nano and microscale structures, and engineered systems. In NFAH, one high frequency acoustic wave is launched from below the specimen, and another one on the cantilever of the scanning probe microscopy (SPM) system, albeit at a slightly different frequency. The resultant beat frequency which forms as a pseudo-standing wave on the specimen surface, acts as a reference lattice. Any perturbation to phase and amplitude of the specimen acoustic wave is then measured with SPM tip as an antenna, and converted in a quantitative pictorial map. Thus, internal features, e.g., voids, cracks, phases, which perturb the acoustic wave, can be seen in such images. This technique will fill a critical void in characterization and investigation of the static and dynamic mechanics of nanoscale systems, ranging from engineering systems to biologically active structures, in-vitro. In the presentation, we will report efficacy of NFAH approach, starting with a model subsurface microstructure of buried Au nanoparticles/prisms underneath a polymer film. These embedded features are readily imaged with NFAH providing proof-of-concept of this novel approach. Additional results on practical systems will be presented, such as high resolution sub-surface imaging of copper vias (without doing any cross-sectioning), metal semiconductor composite structures, low-k dielectrics, and internal features of carbon nanotubes, molecules, stress migration in MEMS devices and 3D Interconnects among others. It will be argued that ramping the acoustic frequency to 100 MHz would enable the extraction of subsurface defects (voids, delamination) with spatial resolution < 5 nm.